LArPix & LightPix

Scalable, cryogenic-compatible pixelated readout for noble liquid detectors

Brooke Russell on behalf of the LArPix and LightPix Teams

XIII Front-End Electronics Workshop
May 22, 2026

Outline

I. LArPix
   - DUNE NDLAr Implementation
   - Prospective DUNE Far Detector

II. LightPix
   - Scale-able cryo-compatible SiPM readout

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I. **LArPix**
   - **DUNE NDLAr Implementation**
   - **Prospective DUNE Far Detector**

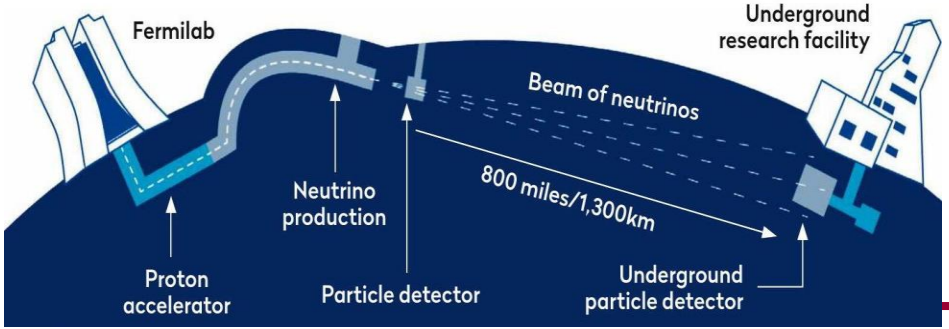
II. LightPix
   - Scale-able cryo-compatible SiPM readout

Deep Underground Neutrino Experiment (DUNE)

1.2 MW (upgradeable to 2.4 MW) LBNF (anti-)neutrino beam

LArTPC charge signal:

- inherently *slow & sparse*
- millimeter-scale charged particle tracking
- O(100) keV charge signal threshold



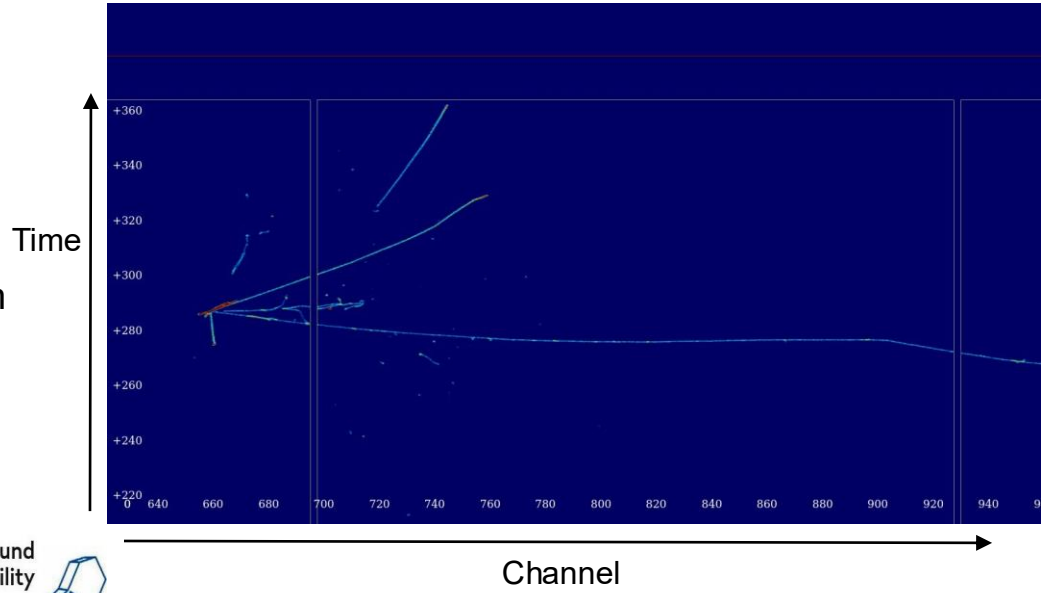
DUNE Far Detectors 1 & 2

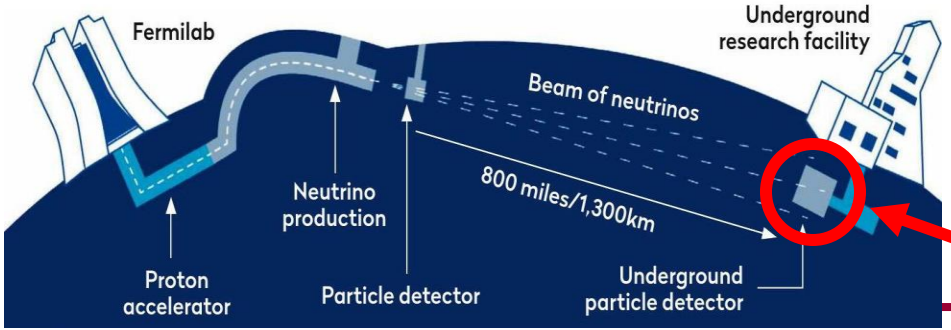
Wire and strip continuous readout with in-situ cryogenic readout electronics

- **LArASIC** front-end amplifier

  ==> See next talk on **CHARMS** by P. Mukim

- **ColdADC** digitization
- **COLDATA** manage data & fast commands-





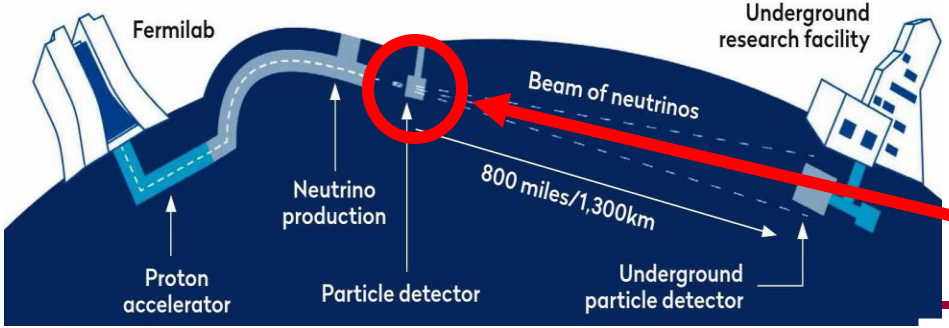
DUNE FD will collect ~30 neutrino interactions per week

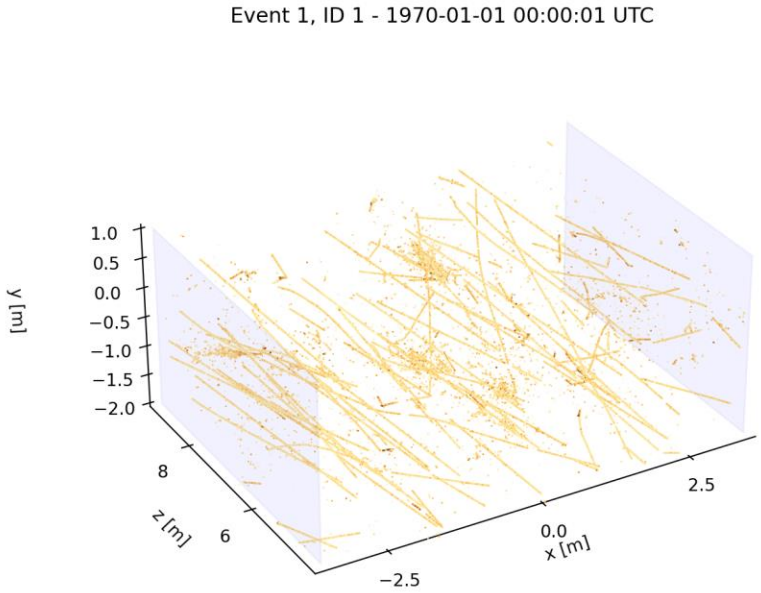
DUNE LAr Near Detector

Anticipate O(100) interactions per 10μs beam spill

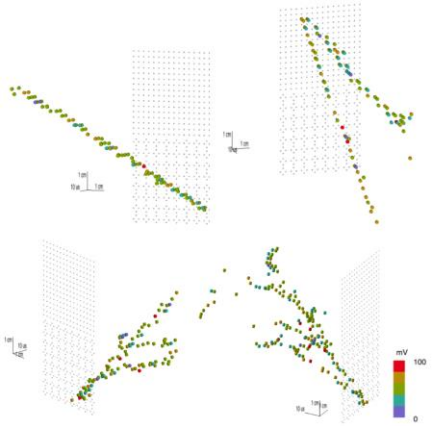
70 optically-segmented LArTPCs with pixelated readout charge sensing in NDLAr

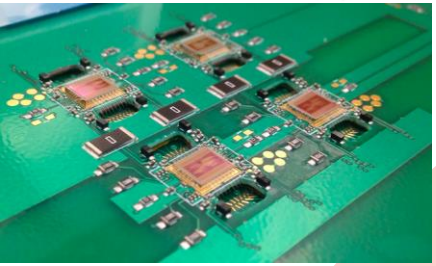
- 200 m^2 active anode area
- 224k LArPix ASICs
  - 14.3M channels at 3.7 mm pixel pitch





DUNE ND will collect ~1.5 million neutrino interactions per week





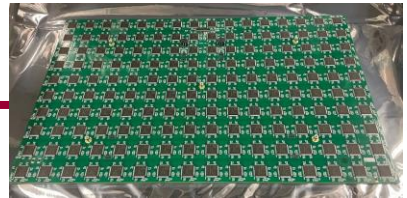
LArPix Evolution

LArPix-v1, 2016-2018

- 32 channel inputs
- 275 e- ENC @ 87K
- O(10^3) channel readout via 2 wires demonstrated technical feasibility

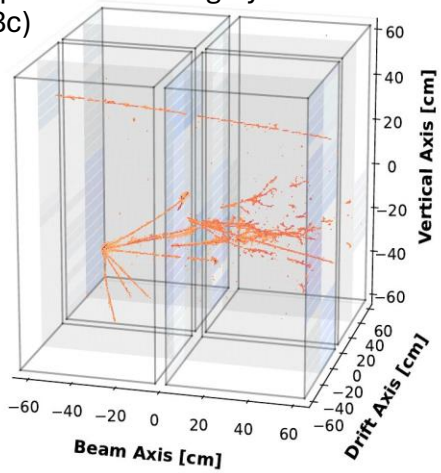
LArPix-v2, 2019-2024

- 64 channel inputs
- 800 e- ENC @ 87K
- >10k digital multiplexing
- O(10^5) channel prototypes demonstrated industry-produced, scalable system architecture



LArPix-v3, 2025-

- 350 e- ENC @ 87K
- Differential, asynchronous 10-bit ADC (v3a)
- Differential buffer (v3c)
- Improved data integrity (v3c)



LArPix-v3 ASIC Overview

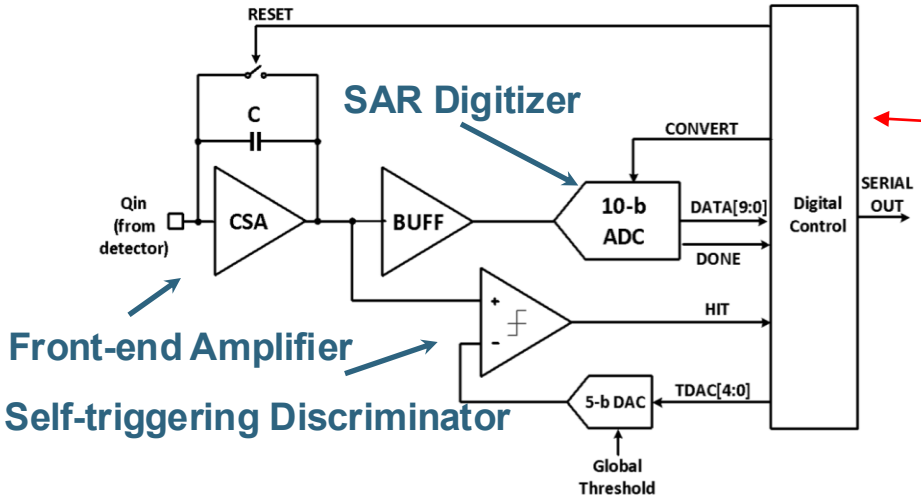
Cryo-compatible, low-power mixed-signal ASIC (TSMC 130 nm) designed for pixelated, true 3D readout of LArTPC detectors

Continuous self-triggered pixelated free streaming readout, ~100% uptime

Principal component of the end-to-end LArPix readout system: \$0.10/channel (\$10k/m^2)

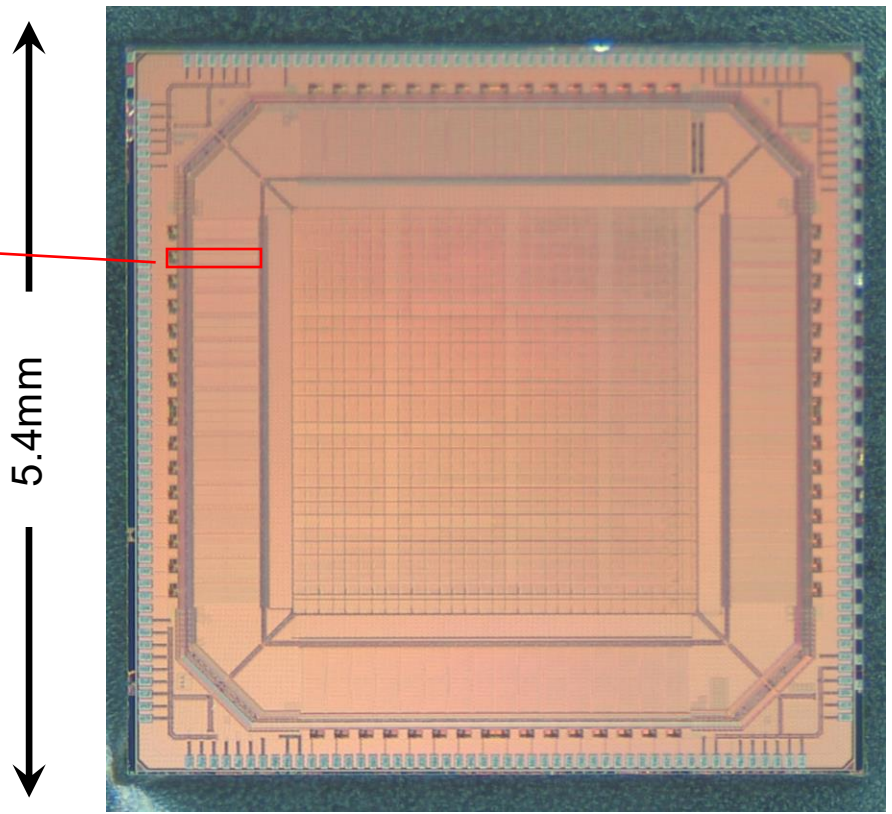
Specification	Value
Analog Inputs	64
Gain	3.4 μV/e-
Noise	350 ENC
Power	<170 μW/channel
Dynamic Range	340 ke-
AFE Settling Time	<200 ns
Minimum Resampling Time	1.4 μs
Timestamp Precision	100 ns
Linearity	0.9%
ADC Resolution	10 bits
Operating Temperature	77 K to 300 K

LArPix Analog Front-End

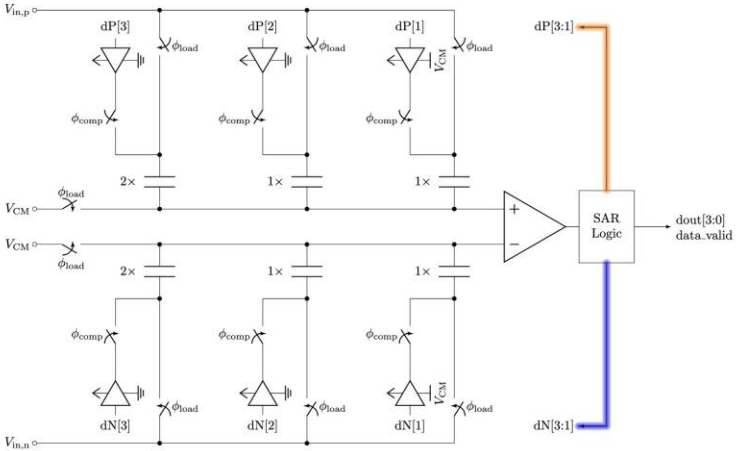


Charge sensing: per-pixel integrating amplifier with self-triggered digitization and readout

64-channel SoC, in 130nm

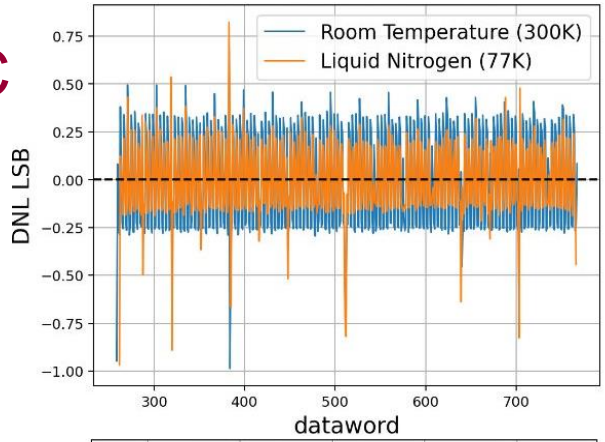


Asynchronous 10-bit SAR ADC

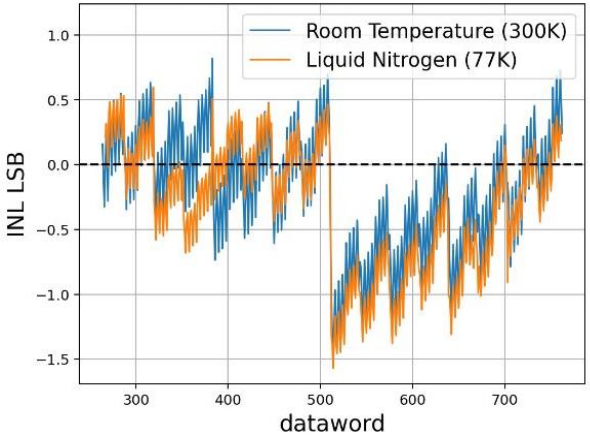


Design and implementation by Panos Zarkos (LBNL)

- Differential design with bi-directional switching, reduces area and power
- Asynchronous logic: internally-generated clock speeds ADC conversion



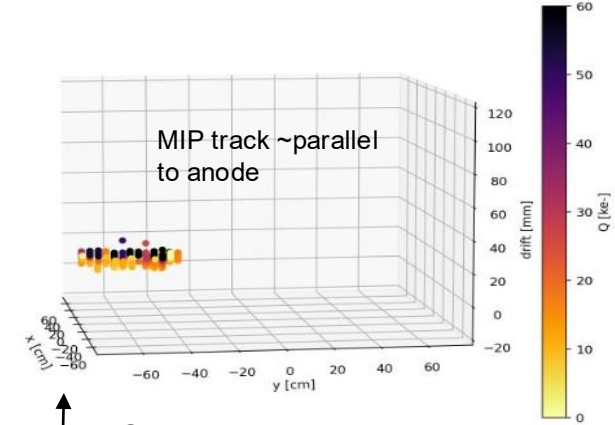
DNL <1 LSB



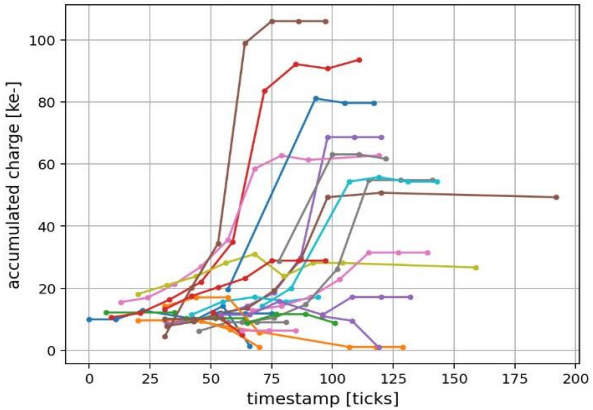
INL <1.6 LSB
(512 is a missing code attributed to a layout artifact)

Triggering Schemes

- Self-trigger reset (nominal operating mode): digitize and drain charge after threshold crossed
- Cross-trigger reset: digitize and drain sub-threshold charge based on self-trigger of another pixel
- External-trigger reset: digitize and drain sub-threshold charge based on external signal
- Periodic-trigger reset: periodically digitize and drain sub-threshold charge at fixed cadence on a channel rolling or chip-synchronous basis
- Optional burst modes
    - Fixed burst: process N hit cycles for each self-trigger
    - ADC threshold: continue to process hit cycle until an ADC dataword ceiling (or floor) is exceeded
    - ADC settle: continue to process hit cycles until change in ADC value is below set value

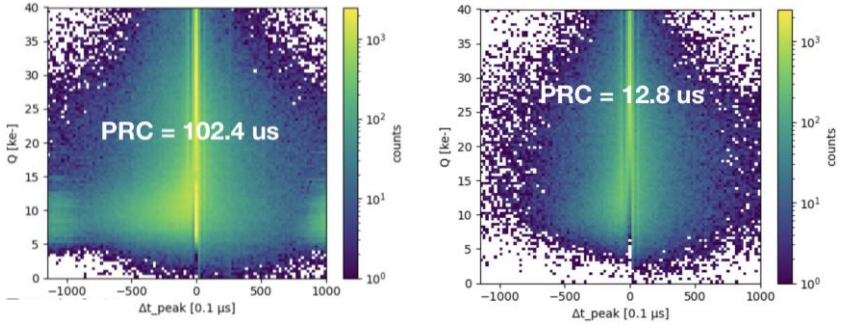


ADC settle triggering scheme

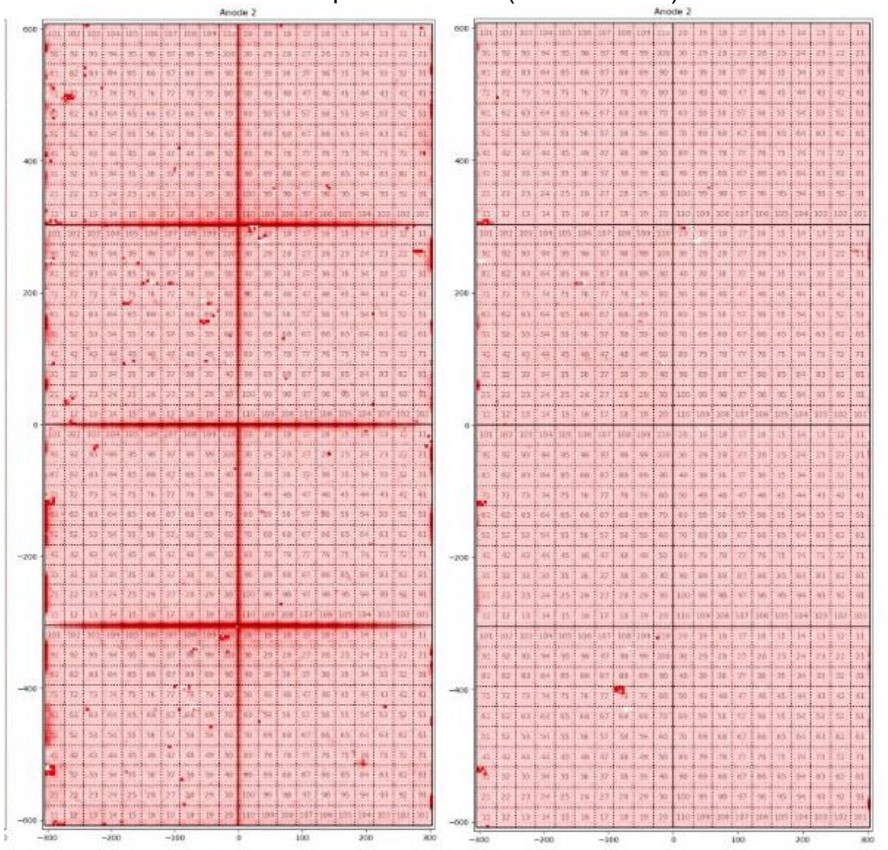


Reset Schemes

- Front-end periodic reset at a configurable cadence on a channel rolling or chip-synchronous basis
  - Highly effective in mitigating detector environment noise
    - Microphonics
    - Cryocooler power cycling
  - Long-range induction mitigation
- 100 ns AFE deadtime incurred with each reset



Pixel pedestal RMS (50k channels)

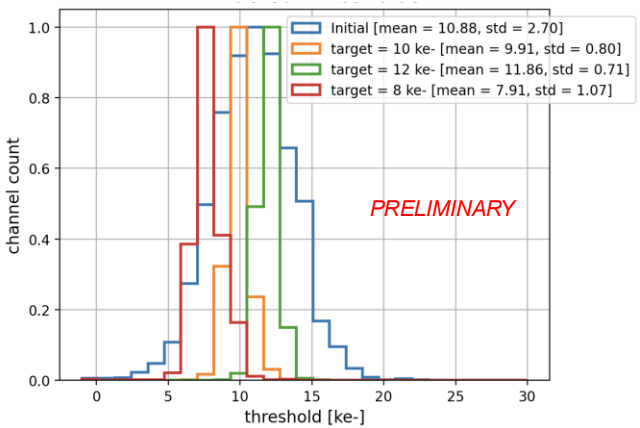


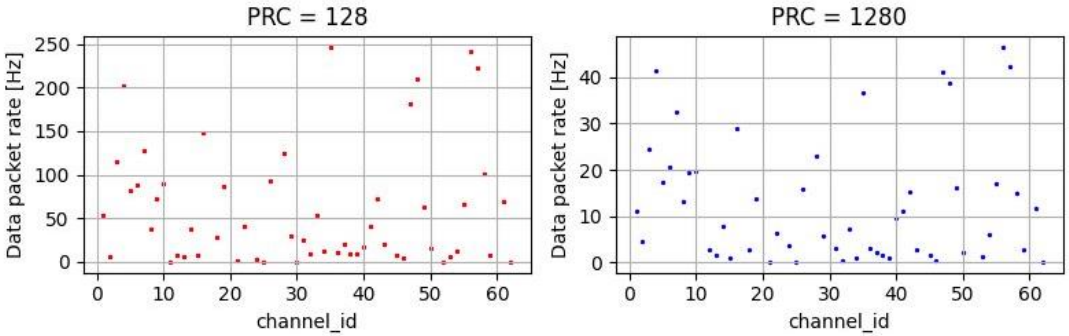
Reset at 2.4 Hz

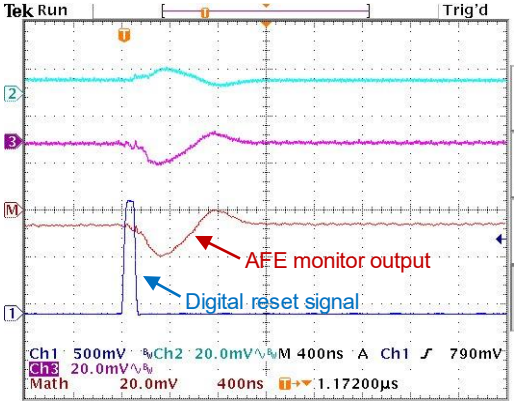
Reset at 2.4 kHz

Operating Thresholds

- Channel thresholds are highly configurable
  - Ability to dynamically set/change thresholds during operation
- Investigating channel reset-induced pickup
  - Results in spurious triggers at ~3000 e- threshold level



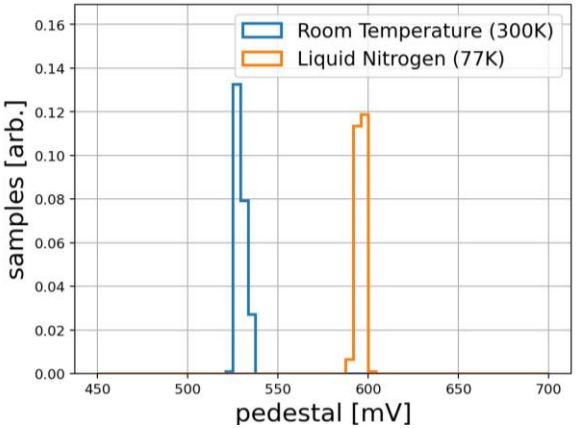


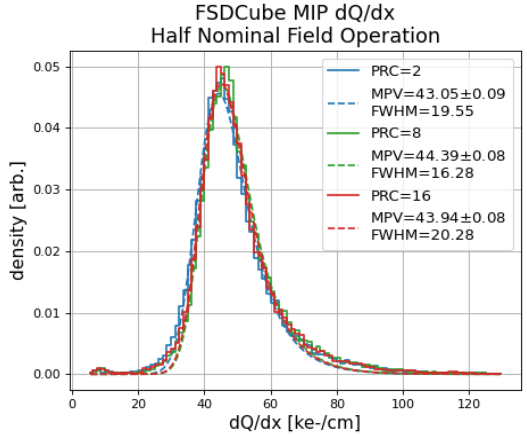


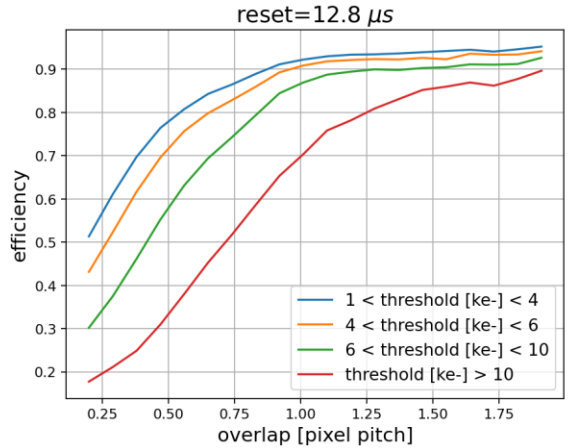
Analog Front-End

Key design changes:
- Super source follower front-end buffer
- Asynchronous 10-bit SAR ADC
- Correlated-double sampling

Performance benchmarked in small-scale LArTPC

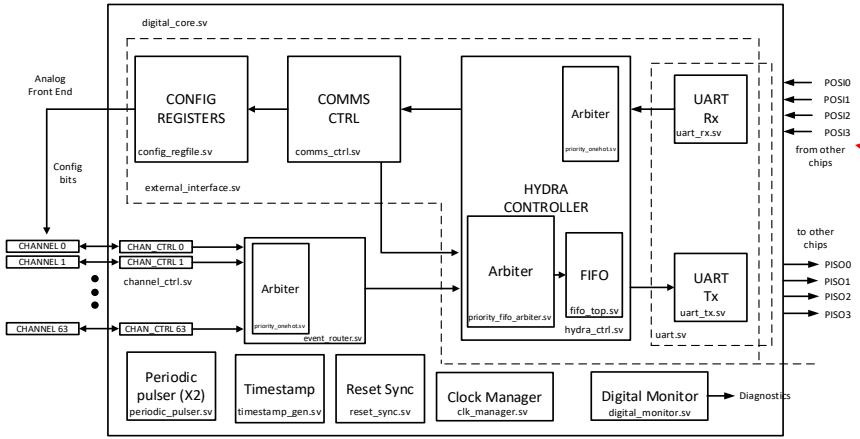






Known bug in management of memory buffer causes few percent data loss

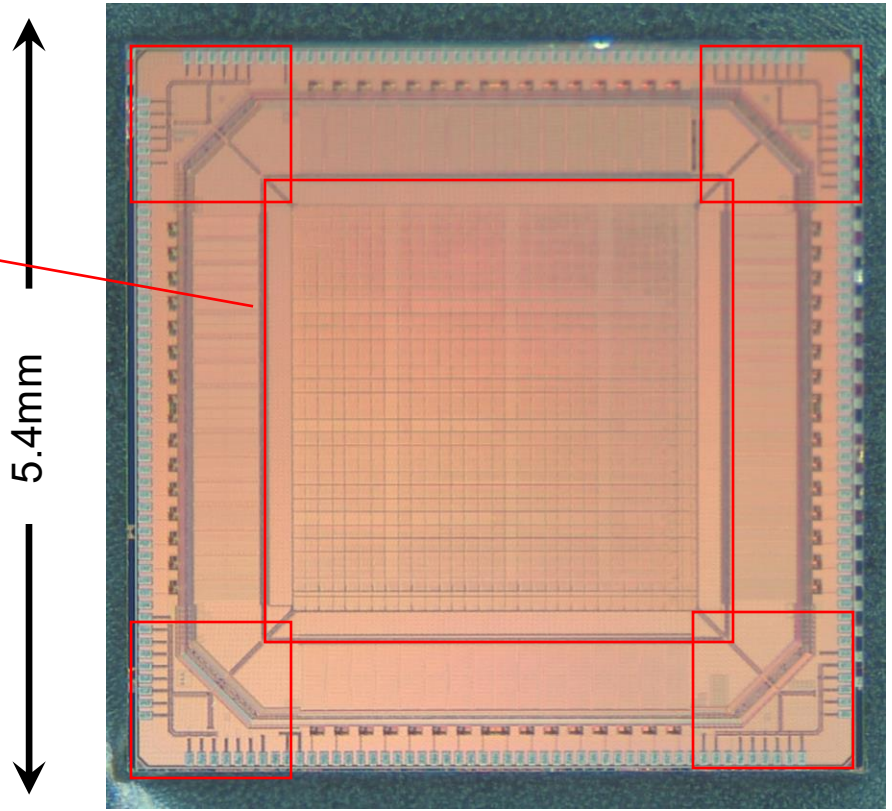
LArPix Digital Back-End



Digital control: data aggregation, amplifier configuration, inter-chip communication

Data transmitted on every rising clock edge (10 Mbit at 10 MHz CLK)

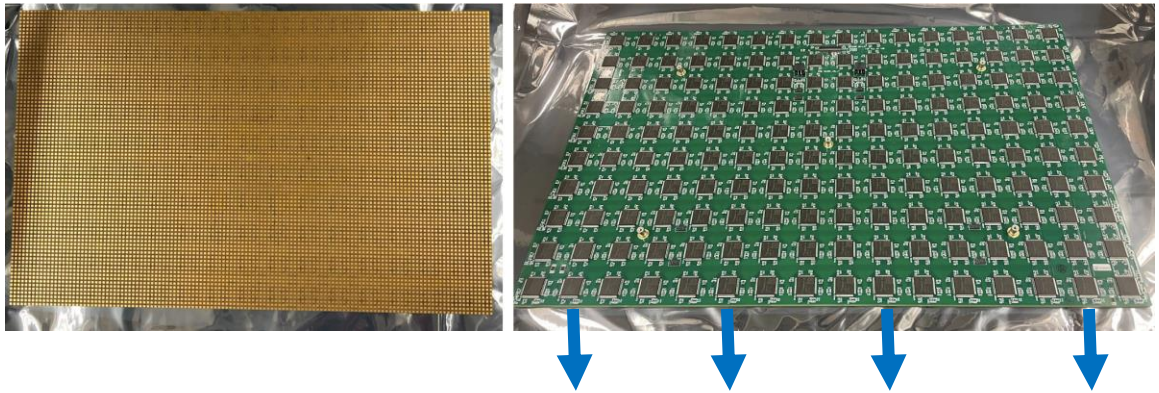
64-channel SoC, in 130nm

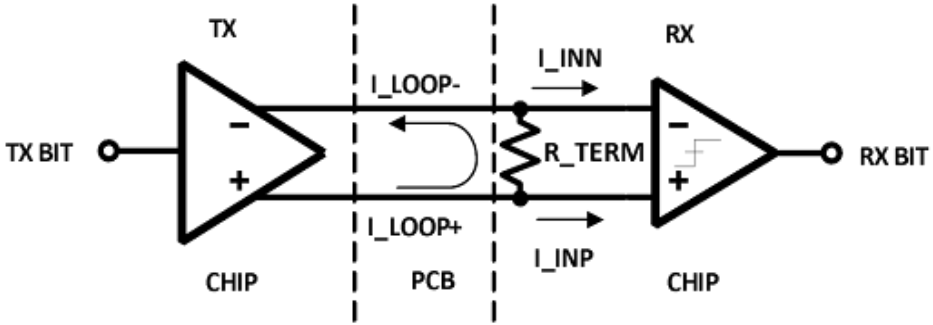


Digital I/O

Custom tunable low-voltage digital transmitter and receiver

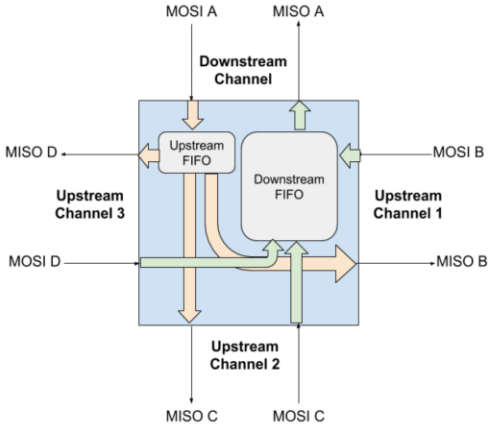
- Similar to LVDS in concept, but much lower power: O(10 μW) per transmitter & receiver
- Highly-tunable loop current and termination resistance supports multiple modes of operation (chip-to-chip, chip-to-controller)
- Optional mode for automatic transmitter power-down when no data



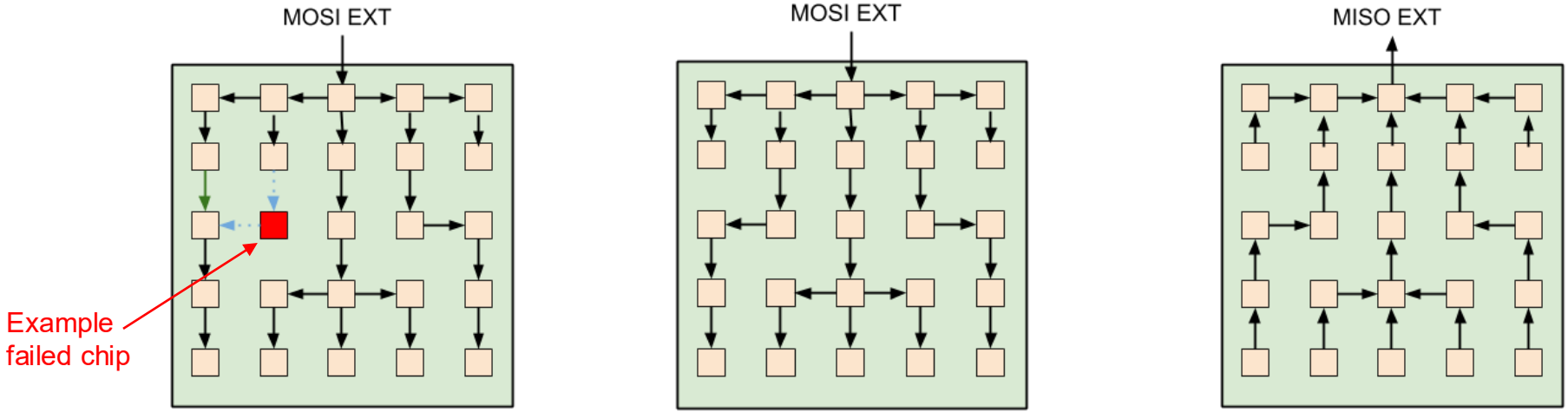


Hydra I/O

- Each ASIC capable of configurable I/O in any cardinal direction
- I/O can occur between any neighboring chips on pixel tile
- ASIC network constructed by explicit configurable connection between neighboring ASICs in a determined fashion



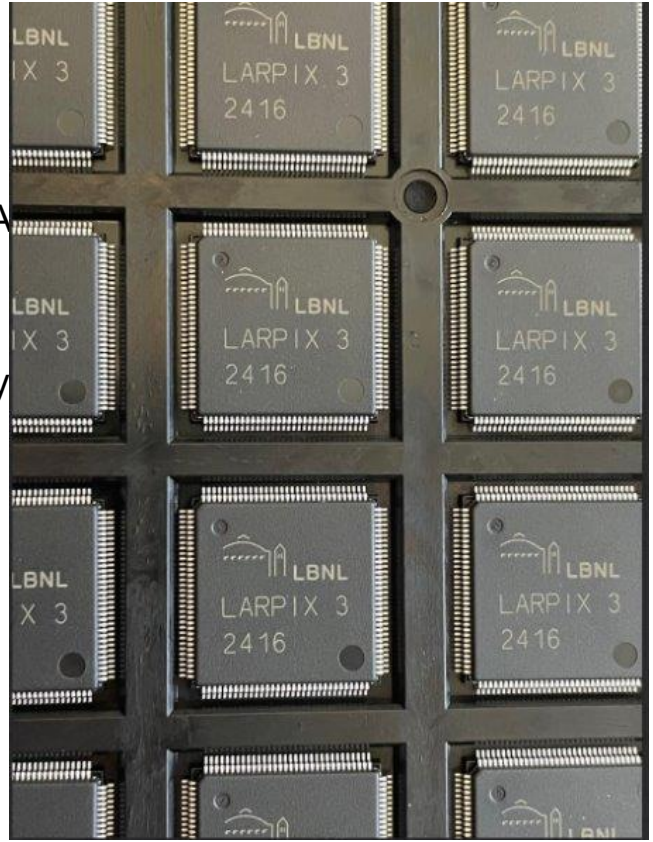
Example 5x5 pixel tile network



Power

Power dissipation is reduced with:

- Low voltage supplies (VDDA 2.2 V, VDDD 1.2 V)
- Low data rates
  - Channel power is lowered by avoiding digitization and readout of mostly quiescent data
- Minimizing the number of active components in the cryogenic environment



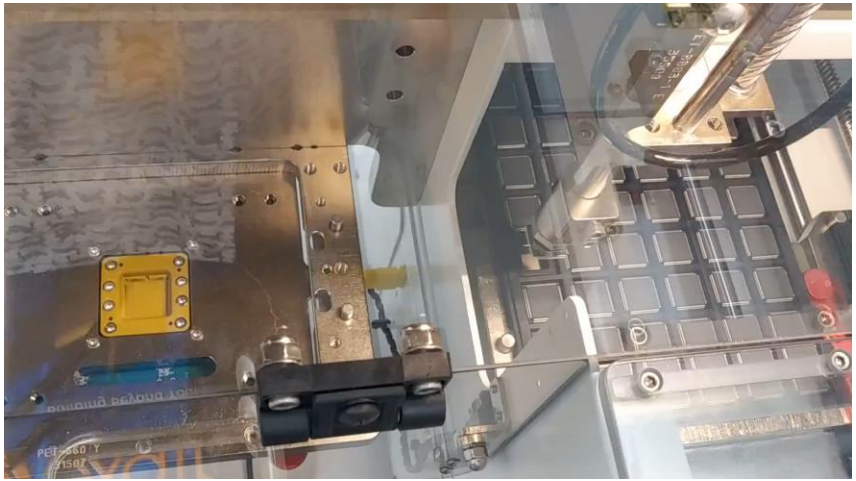
Use a standard TQFP128-EP package ==> ground pad serves as a heat sink to aid thermalization and mitigate localized heat density

ASIC Yield

6457 LArPix-v3 ASICs screening:

- 94.7% good
- 2.6% fail due to high noise/leakage
- 2.7% fail due to I/O fail (includes DOA)
- <<1% fail due to bit flips

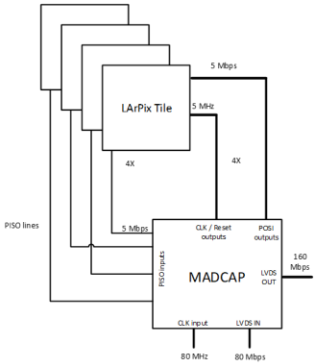
900 chips/day testing throughput with 1 robot

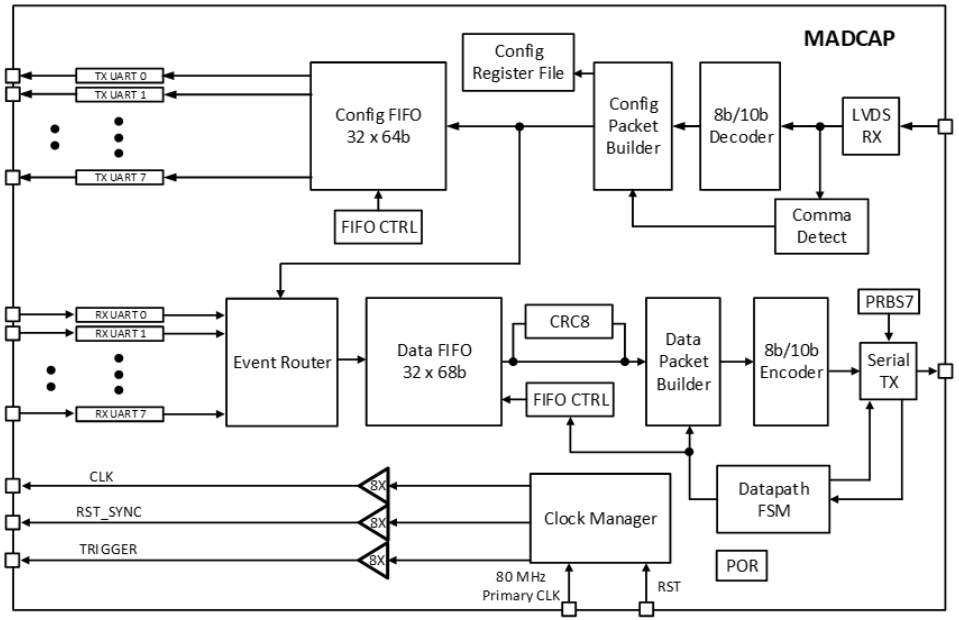


Robotic chip testing @ Caltech

Prospective DUNE Far Detector

- To reach O(10^8) pixel system scale, need to reduce the number of cables/feedthroughs
  - Aggregate data I/O from multiple pixels to reach O(10^5) pixels per data channel
- MADCAP (multiplexer ASIC for data and clock aggregation) in development as a cryo-compatible digital multiplexer
  - 130 nm TSCM MPW tapeout next month





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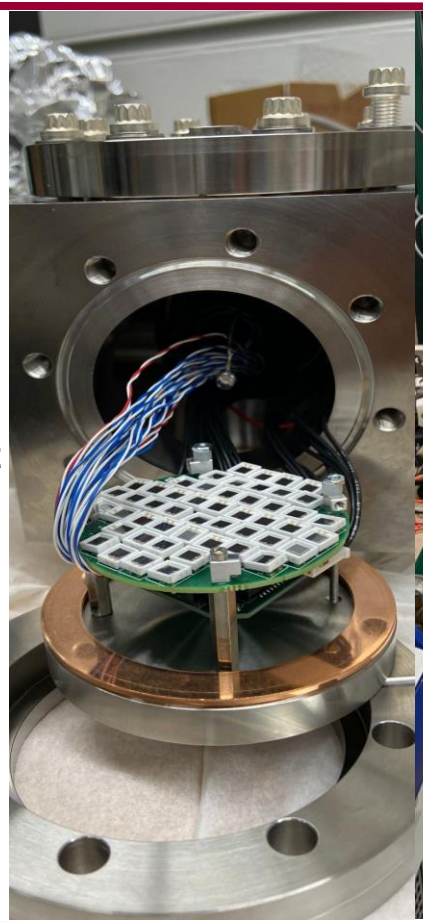
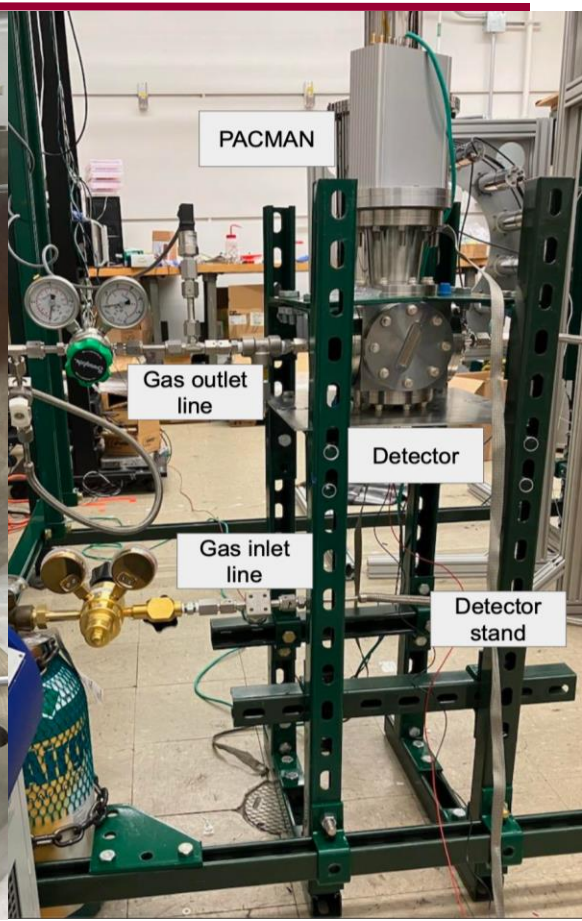
   - **Scale-able cryo-compatible SiPM readout**





LightPix-v1 readout system for GHe applications at UC Berkeley: 50x 3 mm by 3 mm VUV SiPMs with single cable power, I/O

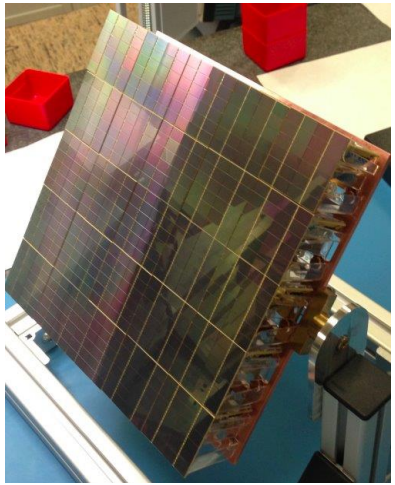
Motivation

Traditional tradeoff for SiPM-based applications requiring high photocoverage: sacrifice spatial resolution for collection efficiency

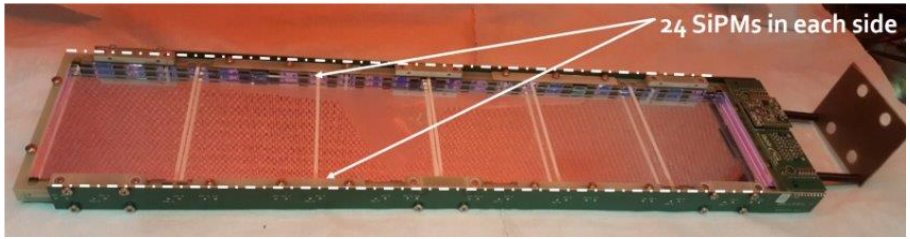
Design considerations driving multiplexing requirements:

- Cost
- Power dissipation

Technical need for scalabe (high collection efficiency, high channel count), low-power SiPM readout **without ganging** signals and operating 77 K to 300 K

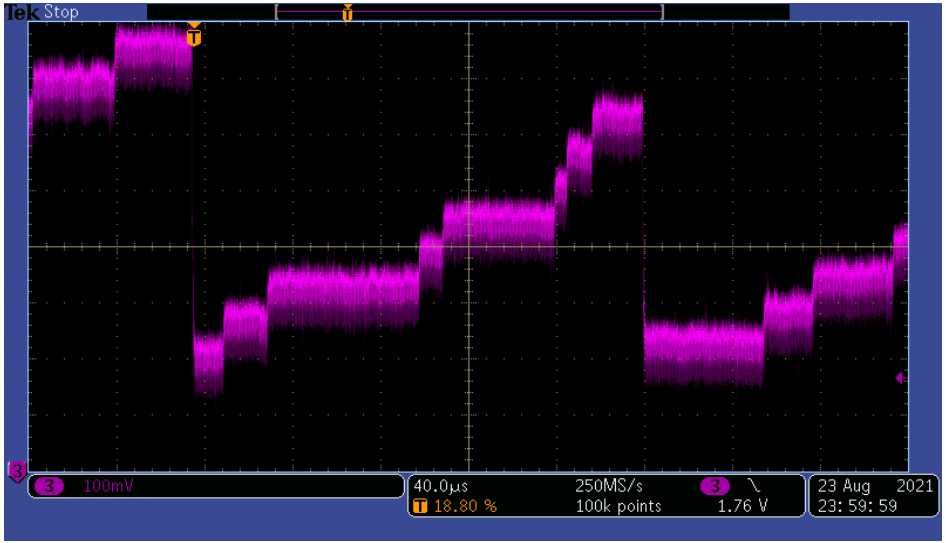


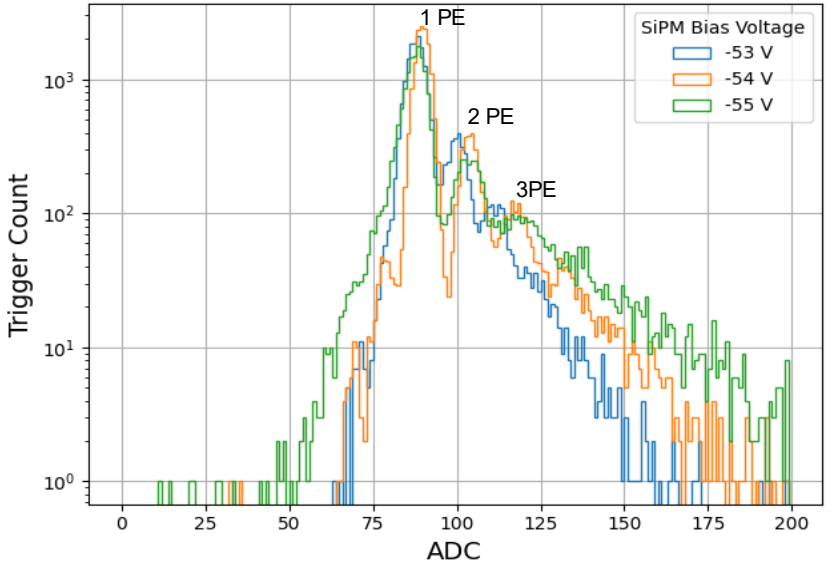
Example of direct SiPM detector format from DarkSide-20k prototype



Example of large area light trap with X-ARAPUCA

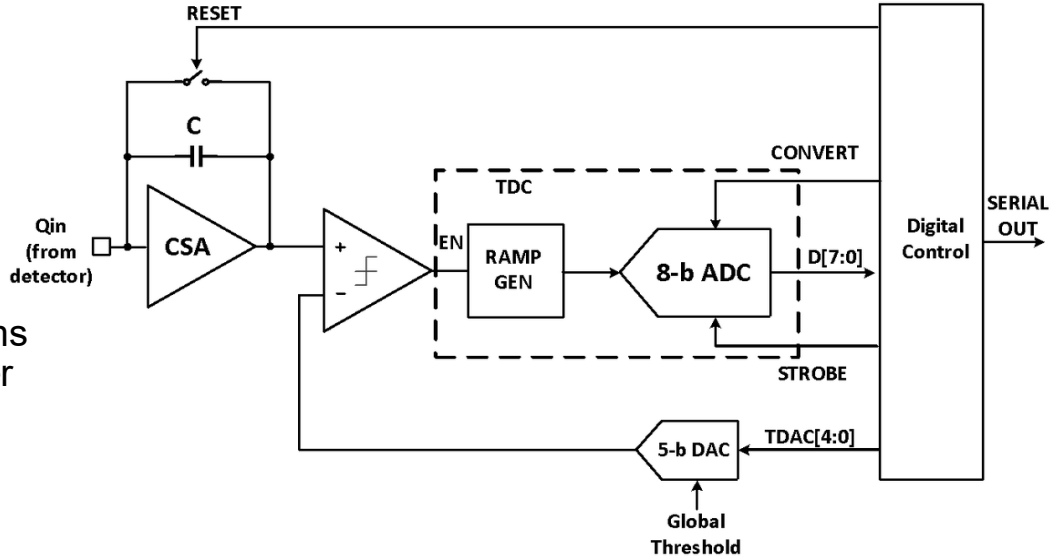
SiPM Dark Counts on LArPix-v2 AFE

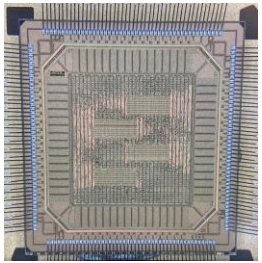




LightPix-v1

- Unique channel input for each SiPM
- A single photoelectron discriminator with a TDC for fine-timing
- Designed for very-high-channel-count systems with low occupancy, where the typical number of photons per channel is less than one
  - Calorimetry and pulse-shape discrimination achieved through the aggregate distribution of photon arrival times across many SiPMs
- "LightPix-mode": tuneable multi-channel coincidence triggering mode to suppress excess data from dark noise
  - 1-64 channels over threshold in 100 ns to 13 μs window

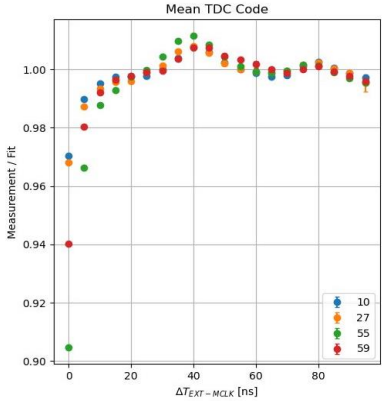


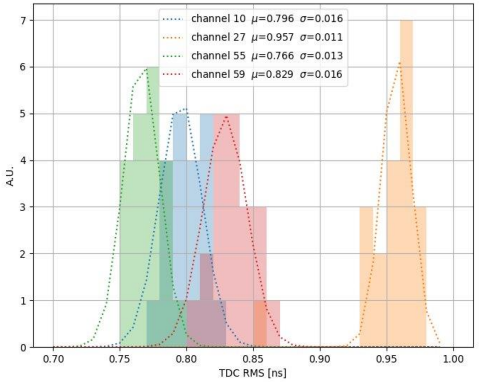


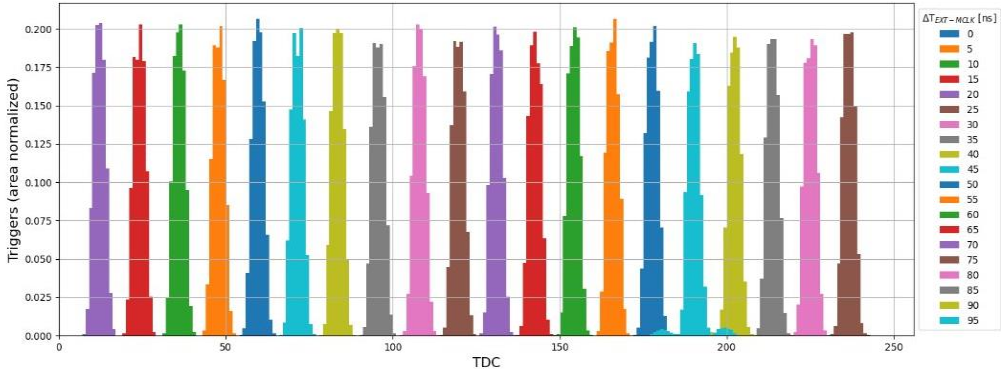
LightPix-v1 produced in 180 nm TSCM

LightPix-v1 Performance

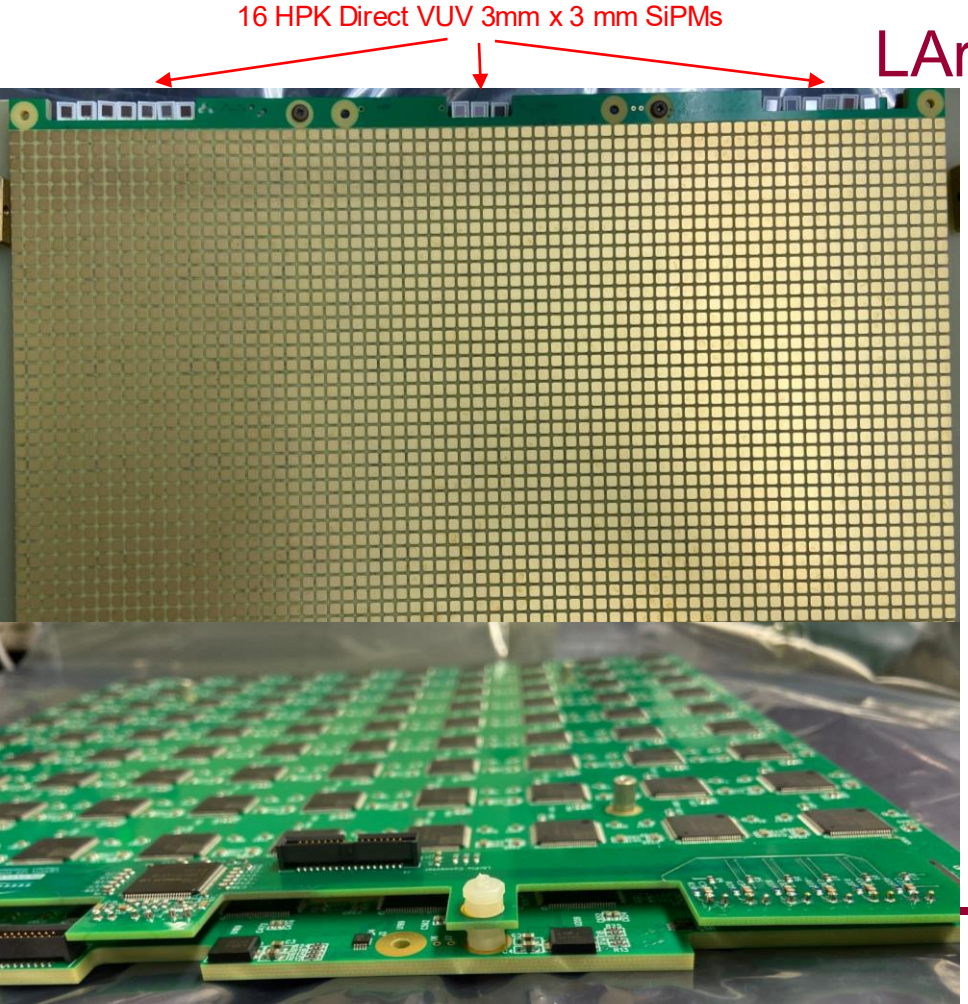
- TDC evaluation for O(1) PE inputs:
  - TDC linear to <10% within 10 ns of ramp generator start
  - < 1 ns jitter
  - < 2 ns time-walk bias
  - <1 ns RMS global timing accuracy
- Dark count suppression logic validated







LArPix-LightPix Dual TPC Readout



- Proof of concept for joint charge/light readout with direct VUV light detection in LArTPC
- SiPM PCB attaches directly to LArPix anode tile
- Single PACMAN controller, two shared data/power cables

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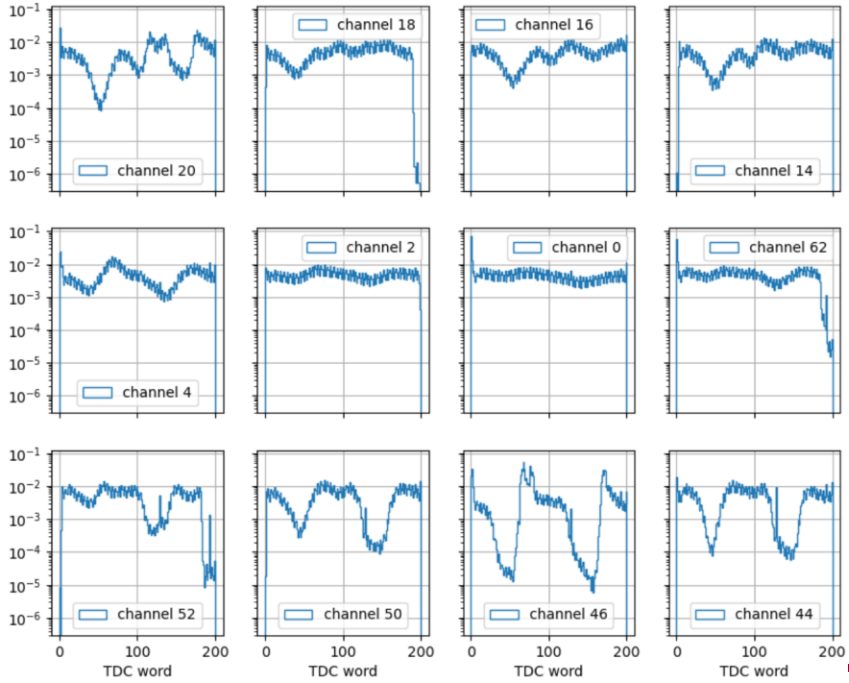
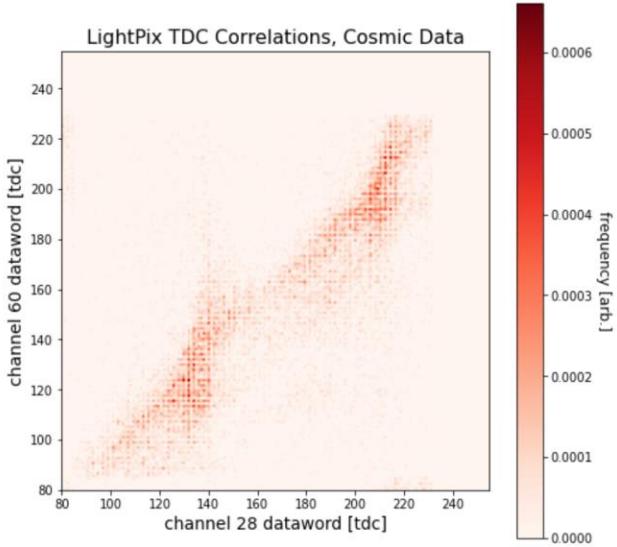
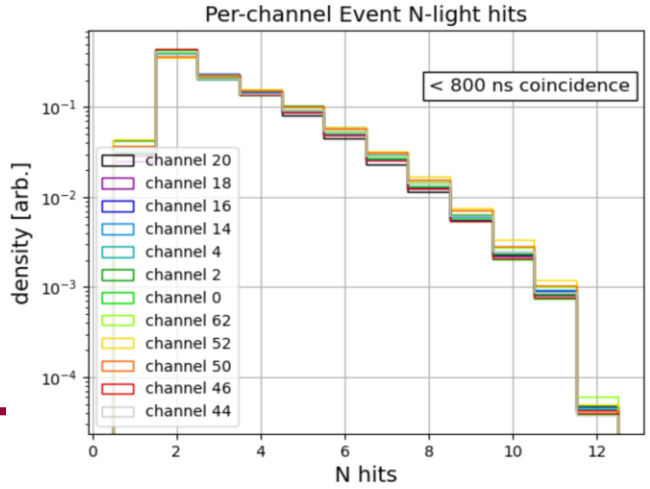
LightPix TPC Performance



Issue: significant cross-talk from LArPix-v2a single-ended I/O

Per-event timing correlations slewed by pickup from single-ended clock & digital I/O

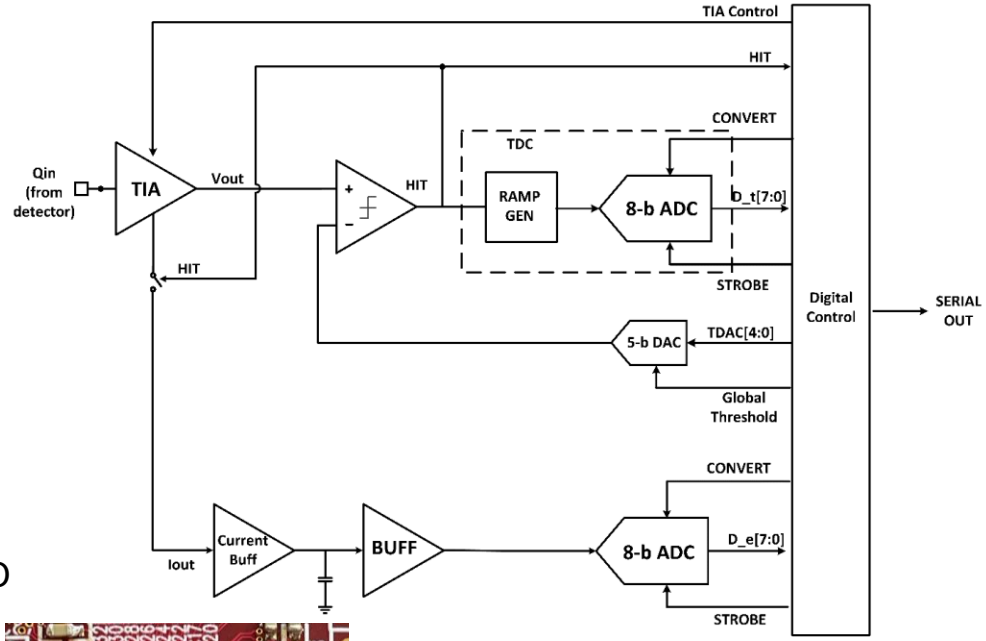


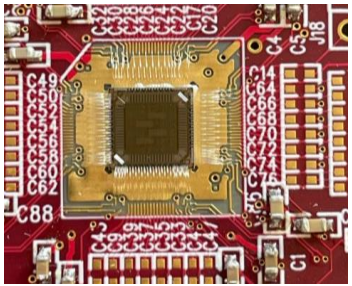


LightPix-v3

Design changes relative to version 1:

- Replaced CSA with TIA optimized for larger SiPM capacitance (6 mm x 6 mm or larger)
- Added ADC in parallel with TDC for use in higher-occupancy detectors
- Fully differential, low-swing clock and digital I/O
- 32 "super channels" with sub-ns timing +multi-PE calorimetry

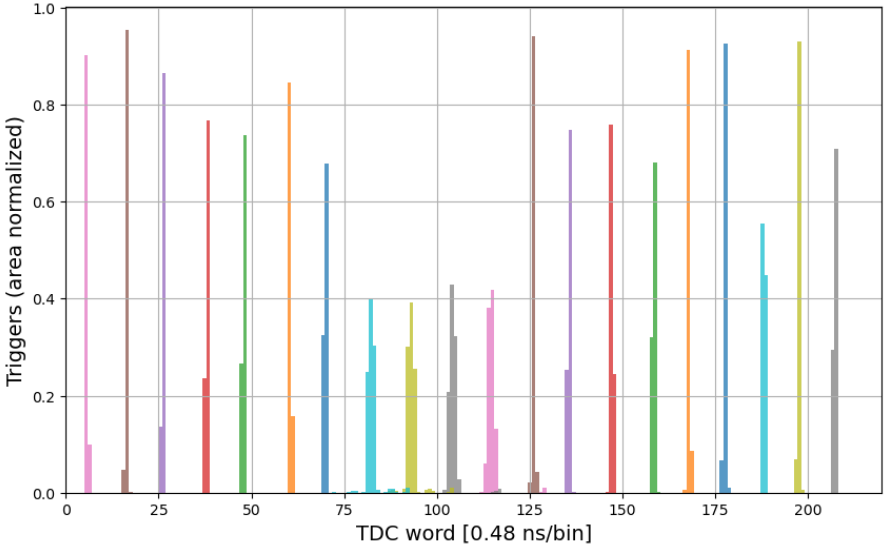


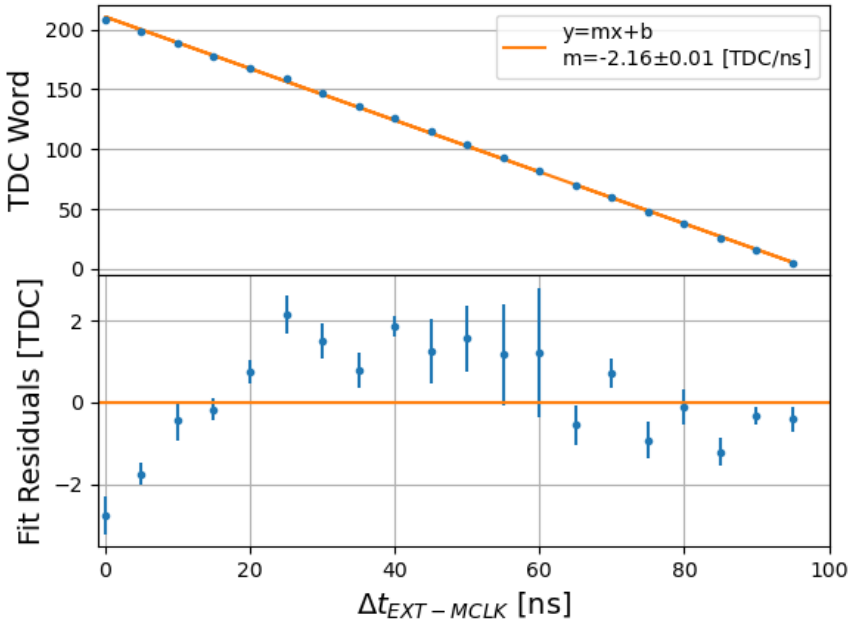


LightPix-v3 produced in 180 nm TSCM

LightPix-v3 TDC

TDC resolution and linearity < 1 ns





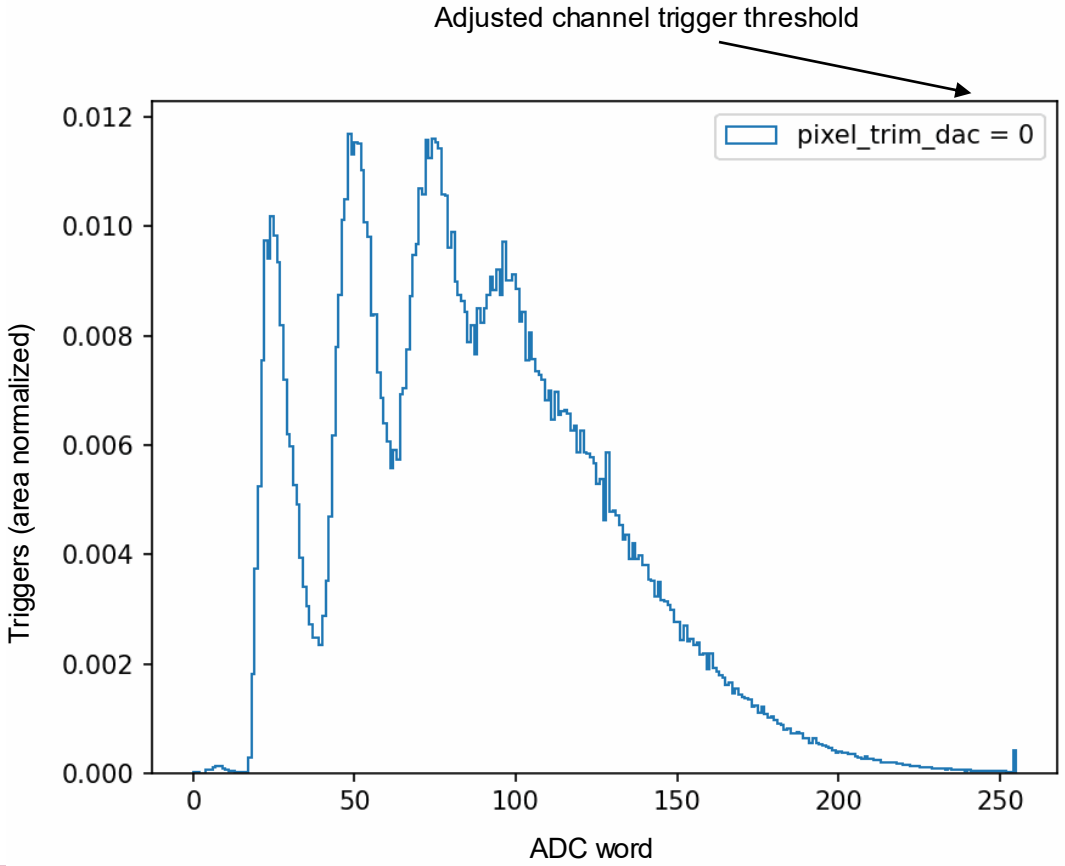
LightPix-v3 ADC

Demonstrated multi-PE discrimination and single-PE self-trigger efficiency

Flexible application:

- Channel threshold tunability for single-channel dark count rejection
- Chip-level dark count rejection

Initial studies (without optimization) demonstrate ~20 PE dynamic range



Summary & Outlook

- LArPix has demonstrated continuous self-triggered pixelated free streaming readout at the O(10^5) channel scale
  - Targeted improvements to be incorporated into the next ASIC tapeout (v3c in Summer '26)
    - Fully-differential front-end buffer
    - Remediate data loss from FIFO event contention
    - Remediate reset correlated front-end pickup
  - Further system channel scaling requires implementation and system integration of a digital multiplexer (MADCAP)
- LightPix is a low-power, cryo-compatible, scale-able readout ASIC for targeting a general multipurpose, high-channel-count SiPM systems
  - Multiple development threads in progress:
    - LightPix+SiPM timing-energy correlation evaluation in progress
    - LightPix-specific system controller architecture
    - In-situ detector format implementation