Low-Noise Wide Dynamic Range Charge Sensitive Amplifier in 65 nm CMOS Technology for the Second Flight of the GAPS Experiment

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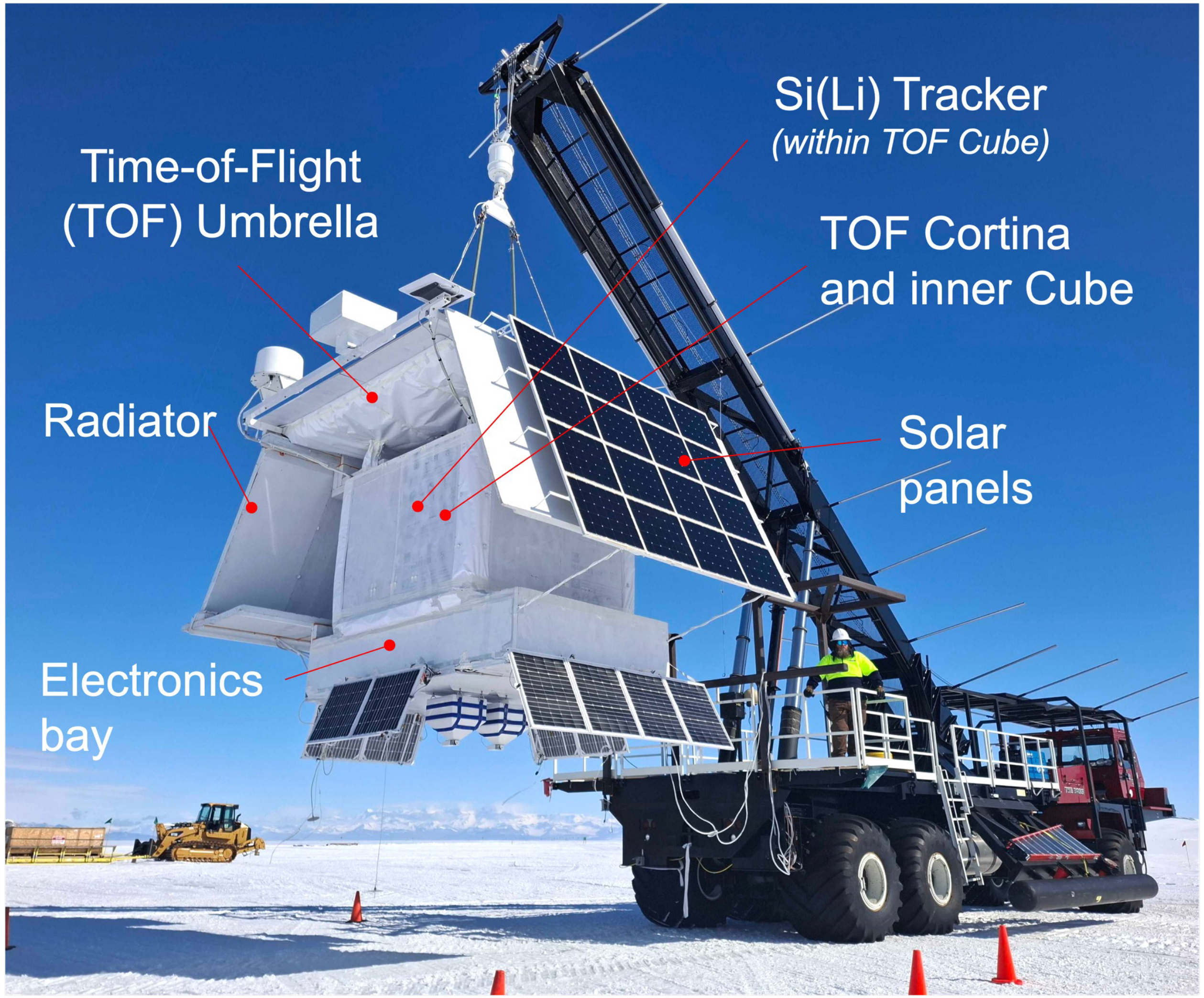
The General AntiParticle Spectrometer (GAPS)



GAPS instrument suspended from the launch vehicle – December 2024

GAPS is an **Antarctic balloon experiment** designed to detect low-energy cosmic antinuclei as an indirect signature of **Dark Matter**

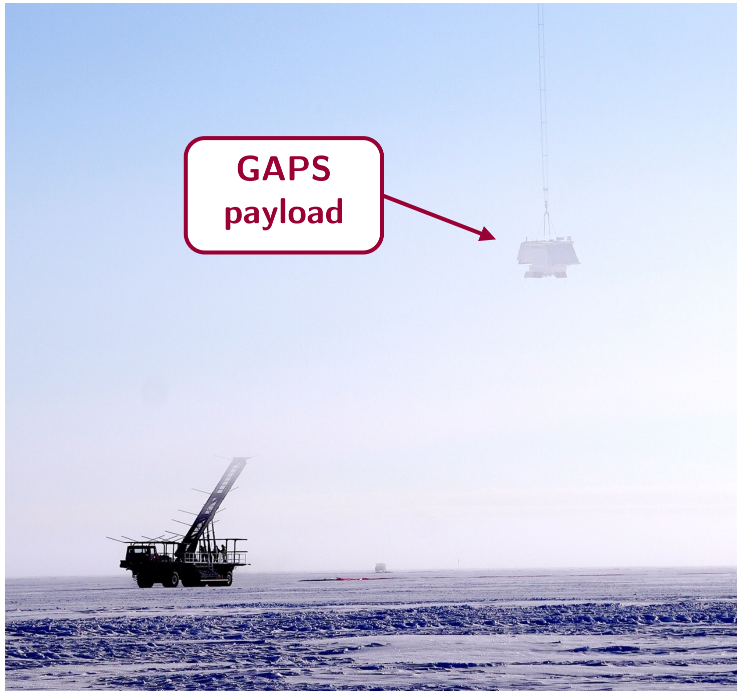
The instrument

- **Time-of-Flight System (TOF)**
  - 160 plastic scintillator paddles with Si-PM readout
- **Si(Li) Tracker**
  - 1009 lithium-drifted silicon (Si(Li)) detectors
  - 7 layers with 10 cm spacing
  - 12x12 Si(Li) detectors per layer
- **Support instrumentation**
  - Thermal Oscillating Heat Pipe (OHP) system
  - Electronics, Solar panels

Final integration at the NASA LDB facility at McMurdo station in Antarctica to assemble and validate the instrument in **December 2024**

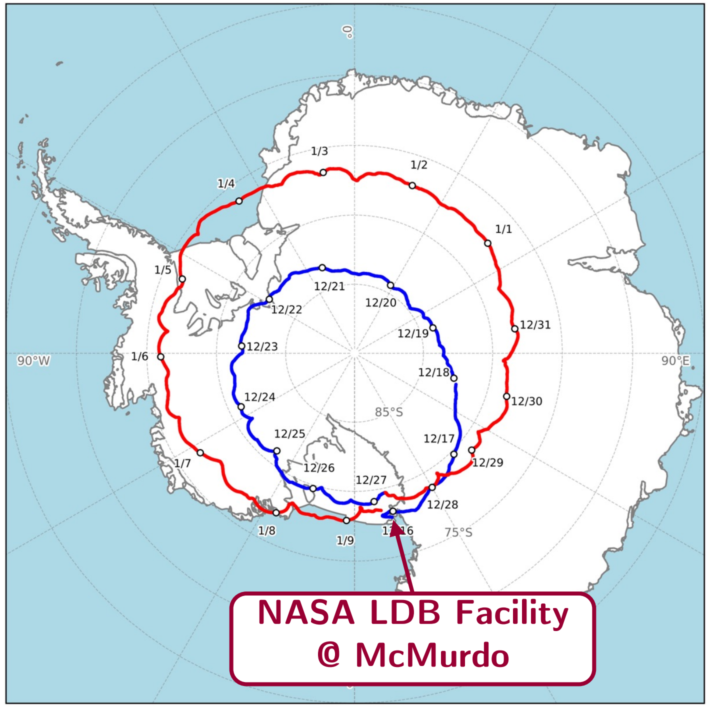
"The General Antiparticle Spectrometer (GAPS) Antarctic Balloon Payload", https://doi.org/10.48550/arXiv.2604.19830

GAPS First Flight in 2025



GAPS launch

- **First successful launch** on Dec 15 at 16:37 UTC
- **Total flight time** 25 days 2 hours 53 minutes
- **Recovery** on ground



Trajectory

- **Two full circumnavigations** of the Antarctic continent
- **~35 km** float altitude
- **~12000 km** total distance
- **~22 km/h** average speed

On ground payload recovery

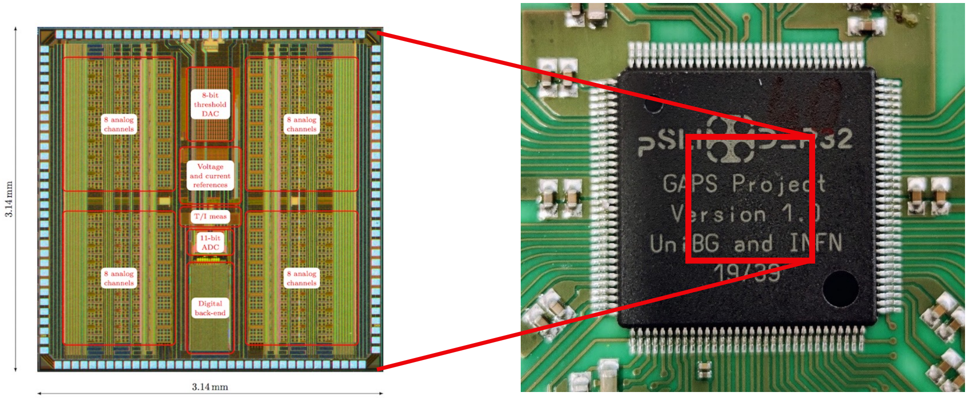
- Total number of triggers: **540 M**
- **1 TB** of data over Starlink
  15 TB of data stored on hard disks

Two additional flights
(~100 days total)

The Si(Li) Tracker

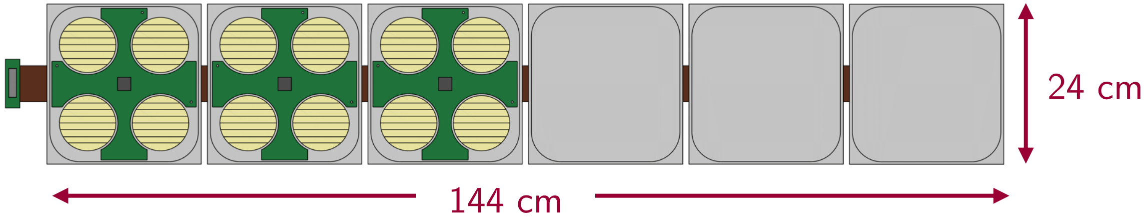
Module[1]

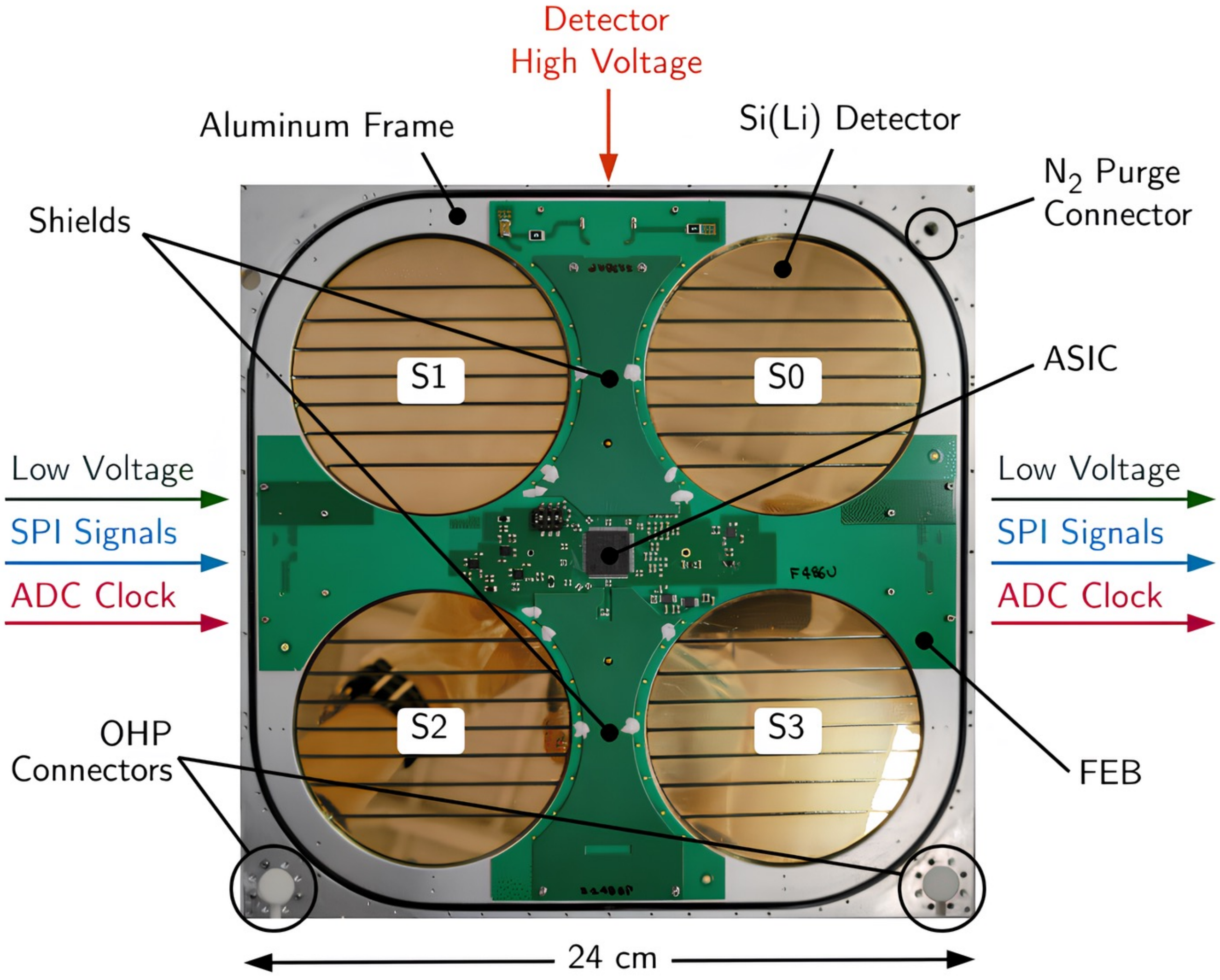
- **4 Si(Li) detectors** with 8 strips each
- **Front-End Board** connected via flex-rigid boards
- **Aluminum frame** and top and bottom windows
- **SLIDER32 Readout ASIC**[1] (180 nm CMOS)



Tracker layer assembly

- **6 modules** connected in series to implement a row
- **6 rows** side by side to implement a plane





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[1] “X-ray and Particle Detection with the Si(Li) Tracker Module of the GAPS Experiment”, https://doi.org/10.1109/TNS.2025.3616408

Charge sensitive amplifier

Main requirements

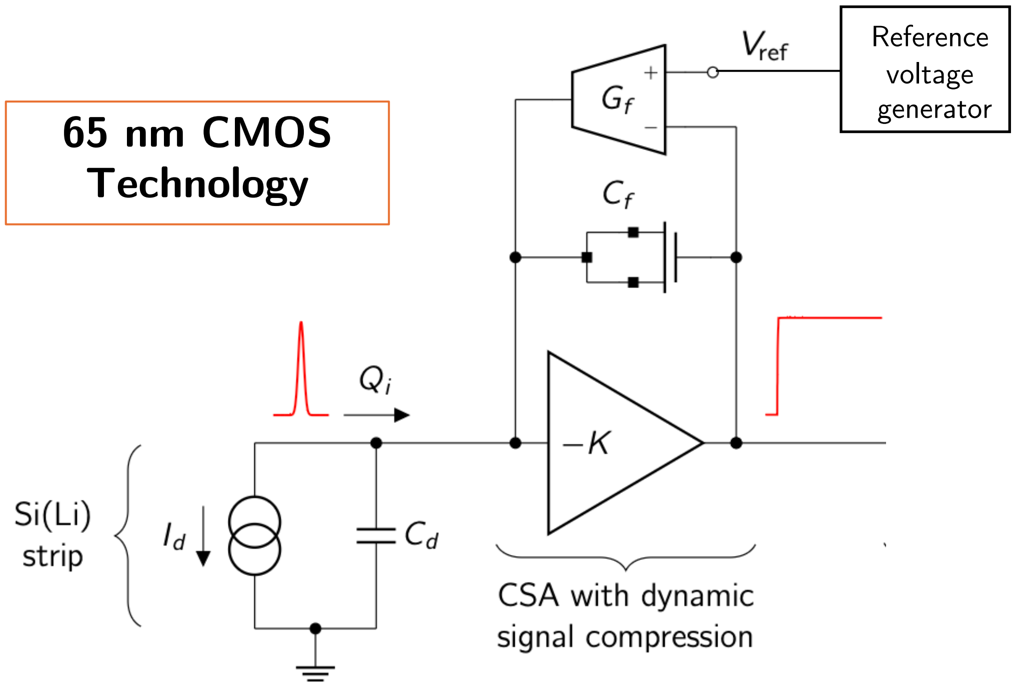
- Dynamic range: 10 keV – 100 MeV
- Power consumption < 10 mW/channel
- Leakage current: 2 nA (-40 °C) up to 200 nA (+30 °C)
- Detector Capacitance: 40 pF
- Resolution: 5 keV FWHM (≈ 600 e- rms)
- Operating temperature: -40 °C

Envisioned applications

- Readout of capacitive sensors in applications with **high input dynamic range** and **high resolution** at low energies

- Upgrade of the ASIC[1] developed in **180 nm CMOS** technology for the readout of Si(Li) detectors in tracker of the **GAPS experiment (second and third flights)**

65 nm CMOS Technology



Distinctive features in CSA feedback

- **Feedback capacitance** C_f is implemented using a MOS capacitor to achieve **Dynamic Signal Compression**
  - Cope with 10 keV to 100 MeV incoming energy range
  - Preserve sensitivity in the X-ray detection region (up to 100 keV)
- **Reference voltage** as a function of temperature
- **Improved Krummenacher** circuit for charge restoration and detector leakage current compensation (up to 200 nA)

[1] "A 32-Channel Readout ASIC for X-Ray Spectrometry and Tracking in the GAPS Experiment", https://doi.org/10.1109/TNS.2023.3336192

Dynamic signal compression with MOS capacitor

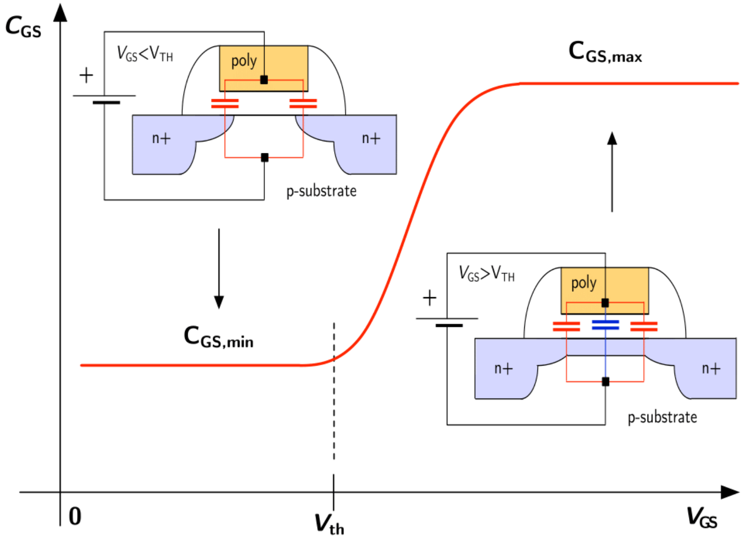
Drain-source shorted to form one capacitor terminal, the **gate** forms the other

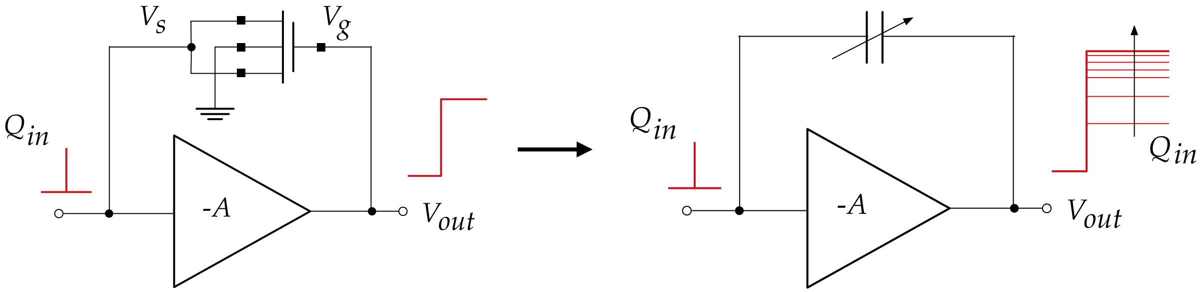
- $0 < V_{GS} \ll V_{Th}$ → C_{GS} is set at its minimum and it is mainly due to the overlap gate-to-source $C_{\mathrm{GS,ov}}$ and gate-to-drain $C_{\mathrm{GD,ov}}$ capacitances:

$$C_{min} \approx C_{GS,ov} + C_{GD,ov} = 2W\Delta LC_{OX}$$

- $V_{GS} \gg V_{Th}$ → C_{GS} shows a maximum value mainly given by C_{GC} capacitance:

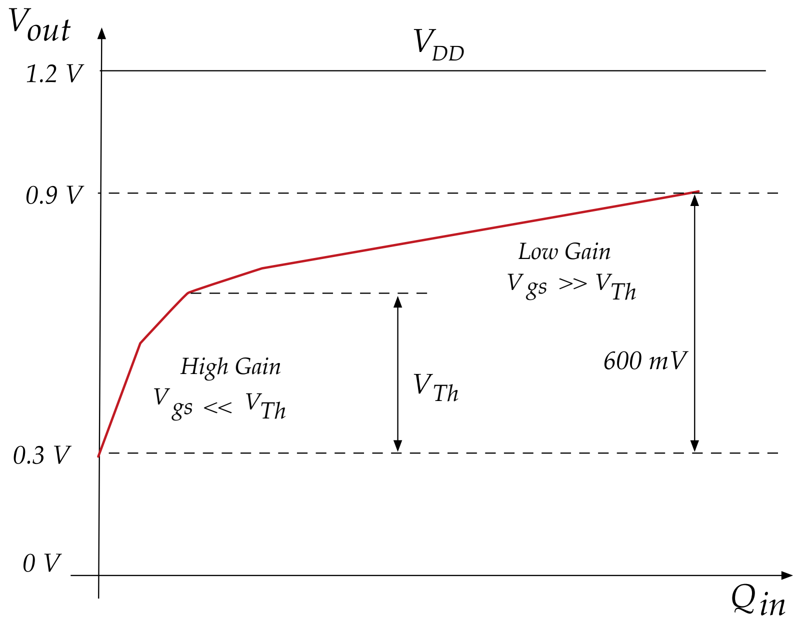
$$C_{max} \approx C_{GC} = WLC_{OX}$$





CSA Gain

$$G = \frac{1}{C_{GS}}$$



Limitations related to the MOS threshold voltage

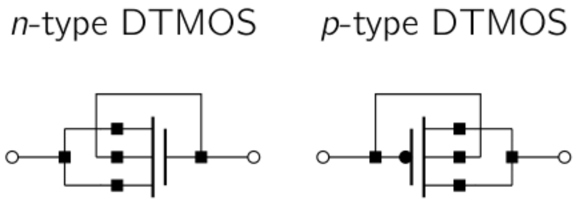
- CSA output voltage range must be greater than V_{Th} (V_{Th} is increased by the body effect)
- V_{Th} depends on temperature

"Dynamic compression of the signal in a charge sensitive amplifier: from concept to design", https://doi.org/10.1109/TNS.2015.2477461

CSA feedback capacitor

DTMOS: Dynamic Threshold MOSFET

- Originally proposed in 1994 by Assaderaghi in *"A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation"*
- The device **bulk (well)** is connected to the **gate**

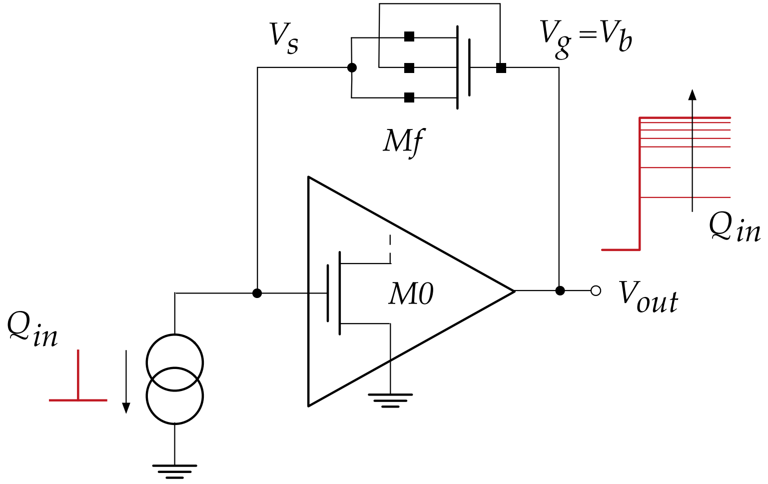


- As a result: $V_{\mathrm{BS}} = V_{\mathrm{GS}}$ and the threshold voltage is changed dynamically with V_{GS}

$$V_{\mathrm{TH}} = V_{\mathrm{TH,0}} + \gamma\left(\sqrt{2\phi + \underset{\substack{\| \\ -V_{\mathrm{GS}}}}{V_{\mathrm{SB}}}} - \sqrt{2\phi}\right)$$

→ V_{TH} decreases as V_{GS} increases

DTMOS as CSA feedback element



$$V_{\mathrm{TH}} = V_{\mathrm{TH,0}} + \gamma\left(\sqrt{2\phi - V_{\mathrm{out}} + V_{\mathrm{S}}} - \sqrt{2\phi}\right)$$

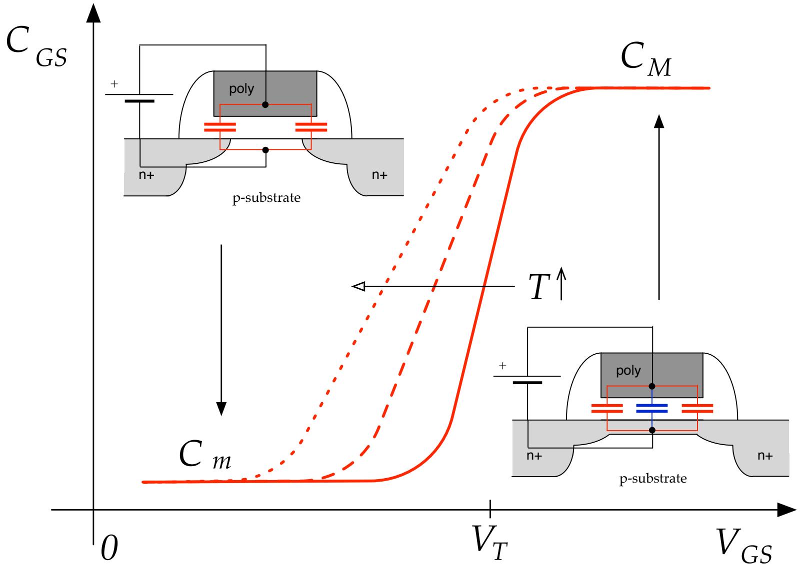
→ V_{TH} decreases as V_{out} increases

Expected differences wrt standard MOS

- reduced requirement for **output dynamic range**
- slightly **sharper transition** between high and low gain region

Temperature effects

C-V curve



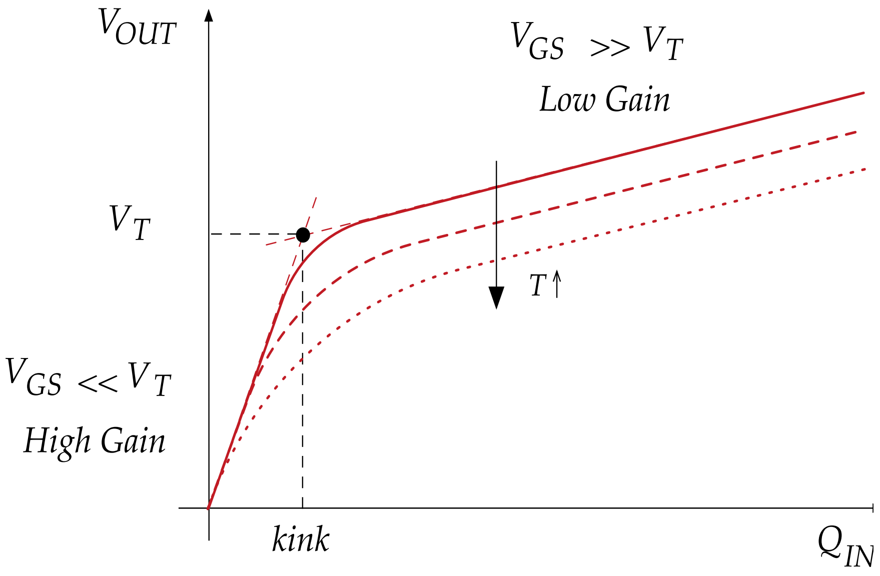
1. Feedback MOS threshold voltage

Transistor threshold voltage decreases with T

$$V_{TH}(T) = V_{\mathrm{TH},0} - K_T T$$

- the C-V characteristic shifts accordingly
- the transition point (kink) between the high and the low gain regions of the CSA transfer characteristic displaces with T

CSA transfer characteristic

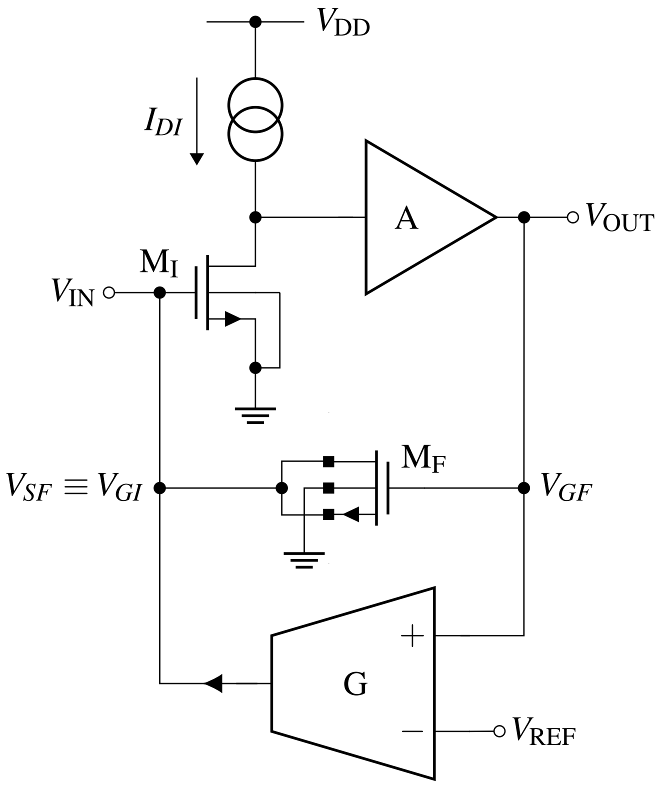


2. Space-charge at the silicon-oxide interface

It depends on temperature and affects the transition between week and strong inversion

- The slope of the transition between min and max values of the capacitance decreases with T
- less sharp transition of the CSA characteristic between the high and low gain regions

Temperature effect mitigation



The CSA characteristic depends on the overdrive voltage of the feedback transistor $\mathbf{M_F}$

$$V_{OVF} = V_{GSF} - V_{TF} = V_{REF} - V_{GI}(T) - V_{TF}(T)$$

it is affected by temperature variations of

- **Threshold voltage** $V_{TF}(T)$ of the feedback transistor M_F
- **Threshold voltage** $V_{TI}(T)$ of the input transistor M_I (that affects V_{GI})

The effect can be mitigated by generating V_{REF} in a way which follows the temperature variations so that V_{OVF} is temperature independent

Temperature dependent reference voltage

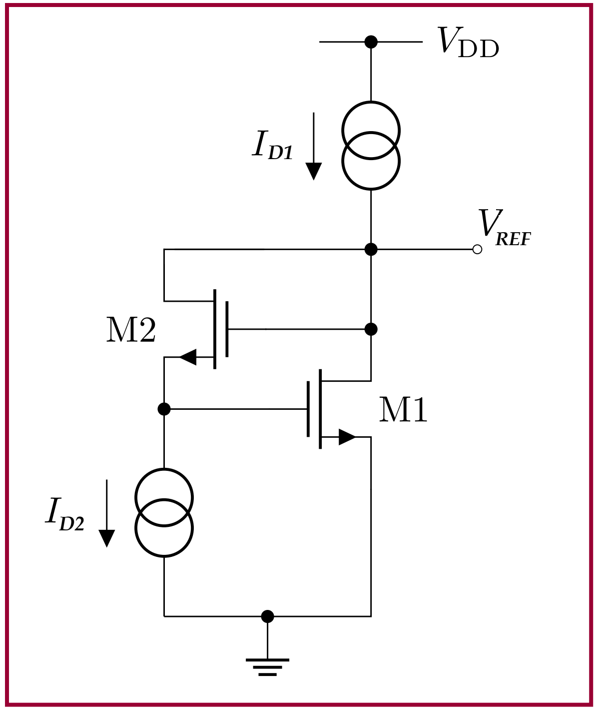
$$V_{REF} = \alpha - \beta \cdot T$$

With:

$$\alpha = V_{OVF}(-40°C) + V_{TF0} + V_{TI0}$$

$$\beta = K_F + K_I + \mathrm{n}\frac{k_B}{q}\ln\frac{I_{DI}}{I_{D0}}$$

Reference Voltage Generator



Assuming

$$\begin{cases} V_{TF}(T) = V_{TF0} - K_F T \\ V_{TI}(T) = V_{TI0} - K_I T \\ I_{DI} = I_{D0} exp\left[\dfrac{q(V_{GI} - V_{TI})}{nk_B T}\right] \end{cases}$$

Charge restoration feedback network

Krummenacher architecture

- **Discharges the amplifier feedback capacitor**
- **Sets the DC voltage at the CSA output node** (gate of $M2$, to the same $Vref$ as gate of $M1$)
- **Compensates for detector DC leakage currents** more than the tail current Ik

Network limit

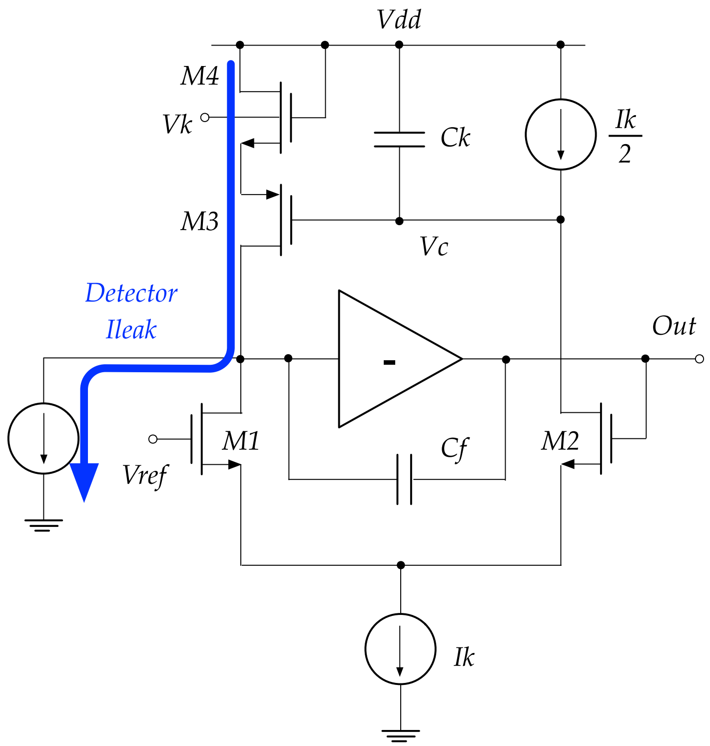
Stage unbalanced for wide output signals

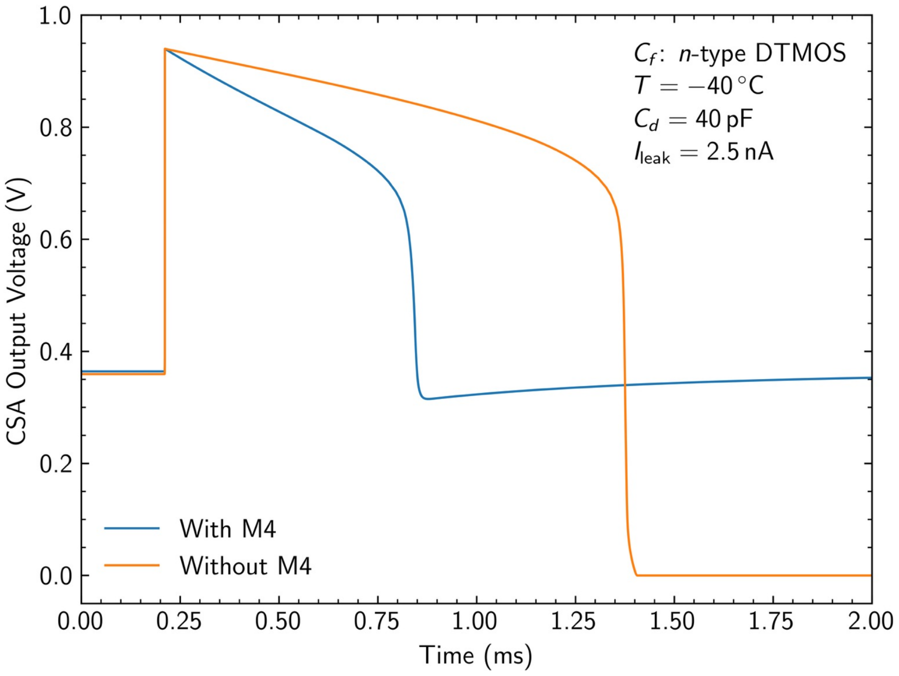
→ $Ik/2$ integrated on Ck (Vc shift)

→ additional output current that can unbalance the stage in the opposite direction when $Vout$ returns to baseline

(large Ck capacitor to reduce the effect)

$$\boxed{i_o = g_{m3} V_C = g_{m3} \frac{I_K}{2C_K} \cdot t}$$





Network improvement

Bulk of additional transistor $M4$ is used to regulate the discharge current

$$\boxed{i_o \approx g_{m3} \left(V_C + \frac{g_{mb4}}{g_{m4}} V_K \right)}$$

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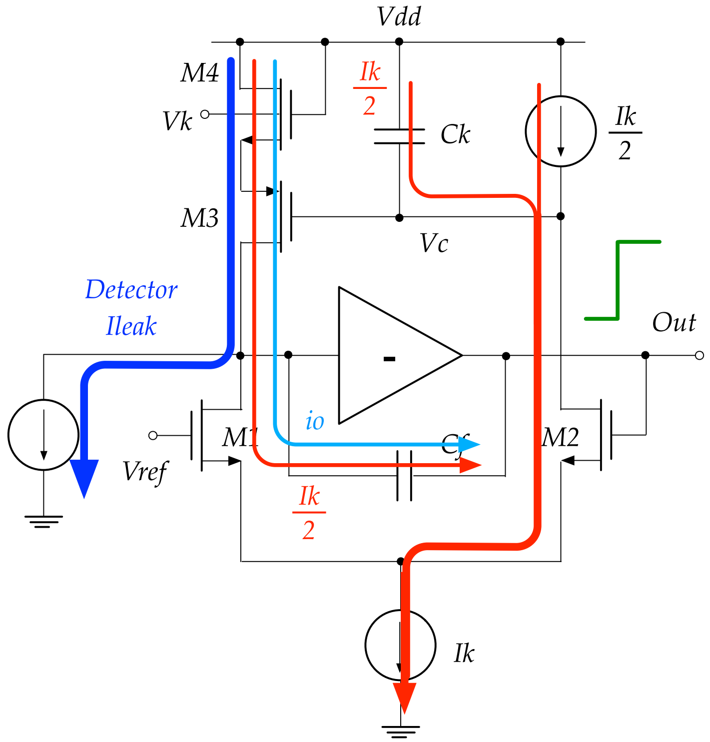

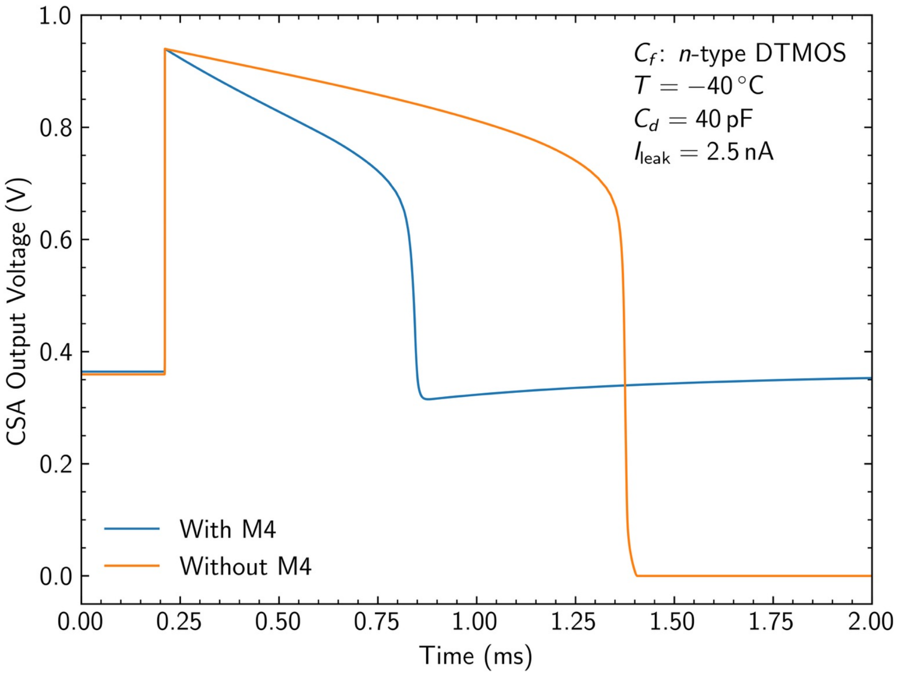

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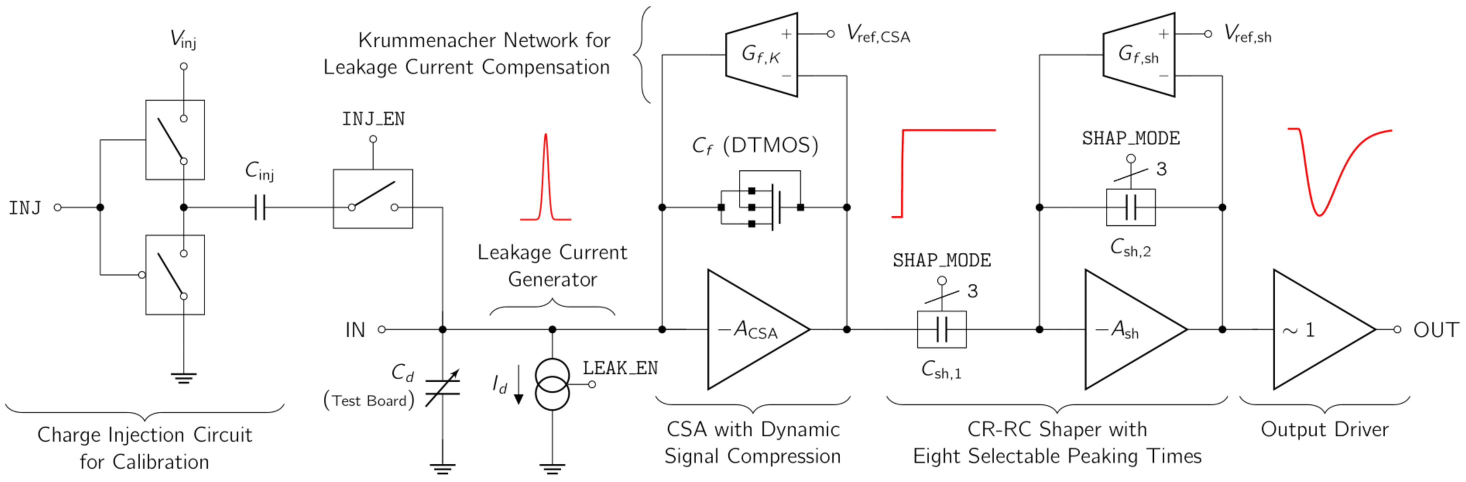
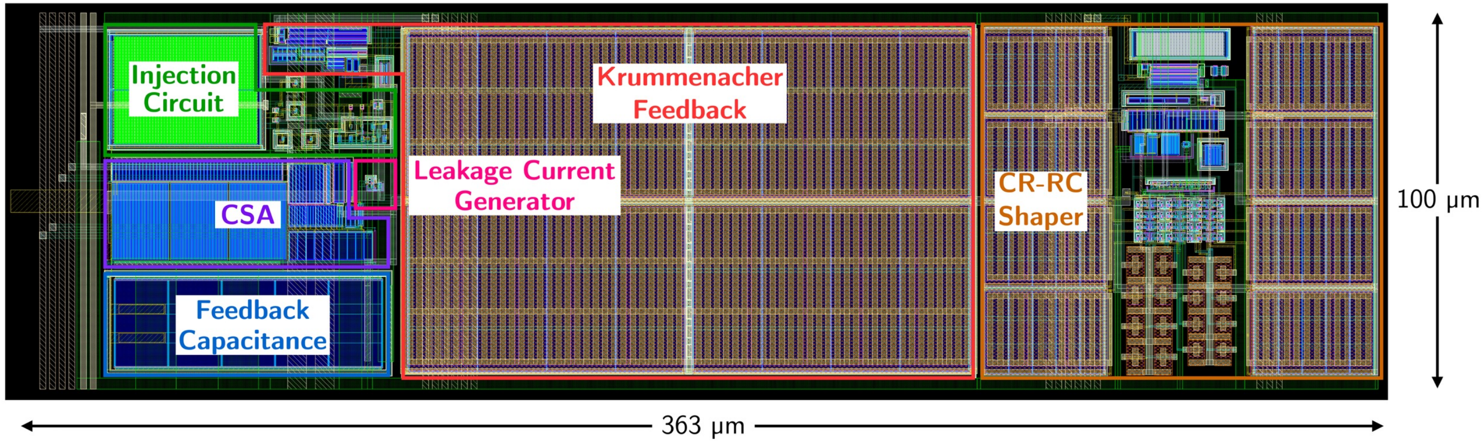
Readout channel





Area 363 µm × 100 µm

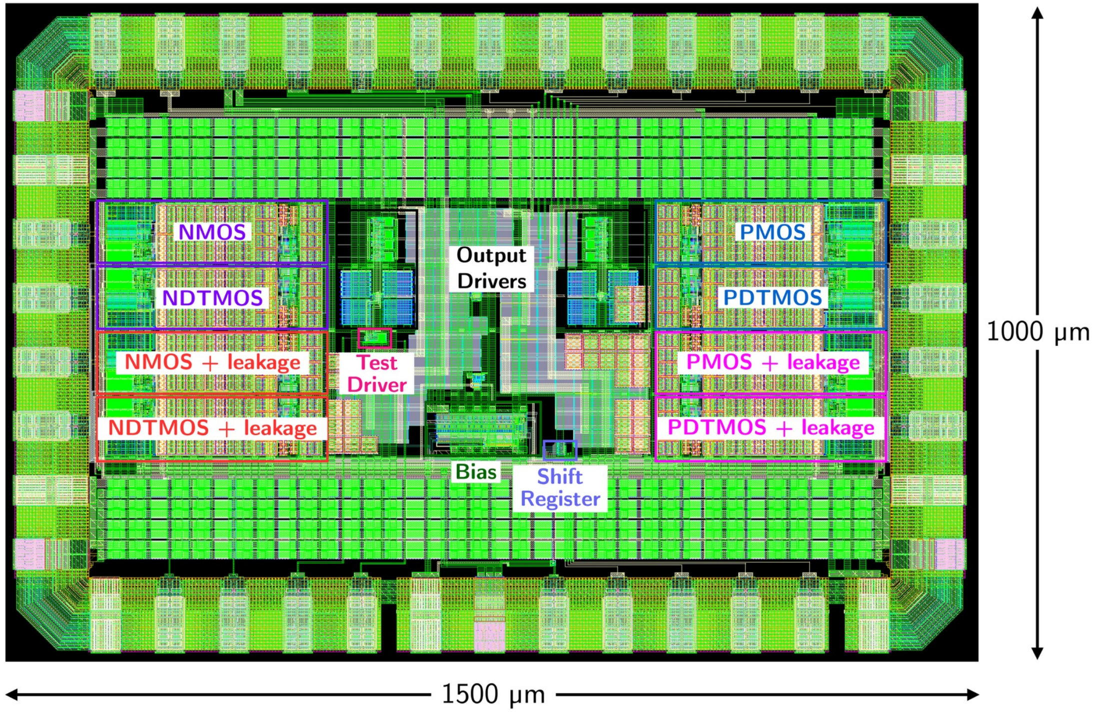
- **Charge sensitive amplifier** with dynamic signal compression
- **CR-RC filter** with 8 selectable peaking times (from 0.2 to 1.6 µs)
- **Charge injection circuit** for calibration in the 10 keV to 100 MeV energy range (External 16-bit DAC provides V_{inj} reference voltage)
- **Leakage current emulator** circuit to test the compensation capabilities of the Krummenacher feedback up to 500 nA
- **Output buffer** to drive the oscilloscope load capacitance

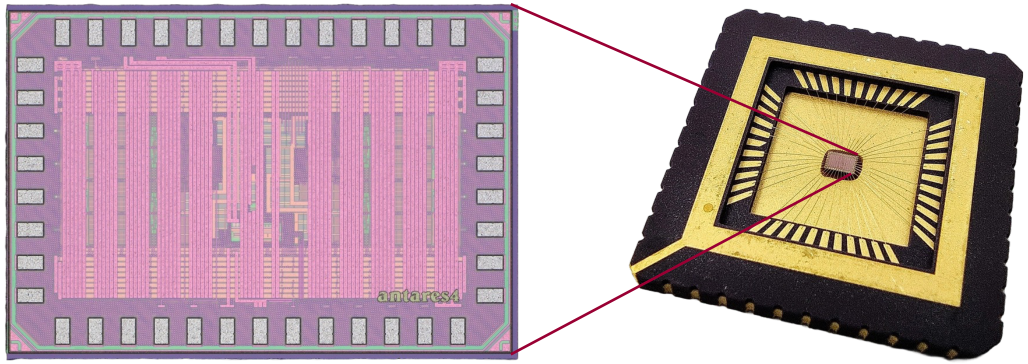
Power consumption

3.5 mW/ch vs 8.3 mW/ch

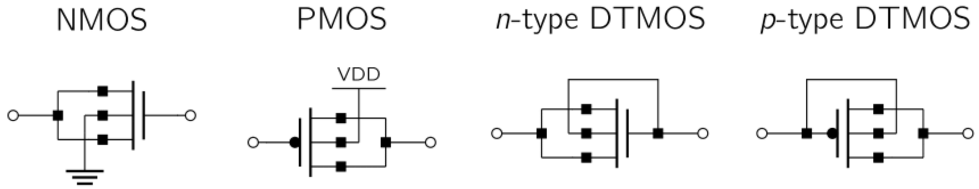
of the 180 nm version

Test ASIC



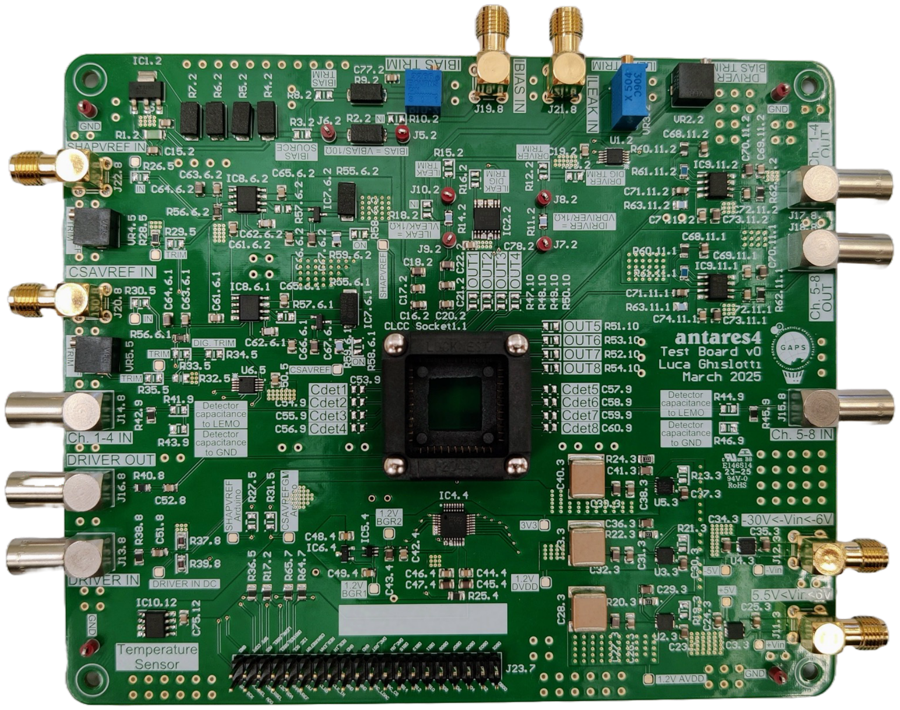


- Design submitted in February 2025 and delivered in late **July 2025**
- Area 1500 µm × 1000 µm with 42 pads
- CLCC44 package
- Eight fully analog channels
- Four CSA feedback configurations (same area for comparison purposes)



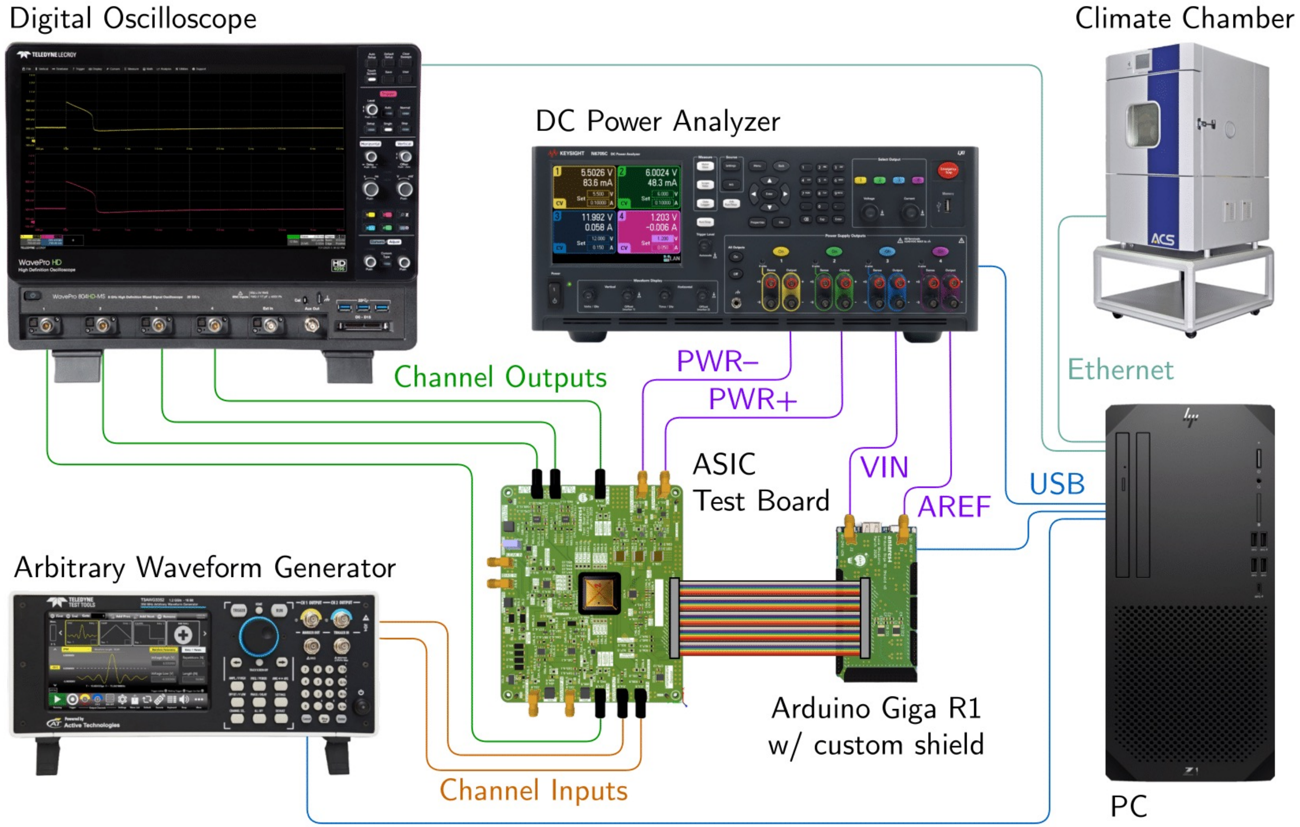
Configuration	**Length** (µm)	**Width** (µm)	**Gate area** (μm^2)
n-type MOS	14.0	114.3	1600.2
n-type DTMOS	14.0	114.3	1600.2
p-type MOS	20.0	80.0	1600.0
p-type DTMOS	20.0	80.0	1600.0

Test setup



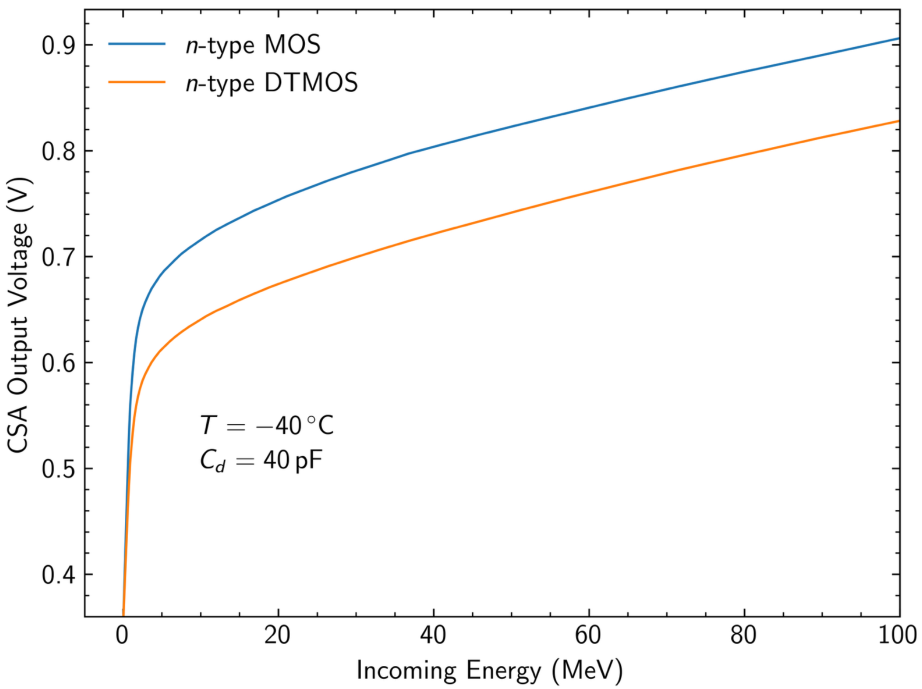
Custom ASIC test board with CLCC44 socket

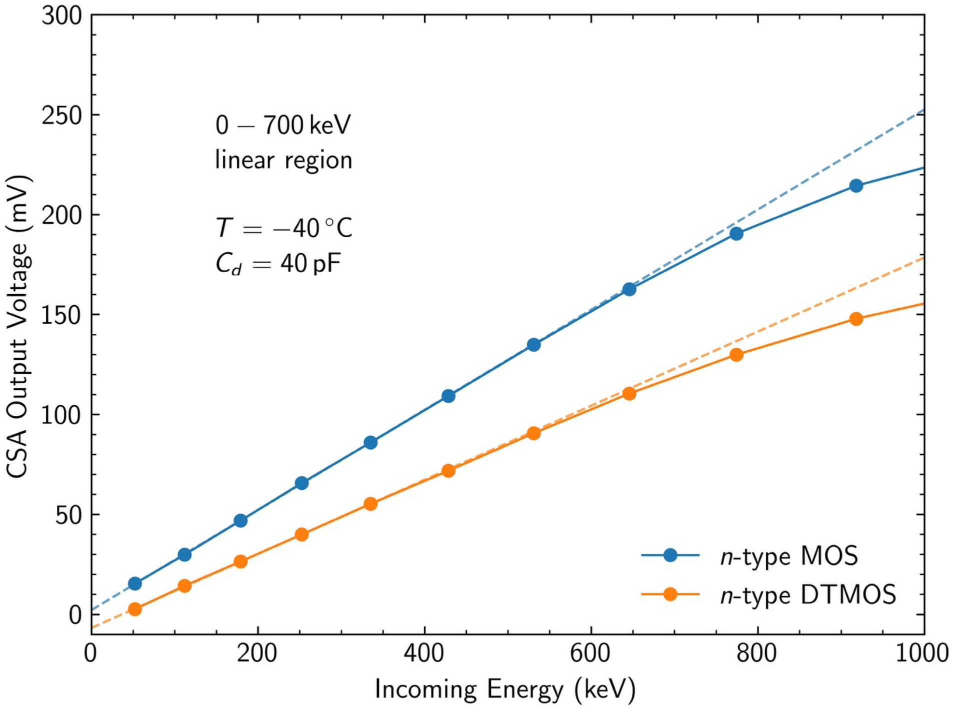
- 16-bit DAC generates the V_{inj} voltage for the charge injection circuit
- Programmable voltage references and current biases for automated testing
- On-board temperature sensor



- Test setup supports full-automated test routines
- **Climate chamber** control for temperature testing and ASIC operation at **-40 °C** flight temperature

CSA transfer characteristic



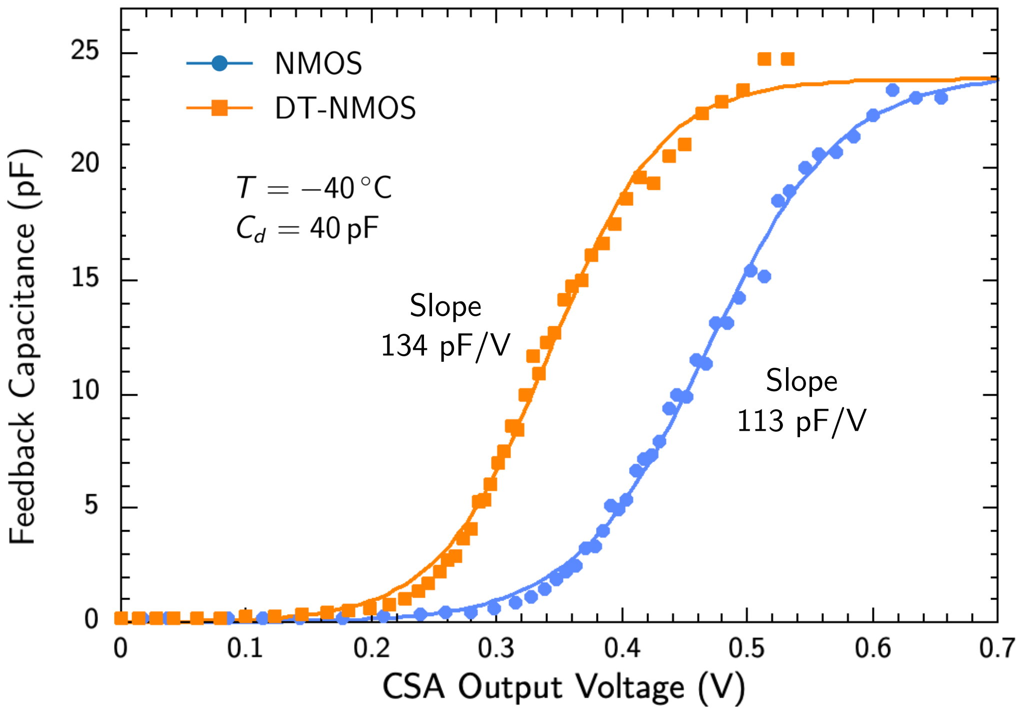


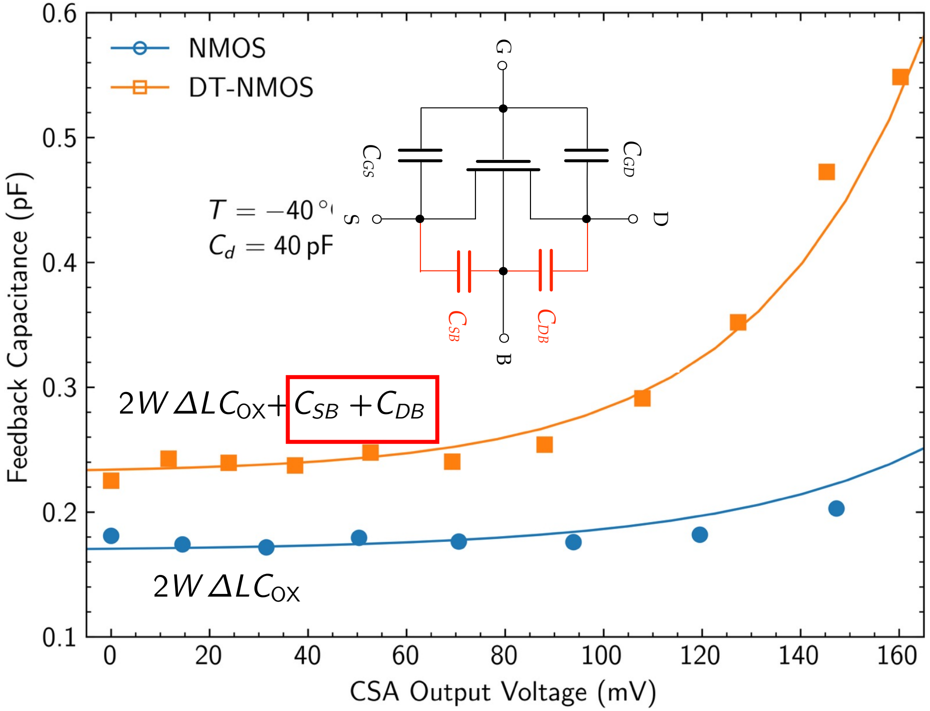
	***n*-MOS**	***n*-DTMOS**
G_{le} (µV/keV)	259	187
G_{he} (µV/keV)	2.03	1.91
Compression factor k	127	98
Kink (keV)	1918	2023
ΔV_{out} (mV)	653	532

***n*-DTMOS** vs ***n*-MOS** feedback shows:

- 30% lower **low-energy gain** ✗
- slightly reduced **high-energy gain** ≈
- 30% lower **compression factor (*k*)** ✗
- 20% smaller **output swing** ✓

Feedback capacitance





Extracted by differentiating the transfer characteristic of the CSA wrt the output voltage and fitted with:

$$C_{\mathrm{F}} = \frac{C_M + C_m}{2} + \frac{C_M - C_m}{2}\tanh[a(V_{out} - b)]$$

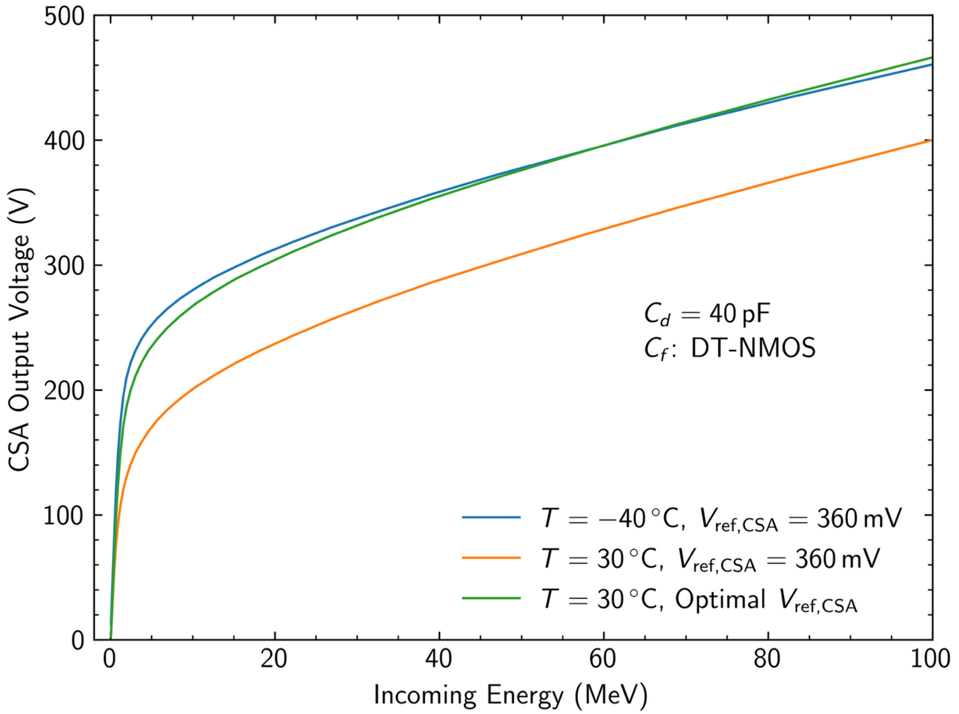
L. Ratti, et al. "A 2D imager for X-ray FELs with a 65 nm CMOS readout based on per-pixel signal compression and 10-bit A/D conversion", https://doi.org/10.1016/j.nima.2016.05.055

***n*-DTMOS** vs ***n*-MOS** feedback capacitance shows:

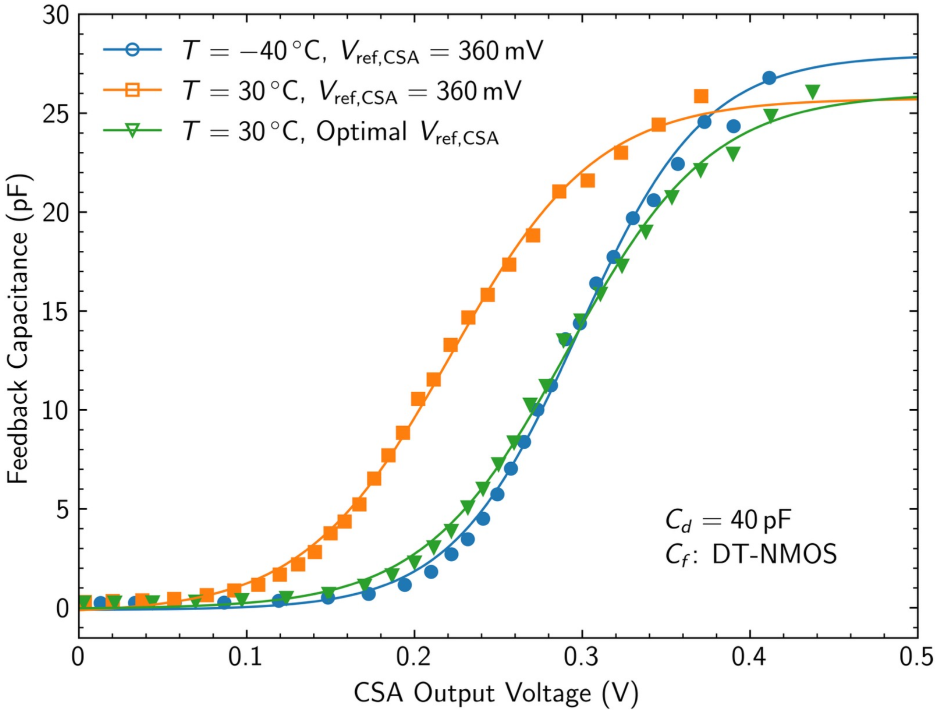
- lower transition voltage ✓
- higher slope of the transition ✓
- higher capacitance in the low-energy gain region
  → lower low-energy gain ✗
  (can be increased by reducing the W of the device)

Temperature effects

CSA transfer characteristic



Feedback capacitance

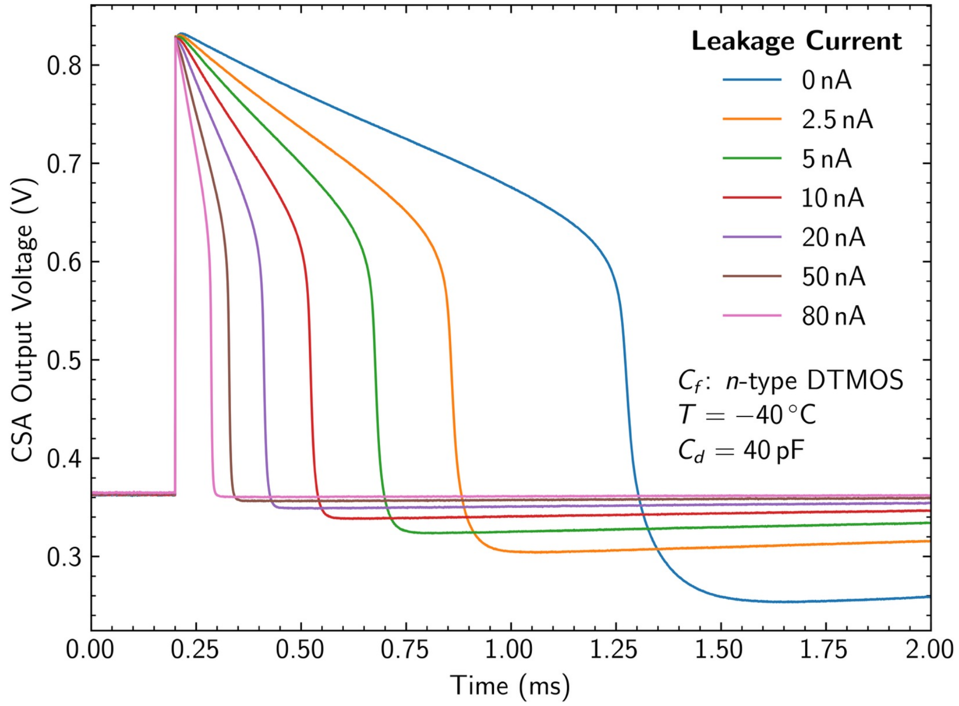


- The reference voltage generator compensates for the effect of temperature on the feedback MOS *Vth* ✓
- It remains the reduction in the slope of the transition between minimum and maximum value of the feedback capacitance ✗

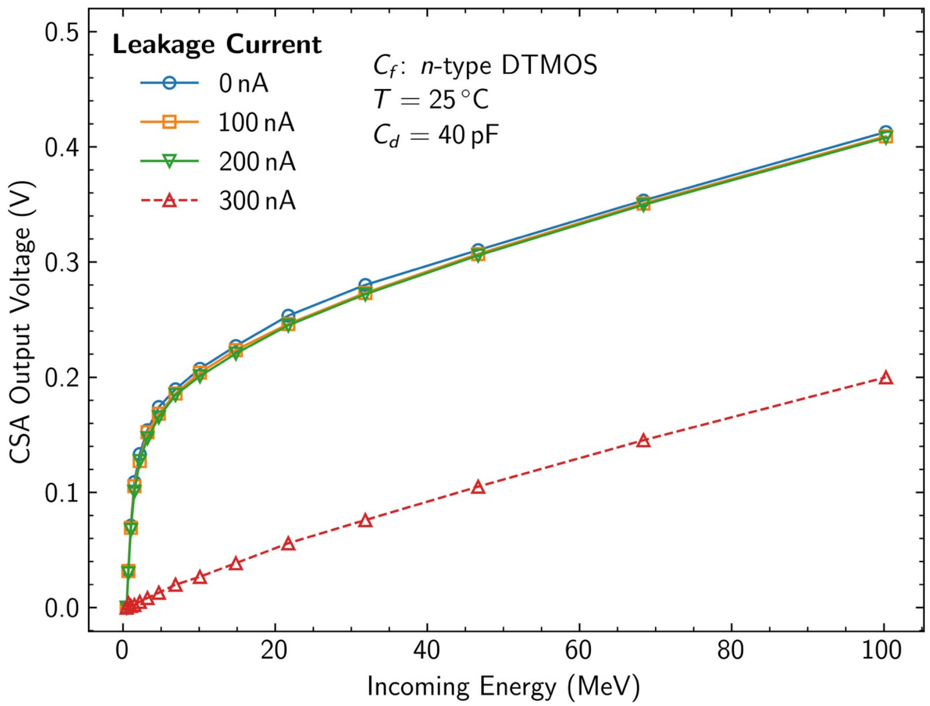
	-40 °C	+30 °C	
		Vref=360 mV	**Vref=f(T)**
Transition (mV)	293	221	291
Slope (pF/V)	145	115	117

Leakage current compensation

Transient response at -40°C



Transcharacteristic at 25°C



Leakage current at – 40 °C

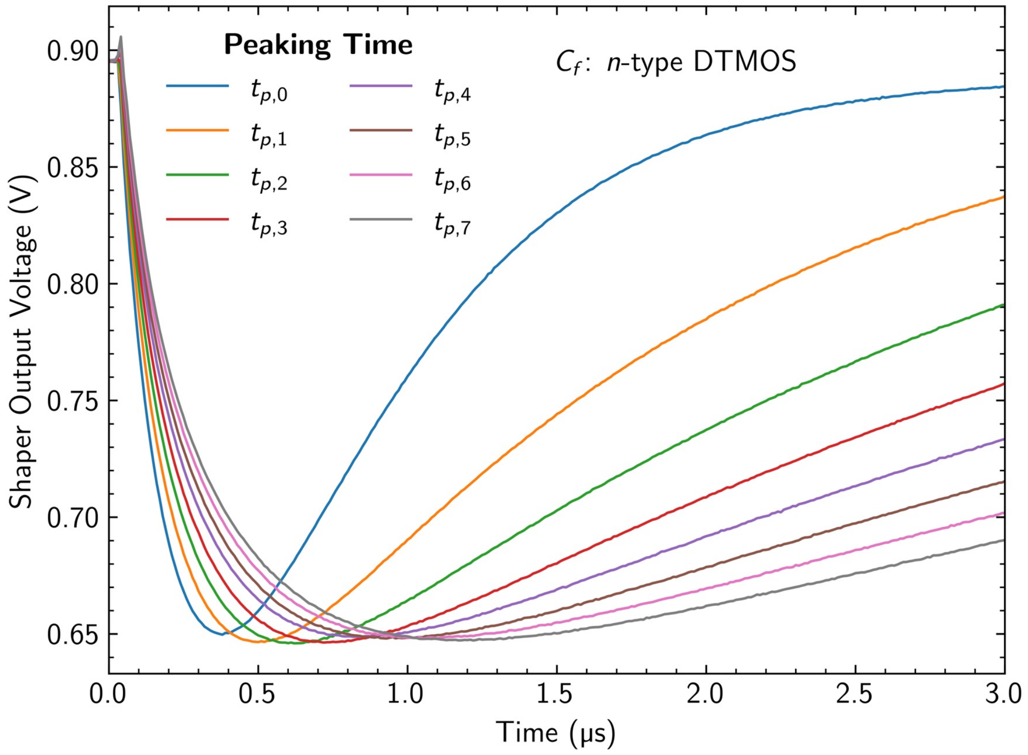
- Up to 80 nA, well above the values expected from the Si(Li) detector in flight conditions ✓

Leakage current at at room temperature

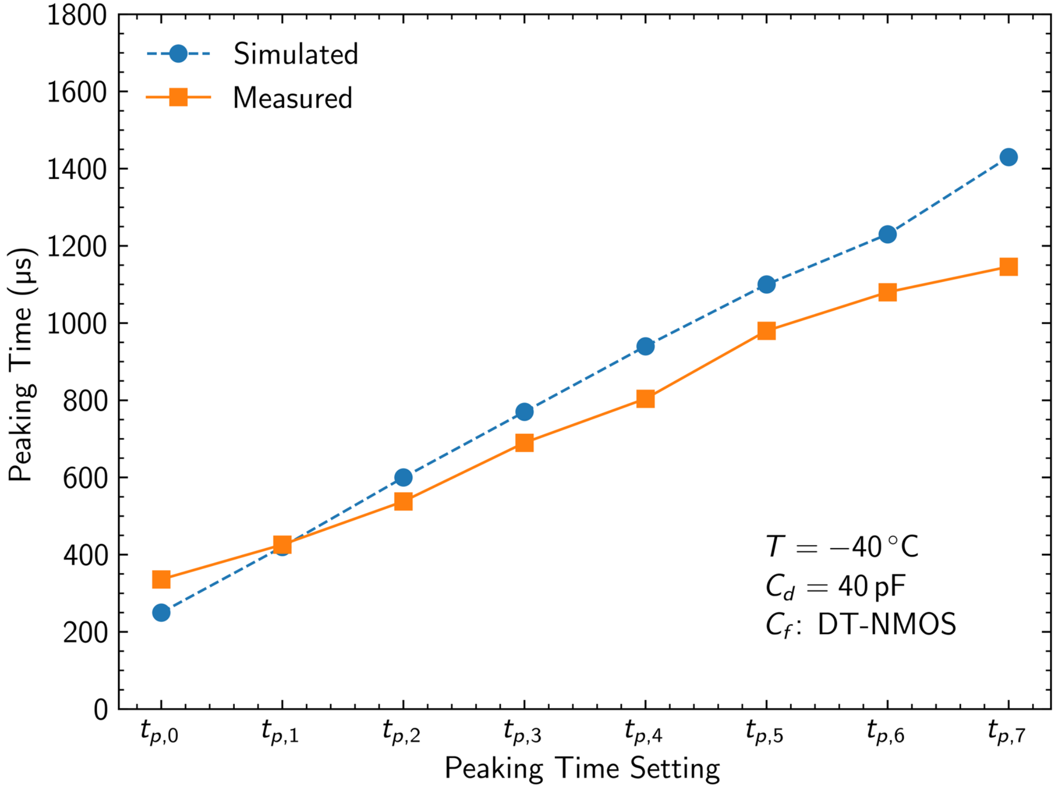
- Tested beyond 300nA
- Up to 200nA ✓

Shaper time response

Shaper Transient response



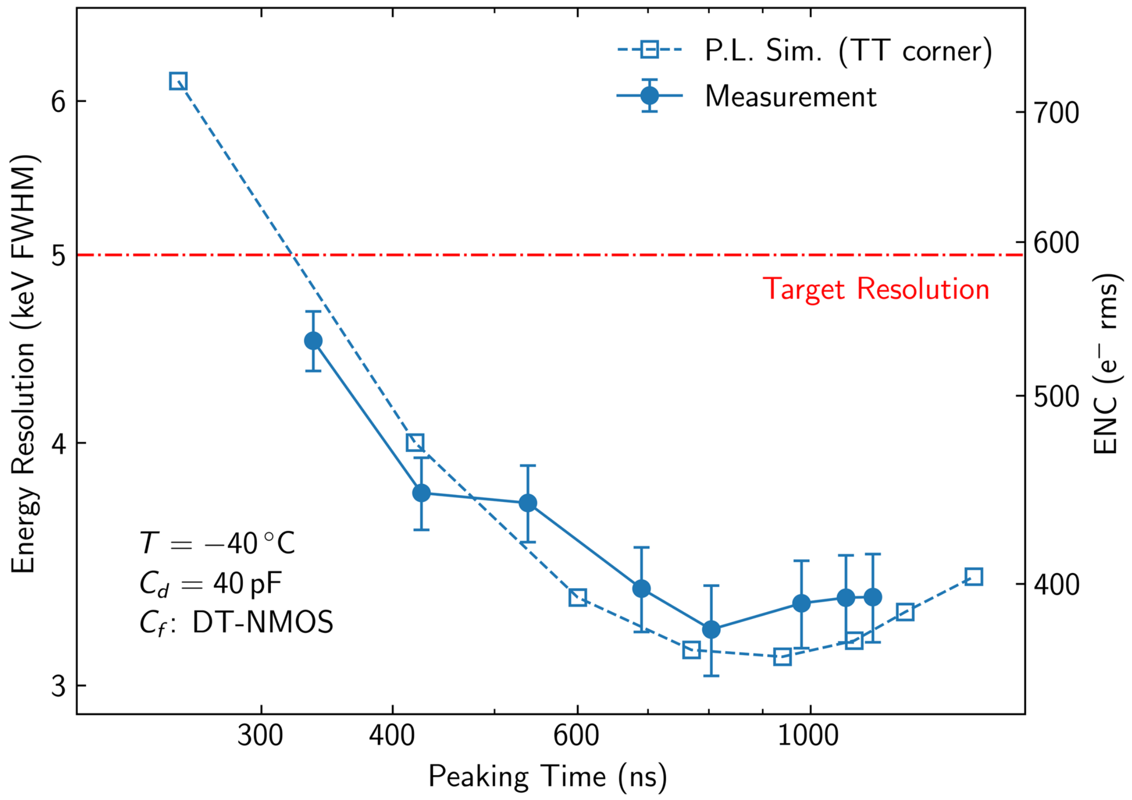
Measured vs simulated peaking times

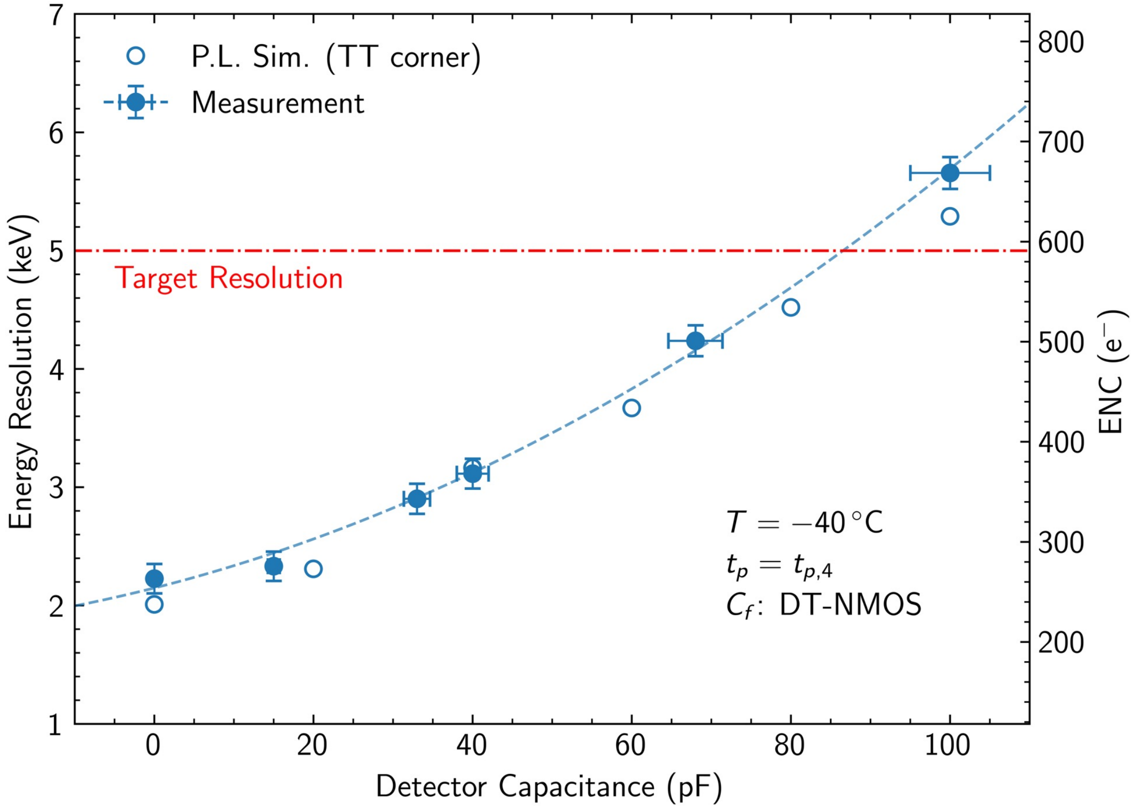


- Good unipolar semi-Gaussian (CR-RC) time response for the 8 peaking times

- Measured peaking times values slightly different wrt simulated ones

Energy Resolution





- Resolution with **nDTMOS** better than the target 5 keV FWHM for all peaking times ✓
- Measurement for NMOS in progress

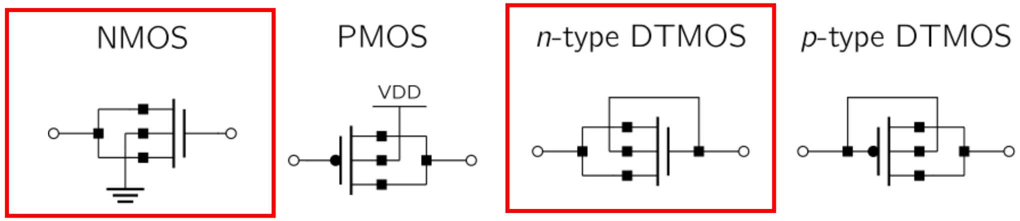
Increase with detector capacitance:

- ∼ 0.04 keV FWHM/pF
- ∼ 5 e-rms/pF

Summary

Use of a **Dynamic Threshold MOS** as the feedback element of a charge sensitive amplifier implementing dynamic signal compression

- Four feedback configurations available (2 tested)



- n-DTMOS provides promising results with the only exception of low-energy gain and compression factor
- This limit can be overcome by reducing the gate width of the device

Reference Voltage Generator to mitigate the temperature effects on the CSA feedback MOS

Bulk controlled MOS in the Krummenacher feedback network validated

CSA parameter	**n-MOS**	***n-DTMOS***
Rise time	✗	✓
Low-energy gain	✓	✗
High-energy gain	≈	≈
Compression factor	✓	✗
Slope of transition	✗	✓
Output swing	✗	✓
Noise	--	✓

Future plans

- Complete the test of the 4 CSA feedback configurations and come to a final decision
- Complete the design of the analog readout channel
- Submit a chip with 8 channels + ADC and Digital Backend by the end of 2026
- Submit the **flight ASIC with 32 channels** by the end of 2027 (ready for second flight of GAPS experiment)