Development of the COFFEE Chip for Particle Tracking

— A MAPS in 55 nm HVCMOS process for CEPC ITK and LHCb UP

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COFFEE

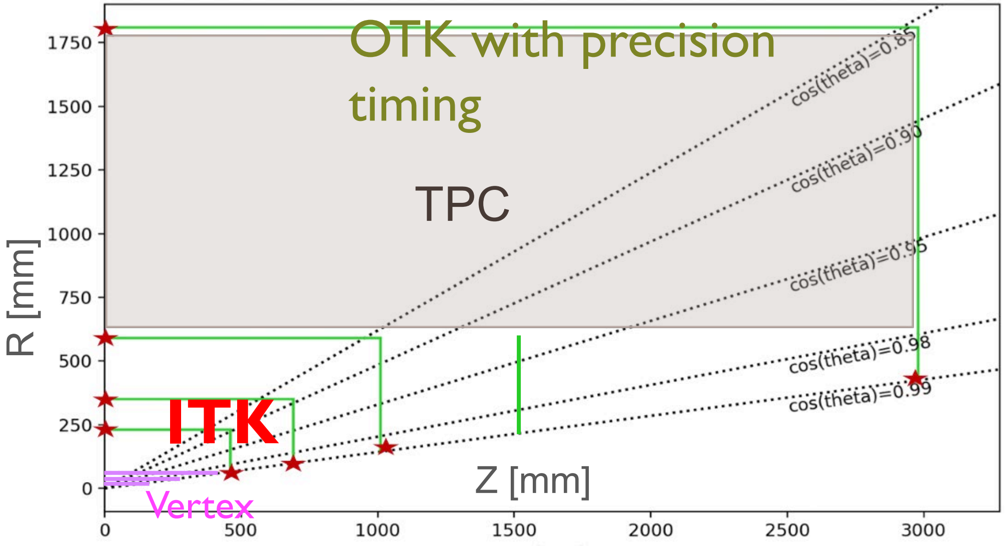
CMOS SENSOR IN
FIFTY-FIVE NM PROCESS

On behalf of the HV-CMOS pixel sensors in 55nm process collaboration

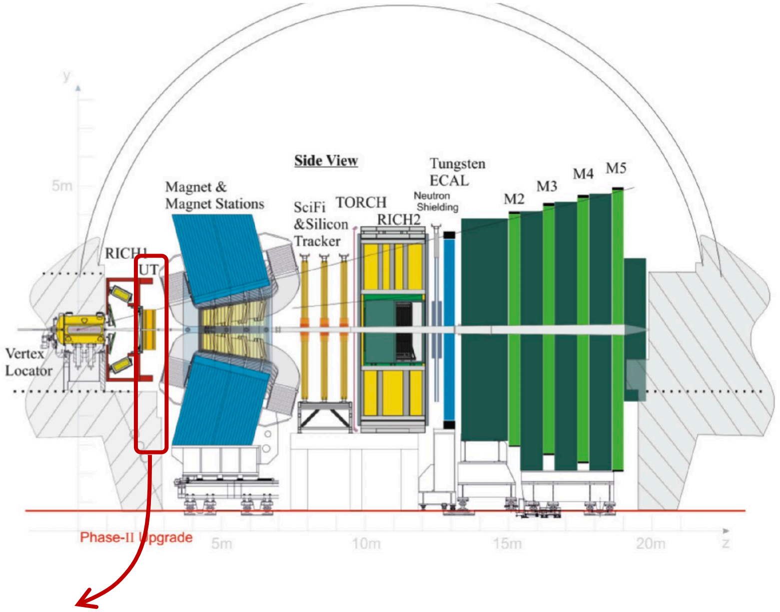
The XIII FRONT-END ELECTRONICS WORKSHOP, Paris, France, 18-22 May, 2026

Background & Motivation

Current R&D targets for two applications：

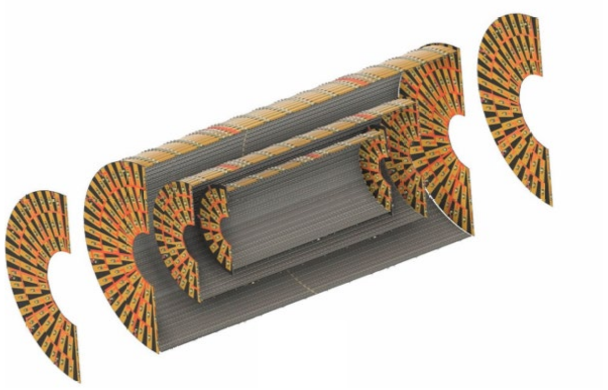


The CEPC Inner Tracker (ITK)

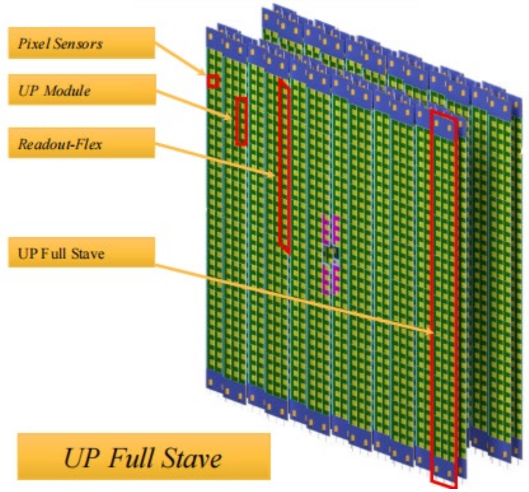


LHCb Upstream tracker upgrade II (UP)

Key Performance Metrics for Both Applications



CEPC ITK： 3 barrels layers + 4 pairs of endcap disks



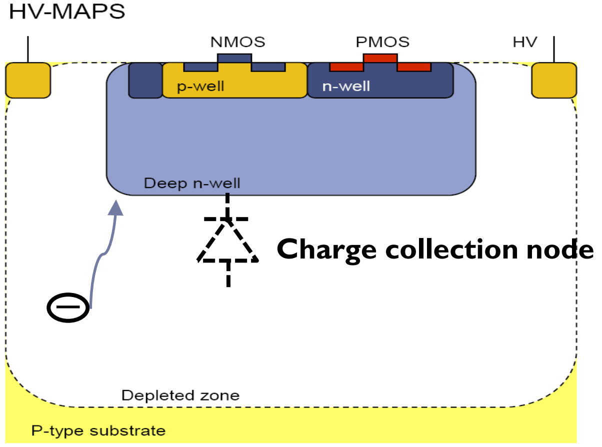
LHCb UP： 4 layers of endcap

- **Time resolution: ~ 3 — 5 ns for precise** tagging of bunch crossing (~23 ns for CEPC, 25ns for LHCb);
- **Spatial resolution:** Spatial resolution: **~8 µm** in the R-φ (bending) direction for CEPC, with less stringent requirements for LHCb;
- **Power dissipation: < 200 mW/cm^2 ;**
- **Max hit rate: ~100 MHz/cm^2 for LHCb UP；**
- **Radiation tolerance: 250 Mrad & $4\times10^{15}n_{eq}/cm^2$；**
- **Sensor thickness： < 200** µm;

HV-CMOS Pixel Sensor： a promising candidate for both applications

Target specifications for design

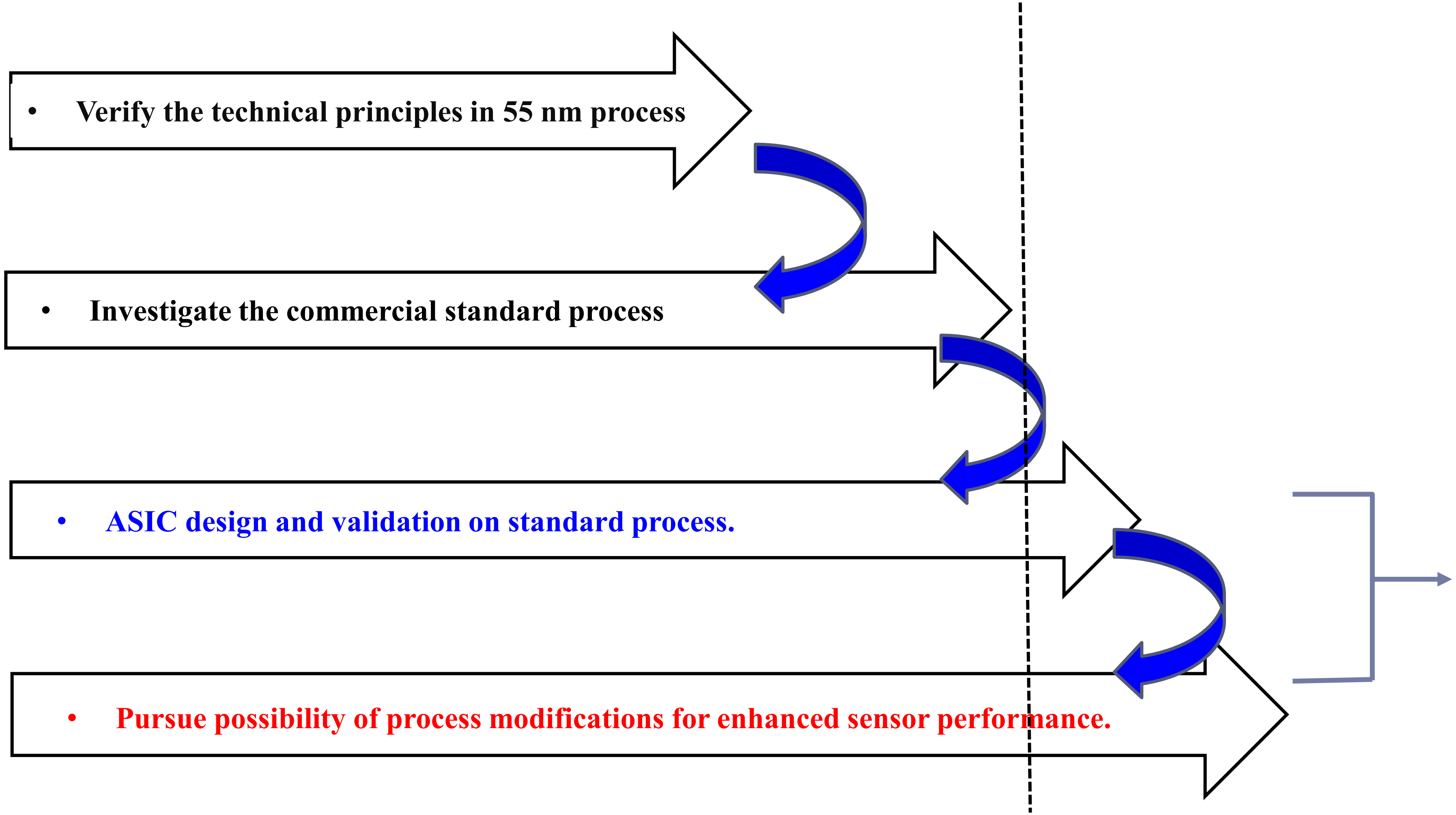
Performance Metrics	Sensor Design Specifications
Time resolution	~3–5 ns
Spatial resolution (Pixel size)	~ 30 μm × 150 μm
Power dissipation	< 200 mW/cm²
Max hit rate	~100 MHz/cm²
Radiation tolerance	250 Mrad & 4×10¹⁵ neq/cm²
Sensor thickness	< 200 μm
Sensor dimension	~2cm×2cm， ~90% sensitive area



Cross-section of a typical HV-CMOS pixel sensor.

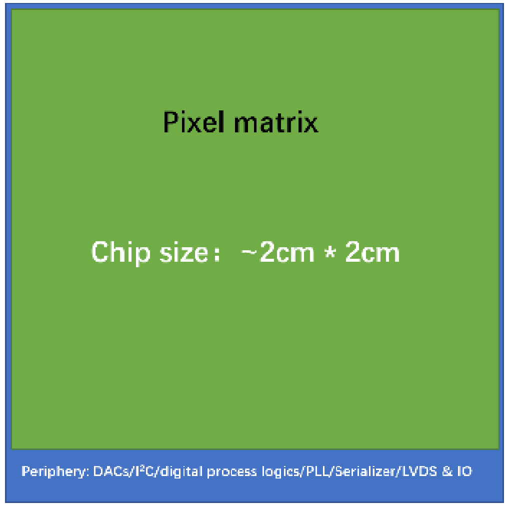
- The sensor can be fully depleted, featuring fast signal collection and good radiation tolerance.
- Since this technology was first developed in the early 2000s. A wide range of chips have been designed, exhibiting outstanding performance. Such as ATLASPix， MuPix， LF-MonoPix， RD50-MPW series , RadPix， MightyPix …….. (All fabricated using the 180 nm/150 nm process).
- Starting from the 55 nm process, we intend to meet the overall performance demands of both applications, while expanding available MAPS process possibilities for the high-energy physics community.

Main Tasks Carried Out in Parallel



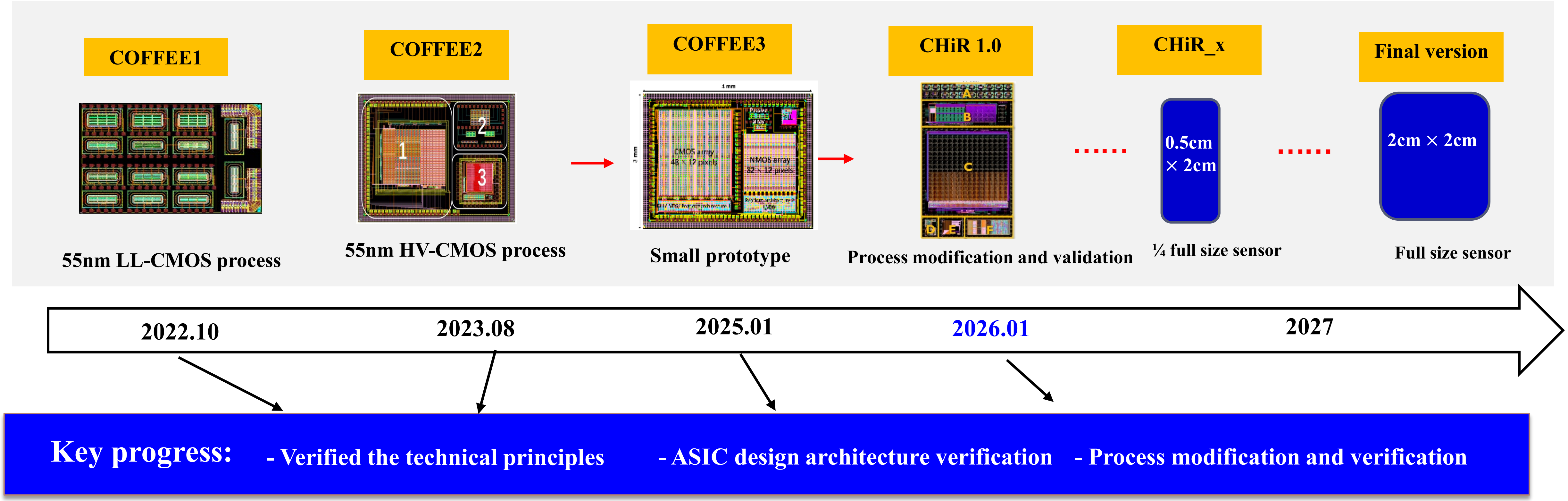
- **Verify the technical principles in 55 nm process**
- **Investigate the commercial standard process**
- **ASIC design and validation on standard process.**
- **Pursue possibility of process modifications for enhanced sensor performance.**

Now we are here



Performance Optimization Combining modified Process and Validated ASIC.

COFFEE Series Development Roadmap



COFFEE1
55nm LL-CMOS process

COFFEE2
55nm HV-CMOS process

COFFEE3
Small prototype

CHiR 1.0
Process modification and validation

……

CHiR_x
0.5cm × 2cm
¼ full size sensor

……

Final version
2cm × 2cm
Full size sensor

2022.10
2023.08
2025.01
2026.01
2027

Key progress: - Verified the technical principles - ASIC design architecture verification - Process modification and verification

Design Overview of COFFEE2

Three independent regions in COFFEE2：

1. **Passive diode arrays：**
   - Various sensing structures: DNW size, distances, with/without P-stop；

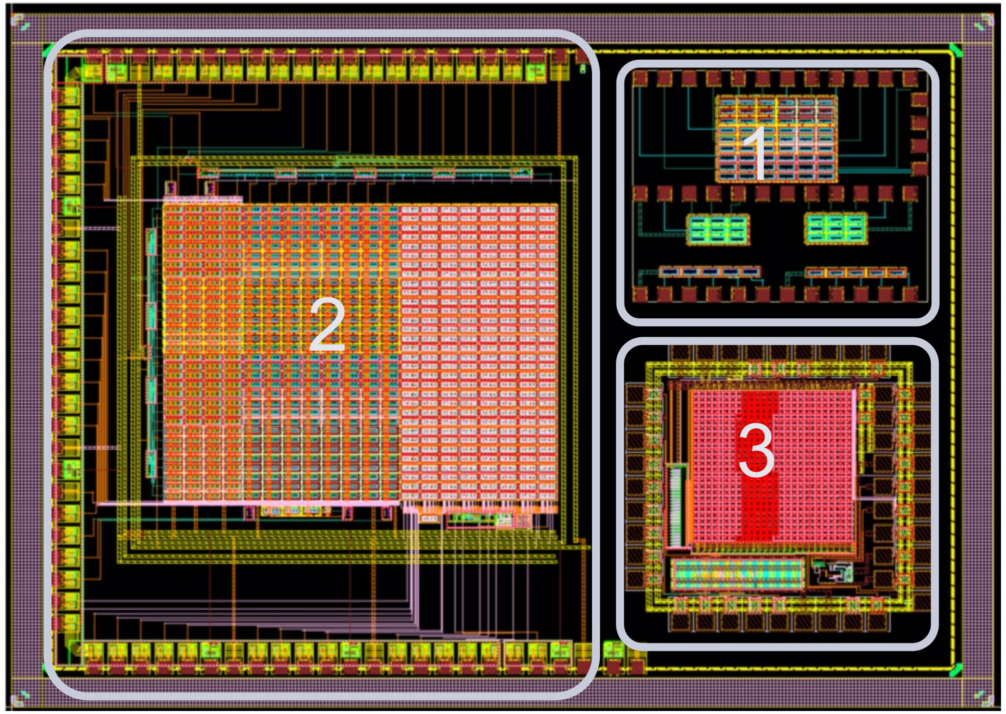
For the commercial process characteristics study

2. **An active pixel matrix including 3 variations of pixel design：**
   - To quantitatively evaluate the "cross-talk" issue of HV-CMOS pixel sensor technology in the new process and guide the overall design of the future detector chip

For charge sensing diode + in-pixel AFE study

3. **An active pixel matrix with a new readout architecture：**
   - Very small pixel size 25×25μm^2 (for a HV-CMOS pixel sensor)；
   - New matrix readout architecture；
   - Digital peripheral data processing included；

For new architectures in 55nm process @ Designed by KIT



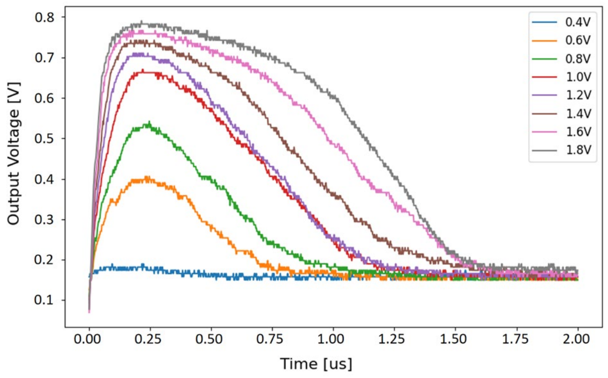
The COFFEE2 design includes three independent regions.

Published paper: 1. NIMA Volume 1069 P169905 (2024) https://doi.org/10.1016/j.nima.2024.169905;
2. 2025 JINST 20 C03023 . https://doi.org/10.1088/1748-0221/20/03/C03023;
3. 2025 JINST 20 C10011. https://doi.org/10.1088/1748-0221/20/10/C10011;

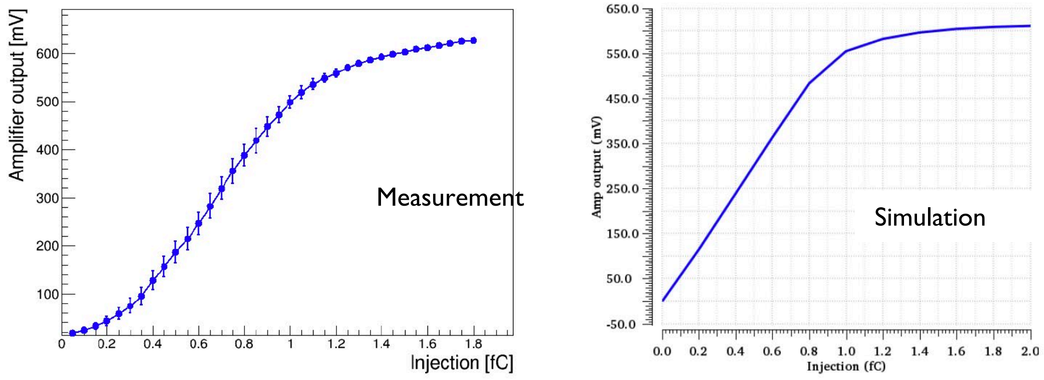
Investigation of the Commercial Standard Process: results from COFFEE2

CMOS SENSOR IN FIFTY-FIVE NM PROCESS

➢ The in-pixel amplifier & comparators work as the simulation predicts

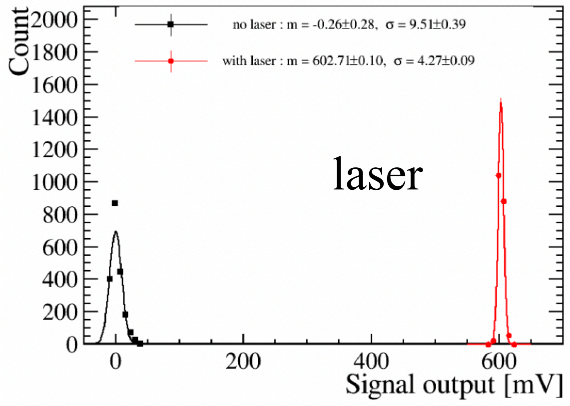


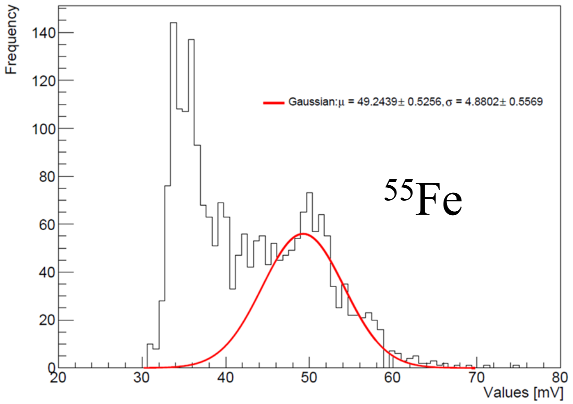
The CSA output versus different injection voltages

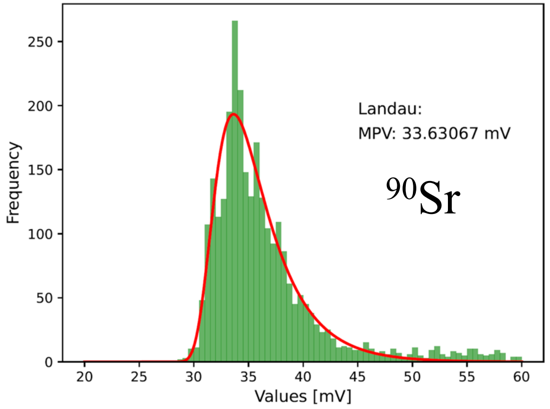


CSA output as function of charge injection

➢ Clear response to laser/ ^{55}Fe / ^{90}Sr sources: depleted depth ~ 10 µm @ sensor bias -30V

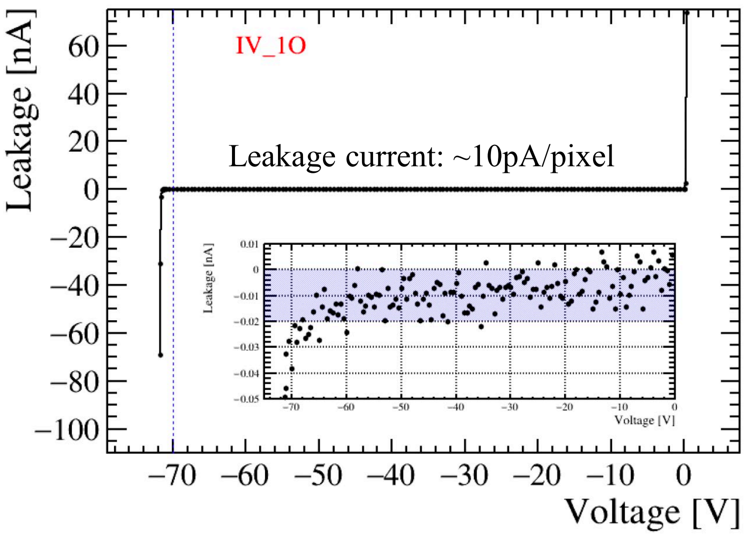






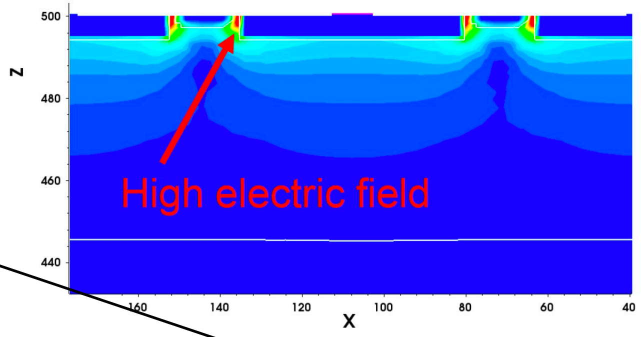
Investigation of the Commercial Standard Process: results from COFFEE2

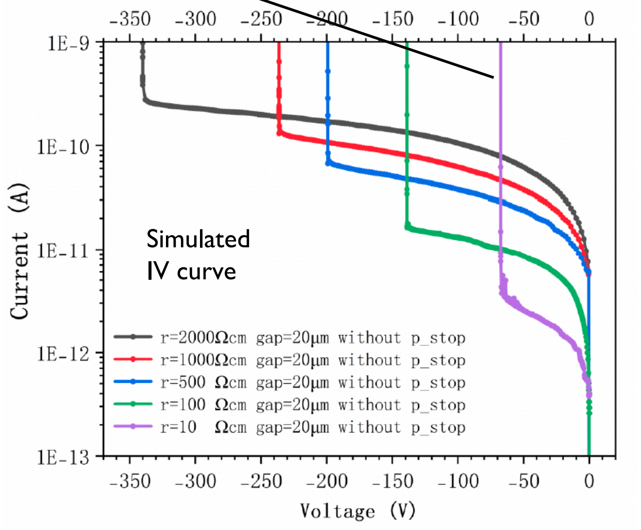
- **Breakdown voltage： ~ -70V for regular resistivity wafer (10 Ω·cm).**



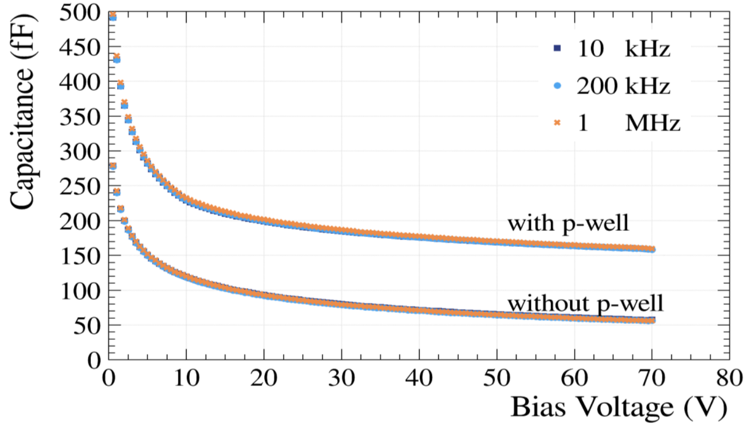
IV curve test result

Breakdown takes place between DNW and p-type surface. **Lowering p-type concentration at DNW edge (using high-resistivity wafers) improves breakdown voltage.**





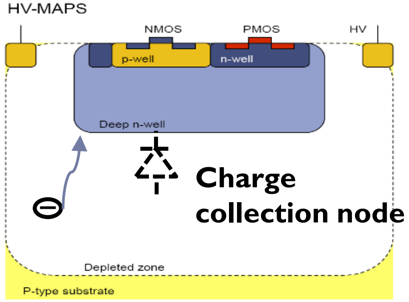
TCAD simulation



CV test results of a pixel with or without P-well inside.

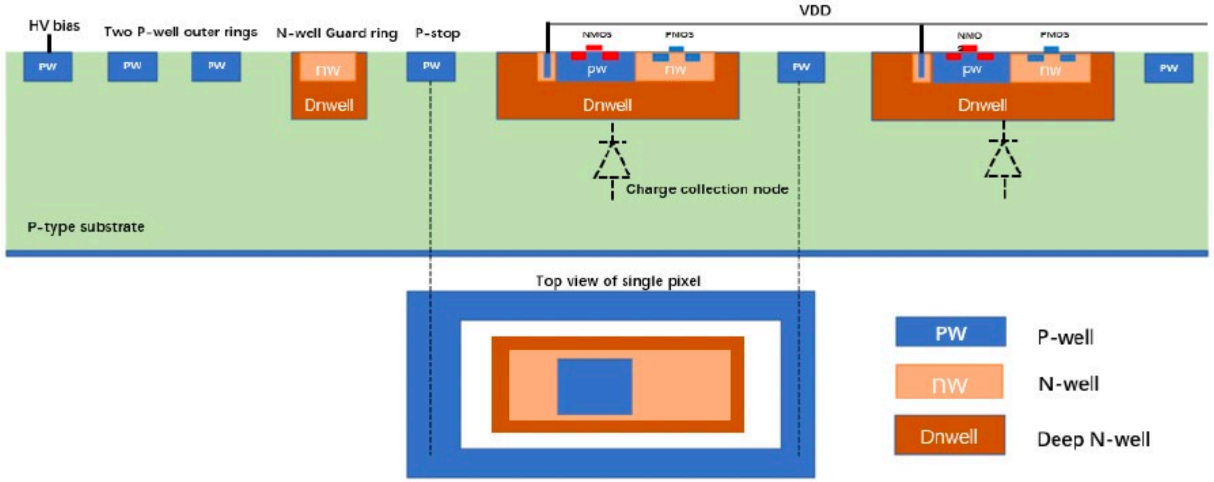
Pixel layout size:40×145 μm^2

P-WELL inside version cover ~50% area of the pixel



- **C_{diode} is ~ 200 fF, dominated by P-well-to-DNW capacitance.**

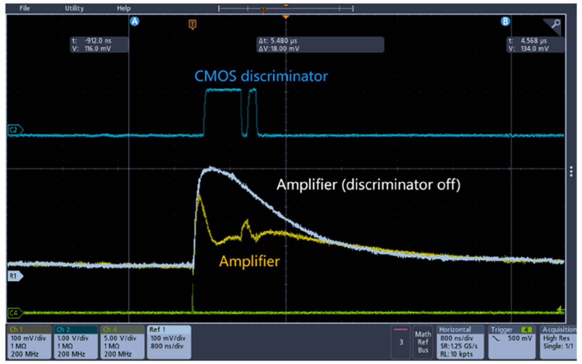
Investigation of the Commercial Standard Process: results from COFFEE2



- ➢ Process limitation: in-pixel design

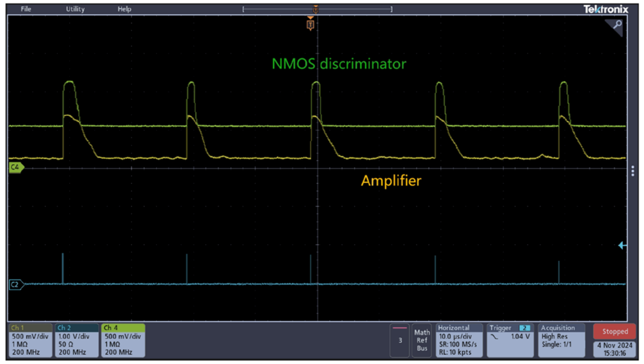
In-pixel digital signal may cause parasitic charge injection throw NW into sensing DNW. (cross-talk)

In-pixel CMOS comparator design



(a)

In-pixel NMOS comparator design

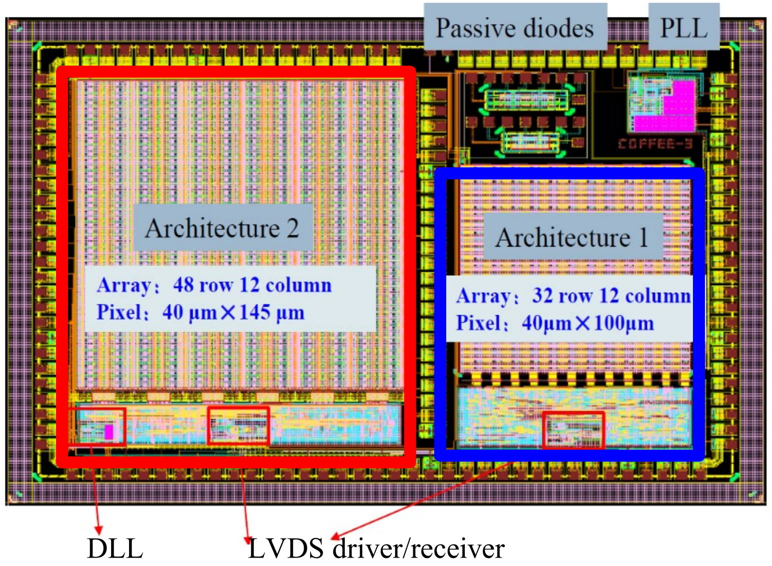


(b)

Test results of cross-talk issue:

- (a) CSA output when the CMOS discriminator on (yellow) and off (white) with the corresponding CMOS discriminator output (blue);
- (b) CSA output (yellow) when the NMOS discriminator on (green).

Layout and Targets of COFFEE3



COFFEE3 layout，3×4 mm^2.

- ➢ **Architecture 1：In-pixel NMOS design to avoid cross-talk risk.**
- ➢ **Architecture 2：In-pixel CMOS design for Potential Future Process Modifications**

Main design:

- ➢ **Two independent readout architecture**, both could be scaled to large sensor (~2×2 cm^2);
- ➢ Necessary digital and analogue Peripheral Function Modules;

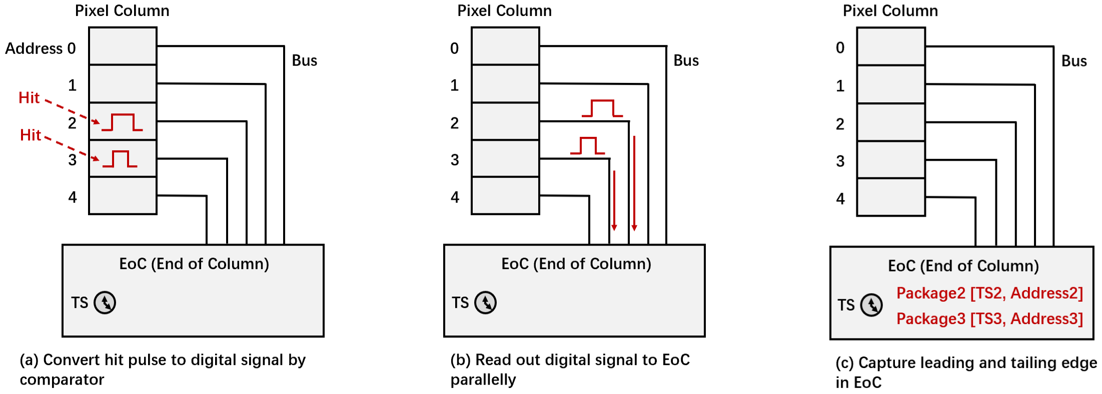
To answer:

1. **If it possible to meet**（**Time resolution** ~ ns；**Spatial resolution** ~10 μm; **Hit rate** ~ 100MHz/cm^2, **Power dissipation** < 200mW/cm^2） **at the same time?**
2. **What's more can 55 nm process bring to HV-MAPS?**

Readout Architectures

Architecture 1： In-pixel NMOS design, after digitization, each pixel data is transmitted in parallel to the bottom of the array, where time stamps are added.

Architecture 2： employs a TDC within each pixel. Particle hit information (arrival time, end time) is recorded locally in each pixel and then read out to the bottom of the array in priority order.

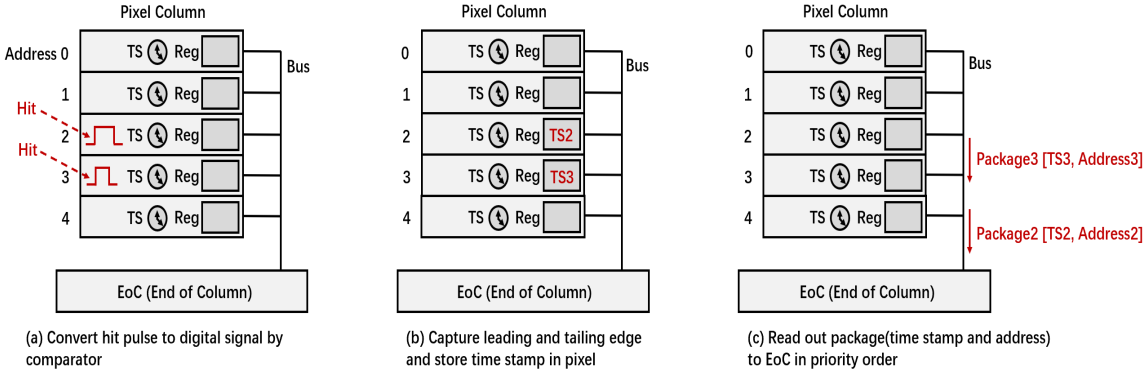


(a) Convert hit pulse to digital signal by comparator

(b) Read out digital signal to EoC parallelly

(c) Capture leading and tailing edge in EoC

Readout concept of Architecture 1, similar with ATLASPix, MightyPix, MuPix, etc



(a) Convert hit pulse to digital signal by comparator

(b) Capture leading and tailing edge and store time stamp in pixel

(c) Read out package(time stamp and address) to EoC in priority order

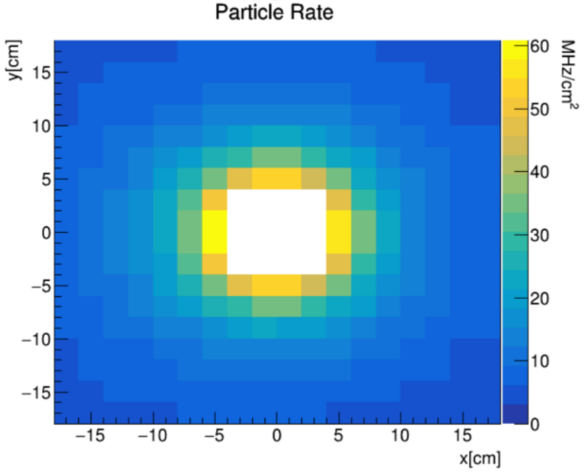
Readout concept of Architecture 2, similar with RadPix, MonoPix, Timepix (hybrid), etc.

Targets:

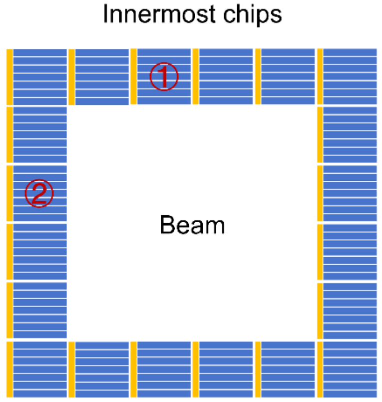
- *Potential for Low power consumption* or *high position accuracy*

- *More possibilities & High hit density processing capability*

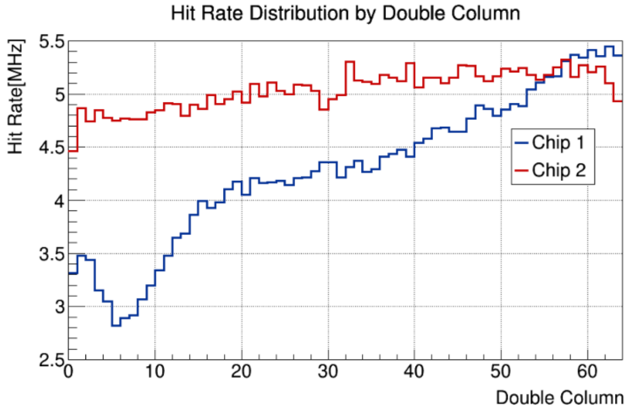
Design Specifications: **Chip System-Level Simulation**



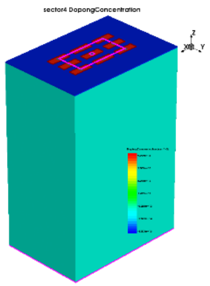
50 000 Bunch crossing physics simulation data at LHCb UP for future LHC upgrades.



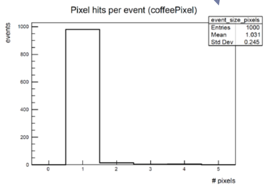
The final chip arrangement on the detector.



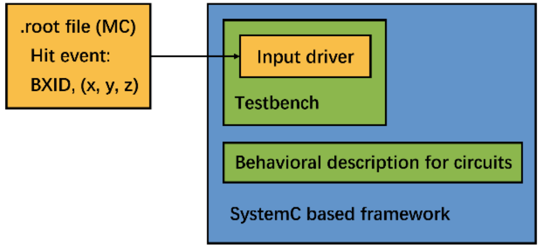
Hit-rate Variation of Pixels Inside Extreme-Position Chips



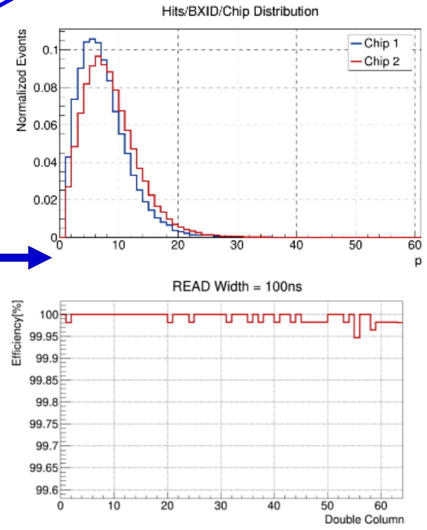
Electric field conditions obtained from TCAD.



Signal collection information provided by Allpix².



System C based ASIC behavioral description framework, to guarantee >99% detection efficiency.

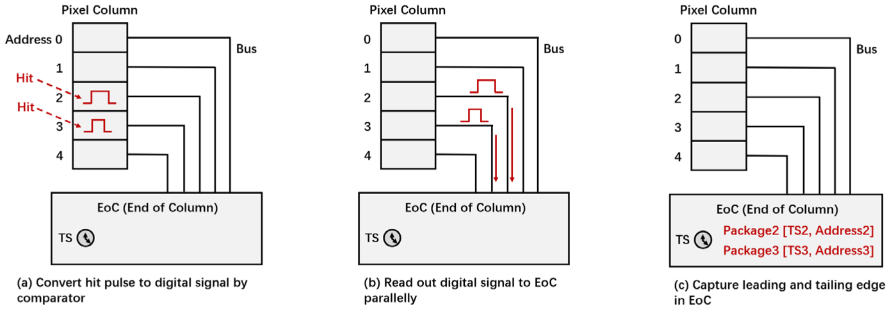


- **Analogue pile-up**: Analogue signal width;
- **Digital pile-up**: Data processing speed and FIFO depth;
- **Output Link Num. and speed and on chip Data Compression Algorithm**;

……

Architecture 1: design for Higher Hit Density Processing Capability

Architecture 1: Pixel Hit Parallel Transmission to Array Bottom

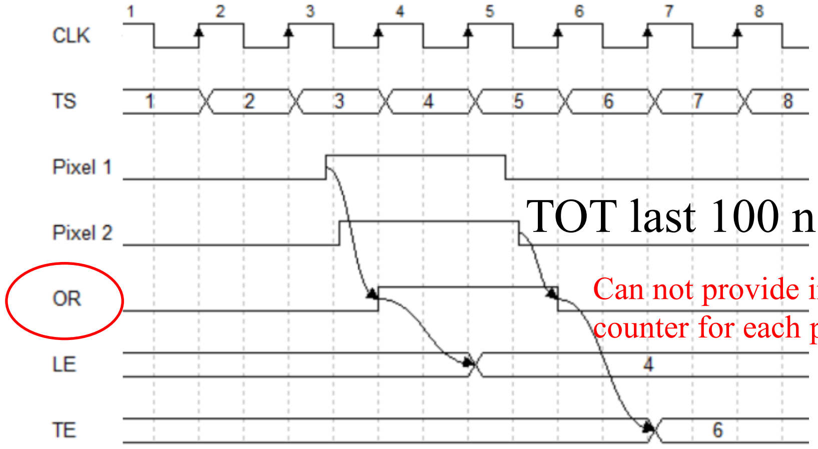


(a) Convert hit pulse to digital signal by comparator

(b) Read out digital signal to EoC parallelly

(c) Capture leading and tailing edge in EoC

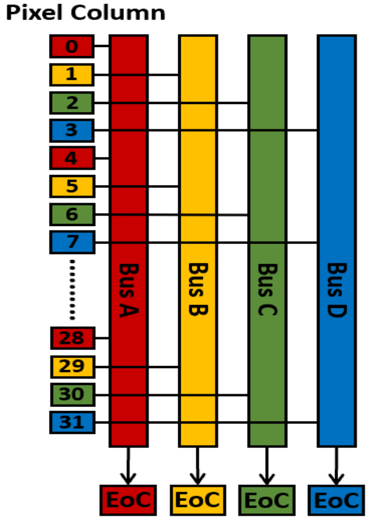
Each column shares an EoC module



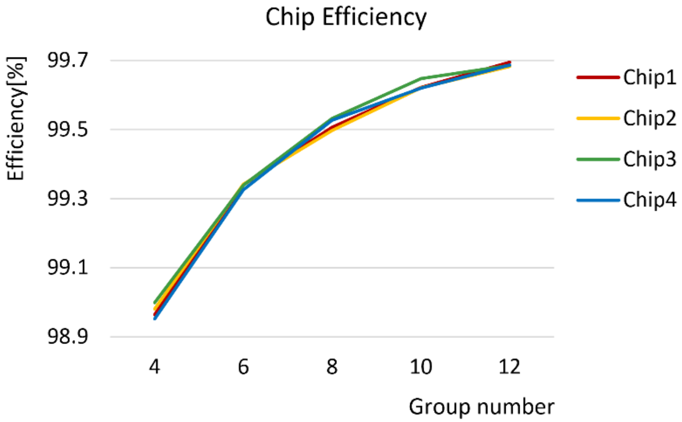
TOT last 100 ns -1.6 µs

Can not provide independent time stamp counter for each pixel at EoC

- This concept with 1 EoC for each column, while hit density increase, the timestamp information maybe inaccurate.



One pixel column architecture in COFFEE3.

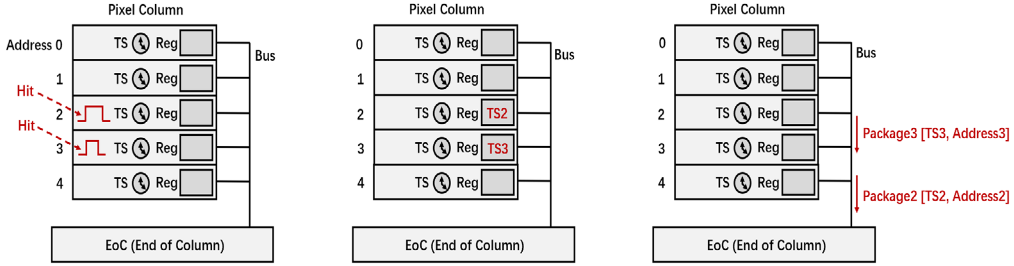


At UP extreme positions, digital logic induced efficiency loss is ~1%.

- **Limitation: while hit density increase (eg. > several tens of Mhz/cm^2)**
  - **Timestamp information inaccurate;**
  - **Efficiency loss;**
- **To handle higher hit rates: 4 EoC modules for each column, and two FSMs for each Eoc in COFFEE3.** The area of the peripheral digital circuits does not significantly increase (still much less than 10% of the whole sensor).

Architecture 2: for more possibilities & High hit density processing capability

Architecture 2: the event time information are **recorded within each pixel**. Then read out to the bottom of the array in order of priority (Efficiency > 99.9% @ UP while READ ⩽ 100 ns).

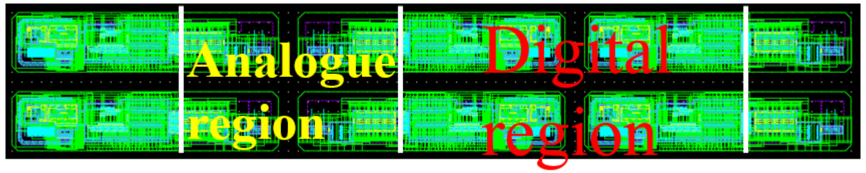


(a) Convert hit pulse to digital signal by comparator

(b) Capture leading and tailing edge and store time stamp in pixel

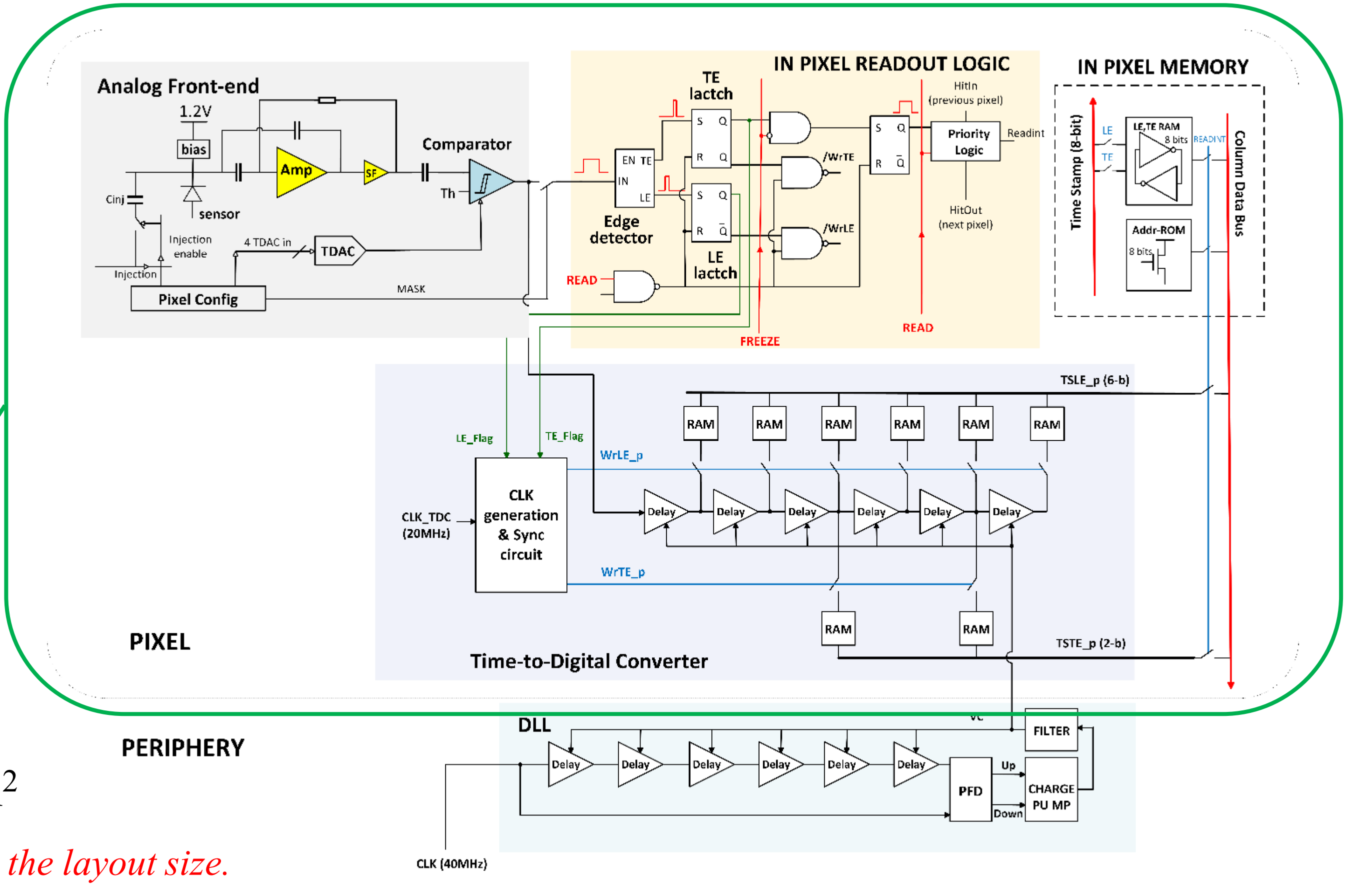
(c) Read out package(time stamp and address) to EoC in priority order

No limitations like Architecture 1, time information is accurate.



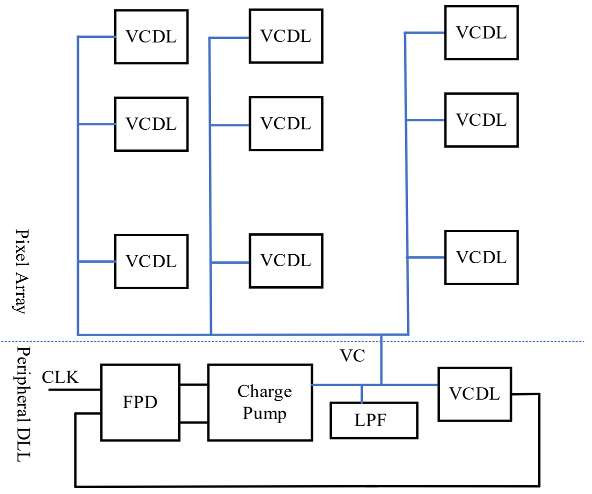
Layout of 2×3 pixels, signal pixel size is 40×145 μm^2

**The actual manufacturing size will be scaled down to 0.9 times the layout size.*

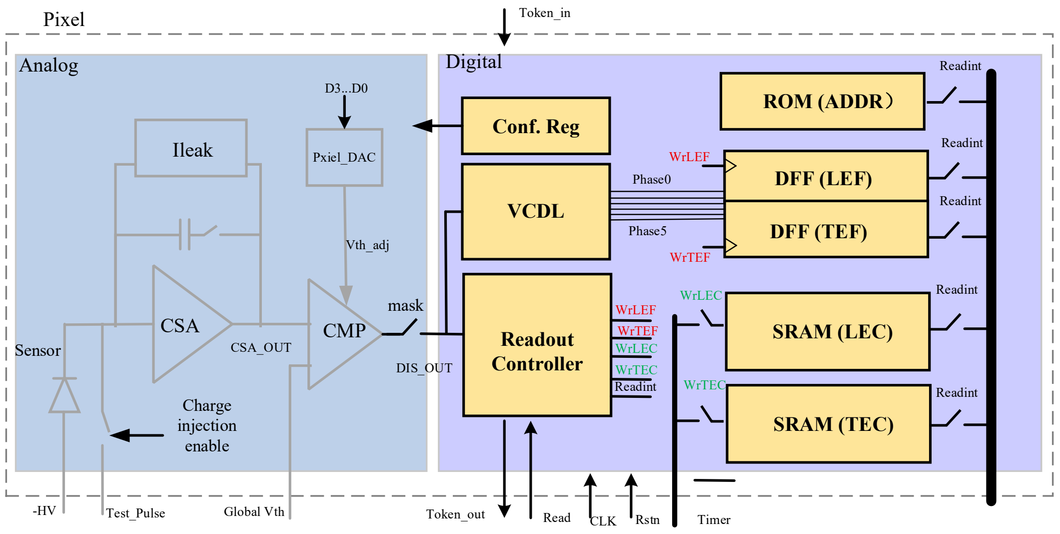


- More integration in-pixel: The analog front-end, comparators, in-pixel DACs, priority readout structure, memories, and TDCs have all been integrated within a limited pixel area. This further enhances the capability of HV-MAPS to provide high-precision hit information in high hit density applications.

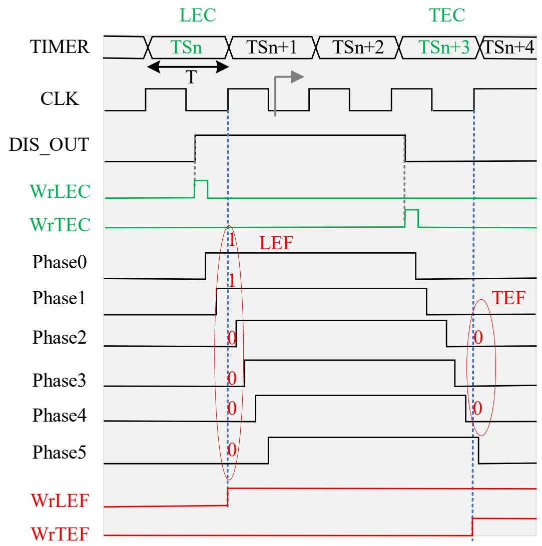
Architecture 2: Low-Power Design Considerations



Peripheral DLL and duplicated in-pixel VCDL



The comparator output is used for VCDL



6 phases are used for Leading edge and 2 of them are used for tailing edge.

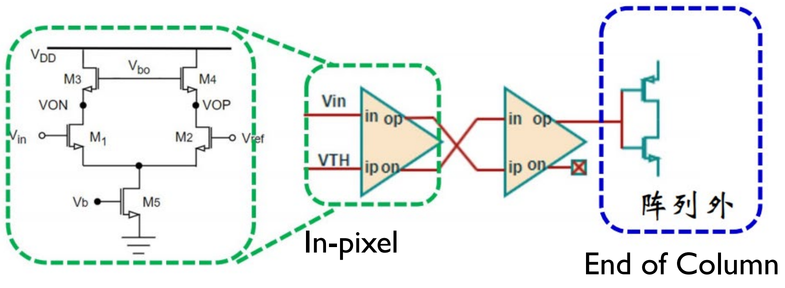
4.16ns fine timestamp for LE

Deign of in-pixel Coarse-fine TDC: for lower power dissipation

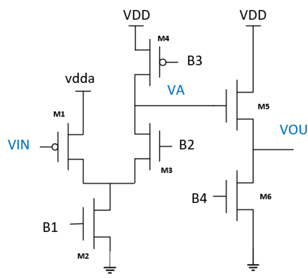
- Only a small VCDL block in-pixel (DLL is at the Peripheral);
- Almost no static power consumption for in-pixel TDC: only works while pixels are fired;
- Low power for Coarse time-stamp distribution into pixel matrix: 20 Mhz (Convert to 40 MHz, within the pixel);
- One delay line for both Leading edge and Tailing edge information.

Common design: In-pixel Analogue Front-end

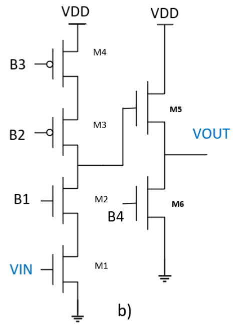
- CSA+NMOS comparator in Architecture1



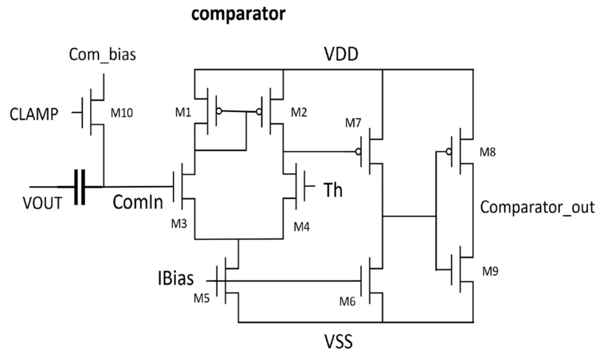
- CSA+CMOS comparator in Architecture 2



2). CSA2: fold-cascode + SF



1). CSA1: cascode + SF



Simulation based on the expectation of using high-resistivity wafers in the future.

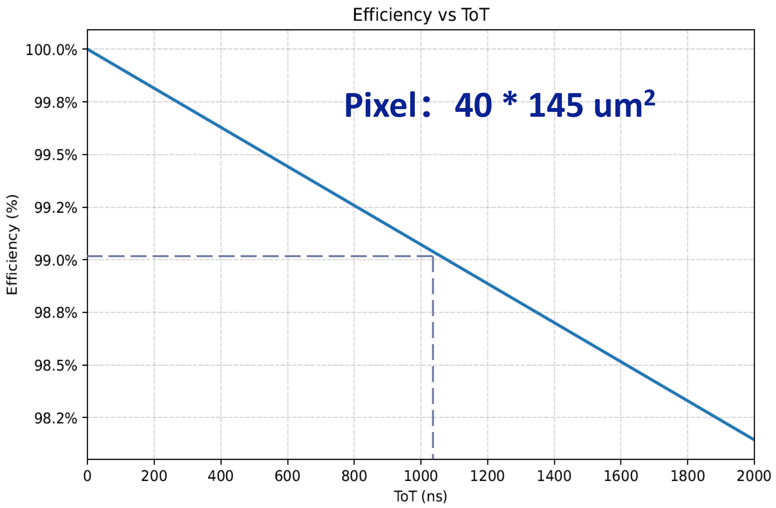
C_{diode}	~200 fF （Estimated）
Signal distribution	2k - 20ke- （Assuming high-resistivity wafer）
Threshold set	5 times of noise values

Key design performances:

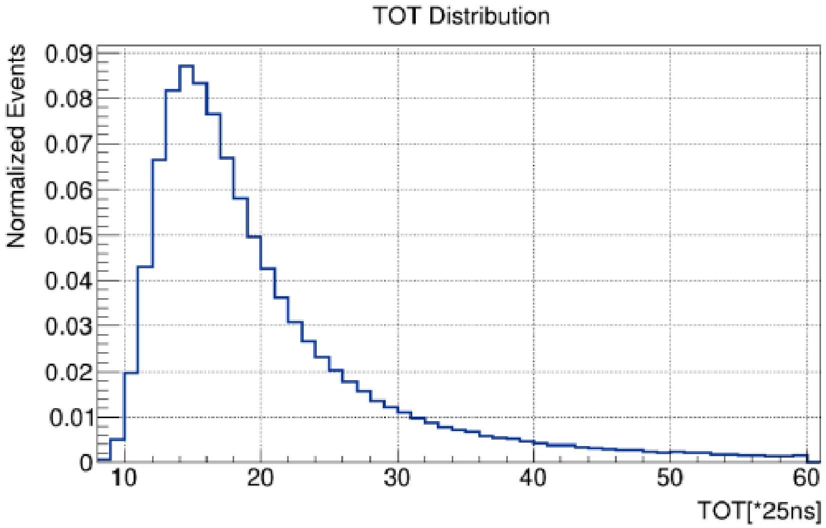
- **Response time:** one contribution to time resolution;
- **Power dissipation：** main contribution to total power;
- **Time Over Threshold：** analogue pile-ups in high hit density applications;
- **Noise：** one contribution to time resolution, also affect detection efficiency and fake hit rate;

Common design: In-pixel Analogue Front-end

◆ **Time over Threshold:**



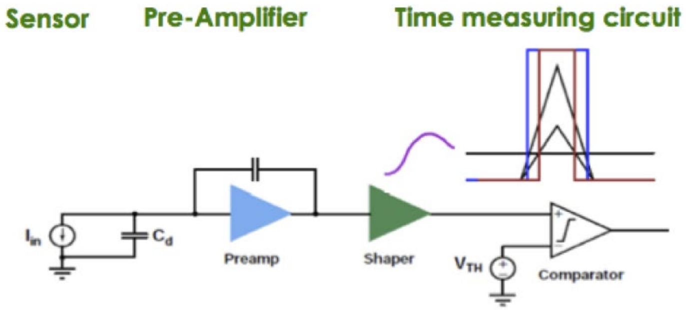
Efficiency vs ToT while the hit density @ 100 Mhz/cm^2 (only analogue part)



Simulation results of ToT distribution of a MIP in HV-CMOS pixel sensor (2ke- --> 20ke-).

The maximum ToT (for MIP) is limited to ~1μs, ensuring far less than 1% efficiency loss due to analogue pile-up while the hit density reaches 100Mhz/cm^2.

Timing Resolution Budget



Typical time measurement detector structure.

$$\sigma_{\mathrm{t}}^2 = \sigma_{\mathrm{TW}}^2 + \sigma_{\mathrm{J}}^2 + \sigma_{\mathrm{TDC}}^2 .$$

（TOT compensation not included）

Signal charge distribution、analog front-end design、 comparator threshold setting, etc.

$<（4\ \mathrm{ns}）^2$

Electronics noise、threshold inconsistency from pixel to pixel, etc.

$<（2\ \mathrm{ns}）^2$

TDC quantization noise：
Time stamp bin size/√12

$<（2\ \mathrm{ns}）^2$

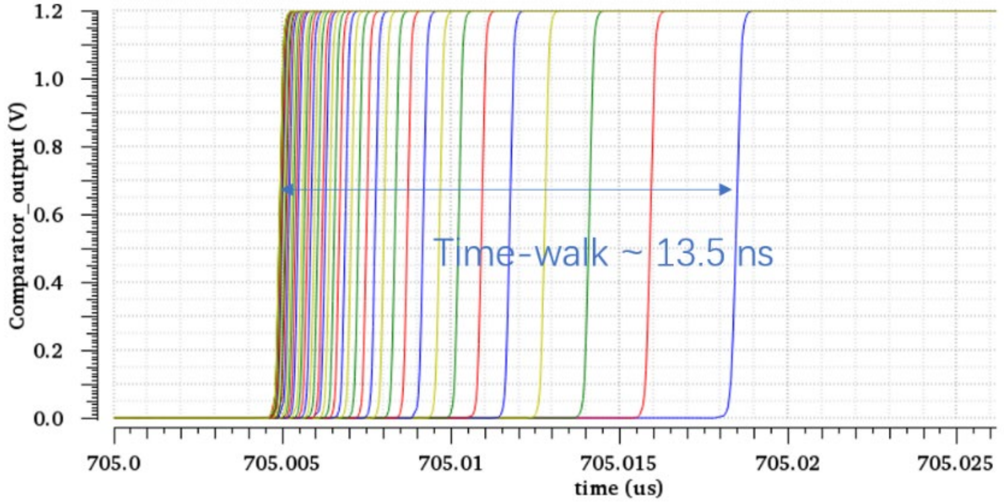
Time resolution < 5 ns

The current analysis does not incorporate TOT compensation, clock delay (~1ns, compensable), or clock jitter (ps-level) effects.

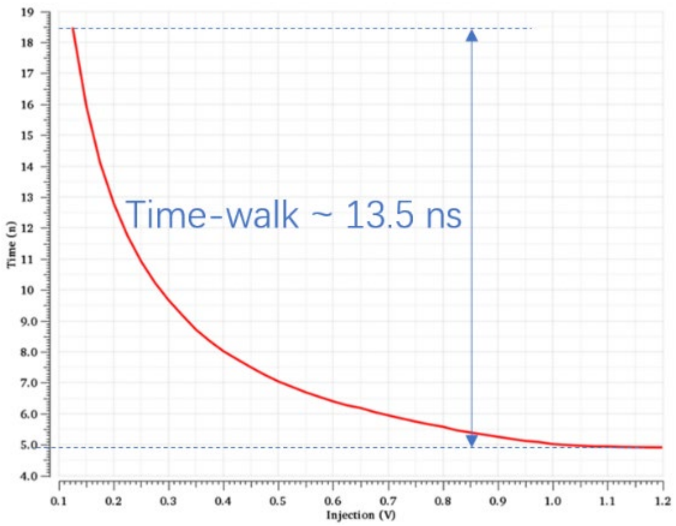
The final performance highly depends on the final process condition we could access.

Common design: In-pixel Analogue Front-end

◆ **The time-walk:** simulations for MIP in fully depleted 200 µm thick sensor.



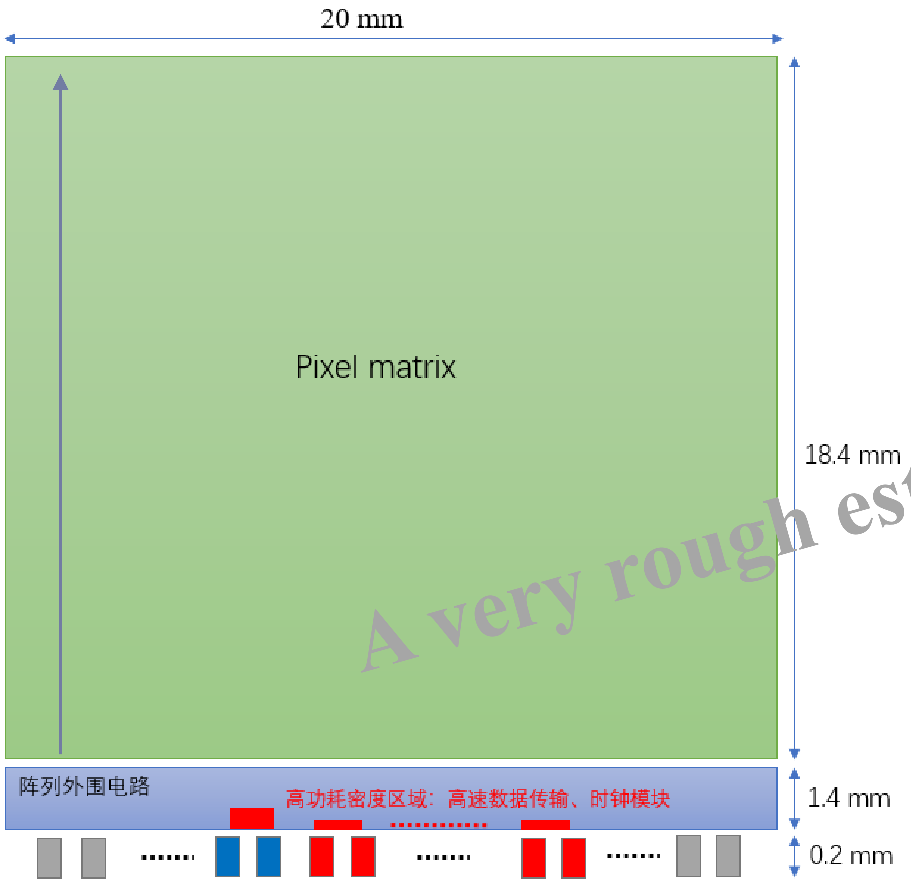
Time walk: 13.5 ns



Time of Arrive: 5 ns - > 20 ns

- **Power:** ~ 10 µW/pixel for in pixel CSA + Comparator
- **Noise:** ~120 e$^-$ (in test results section)

Preliminary Estimation of Chip Power Consumption and Area



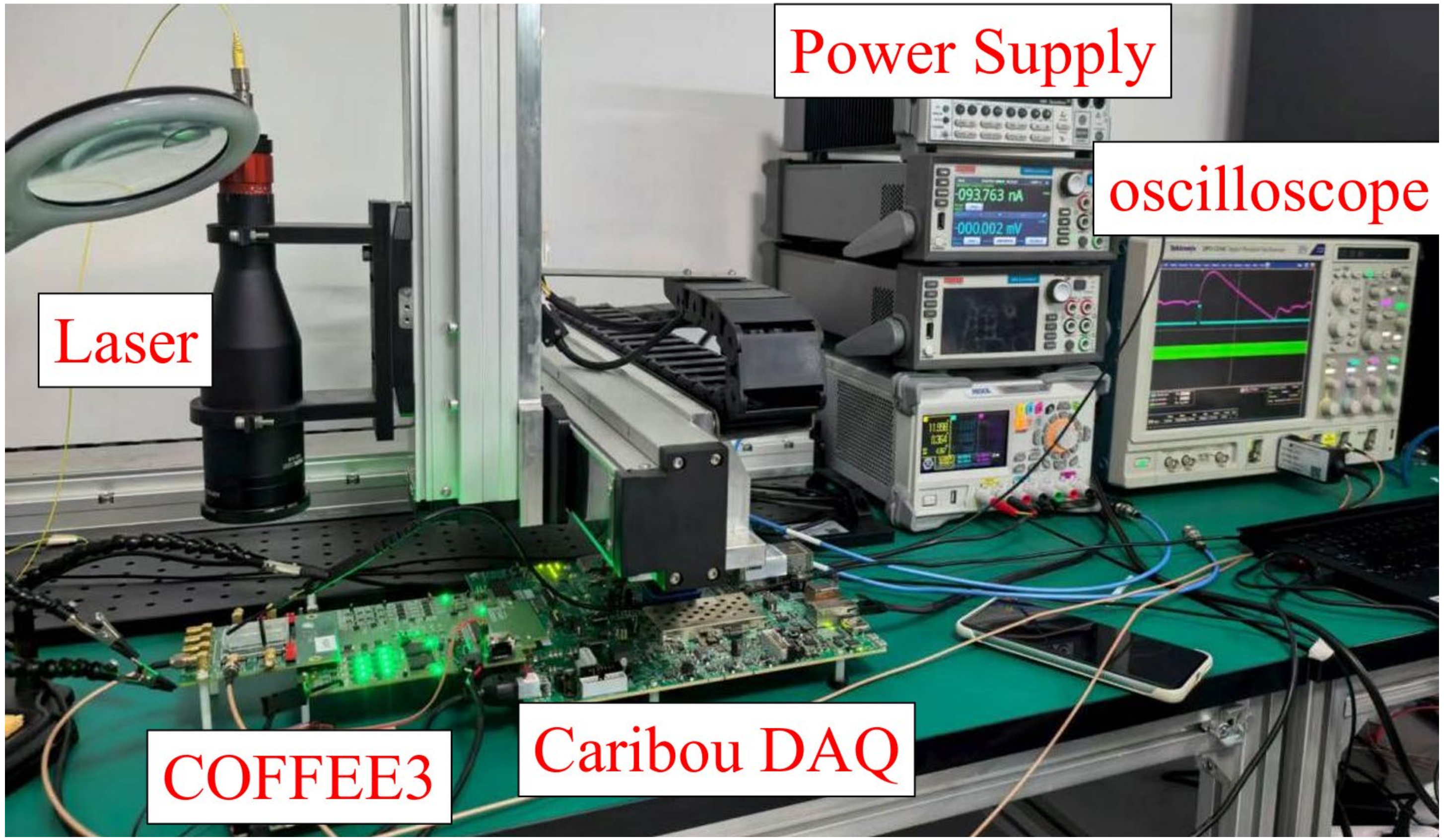
Estimated layout of a full size HV-CMOS sensor.

Estimated overall power consumption and area (based on architecture 2)

--- on the expectation of using high-resistivity wafers in the future.

	Pixel matrix	**Peripheral**	**Overall**
Area	20 × 18.4 mm^2	20 × 1.6 mm^2	20 × 20 mm^2
Total power consumption	~580 mW	~ 22 mW (may overly optimistic)	~ 602 mW
Power density	**~158 mW/cm^2**	**~123 mW/cm^2** （estimate one data Transmitter channel）	**~ 150 mW/cm^2** （hit density related dynamic power not included yet）

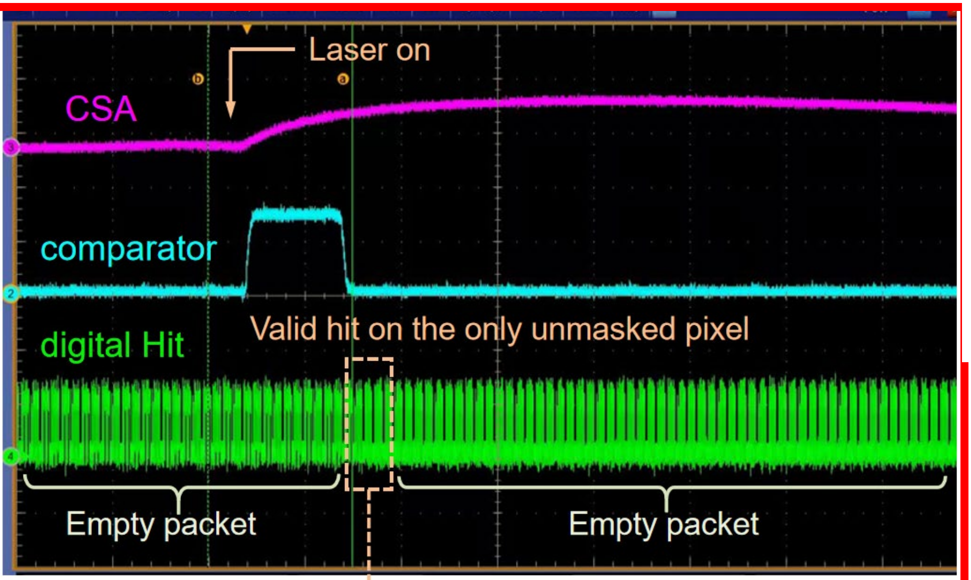
The Preliminary Test Results of COFFEE3



Response of Full Readout Chain with Laser Test

Architecture 2: in-pixel TDC

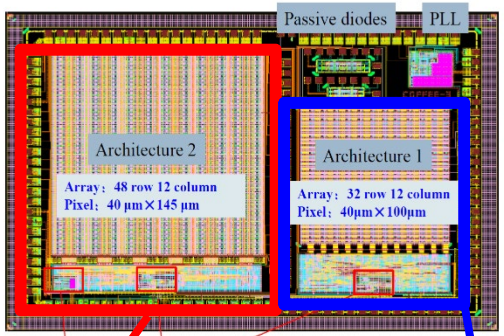
Architecture 1: in-pixel NMOS design



4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

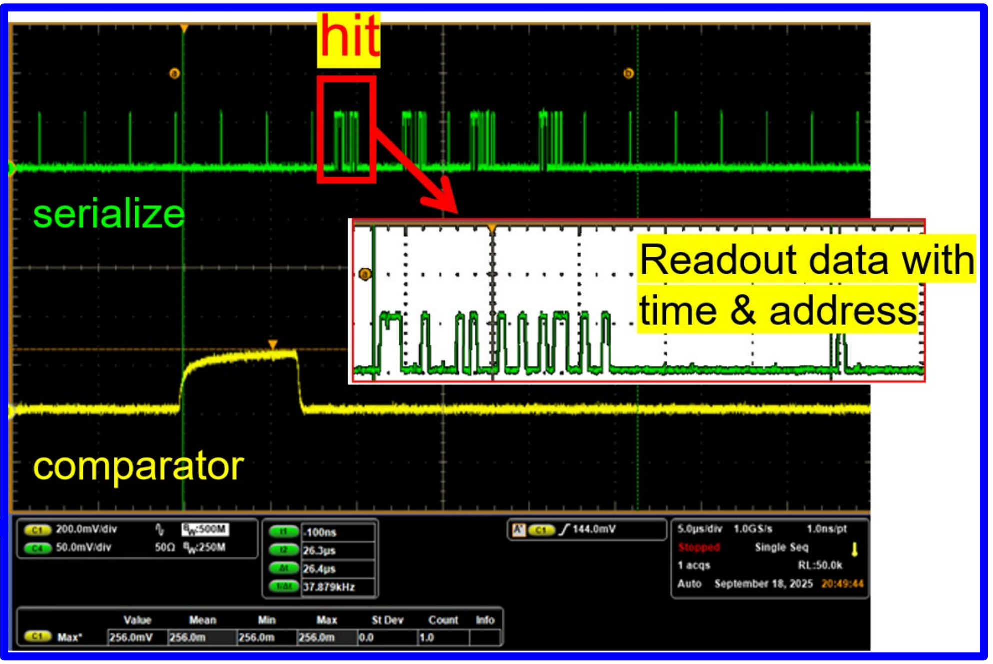
A valid transmission packet corresponding to a hit

Correct row & column address



DLL LVDS driver/receiver

Layout of COFFEE3



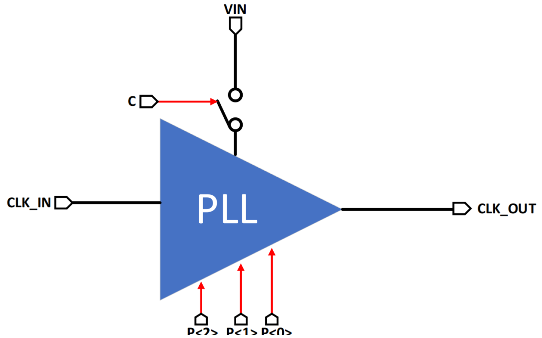
The full readout chain works for both of the two readout architectures.

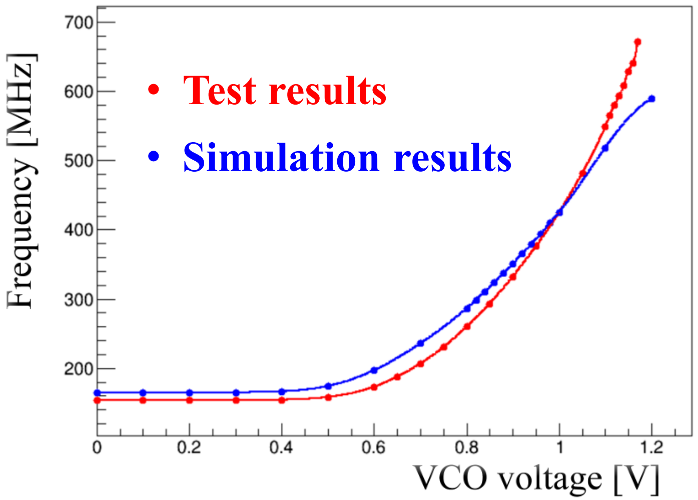
Sensing diode → in-pixel (CSA\comparator\TDC) → EOC (digital peripheral) -> data link-> DAQ

Test Results of Functional Modules

All the functional modules designed in COFFEE3 work:

- PLL works ups to 640Mhz





- LVDS driver/receiver works at 640 Mhz support 1.28 Gbps data link

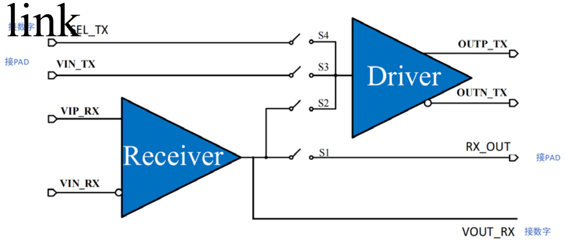
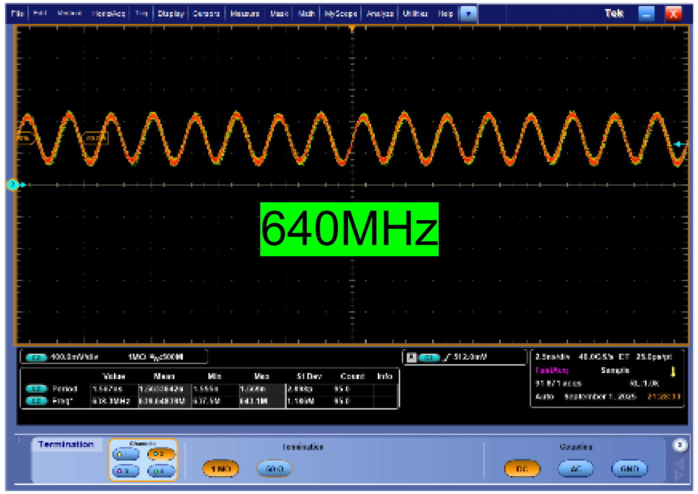
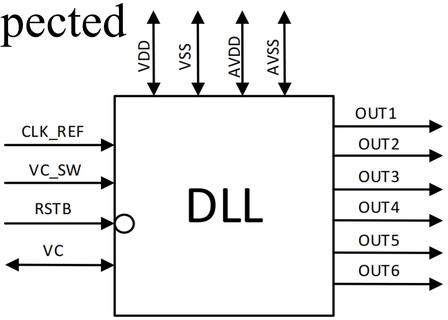


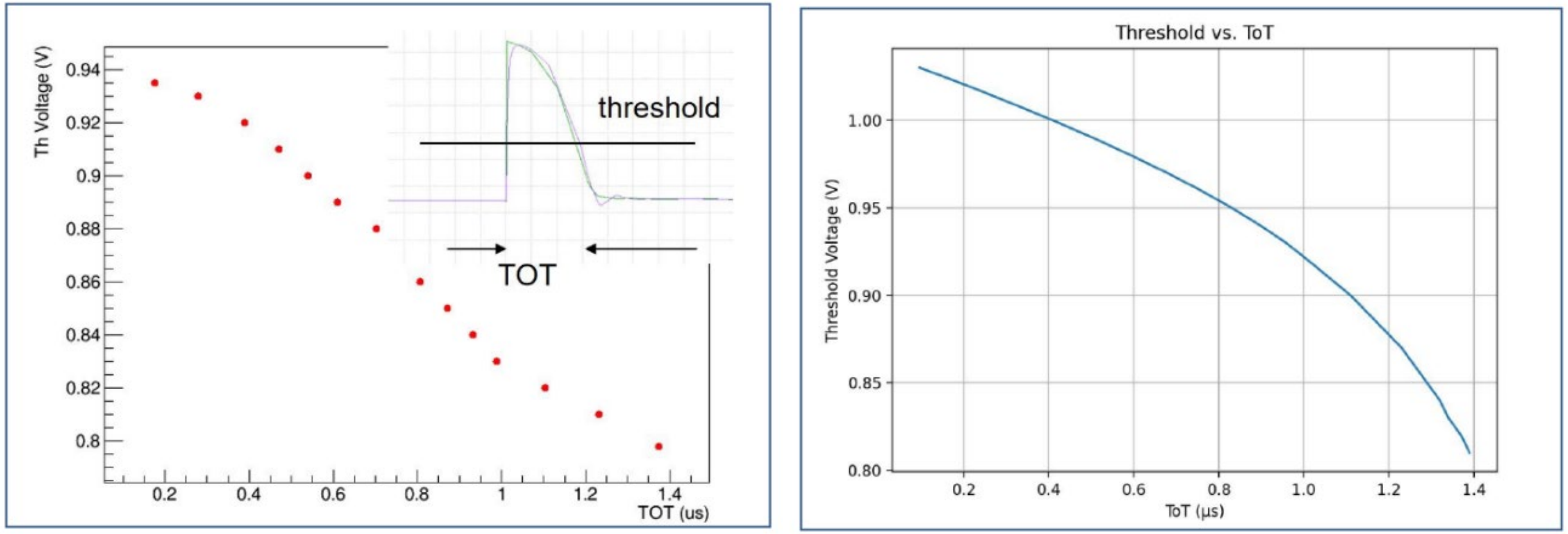
Fig 3.1.1 LVDS block diagram



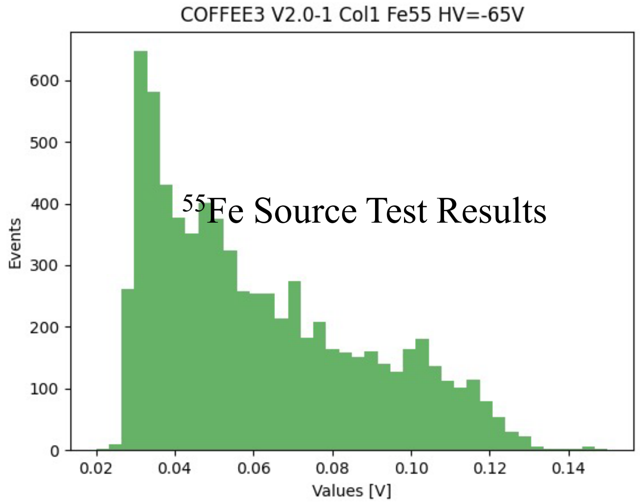
- Delay line for in-pixel TDC works as expected



In Pixel Analog Front-End Test Results



Measured TOT-threshold relationship matches simulation results.



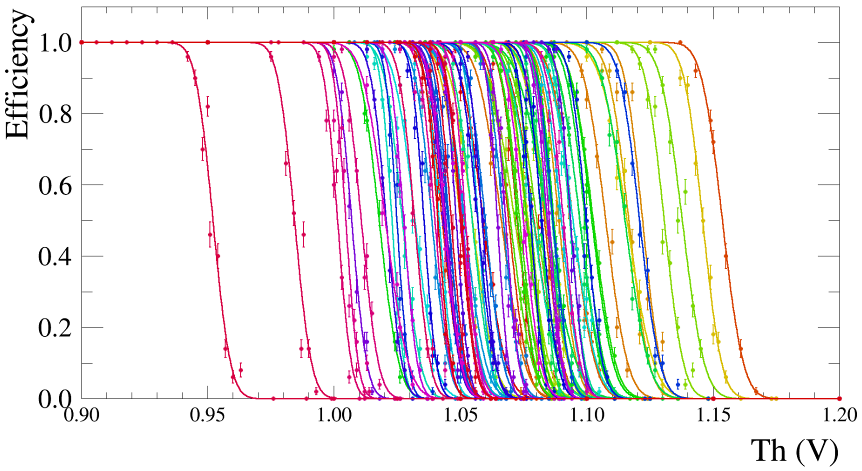
^{55}Fe Source Test Results

No significant calibration peak (1640e$^-$ for 5.9 keV X-ray) is observed.

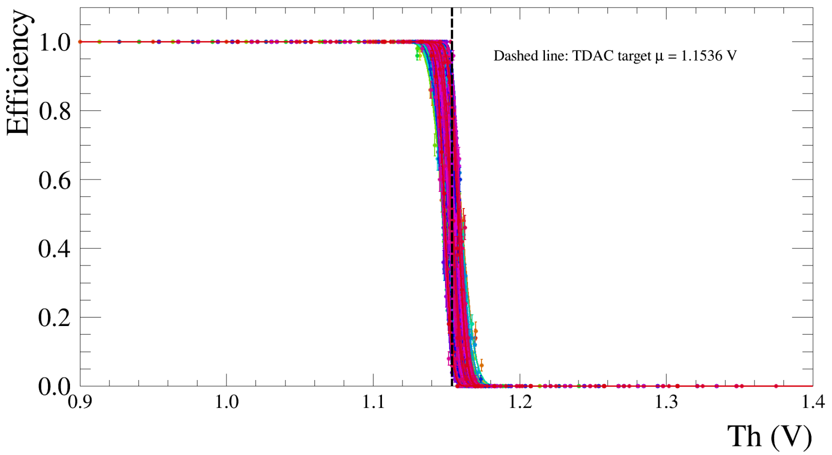
In Pixel Analog Front-End Test Results

S-curve results of the In-pixel TDC version: Each pixel integrates a 4-bit DAC for threshold tunning

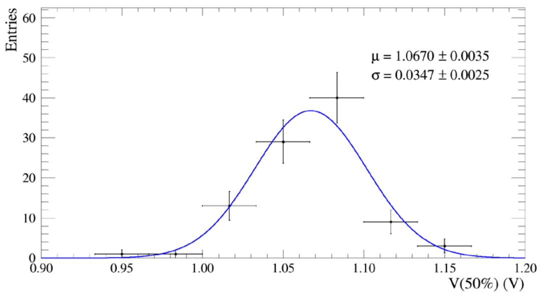
Before threshold tunning



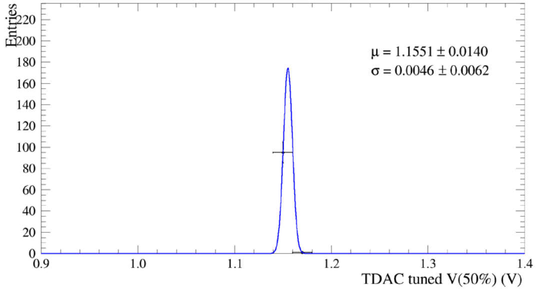
After threshold tunning



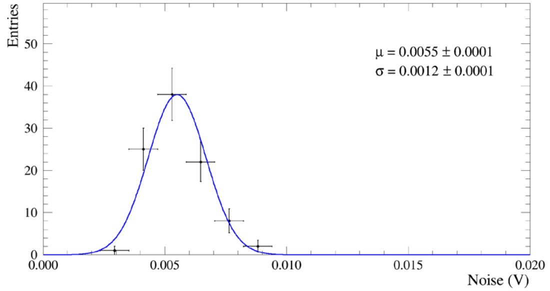
Threshold Variation Noise: 34.7mV



Threshold Variation Noise: 4.6 mV

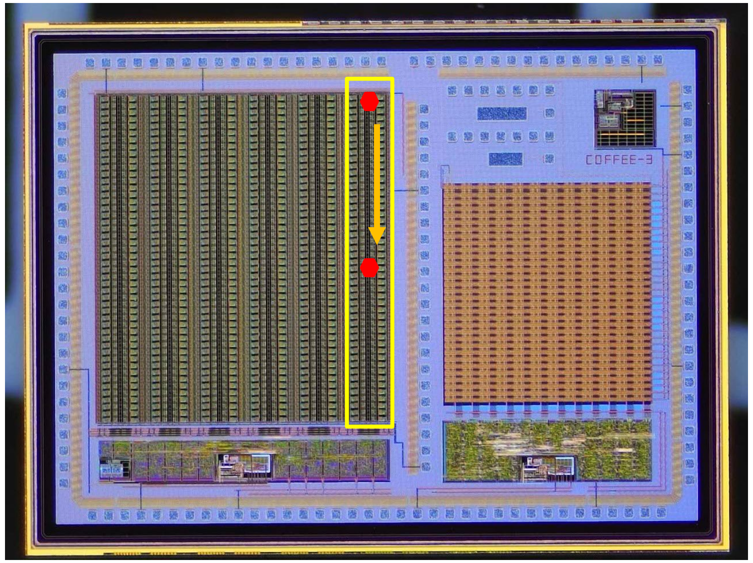


Temporal Noise:5.5 mV

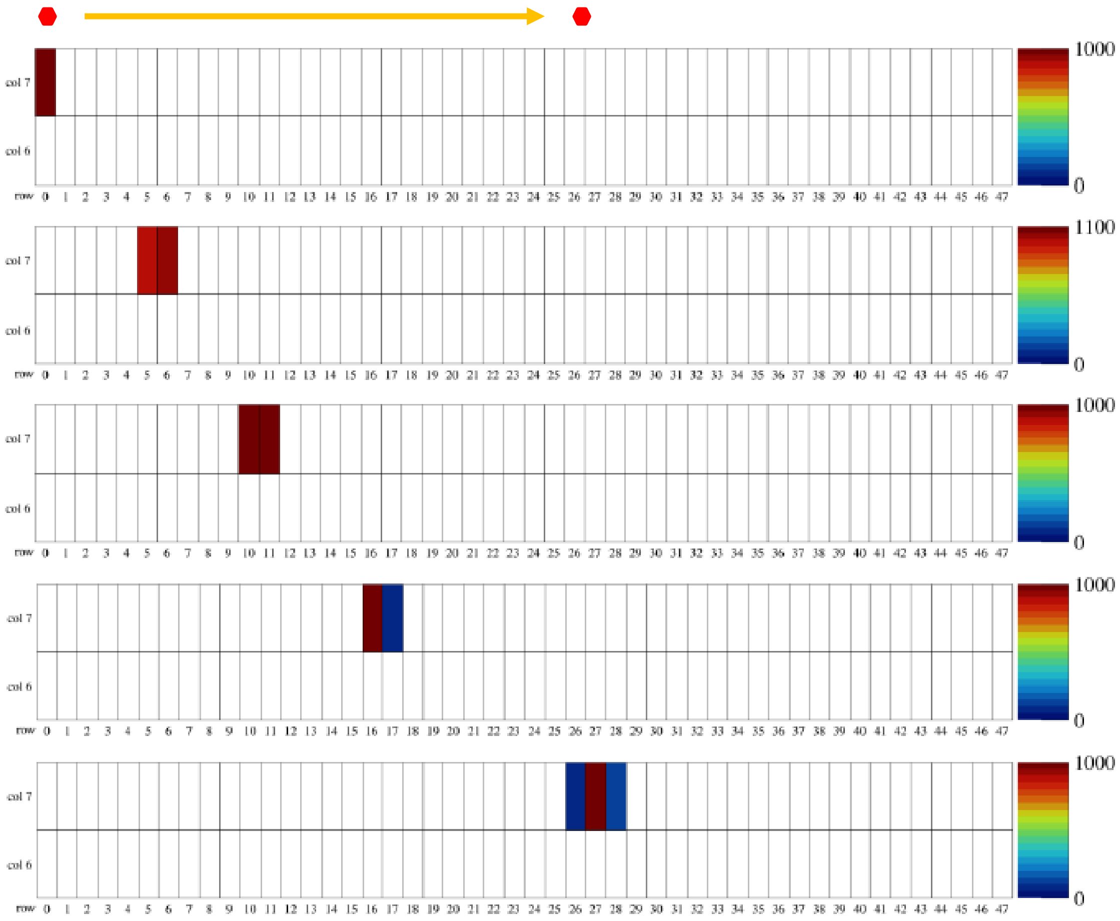


If we take 0.1V as the calibration peak of ^{55}Fe, noise after tunning would be ~ 120 e^- (results are just obtained, very preliminary and need further confirmation.)

Laser Response of Dual-Column Pixels



2column×48 rows pixel

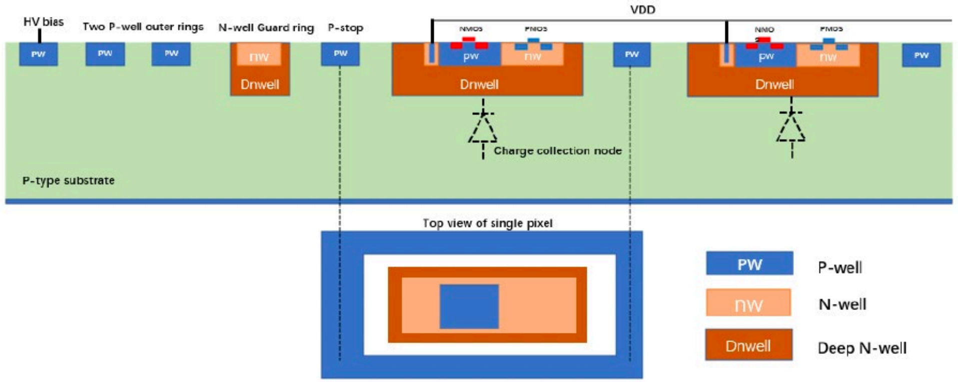


Laser response test of pixel array:

1000 laser injections per position with a 200 μm moving step, covering an equivalent pixel interval of ~5 pixels (180 μm, pixel size = 36 μm).

The preliminary test results are positive

However, standard commercial 55nm HV-CMOS process is by no means the ideal MAPS process



1. Triple-well process → cross-talk risks between sensor (deep-n) and PMOS transistors； → **Restrict the flexibility of in-pixel design;**
2. Break down at ~-70V; → **Extremely limits the SNR.**
3. No access of high-resistivity wafers;

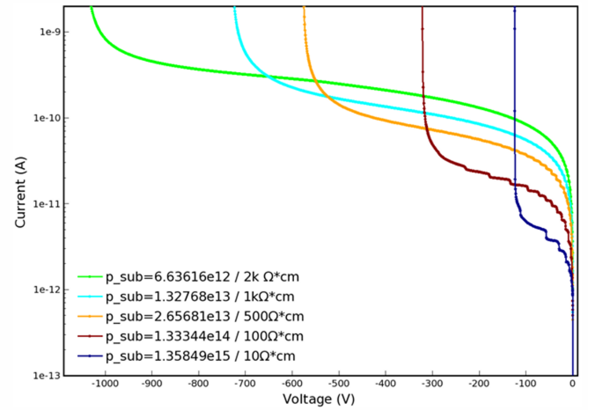
In collaboration with the Foundry, some process modifications have just been made

for better sensor performances

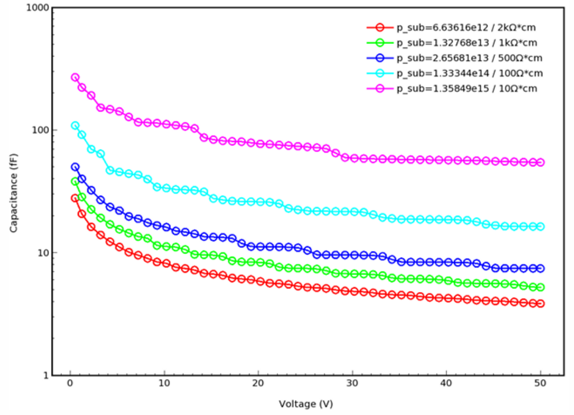
Process Modifications for better Sensor Performances

Modifications：

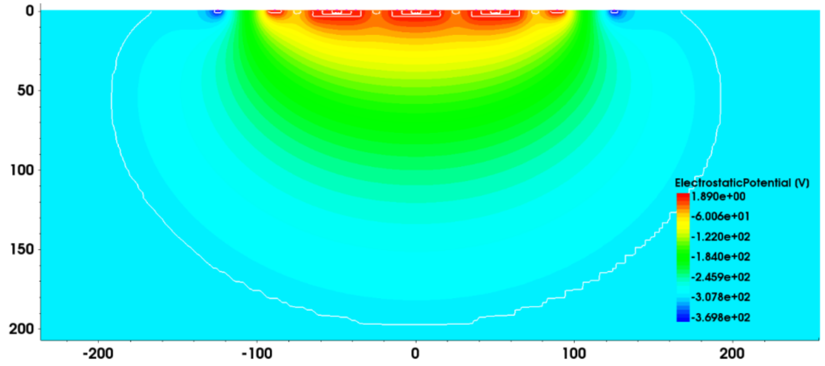
- ◆ Add layers: Deep-PW & Very-deep-NW;
- ◆ Change doping rules affecting breakdown voltage;
- ◆ Replace wafer: from 10 Ω·cm --> >1k/2k/4k Ω·cm;



- ➢ Breakdown V: **70 --> > 400V**



- ➢ Capacitance of VDNW/p-sub: **~ hundreds fF --> ~ tens of fF**



- ➢ Depletion depth: ~10 µm → >200 µm

Huge S/N gain : Signal increase >10 times, while C_{diode} reduce

First Design based on Modified Process: CHiR 1.0

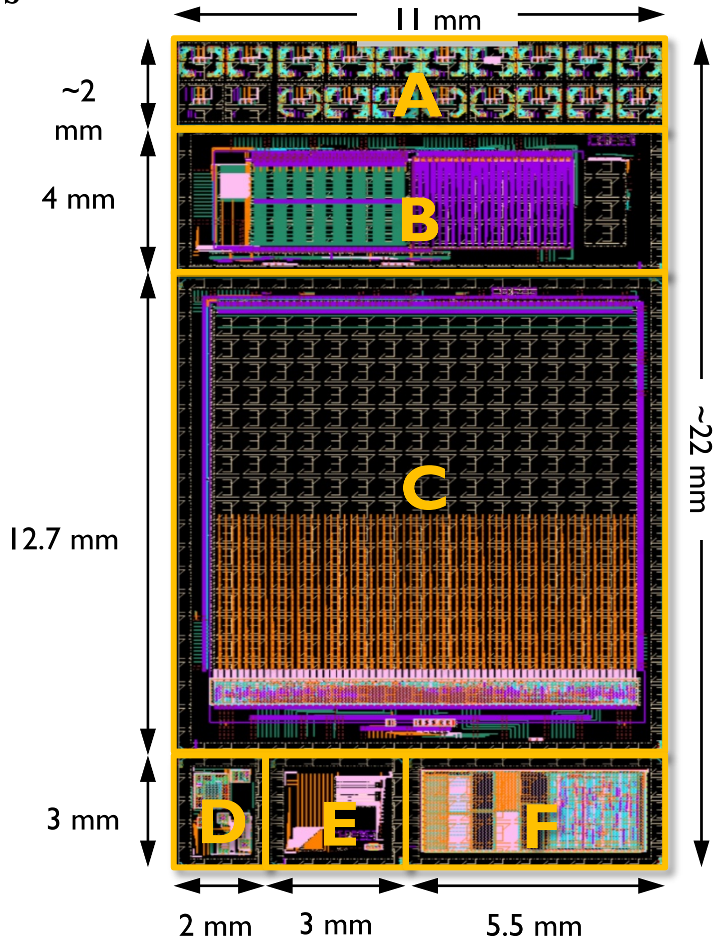
20 times the layout size of COFFEE3, can be diced into a number of chips serving various goals:

- **Guard rings & Passive sensor design validation:**
  - **(A)** 20 arrays of 3x4 passive pixels with diff guard ring designs, each can be diced into individual 1x1 mm^2 chip;
- **In-pixel FE and Active pixel matrix design validation:**
  - **(B)** 9 variations of in-pixel FE designs & 12 variations of pixel sizes;
  - **(C)** A 256 × 64 pixel matrix (pixel size 38 μm x 150 μm) with digital periphery;
- **Analogue IP & Digital modules and transistors validations**
  - **(D)** necessary analog IPs: PLL, DAC, LVDS, SLDO …
  - **(E)** alternative small pixel arrays and SLDO versions
  - **(F)** digital modules and transistors for TID and SEE studies

The chip is expected to be returned next month.

Answers to many key questions can be expected!

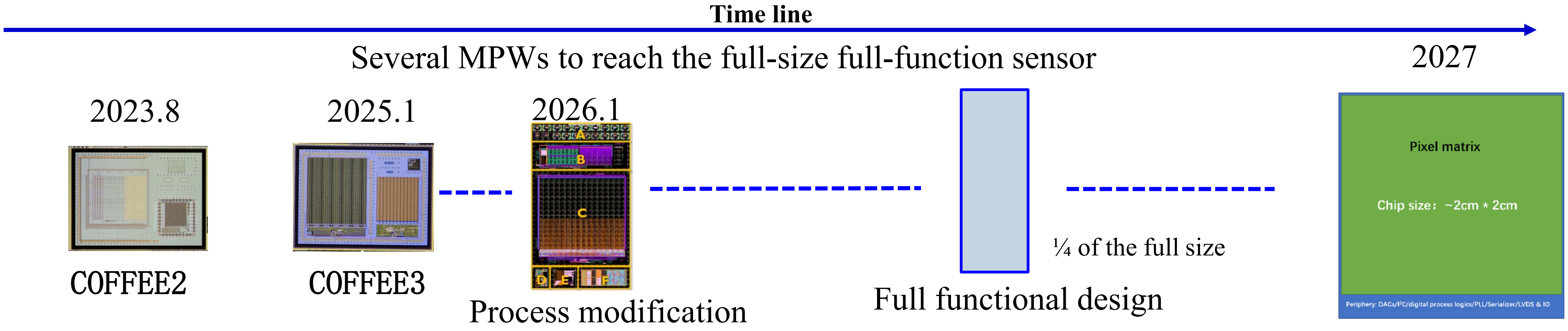
*CHiR (COFFEE-HiRes)



Layout of CHiR1.0, submitted Jan. 24, 2026

Summary and Outlook

- We have complete the design of COFFEE2/3 in a commercial 55nm HV-CMOS process； The preliminary test results are positive, more performance tests are in progress;
- The first design CHiR 1.0, based on the modified process has been submitted; answers to many key questions can be expected! If everything goes well, the design optimization will be implemented based on the modified process.
- Hopefully, we could have the full-function and full-size chip at the end of 2027.



Time line

Several MPWs to reach the full-size full-function sensor

Target: Time resolution ~ ns； Spatial resolution ~10 μm; Power dissipation < 200mW/cm^2 ;

Acknowledgements

Name list: Random ranking

Leyi Li, Xiaoxu ZHANG, XiaoMin WEI, Weiguo LU, Pengxu LI, Mei ZHAO, Yang ZHOU, Bingchen Yan, Anqi WANG, Yuanhong JIAO, Yang CHEN， Yujie WANG, Huimin Wu, Zexuan ZHAO, Yu ZHAO, Zheng Wei, Jianpeng DENG, Zhan SHI, Kunyu XIE, Xinhao XIE, Xiaolong WANG, Ziying ZHANG, He HUANG, Junyuan YAN, Shenyao TANG, Hui ZHANG, Ruoshi DONG, Yang CHEN, Xuekang LI， Xinyang GUO, Zhuojun CHEN, Hui ZHANG, Zhiyu XIANG, Zijun XU, Zeng CHENG, Kang LIU, Menke CAI, Boxing WANG, Yuman CAI, Mingjie FENG, Lei ZHANG, Meng WANG, Hongbo ZHU, Yiming Li, Jianchun WANG ……..

& **Independent KIT design in COFFEE2**: Hui ZHANG, Ruoshi DONG, Ivan PERIC；

Thanks for your attention!

Power Dissipation

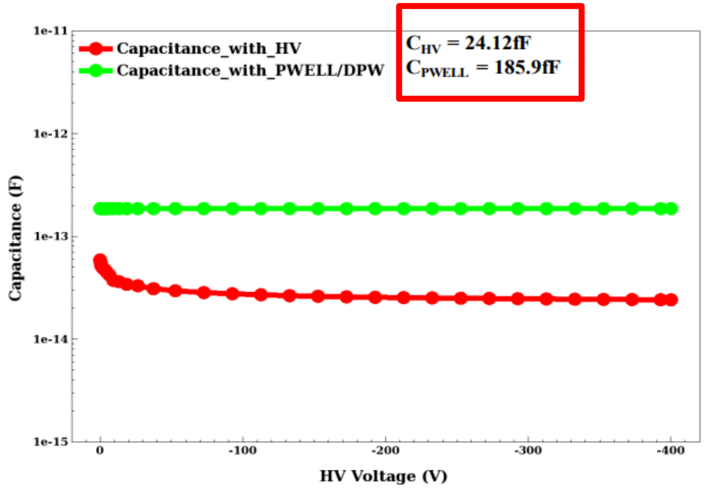
Architecture 1：
- ➢ in pixel matrix: ~10μW/pixel

Architecture 2：
- ➢ in pixel matrix：
  - Two analogue FE design：~10 μW/pixel；
  - Power for time-stamp distribution：~ 20 mW/cm^2;
  - Fine time TDC：only work in fired pixel;
  - Hit density related dynamic power consumption：not yet evaluated；

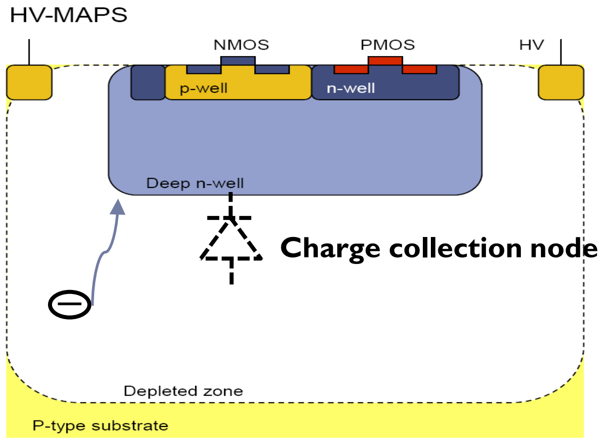
Layout area and simulated power consumption of the peripheral functional modules

Peripheral modules	area	Frequency	Power consumption
Digital module	~ 1.2mm ×18 mm	40 Mhz	~ 40 mW/cm^2 (estimated)
PLL	360×360 μm^2	160/320/640 Mhz	0.98/1.76/2.66 mW
LVDS Receiver	70×140 μm^2	40/160/320/640 Mhz/	1.13/1.58/2.18/3.38 mW
LVDS Transmitter	112×250μm^2	40/160/320/640 Mhz	4.87/5.04/5.27/5.73 mW

Architecture 1: a simple in-pixel design leads a small C_{diode}



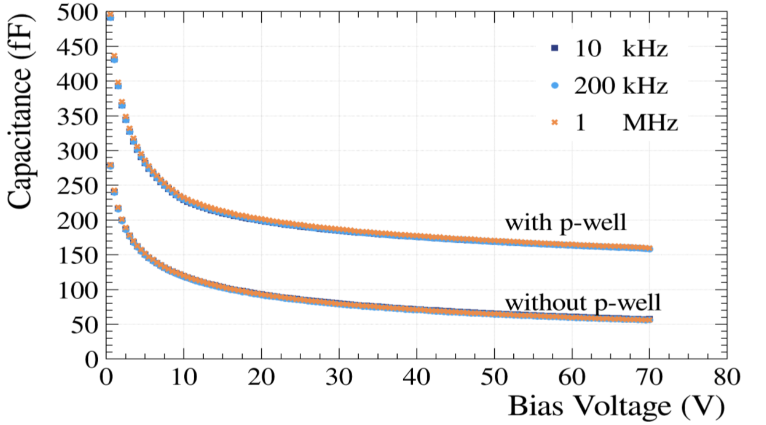
TCAD simulation of the CV for one pixel.



- **The power consumption:**

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f}$$

$$TW \propto \tau_{CSA}\frac{V_{TH}}{V_{sig,min}}$$



CV test results of a pixel with or without P-well inside.

For a determined temporal response, **a smaller C_d and larger signal** are crucial to reduce the power consumption of the in-pixel amplifier.

Architecture 1: only a CSA and a comparator in pixel → very compact in-pixel ASIC layout.

--» potential for low power or small pixel size (high position accuracy)