Session 13:

Cryo-CMOS @ SLAC

Characterization and Design for Liquid Noble Experiments and Superconducting Sensors and Qubits

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TID-ID Integrated Circuits Department

May 5th, 2026

Cryo-CMOS @ SLAC – From 165K → 4K (and below)

Noble Liquid Experiments

Superconductive Sensors/Qubits

Liquid Xenon (LXe) | ~165K

Liquid Argon (LAr) | ~87K

Liquid Helium | < 4K

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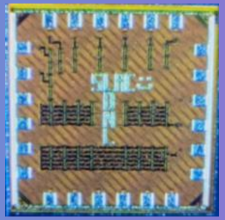

Cryo-PDK in 28 nm
165 K, 87 K (possibly 4 K)

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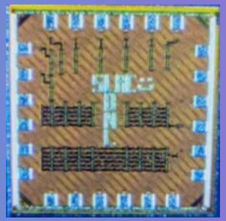

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PHOCA ASIC

Photon readout ASIC in 28nm

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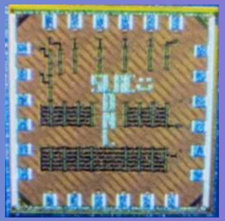

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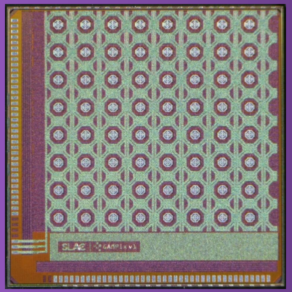

GAMPix v1

Pixelated charge readout
in 130nm

Cryo-CMOS @ SLAC – From 165K → 4K (and below)

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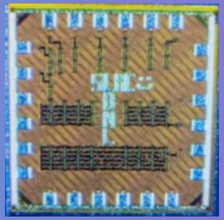

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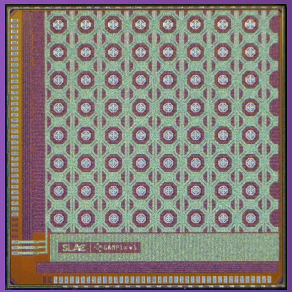

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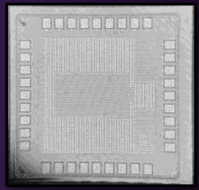
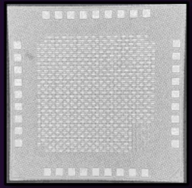
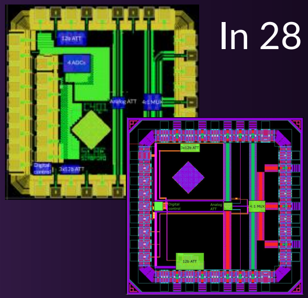


VESPER v1
Single-channel INA in 28 nm



BOREAS v1
Dual-channel INA in 22 nm FDSOI

C4Q1 - **recently tape outed**
RF SWs & Attenuators



In 28 nm

In 22 nm FDSOI

Cryo-PDK: Motivation

Why we need tech characterization at cryogenic temperatures?

Reason 1:

Transistor models from standard PDKs are designed for industry-standard temperatures (~400 K-233 K)

Reason 2:

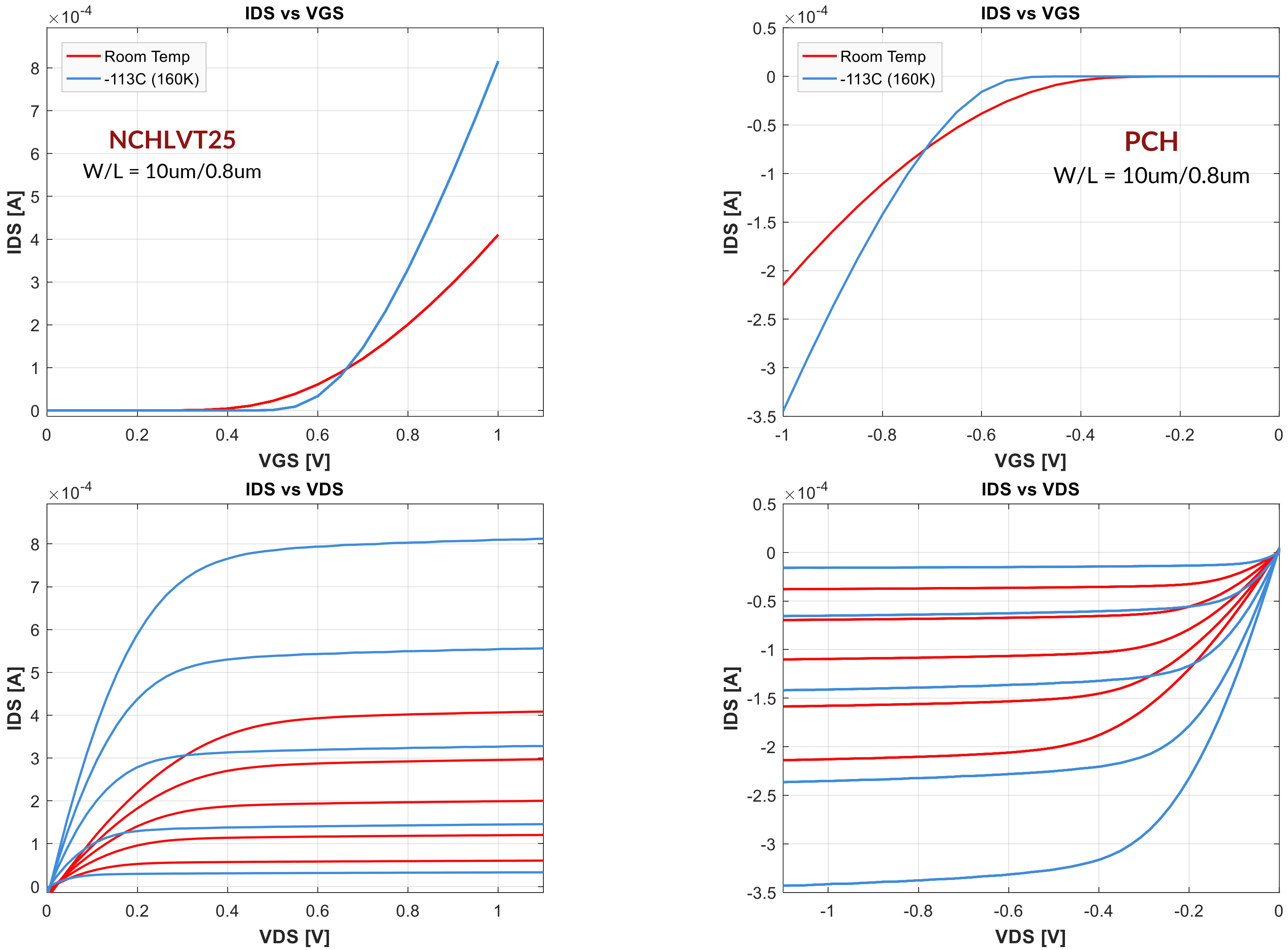
Devices behavior changes dramatically when cooled to 165 K, 77 K and 4K (or below)

Reason 3:

Strong interest from Science & Industry

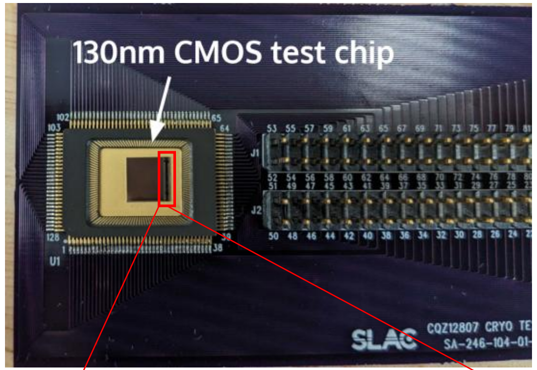
Param	Effect in cold
Mobility	Increases
Threshold voltage	Increases
Subthreshold slope	Improves
Leakage current	Collapses
Mismatch	Changes
Thermal noise	Reduces
Kink effect	Can appear
Flicker noise	Unpredictable

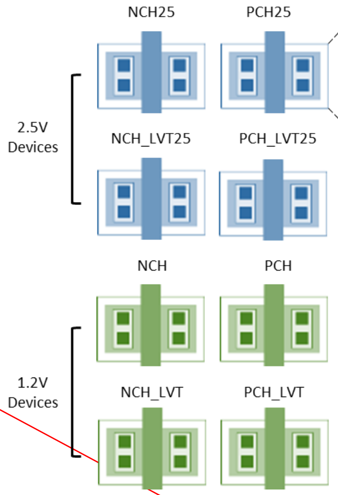
Cryo-PDK: Example of Device I-V Curves (130 nm)



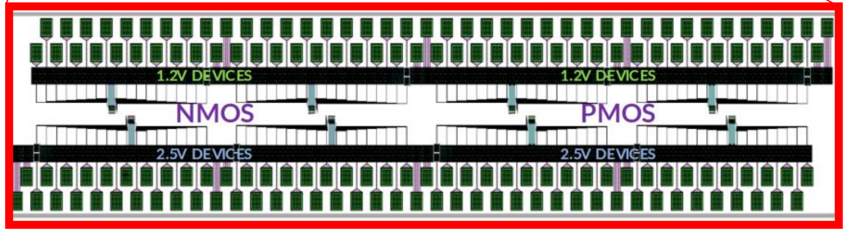
Cryo-PDK: 130 nm vs 28 nm (LBL-SLAC Joint Effort)

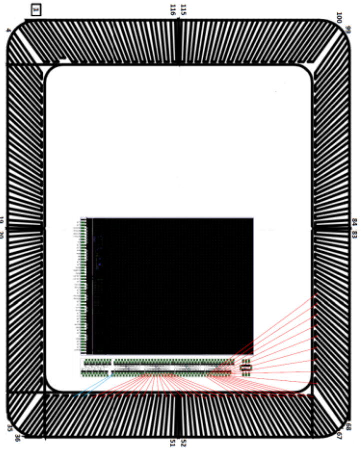
130 nm Cryo-PDK (back in 2016)





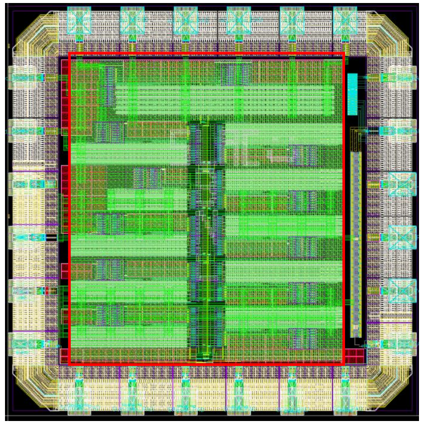
W/L	L1	L2	L3	L4
W1	DUT1	DUT5	DUT9	DUT13
W2	DUT2	DUT6	DUT10	DUT14
W3	DUT3	DUT7	DUT11	DUT15
W4	DUT4	DUT8	DUT12	DUT16





Array of NMOS and PMOS devices (nominal and LVT at 1.2V & 2.5V)

28 nm Cryo-PDK (recent effort!)



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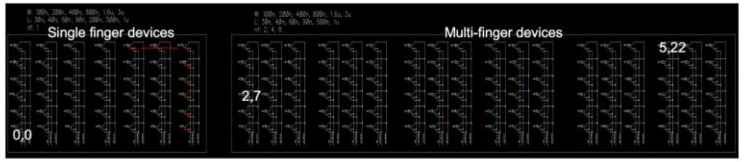
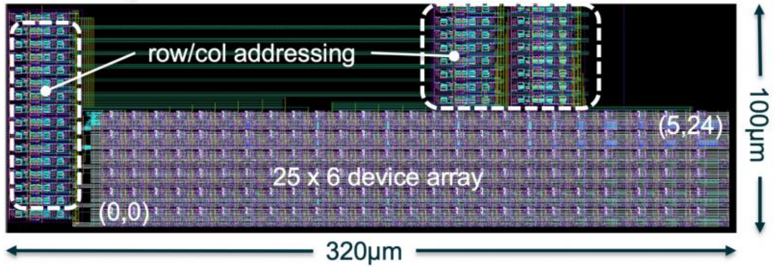
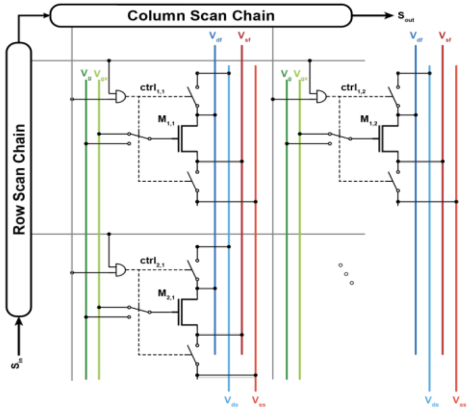
Example of NMOS devices

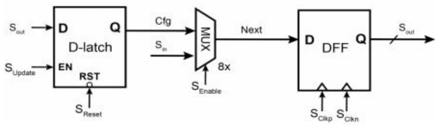


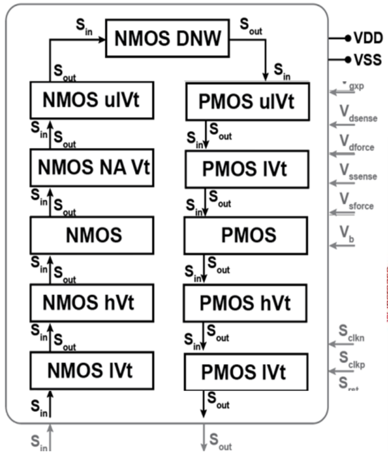


Row/Column selection

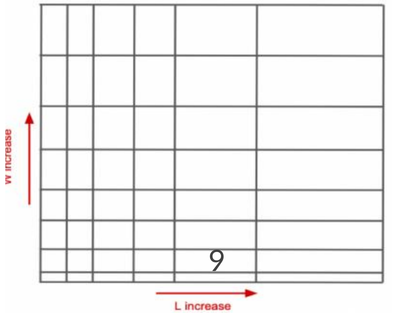


Internal logic for device selection





Array of core devices



Cryo-PDK: The R&D Prototype

Chip prototype

- Previous LBLN design tailored into a mini-ASIC with improvements (chip size: 1 x 1 mm^2 area)
- **Modifications carried out by graduate students (ex-HEPIC):**
  - Victor Turbiner, Will Johnson, Marissa Hsu, Kevin Boateng
  - Great opportunity for new designers to do a tape-out
- Test structures include a variety of device flavors and geometries

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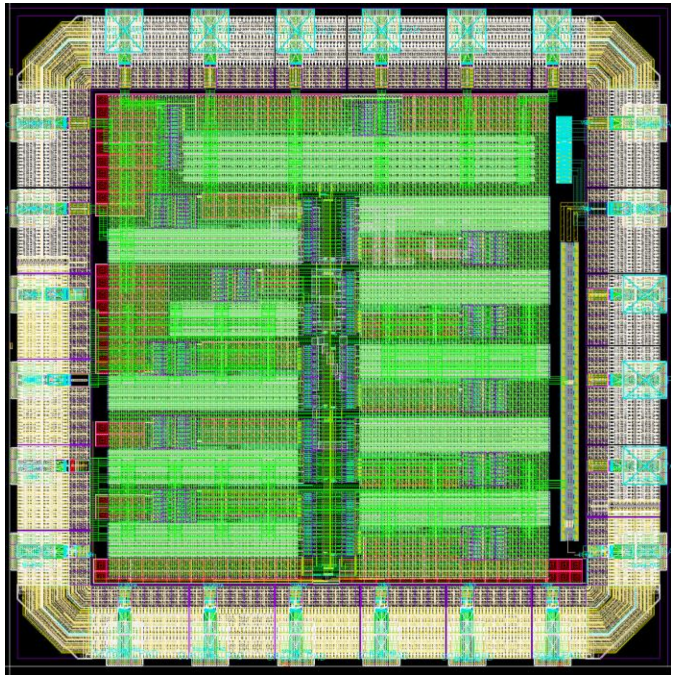


LBL-SLAC R&D Prototype
(28 nm CMOS)

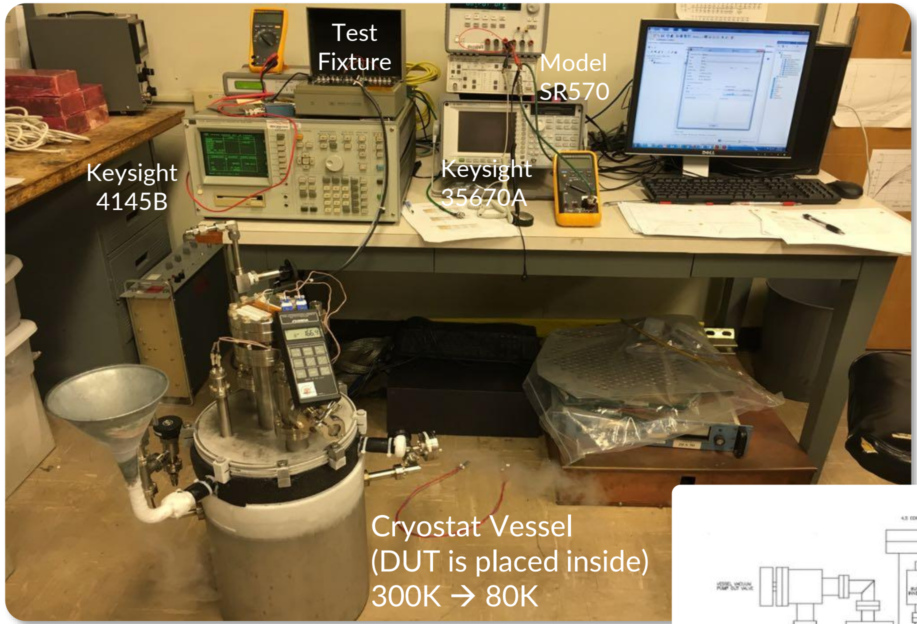
Deliverables for 2026:

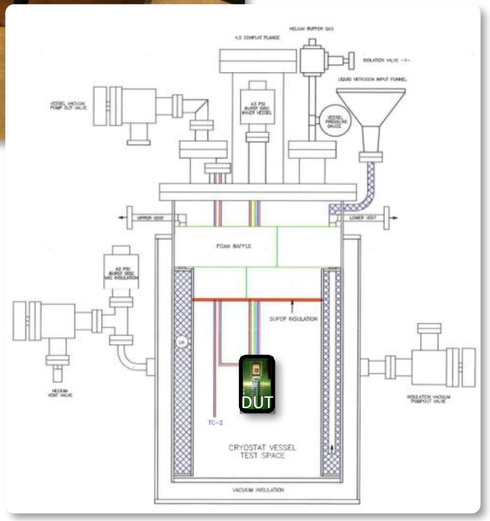
- Joint characterization campaign between LBL and SLAC
- Targeting different temperatures: 165 K, 87 K, and probably 4 K
- Develop the data fitting and model extraction platform

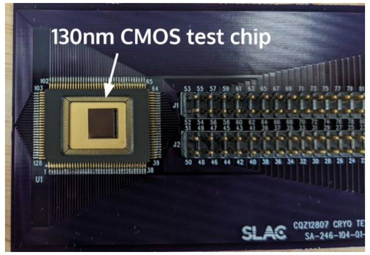
Cryo-PDK: Test Setup (130 nm vs 28 nm)

Valeria Zarco
BSc UC Davis

130 nm Cryo-PDK (back in 2017)

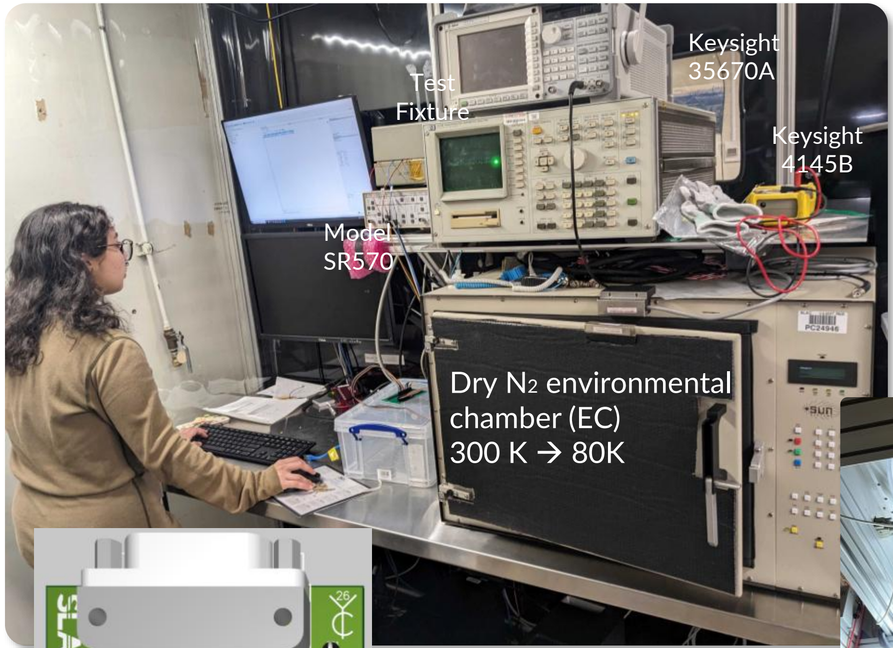


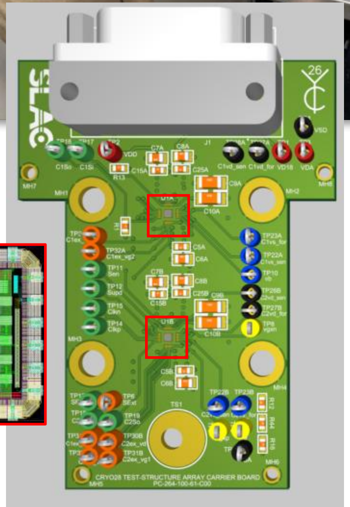


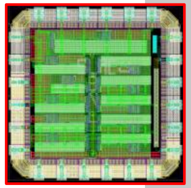


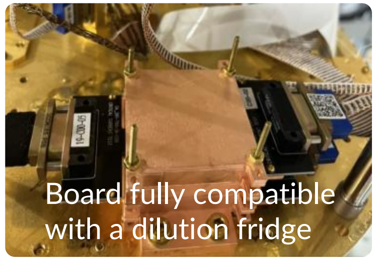
Drawing:
Courtesy of Bob Conley

28 nm Cryo-PDK (new effort)







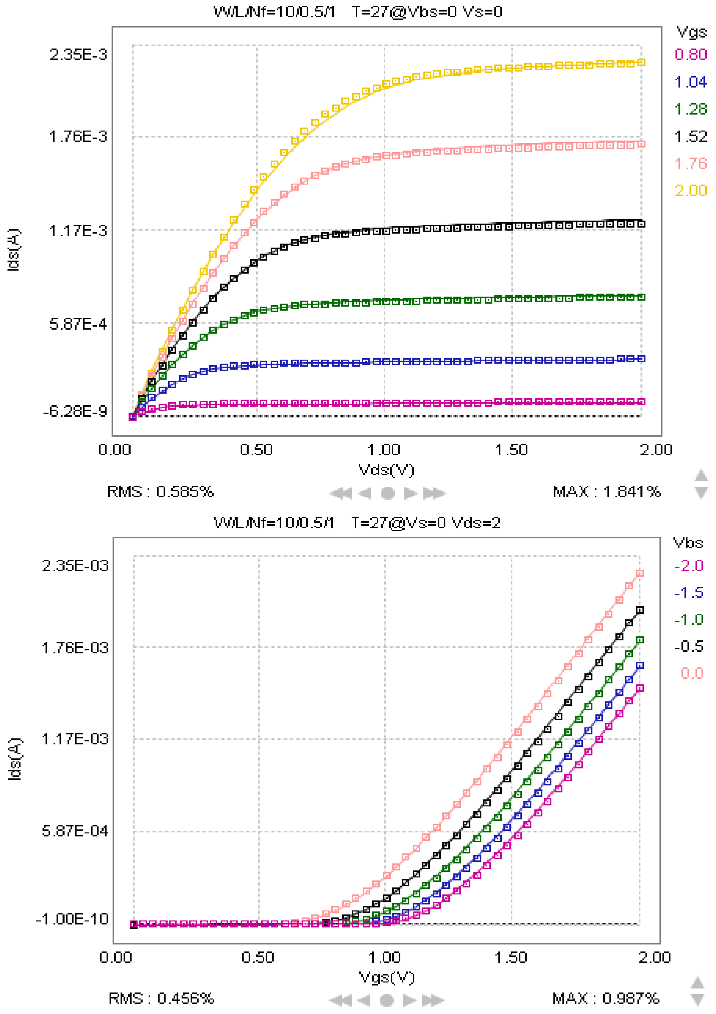


Data vs model - Example of I-V curves across temperatures (130 nm)

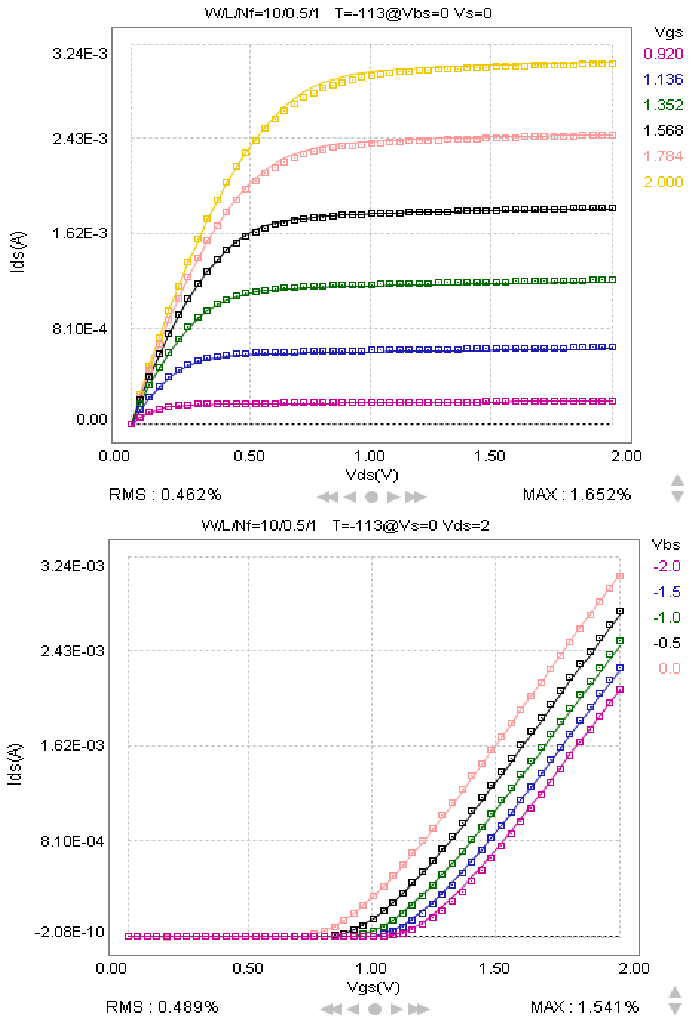
DC Model (solid line) vs Measured Data (marker)

Device: NCH25 | W/L = 10u/0.5u

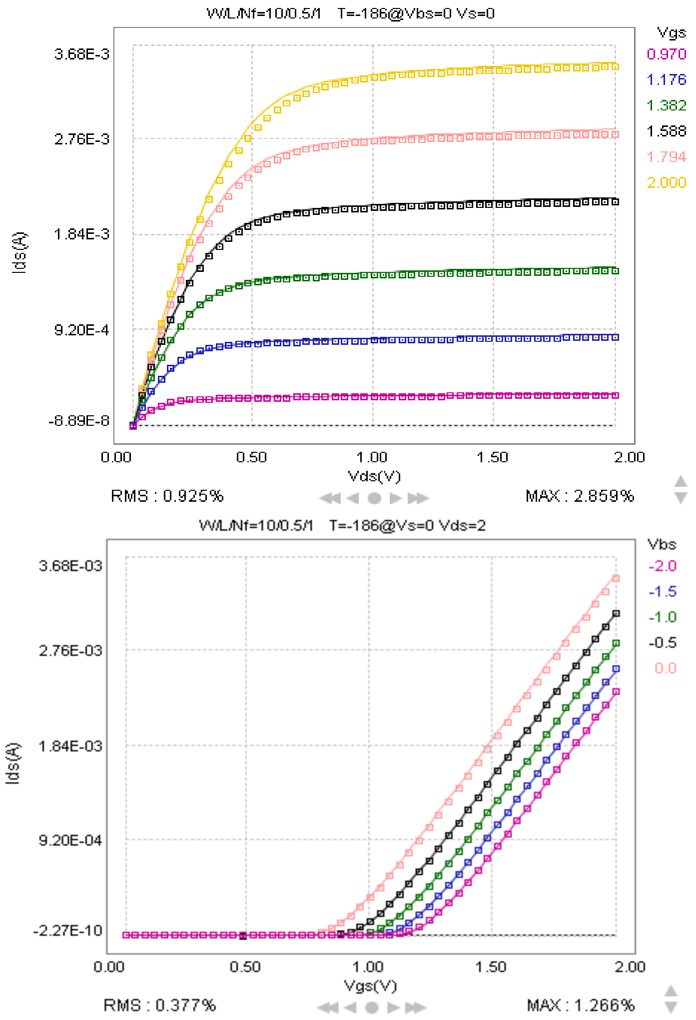
Room Temp: 300K | 27C



LXe Temp: ~165K | -113C



LAr Temp: ~87K | -186C

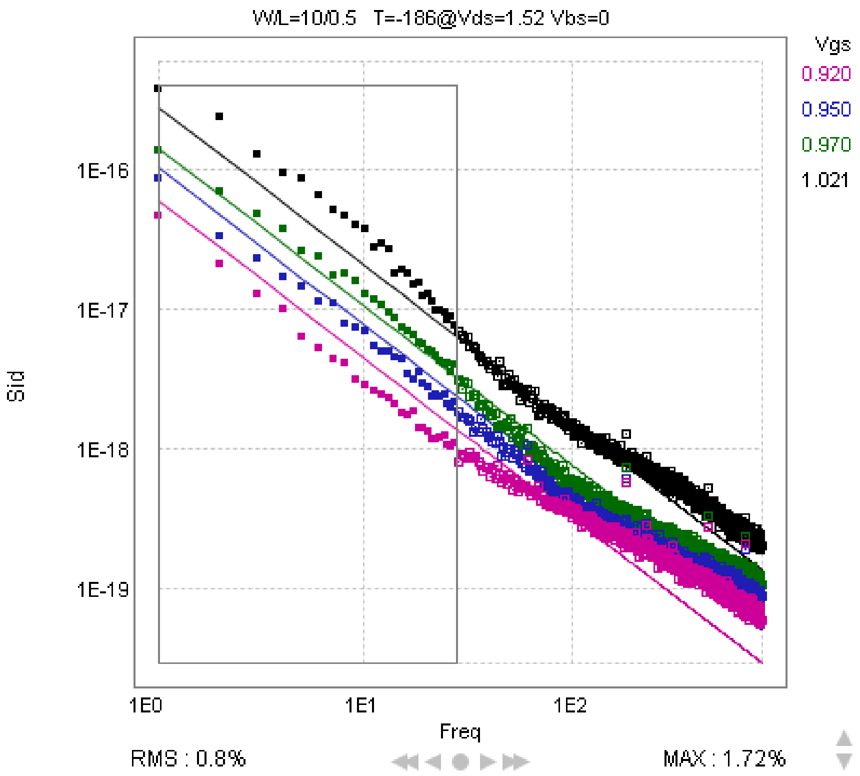


Data vs model - Example of PSD curves across temperatures (130 nm)

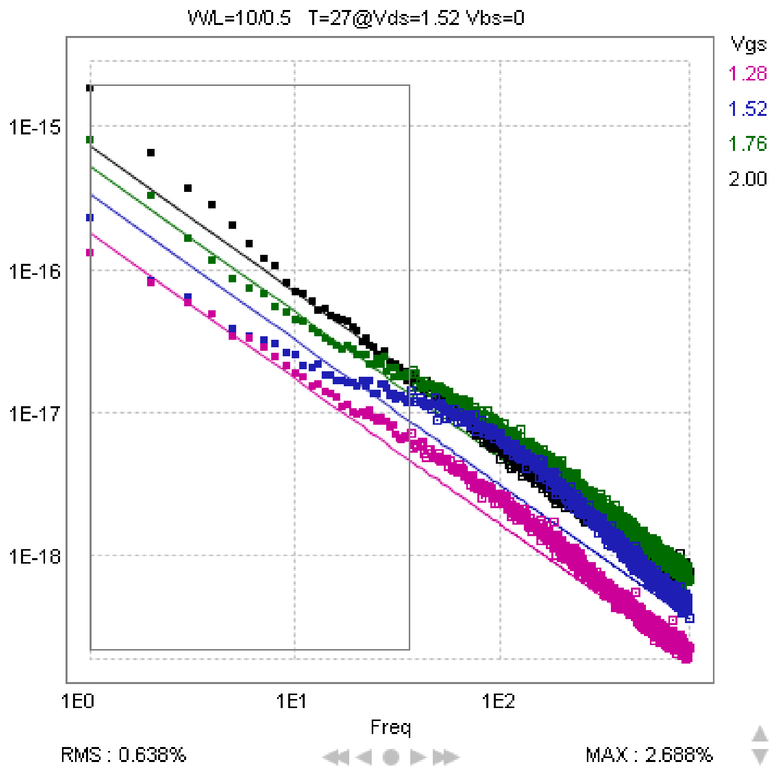
DC Model (solid line) vs Measured Data (marker)

Device: NCH25 | W/L = 10u/0.5u

Room Temp: 300K | 27C



LXe Temp: ~165K | -113C



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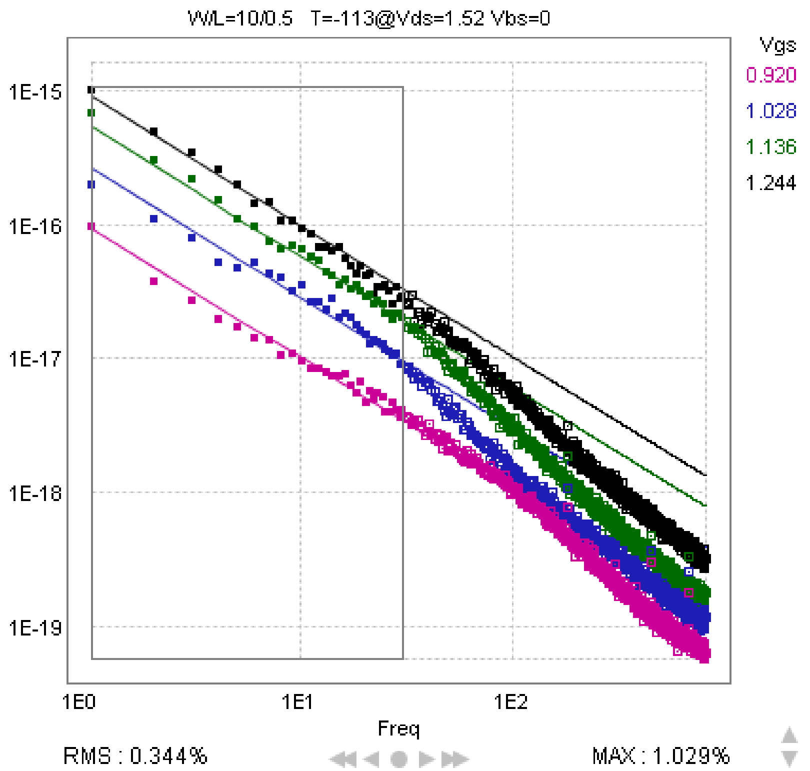


1/f Noise Coefficient

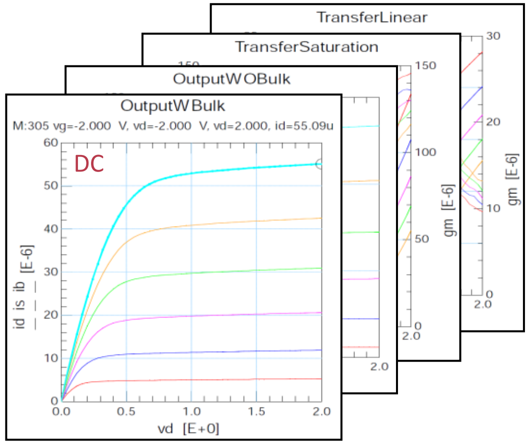
1/f Noise Exponent

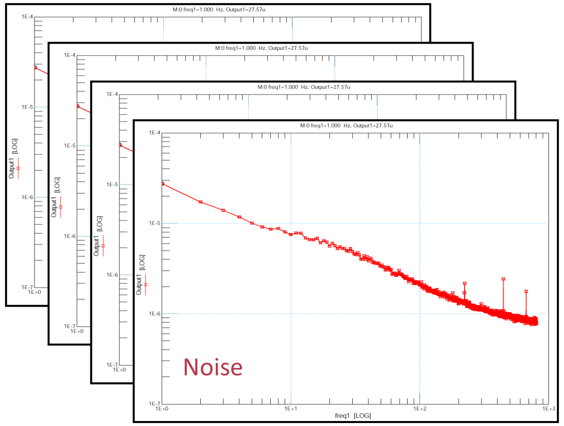
$$S_{id} = \frac{Kf \cdot I_{DS}^{Af}}{Cox \cdot Leff^{2} \cdot f^{Ef}}$$

1/f Noise Frequency Exponent (or Slope Correction)

SLAC

Cryo-PDK: Model Extraction Flow

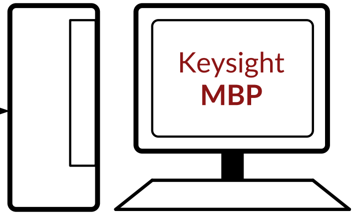


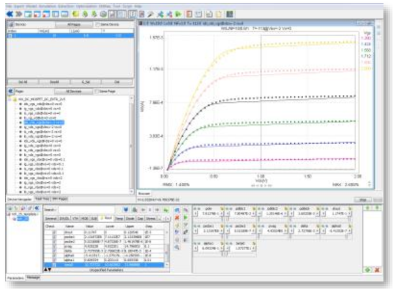


Flow to generate cryogenic models

~165K and ~87K

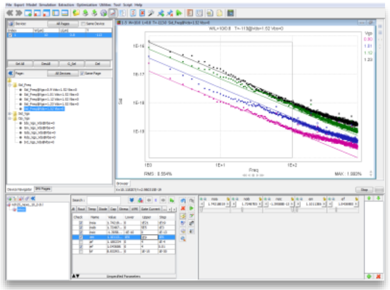
Keysight | MBP
(Model Builder Pro)
Fitting Process
Cryogenic Model





DC Fitting & Parameter Extraction

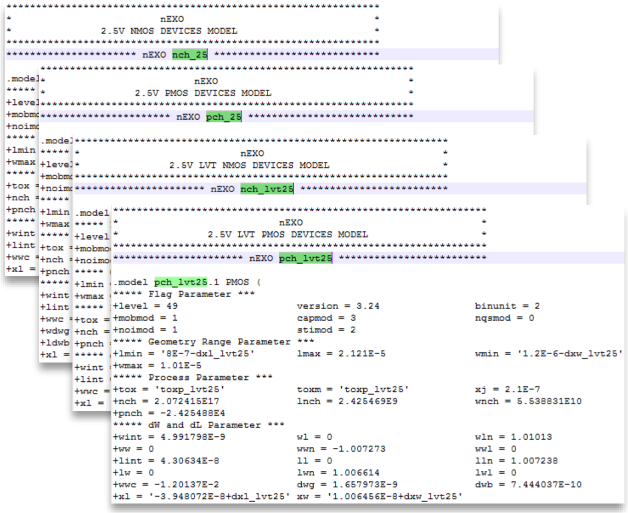
Binned Model

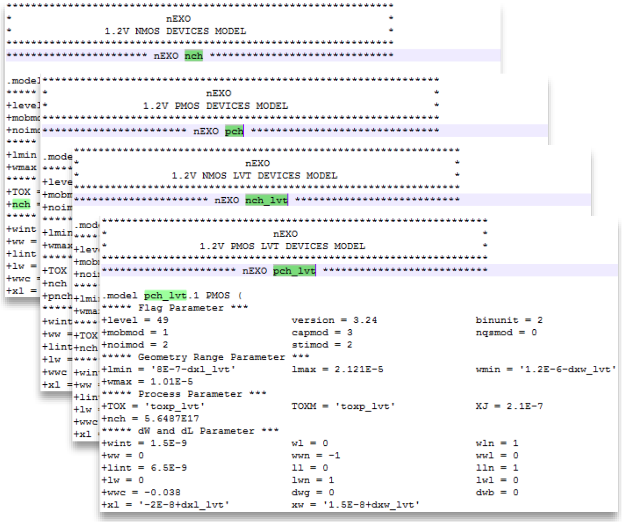


Noise Fitting

1/f Parameter Extraction

Models

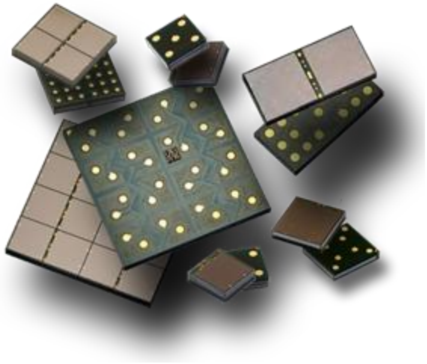




PHOCA: Motivation

Goals of the Photon Readout ASIC Development

- **Support** dark matter, neutrino science, and noble liquid detectors in HEP experiments
- **Detect** faint optical signals for rare particle interactions
- **Utilize** PMTs and SiPMs for low noise, fast timing, and scalability
- **Ensure** compatibility with cryogenic environments
- **Enhance** energy resolution for better discovery potential
- **R&D prototype** integrating analog and digital IPs in 28 nm CMOS

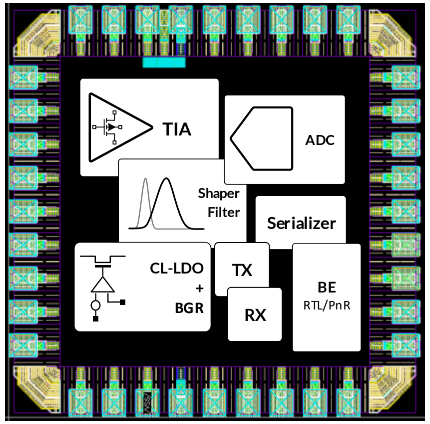


Potential science case

- **XLZD** - Next generation liquid xenon observatory for dark matter experiment and neutrino physics

  [https://arxiv.org/pdf/2410.17137]

R&D prototype



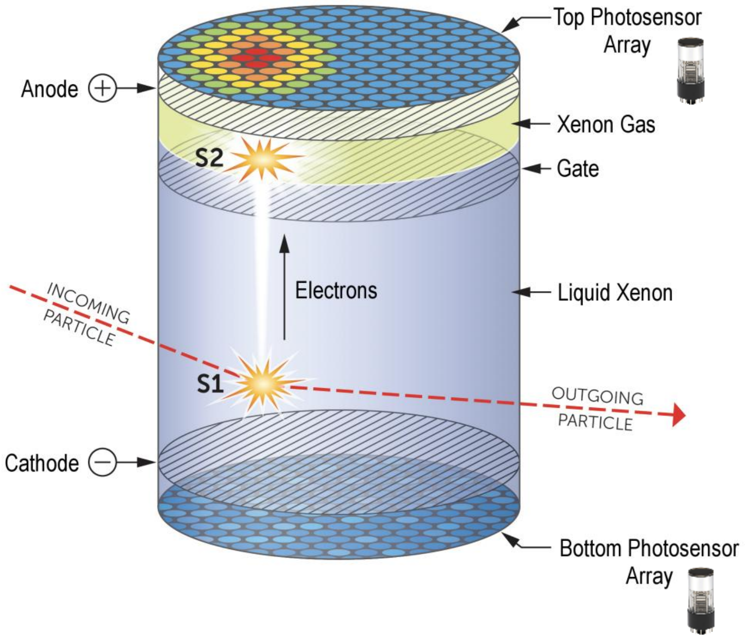
PHOCA: Science Case - XLZD Signals

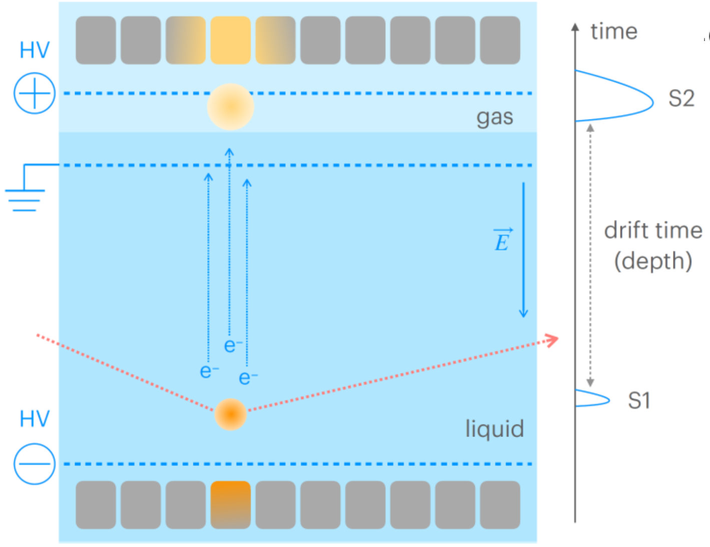
Detection principle:

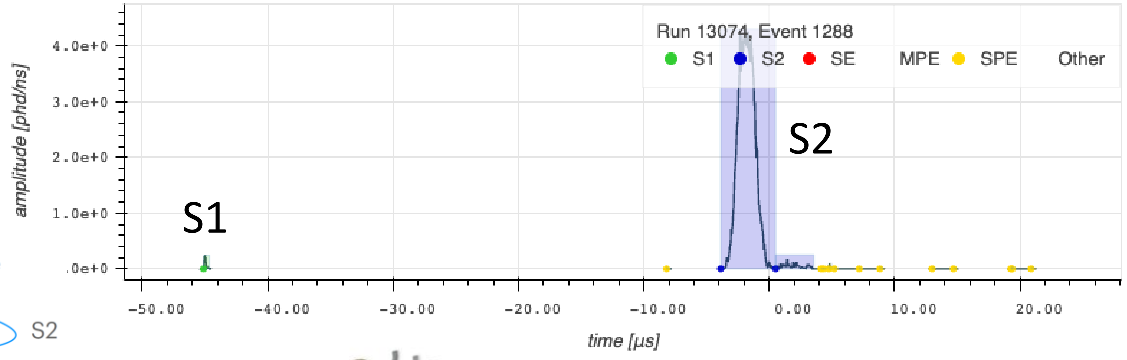
- Particles interact with xenon and produce two light signals: **S1 (~100-200 ns wide) and S2 (~1 us)**
- Maximum time difference between S1 & S2: ~15 ms (event windows of ~5ms or longer)

Goal of this development:

- **Detect & digitize** S1 & S2 signals from particle scatters







- TPC in early stages of design
- 3 m tall filled with ~40-80 tonnes of LXe
- PMT arrays on top (~1000) and bottom (~1000)

PHOCA: Specifications

Technology	CMOS 28 nm
Supply voltage	1.6 V – FE readout 0.9 V – ADC, digital backend, output drivers
Temperature	**300 K → 160 K (LXe regime)**
Min. signal | Max. signal	**1-2000 photo-electrons @ PMT/SiPM gain 1e6**
x3 channel gain (parallel readout)	**High-Gain x1** **Medium-Gain x1/40** **Low–Gain x1/400**
Filter	**Semi-gaussian with 30/60 ns shaping time**
Signal-Noise-Ratio @ 1 ph. el.	**50 @ 300 K | 60 @ 160 K**
On-chip digitization	**100 MSps sampling rate, 12-bit resolution**
On-chip supply regulation	**Optional at 1.6V, on-chip band-gap reference generation**
Fast I/O drivers	CML standard operating at 10 Gbps
Power consumption	< 50 mW / channel

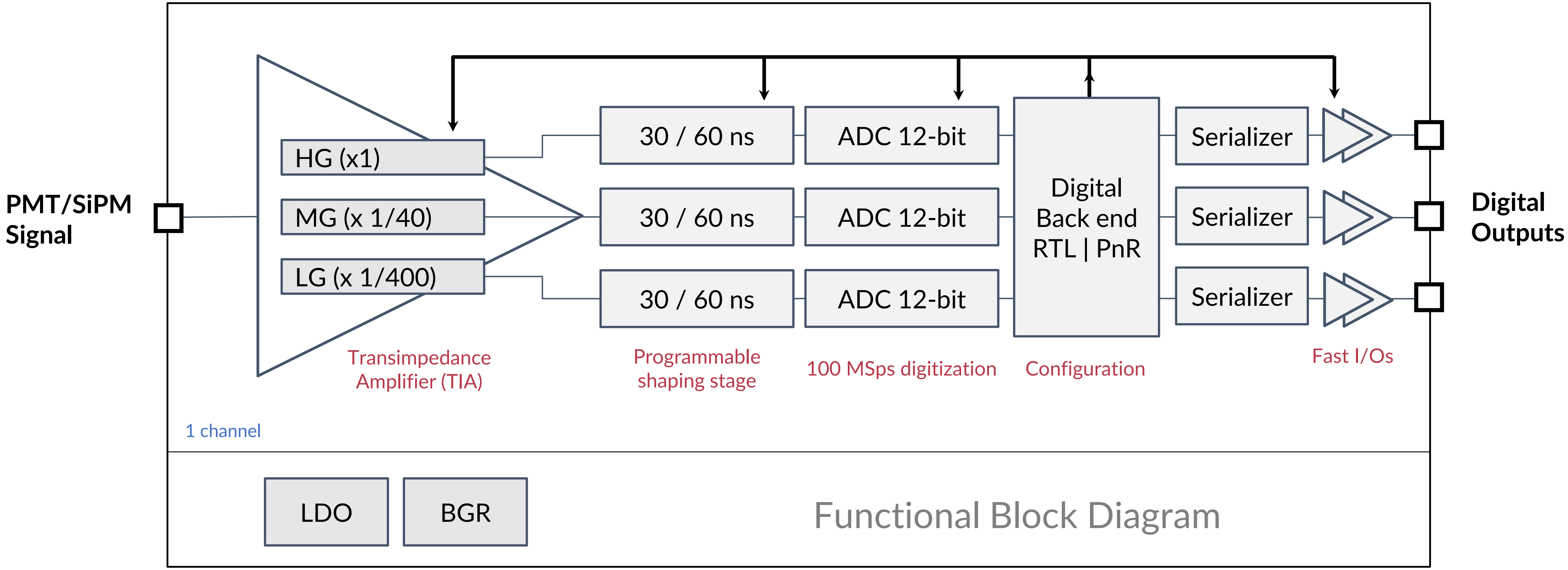
PHOCA v1

PHOton
Cryogenic
ASIC

PI: Hugo Hernandez Herrera

PHOCA v1: top-level layout sent for fabrication in July

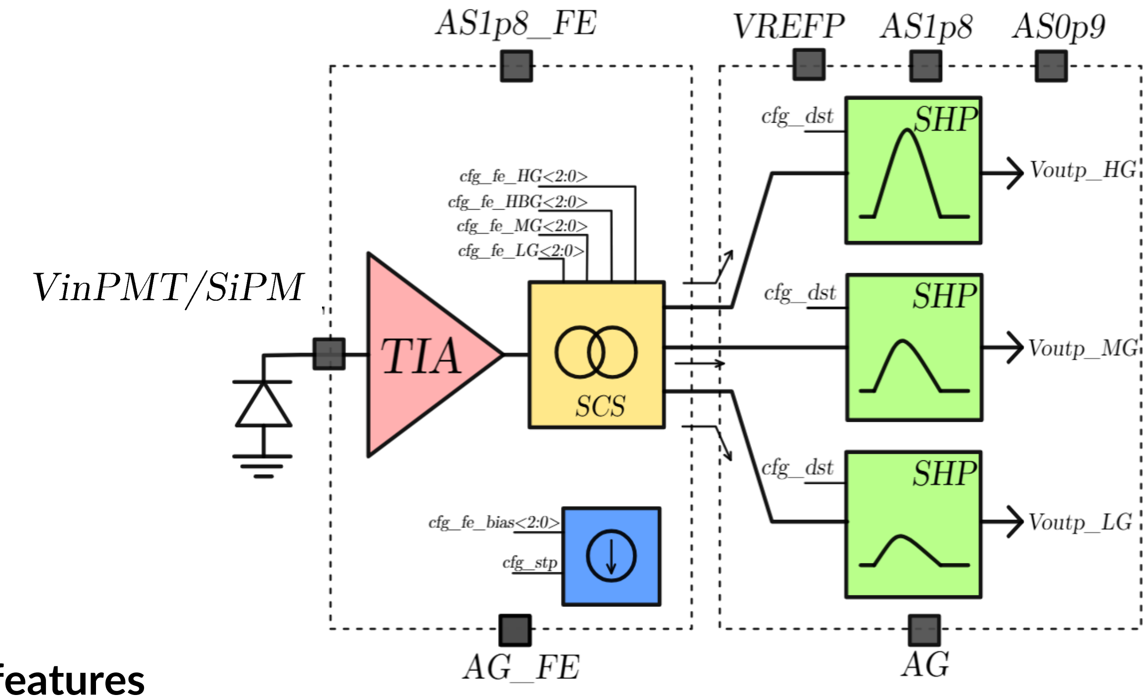
PHOCA: Block Diagram

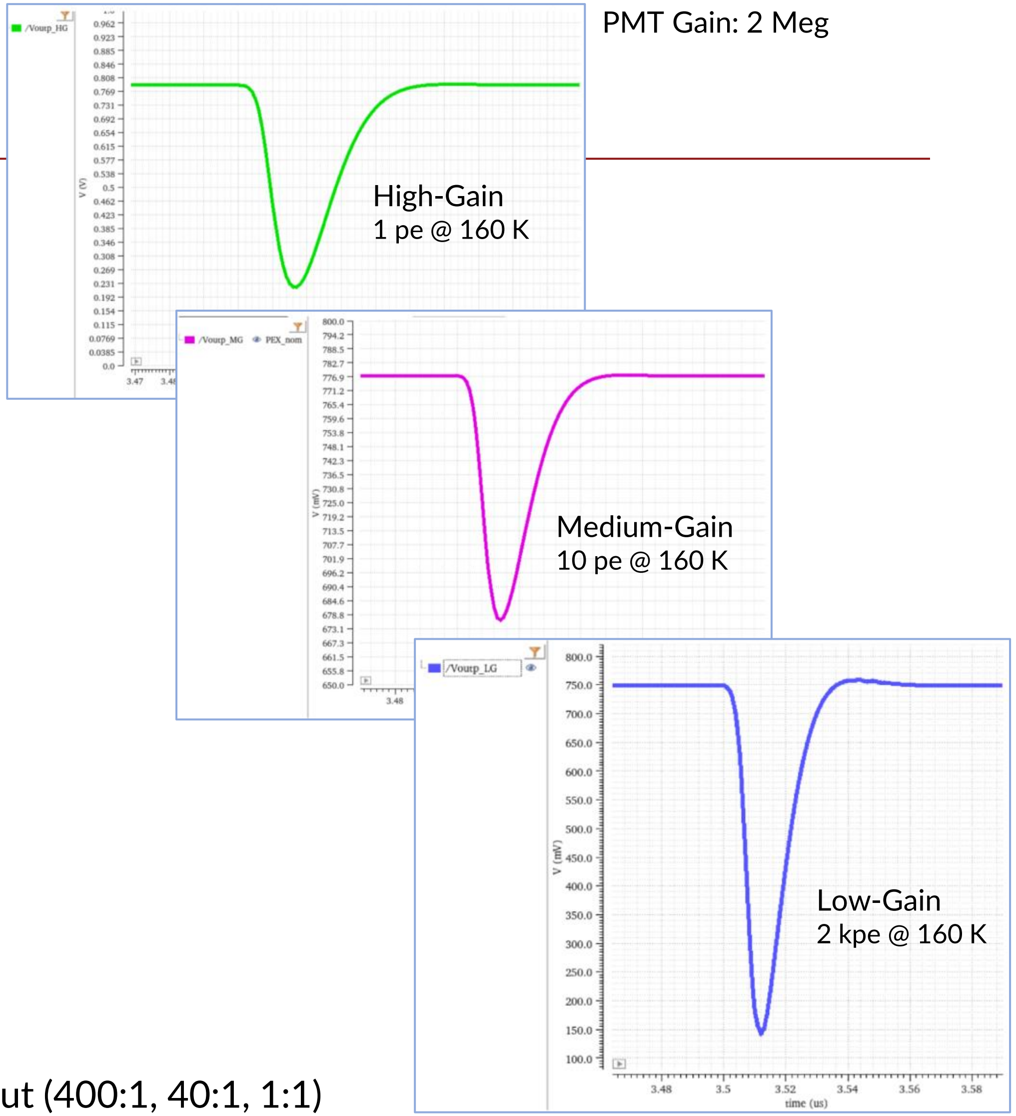


- Target specifications derived from potential upgrade of PMT readout in XLZD experiment
- Collaboration with XLZD partners will help characterization efforts at cold temp in real experimental setup

PHOCA: Front-end

Front-End Channel



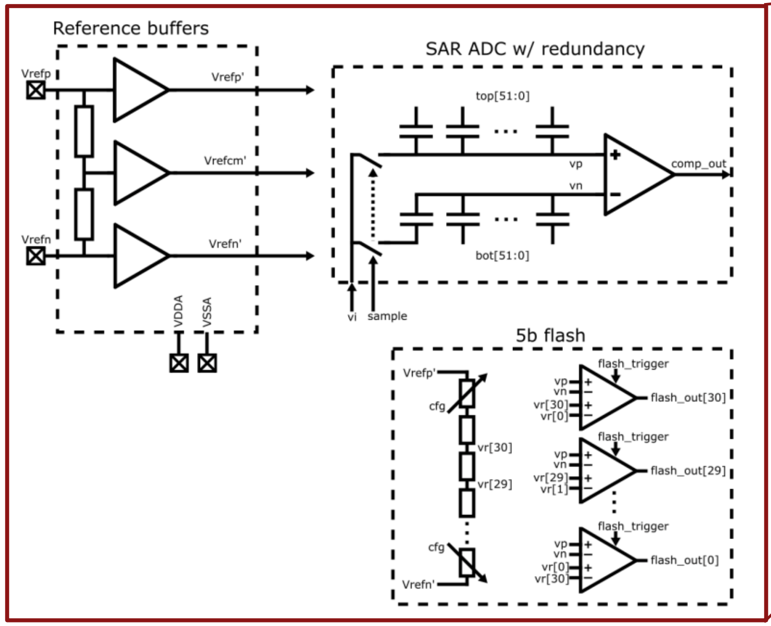


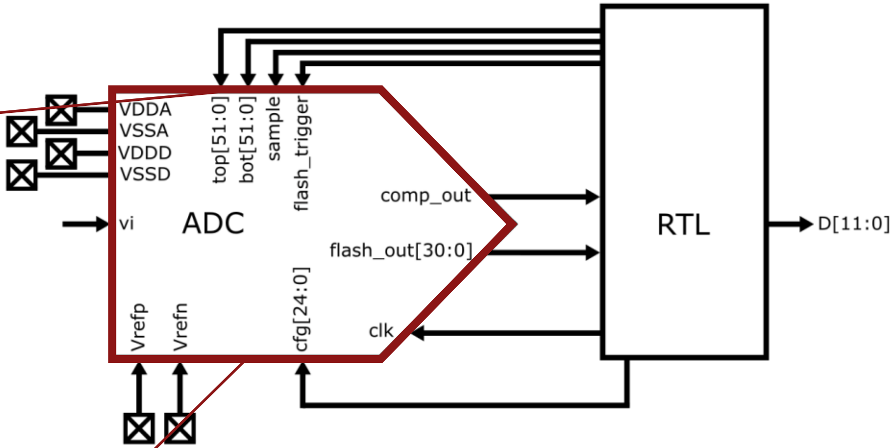
Key features

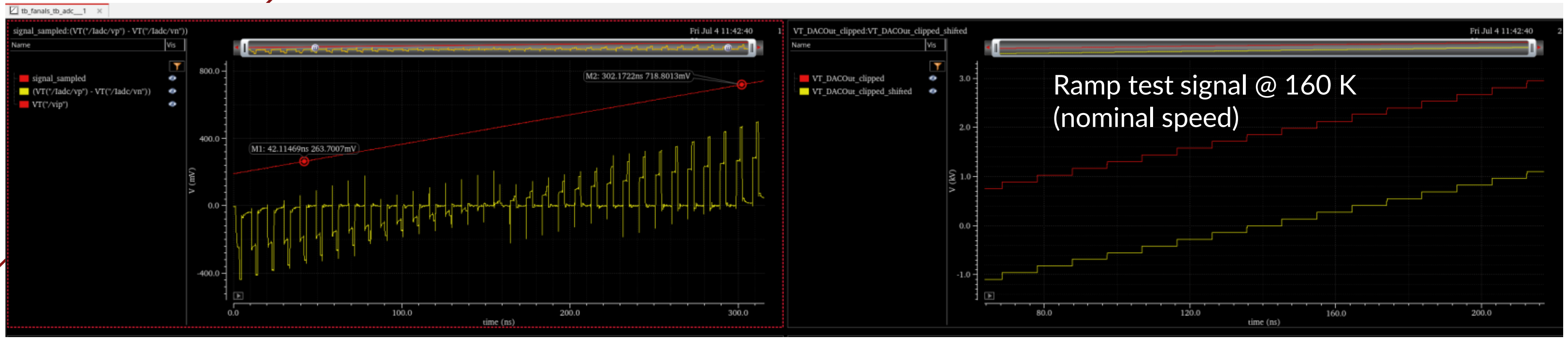
- **Transimpedance Amplifier (TIA):** Converts input current into voltage
- **Current Signal Scaling (CSC):** Generates three scaled copies of the TIA output (400:1, 40:1, 1:1)
- **Semi-Gaussian Shapers (SHPs):** Three-pole low-pass filters producing semi-Gaussian pulses to limit bandwidth and improve SNR
- **Programmable settings:** Bias, shaping time, baseline and gain to optimize operation and performance at cryogenic temperatures

PHOCA: Flash + SAR ADC

A/D Converter





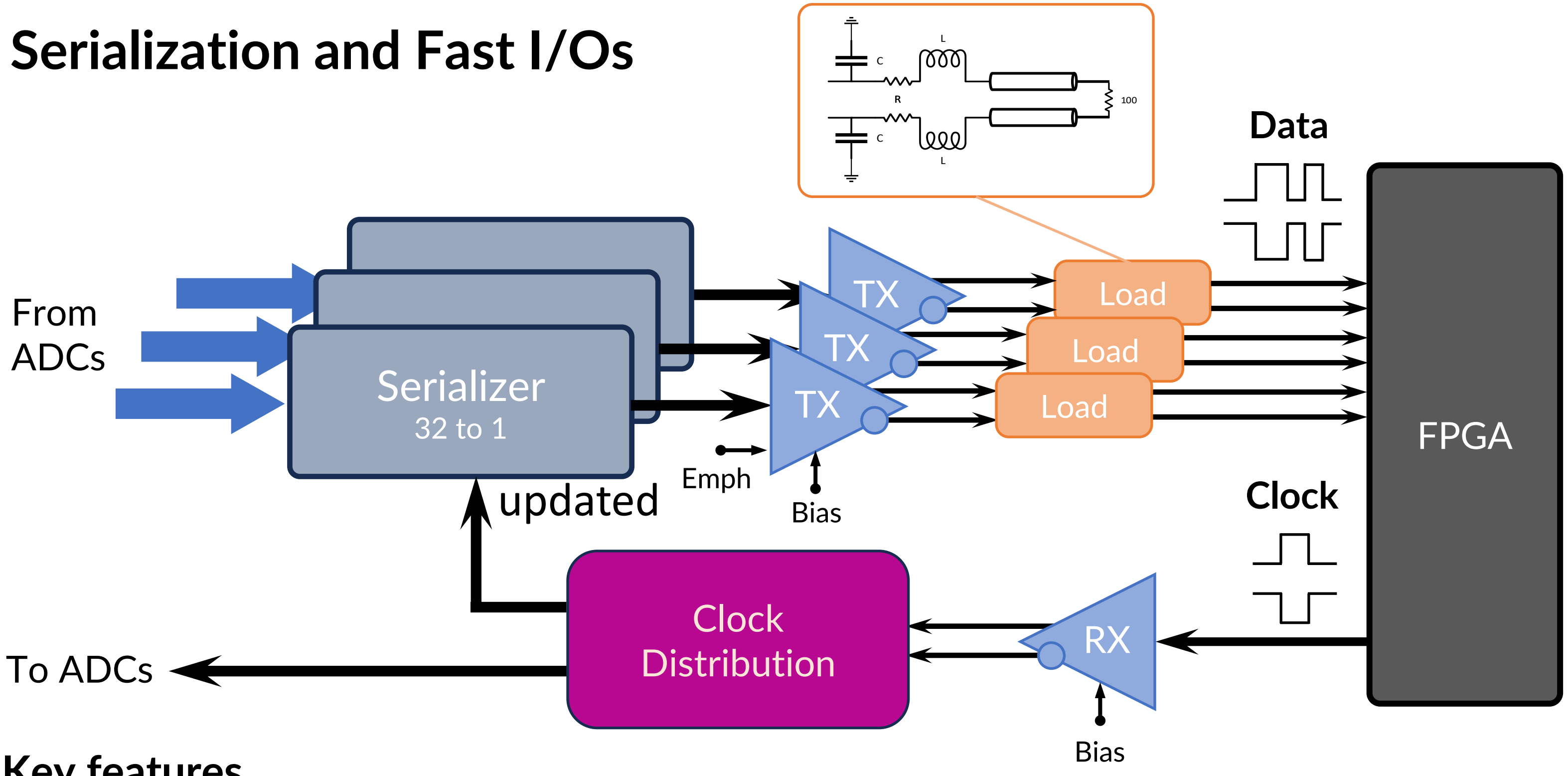


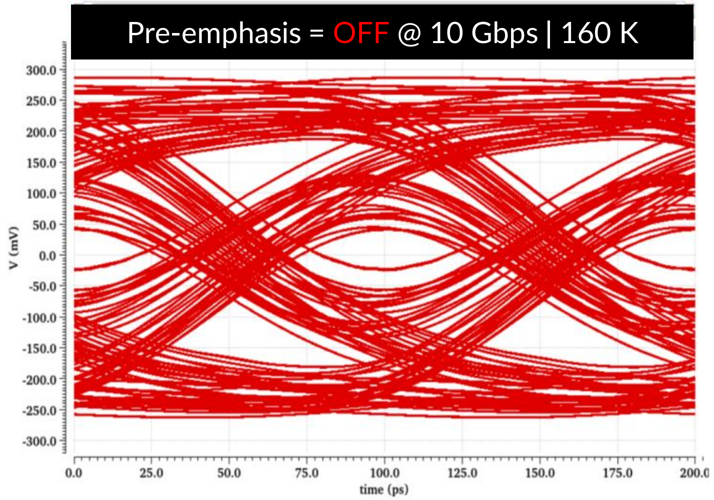
Key features

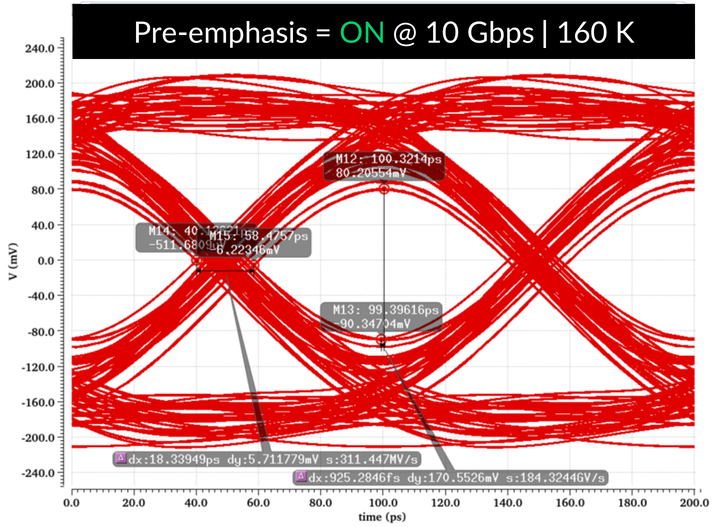
- **Hybrid 12-bit ADC architecture:** 7-bit SAR + 5-bit Flash
- **High-speed operation:** 100 MSps sampling rate
- **On-chip reference:** Three reference buffers provided
- **Programmable settings:** Bias, reference signals and dynamic range to optimize performance at cryogenic temperatures

PHOCA: Backend and CML drivers

Serialization and Fast I/Os





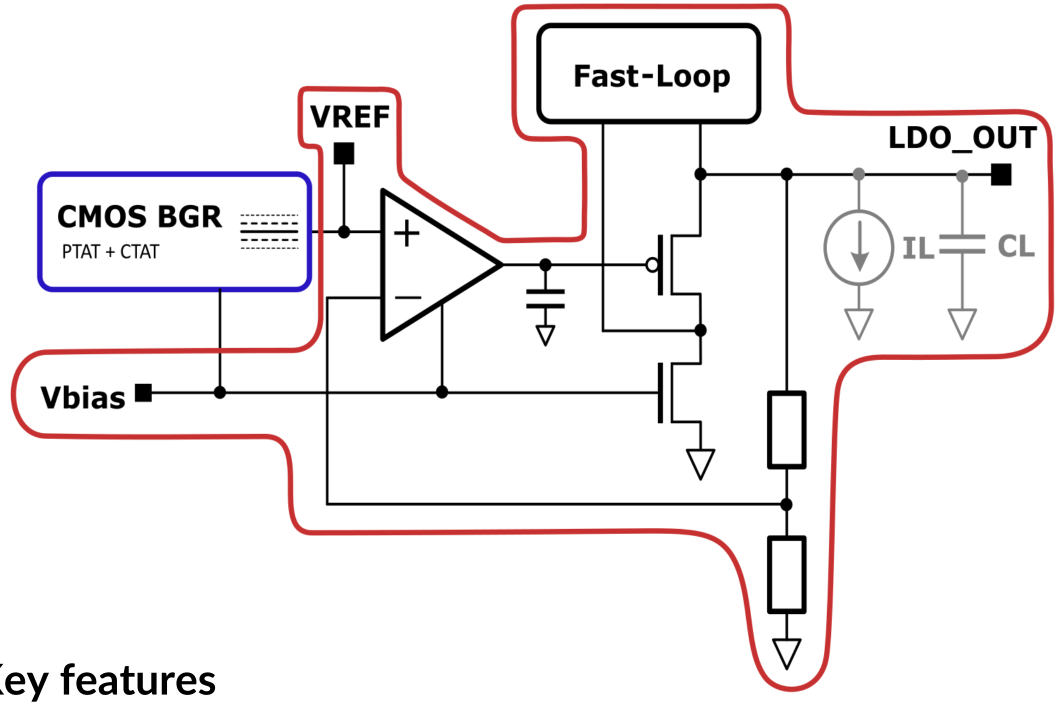


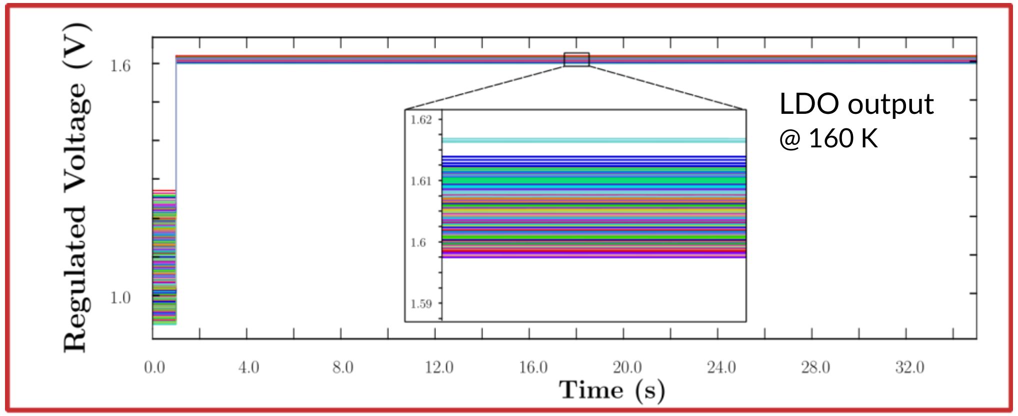
Key features

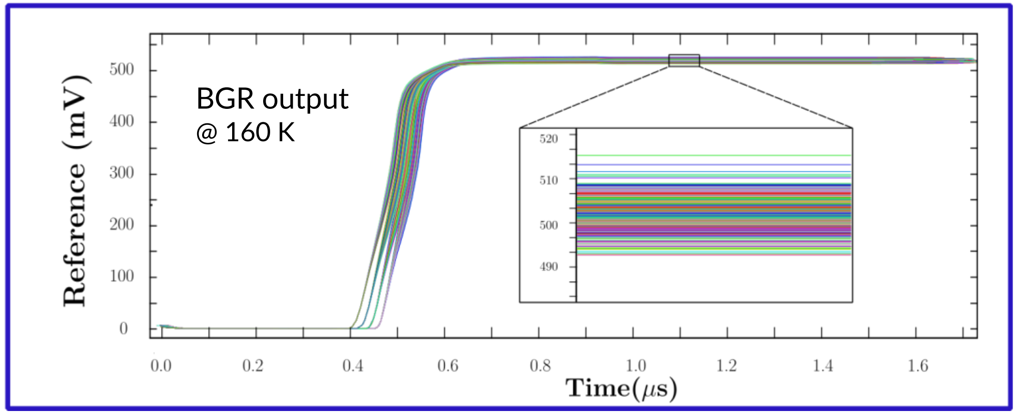
- **TX architecture:** CML standard with pre-emphasis for 10 Gbps operation
- **RX architecture:** CML standard
- **Serializer:** 32-to-1 full custom design
- **Programmable settings:** Bias and pre-emphasis circuitry to optimize performance at cryogenic conditions

PHOCA: BGR + LDO

On-Chip Supply Regulation



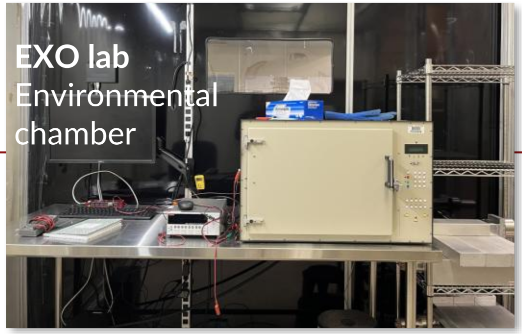


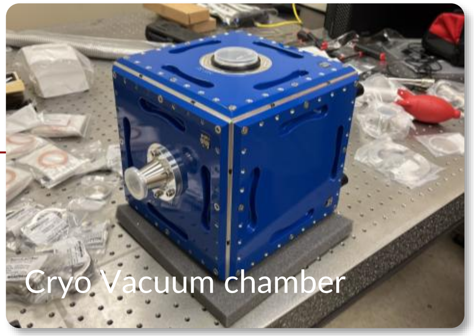


Key features

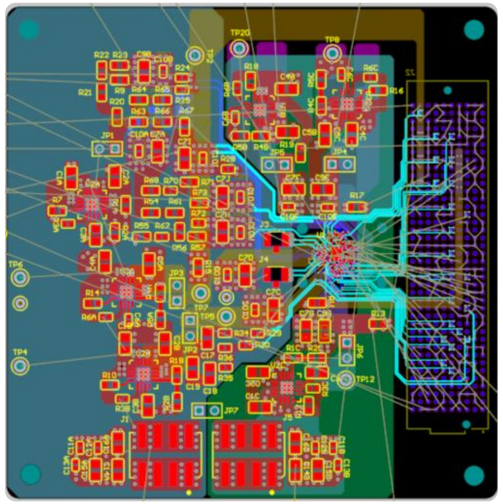
- **Supply regulation architecture:** Cap-less LDO with CMOS-based bandgap reference
- **Supply voltage:** 1.6 V @ 50 mA load
- **Reference signal:** 500 mV (programmable)
- **Programmable settings:** Bias and bandgap reference voltage to optimize performance at cryogenic temperatures

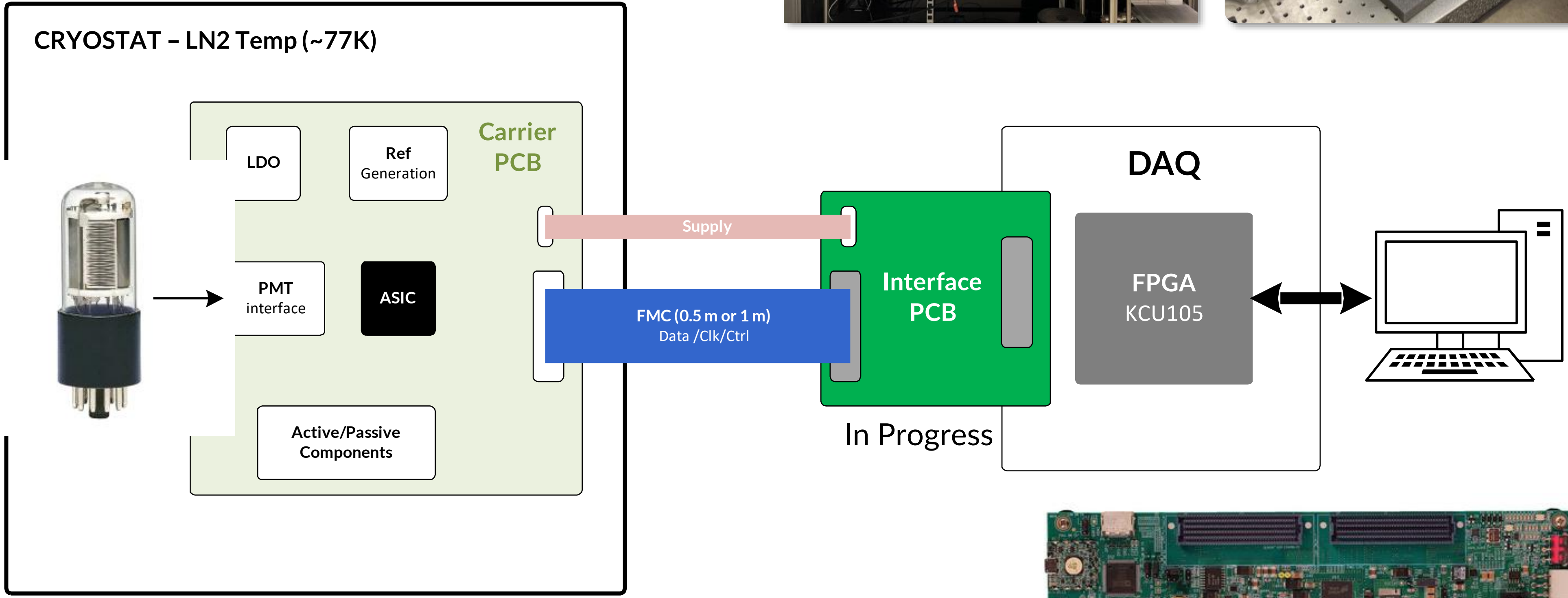
PHOCA: Toward Prototype Testing

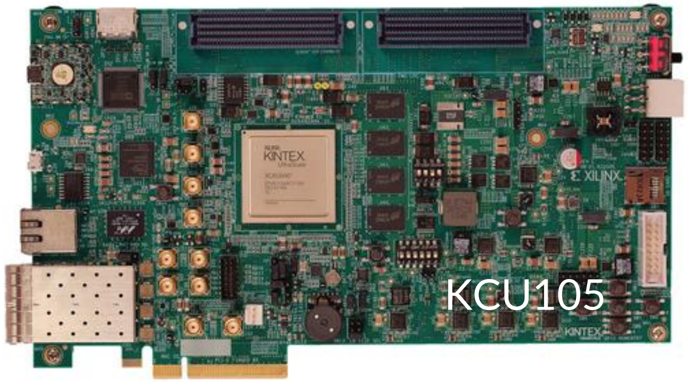




Carrier PCB
(In progress)





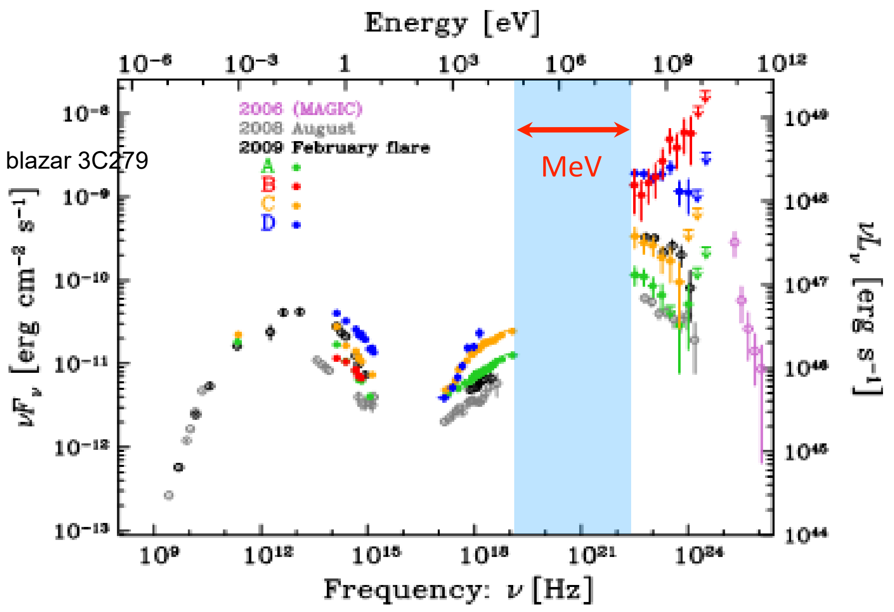


- PHOCA ASICs are at SLAC
- Carrier PCB, interface PCB and firmware are under development
- **Chip characterization will start in middle June**

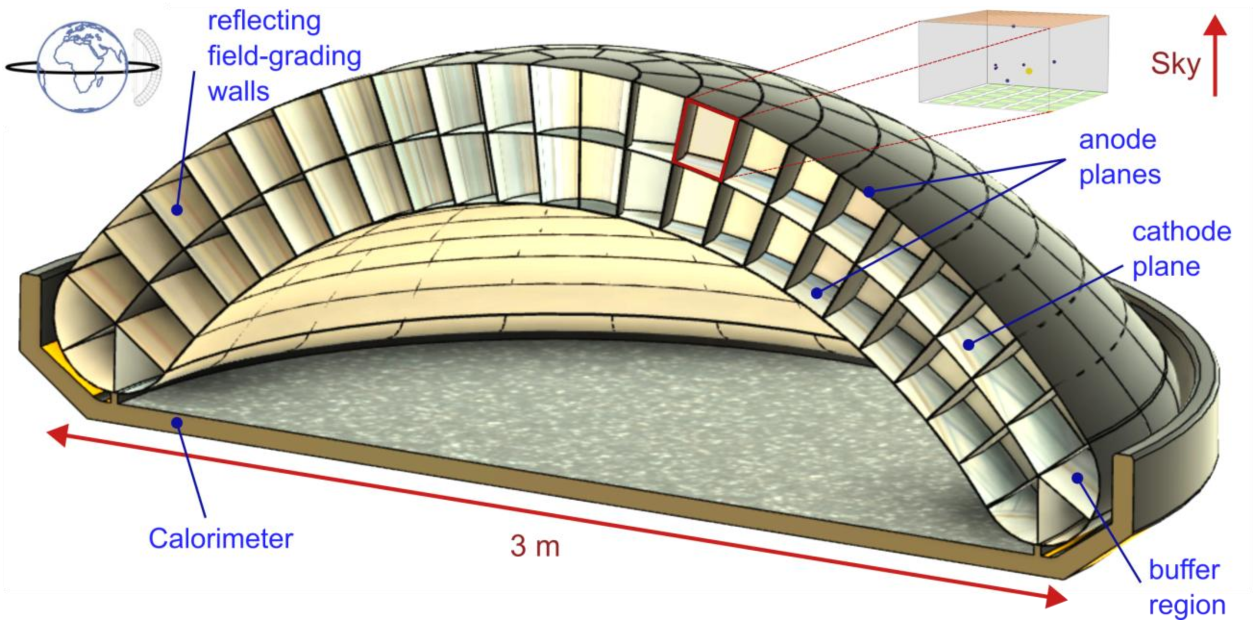
GAMPix: GammaTPC Telescope Concept

Website: https://gammatpc.replit.app/

[ArXiv/2502.14841]



LAr-based TPC: 10 m^2, 4 ton configuration



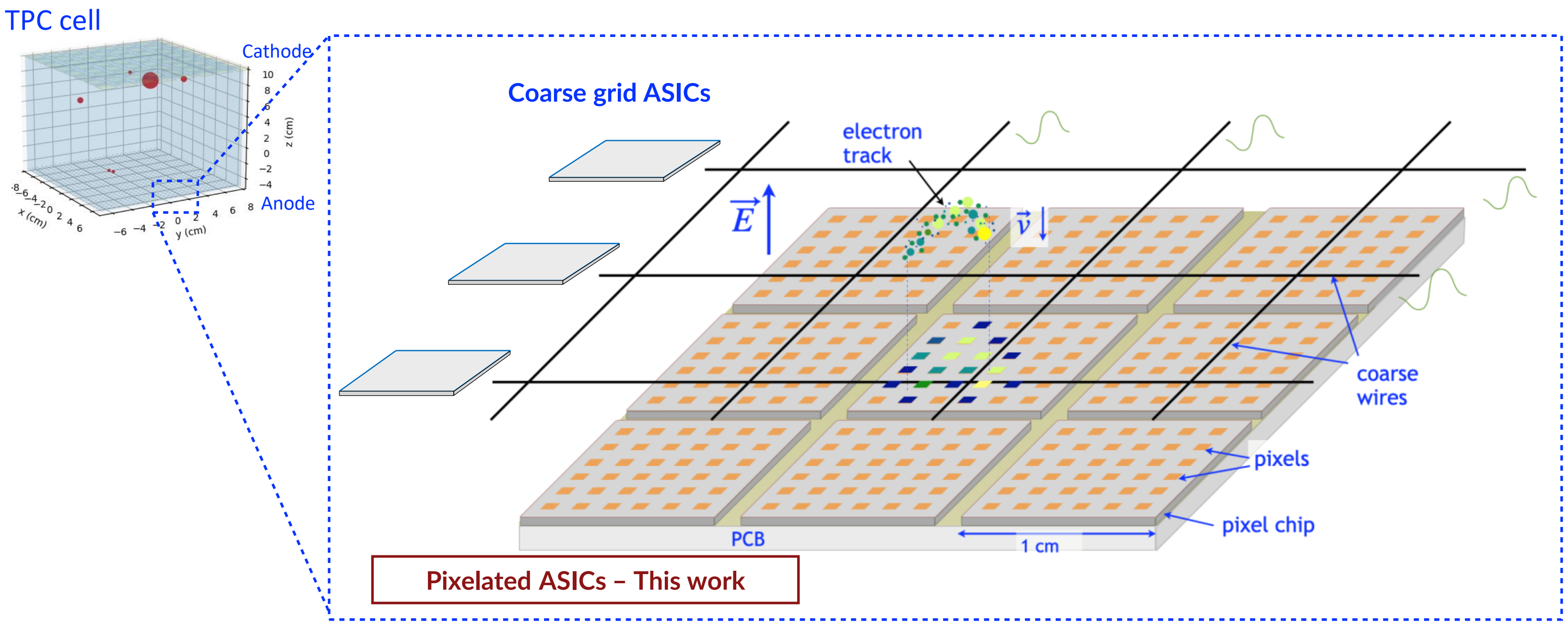
- Fill the long-standing **"MeV sensitivity gap"** in gamma-ray astronomy
- Study extreme astrophysical events: **supernovae, black holes, neutron stars, and cosmic-ray interactions**
- Enable **large-scale 3D imaging** of gamma-ray interactions with sparse, self-triggered readout electronics

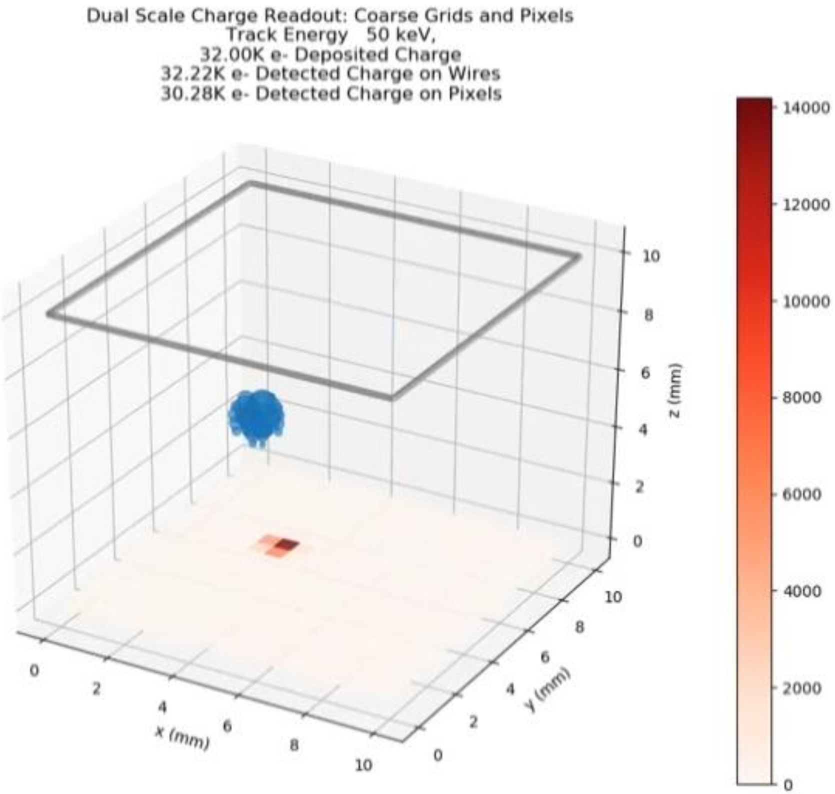
Tom Shutt
Main scientist

Bahrudin Trbalic
PhD student

Paper or ArXiv ☺

GAMPix: GammaTPC Telescope Concept





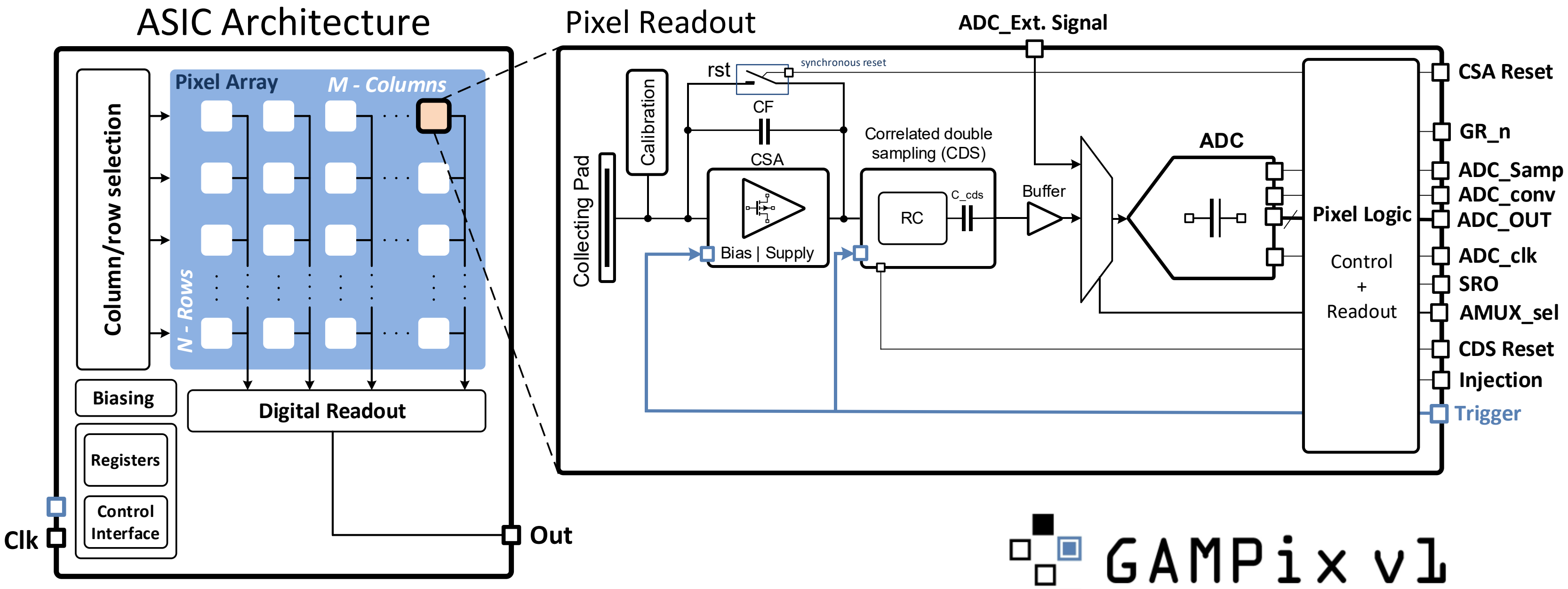
[arXiv:2502.14841v1]

GAMPix - Grid Activated Multi-Scale Pixel readout

Two-stage charge sensing:

- Induction wires → Provide coarse event detection and localization
- Pixels → Provide fine-grained 3D imaging
- Power cycle pixels based on coarse signal → Reduces power by ~10^3
- Sparse self-triggered readout → Read out only regions with activity

GAMPix: ASIC Architecture / Specs



GAMPix v1

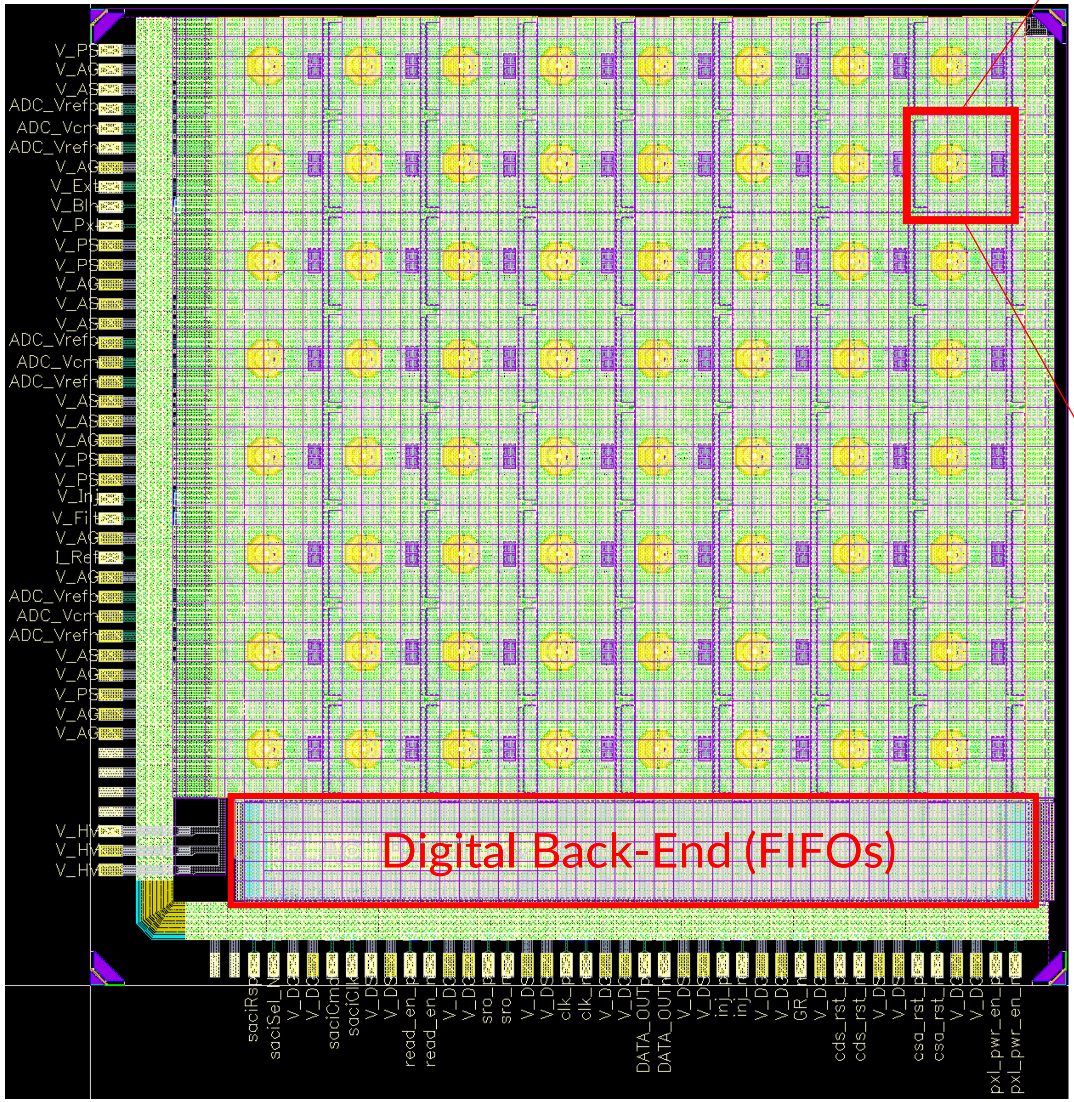
GammaTPC

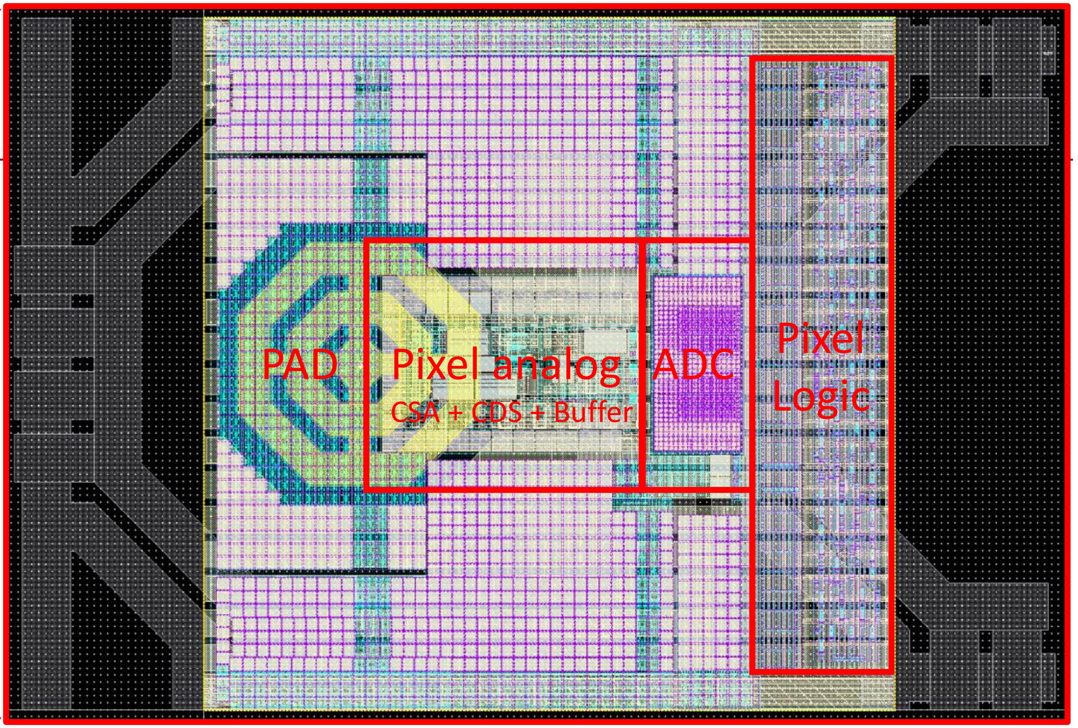
Param	Value
Technology	130 nm CMOS
Supply voltage	1.2 V (nominal), 1.0 V
Temperature	LAr (87 K)
Pixel size	**500 um x 500 um**
Pad size	~ 200 um
Pad capacitance	**~ 500 fF**
Noise – requirement	**< 50 e-**
On power	**~ 250 uW/pixel**
Off power	**~ 300 nW/pixel**
Dynamic range	7000 e- (Qin = ~1.12 fC)
Settling time after trigger	< 5 us
Sampling rate	Up to 2.0 MS/s
Resolution	**10 bit → ENOB = 9 bit (7000 e- /25 e-)**
RC filter	150ns – 600ns (programmable)

Pixelated ASIC - Key features

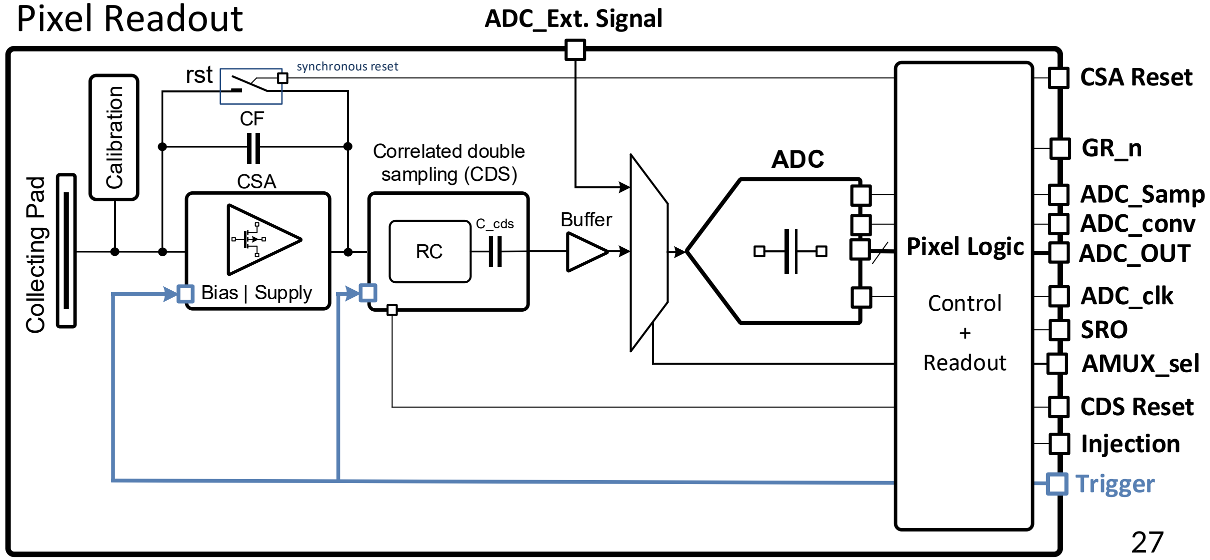
- Synchronous reset pixel readout architecture
- Pad for charge collection → low noise performance
- In-pixel waveform digitization (power- and area-efficient SAR ADC)
- Power pulsing scheme → Enabled by coarse readout

GAMPix: ASIC Layout

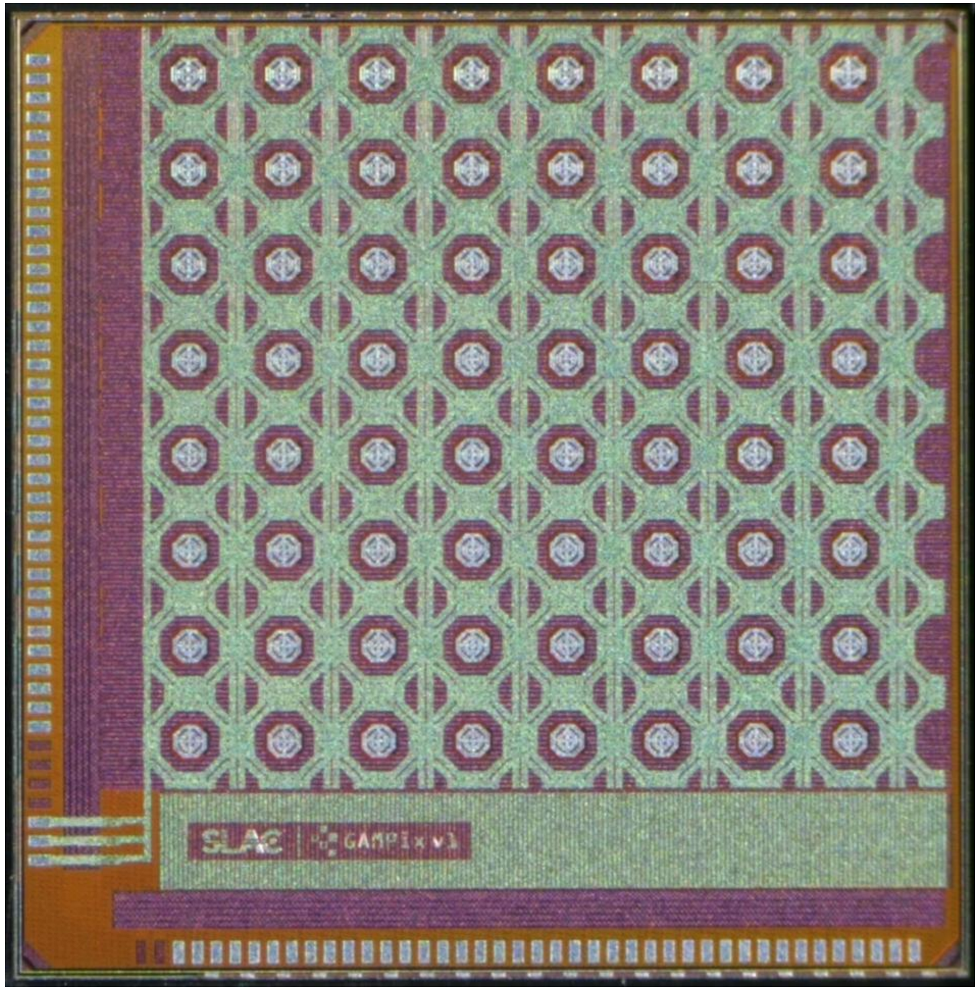


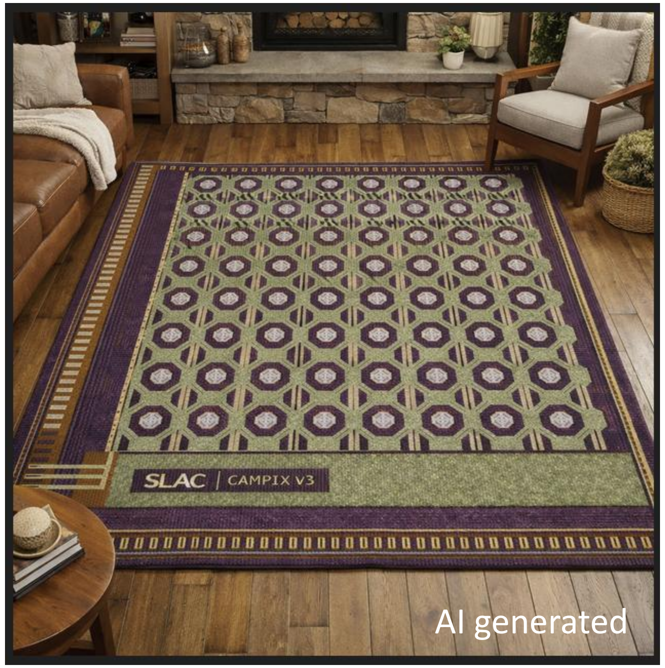


Pixel Readout



GAMPix: ASIC Photograph

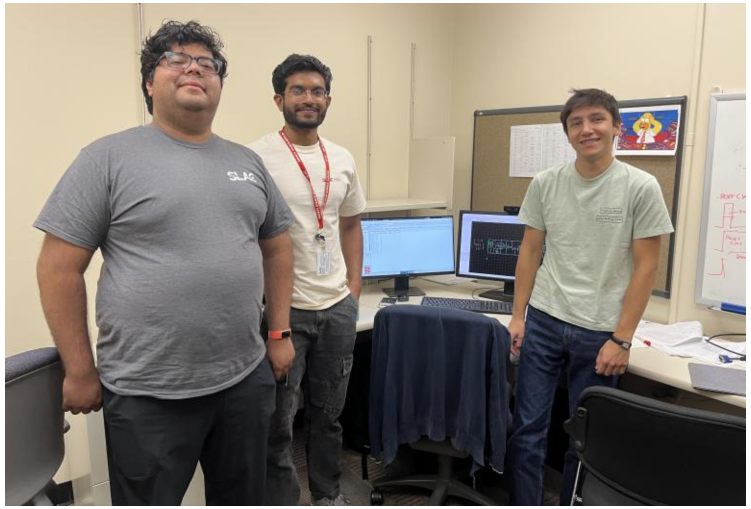




Pixelated ASIC - R&D prototype

- 130 nm CMOS technology
- 5 mm x 5 mm MPW

TID-ID INTEGRATED CIRCUITS DEPARTMENT



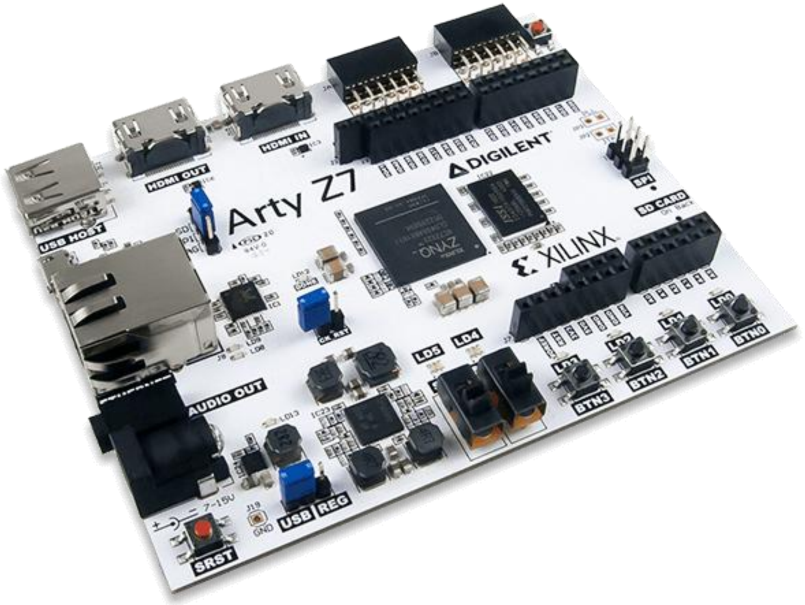
Students involved on the ASIC design/integration

(From left to right)

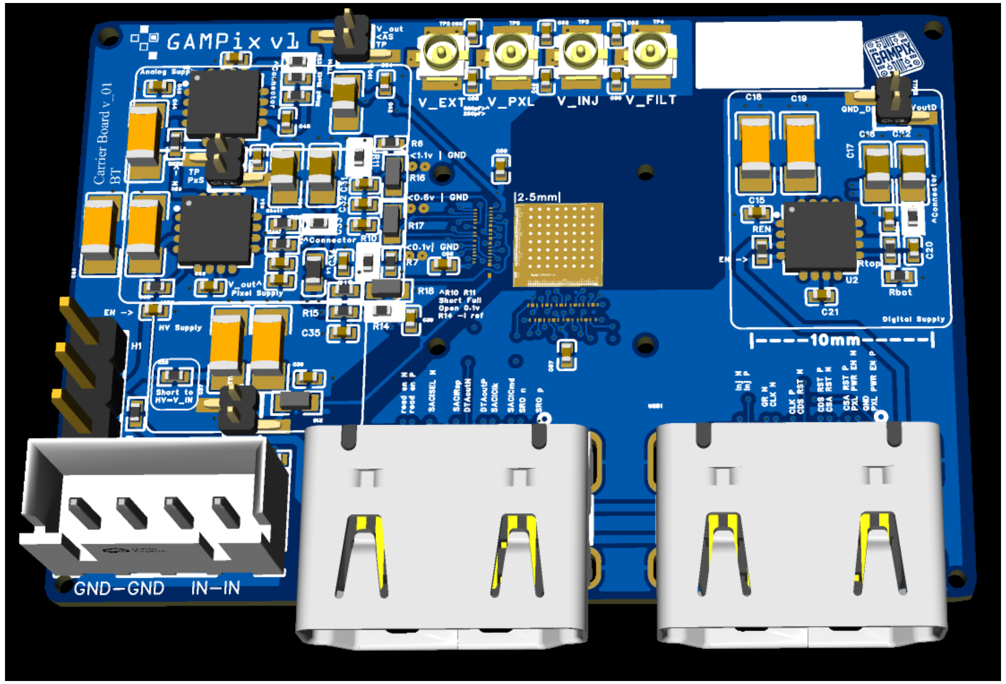
- Humza Syed (BSc)
- Nihar Ahire (MSc)
- Mattia Amadori (PhD)

GAMPix: Toward Prototype Testing

Artix-7 FPGA Development Board

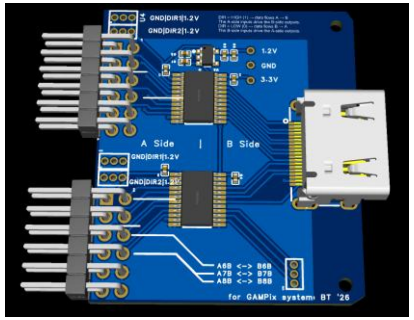


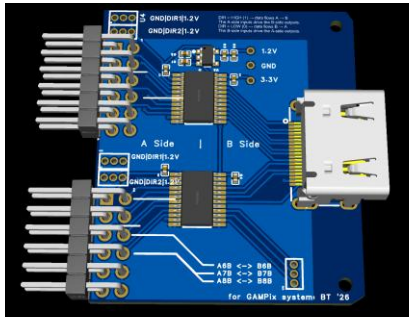
Custom carrier board



ToyTPC

Custom board with level translators





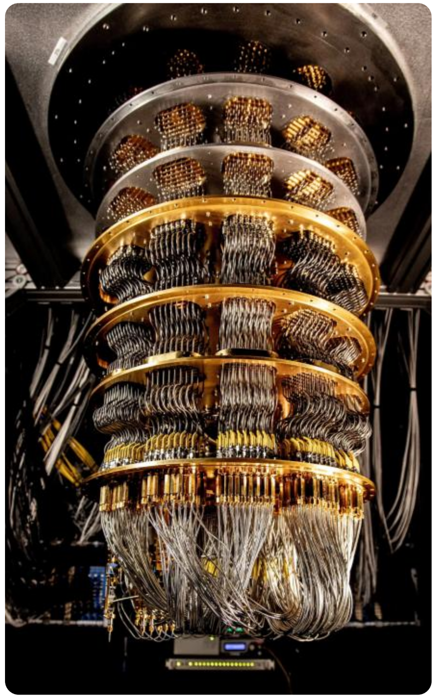
- GAMPix ASICs are at SLAC
- **Custom boards submitted for fabrication. Initial testing to begin soon**

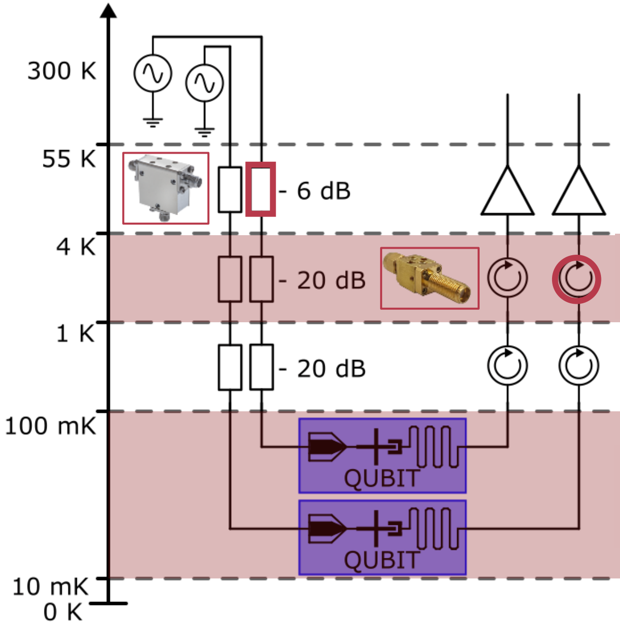
Bahrudin Trbalic
PhD student

C4Q1: Superconducting Sensors and Qubits

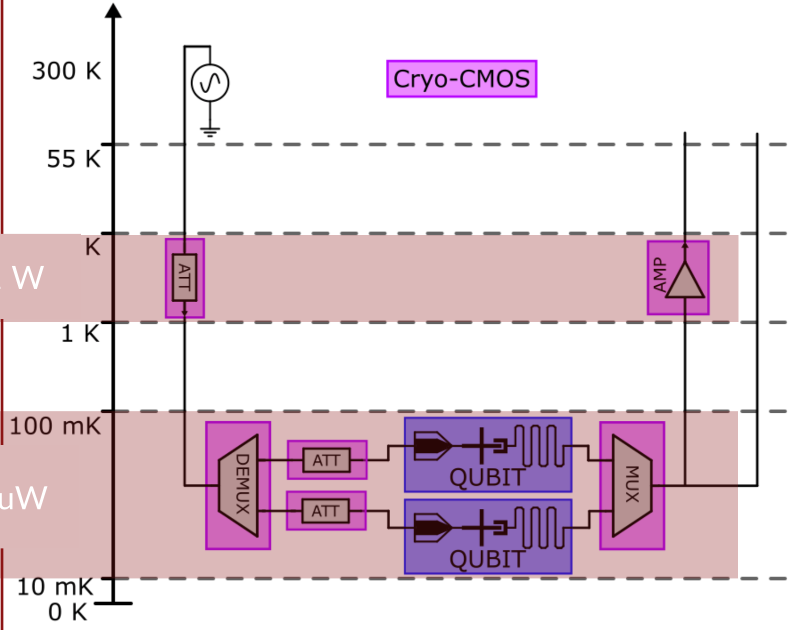
PI: Llorenc Fanals-i-Batllori

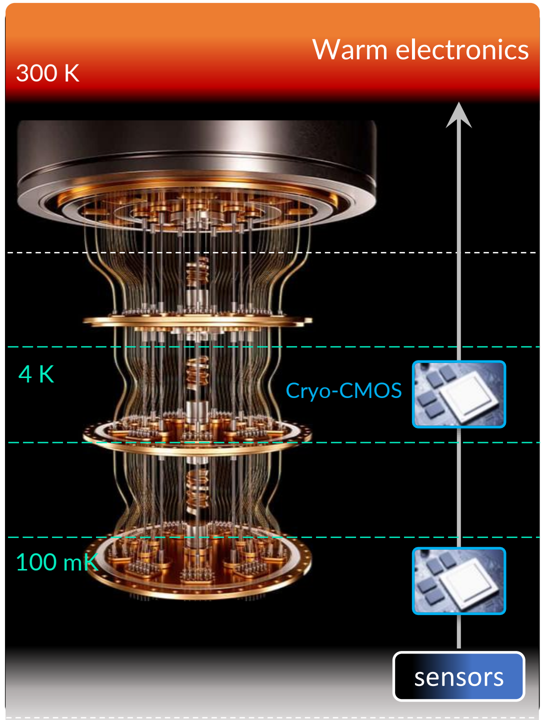
Current cryo systems for quantum computing and rare event experiments rely on bulky and expensive discrete devices





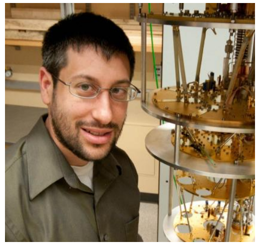
Cryo-CMOS could enable cost-effective, tunable, and scalable quantum computing and rare-event detection systems within power requirements





Quantum computing

Dave Schuster
Stanford professor



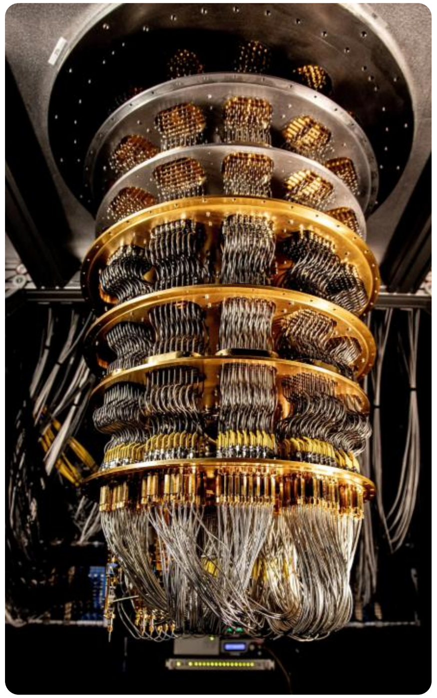
Dark matter

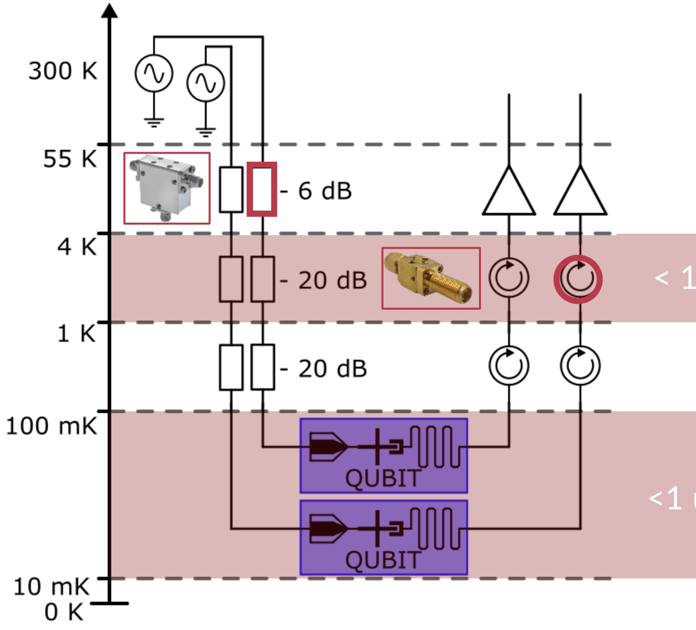
Noah Kurisnky
SLAC scientist

C4Q1: Superconducting Sensors and Qubits

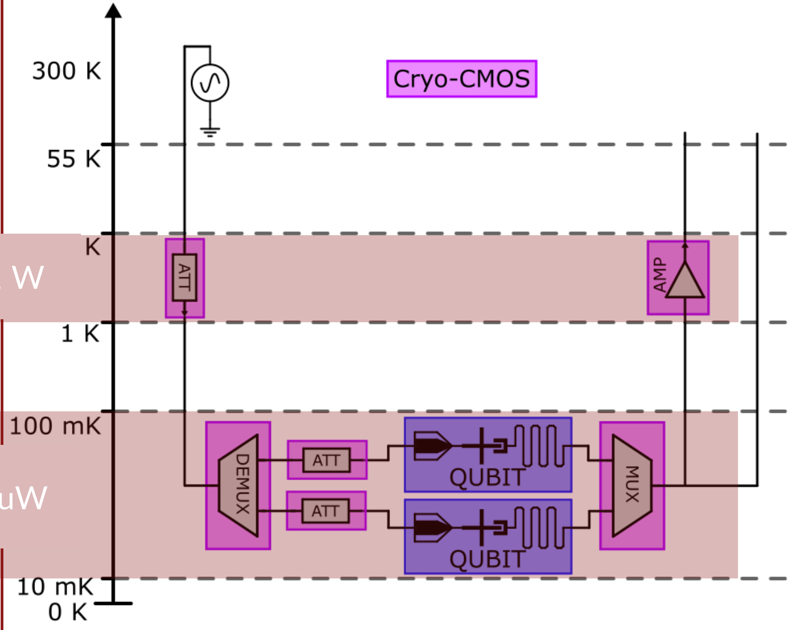
PI: Llorenc Fanals-i-Batllori

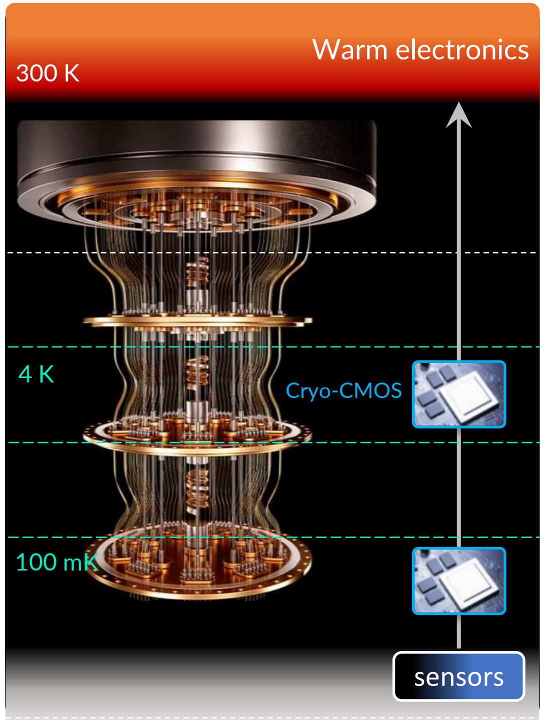
Current cryo systems for quantum computing and rare event experiments rely on bulky and expensive discrete devices

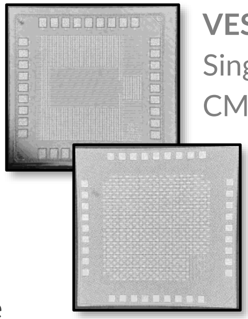




Cryo-CMOS could enable cost-effective, tunable, and scalable quantum computing and rare-event detection systems within power requirements

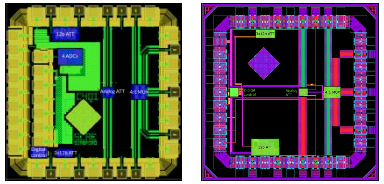






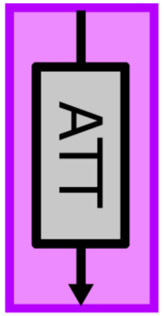
VESPER v1
Single-channel INA
CMOS 28 nm

BOREAS v1
Dual-channel INA
GF 22 nm FDSOI



C4Q1
Tape outed recently
RF SWs & Attenuators
28 nm CMOS | GF 22 nm FDSOI

C4Q1: Tunable Attenuator Key Specifications



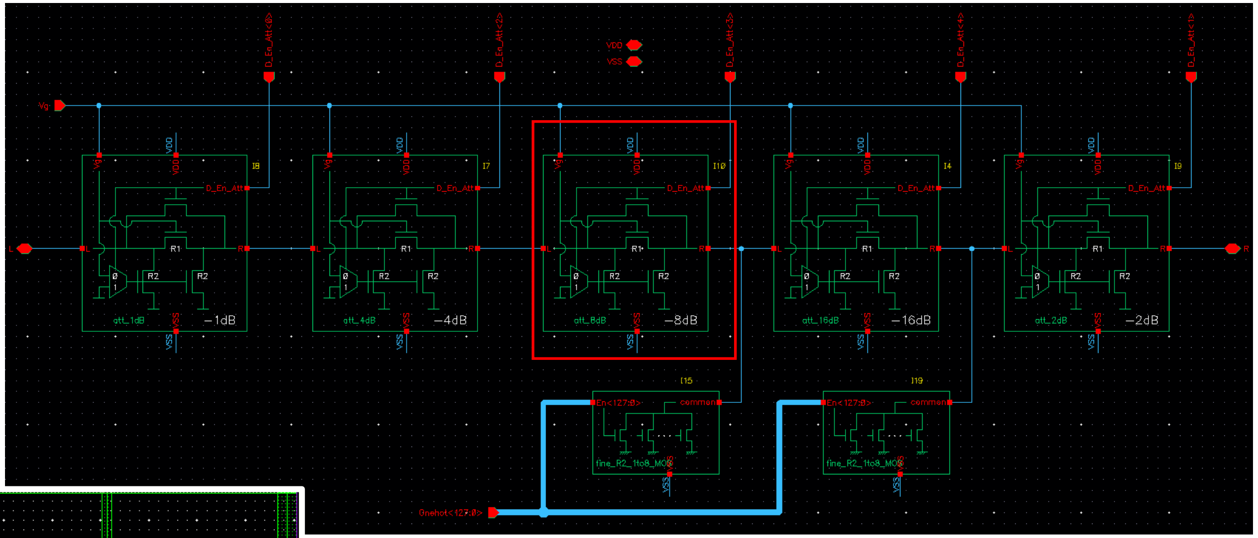
Metric	Magnitude	Comment
Range of operation	[DC - 10 GHz]	
Temperature	4 K – 20 mK	
Resolution	**12 bit**	**Ensure stability over time**
Range of attenuation	**[2 dB, 32 dB]**	**Critical for the readout side**
Power Consumption	**< 1 uW**	**Critical, near to zero after configured**
Zo	50-Ω	
Digital control	--	I2C + parallel

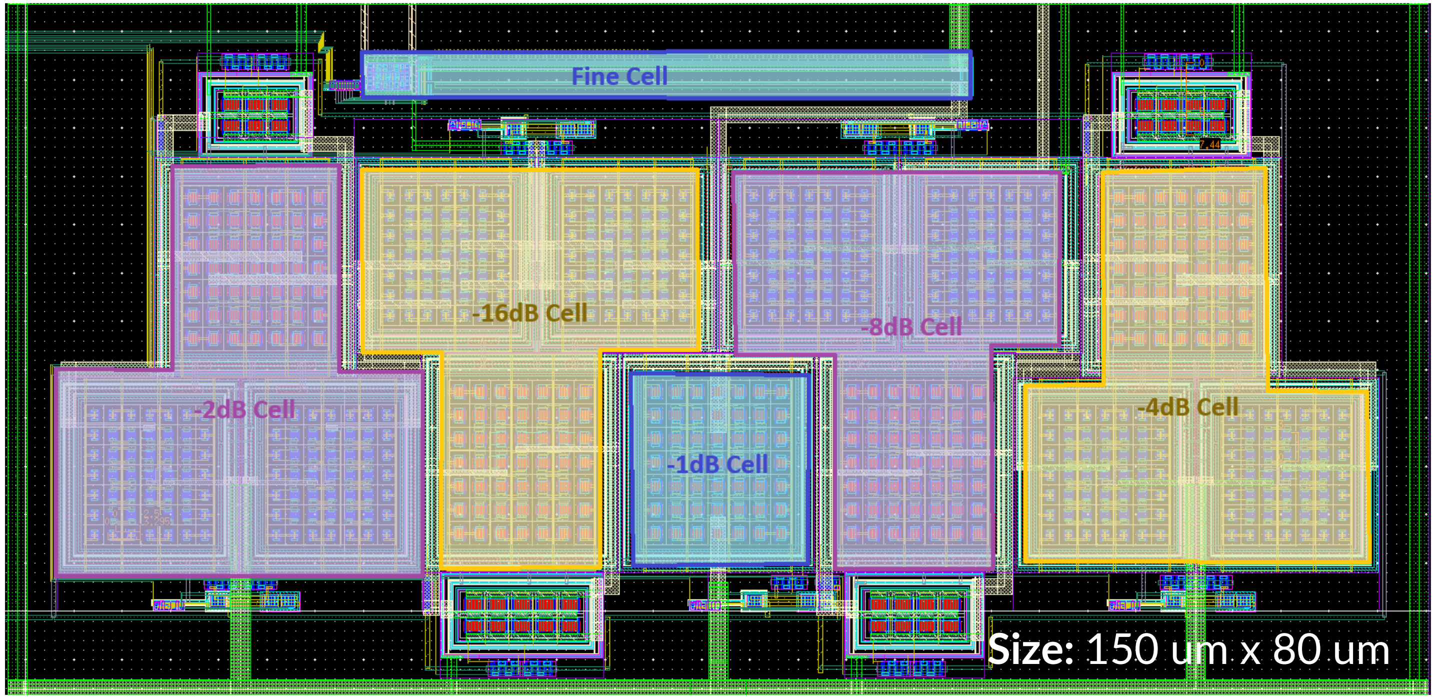
C4Q1: Tunable Attenuator-1 Architecture

Digital Step Attenuator

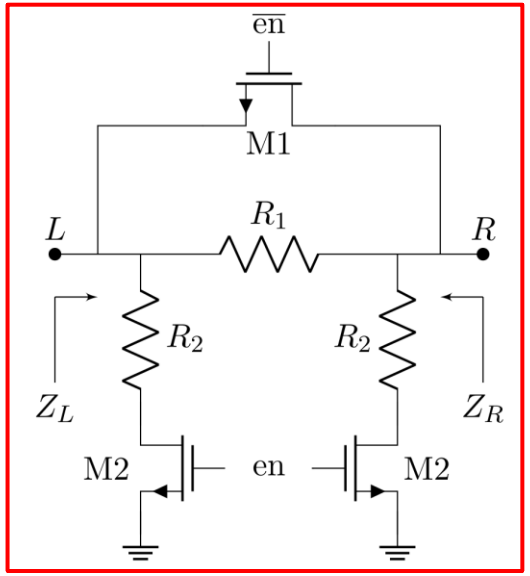
Key features:

- Passive 12-bit architecture for low power
  - 5b coarse + 7b fine
- **Core cells:** π-type attenuator with MOS-resistors
- **Fine cells:** two programmable shunt resistors

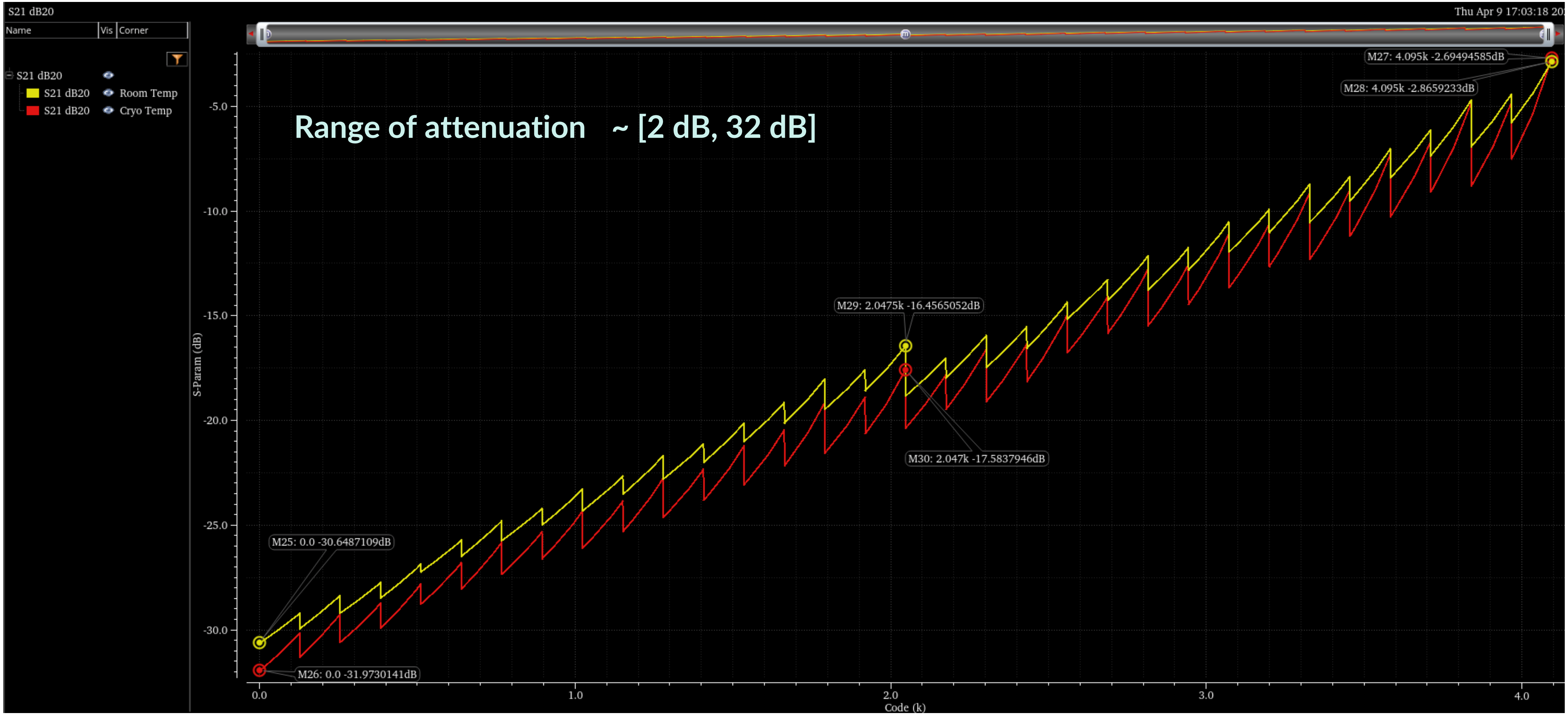




Size: 150 um x 80 um



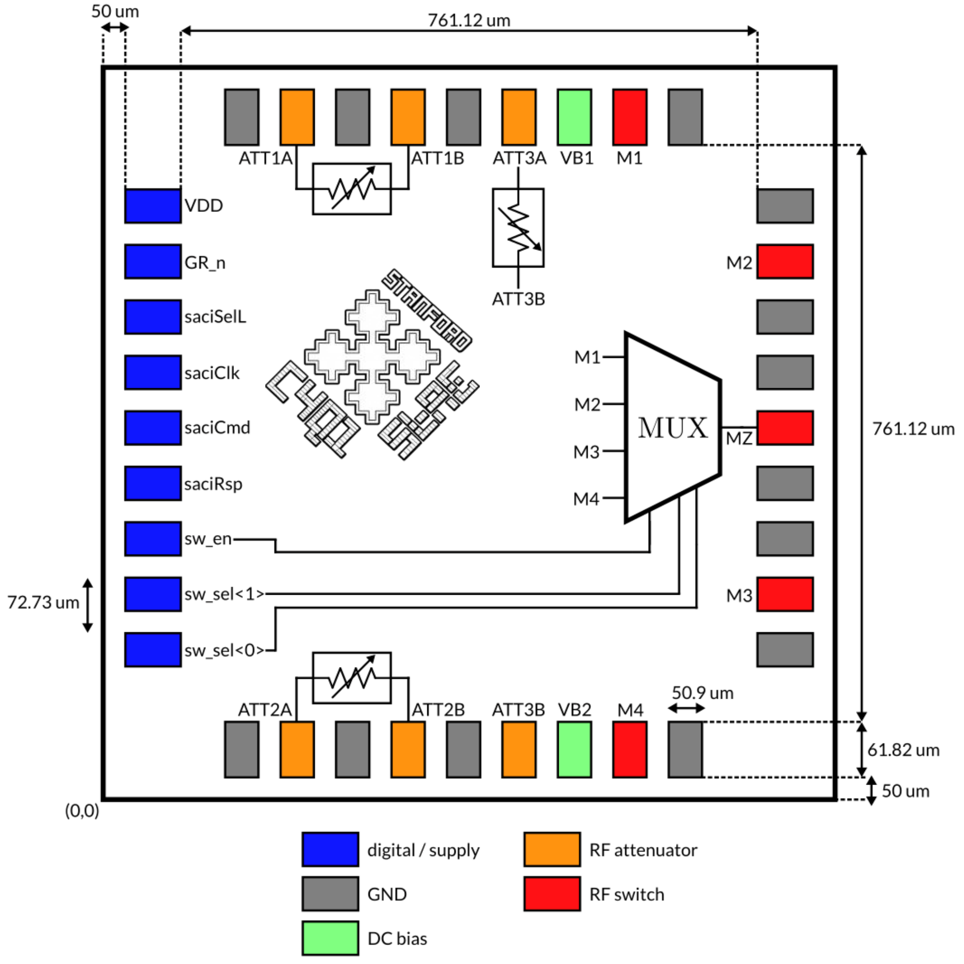
C4Q1: Simulation Results (Attenuation vs Code)



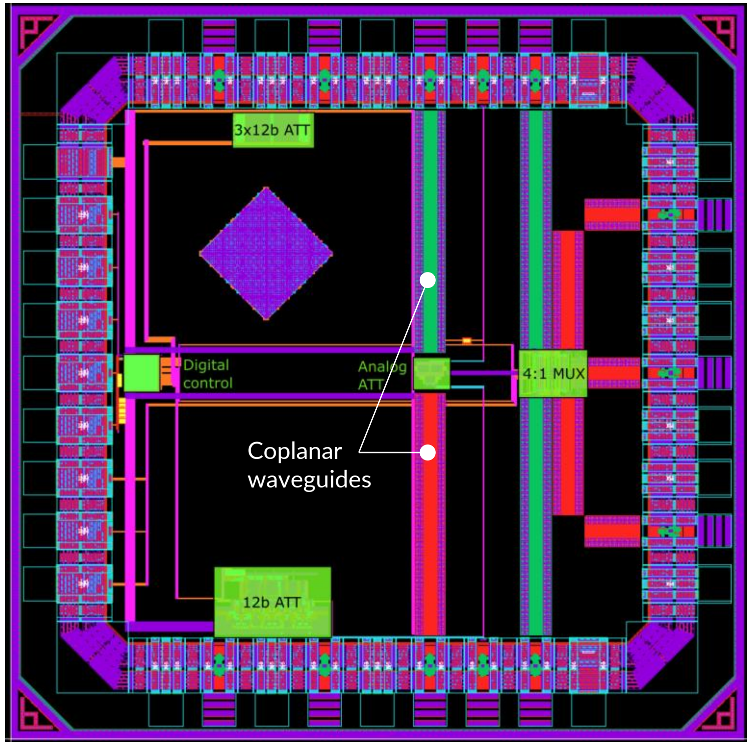
C4Q1: Top Level

GF22FDX/TSMC28

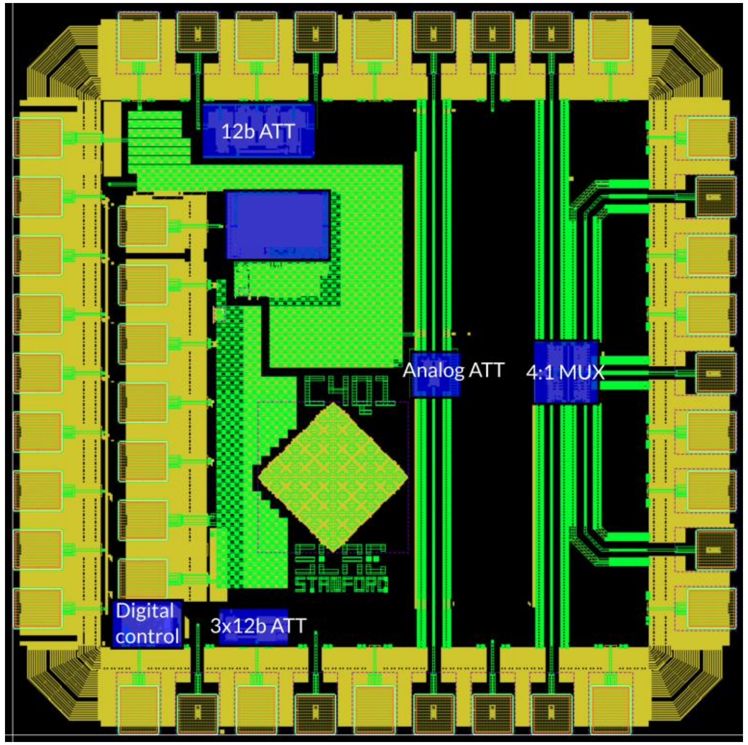
Die thickness: ~200 um



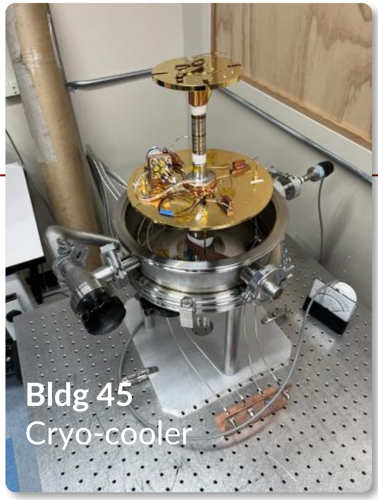
22 nm FDSOI Chip

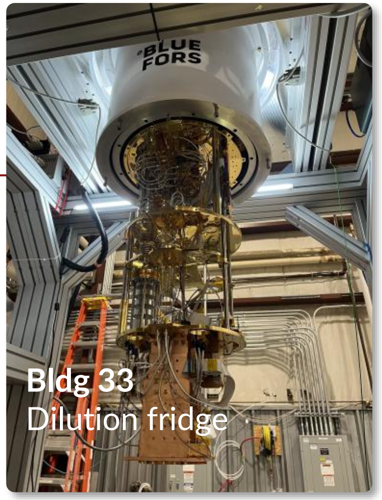


28 nm Chip

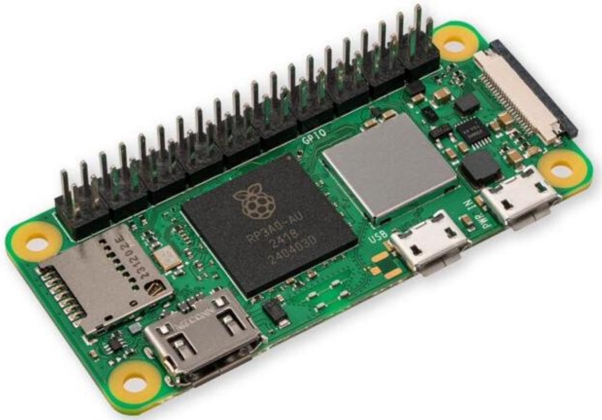


C4Q1: Toward Prototype Testing

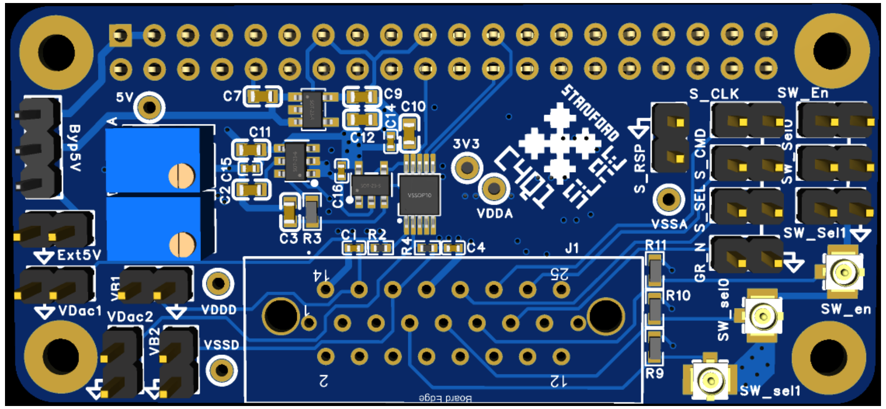




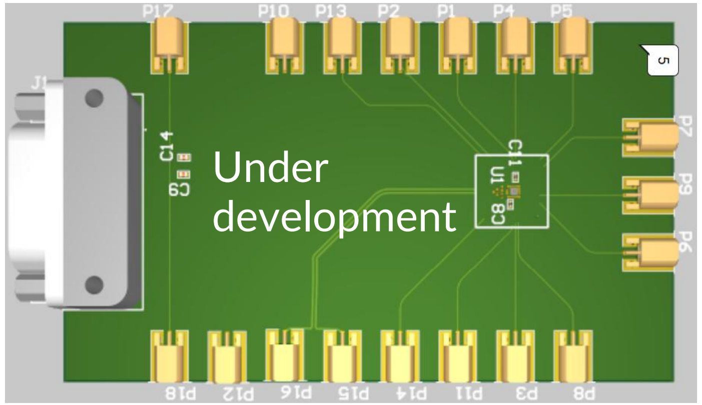
Raspberry Pi evaluation board



Custom interface board



Custom carrier board



- C4Q1 ASICs will be delivered at SLAC in July.
- Custom interface board submitted for fabrication. Carrier board under development.
- **Chip characterization will start in August.**

Joan Serrano Aporta
MSc Student

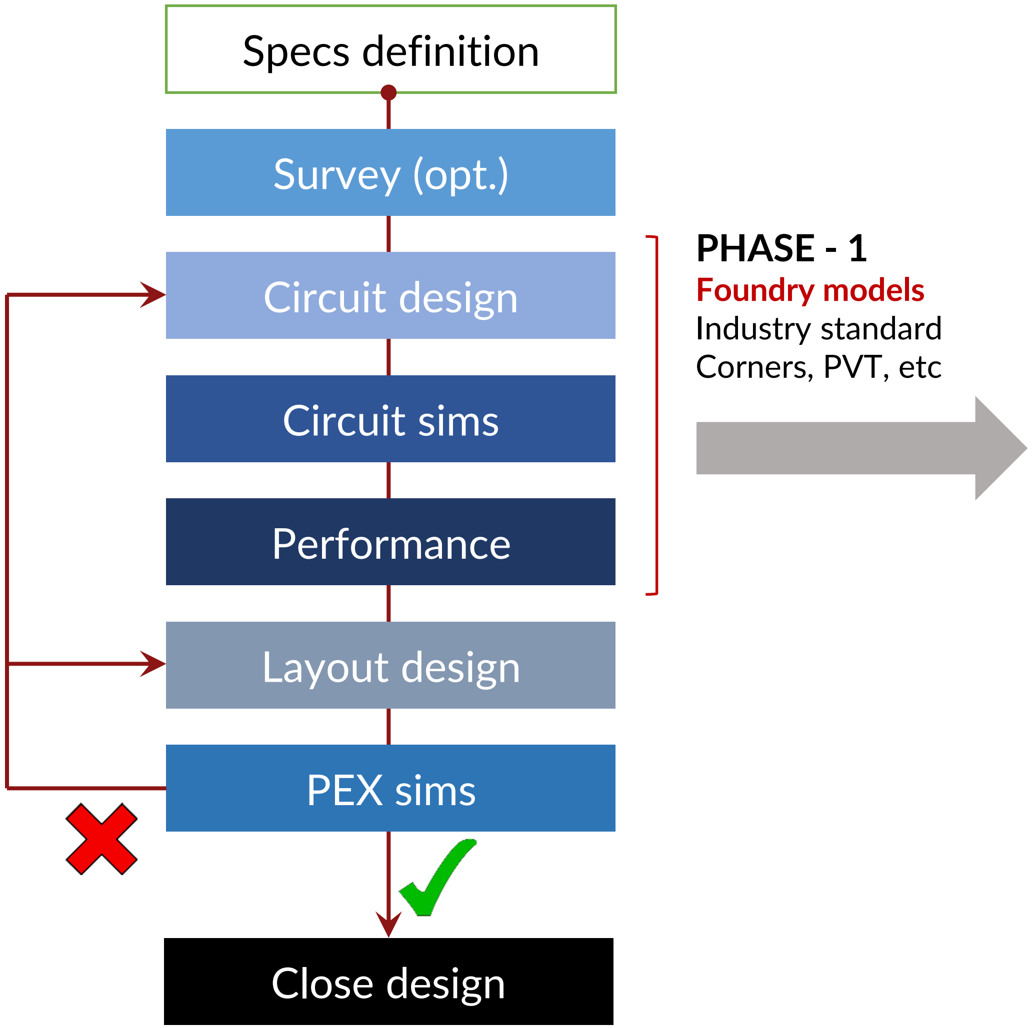
Acknowledgments

- **SLAC**
  - Ann Wang
  - Tom Shutt
  - Brian Lenardo
  - Noah Kurisnky
  - Shawn Henderson
  - Bahrudin Trbalic
  - Will Johnson
  - Marissa Hsu
  - Kevin Boateng
  - Chase Parker
  - Valeria Zarco
  - Ariella Atencio
  - Michael Lu
  - Mattia Amadori
  - Nihar Ahire
  - Kevin Boateng
  - Humza Syed
  - Matt Cherry
  - Andrew Young
  - Victor Turbiner
  - Joan Serrano
  - Miao Yu
  - Hugo Hernandez Herrera
  - Llorenç Fanals-i-Batllori
  - Gang Liu
  - Aseem Gupta
  - Bojan Markovic
  - Lorenzo Rota
  - BUAP team
- **LBL**
  - Panagiotis Zarkos
  - Timon Heim
  - Bryan Kwe
  - Aikaterini Papadopoulou
  - Carl Grace
  - Maurice Garcia-Sciveres
  - John Groh
  - Meriam G. Bautista-Jurney
- **Stanford**
  - David Schuster

Many others!

General Backup

Design flow

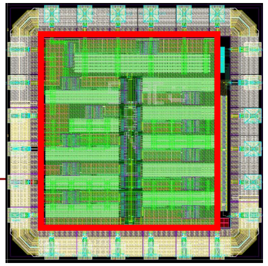


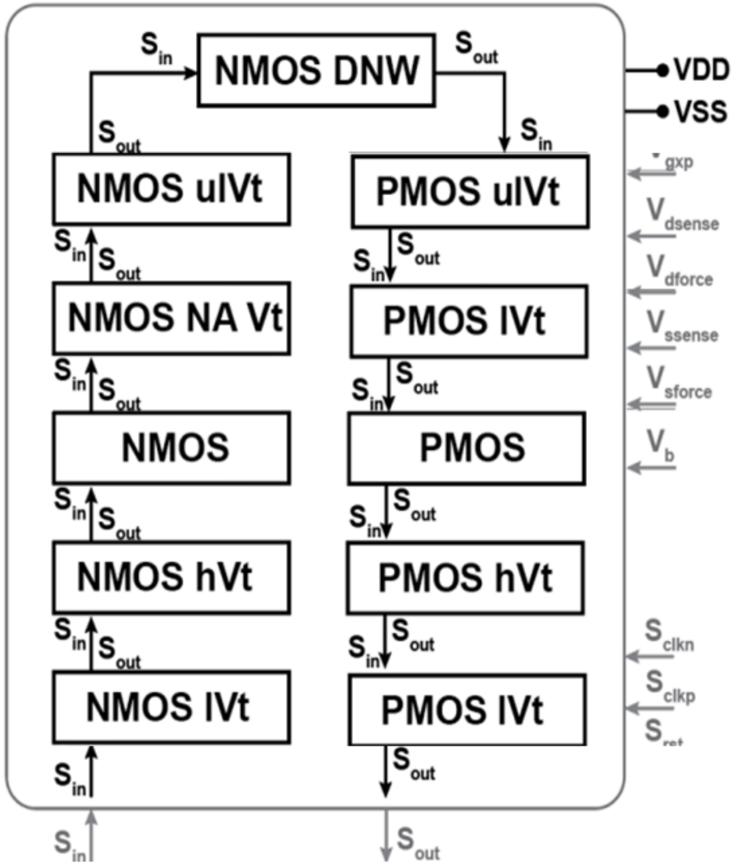
PHASE - 1
Foundry models
Industry standard
Corners, PVT, etc

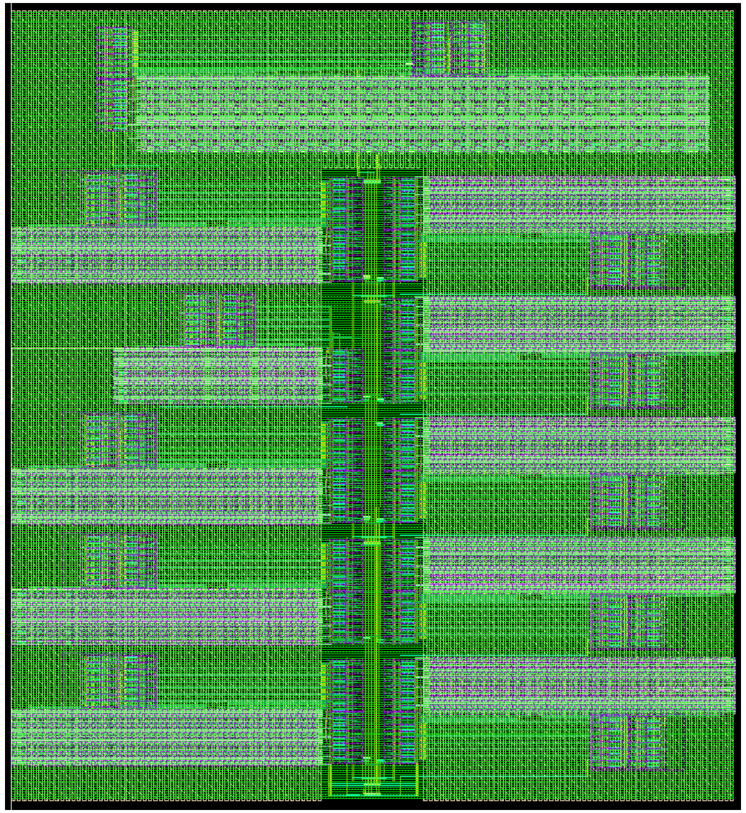
PHASE - 2
Cryo models (if available)
Cold conditions
Extrapolate params
Corners, PVT, etc

Backup Cryo-PDK

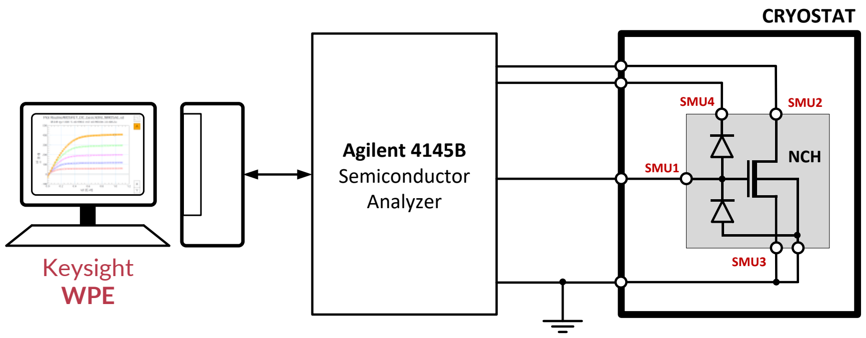
Cryo-PDK: Core Cell and Device Flavors



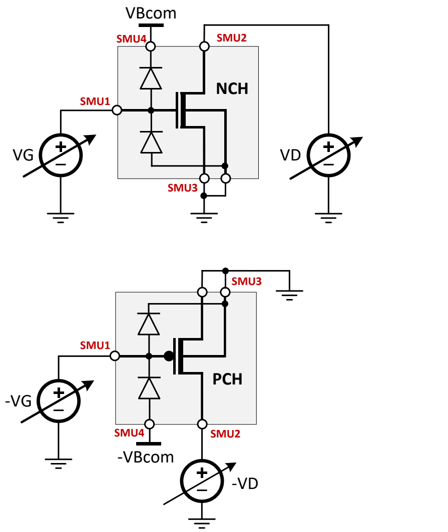




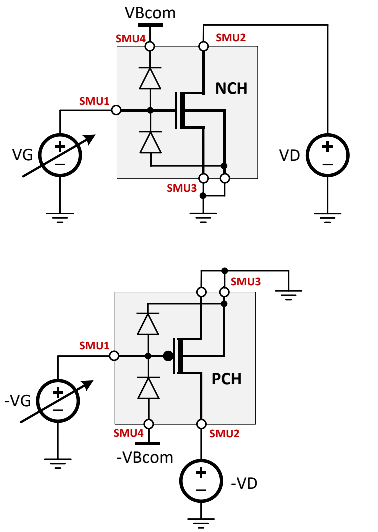
Cryo-PDK: DC Characterization (130 nm Example)

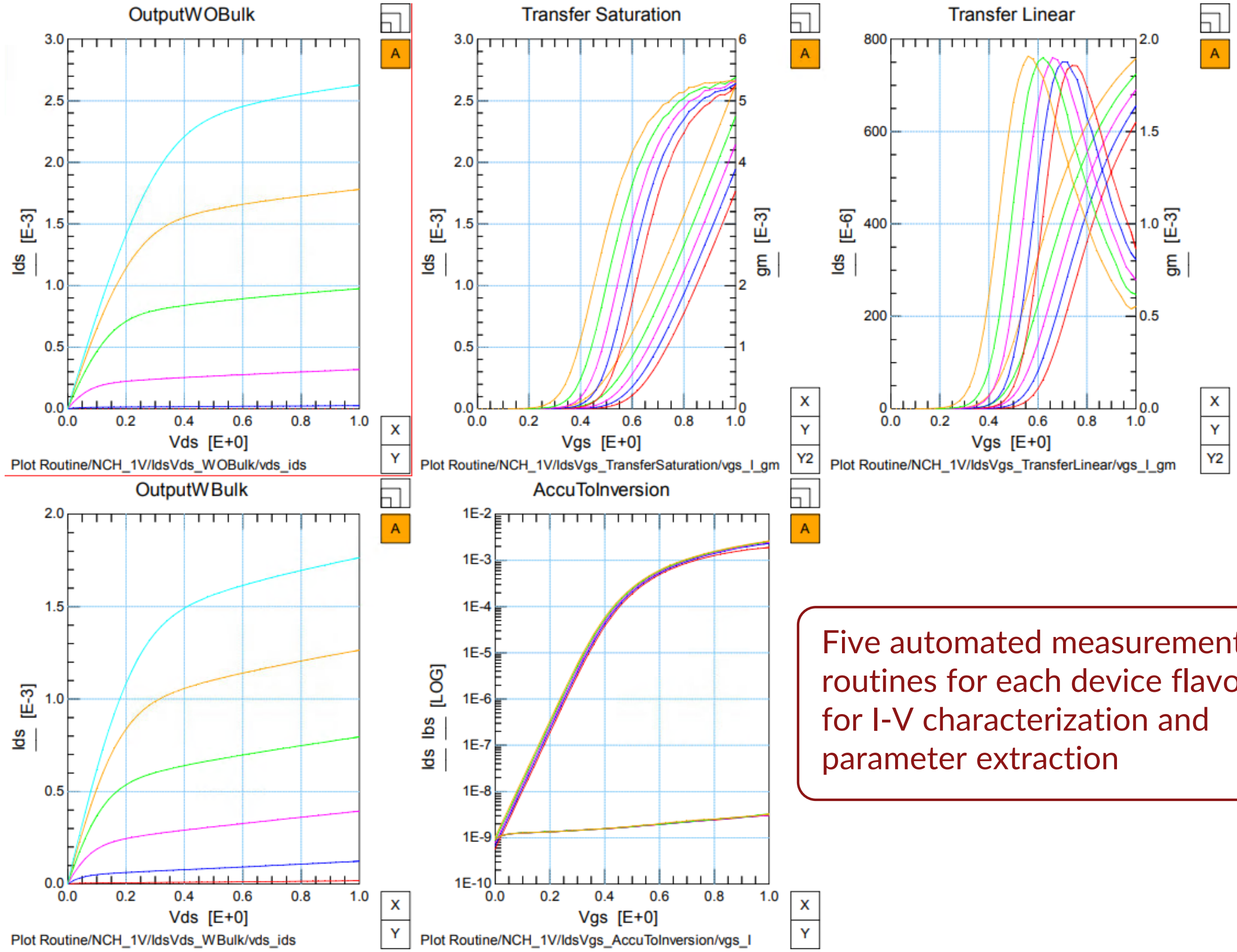


I_{ds} vs V_{ds} Curve @ Different V_{gs}



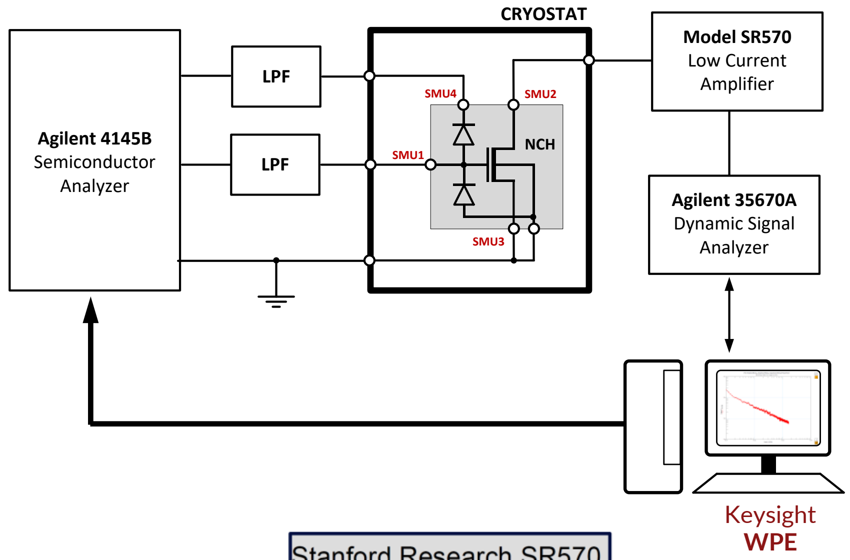
I_{ds} vs V_{gs} Curve @ Fixed V_{ds}

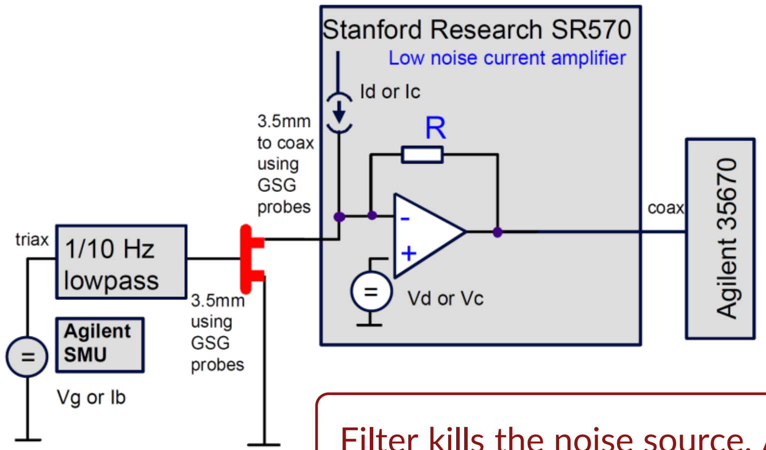


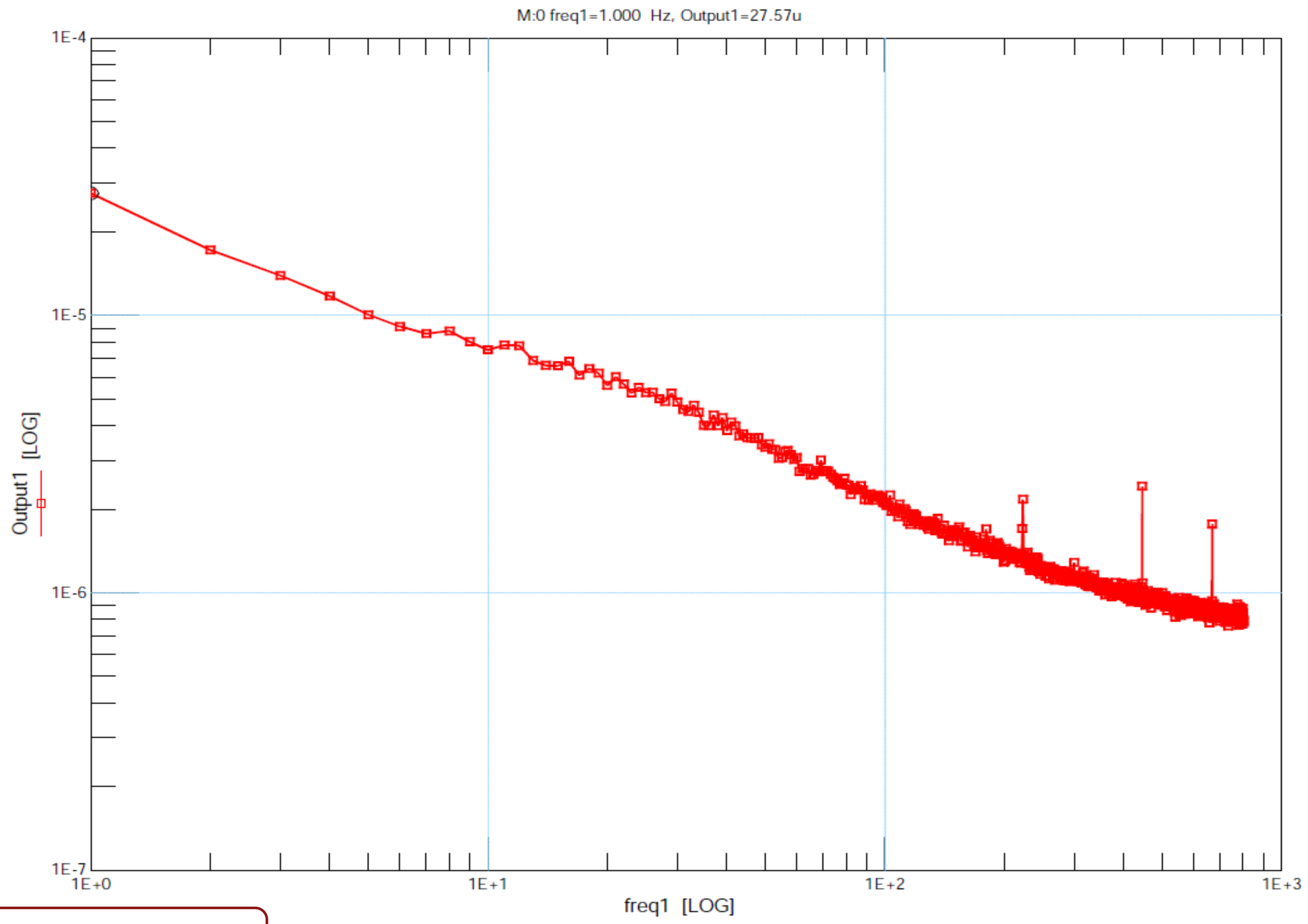


Five automated measurement routines for each device flavor for I-V characterization and parameter extraction

Cryo-PDK: Noise Characterization (130 nm Example)







Filter kills the noise source. Amplifier lifts the DUT signal. Both serve SNR (from opposite directions)!

Backup PHOCA

PHOCA: List of Key IPs

Designed for operation at room and/or cryogenic temperature

[*] HEPIC intern

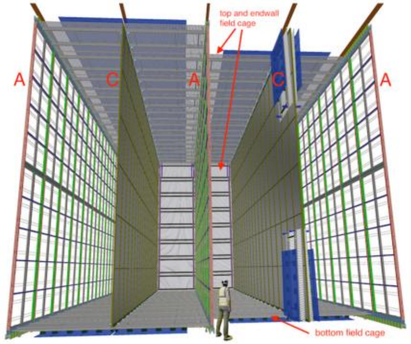
IPs developed as part of KA25 in 2025:

- Transimpedance amplifier (TIA) for PMT/SiPM readout (IC team, M. Hsu)
- Semi-gaussian shaper (IC team)
- 100 MS/s, 12b Analog-to-Digital converter (IC team, K. Boateng)
- High-speed serializer, input/output CML drivers (IC team)
- Bandgap reference (BGR) circuit (IC team, BUAP)
- Low dropout (LDO) capacitor-less voltage regulator (IC team, BUAP)
- Top-level integration (IC team, V. Turbiner)

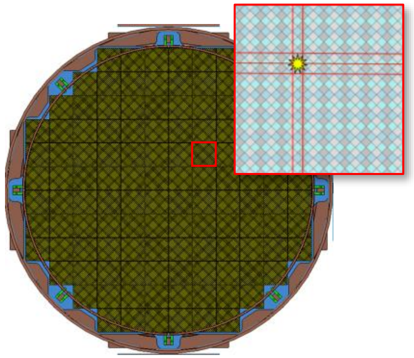
TPC sensing elements

a TPC typically combines

Electrical charge readout
(e.g., wires, strips, pixelated planes)



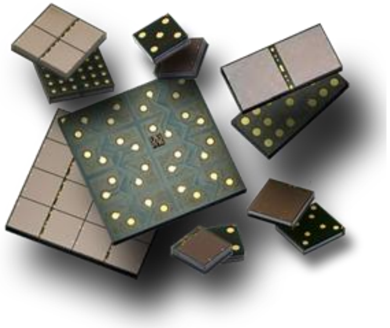
DUNE
[B. Abi et al 2020 JINST 15 T08008]


nEXO
[DOI: 10.48550/arXiv.1907.07512]

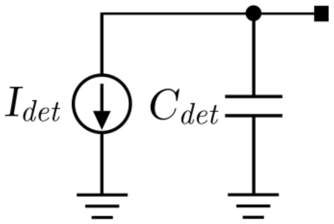
Optical sensors
(e.g., photomultiplier tubes, silicon photomultipliers)

PMTs

SiPMs



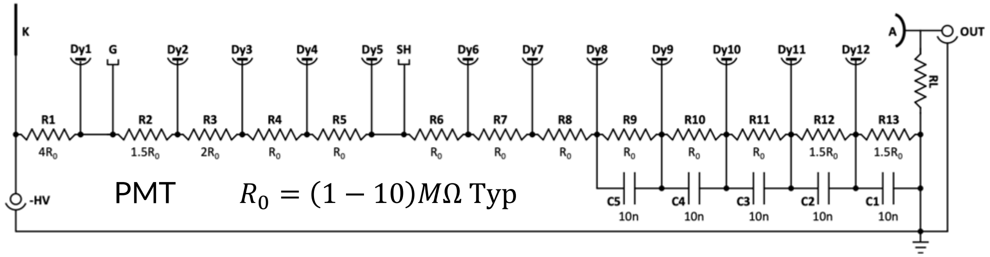
Simplified model



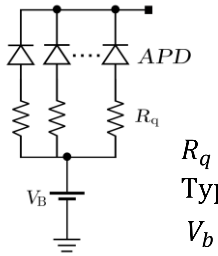
$C_{det} = Detector\ cap$
Typ: $\sim(50-200)\mathrm{pF}$

$I_{det} = Detector\ current$
Typ: few pA

Simplified models



PMT $R_0 = (1-10)M\Omega$ Typ



SiPM

$R_q = Quenching\ res$
Typ: $\sim(100-500)\mathrm{k\Omega}$
$V_b = (24-30)V$ Typ

Features

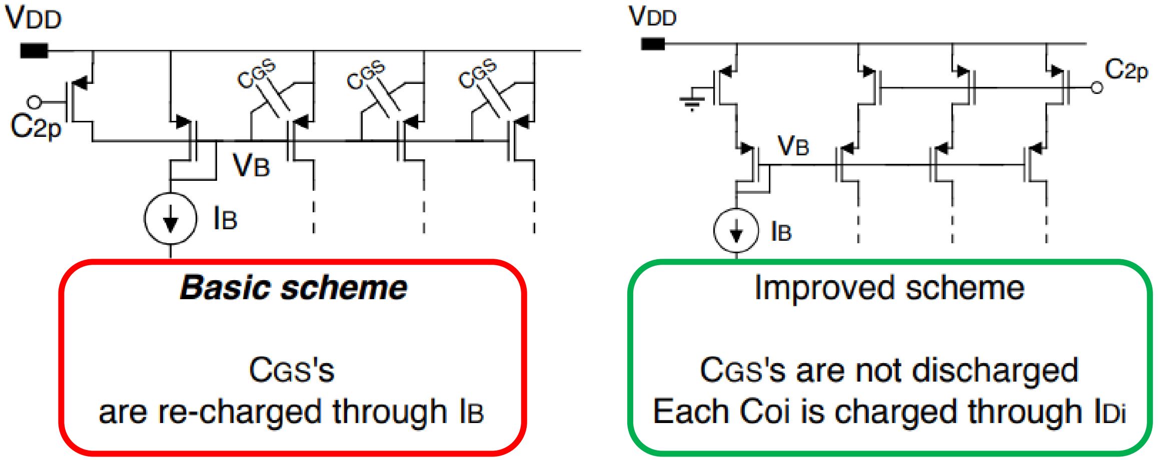
- Fast signals: ~ns
- High capacitance: ~nF
- High internal gain: ~10^6

Backup GAMPix

GAMPix: Power Pulsing

Power Pulsing

- Key problem: re-charge capacitance {Current sources cap. / Compensation cap.}
- #1 - Current source turn-off



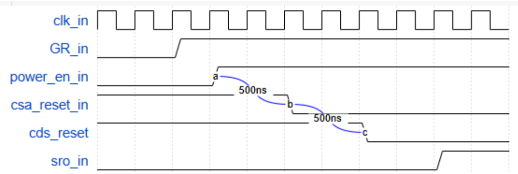
- **Tight power budget allows only for a single matrix bias for the entirety of the ASIC.**
- The **biasing branch is always on** and sets the voltage across every Cgs to have fast turn on times
- Tight power budget → **5uA bias current**
- **5uA / 64 = 78 nA per Pixel →** power overhead for other blocks

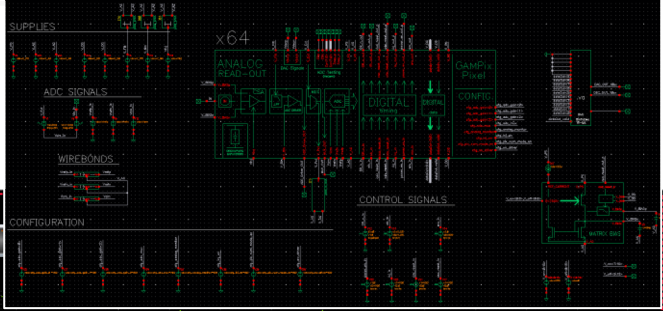
Limited design possibilities:

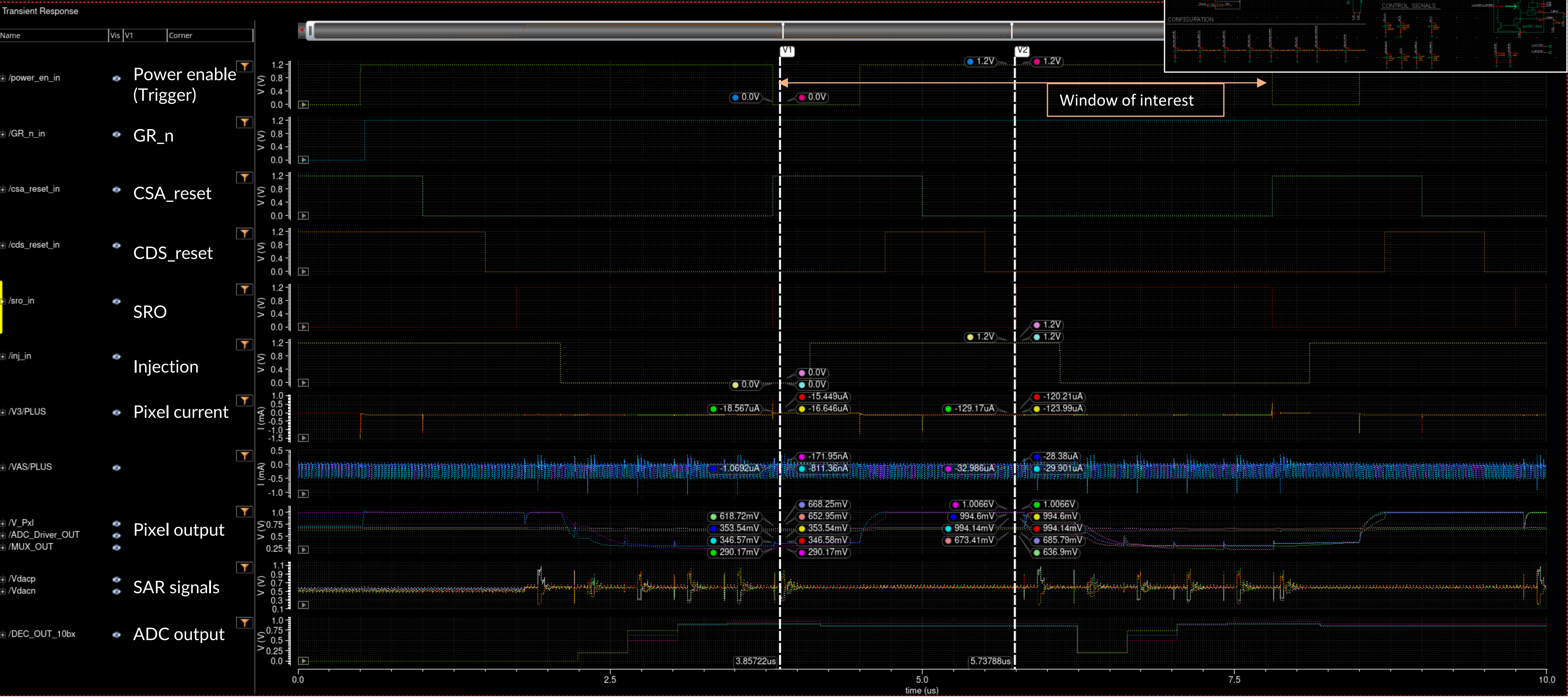
- **Bias MOSFET** should be **2.5V LVT** to reduce leakage current
- The tail current generator of the CSA is the same as the bias MOSFET

A. Baschirotto, "LV Analog Design in scaled CMOS technology" – pp:256/263

GAMPix: PEX Results (RT, 160 K, 87 K)

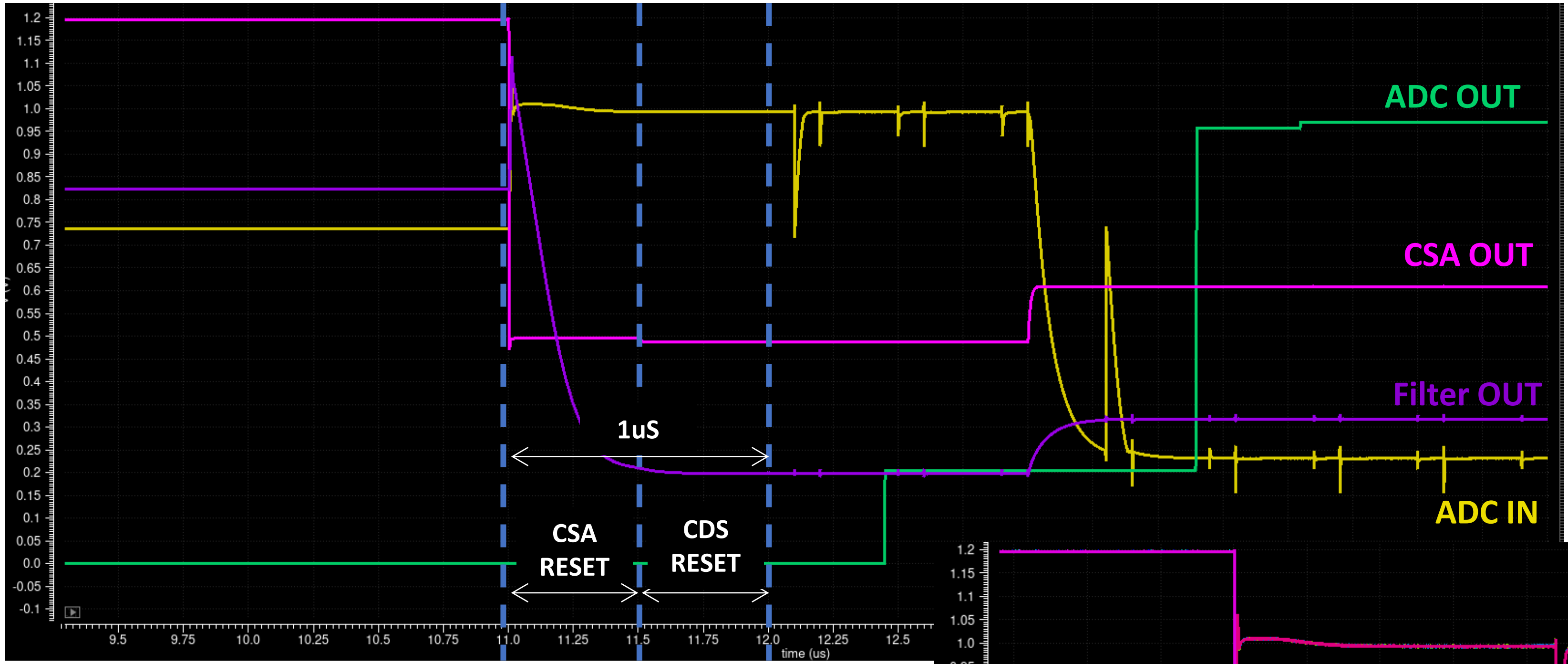






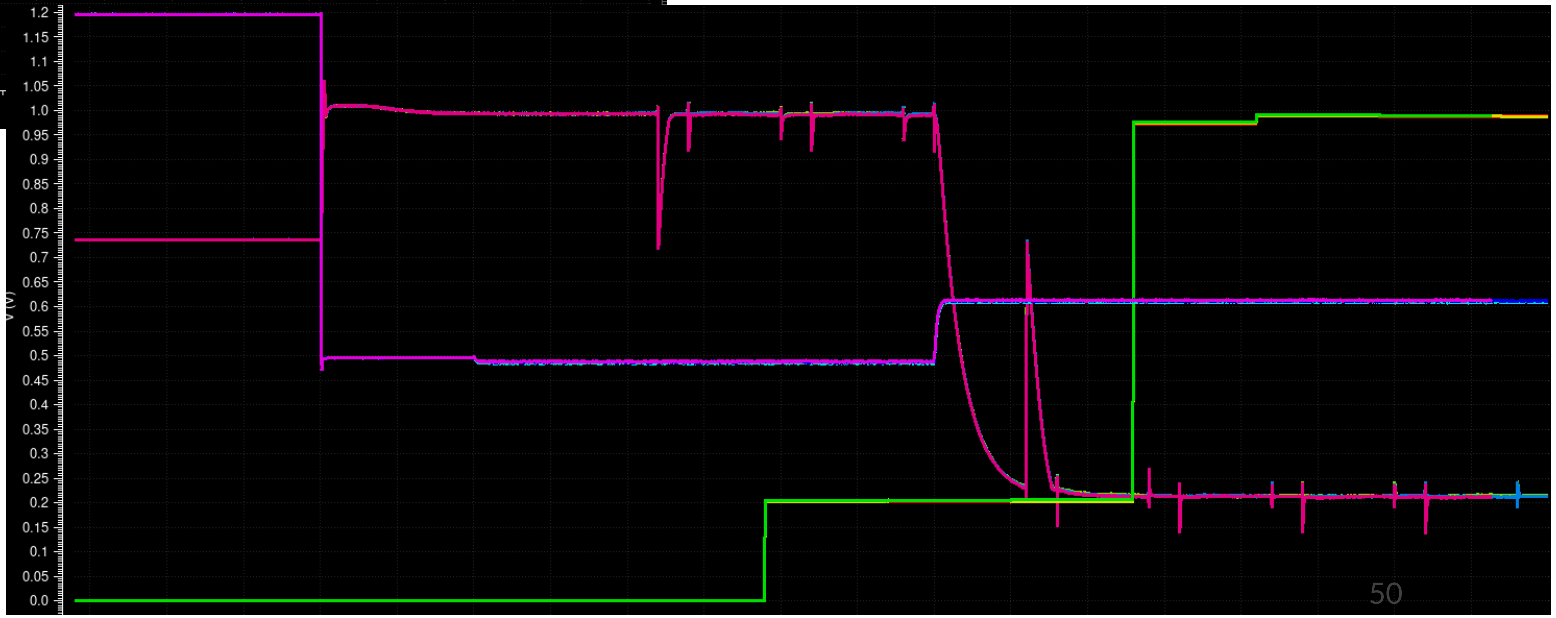
GAMPix Pixel - Signal Chain Simulations at 87K

Power ON	Power OFF
< 200uW/pixel	≈265nW/pixel



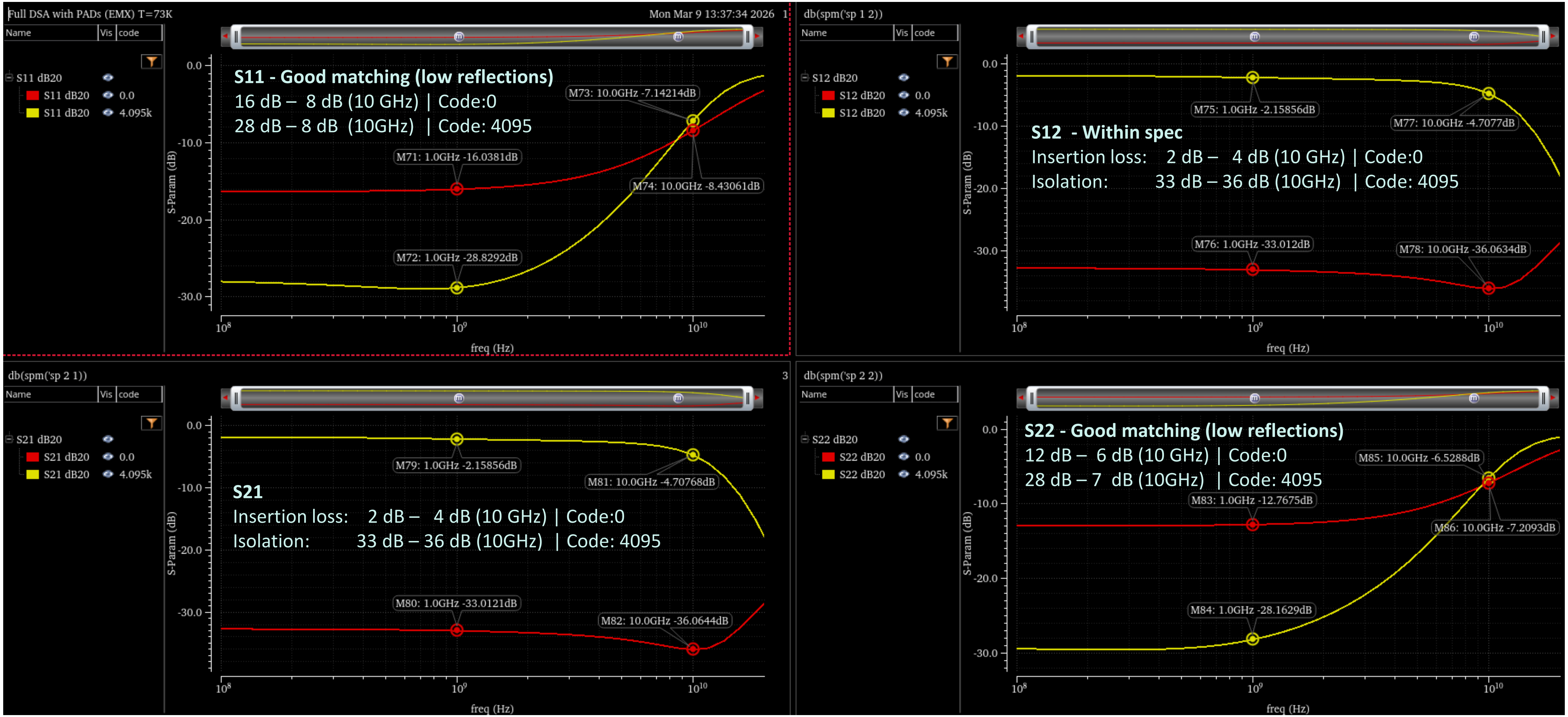
Ideal Transient Simulation 87K

Noisy Transient Simulation 87K

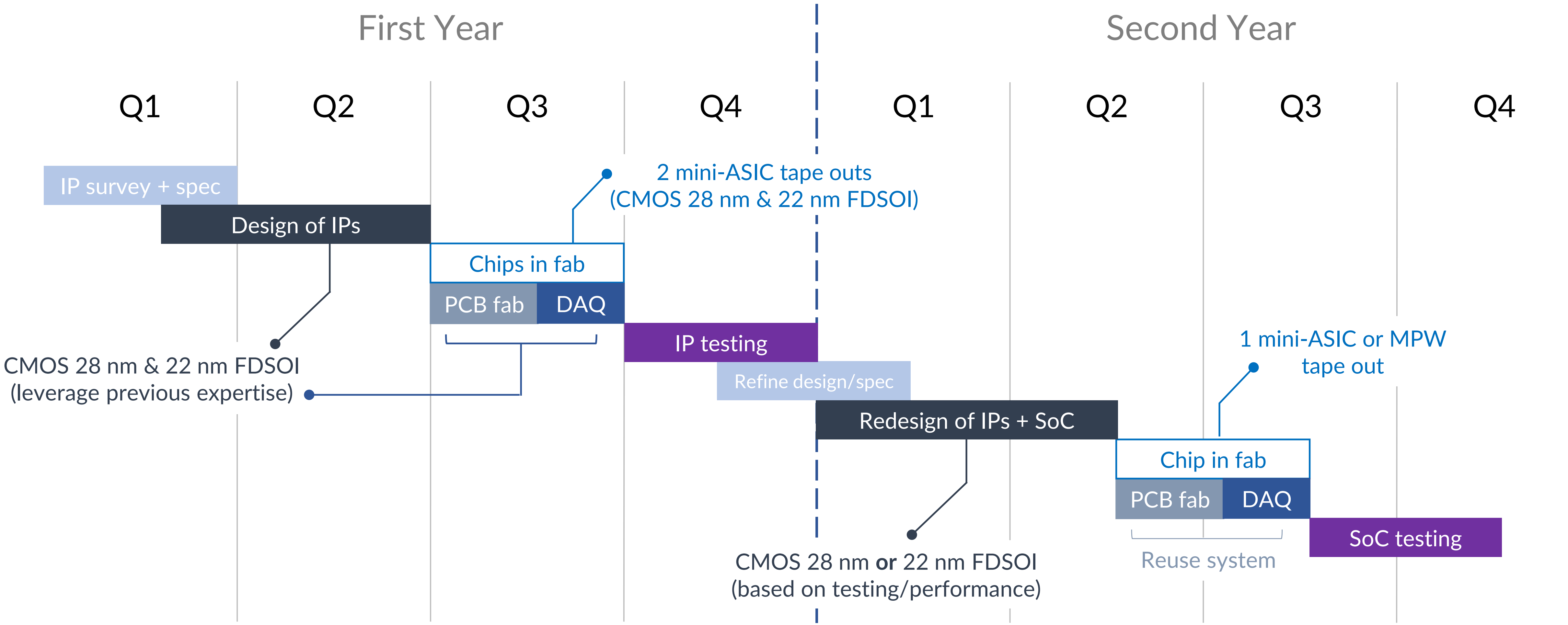


Backup C4Q1

C4Q1: Attenuator-1 Simulation Results (S-Parameters)



Fast-paced LDRD roadmap



C4Q1: R&D Prototype Goals

- Scalable cryo-CMOS RF attenuators/switches for large superconducting qubit arrays
- Shift from active to static RF control with ultra-low-power operation (<1 uW/channel)
- Cryogenic operation at 4 K with a pathway toward mK-stage integration
- Reduced wiring complexity and thermal load for scalable cryogenic systems
- Enable/support next-gen dark matter (Noah) and quantum computing (Prof. Dave) experiments

Noah Kurisnky
SLAC scientist

Dave Schuster
Stanford professor