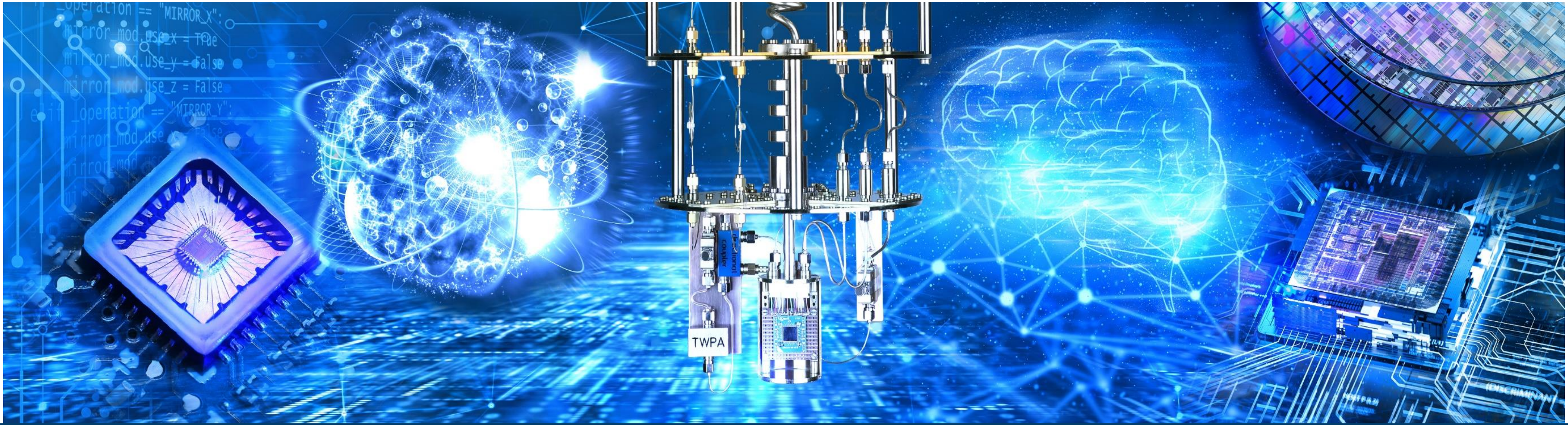

CRYOGENIC CMOS DESIGN FOR SCALABLE QUBIT CONTROL AND READOUT

2026-05-21 |DENNIS NIELINGER, Jonas Bühler, Phanish Chava, Carsten Degenhardt, Andre Kruth, Sabitha Kusuma, Daniel Liebau, Jonas Mair, Lea Schreckenberg, Patrick Vliex, Stefan van Waasen

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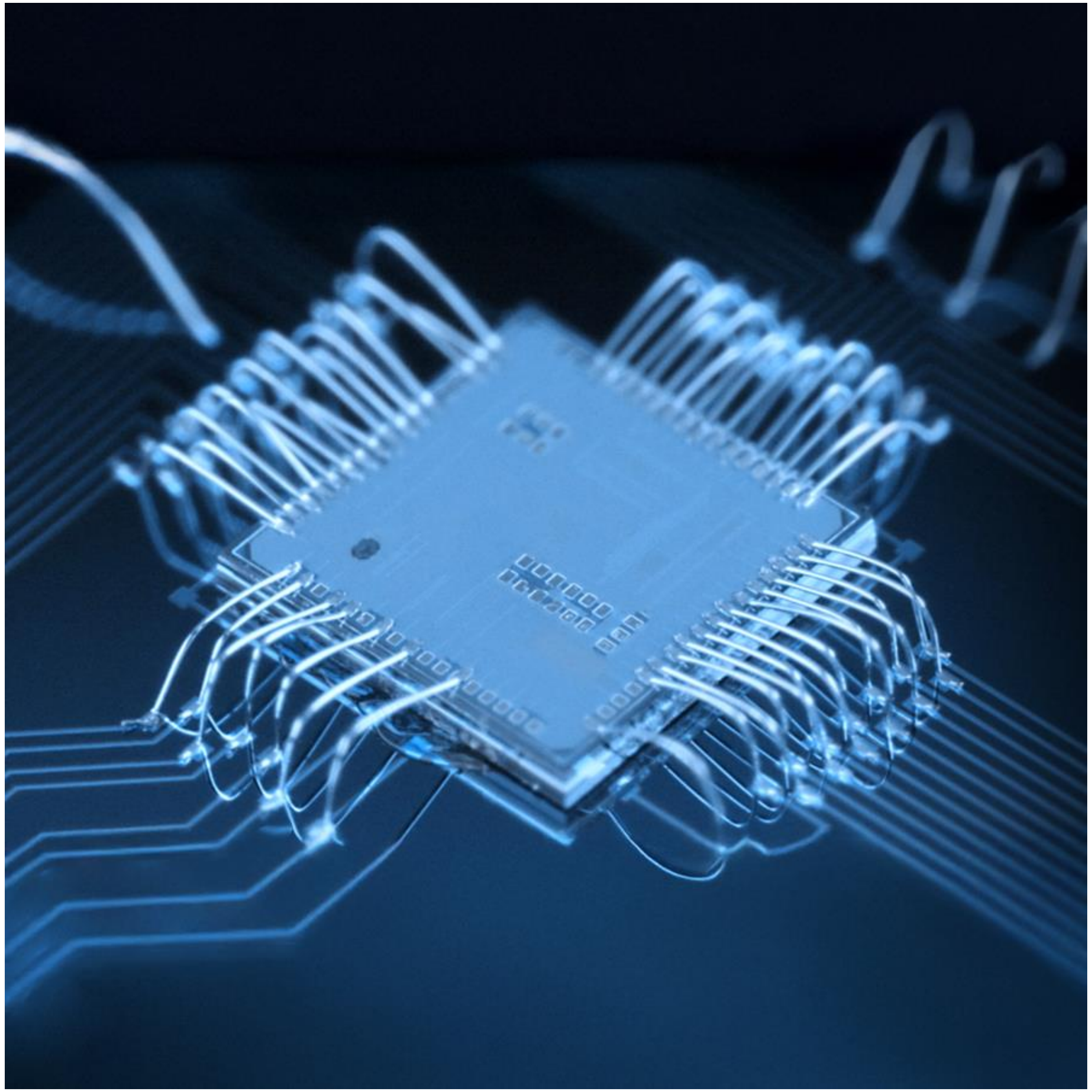
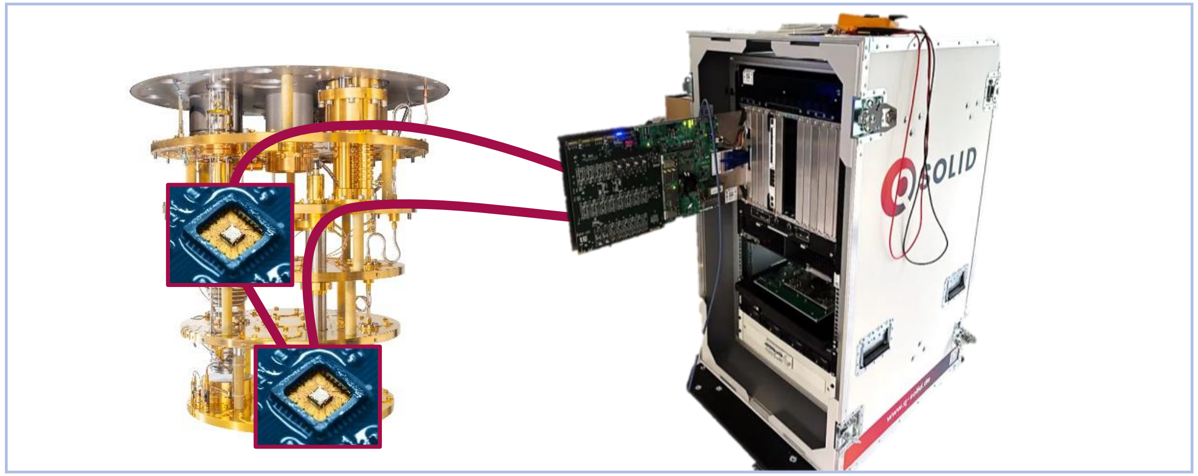
CONTENT

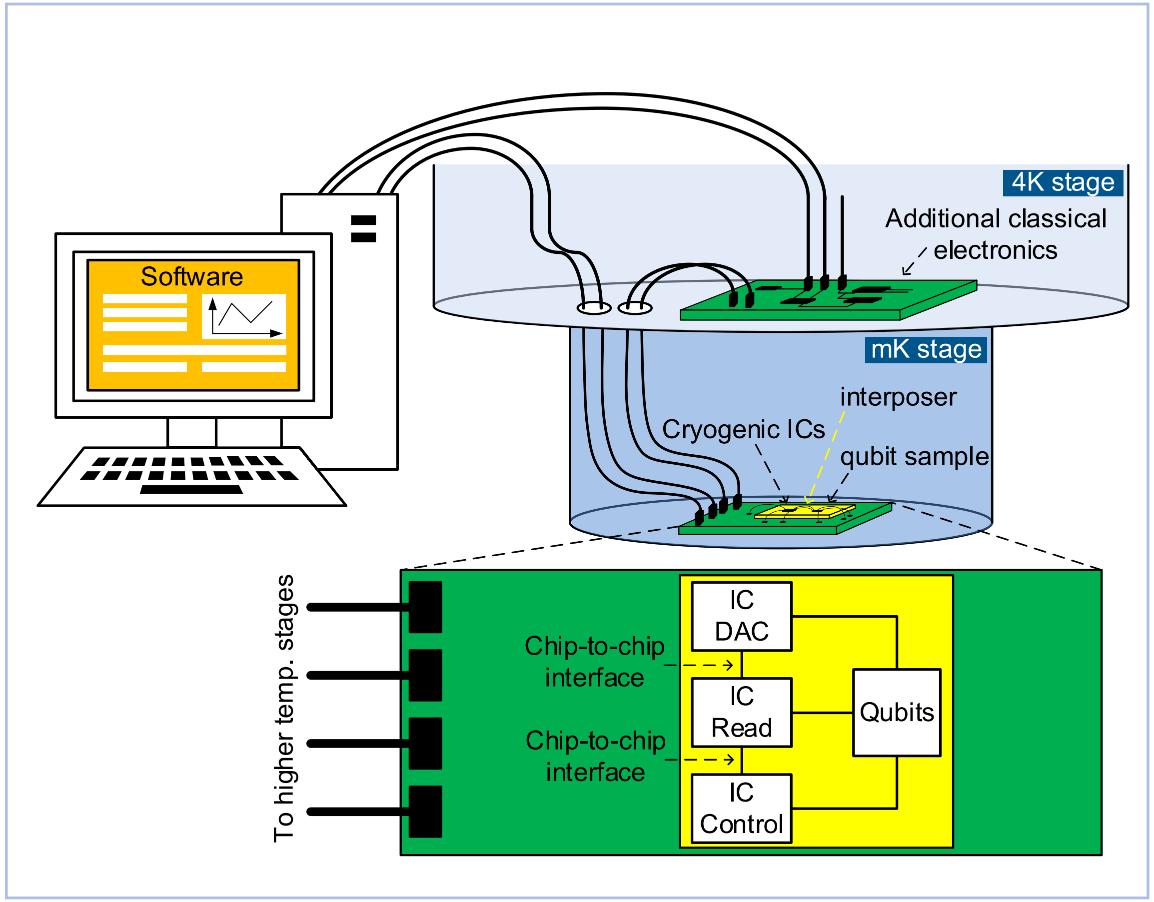
- **Designs in 65nm bulk and 22 nm FD-SOI**
  - Cryogenic measurement results
  - Lessons learned (what to watch out for)
- **Co-integration experiment with qubits at mK**
  - Thermal management
- **Other activities at ICA for QC:**
  - Cryogenic device measurement and modelling
  - Cryogenic photonic link (for superconducting qubits and cryo. electronics)



CRYOGENIC CMOS DESIGN



- Move (parts) of classical control & readout electronics closer to the qubit
- Consequence → operate at cryogenic temperature
- Cryogenic CMOS enables high-integration
  - Comply to ultra strict cooling power budget
- Qubits are evolving quickly → modular IC framework



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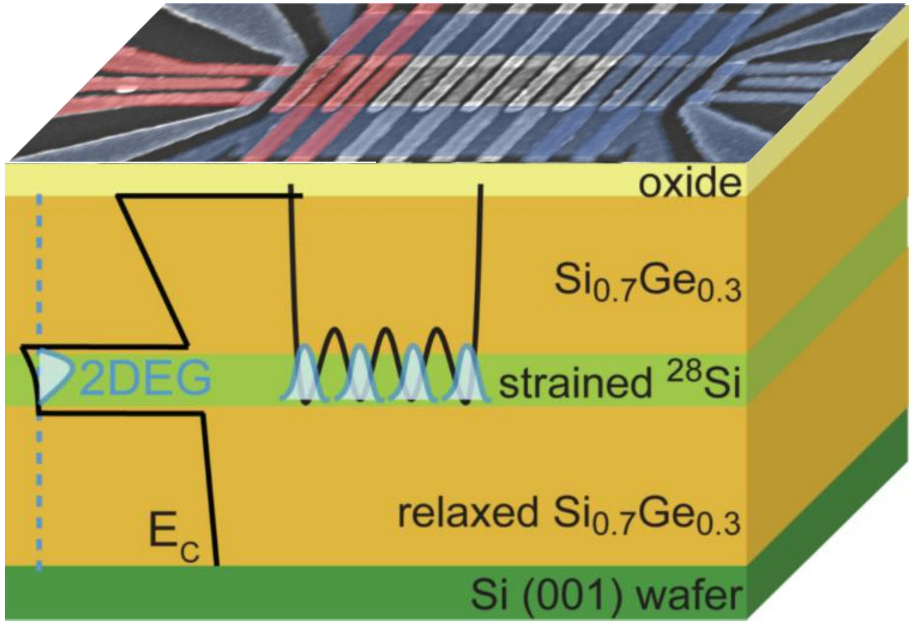
DC BIAS

Specification

Specification for DC Bias via DAC

- Several uncorrelated bias voltage per qubit to form potential wells
- Voltage range up to approx. 1.7V
- A step size in the hundreds of μV

Si/SiGe Architecture[3]



[3] I. Seidler, T. Struck, R. Xue et al., "Conveyor-mode single-electron shuttling in Si/SiGe for a scalable quantum computing architecture," npj Quantum Inf 8, 100, 2022.

DC BIAS

QUOCCA

Digital[4]:

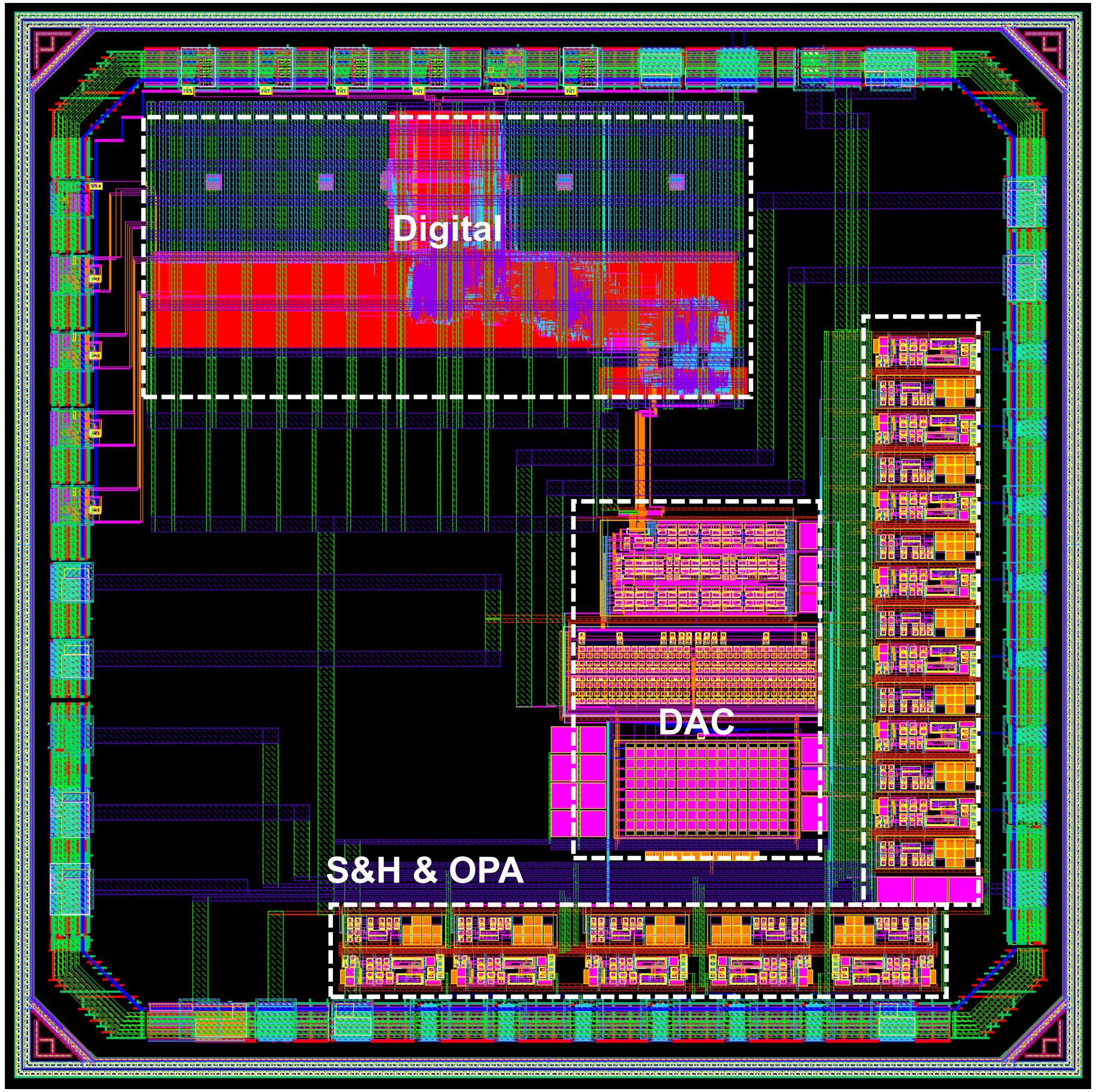
- JTAG Interface
- RISC-V Processor
- DAC FSM

Bias DAC:

- Charge-redistribution topology
  - Negligible static power

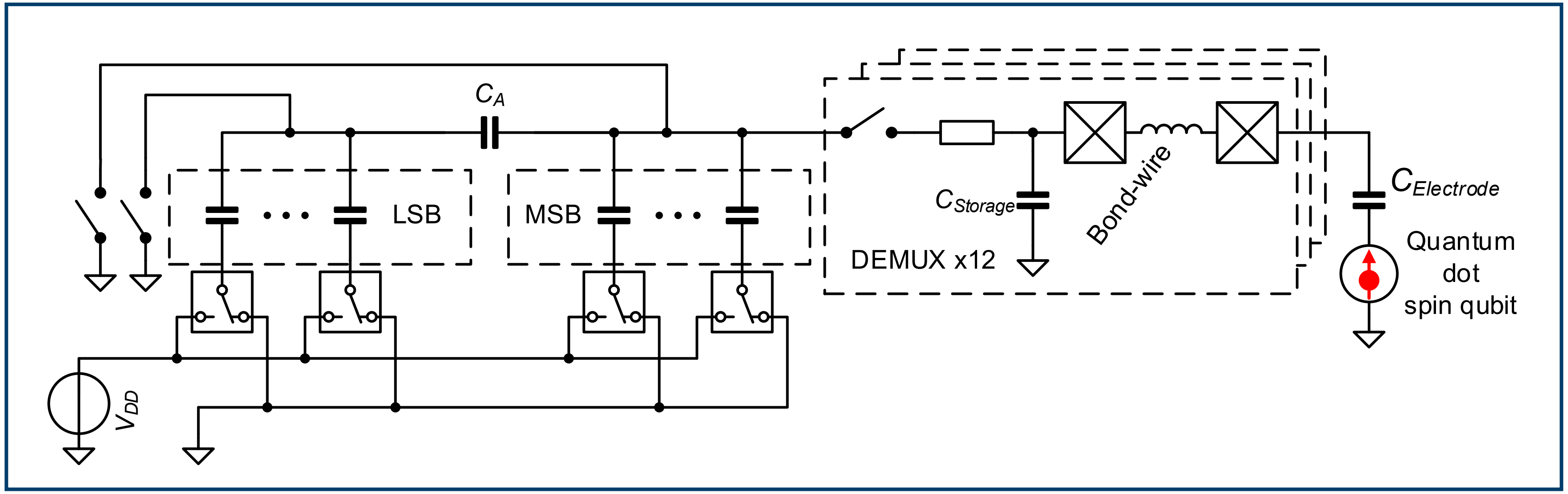
Sample & Hold Output Channel:

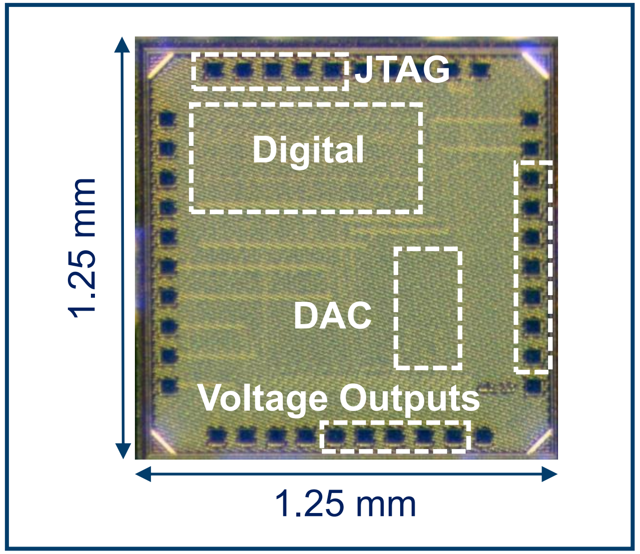
- Individual refreshable
- Testing amplifier



DC BIAS

CMOS Bias DAC



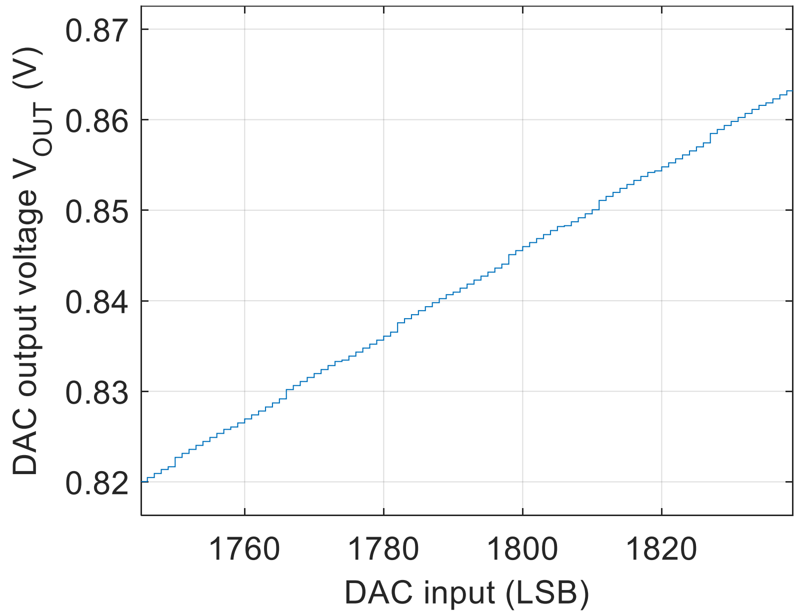


Characteristics	Specification
Output Channels	12
Voltage Range	0V to 1.8V
Resolution	12 Bit
Step Size	~ 439 µV

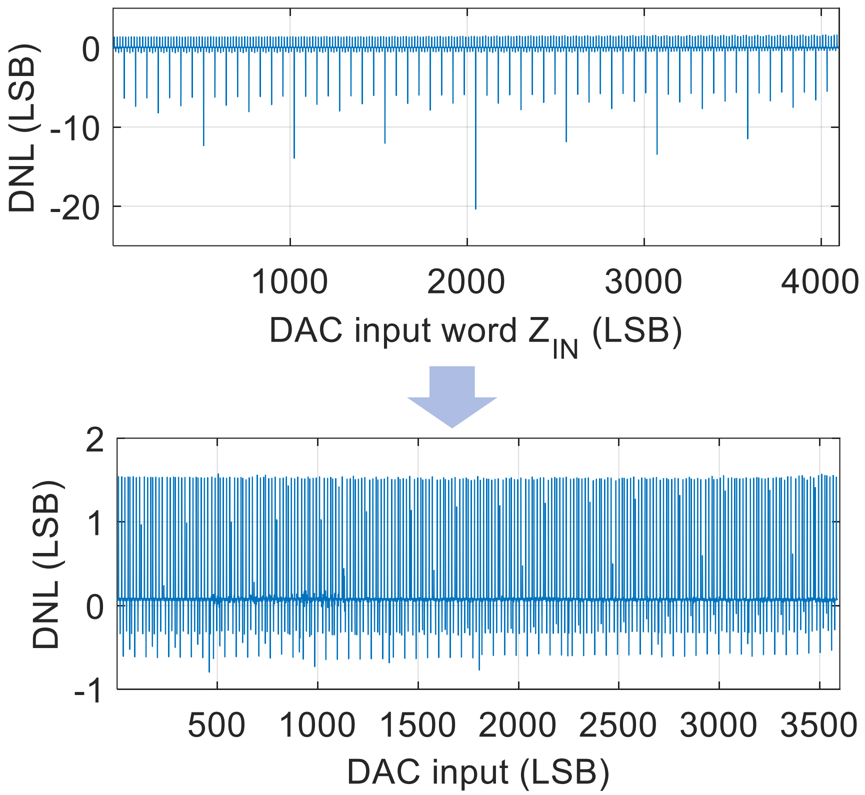
- No output buffer needed due to low leakage
  - Reduce power and noise
- Defined control of the DAC refresh
  - Internal or external trigger signal

DC BIAS

DAC Output



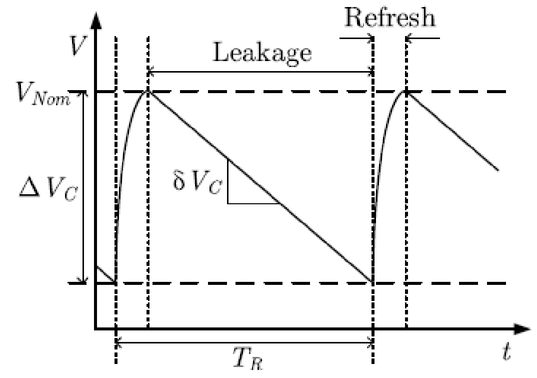
506 skipped input words → 11.81 Bit



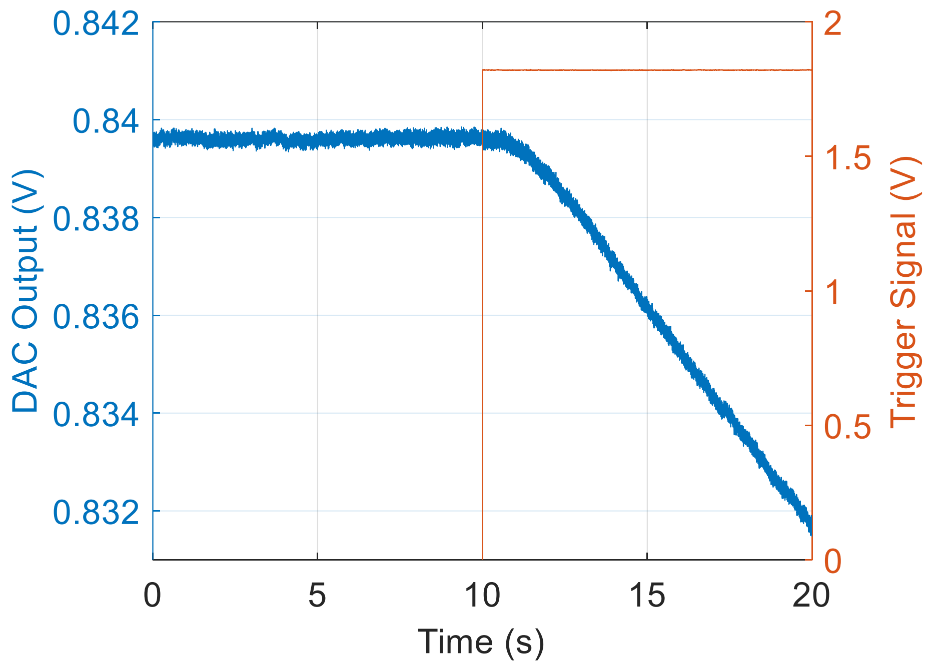
MEASUREMENTS

Defined hold trigger for qubit operation between refresh

- Defined hold trigger for qubit operation between refresh
- Periodical refresh due to leakage in S&H channels
- Refresh increases noise at qubit gates
- Low temperature makes long hold time possible



[5]



Voltage drift: 746 $^{\mu V}/_{s}$

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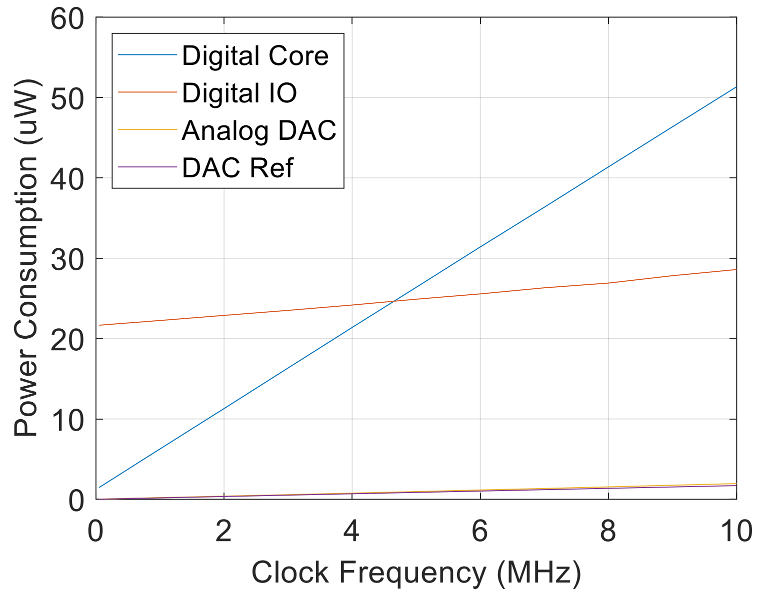
DC BIAS

Power Consumption And Noise

Component	Power Consumption @ 5 MHz Clock
Analog DAC	0.96 μW
Analog DAC reference	0.86 μW
Analog DAC total	1.8 μW (152 nW per channel)
Digital IO	24.9 μW
Digital Core	26.4 μW
Total	53.1 μW



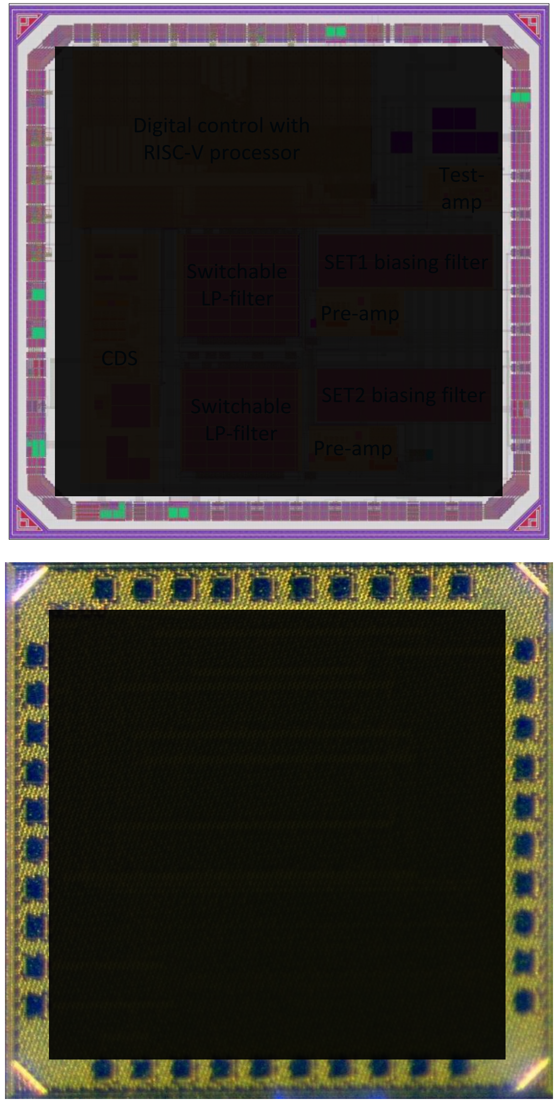
12 Channel running at 24 kHz channel refresh rate at 5 MHz Clock
Integrated noise added by DAC @ 1MHz Clock $\approx 119\ \mu V_{rms}$

POWER DRAW IN PADFRAME

Padframe IP Considerations

- Padframe IP is not made for cryo. temperature
- **Analog pads** are good
  - Typically less leakage in ESD structures

- **Digital pads**:
  - Functionality (mostly fine)
    - even with complex internal circuitry
  - Power (every µW counts at mK)
    - Consider internal power OK generation
    - May generate internal bias voltages (e.g. for IO ↔ core voltage levelshifter)

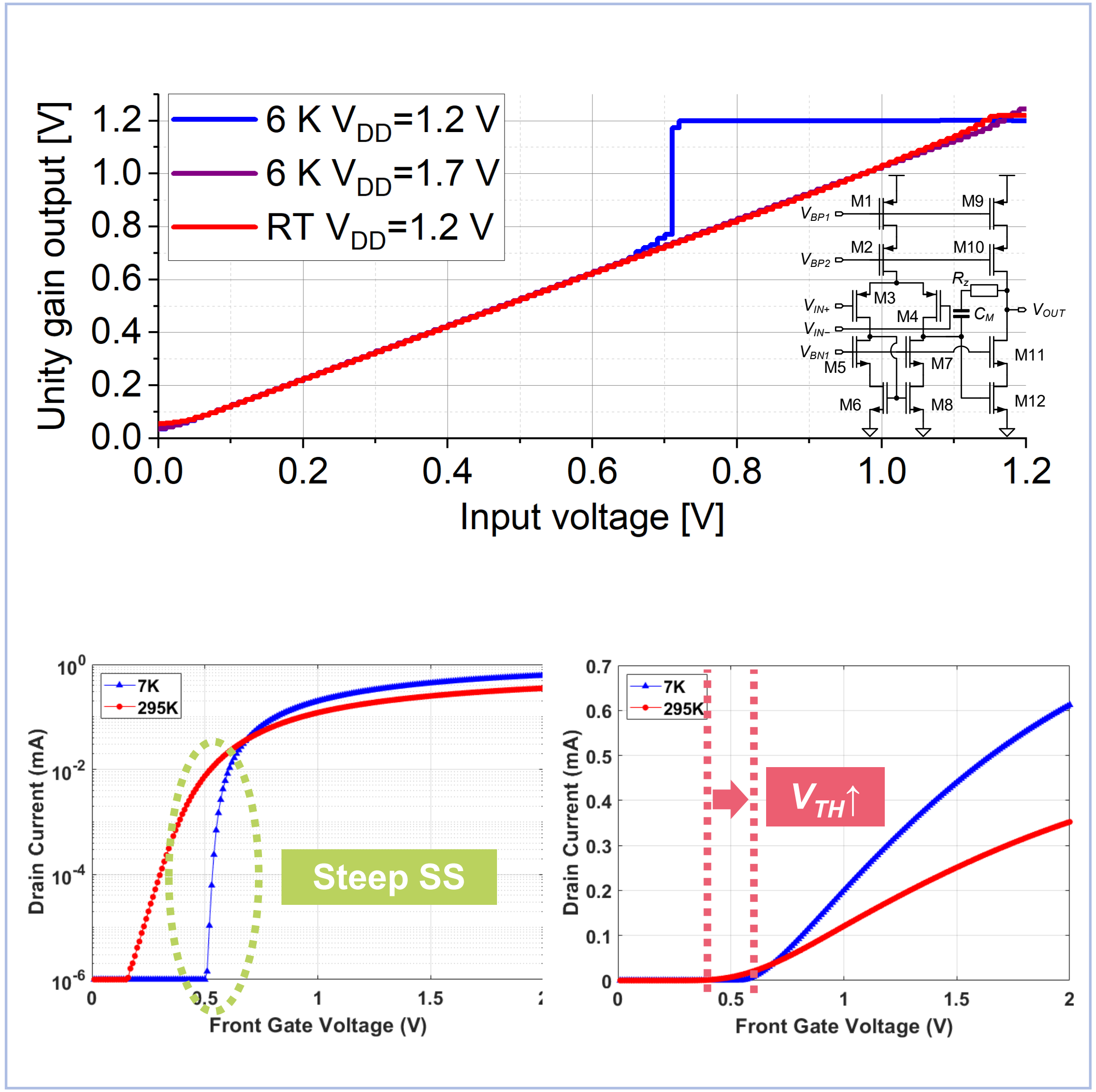


OPAMP

- Clipping of Opamp output at cryo temp.
  - Subthreshold operation problemetic
  - Due to steep SS

- Increase supply for extra headroom
  - Use **low supply circuit topologies**

- **Pay extra attention to stay in strong inversion**
  - Compensate or be aware of V_{TH} shift



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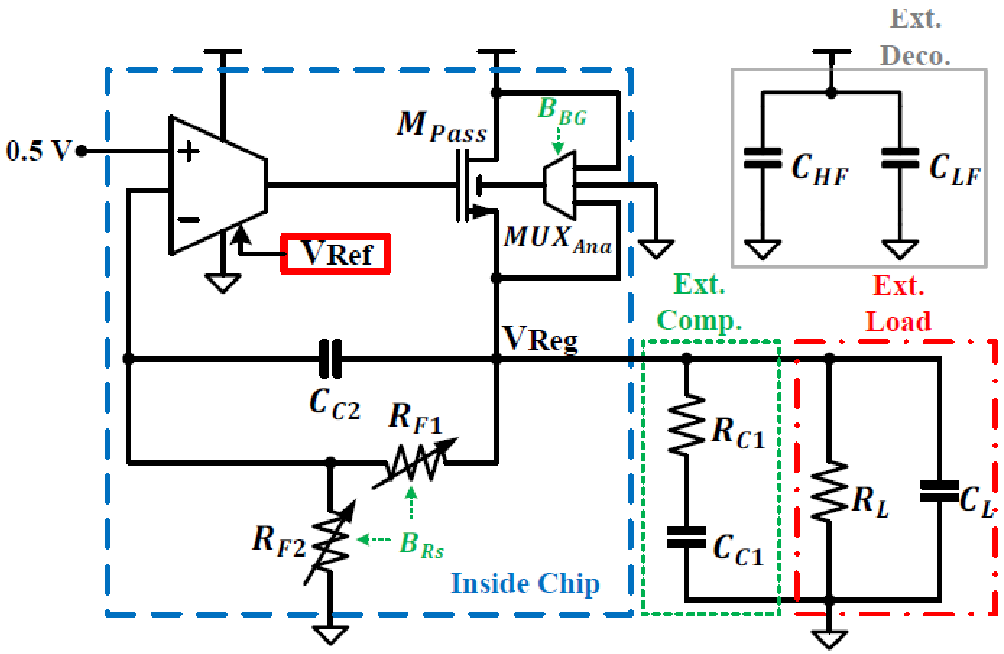
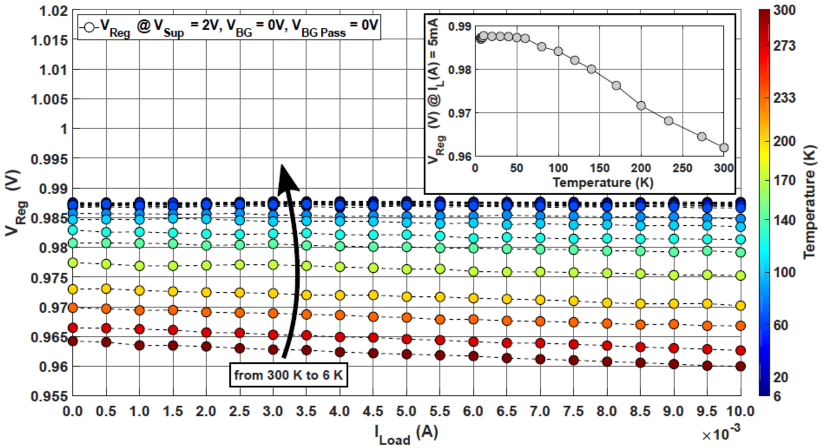
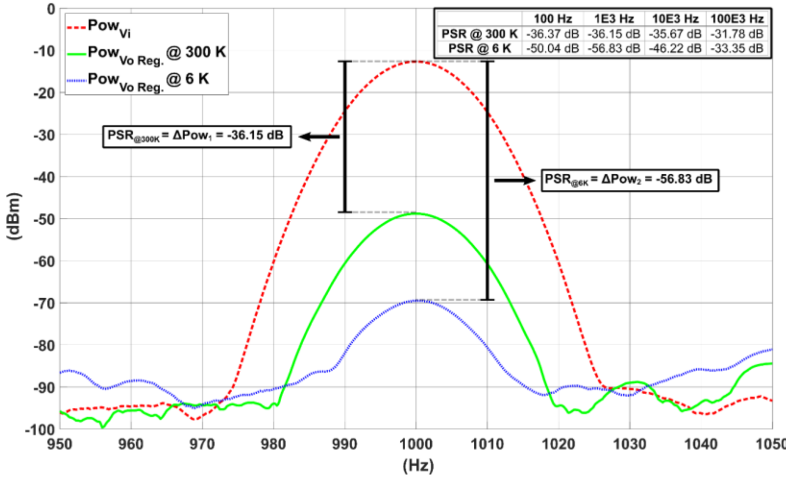
VOLTAGE REFERENCES

Voltage Reference and Regulator Circuit in 22nm FD-SOI





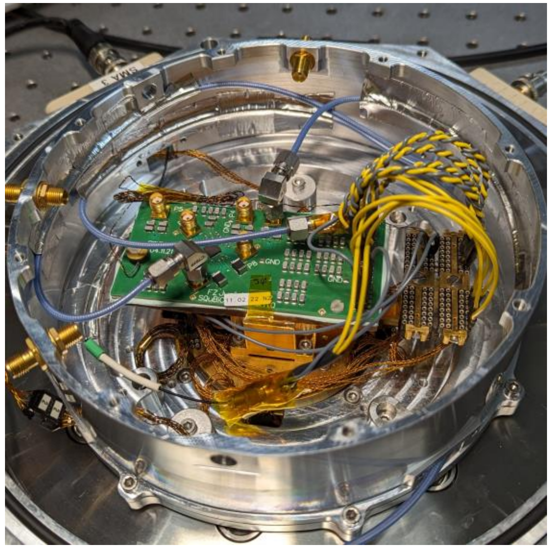


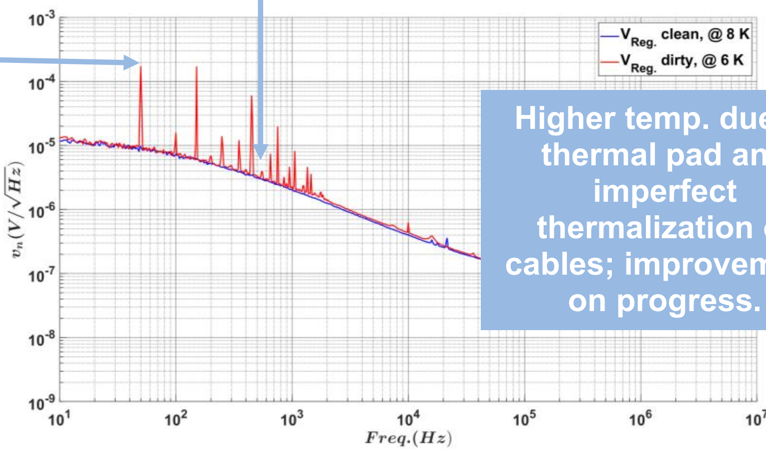
[2] A. R. Cabrera-Galicia, et.al, "Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22nm FDSOI Technology," in IEEE Open Journal of Circuits and Systems, vol. 5, pp. 377-386, 2024, doi: 10.1109/OJCAS.2024.3466395

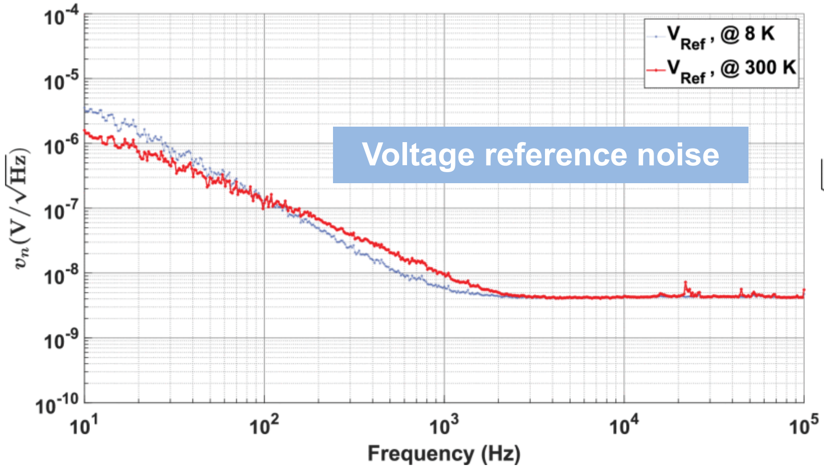
NOISE

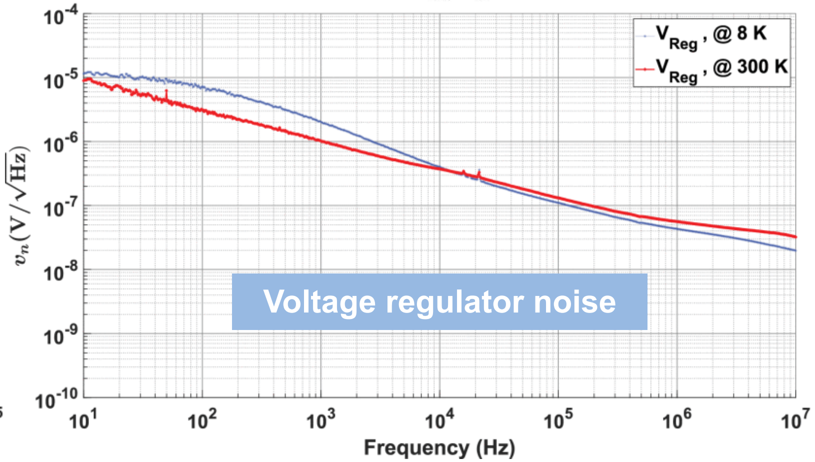
Cryostat and Voltage Reference & Regulator

- Avoid GND loops in the cryostat
  - Counteracting the wish to thermal couple
- Increased 1/f noise; decreased thermal noise







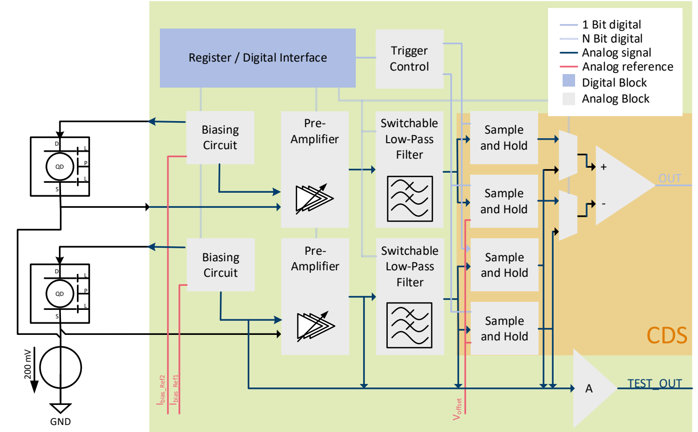


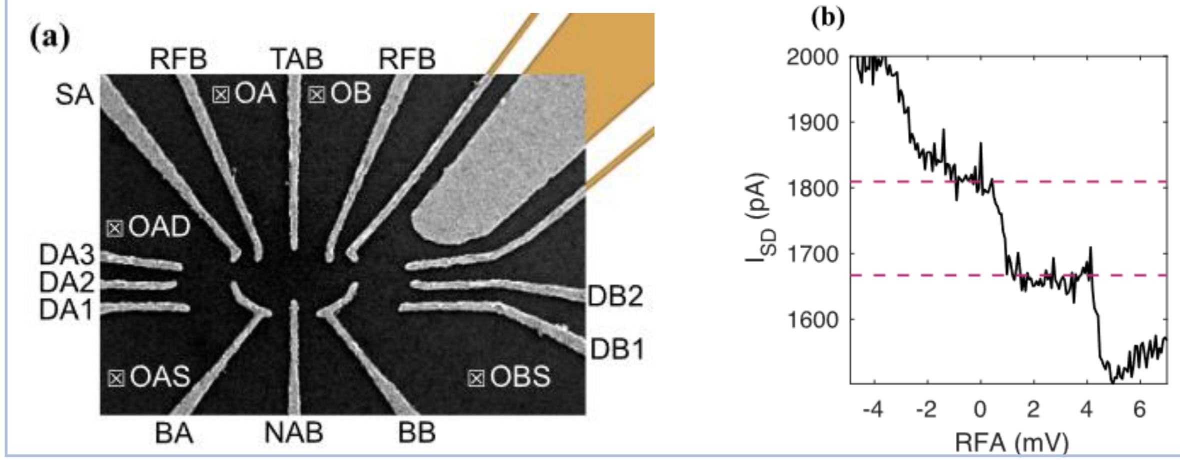
[2] A. R. Cabrera-Galicia, et.al, "Voltage Reference and Voltage Regulator for the Cryogenic Performance Evaluation of the 22nm FDSOI Technology," in IEEE Open Journal of Circuits and Systems, vol. 5, pp. 377-386, 2024, doi: 10.1109/OJCAS.2024.3466395

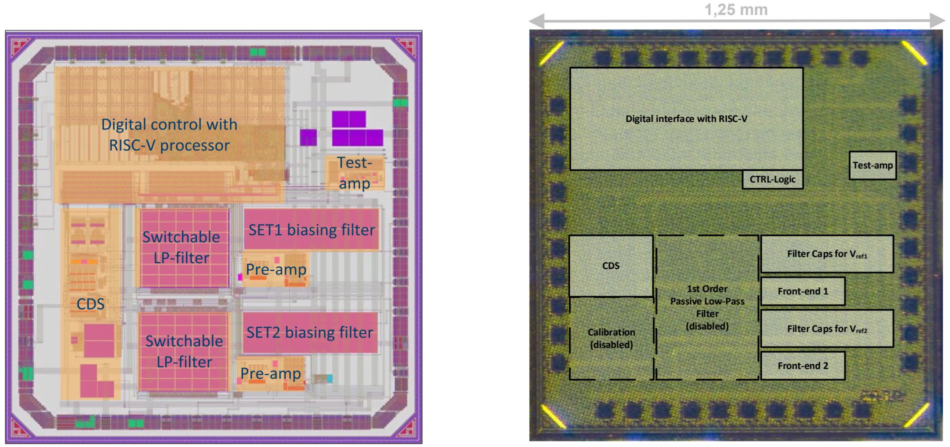
QUBIT READOUT

Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- **Target: Current readout of quantum dots**
- Pauli spin blockade to convert spin to charge
- Single electron transistor (SET) to convert charge to current (signal ca. 250 pA)







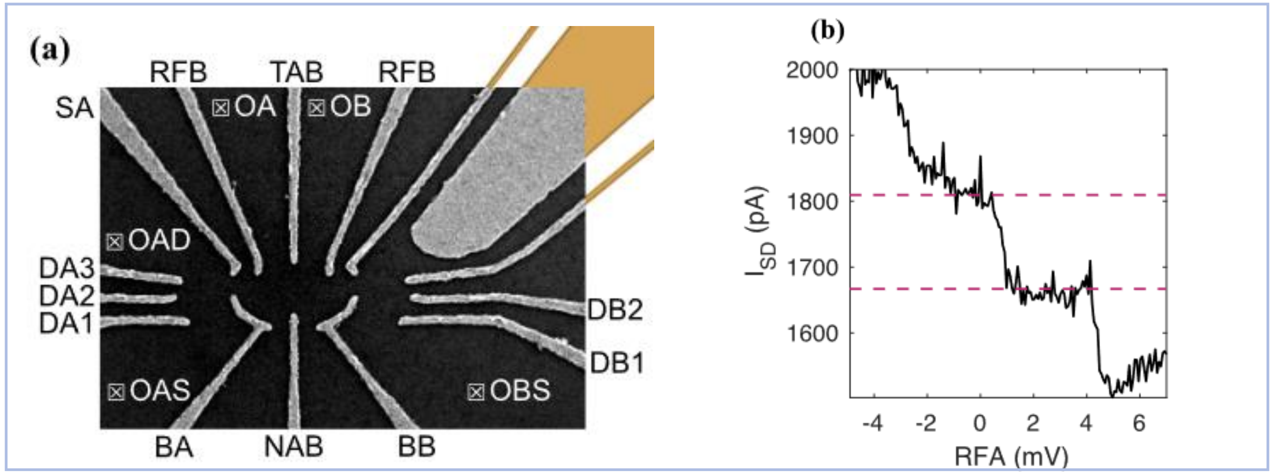
[3] J.Buehler et al., "QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots", Global Physics Summit 2025, MAR-G19/4
[[10] Kammerloher, E. (2022) Improving the output signal of charge readout for quantum computing in electrostatically defined quantum dots with a new sensing dot concept.

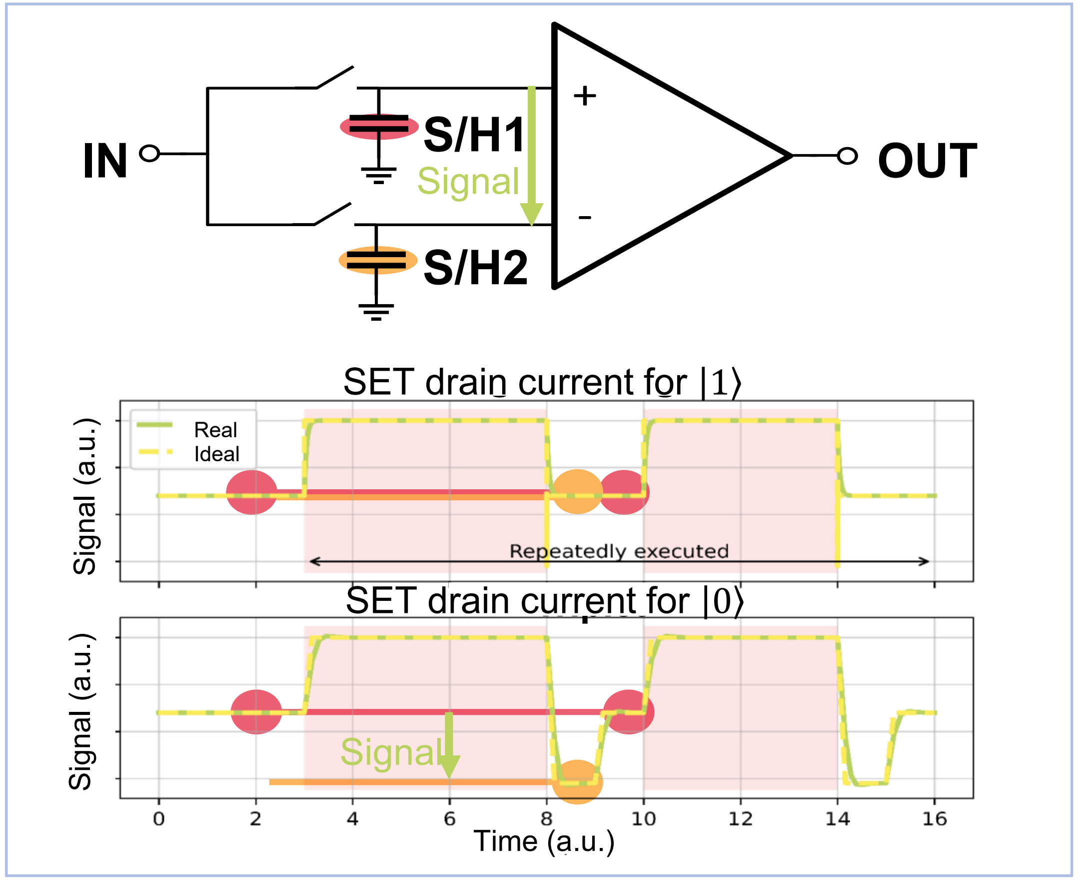
QUBIT READOUT

QUOCCA.SET
SET Readout

Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- **Correlated Double Sampling (CDS)**
  - 1st sample after qubit initialization
  - 2nd sample after qubit operation
  - Cancellation of low frequency noise





[3] J.Buehler et al., "QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots", Global Physics Summit 2025, MAR-G19/4

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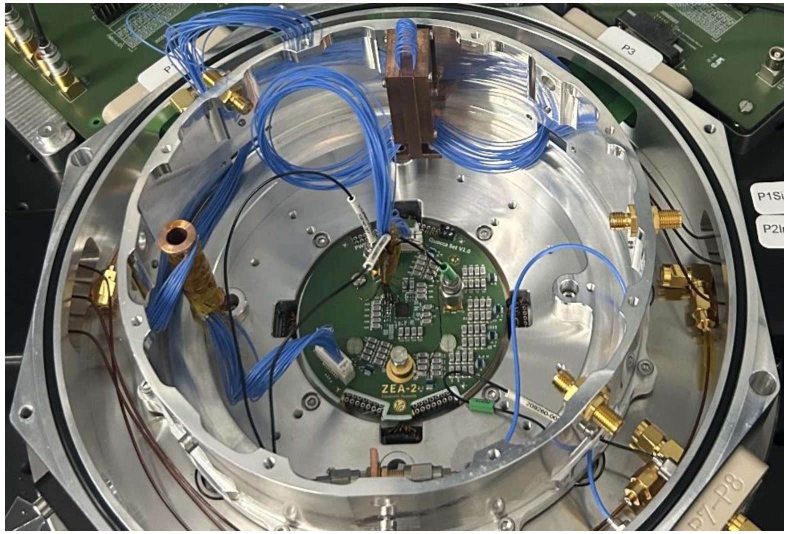
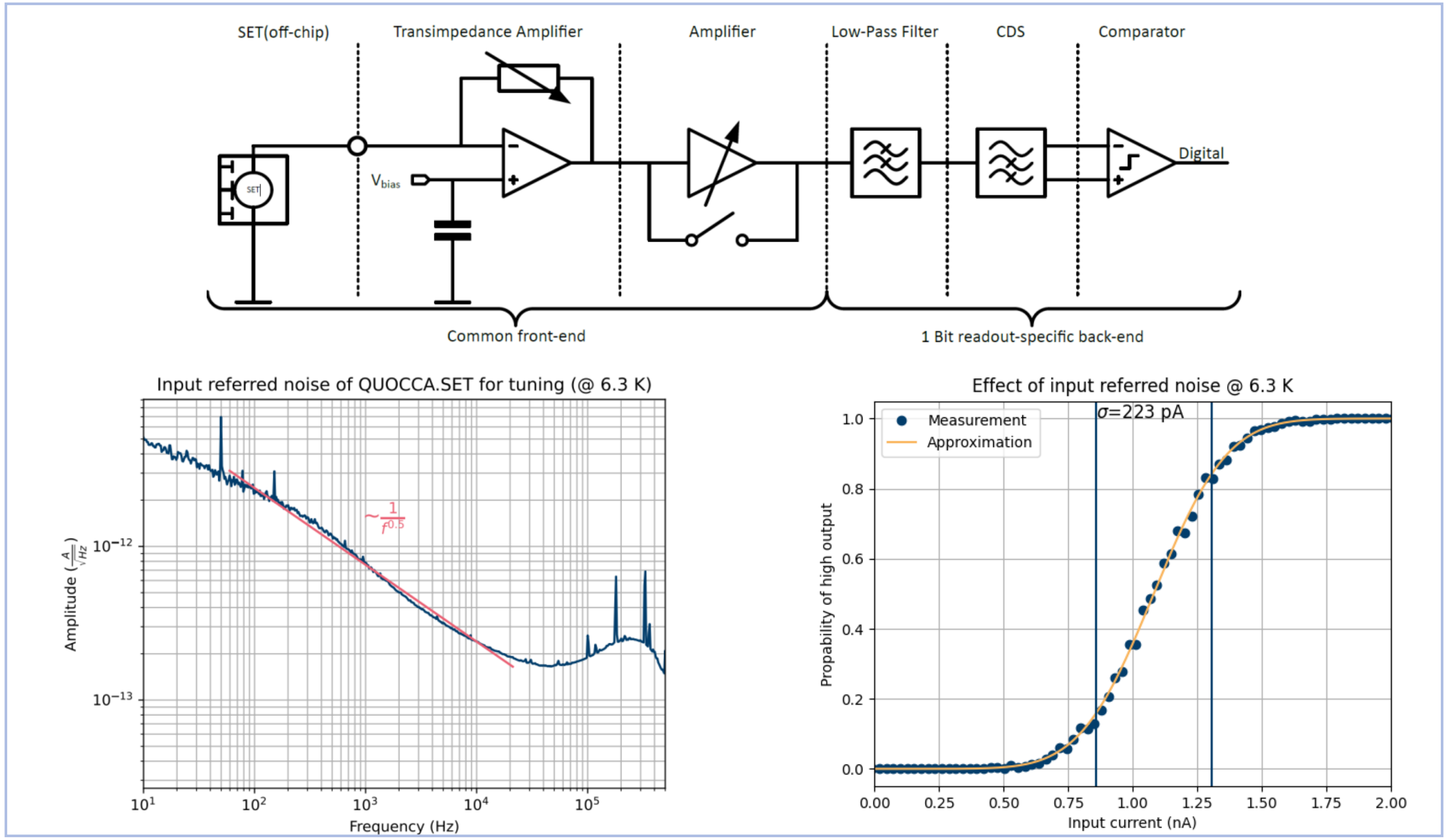
QUBIT READOUT

Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- 223 pA RMS @ 1 µs, max. BW
- 111 pA RMS @ 1 µs, 1 kHz BW
- Digital Power: 41 µW
- Analog Power: 33.6 µW/SET



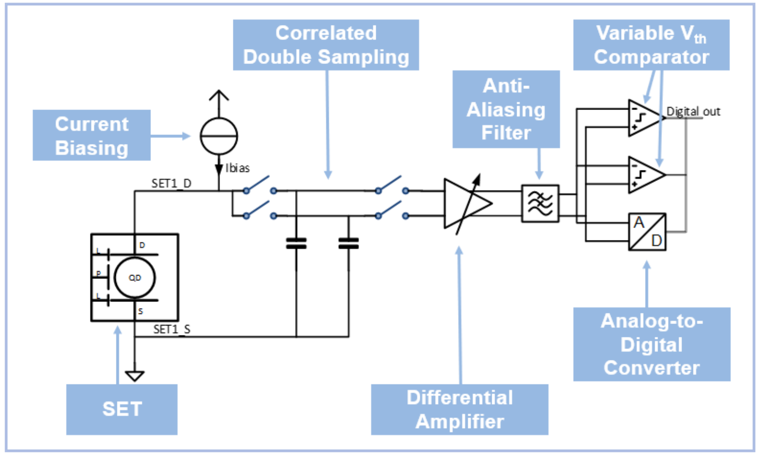


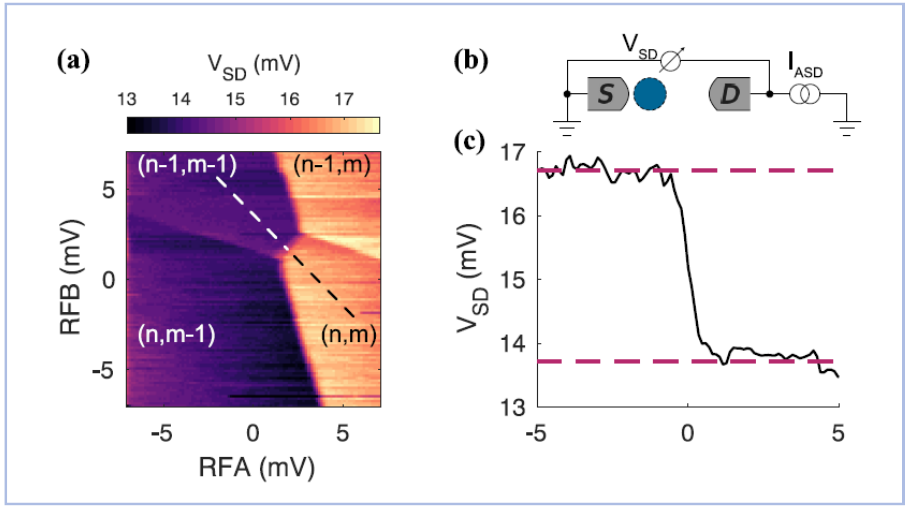
[3] J.Buehler et al., "QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots", Global Physics Summit 2025, MAR-G19/4

QUBIT READOUT

Qubit Readout - QUOCCA.SET: A Scalable Readout IC for Semiconductor Quantum Dots

- **Target: Voltage readout of quantum dots**
- Pauli spin blockade to convert spin to charge
- Single electron transistor to convert charge to voltage
- Signal: ≈ 3 mV [5]



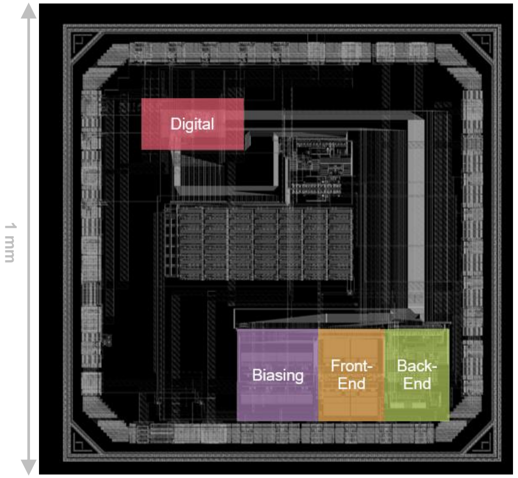


Digital
- Triggerd FSM
- JTAG and UART

Front-End
- S/H with variable Capacitances

Biasing
- Current-mirror bank

Back-End
- Dynamic Comperator
- 7 bit SAR ADC

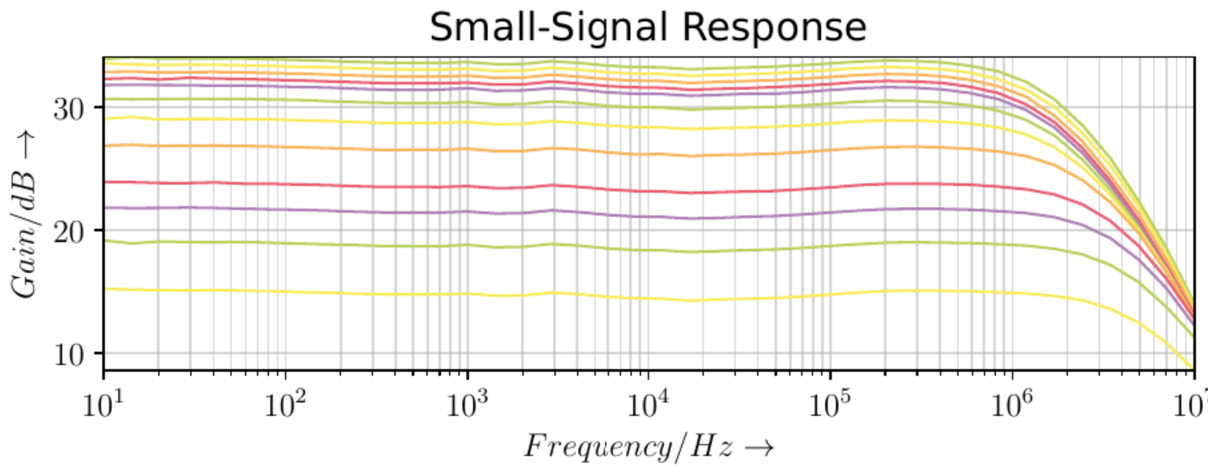


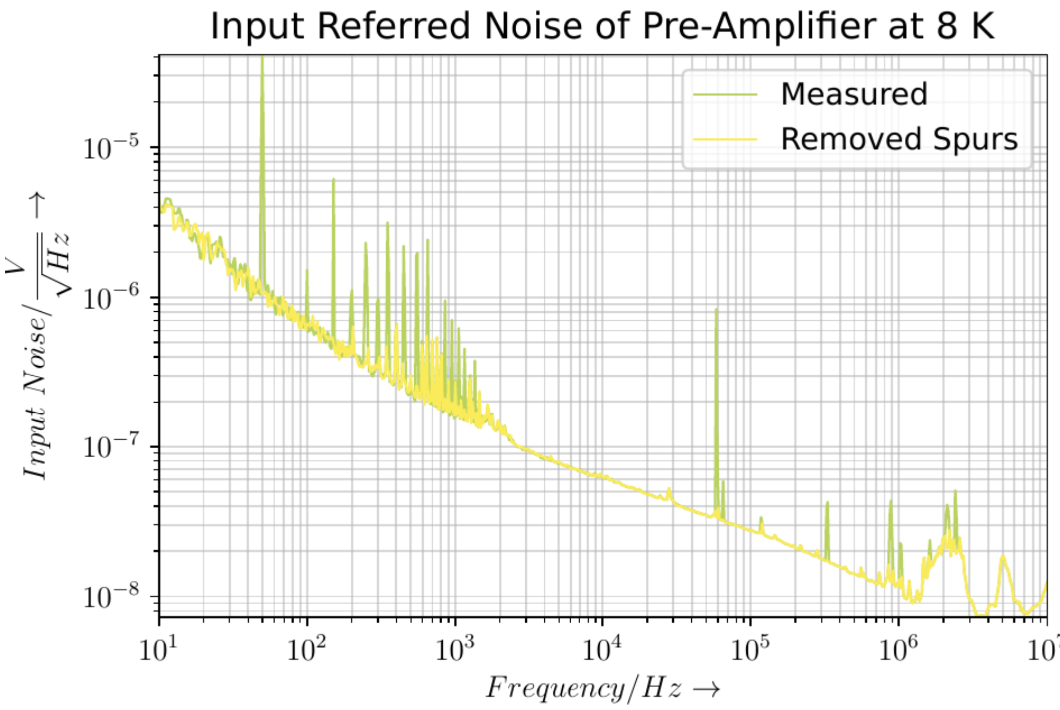
[4] J.Buehler et al., "Scalable integrated readout of semiconductor quantum dots using current biasinG", Global Physics Summit 2026 https://summit.aps.org/smt/2026/events/MAR-Z17/15
10] Kammerloher, E. (2022) Improving the output signal of charge readout for quantum computing in electrostatically defined quantum dots with a new sensing dot concept.

QUBIT READOUT

Amplifier Measurements at 8 K

- Power: ≈ 57 μW
- Gain: ≈ 8 - 45 dB
- Bandwidth: ≈ 1.5 - 5.5 MHz
- Active area: ≈ 1500 μm²





[4] J.Buehler et al., "Scalable integrated readout of semiconductor quantum dots using current biasinG", Global Physics Summit 2026
https://summit.aps.org/smt/2026/events/MAR-Z17/15

QUBIT READOUT

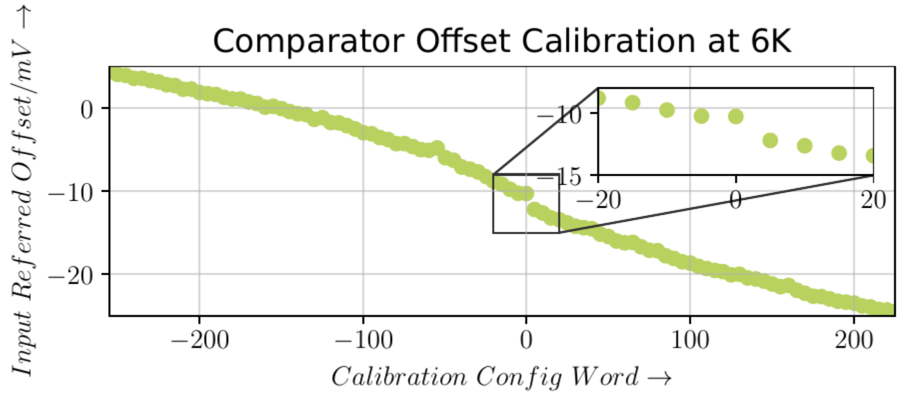
Performance of 1-Bit readout

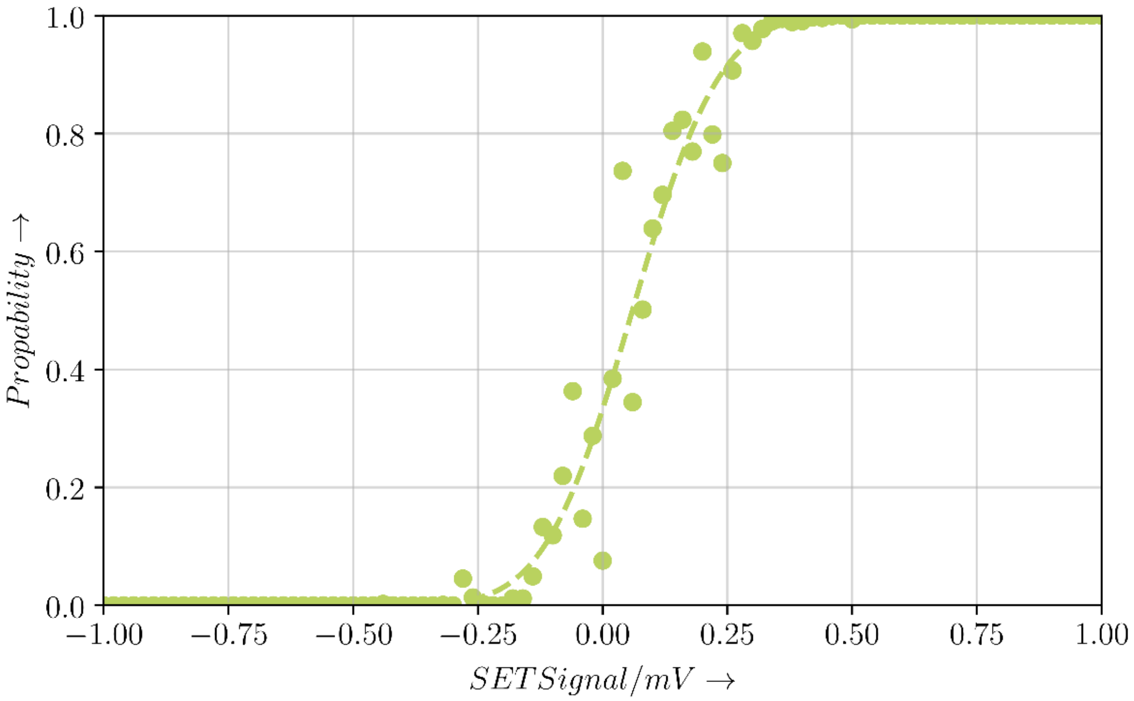
500 ns Sampling Time

- 138 µV RMS @ $C_{sample} \approx$ 20 pF
- 318 µV RMS @ $C_{sample} \approx$ 0,2 pF

Power:

- Digital Power: 8.5 µW
- Analog Power: 115 µW



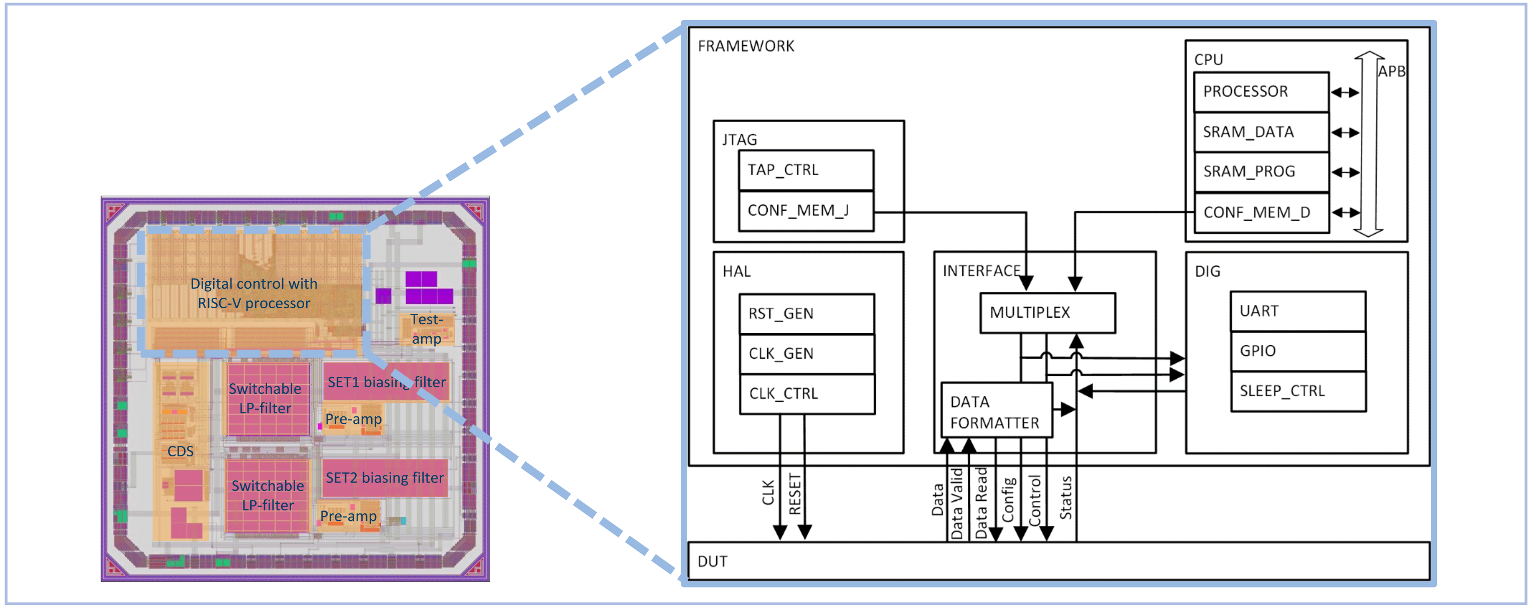


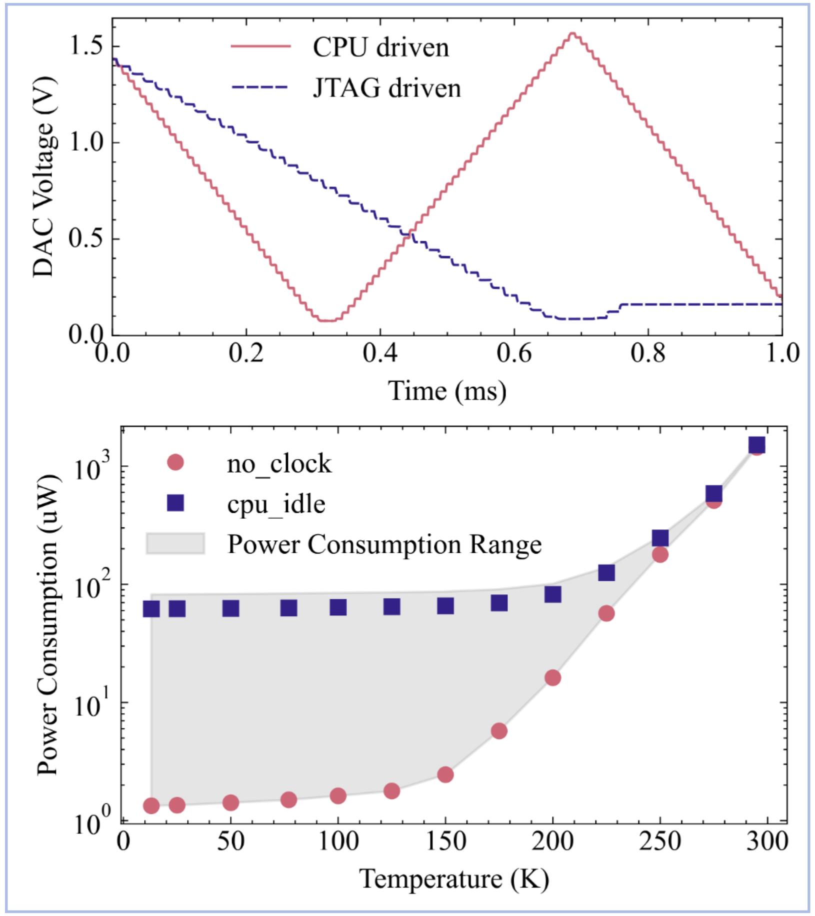
43] J.Buehler et al., "Scalable integrated readout of semiconductor quantum dots using current biasinG", Global Physics Summit 2026
https://summit.aps.org/smt/2026/events/MAR-Z17/15

INTEGRATED RISC-V

Rapid Prototyping Platform for Integrated Circuits for Quantum Computing

- RISC-V with SRAM and APB
- Enables flexibility in control (algorithms)
- Leakage negligible at cryo





[5] J. Mair et al., "Rapid Prototyping Platform for Integrated Circuits for Quantum Computing," 2024 20th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Volos, Greece, 2024, pp. 1-4, doi: 10.1109/SMACD61181.2024.10745395.

DIGITAL INTERFACE

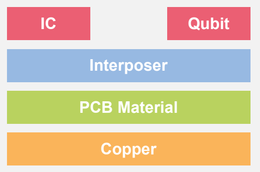
Comparison of Industry Standard Protocols

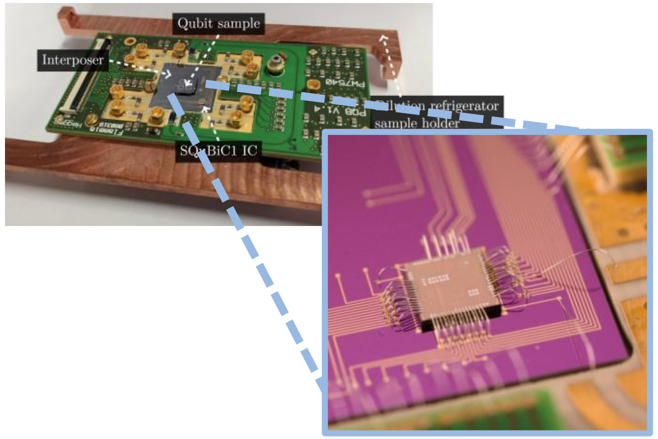
Protocol	Pro ☺	Cons ☹
UART	2-wire interface (RX TX) No pull-up/down	Requires sync.
I²C	2-wire interface (SDA SCL)	Pull-ups
SPI	No pull-up/down	3[4]-wire interface (SCLK MOSI MISO [CE])
JTAG	No pull-up/down	4-wire interface (TCK TMS TDI TDO) Complex state-machine
cJTAG	2-wire interface (TCKC TMSC)	Complex state-machine Less established Optional Pull-ups/downs

- Write & read IC config regs
- Configuration of IC blocks

CRYOGENIC CO-INTEGRATION

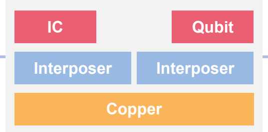
Multiple Approaches



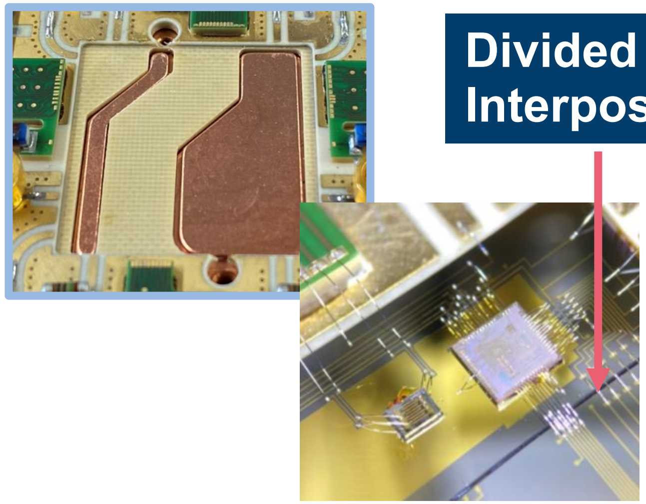


IC and Qubit:
Same Interposer

Electron Temperature Qubit: ca. 2-3K

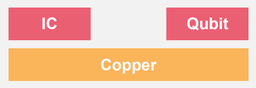


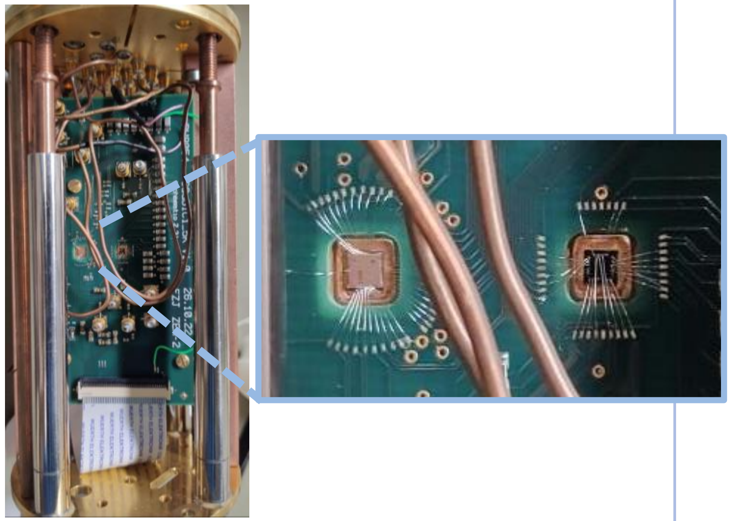
Divided Interposer



IC and Qubit:
Two Interposer

Electron Temperature Qubit: ca. 0.5-1K





IC and Qubit:
Direct Copper

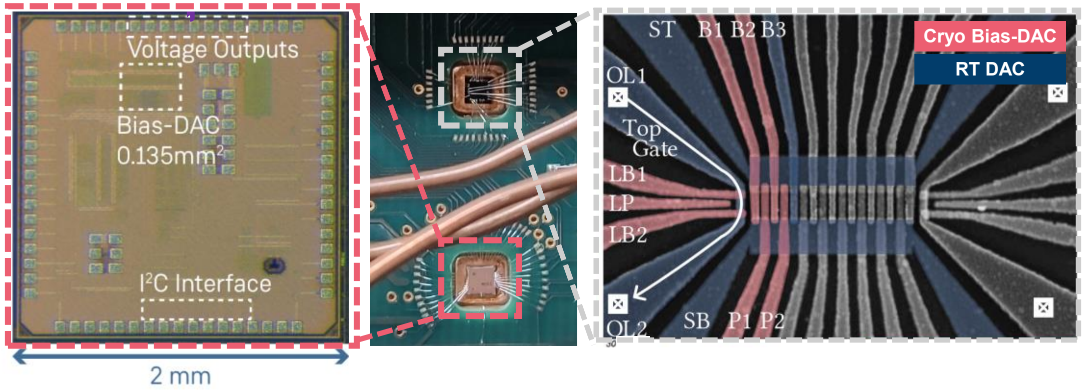
Electron Temperature Qubit: < 0.4K

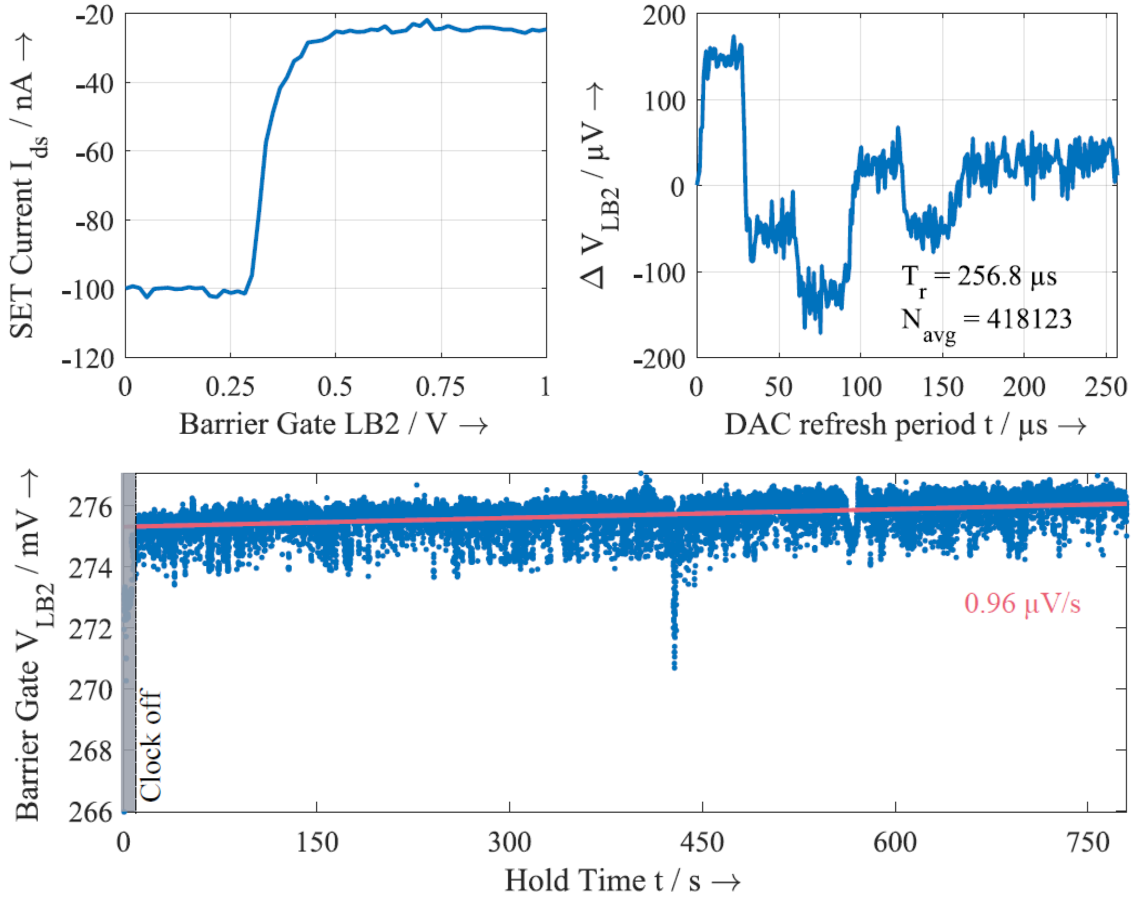
[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

CRYOGENIC CO-INTEGRATION

Ultra-low Leakage Currents

- Bias DAC cycling through 7 metal electrodes
  - SET used as measurement amplifier
  - Visible cross-talk depending on location
- Leakage rates on metal electrodes meas.
  - 2 pF on-chip cap.; ca. 300 fF off-chip cap.
  - Ultra-low voltage drift of <1 µV/s



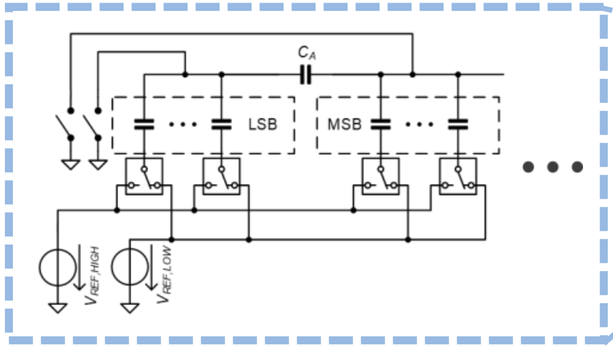


[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

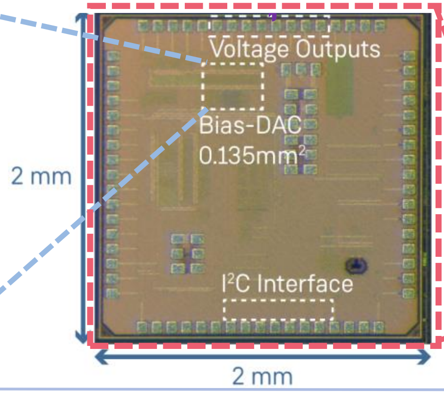
CRYOGENIC CO-INTEGRATION

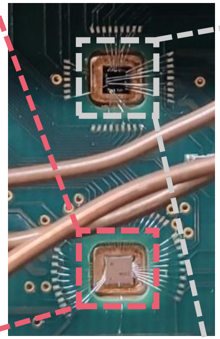
Qubit DC Biasing

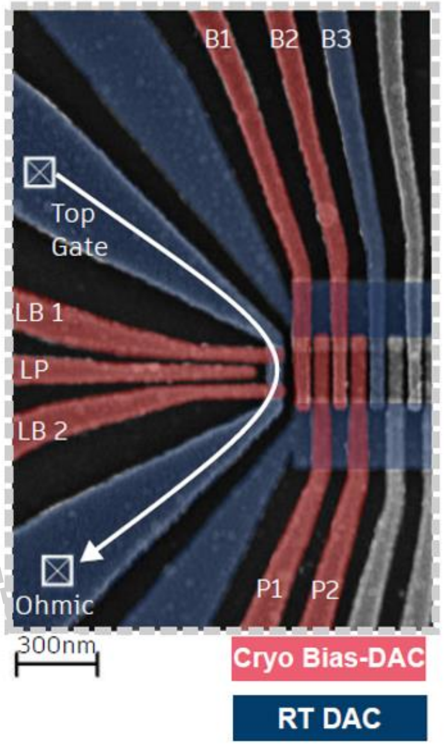

CO-INTEGRATION BIAS DAC WITH Si / SiGe QUBIT



[5]

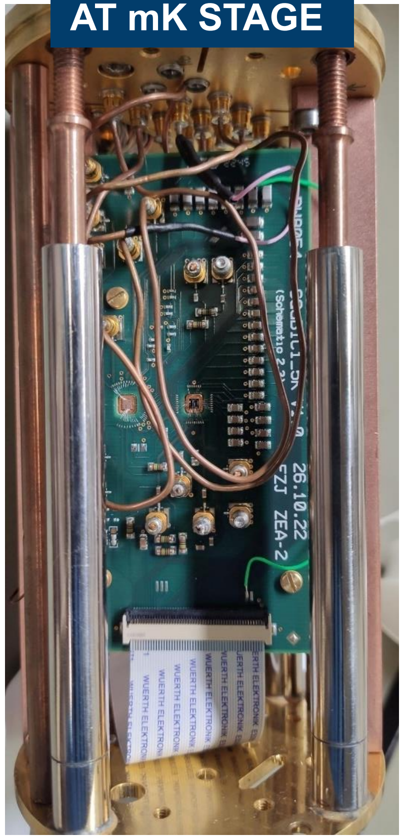




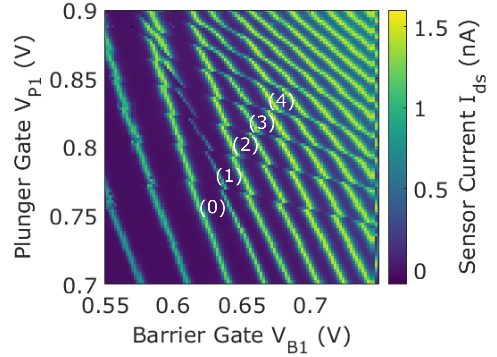


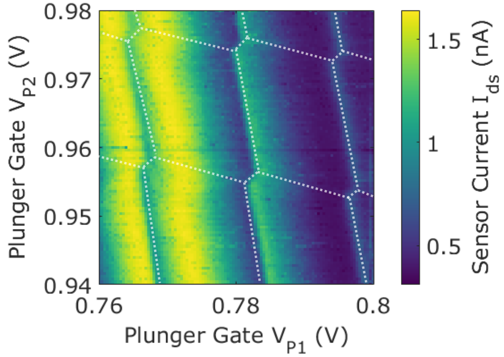
[6]

CRYO SETUP AT mK STAGE



CHARGE SENSING OF SINGLE AND DOUBLE QUANTUM DOT





[7] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," IEEE Solid-State Circuits Letters, 2020
[6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023

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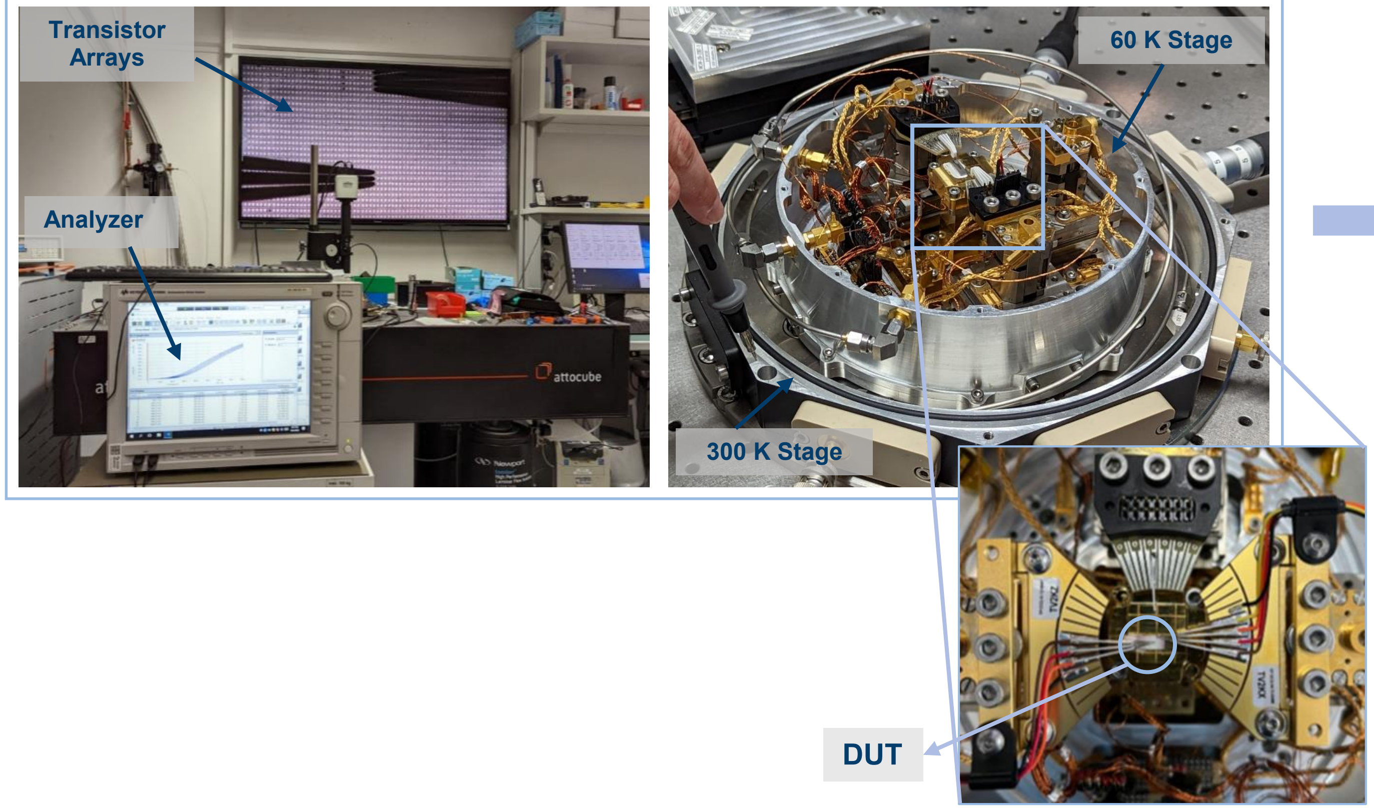
CRYOGENIC MEASUREMENTS

Inputs for a Cryo-PDK for 22 nm CMOS

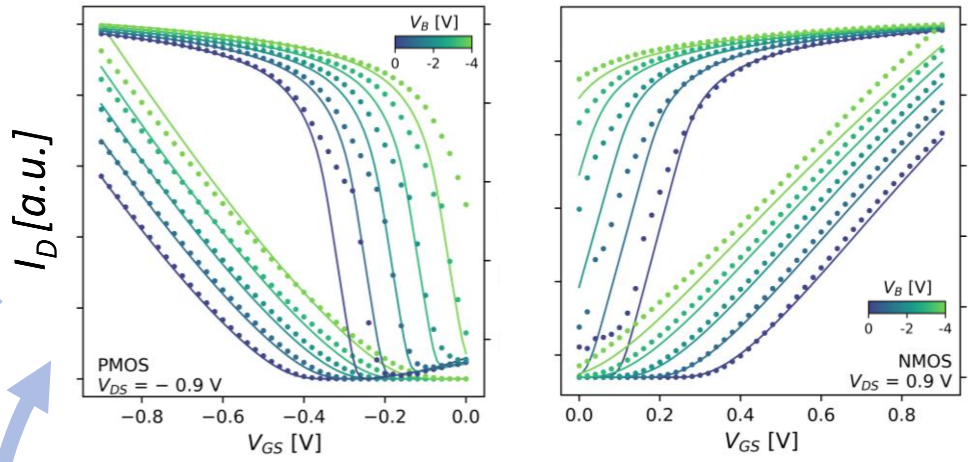
SPONSORED BY THE Federal Ministry of Education and Research

QSOLID

Setup @ ICA | FZJ: T_{min} ~ 7 K



Short-Channel I-V-Curves [8]



Input Data for BSIM-IMG Based Modeling

AdMOS

done by AdMOS GmbH

Cryogenic Model Library

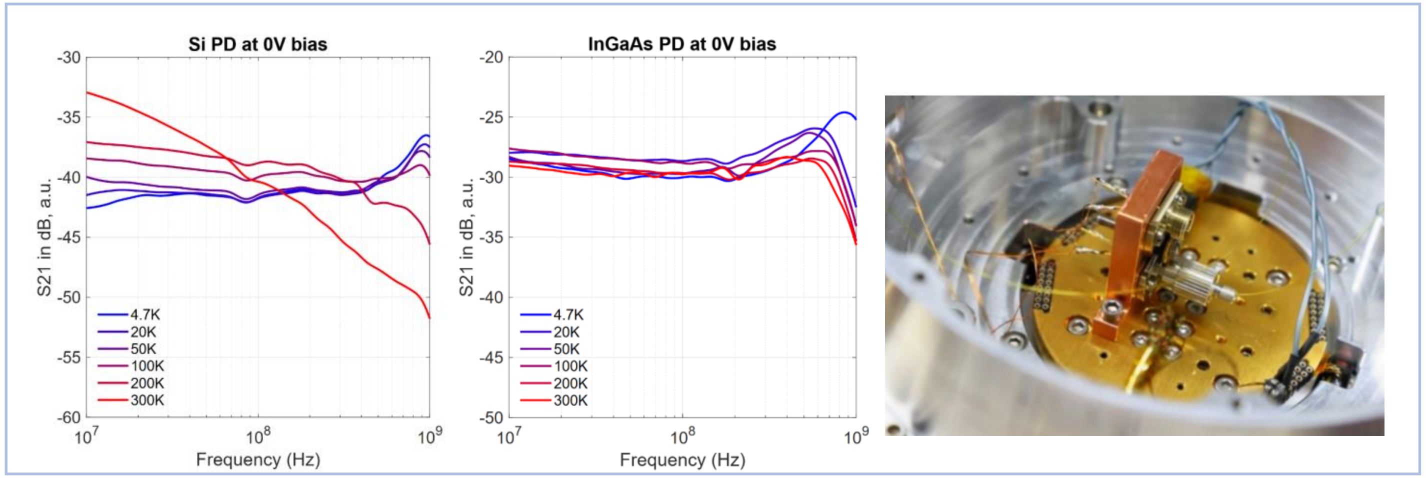
[8] Chava, Phanish, et al. "Evaluation of cryogenic models for FDSOI CMOS transistors." 16th IEEE Workshop on Low Temperature electronics. No. FZJ-2024-05369. Zentralinstitut für Elektronik, 2024.

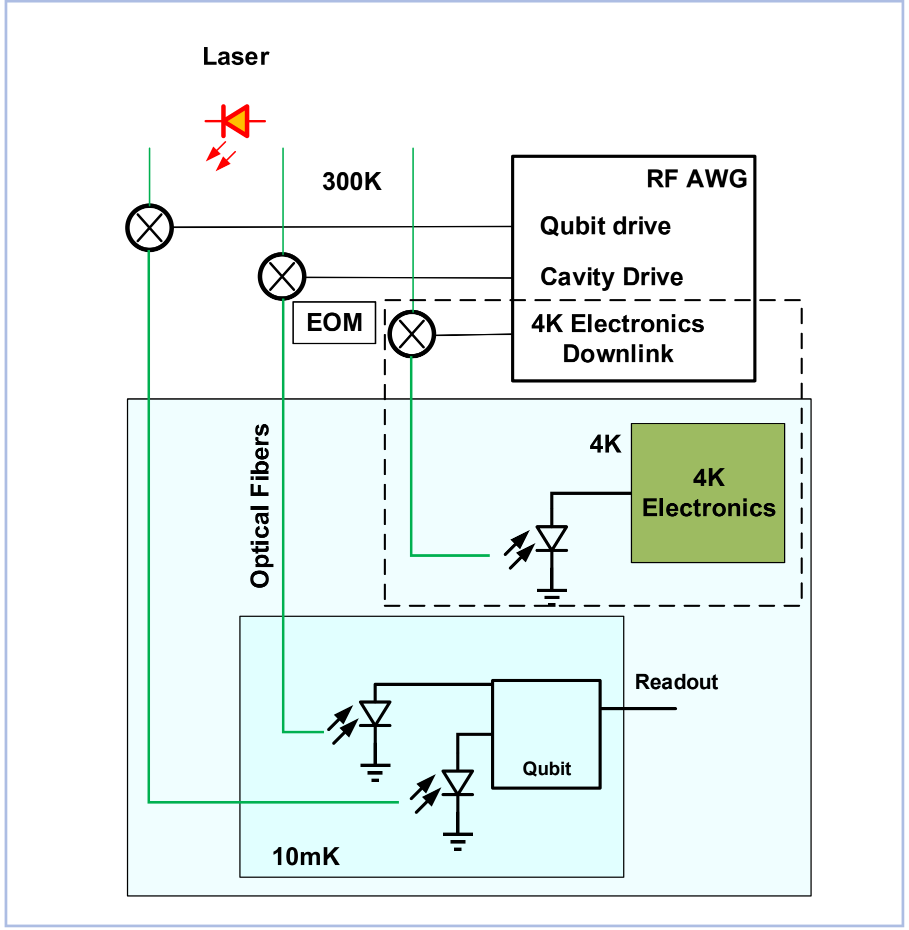
The QSolid project acknowledges the support of the Federal Ministry of Education and Research (BMBF) within the framework programme "Quantum technologies – from basic research to market" (Grant No. 13N16149).

QSOLID – PHOTONIC LINK

Optical Data and Power Link to Cryo

- Passive optical photodiode link as alternative approach
  - Significantly improved bandwidth & dark currents at cryo
  - Purely passive operation, no bias needed
  - Power and data communication envisioned
- Measurement with SC Qubit in Munich ongoing





[9] S.Mutum, et. Al, "A Photonic Link at 4.7K with >1 GHz bandwidth towards an Optical Quantum Computing Interface", IEEE MTT-S International Microwave Symposium (IMS) 15-20 June 2025, Moscone Center, San Francisco, CA

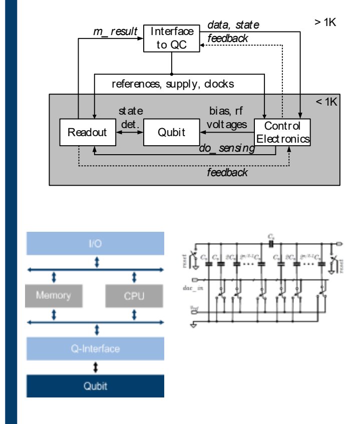
The QSolid project acknowledges the support of the Federal Ministry of Education and Research (BMBF) within the framework programme "Quantum technologies – from basic research to market" (Grant No. 13N16149).

SUMMARY

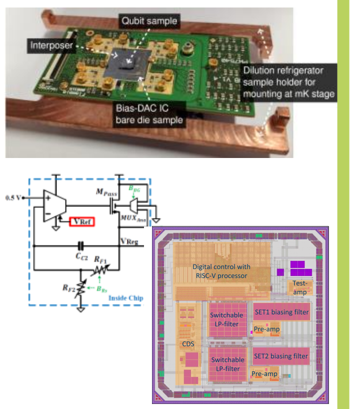
- Cryo-CMOS readout shown with current and voltage biasing.
- DC qubit biasing demonstrated in 22 nm and 65 nm, at cryo and with qubits

Cryogenic Pitfalls:

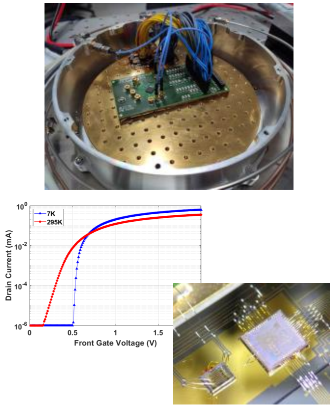
- Hidden IP power
- Cryo model shifts
- Ground loops in the cryostat
- Steep subthreshold slope
- Thermal anchoring



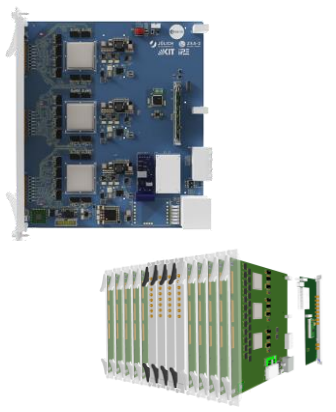
System Modeling



Cryogenic IC Design



Cryo Measurement



System Engineering

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- [6] L. Schreckenberg et al., "SiGe Qubit Biasing with a Cryogenic CMOS DAC at mK Temperature," ESSCIRC 2023
- [7] P. Vliex et al., "Bias Voltage DAC Operating at Cryogenic Temperatures for Solid-State Qubit Applications," IEEE Solid-State Circuits Letters, 2020
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- [9] S.Mutum, et. Al, "A Photonic Link at 4.7K with >1 GHz bandwidth towards an Optical Quantum Computing Interface", IEEE MTT-S International Microwave Symposium (IMS) 15-20 June 2025, Moscone Center, San Francisco, CA
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New Spin-Off: icecirc

IceCirc is a spin-off of the Institute for Integrated Computing Architectures at Research Center Jülich which:

- Has 10 years of experience in cryogenic IC design
- Employs state of the art semiconductor technology
- Has demonstrated integration of cryogenic electronics with qubits
- Provides electronic design service for cryogenic integrated electronics

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