CRYOGENIC MODELING AND PROCESS DESIGN KIT FOR A CMOS 28-NM BULK TECHNOLOGY

LUCA CASTELLANI – FEE 2026 PARIS

UNIVERSITÀ DI TORINO

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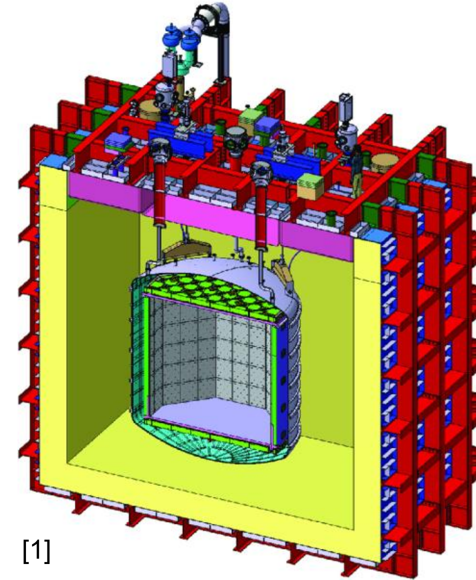
Integrated Computing Architectures

REASON FOR CRYOGENIC PDK DEVELOPMENT

Thesis Goal

- Cryogenic ICs → cryogenic particle detectors readout and quantum computing control
- Dark matter/neutrino detectors → scalability
  quantum processors → interconnect
- Si Foundries → **PDK** (Process Design Kits) for a CMOS tech node. Valid only down to -40° C
- Cryogenic Designs → custom models

Goal :
establish a cryo characterization and extraction methodology for a 28nm bulk CMOS technology → partial cryo-PDK



[1]

Darkside20k liquid Ar cryo-TPC in construction @LNGS, Italy

Example of fixed cryo-T dilution cryostat for quantum computing prototypes

[1] DarkSide-20k sensitivity to light dark matter particles, Acerbi et al. 2024

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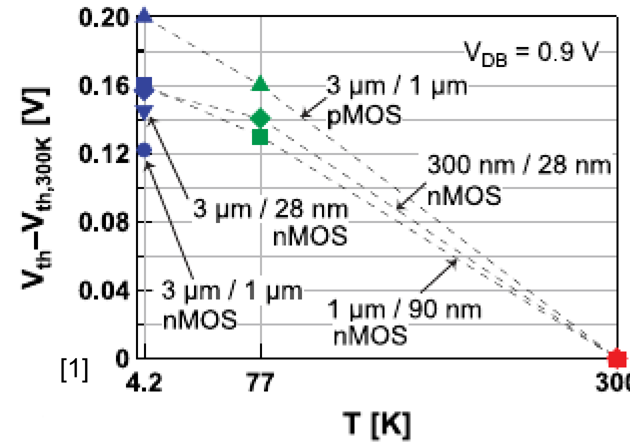
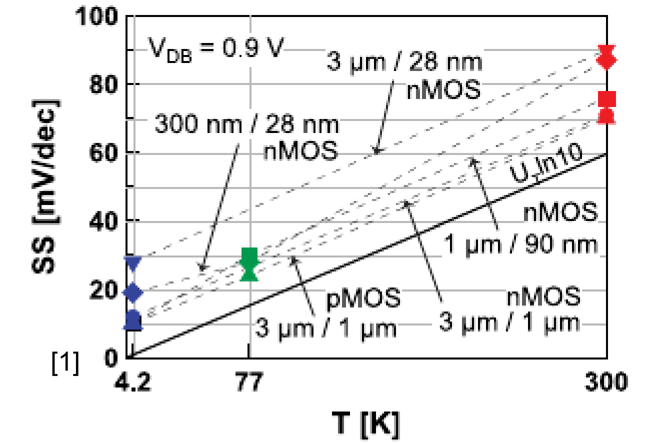
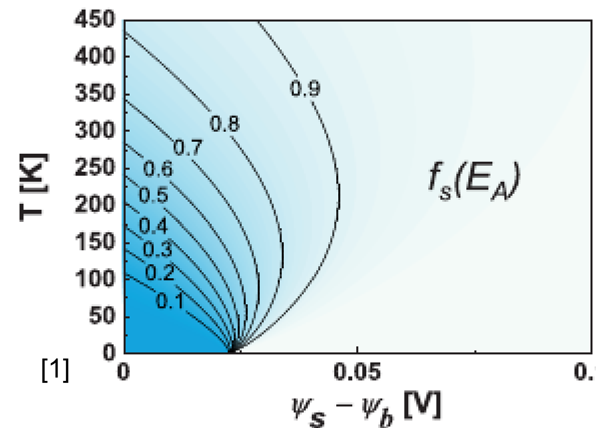
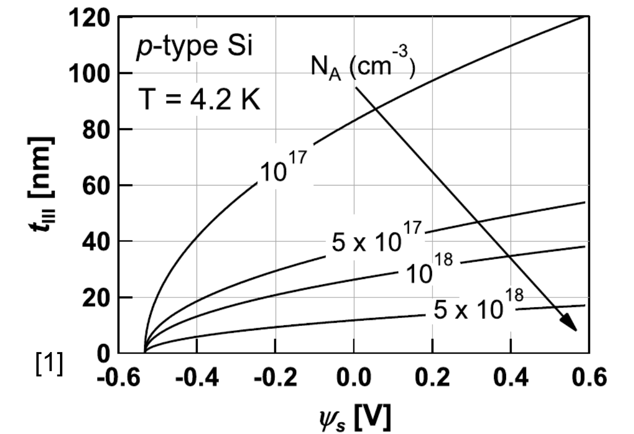
CRYOGENIC PHENOMENA - CMOS ELECTRONICS

- Threshold voltage V_{TH} increases
- Subthreshold swing (SS) decreases → slope increases
- Mobility increases (phonon scatt. red.)
- Dopant freeze-out
- Built-in potentials increrase → PN junction depletion regions widen
- Thermal noise reduction
- (+ short channel effects!)









[1] "Characterization and Modeling of 28 nm Bulk CMOS Technology down to 4.2K" Beckers et al., 2018

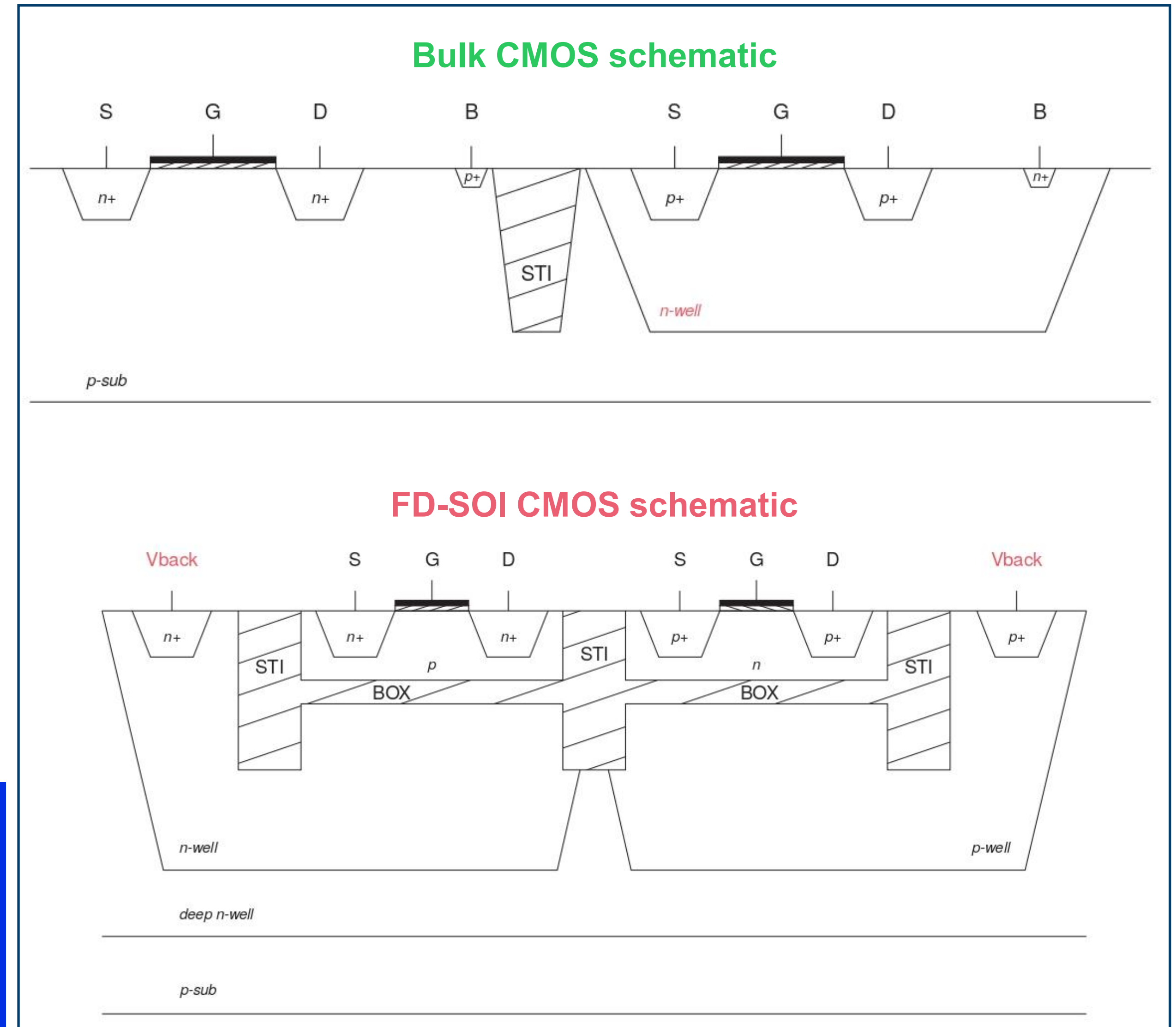
28-NM BULK CMOS

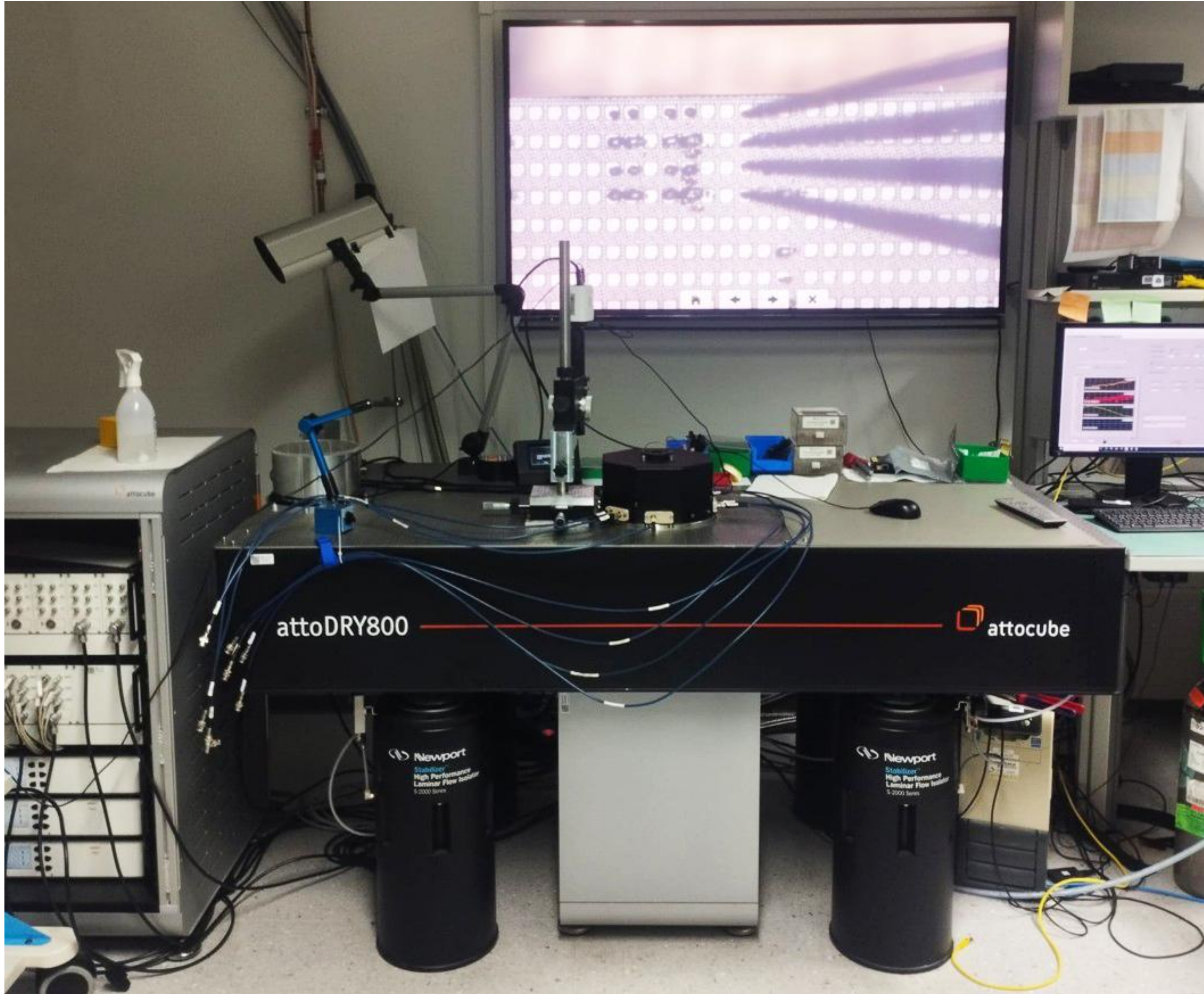
Technology Overview @cryo T

- Mature commercial tech, 2011
- Balance of **cost**, **power consumption** and **performance**
- Dominant in many applications (Detector ASICs, Analog/Mixed-Signal Ics, scientific R&D)
- One of the last av. planar CMOS nodes

BULK vs FD-SOI @CRYO:

- **Cost** effective
- **Less** self heating
- **No** V_{TH} control (V_{back})
- **Freeze out**





CRYOGENIC MEASUREMENT SETUP

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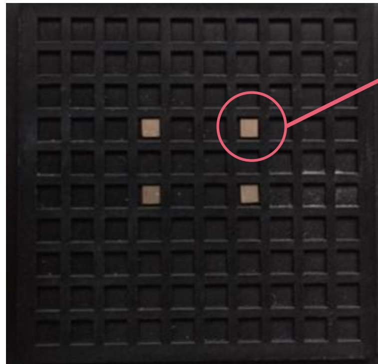
SAMPLE DUT

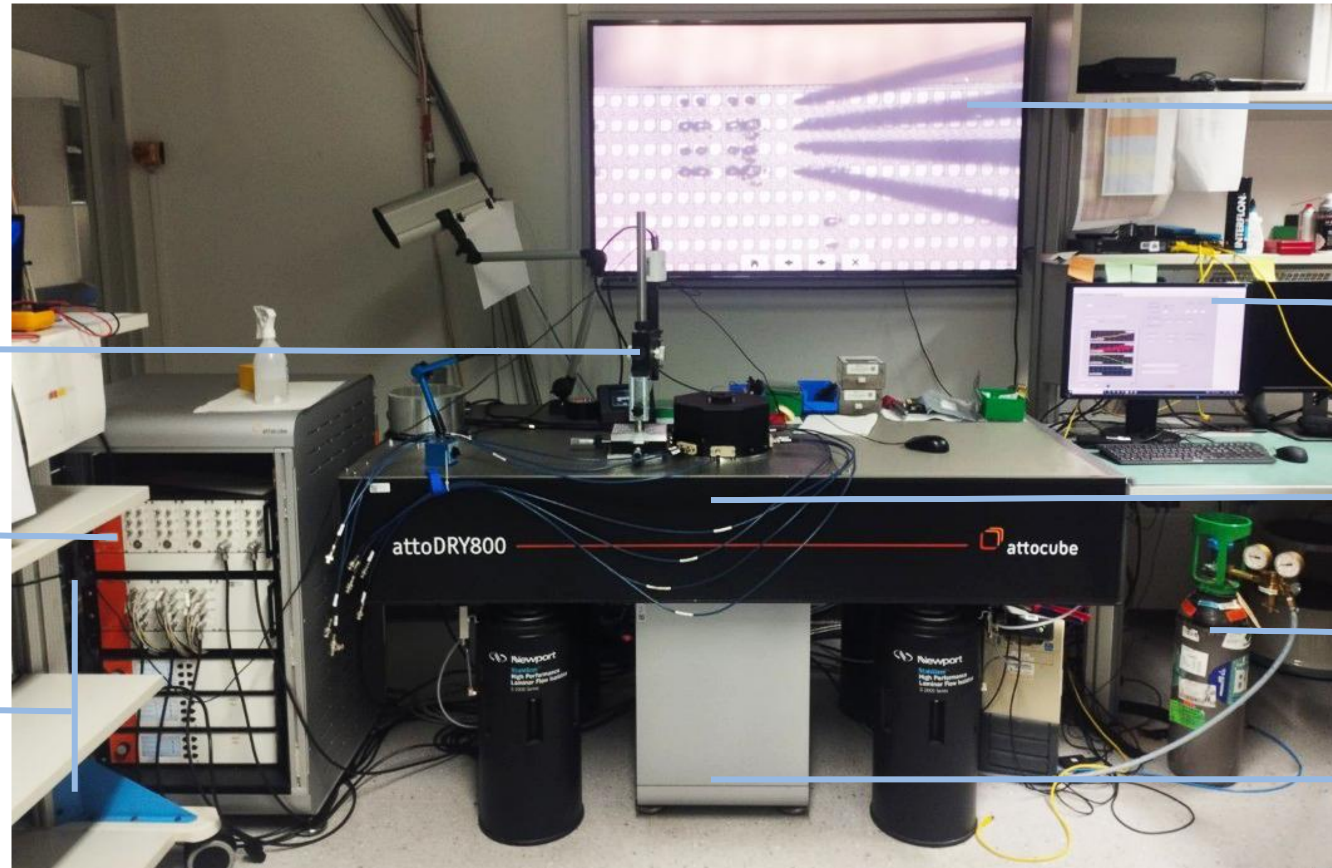
28-nm CMOS multi-geometry chip for needle probing

- Courtesy of Giulio Borghello – DRD7, CERN
- pMOS and nMOS Test-transistors on p-sub
- Intended for Total Ionizing Dose (TID) tests
- 28-nm, 16 pads per Column



1 mm

ATTODRY800 DRY CRYOSTAT WORKSTATION



Probing Screen

Control PC

Microscope

Cryostat

Fischer Lines

N2 Bottle

Piezo Modules

Vacuum Circuit

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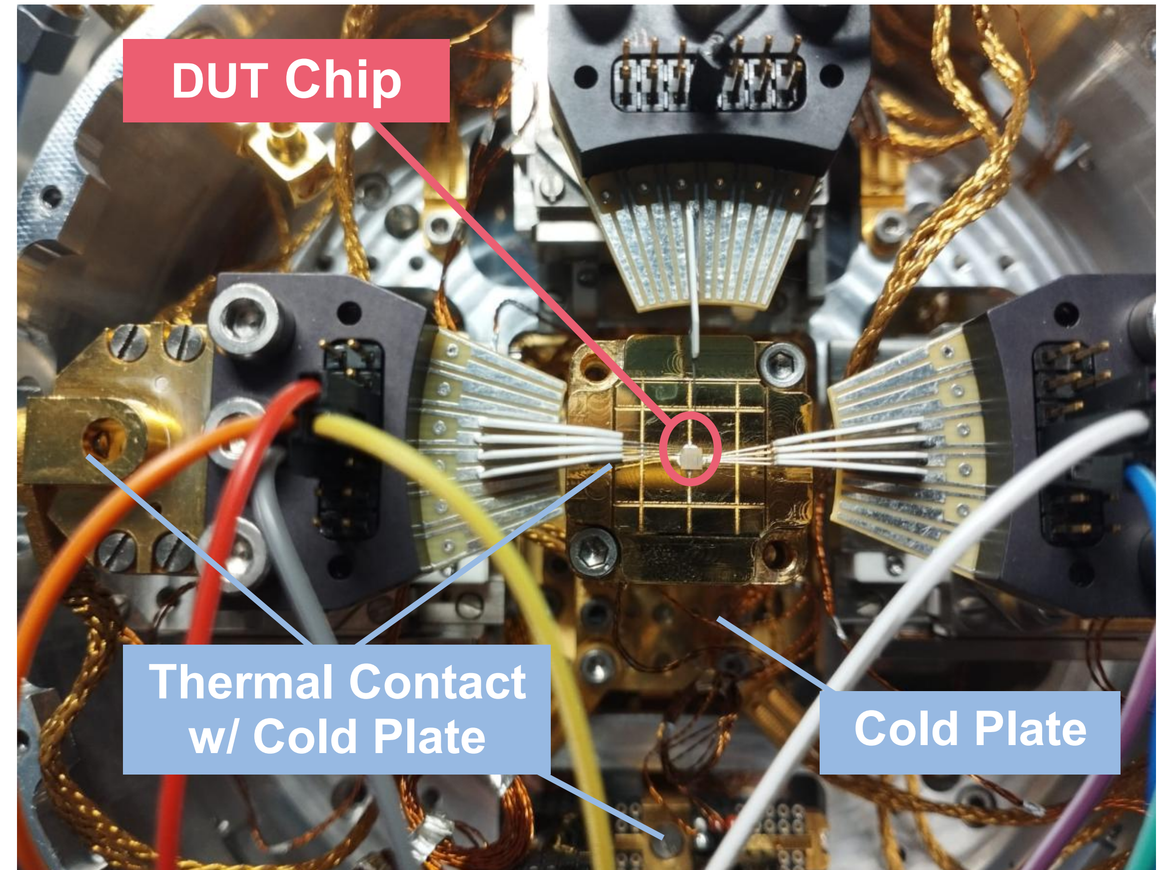
ATTODRY800 CRYOSTAT SETUP

Needle Probing Configuration

- AttoDRY800 dry cryostat @FZJ
- Configuration with 3 **Piezo Positioners**, mounting a needle probe
- DC signal through **Fischer Lines**
- Outer shield: thermalized at **60K**
- Probes, Fischer slots and sample chip thermalized @8K
- Heater and T sensor under sample base



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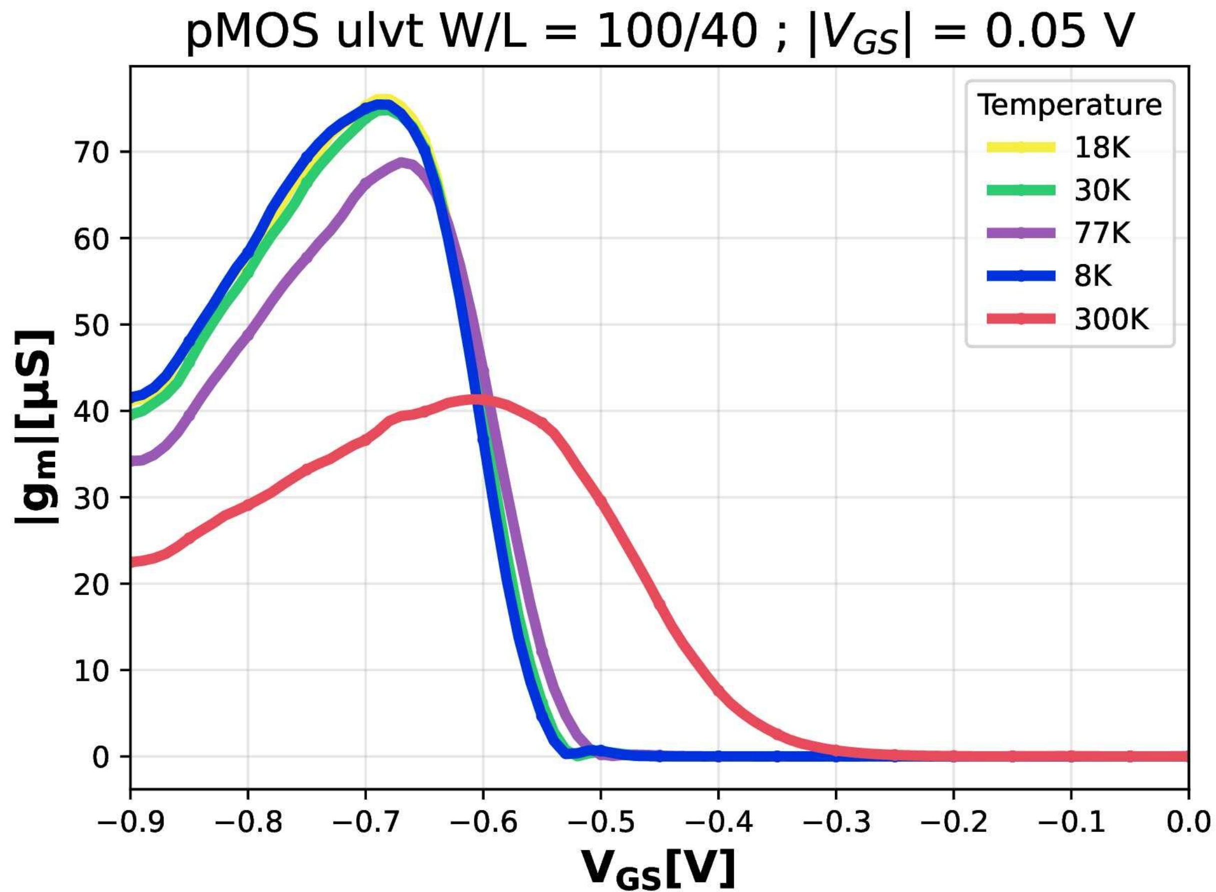

CRYOGENIC TEMPERATURE DEPENDENCE CHARACTERIZATION

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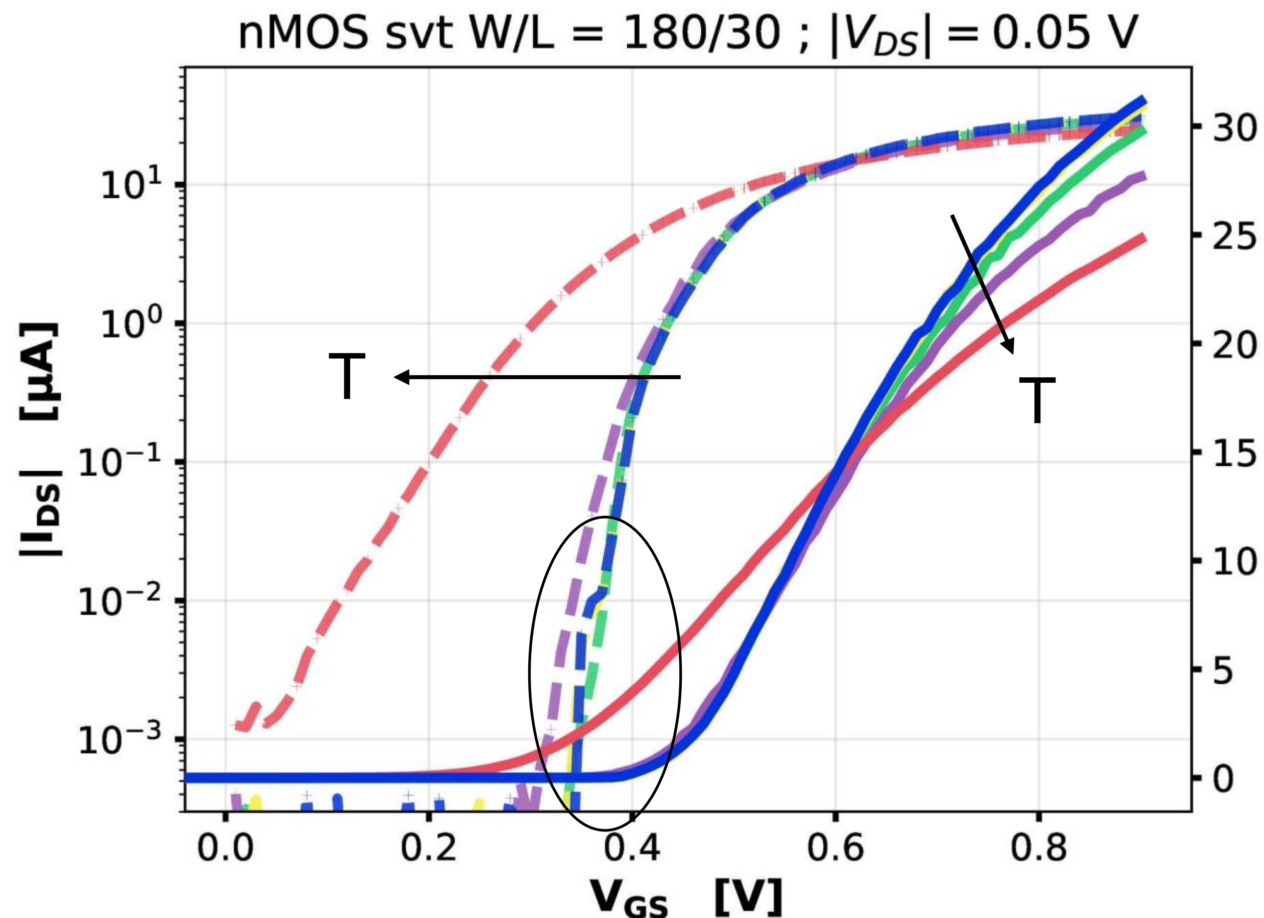
TRANSFER CURRENTS

- Measured @ 300K, 77K, 30K, 18K, 8K
- Different geometries and threshold flavours (svt, lvt, ulvt)
- Example: Standard V_{th} nMOS 180/30
- Dashed lines – log scale; solid lines – lin scale
- Evident increase of subthreshold slope @cryo T



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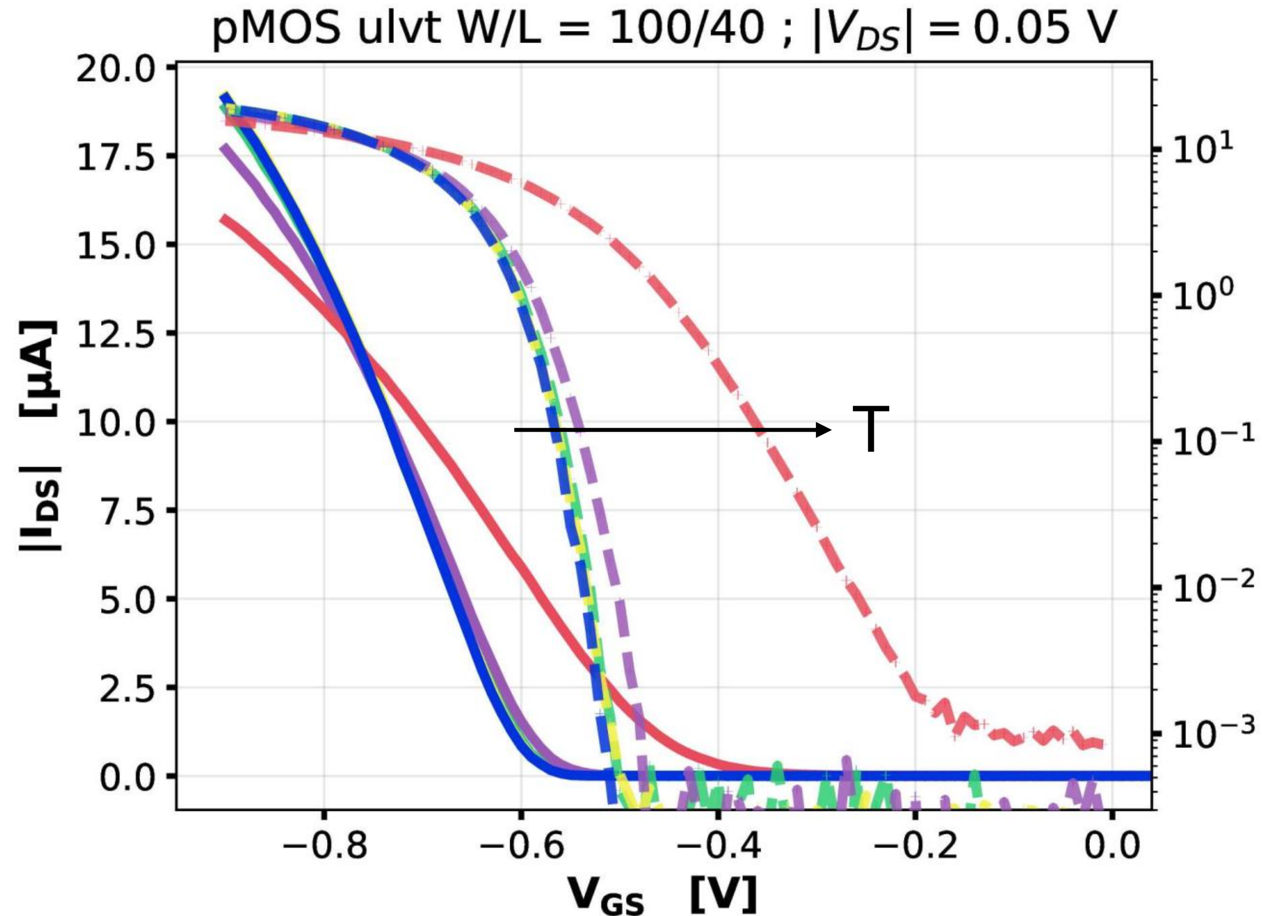
TRANSFER CURRENTS

- Measured @ 300K, 77K, 30K, 18K, 8K
- Different geometries and threshold flavours (svt, lvt, ulvt)
- Example: Ultra-low V_{th} pMOS 100/40
- Dashed lines – log scale; solid lines – lin scale
- Evident increase of subthreshold slope @cryo T



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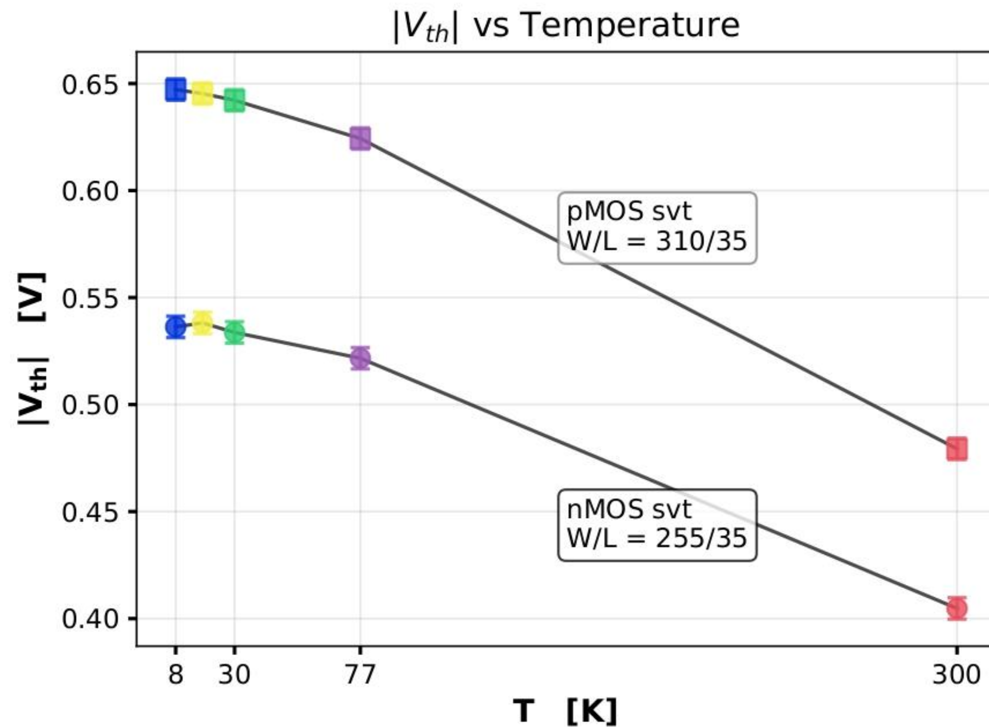
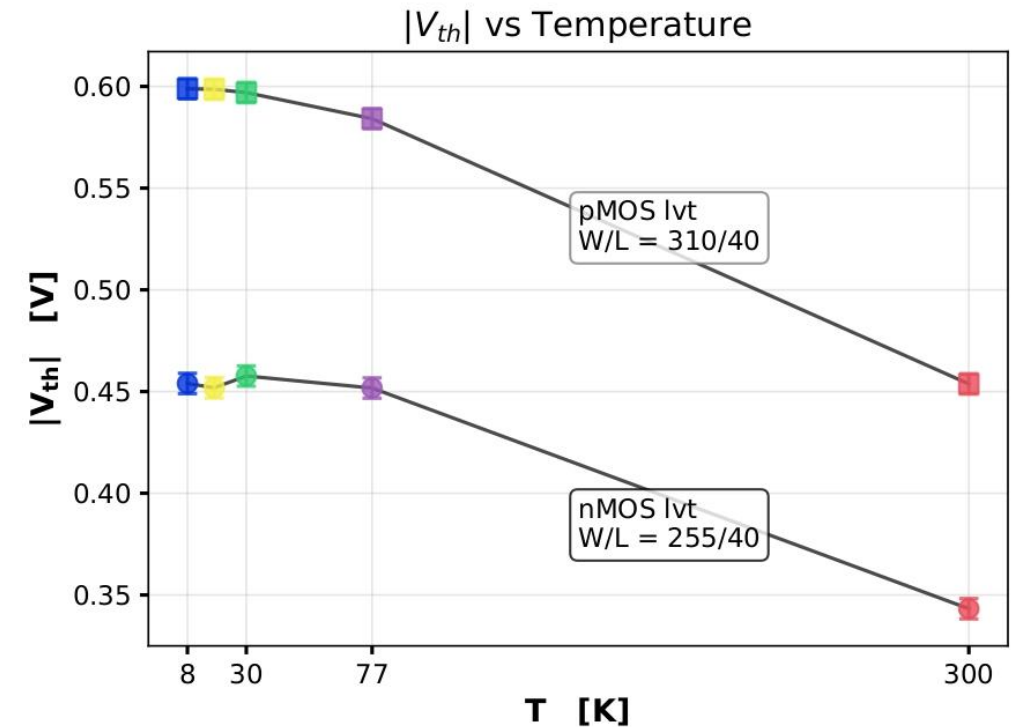
THRESHOLDS

LE (Linear Extrapolation) Method [1]

- Threshold increase of more than 100mV @cryo T observed for every device





[1] "Revisiting MOSFET threshold voltage extraction methods" Ortiz-Conde et al., 2013

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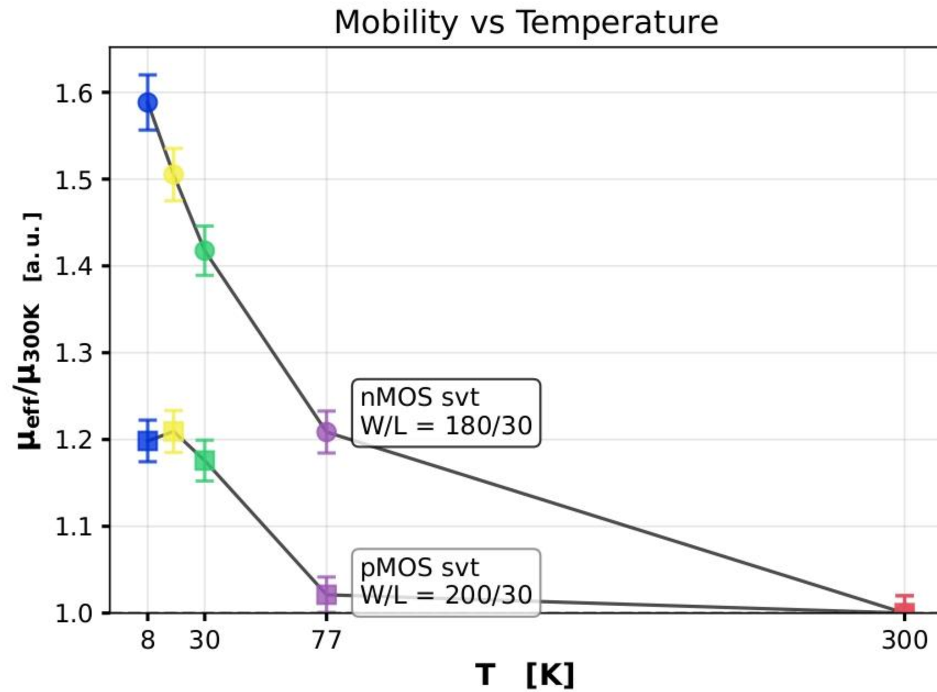
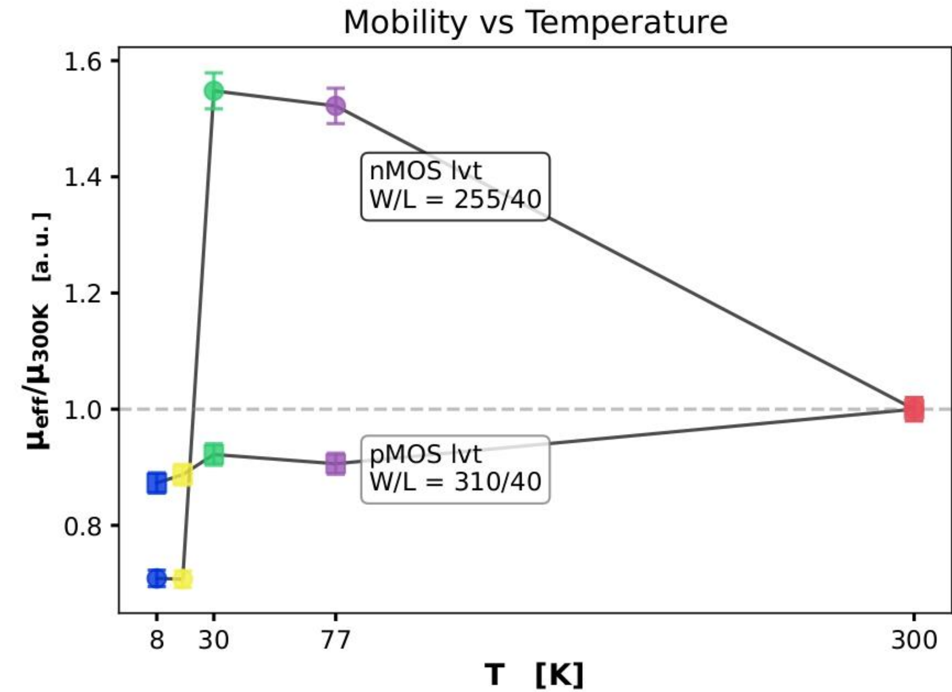
FREE-CARRIER MOBILITIES

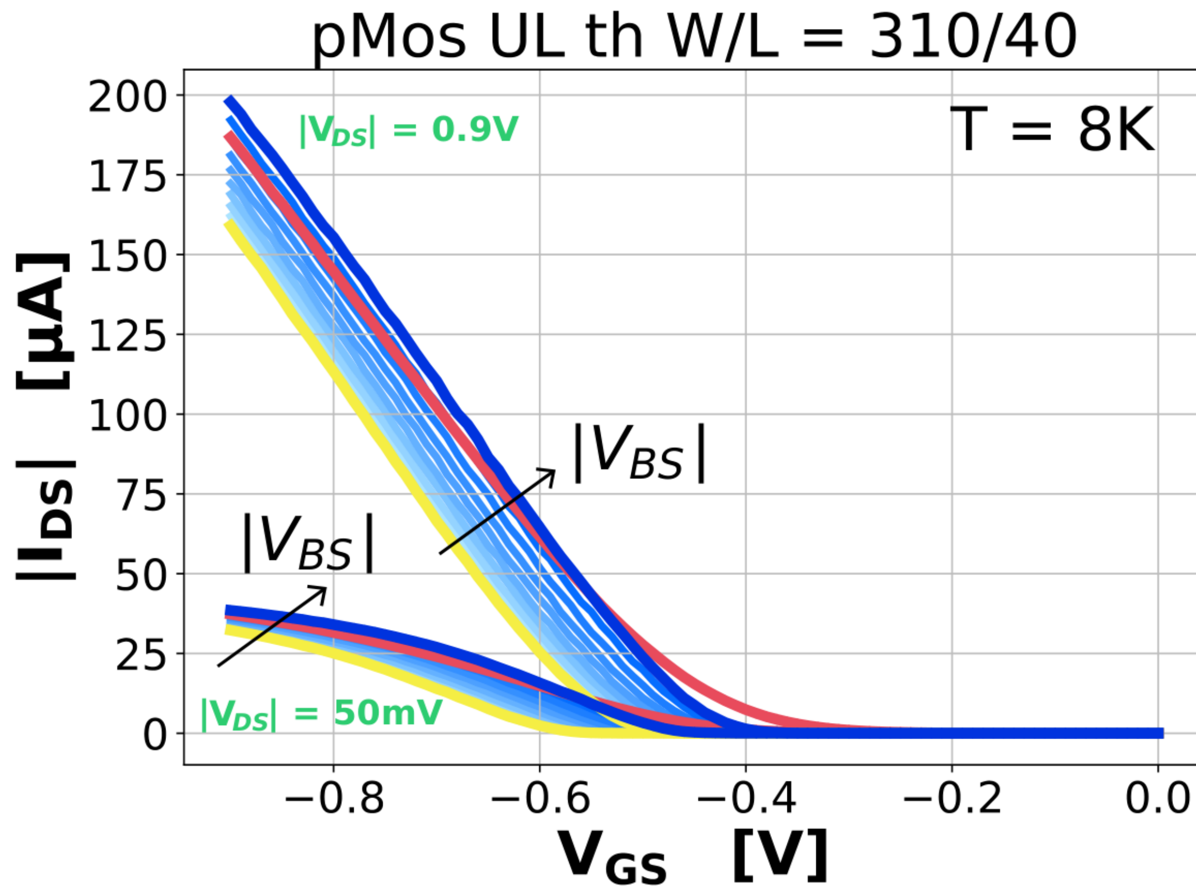
Jazaeri g_{ds} method [1]





- $\mu_{eff} \cong -2 \cdot \frac{L}{W} \cdot \frac{1}{C_{ox}} \cdot \frac{\partial g_{ds}}{\partial V_{DS}}$ where C_{ox} is the gate-oxide capacitance and $\frac{\partial g_{ds}}{\partial V_{DS}}$ is fitted at $|V_{GS}| = 900mV$ (strong inversion) $|V_{DS}| = 50mV$ (linear region)

[1] „Free Carrier Mobility Extraction in FETs", F. Jazaeri et al., 2017



THRESHOLD ADJUSTMENT IN BULK TECHNOLOGY

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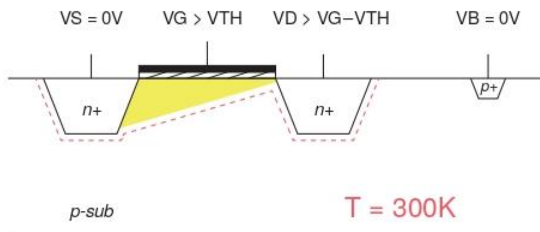
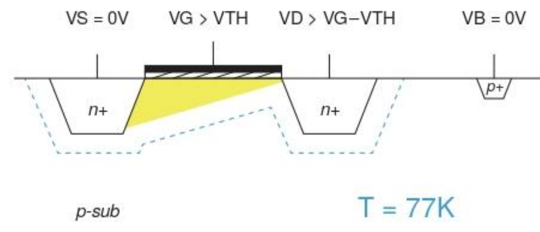
FORWARD BODY BIASING FOR TUNING V_{th}

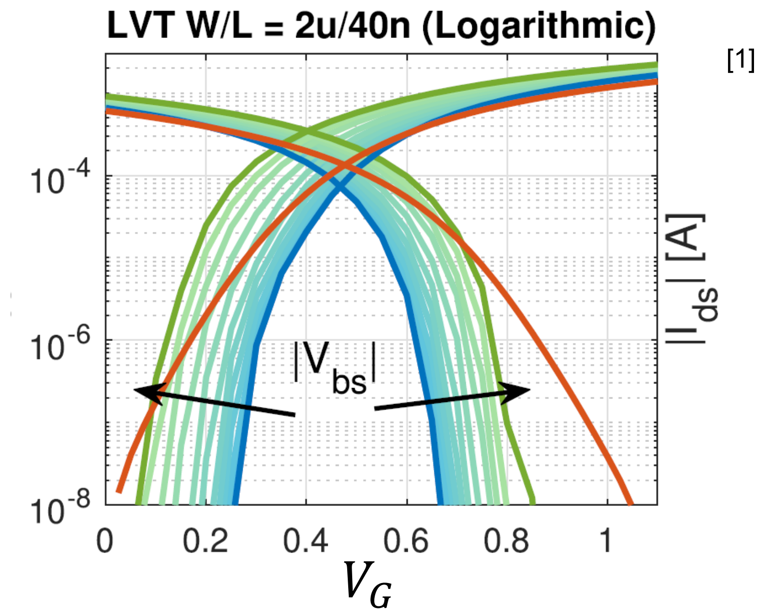
- **In a Bulk Tech:** increasing the Source-Bulk potential: Forward body biasing (FBB) →Compensation of V_{th} (bigger tech nodes)

$$V_{th,n/p} \propto \sqrt{V_{SB}}$$

- Demonstrated in 40 nm Tech → possible because of increasing built-in potentials and depletion regions at cryo T [1]
- First time test on 28-nm, only pMOS FBB







[1] TU Delft : Cryogenic-Aware Forward Body Biasing in Bulk CMOS, Overwater et al. 2024

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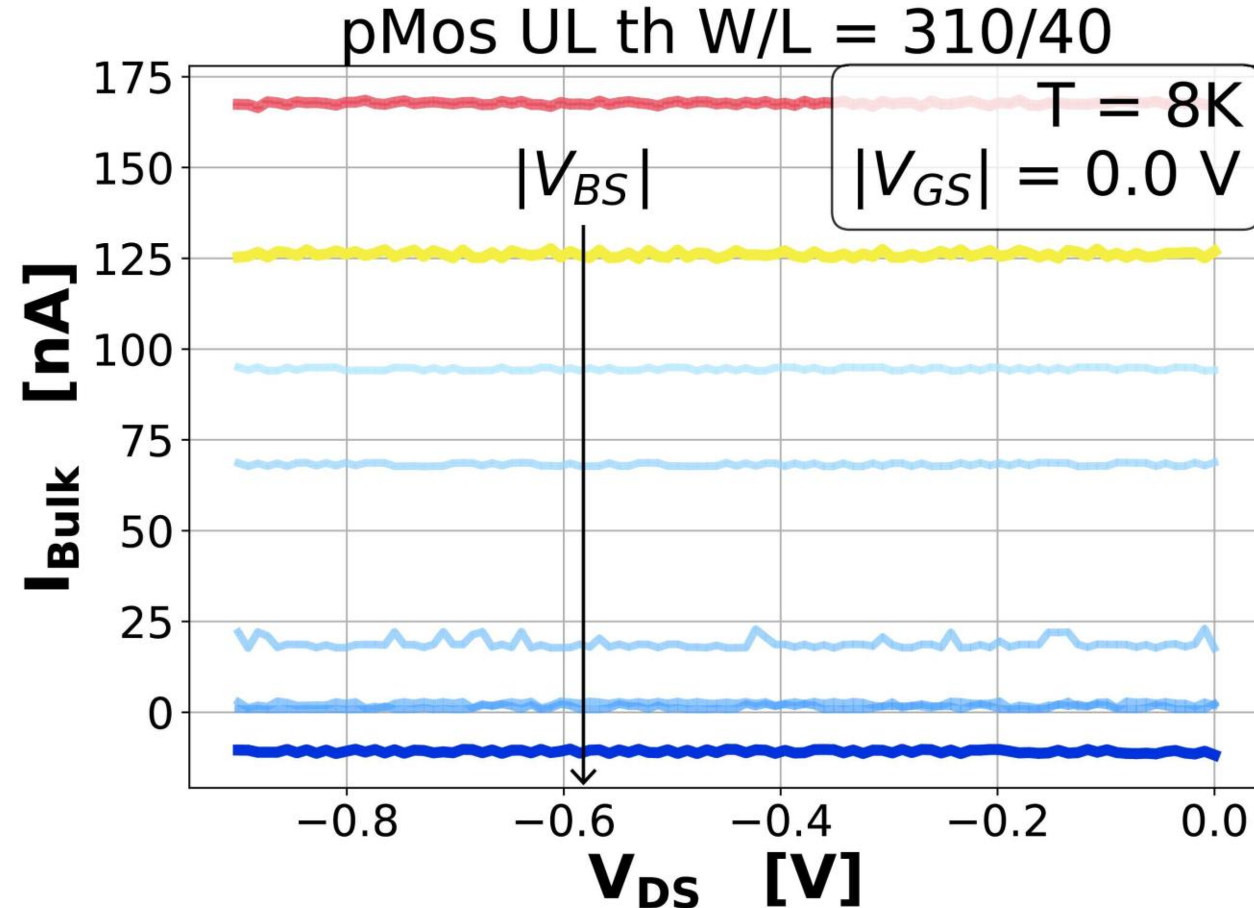
FORWARD BODY BIASING LIMITS AND LEAKAGES

Example UL threshold pMOS 310/40 @T=8K

T	$V_{SB,start}$	$V_{SB,stop}$	V_{step}
8K	0V	900mV	100mV
30K	0V	800mV	100mV
77K	0V	800mV	100mV

- All off/on leakages monitored, $|V_{SB}|$ swept until S-B diode turned on (beyond tech limits at 8K)
- Significant rev-leakage current reduction → ulvt more viable (of interest because of lower V_{TH} and lower doping → less freeze-out impact)



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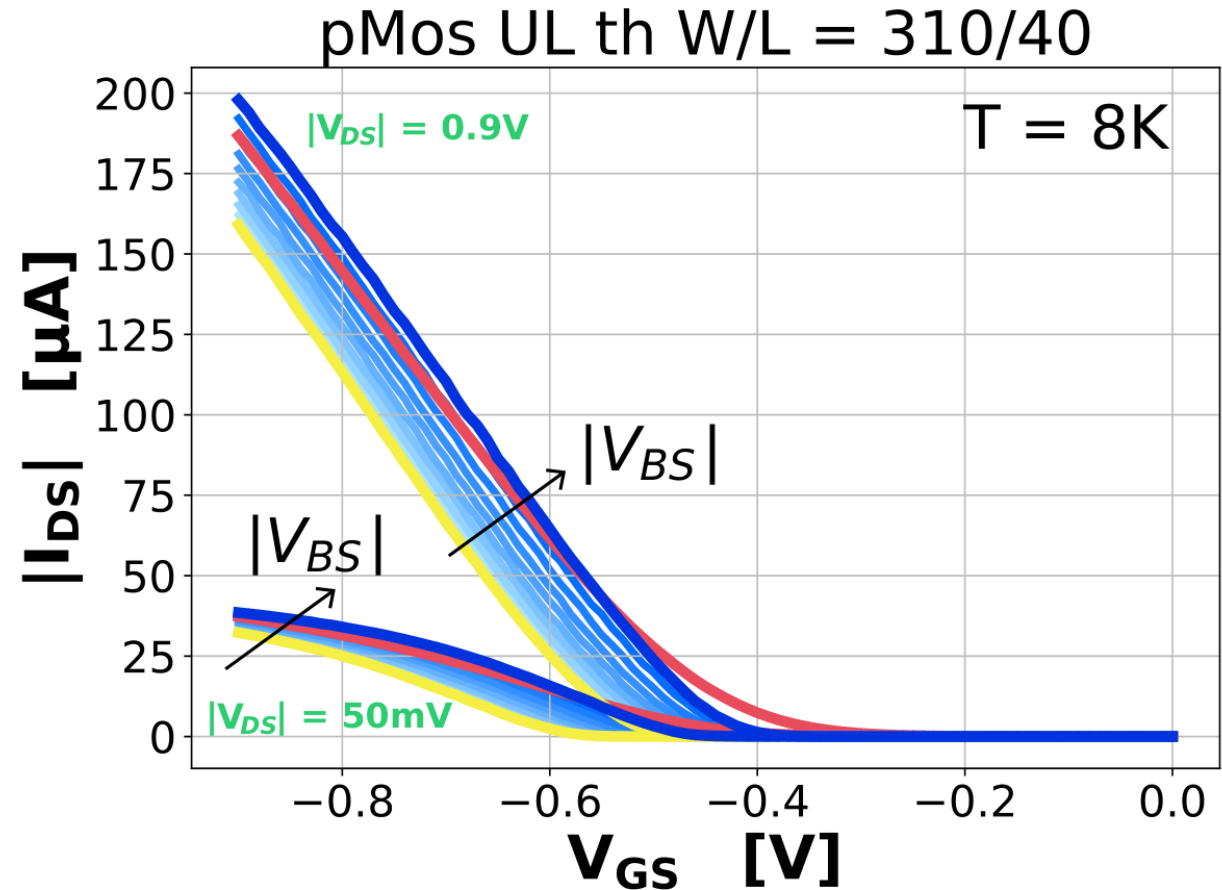
FORWARD BODY BIASING RESULTS

Example UL threshold pMOS 310/40 @T=8K

- Color legend: $V_{SB} = 0V$, $V_{SB} = 900mV$, $V_{SB} \rightarrow increasing$, $V_{SB} = 0V\ and\ T = 300K$

- Transfer and strong inversion output characteristics shown, exhibiting threshold decrease and output current increase



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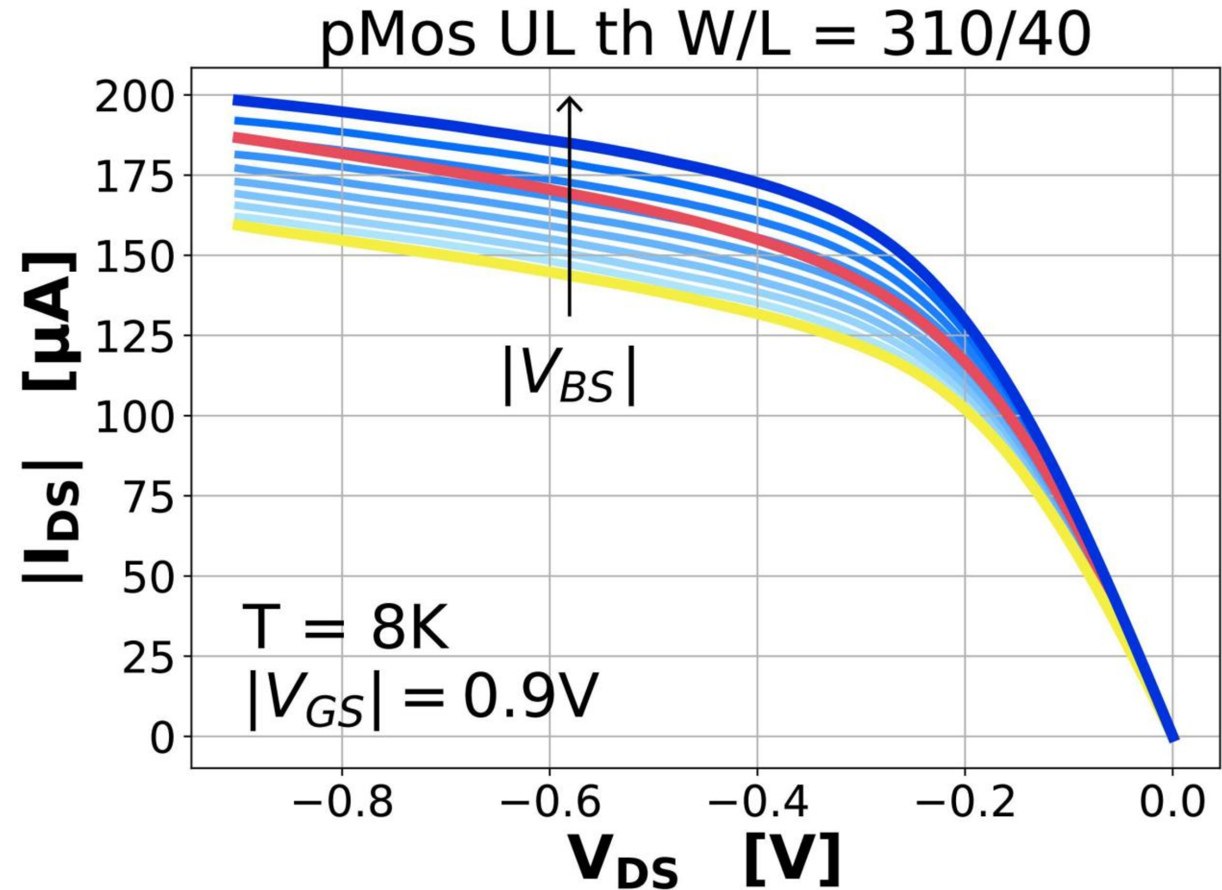

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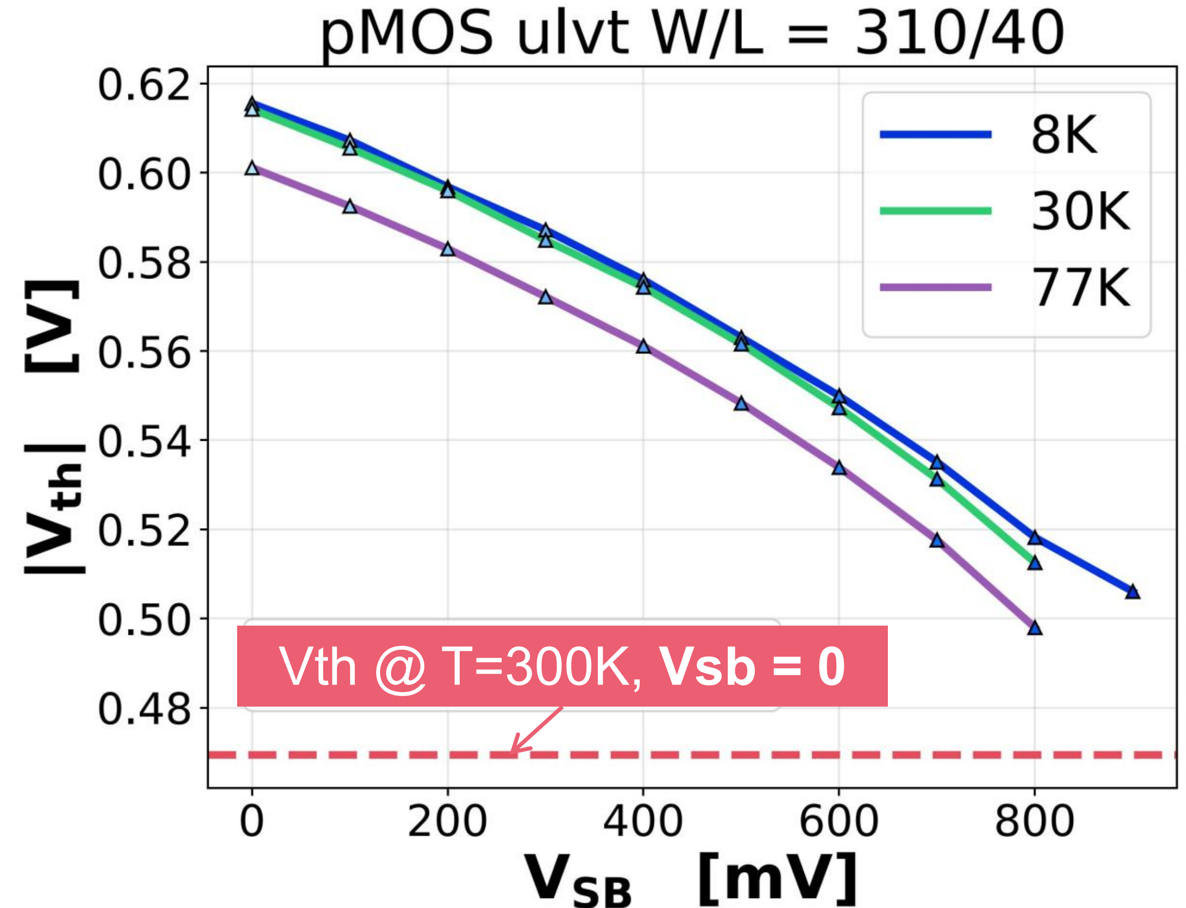
FORWARD BODY BIASING V_{TH} TUNING

Example UL threshold pMOS 310/40

- V_{th} with LE (Linear Extrapolation) Method [1]

- For no measured device V_{TH} reached room T level of operation
- A significant threshold voltage reduction of $\sim 100mV$ is obtained, similarly at every temperature



[1] "Revisiting MOSFET threshold voltage extraction methods" Ortiz-Conde et al., 2013

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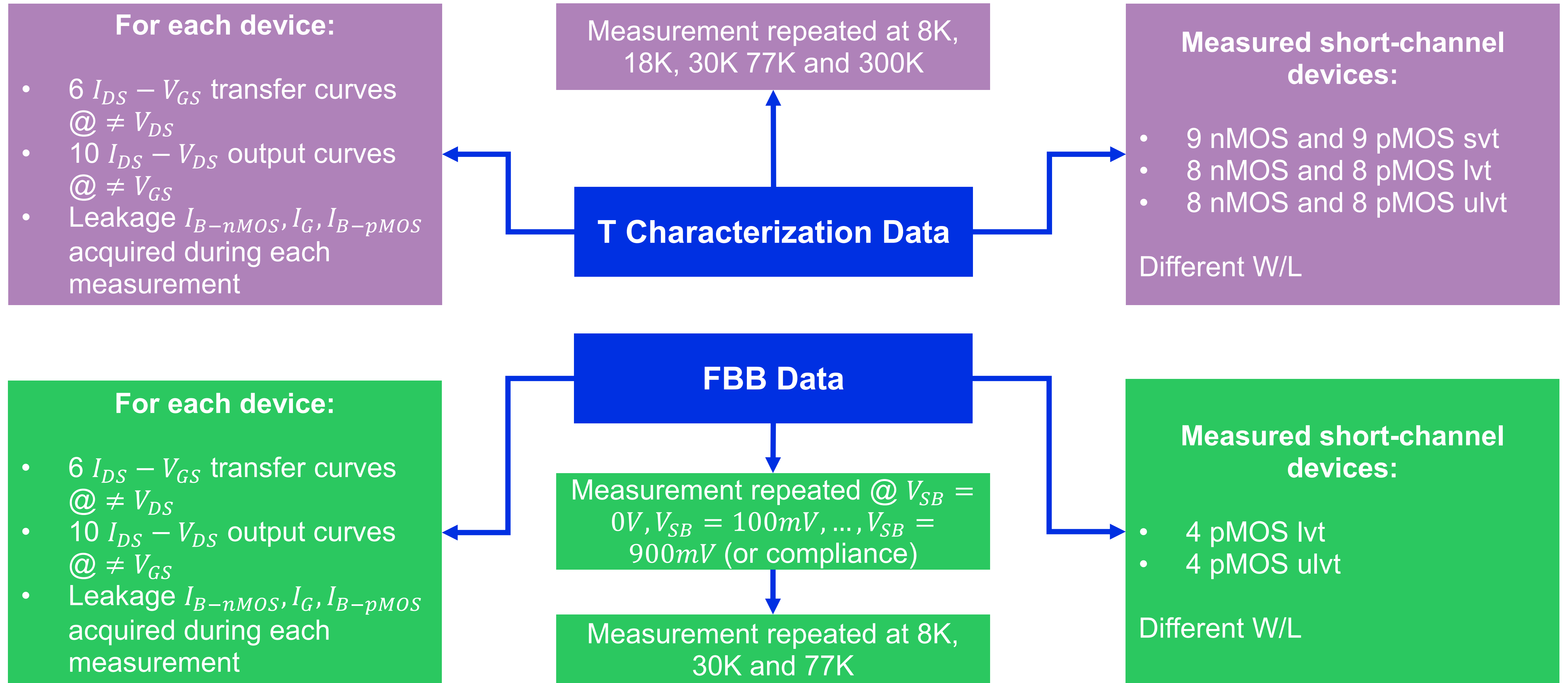
EXPERIMENTAL DATA – IN A NUTSHELL



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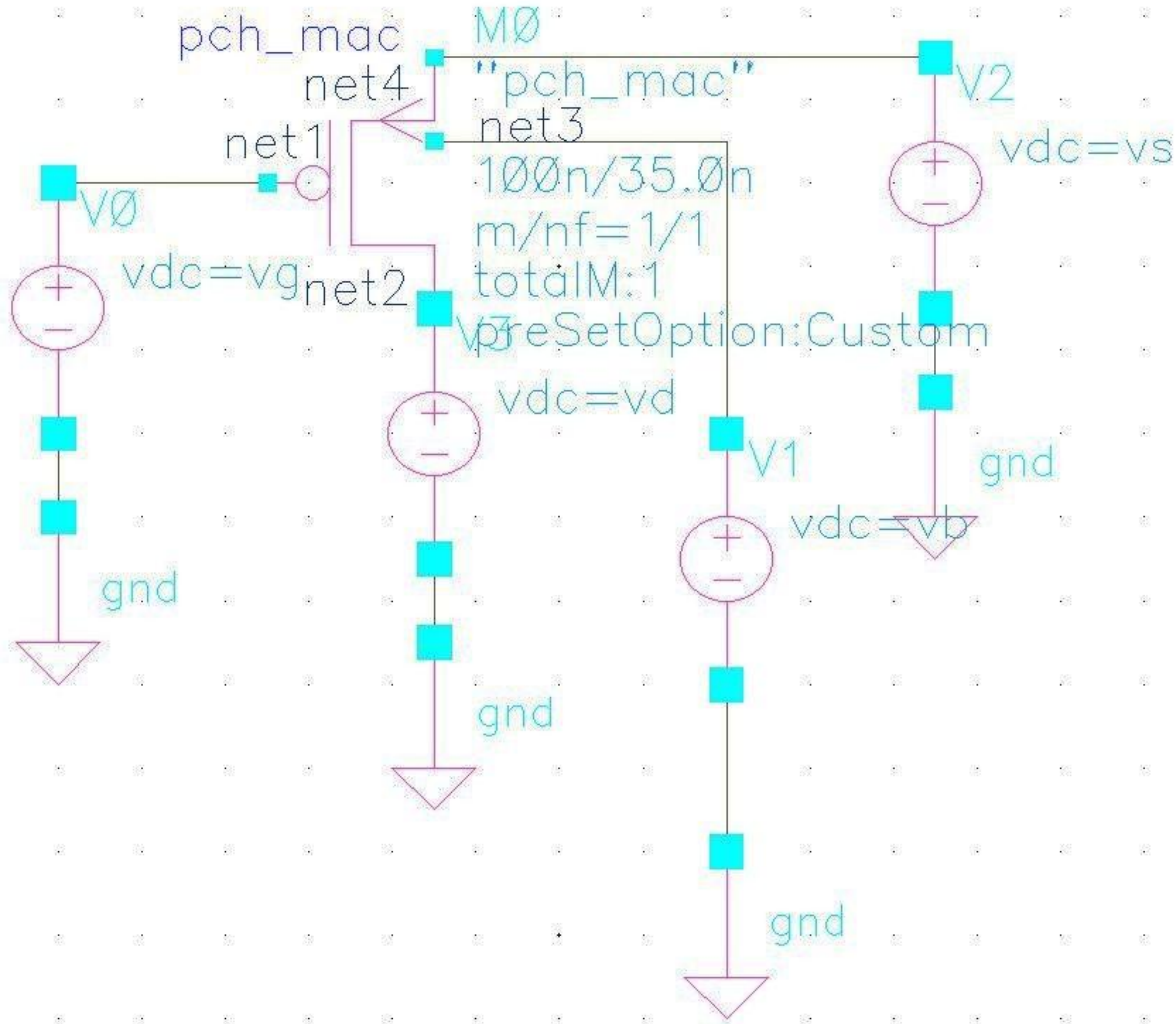

METHOD FOR CRYOGENIC CMOS MODEL EXTENSION

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THE PARTIAL CRYO-PDK PROCEDURE

Software Setup

Goal: partial PDK
establish a **procedure** to create **cryo-corners** in 28-nm, valid at fixed thermal states

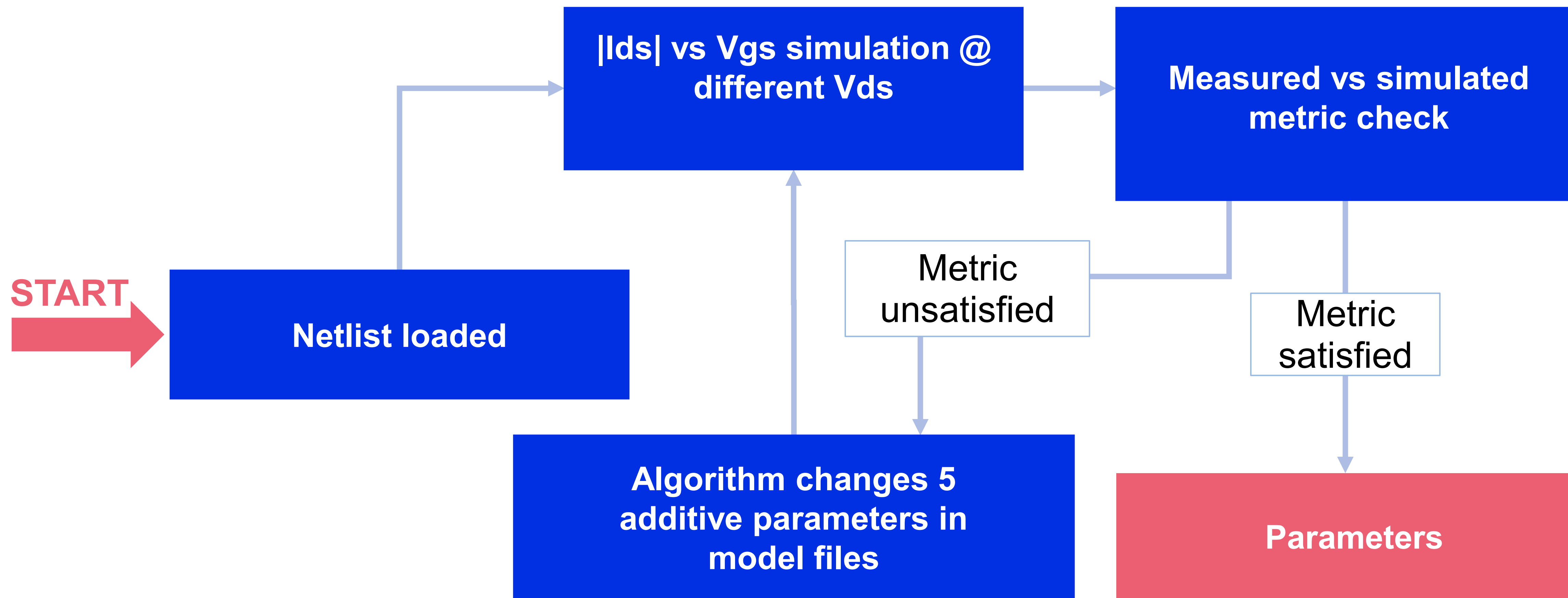
- SW Setup: Cadence Spectre + Python possible thanks to **pyspectre interface** [1]
- Model: **BSIM-BULK** (former BSIM-6) [2]
- Workspace was tested @ FZJ and setup @ INFN Torino

- 5 BSIM-BULK T dependent parameters chosen
- Additive components in custom model files → $par = par_{28nm} + \boldsymbol{par_{CRYO}}$
- Custom model files accessible via pyspectre

[1] "PySpectre: Python interface for Cadence Spectre" GitHub repository. Y. Uhlmann., Version 1.2.0. 2024
[2] "BSIM-BULK 107.2.1 MOSFET Compact Model". Berkeley, CA, 2025

THE PARAMETER EXTRACTION PROCESS

Pyspectre flow



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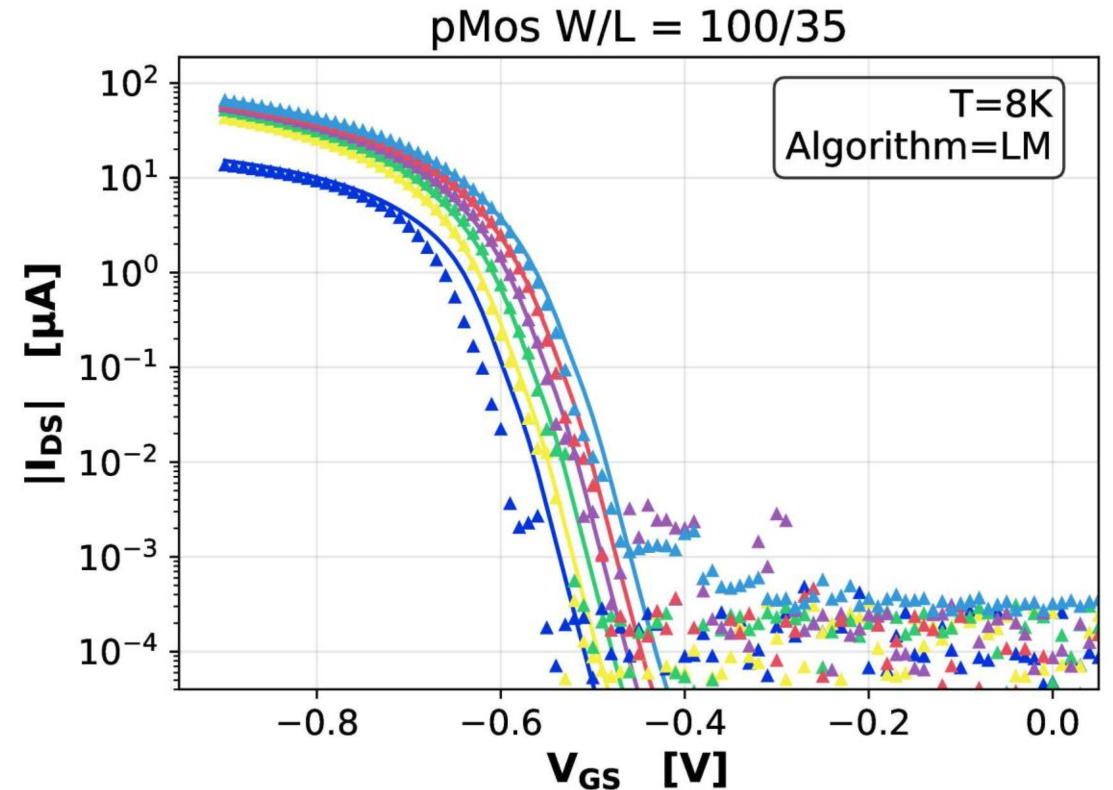
METRIC AND MULTIPLE FITTING ALGORITHM

svt pMOS W/L = 100/35

- Procedure tested on a single svt pMOS W/L = 100/35
- Chosen metric → mean square error sum $[A^2]$ with weightintg: moderate (50x) in strong inversion, heavy (150x) in sharp moderate inversion, light (0.5x) for sub-threshold noise
- Algorithms → two multidim tested: Levenberg-Marquardt and Nelder-Mead



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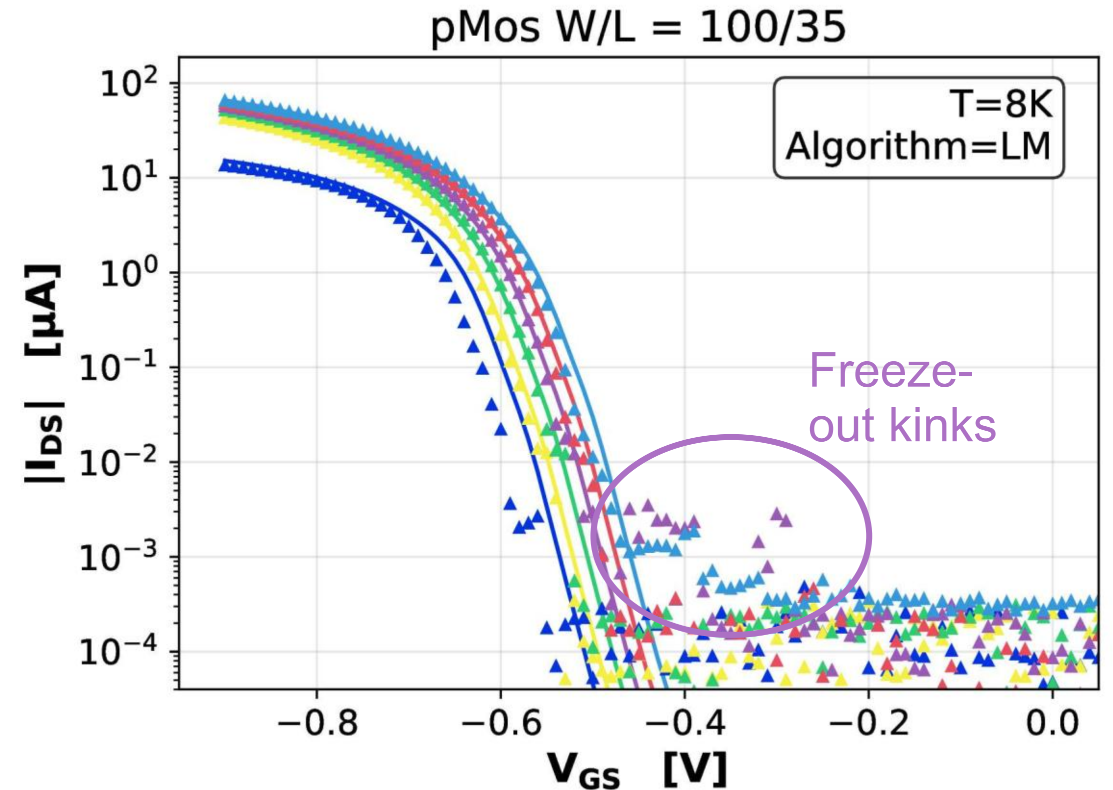

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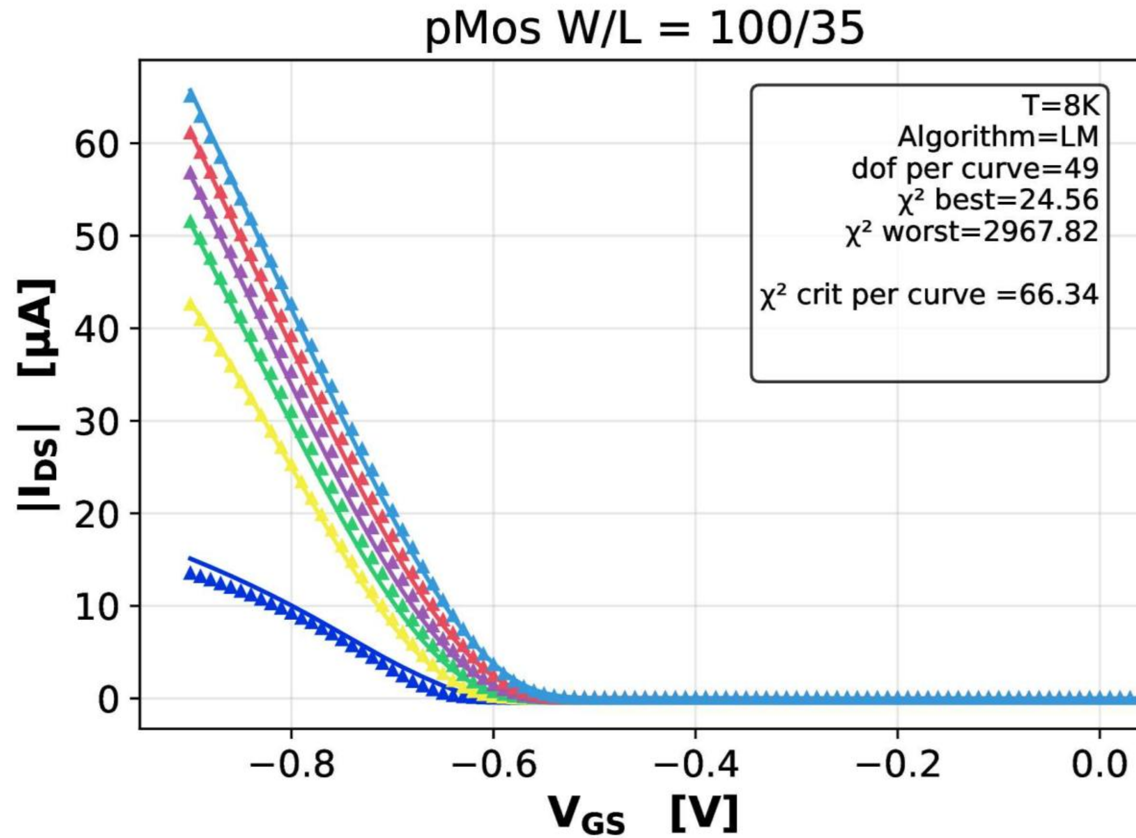
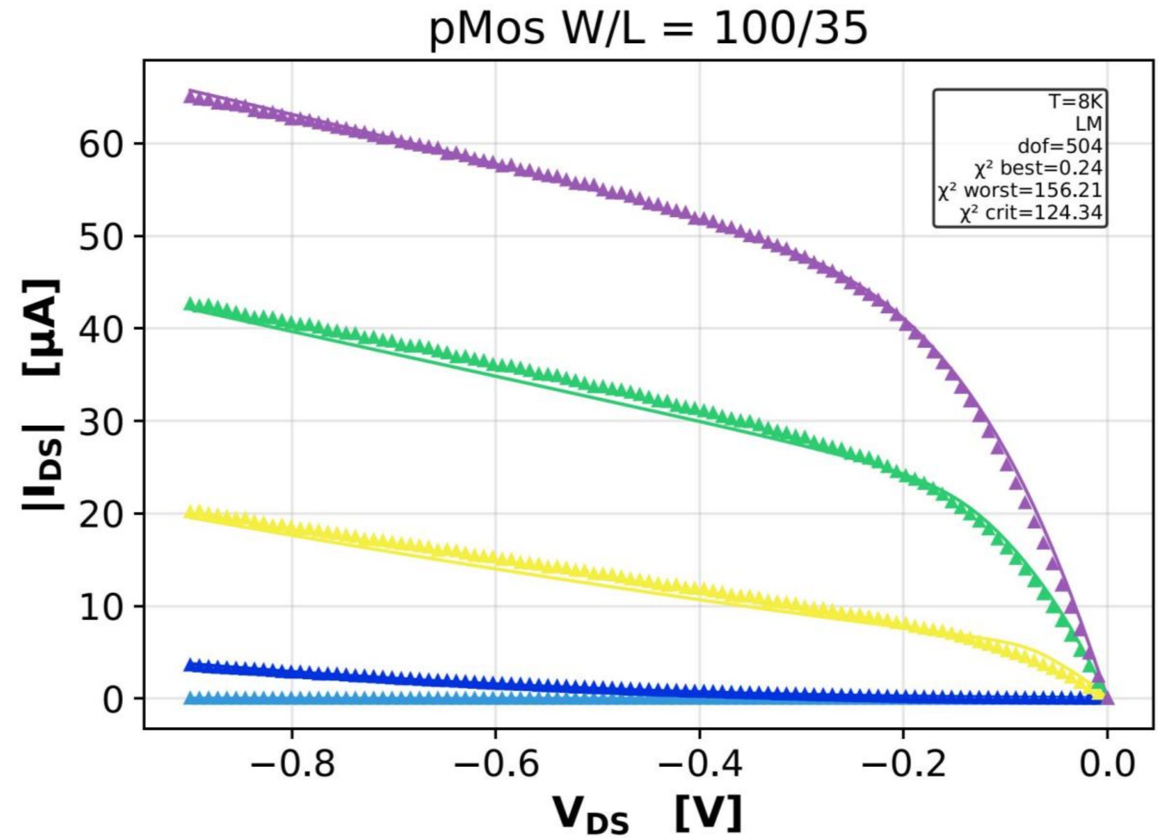
SIM VS MEAS DATA – 8K

svt pMOS W/L = 100/35





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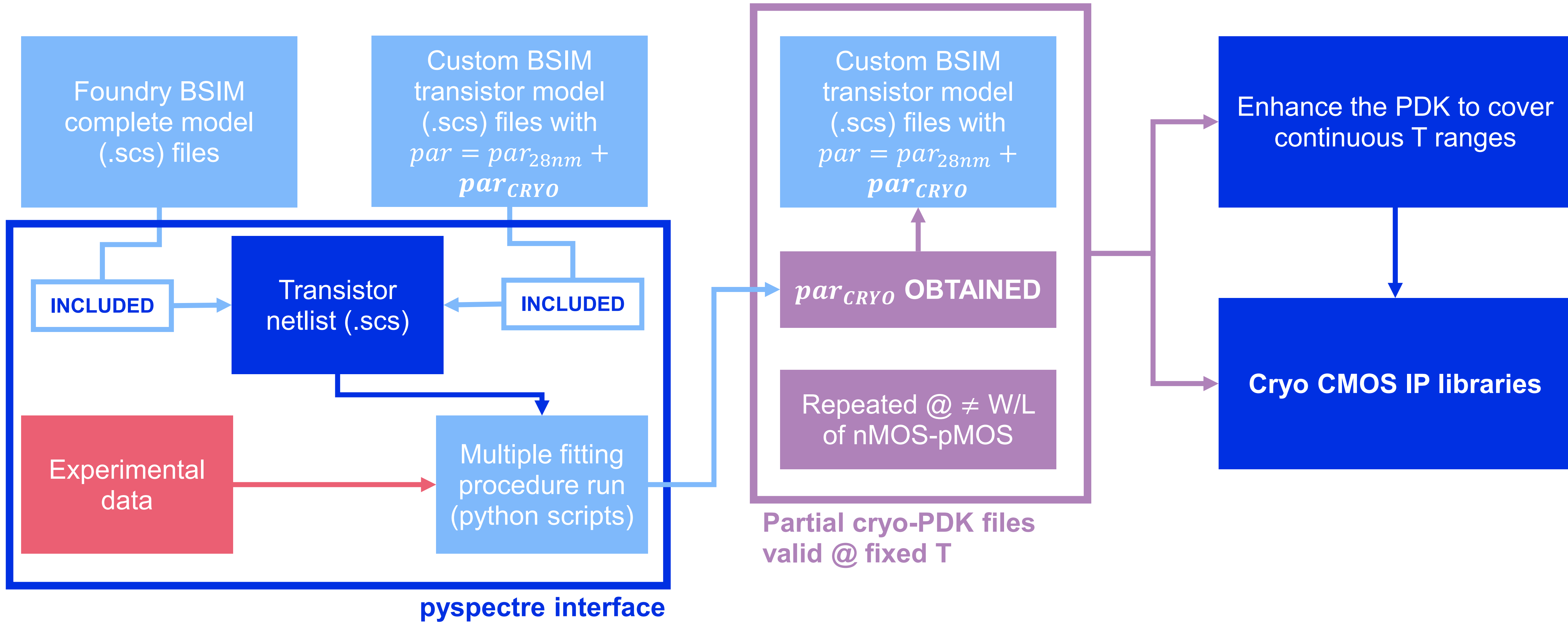
PARTIAL CRYO-PDK – IN A NUTSHELL



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CONCLUSIONS AND OUTLOOK

Conclusions

- Collaborative research between UniTO, INFN and FZJ; 4 months on site at Julich for cryogenic data extraction.
- Implementation of a partial cryo-PDK for a 28-nm bulk CMOS technology, using experimental data at 8-18-30-77K and state-of-the-art methodology for a model extension at fixed temperatures.
- First test of the cyo-FBB technique (used for trimming the device V_{TH}) on a bulk 28nm CMOS technology node.

Outlook

- Development of a new cryogenic device model allowing for simulation over a continuous temperature range (instead of fixed thermal states), in collaboration with TU Graz (Austria).
- Design of a new DUT (bulk-28nm, other techs) optimised for cryogenic measurements – current measurement campaign used a DUT developed for radiation hardness studies.
- Design of a cryo-IP (bulk 28-nm) prototype using the partial PDK developed and available for the complete demonstration of the cryo-PDK.

REFERENCES

Presentation references

- “DarkSide-20k sensitivity to light dark matter particles” Acerbi et al. 2024
- “Characterization and Modeling of 28 nm Bulk CMOS Technology down to 4.2K” Beckers et al., 2018
- “Revisiting MOSFET threshold voltage extraction methods” Ortiz-Conde et al., 2013
- “BSIM-BULK 107.2.1 MOSFET Compact Model”. Berkeley, CA, 2025.
- “PySpectre: Python interface for Cadence Spectre” GitHub repository. Y. Uhlmann., Version 1.2.0. 2024
- “Free Carrier Mobility Extraction in FETs”, F. Jazaeri et al., 2017
- “Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures” Beckers et al. 2019
- “Cryogenic-Aware Forward Body Biasing in Bulk CMOS” Overwater et al. 2024

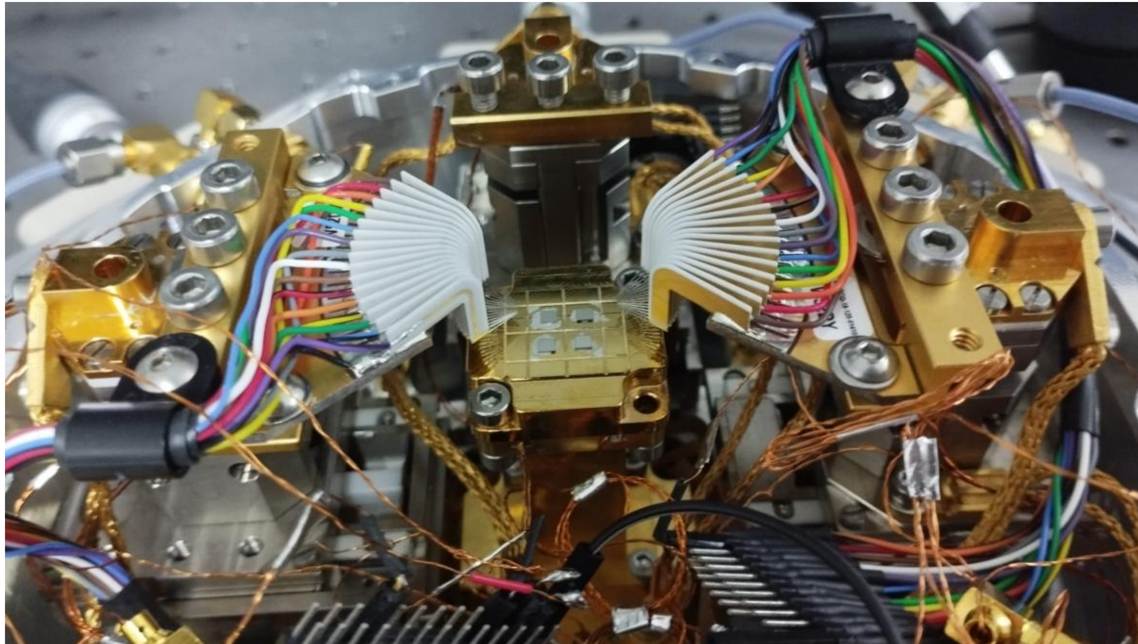
BACKUP - DISCARDED SETUP

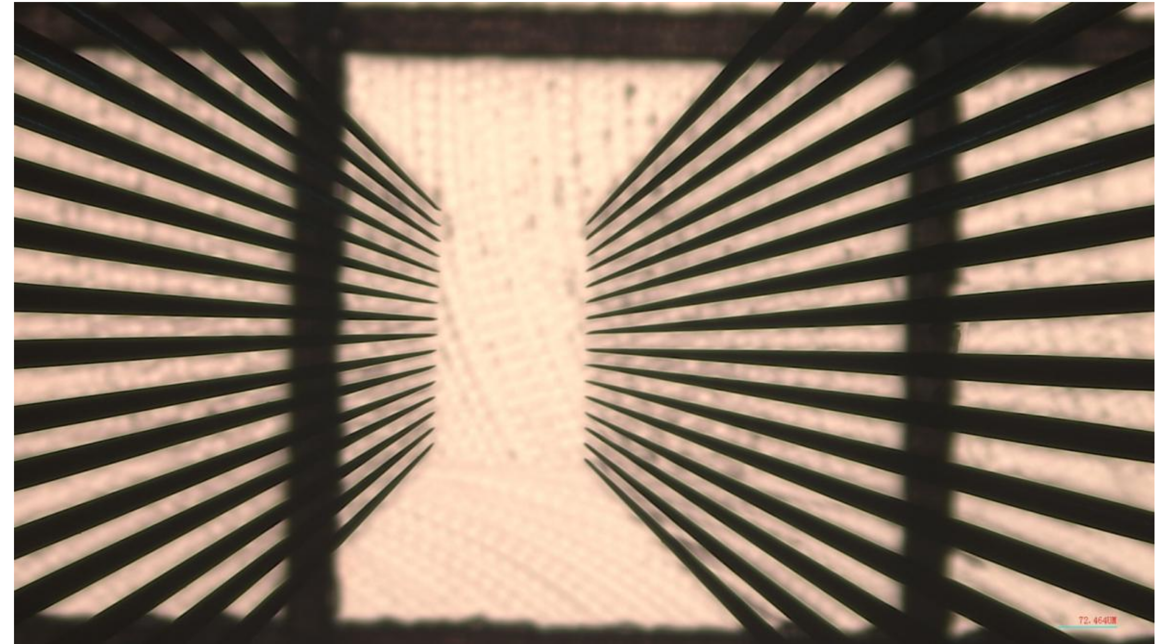
16L + 16R Needle Probes

- TID damage live monitoring:
  many devices contacted on the same cycle
- Contact @CERN: 2 entire columns sim. !!

Tried but **discarded**:

- Hard repeated contacts @cryo
- Vertical bending @cryo
- Lack of cryostat feedthroughs
- Heavy T load





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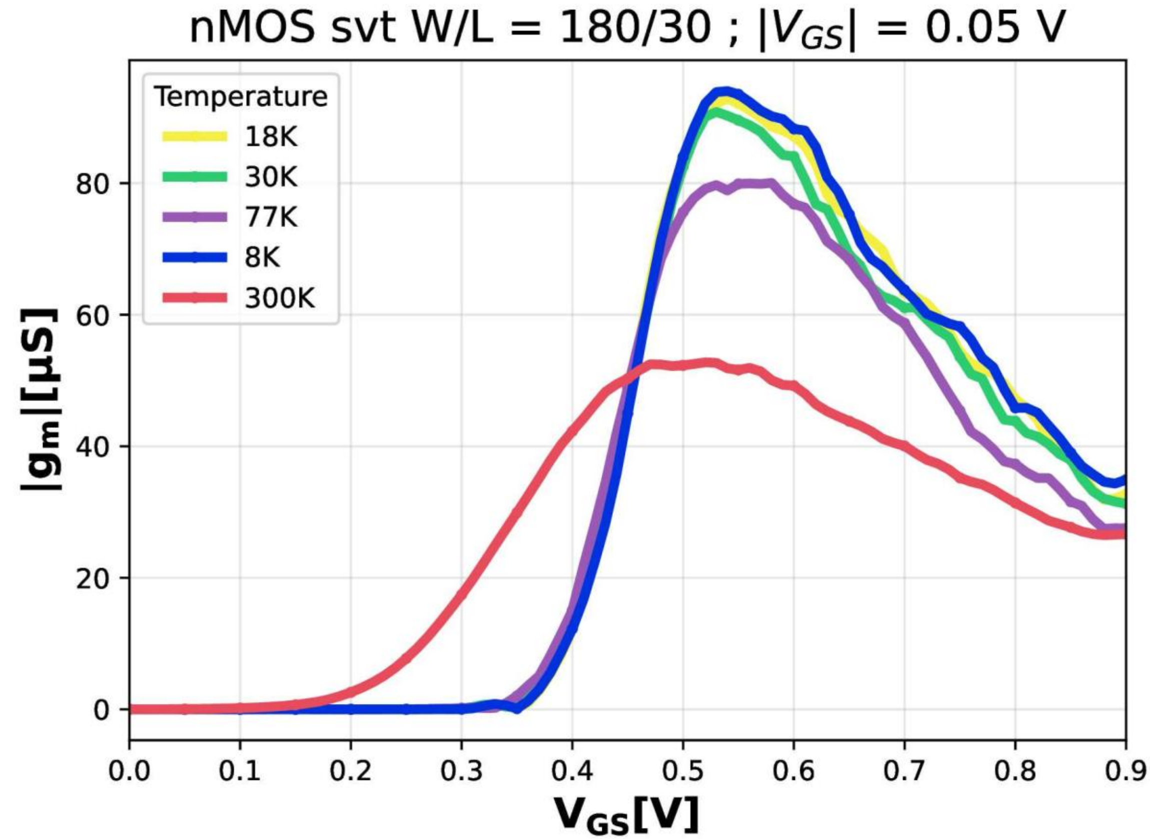
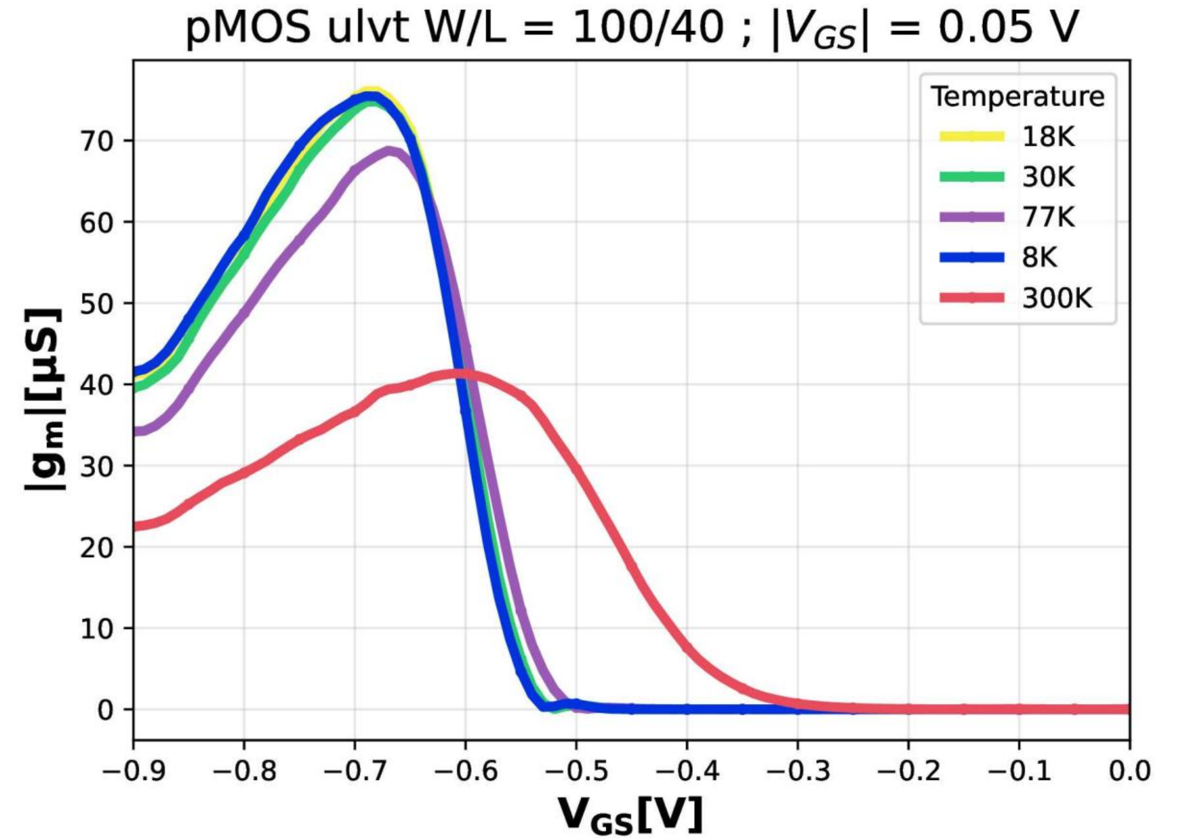
BACKUP - TRANSCONDUCTANCES





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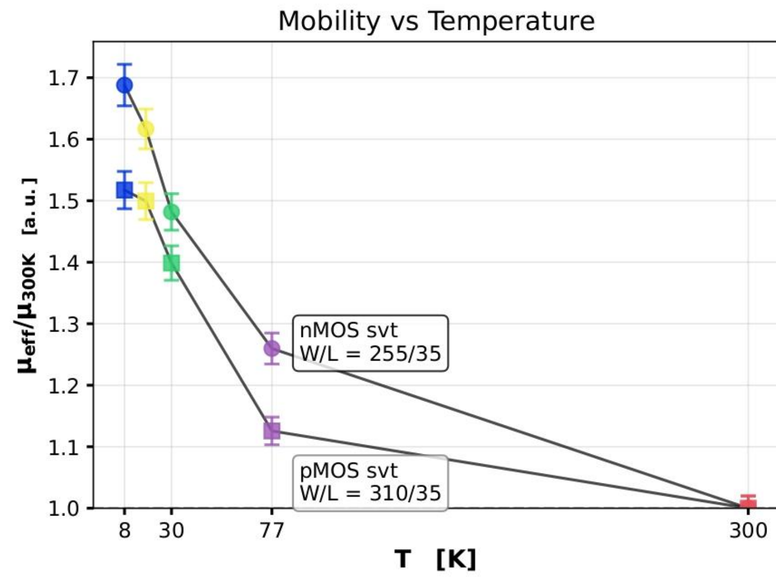
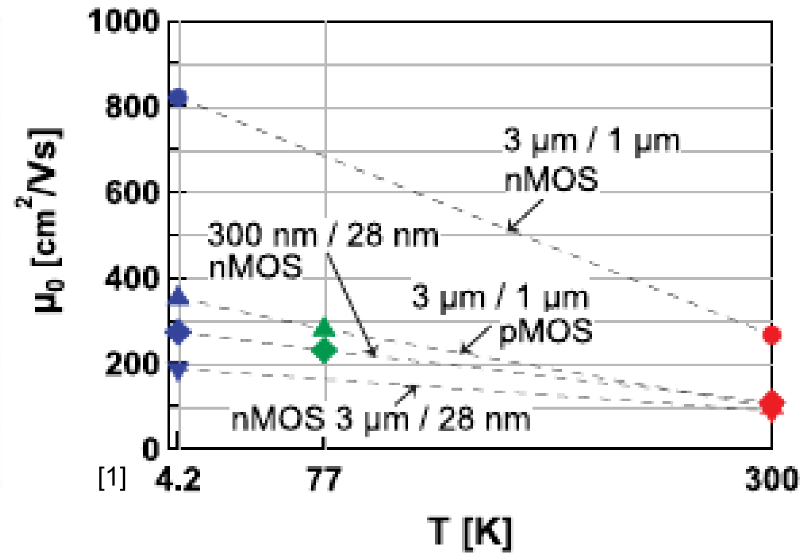
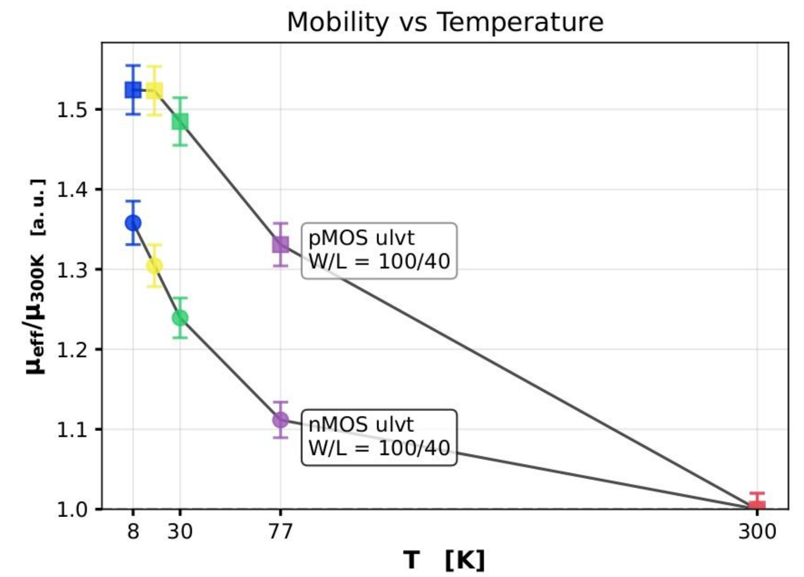
BACKUP - MOBILITIES







[1] “Characterization and Modeling of 28 nm Bulk CMOS Technology down to 4.2K” Beckers et al., 2018

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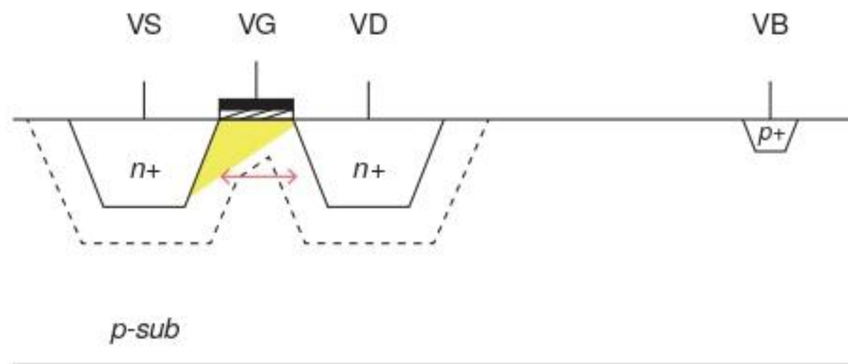
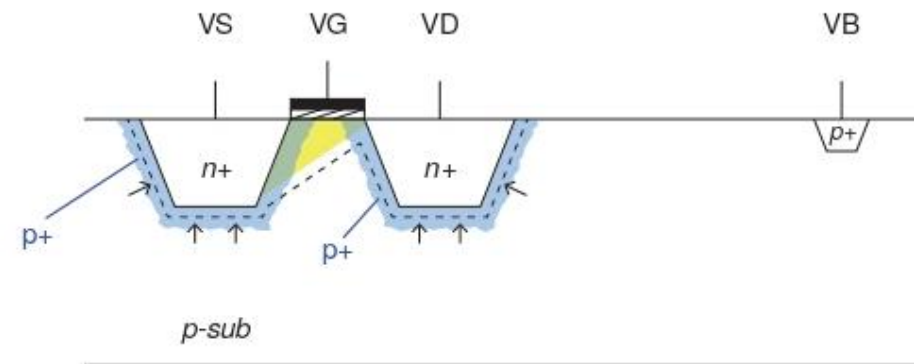
BACKUP – SHORT CHANNEL EFFECTS

Drain-induced barrier lowering



Halo dopings



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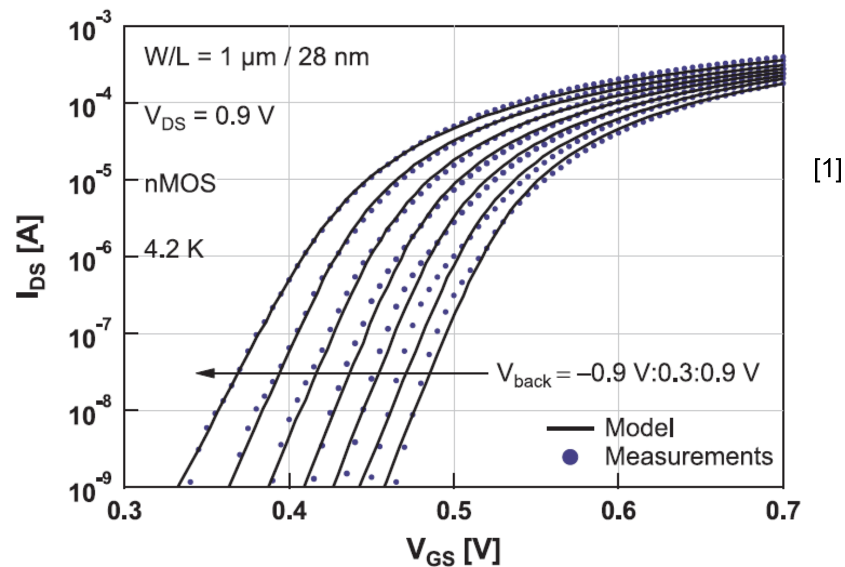
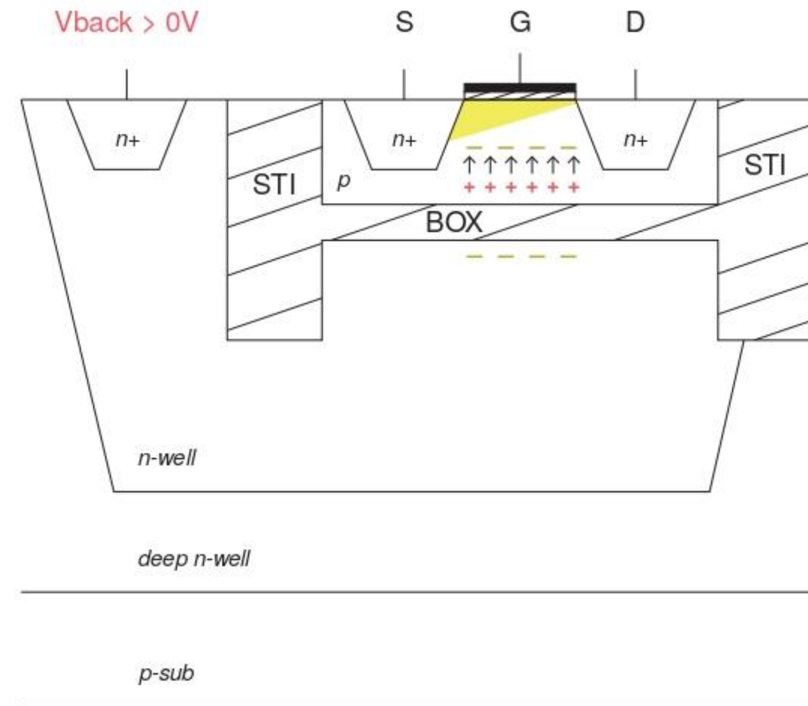
BACKUP - FD-SOI BACKGATE TUNING OF V_{th}

- Increase of V_{th} in cryo
- Adjusted with V_{back}
- One of the **advantages of SOI** for cryo ICs



[1]



[1] Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures, Beckers et al. 2019

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BACKUP - PMOS FBB

- **Only pMOS FBB because:**
  - Substrate in contact with the cold plate
  - CERN Chip: no triple well nMOS devices

Ag Glue

DUT Chip

Cu Alloy Cold Plate

- $V_{B,nMOS}$ ↑ → Ground Loop
- $V_{S,nMOS}$ ↓ → $V_S < V_{SS}$ -> ESD Diode on S

BACKUP – STATYSTICAL TESTING

svt pMOS W/L = 100/35, Levenberg Marquardt algorithm

χ^2	V_D (V)
$3.64 \cdot 10^2$	0.85
$6.64 \cdot 10^0$	0.68
$1.88 \cdot 10^1$	0.51
$1.60 \cdot 10^1$	0.34
$8.73 \cdot 10^0$	0.17
$1.41 \cdot 10^1$	0.0
χ^2_{crit}	$6.64 \cdot 10^1$

Table 4.13: $I_{DS} - V_{GS}$ chi squares at 8 K.

χ^2	V_G (V)
$1.98 \cdot 10^1$	0.0
$2.07 \cdot 10^1$	0.1
$1.56 \cdot 10^2$	0.2
$3.04 \cdot 10^1$	0.3
$2.36 \cdot 10^{-1}$	0.4
χ^2_{crit}	$1.24 \cdot 10^2$

Table 4.14: $I_{DS} - V_{DS}$ chi squares at 8 K.

- $\sigma = \max\{10\% \cdot I_{DS}\ ,\ 0.1\ \mu A\}$

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- $\sigma = \max\{10\% \cdot I_{DS} \ , \ 0.1\ \mu A\}$
- χ^2 not passed → model extension weakness in linear region

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Table 4.14: $I_{DS} - V_{DS}$ chi squares at 8 K.

- $\sigma = \max\{10\% \cdot I_{DS}\ ,\ 0.1\ \mu A\}$
- χ^2 passed, or barely not (low $|V_{DS}|$ regime)

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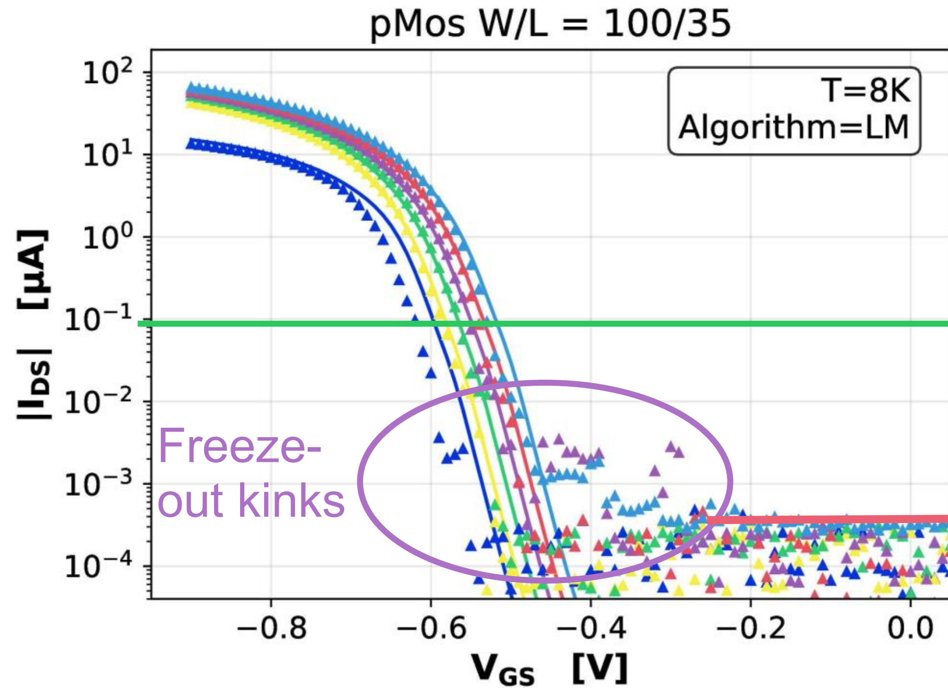
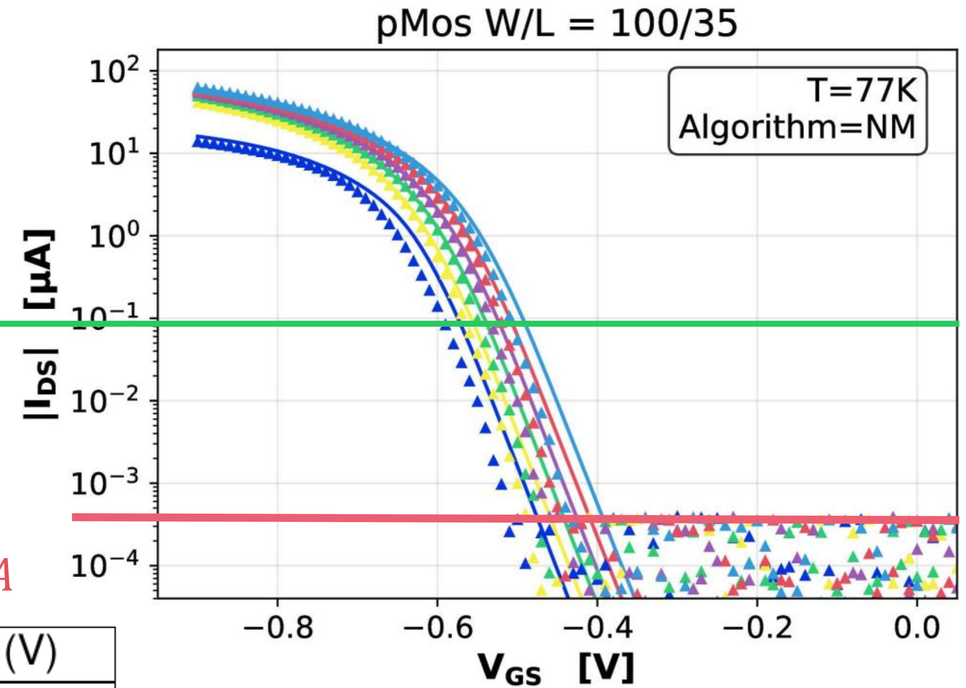
BACKUP – STATYSTICAL TESTING





Max noise levels
$\sim 3 \cdot 10^{-10} A$

χ^2	V_D (V)
$1.11 \cdot 10^4$	0.85
$1.42 \cdot 10^2$	0.28
$9.87 \cdot 10^1$	0.51
$2.24 \cdot 10^2$	0.34
$5.66 \cdot 10^2$	0.17
$1.26 \cdot 10^3$	0.0
χ^2_{crit}	$6.64 \cdot 10^1$

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BACKUP - ALGORITHMS COMPARISON

8K optimization 5 parameters

- **Same initial guess, same 5 pars**
- **Same target RMS → adherence sim-meas**

Levenberg-Marquardt

- Total time: **30.43 s**
- Function evals: 29
- Time per eval: 1.05 s
- Final cost: 9.4e-07 A^2
- Final RMS: 3.5e-05 A
- Quadratic

Faster but **more sensitive** to loc. min. and initial guess

Nelder-Mead

- Total time: **113.50 s**
- Function evals: 149
- Time per eval: 0.46 s
- Final cost: 9.4e-07 A^2
- Final RMS: 3.5e-05 A
- Linear

Less sensitive to loc. min. and initial guess but **slower**