XIDyn

High Flux, High Dynamic-range Hard X-ray detector full-reticle ASIC for 4th generation synchrotrons

Luke Mallett (RAL STFC)
On behalf of the XIDyn Collaboration

UKRI Science and Technology Facilities Council

UNIVERSITÄT HEIDELBERG
ZUKUNFT
SEIT 1386

diamond

ESRF
The European Synchrotron

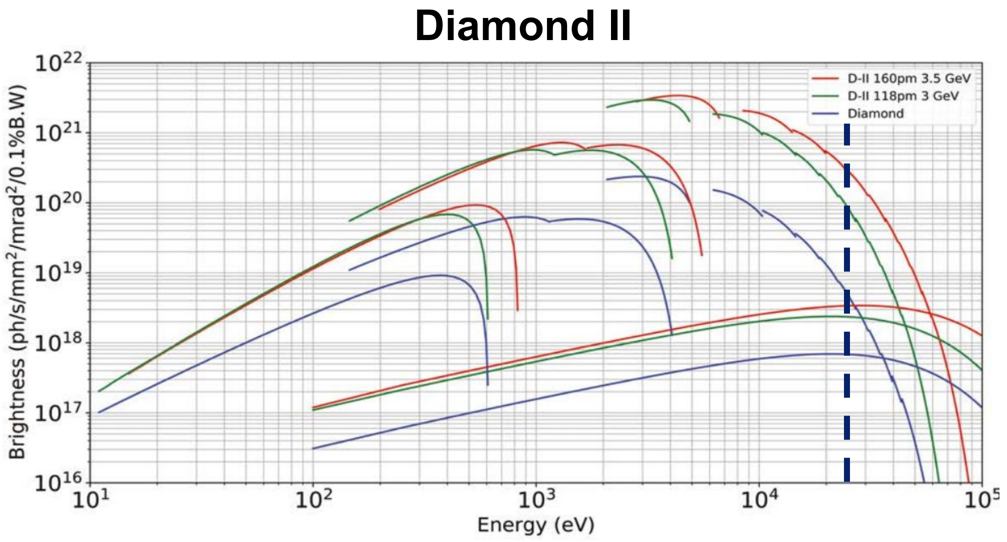
European XFEL

Introduction

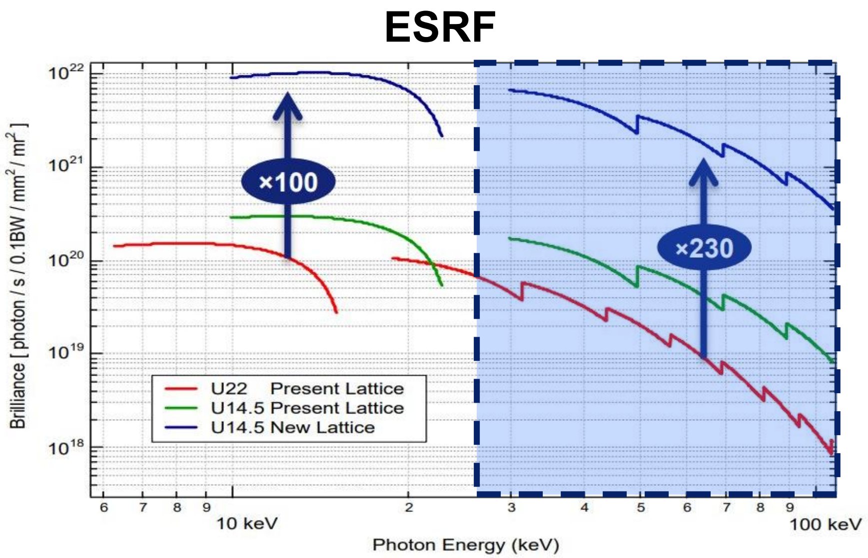
New generation of synchrotrons operate at significantly higher flux and higher energy photons

→ Faster high flux detector systems required

→ Must use higher Z materials (CZT)


Diamond II

Up to 10^{12} photons/s/mm^2


ESRF

Specification

Parameter	Continuous	Burst Timing
Operation	Constant with tolerable deadtimes	256 Frame capture and slower readout
Master Clock Frequency [MHz]	Up to 684.5	500
Energy Range [keV]	25keV typical	30-100keV
Resolution [photon]	0.25-1	1
Noise [e]	<1200 (1/4 photon)	<1200 (1/4 photon)
Flux [ph/pixel/s]	~10^{10}	-
Pixel Size [µm]	110	110
Frame Rate [kHz]	~10-150	5700 for 16 bunch mode
Instantaneous Flux [photons]	~100	~200
Power [W/cm^2]	5	5

Science and Technology Facilities Council

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

diamond

ESRF The European Synchrotron

European XFEL

Introduction

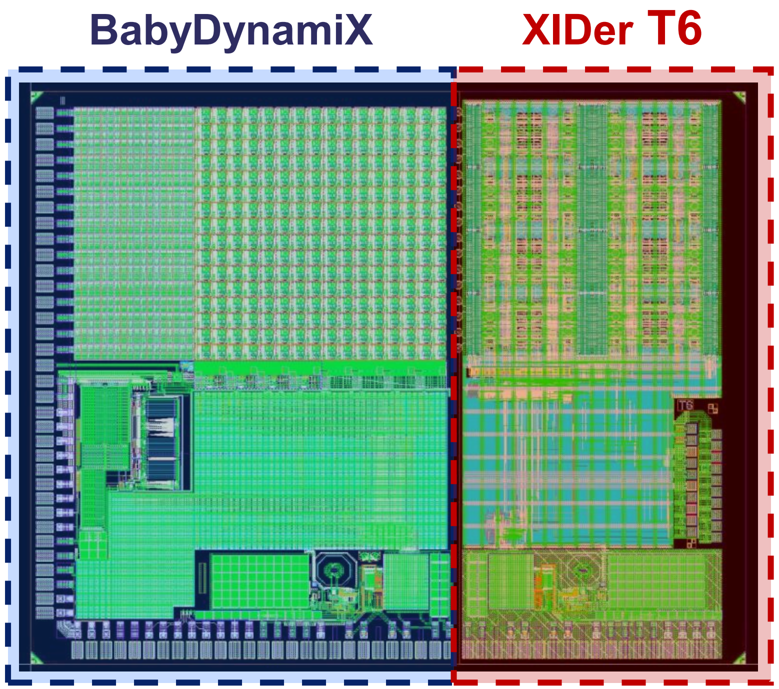
- Rutherford Appleton Laboratory developed DynamiX

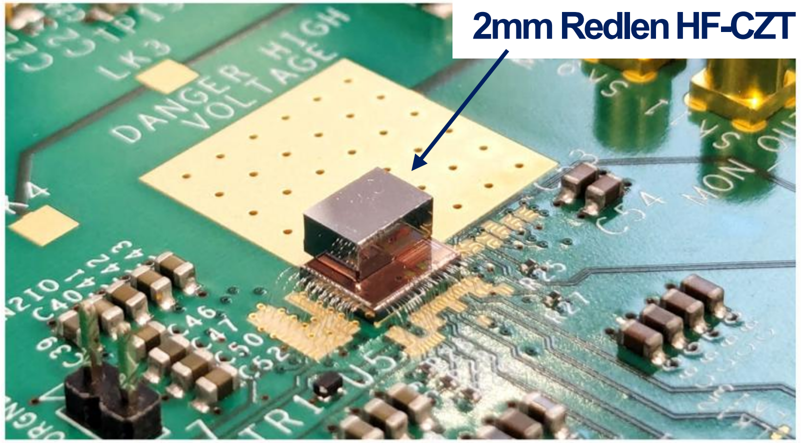
- University of Heidelberg developed XIDer

Both shown at FEE 2023

- Lots of similarities:
  - → 65nm process
  - → Hybrid design for CZT detector
  - → Aiming for 10^{10} photons/s/pixel
  - → 16x16 pixels

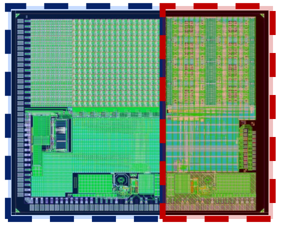
- Test structures shared an MPW

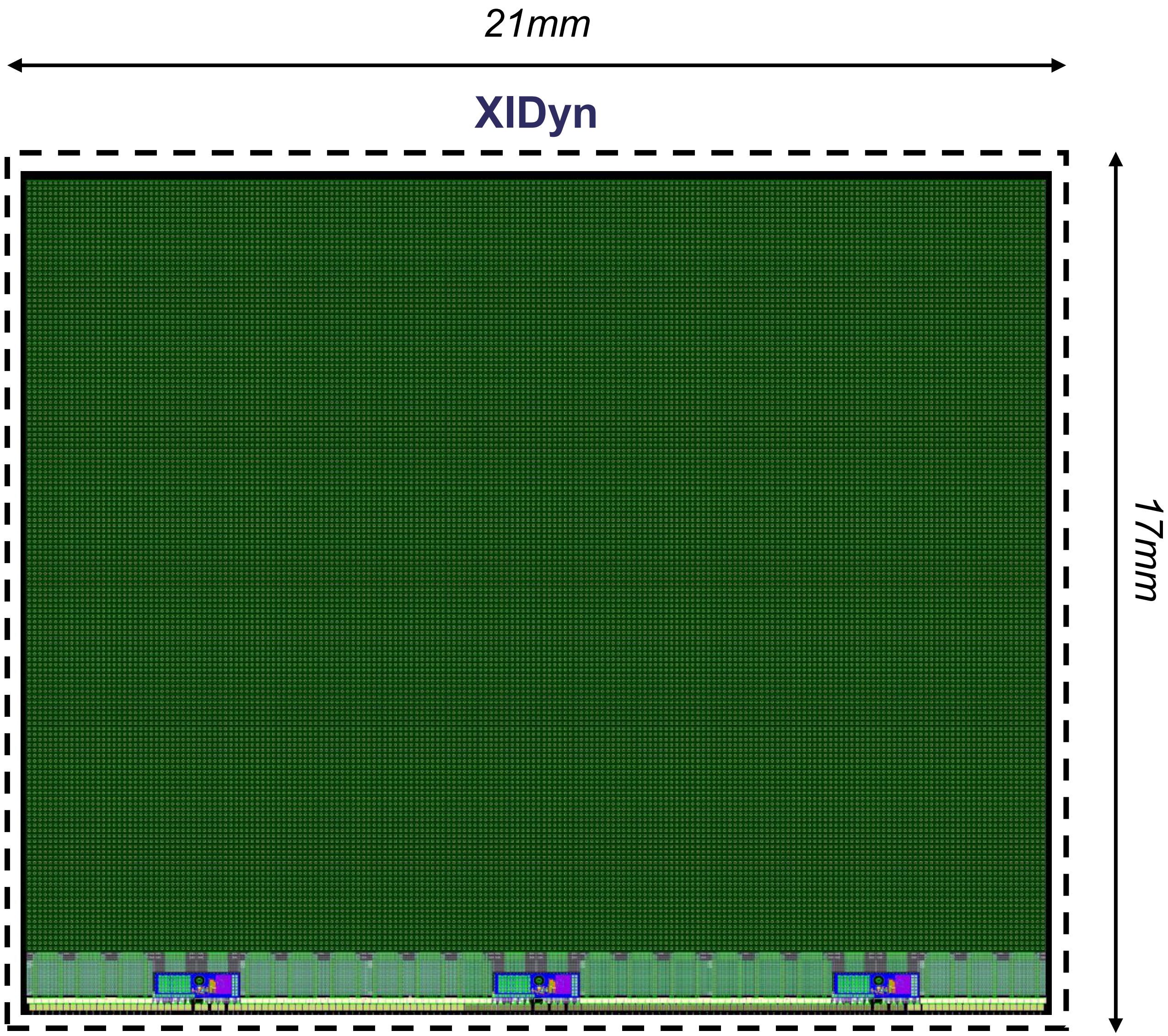




Introduction

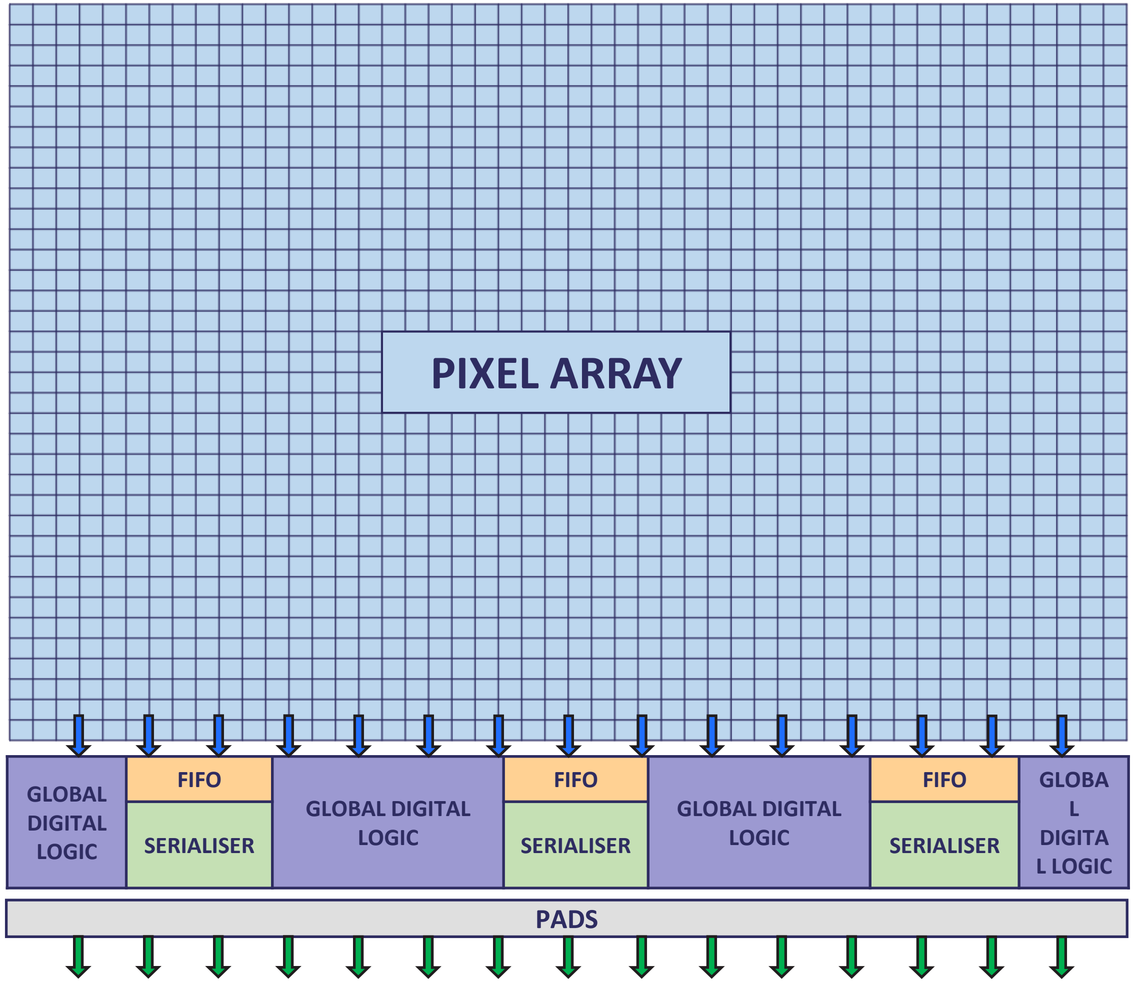
- Efforts combined to **XIDyn** (**XID**er + **Dyn**amiX)
- 192x144 pixels reticle scale ASIC
- Pads only on one edge for tiling
- Using RAM in pixel from XIDER
- Maximum of 20W



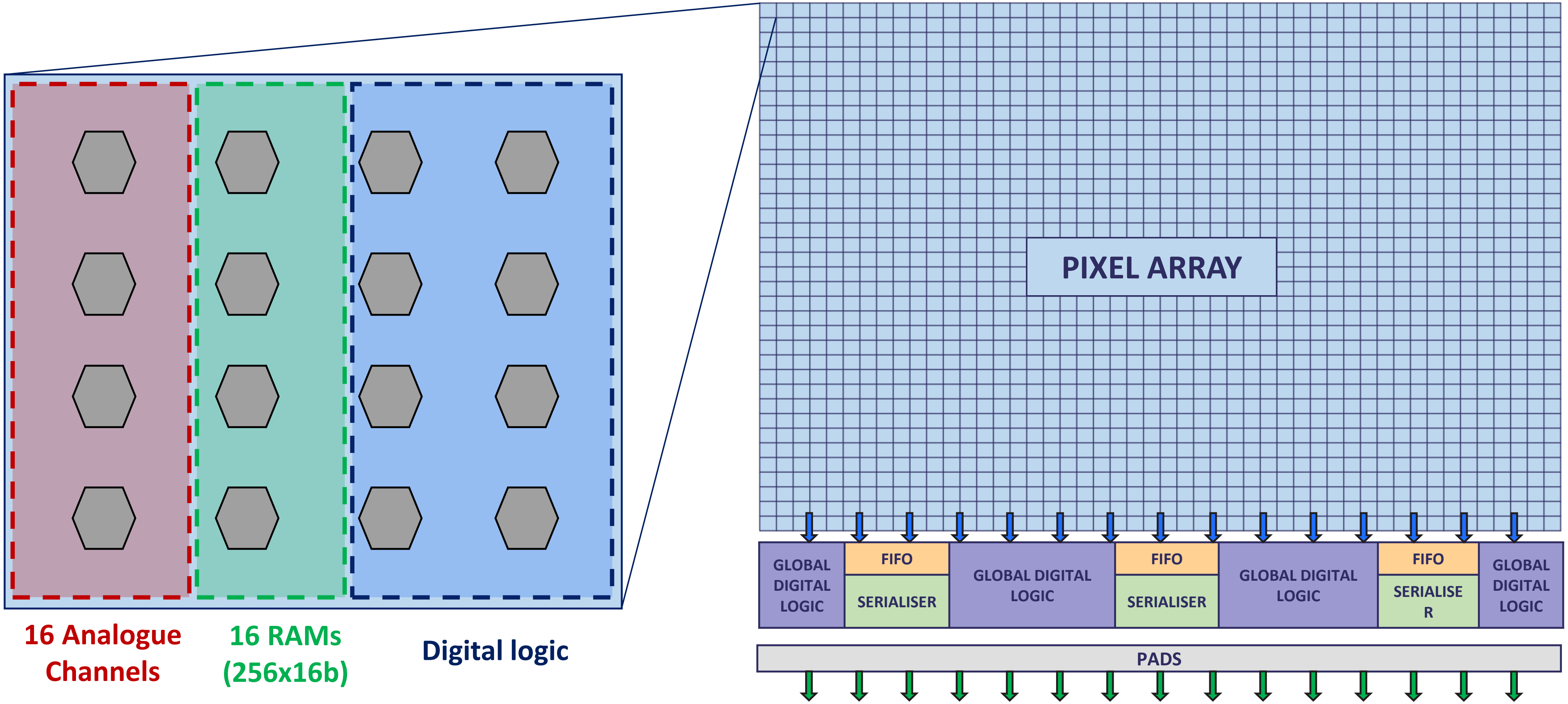


ASIC Architecture

- Large pixel array controlled by global digital logic
- 3 Dual lane 14.1Gbps serializers
- Using 4x4 super pixels
- Digital-on-top approach
- Design challenges:
  → IR drop up columns
  → Pixel mismatch



ASIC Architecture



16 Analogue Channels

16 RAMs (256x16b)

Digital logic

PIXEL ARRAY

GLOBAL DIGITAL LOGIC

FIFO

SERIALISER

GLOBAL DIGITAL LOGIC

FIFO

SERIALISER

GLOBAL DIGITAL LOGIC

FIFO

SERIALISER

GLOBAL DIGITAL LOGIC

PADS

Science and Technology Facilities Council

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

diamond

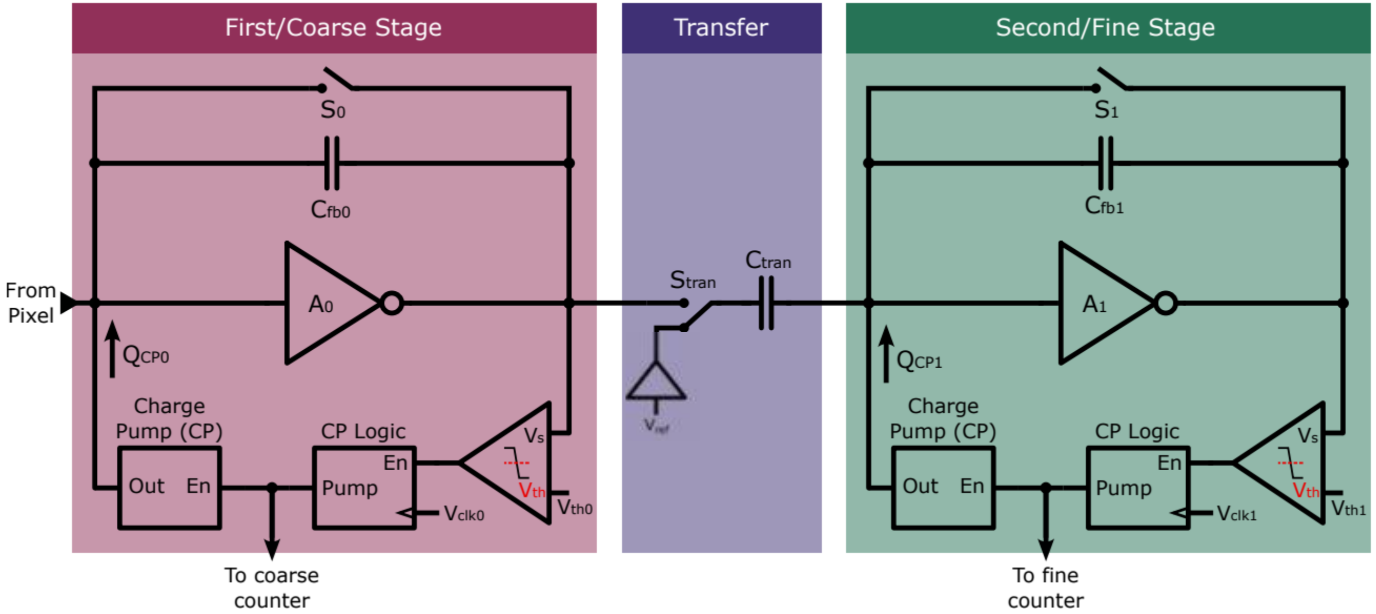
ESRF The European Synchrotron

European XFEL

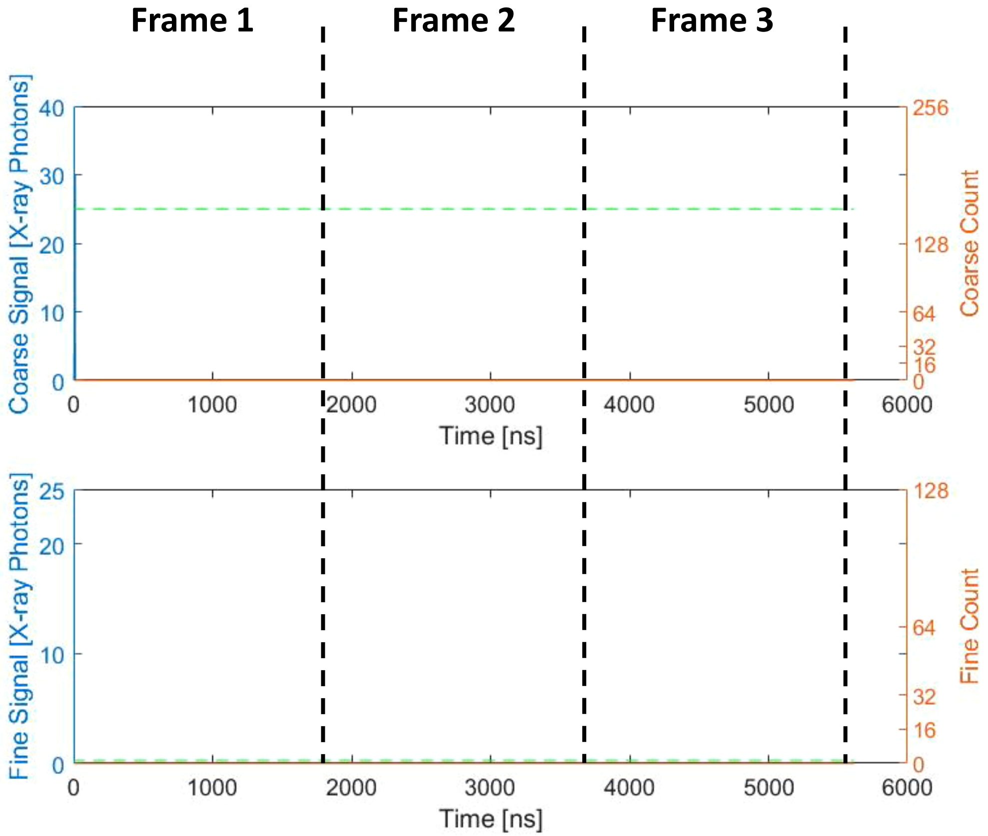
Analogue Channel

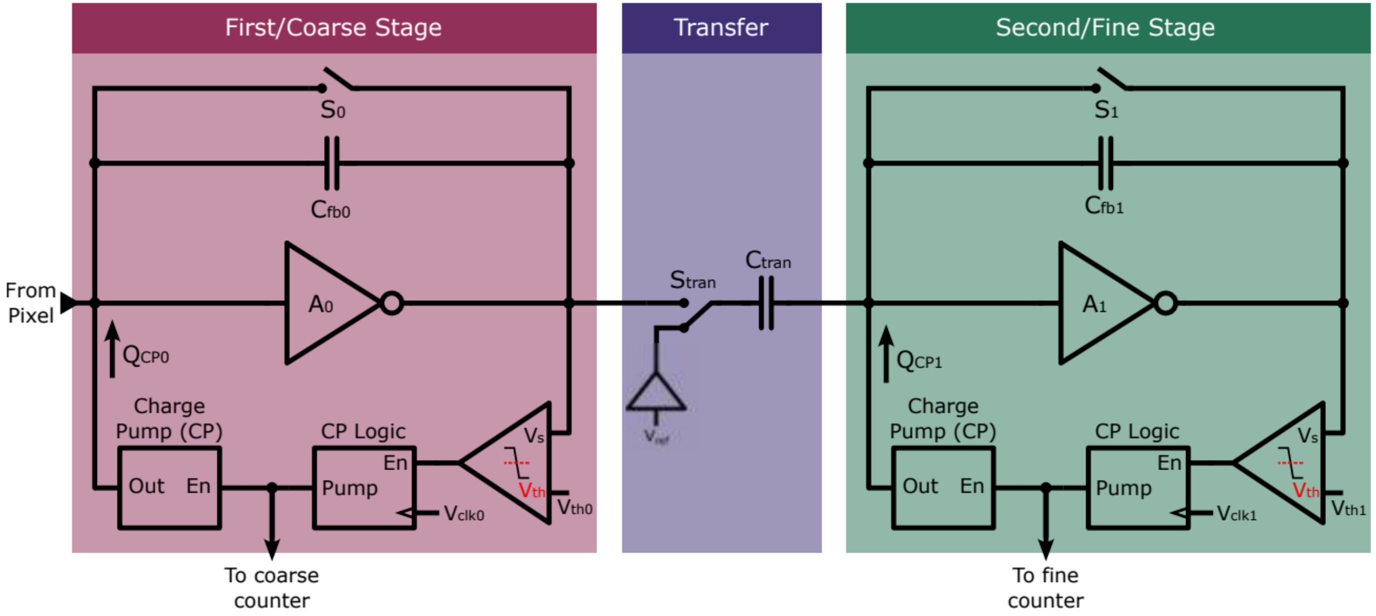
Charge cancellation

- Charge is integrated and removed when amount exceeds threshold
- Allows for constant charge removal from Cf to prevent saturation
- Removes charge in known packet sizes and directly provides digital output (no ADC)
- With the high flux, cannot achieve photon counting with a single stage

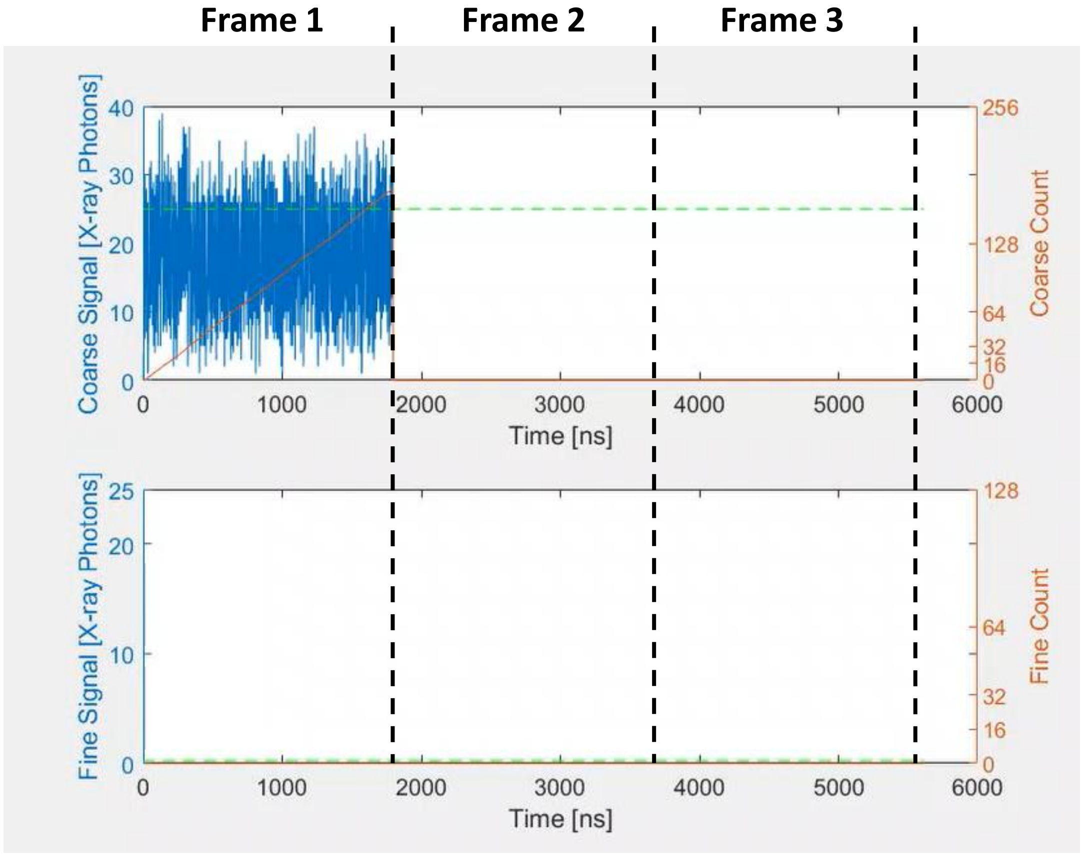


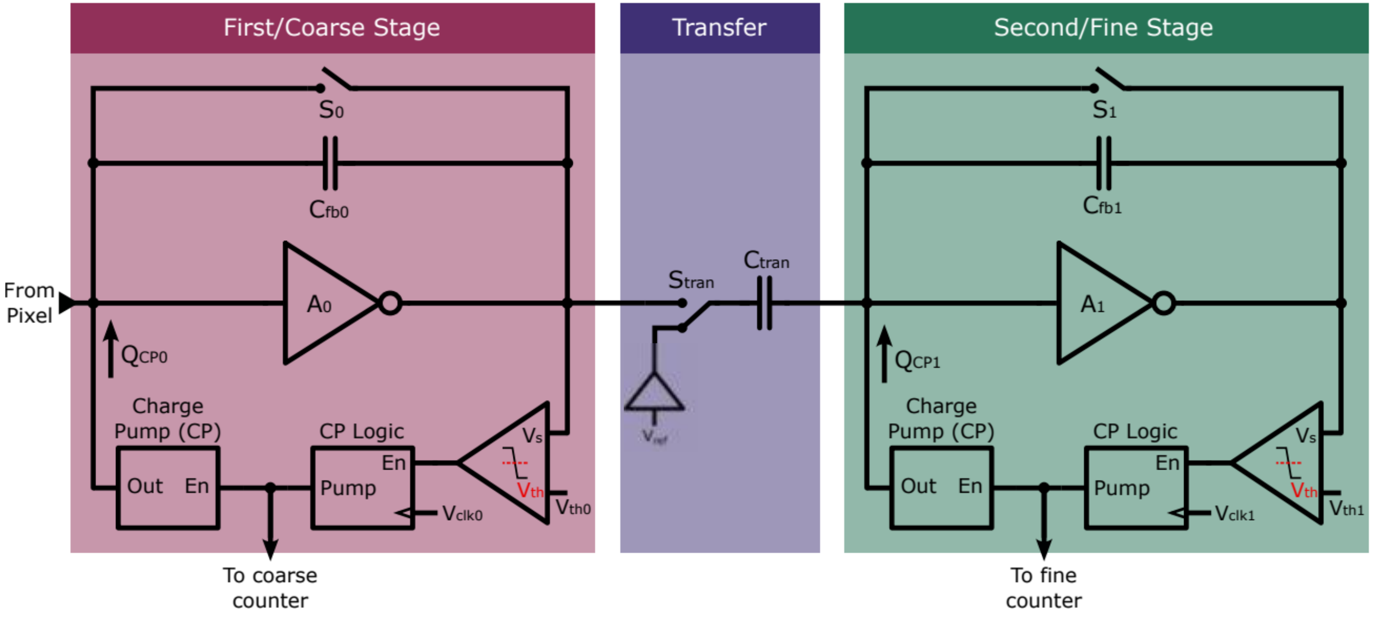
Analogue Channel





Analogue Channel





Science and Technology Facilities Council

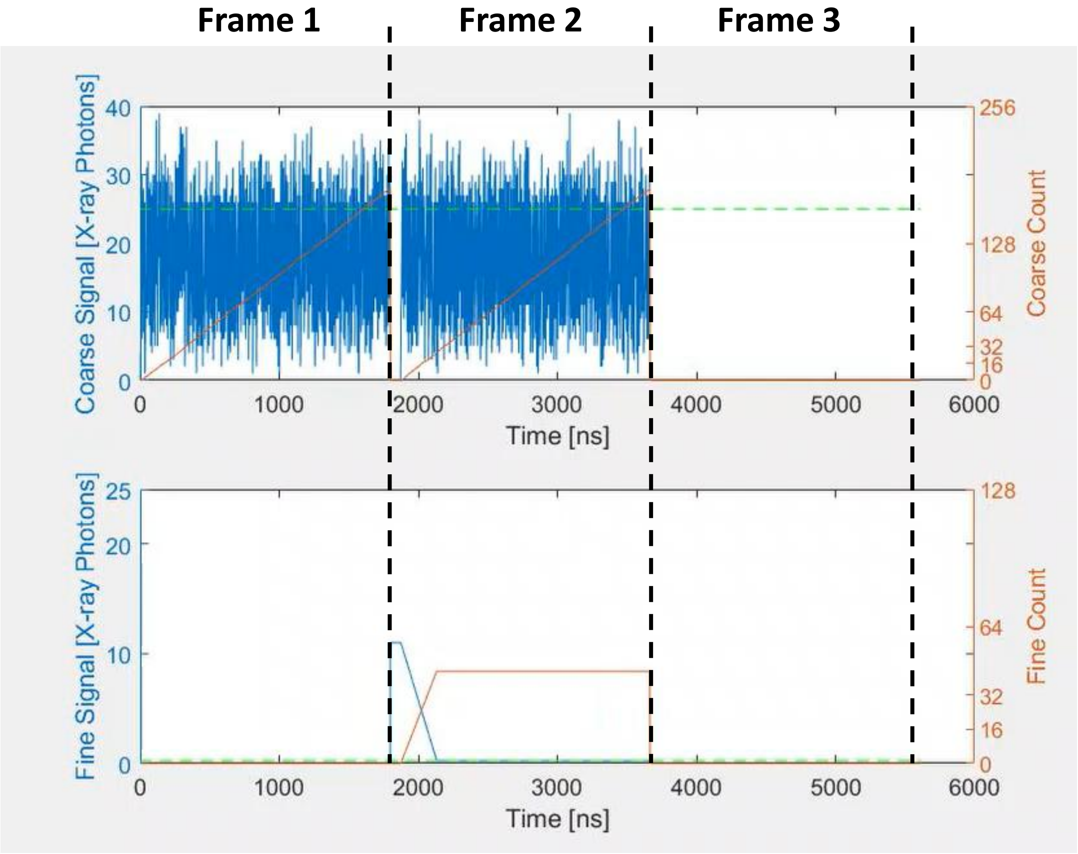
UNIVERSITÄT HEIDELBERG
ZUKUNFT SEIT 1386

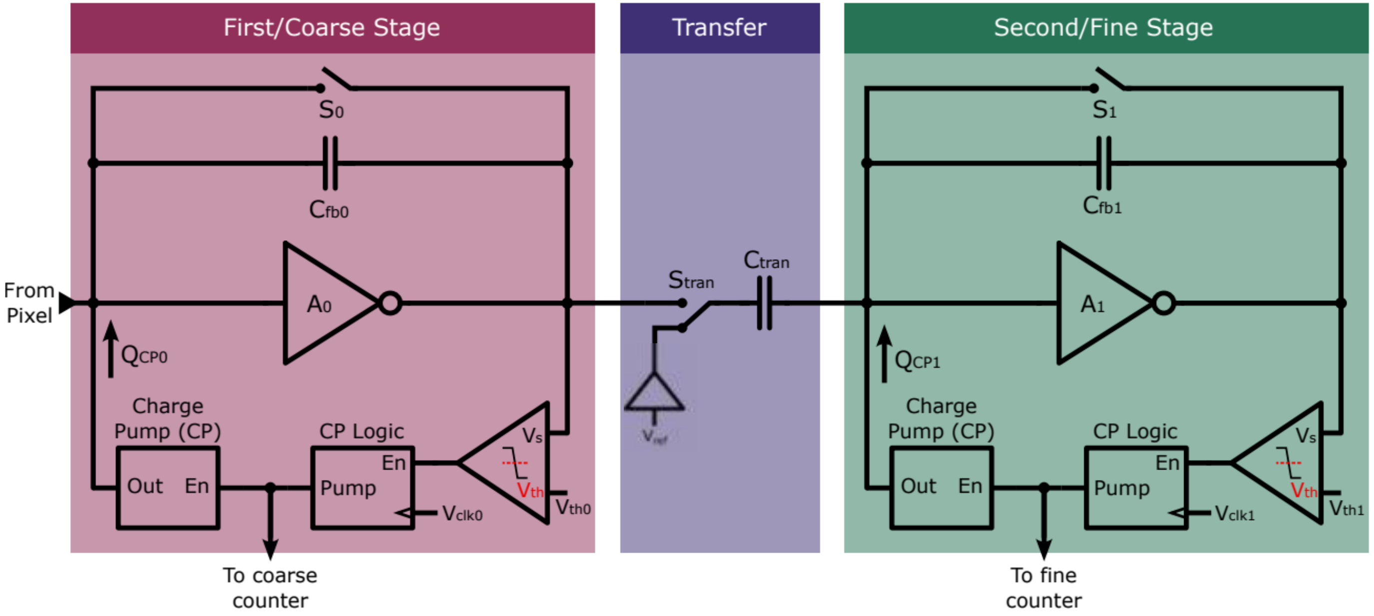
diamond

ESRF
The European Synchrotron

European XFEL

Analogue Channel





Science and Technology Facilities Council

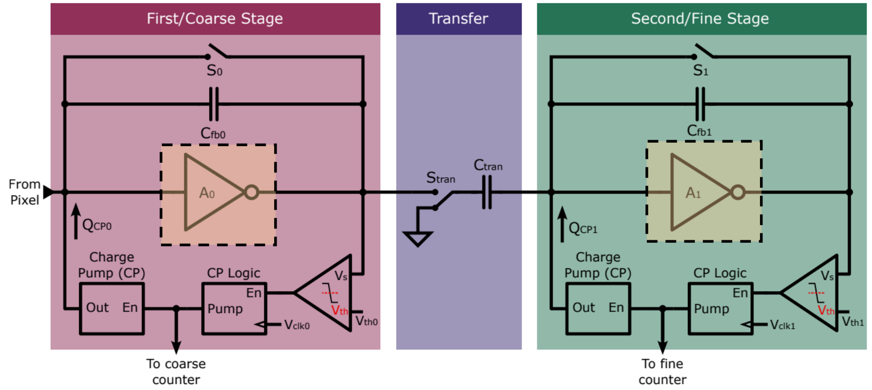
UNIVERSITÄT HEIDELBERG
ZUKUNFT SEIT 1386

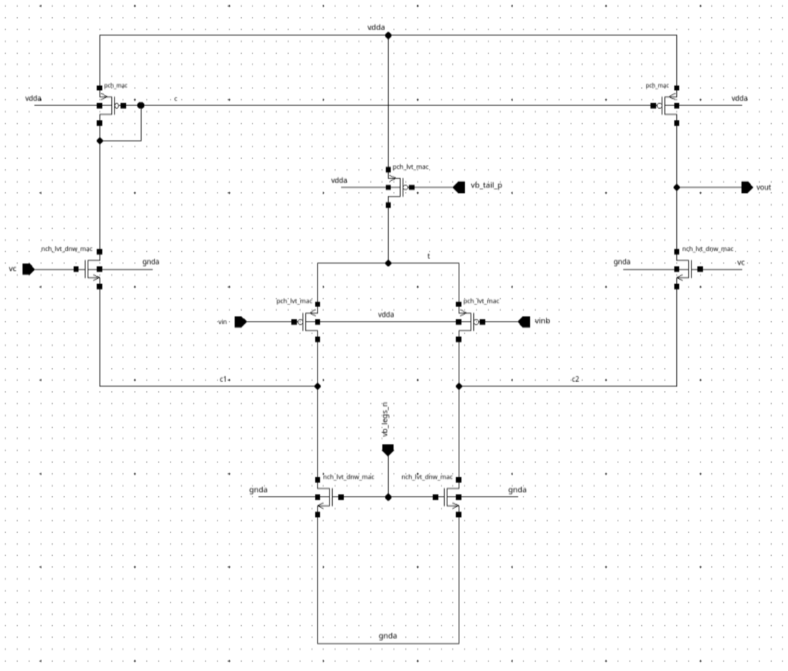
diamond

ESRF
The European Synchrotron

European XFEL

Analogue Channel

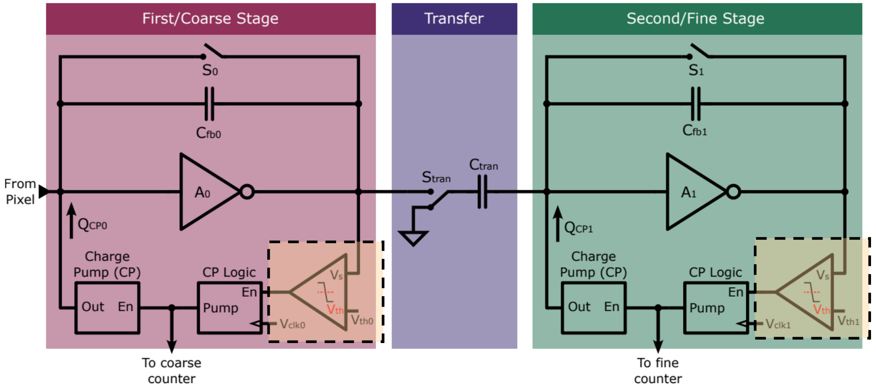




Amplifier

- Folded cascode design
  - → High open loop gain
  - → Fast response time
- Baseline voltage 400mV
  - → Generated at global level
- Coarse stage has 3x higher bias current and different transistor sizing
  - → Increased response time to handle larger charge

Analogue Channel

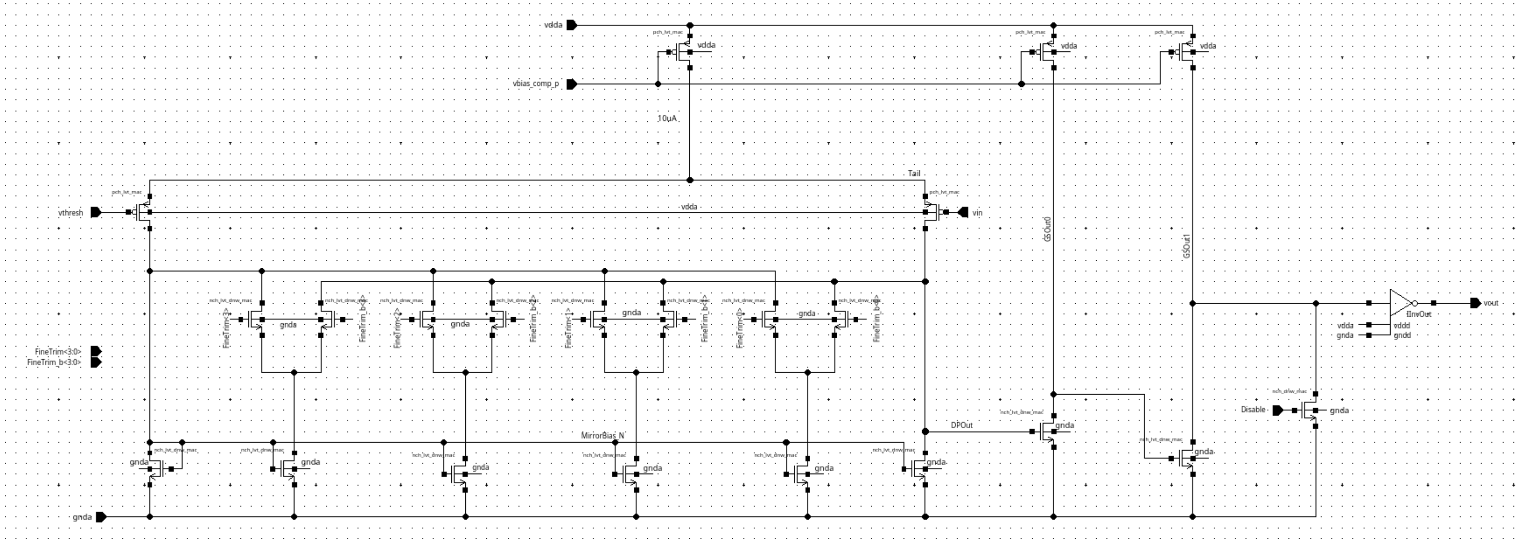


Comparator

- Differential pair with 2 gain stages
  - → Additional gain stage improves current balancing
  - → Improved response time

- 4-bit trim to minimise offset voltage

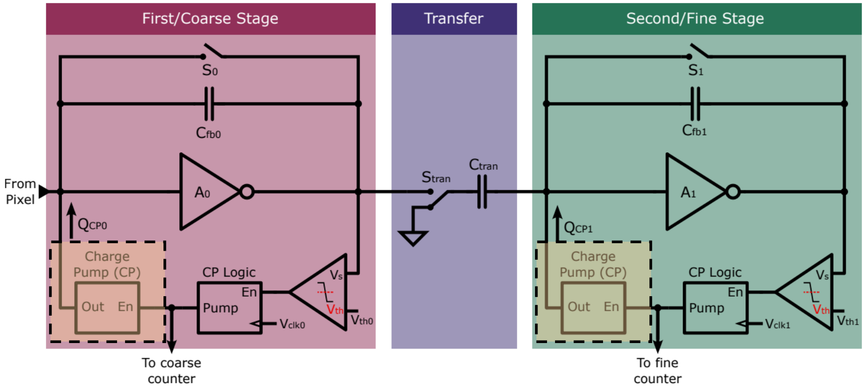
- Coarse comparator sized for improved speed

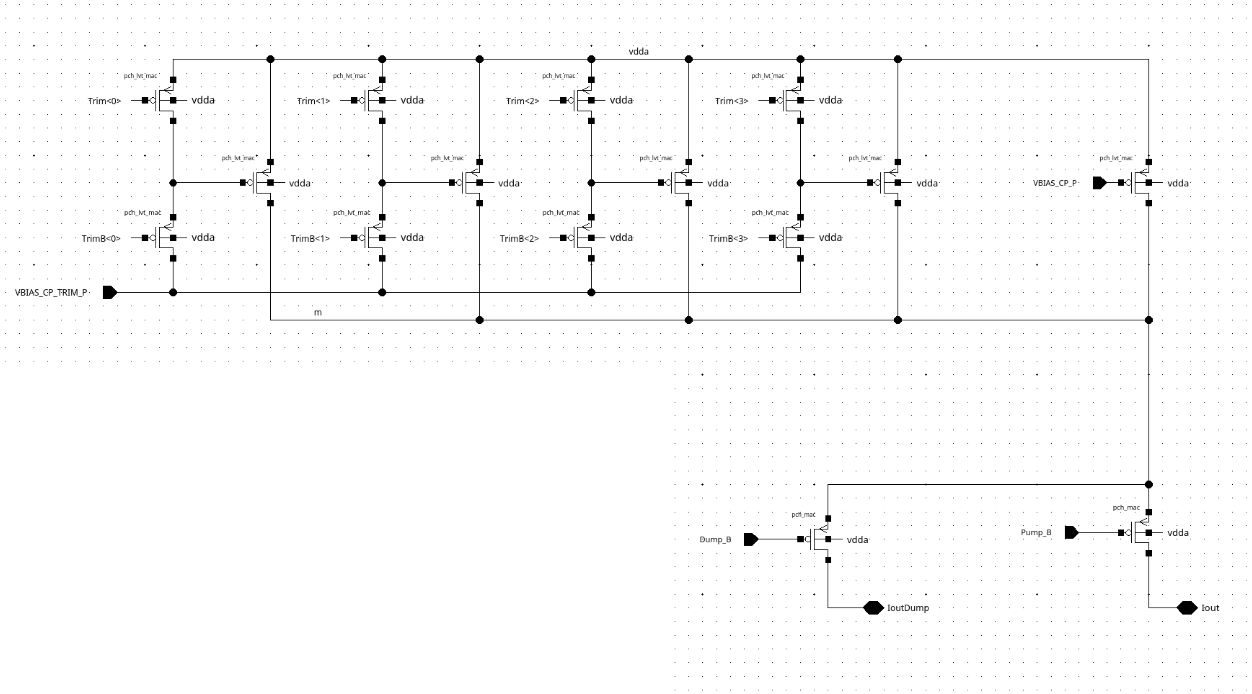


Analogue Channel

Charge pump

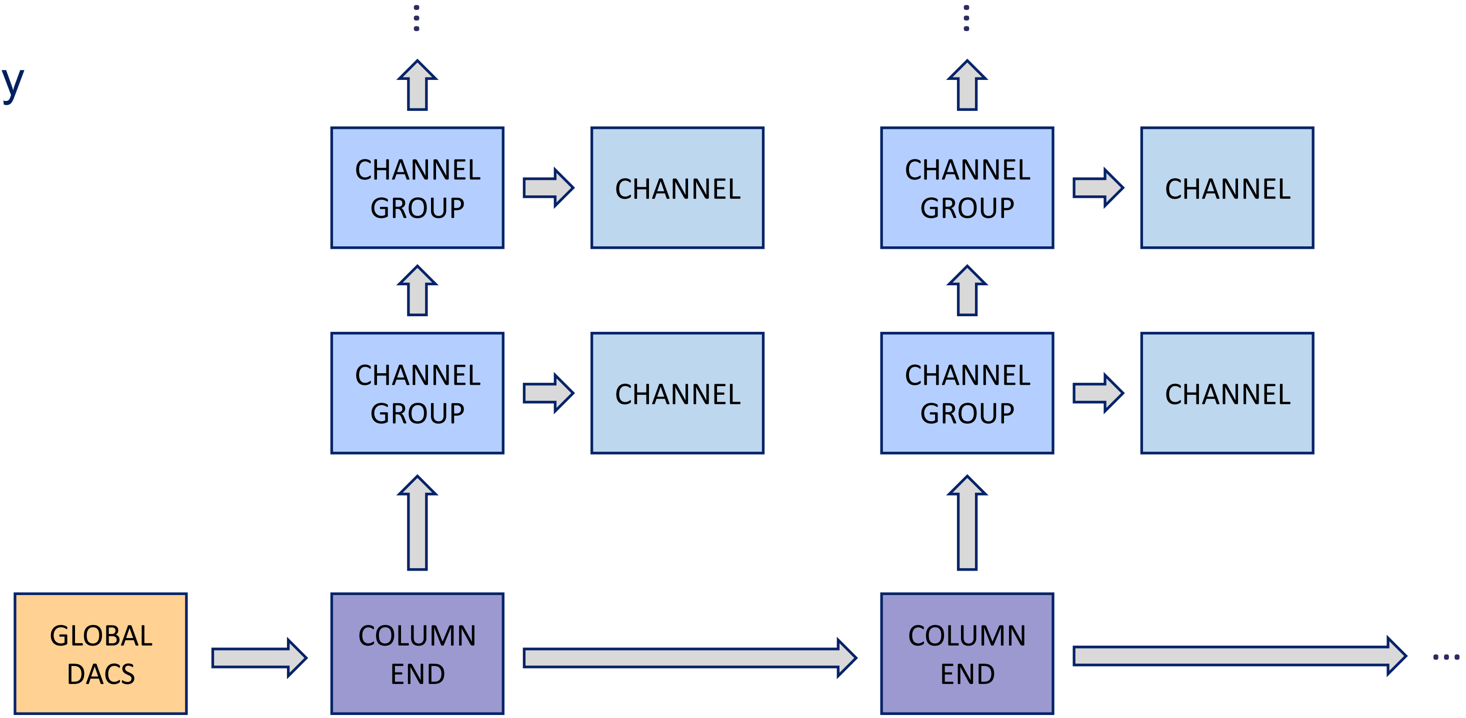
- Bias voltages set globally
  - → Calibrated to match number of photons
- 4-bit trim on pump current
  - → Trim circuit uses separate bias for increased flexibility
- Maximum cancellation in course stage is 48 ph @ 25keV





Pixel biasing

- Bias voltages generated from DACs globally then buffered to channels
  - → DAC codes set via JTAG
  - → Set in initial calibration
- Generated from 1mA current bandgap



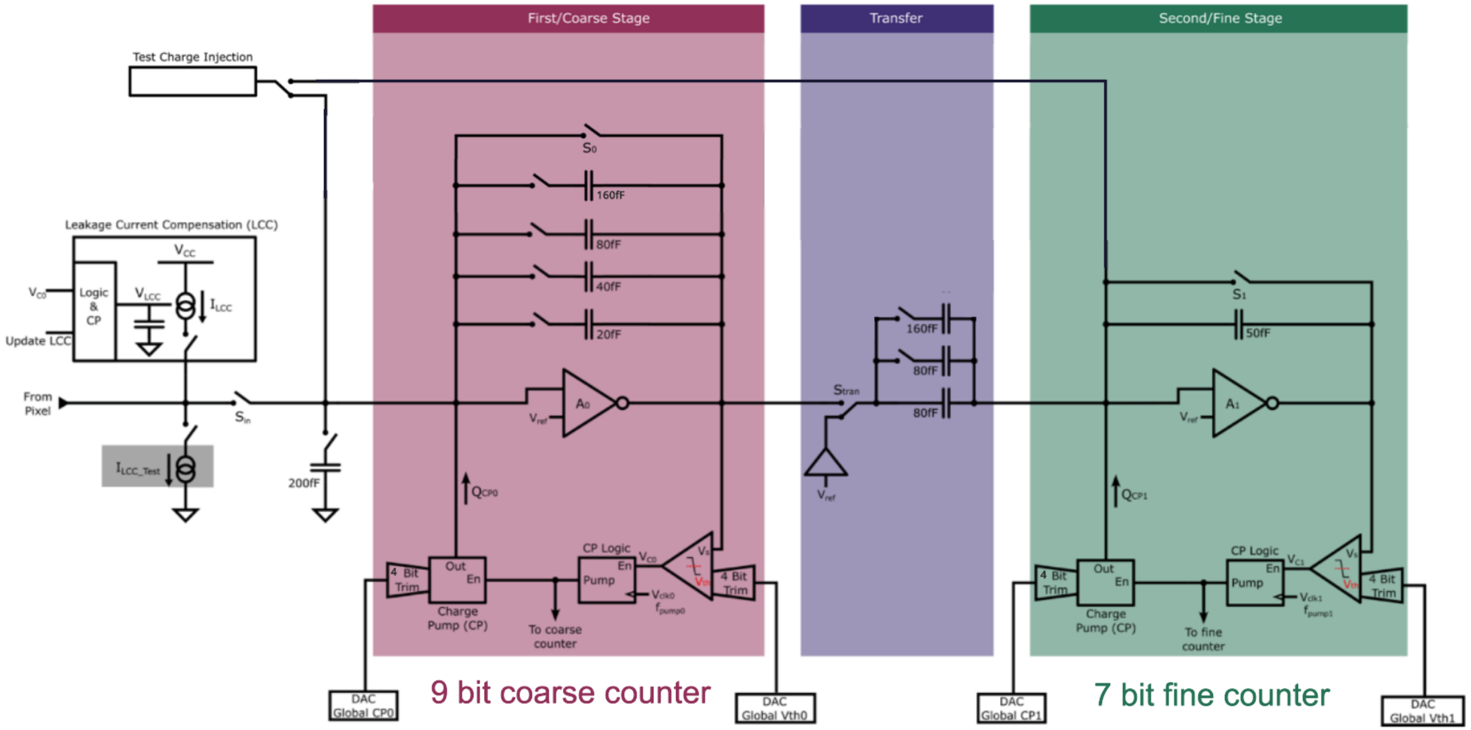
Analogue Channel

Configurable capacitance

- Array of capacitors to suit operating mode
  - → Coarse Cf: 20 – 300 fF
  - → Transfer C: 80 - 320 fF
  - → Fine Cf: Fixed 50 fF

Power consumption

- Each analogue channel consumes 220uA
  - → 264 uW per channel
  - → 7.3 W total

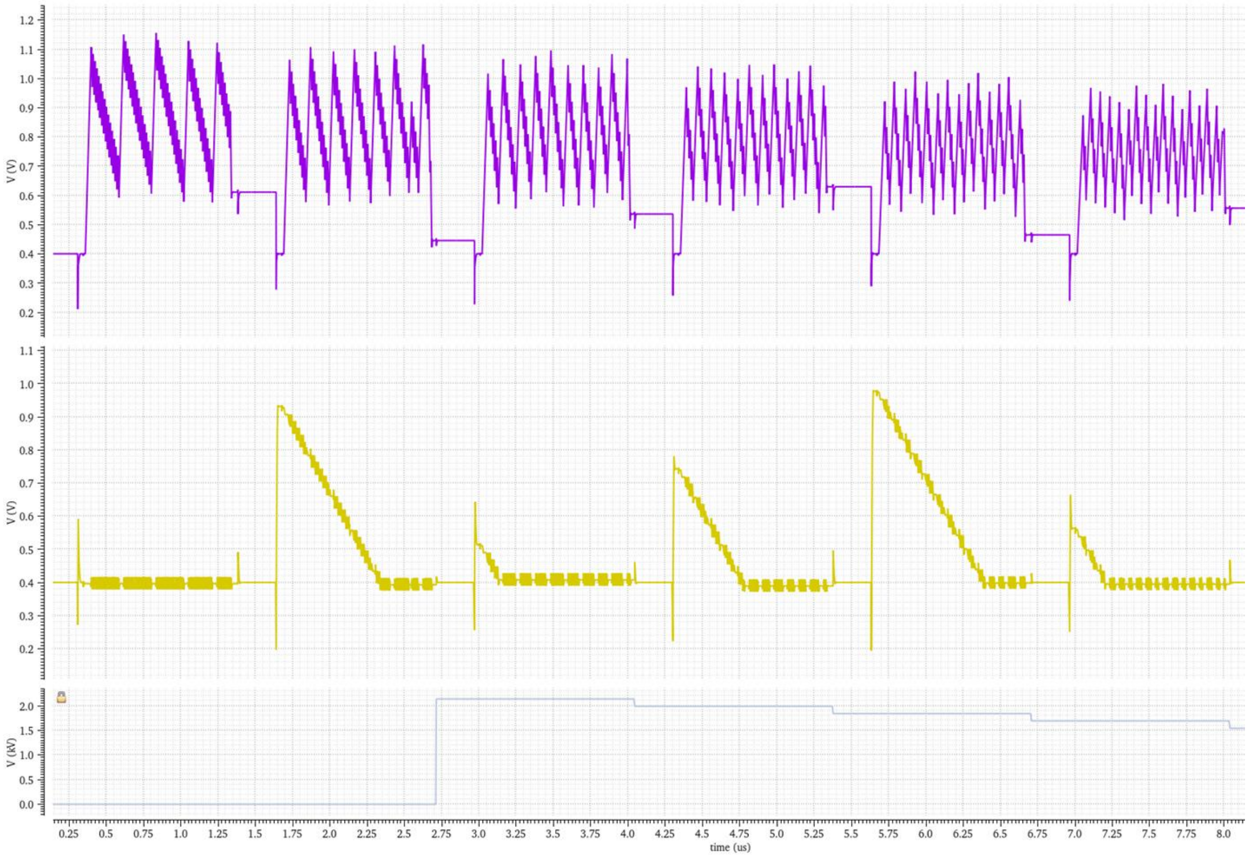


Analogue Channel

Coarse CSA output

Fine CSA output

Combined count

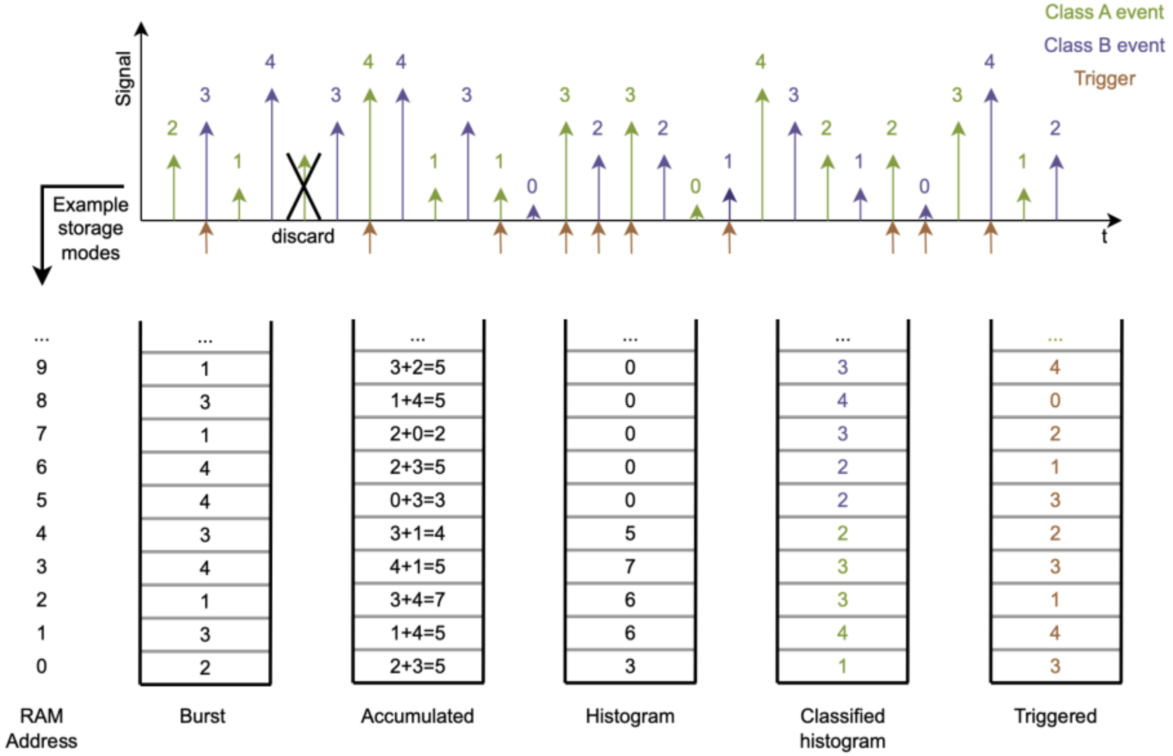


In-pixel RAM

- Each pixel has a 256x16bit RAM
  - → Uses foundry provided 6T SRAM bit cell
  - → Full custom periphery

- Enables increased functionality:
  - → Storing count values
  - → Accumulating values across frames
  - → Histograms

- Estimated RAM will contribute ~60% of digital power for the pixel
  - → 16-bit register available to bypass RAM

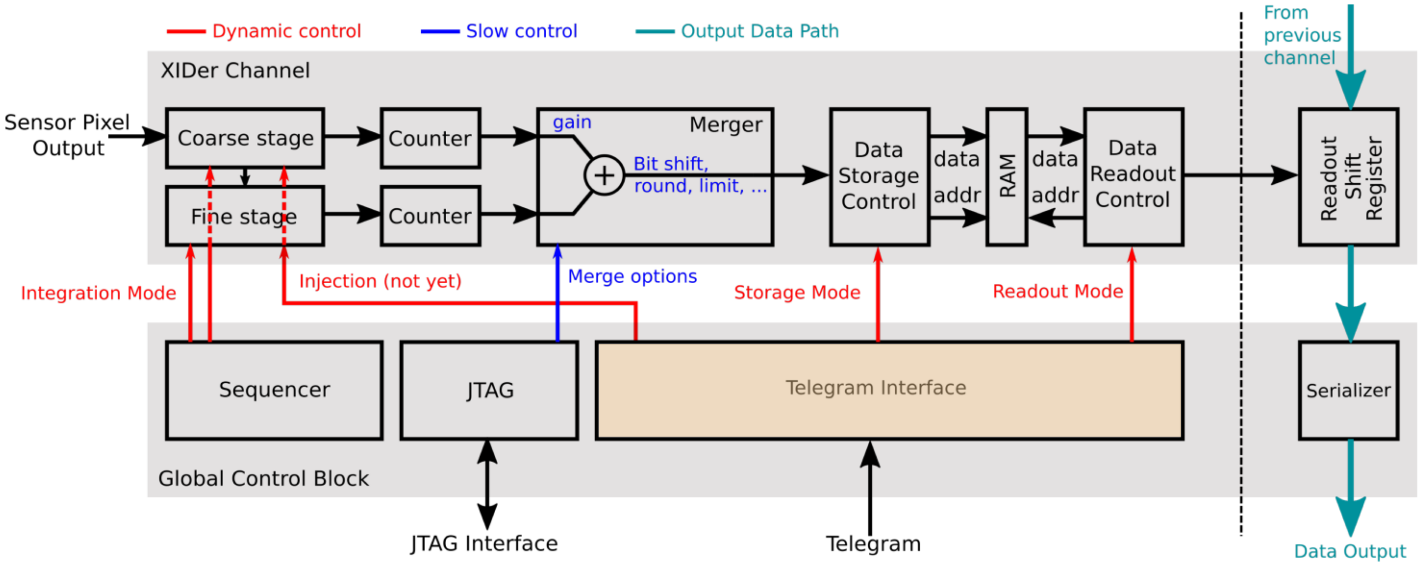


RAM Address	Burst	Accumulated	Histogram	Classified histogram	Triggered
...	...	...	...	...	...
9	1	3+2=5	0	3	4
8	3	1+4=5	0	4	0
7	1	2+0=2	0	3	2
6	4	2+3=5	0	2	1
5	4	0+3=3	0	2	3
4	3	3+1=4	5	2	2
3	4	4+1=5	7	3	3
2	1	3+4=7	6	3	1
1	3	1+4=5	6	4	4
0	2	2+3=5	3	1	3

Digital Control

Telegram

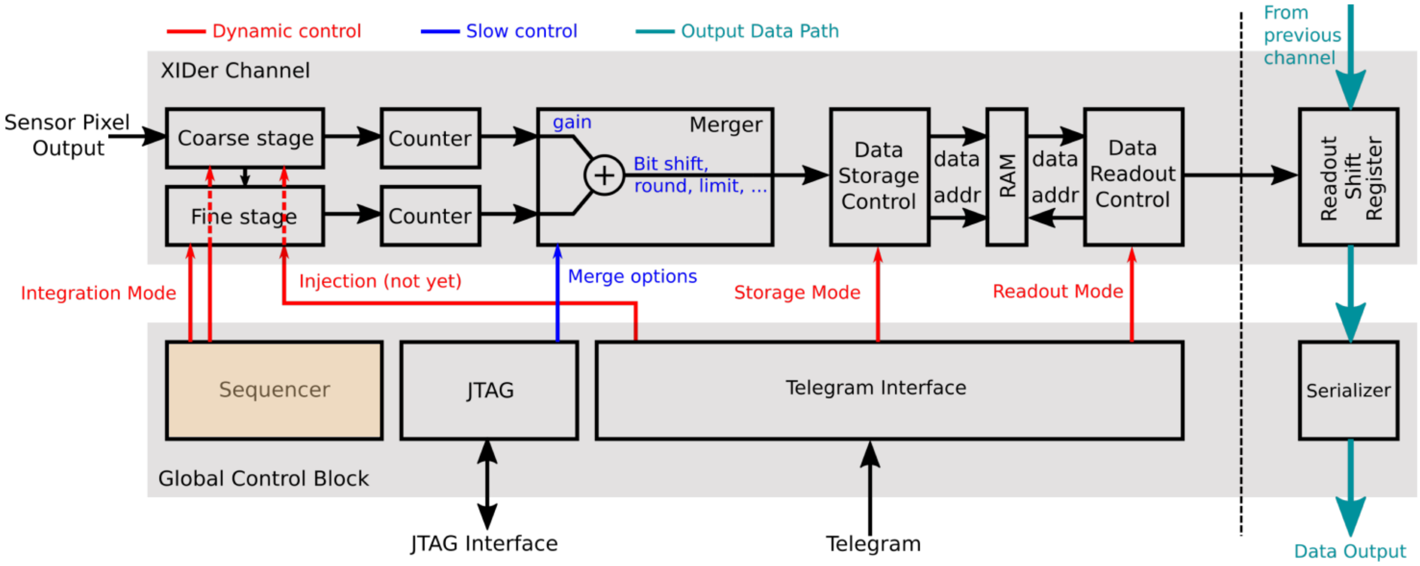
- Operational commands sent through the external Telegram Interface on the fly
  - → Determines what is done with the pixel value
  - → Begins readout from pixels
- Simple commands can be generated on-chip
- Telegram encoded in 8b10b
- Clocked at 68.45 MHz and synchronised to external interface



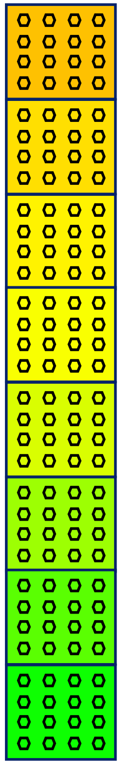
Digital Control

Sequencer

- Dynamic digital control signals generated by Sequencer on chip
  - → Configured through JTAG at start up
- Controls:
  - → Reset
  - → Charge pump enable
  - → Charge transfer from Coarse to Fine
- Clocked at 684.5 MHz and synchronised to start of Telegram Commands



Long column mitigations



- Maximised power tracks up columns for minimal IR drop (on M9 and M8)

- Mirroring bias currents and buffer voltages per column

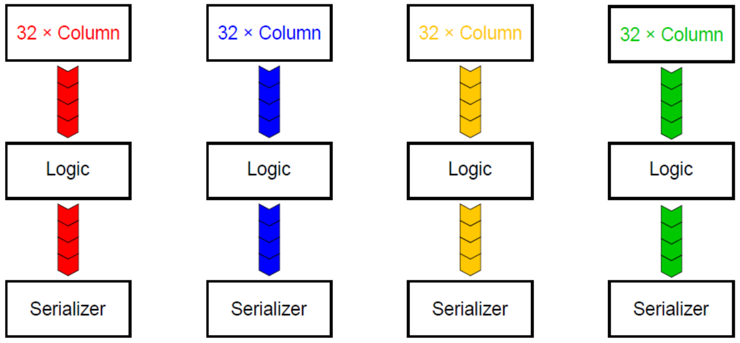
- Channel simulated at 0.96 V for IR drop
  → Accounting for a 120 mV drop along VDD and GND tracks

- Sequencer signals generated per two columns to meet timing

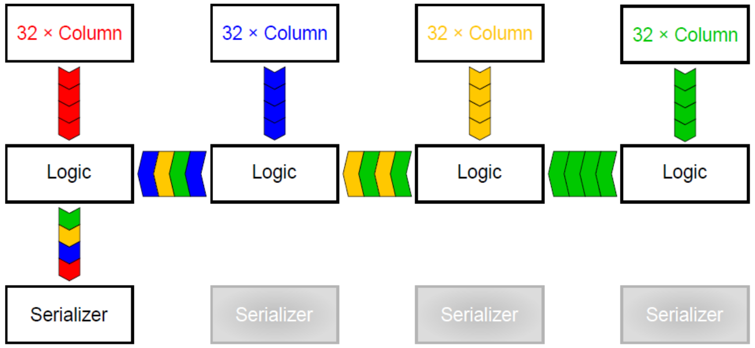
- *Top pixels can be turned off*

Readout

- Pixel values are shifted down columns into global logic at the bottom
- Option for 2x2 pixel binning
- Readout has up to 6 14.1Gbps serializer links available
  - → Used on previous test structures
  - → Can operate with 1, 2, 3, or 6 active



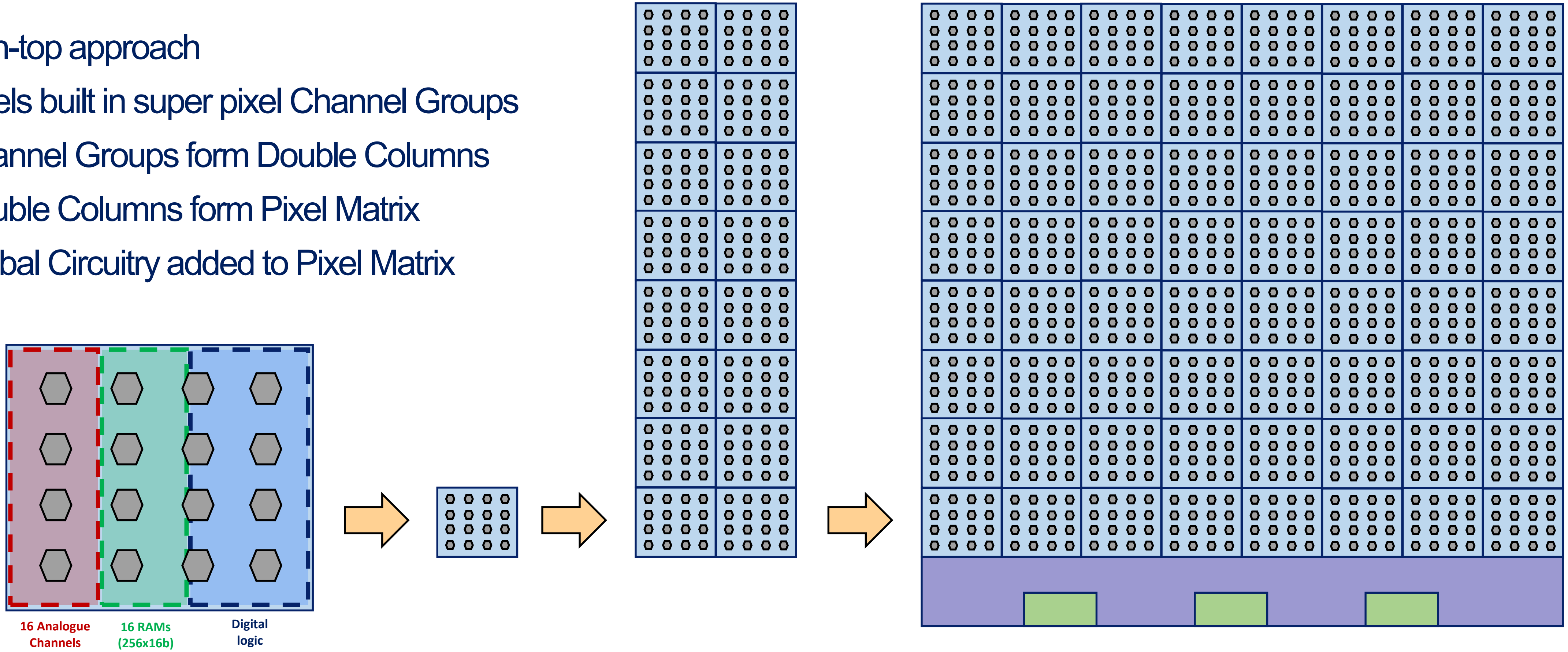
All serializers active



Left-most serializer active

Design flow

- Digital-on-top approach
  - → Pixels built in super pixel Channel Groups
  - → Channel Groups form Double Columns
  - → Double Columns form Pixel Matrix
  - → Global Circuitry added to Pixel Matrix



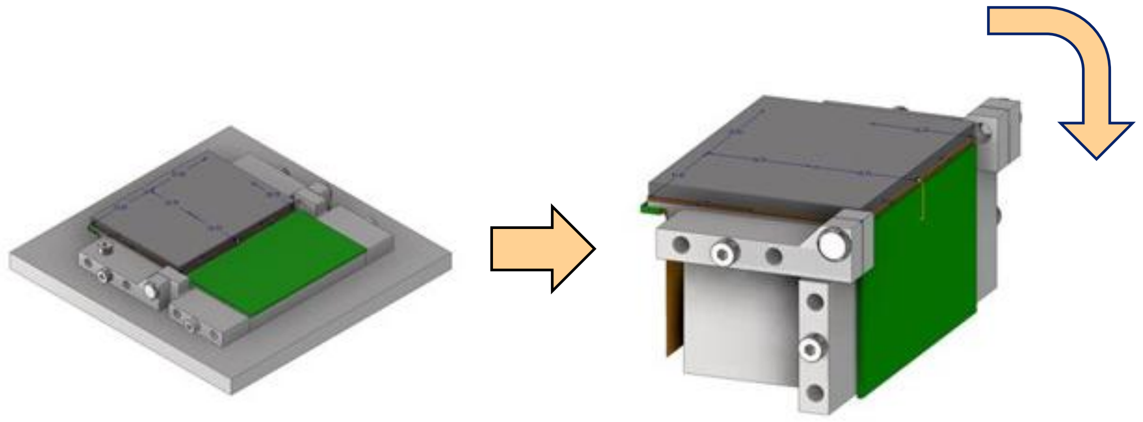
Detector System

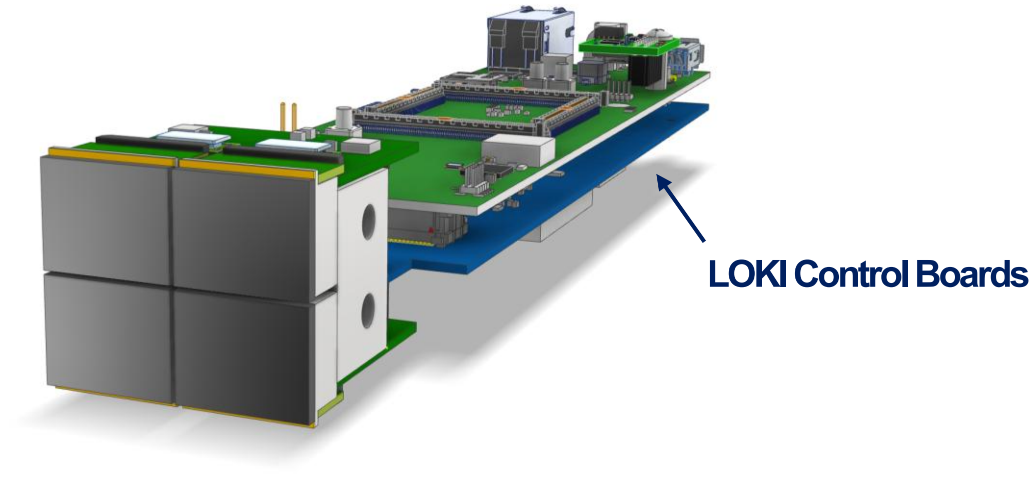
- CZT detector bump bonded onto ASIC

- Ribbon bonds to connect to PCB
  - → PCB folded underneath ASIC using jig

- Full detector system will tile 4 ASICs together
  - → Expected to reach 85-90% fill of image area

- Utilising existing STFC LOKI control boards



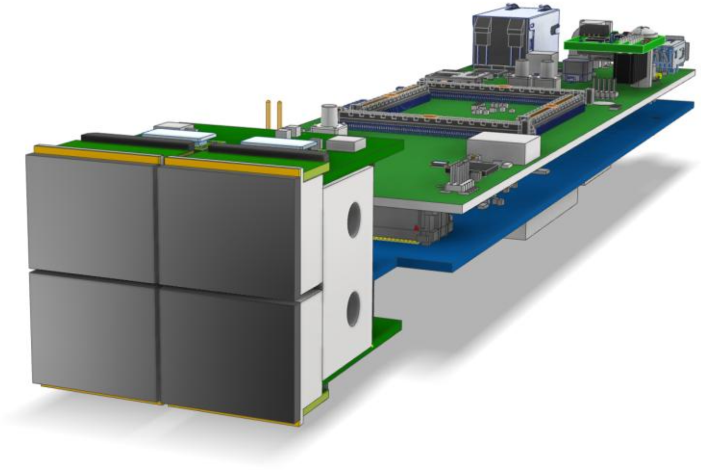


Summary

- Tape-out scheduled for end of June 2026
  - → Initial X-ray tests scheduled for Winter 2026
  - → Beamtime characterisation to follow

- Test detector system in development with plans to scale up to Quad and 1 MP systems

- Calibration
  - → Laser drilled tungsten mask
  - → Software method removing charge sharing events



Science and Technology Facilities Council

UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

diamond

ESRF The European Synchrotron

European XFEL

Science and
Technology
Facilities Council

Questions?

Science and
Technology
Facilities Council

Thank you

f Science and Technology Facilities Council

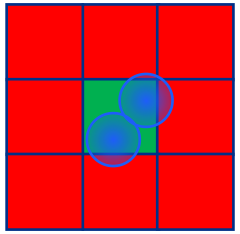
@STFC_matters

▶ Science and Technology Facilities Council

Backup

Simple Software Extraction

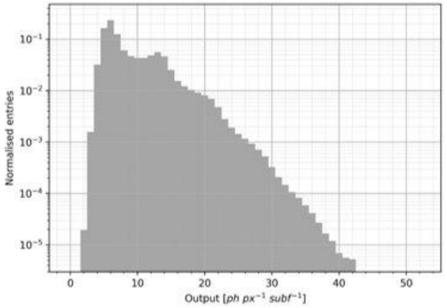
Low Flux < 1 ph/frame

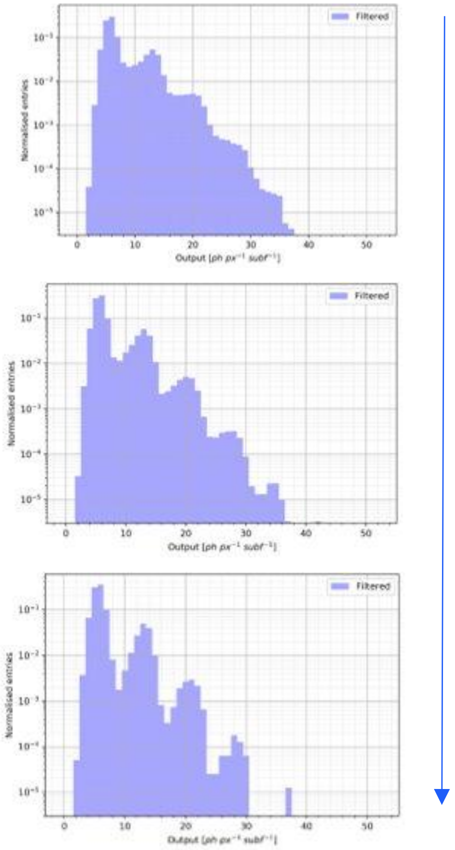


if neighbours > threshold
charge sharing → discard

else 0 or 1 photon in
central pixel → keep

Raw 500k frames

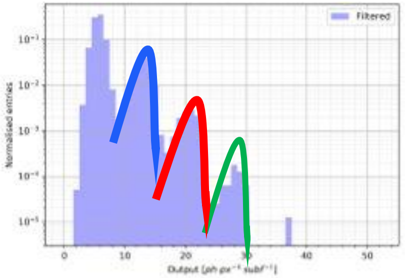




Decreasing
threshold

1% of
events

Still some charge loss
where E lost < Th



Some correction to do?

Science and
Technology
Facilities Council

UNIVERSITÄT
HEIDELBERG
ZUKUNFT
SEIT 1386

diamond

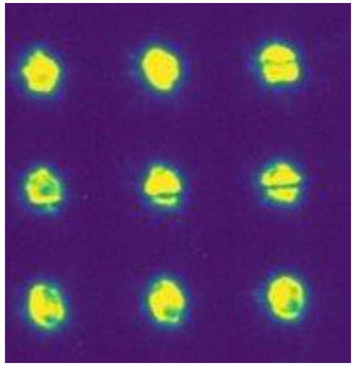
ESRF
The European Synchrotron

European
XFEL

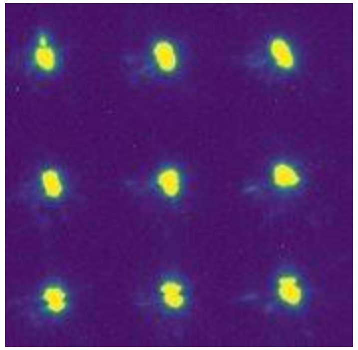
PUBLICATION IN PROGRESS

Physical Mask

Laser drilled array of holes on 110 μm pitch (16x16 trial)



40 μm

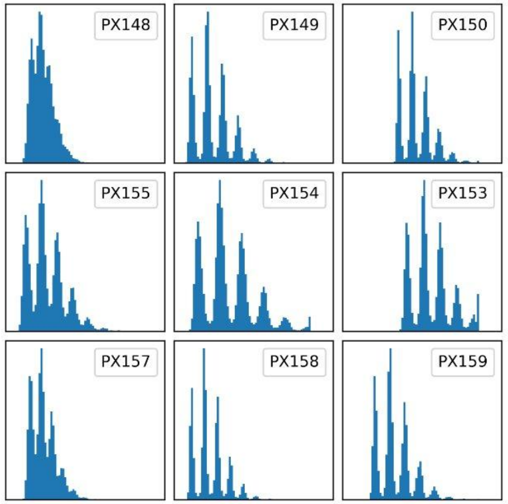


20 μm

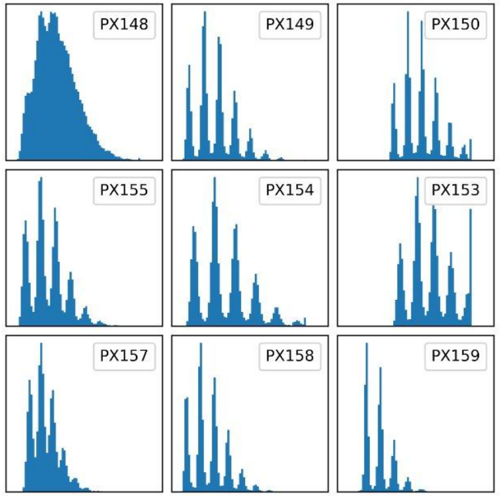
Spacing of holes most important
Holes just need to be small enough

Known Bad Pixel

40 μm



20 μm



No trim on test ASIC

Works fine…
- Probably not practical for deployment
- But maybe a way to get correction for software method?

PUBLICATION IN PROGRESS