# High Timing Resolution Frontend ASIC Development

Xiongbo Yan

on behalf of elec group, IHEP

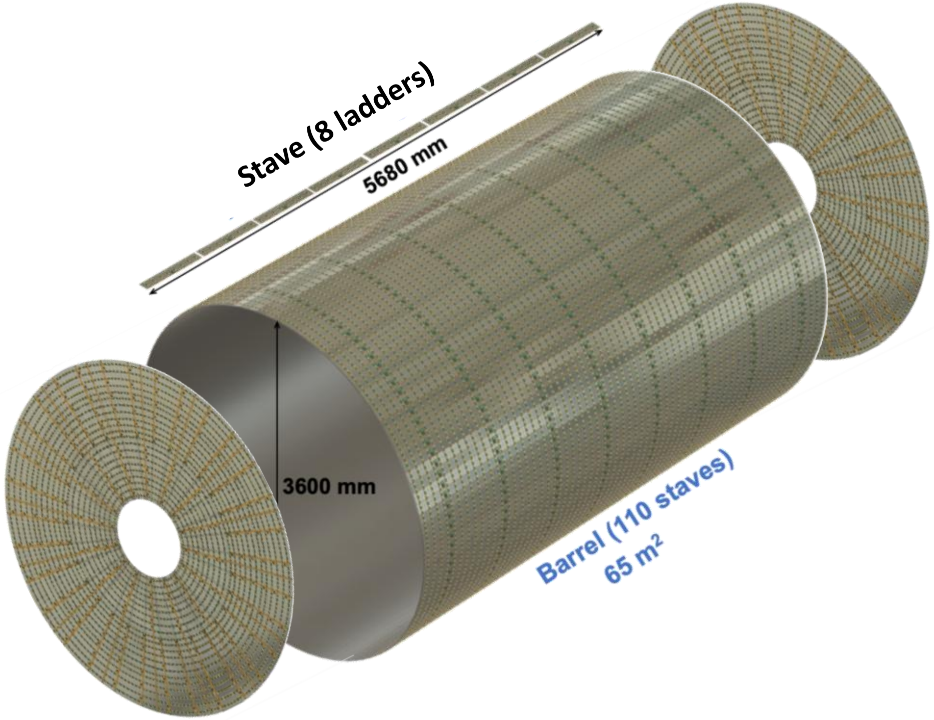
# Outline

- ◆ LATRIC Chip for CEPC OTK
- ◆ FPMROC Chip for ToF-PET

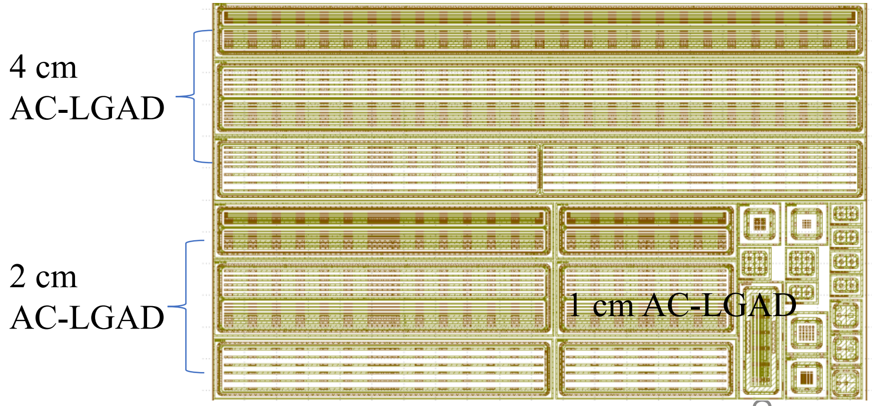
# Outer Traker in CEPC

- As the outermost tracking detector, the OTK functions as a high-granularity Time-of-Flight (ToF) detector, offering precise timing measurement for particle identification.
- Based on microstrip AC-coupled Low Gain Avalanche Detector (AC-LGAD) technology - provides precise spatial measurement and extends the tracking lever arm, enhancing overall tracking performance, particularly in momentum resolution.

| Specification for OTK | |
|---|---|
| Sensor size | (3-4.5) cm × (3-5) cm |
| Strip pitch | ~100 µm |
| Spatial resolution | 10 µm |
| Timing resolution | 50 ps |
| Power | 300 mW/cm² |




- A Long micro-strip is proposed for LGAD design, and a prototype with different length and pitch was submitted.



# LATRIC（LGAD Timing and Readout Integrated Chip）

◆ **LATRIC ASIC specification ( Assumed Cd=8pF )**

| Parameter | Value |
|---|---|
| Voltage | 1.2 V |
| Number of channels | 128 |
| Channel pitch | < 100 μm |
| Single channel noise (ENC) | < 10,000 e⁻ (1.6 fC) |
| Cross-talk | < 10% |
| Maximum jitter | 30 ps at 16 fC |
| Minimum threshold | 4 fC |
| Dynamic range | 8 fC–50 fC |
| TDC conversion time | < 23 ns |
| Power dissipation per ASIC | 1.5 W (for occupancy < 1%) |
| Data size per fired channel | 48 bits |
| e-link driver bandwidth | 43.33 Mbps or 86.67 Mbps |

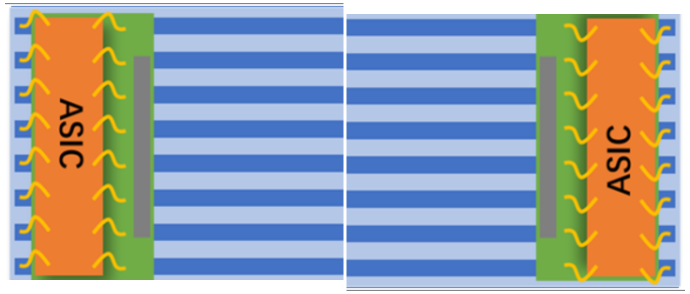
Channel pitch → (Wire bonding channel to channel)

Maximum jitter → (Assume LGAD contributes 40 ps)

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{clock}^2 + \sigma_{elec}^2$$

Power dissipation per ASIC → (Large cap leads to high consumption)

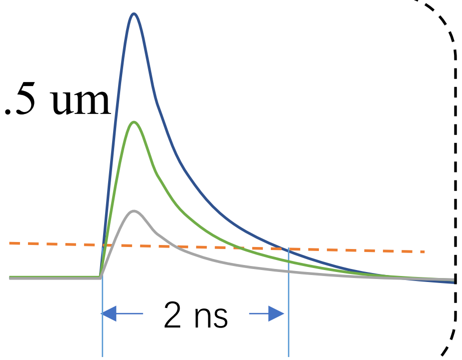
$$\sigma_{jitter} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d} \propto \frac{C_d \sqrt{t_d}}{Q_{in} \sqrt{I}}$$




Layout of module

- LATRIC0 (single-channel, 55 nm, April, 2025)
  - Front-end, TDC, Serializer（720MHz）
- LATRIC1 (8-channel, October, 2025)
  - Front-end, TDC (improved), Event builder, Serializer（40 MHz）
  - 4 channel with Front-end, 4 channel without.

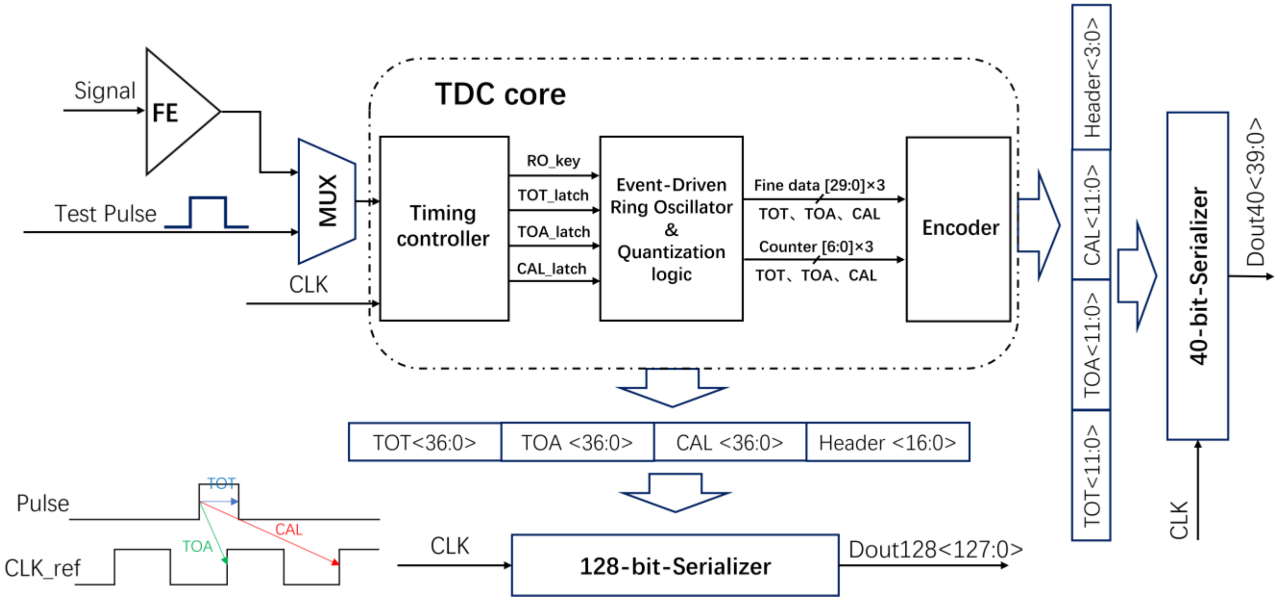
Spacial resolution:
50 ps/2 ns*100 um=2.5 um



# LATRIC0

## ◆Architecture

- Front-End (FE)
  - An amplification and a discrimination.
- TDC core
  - Timing controller;
  - Event-Driven RO & Quantization logic;
  - Encoder.
- Output logic
  - Output the Measured CAL, TOT, TOA codes;
  - 128-bit Serializer for 111-bit raw data;
  - 40-bit Serializer for 36-bit encoded data.




LATRIC0 overall block diagram

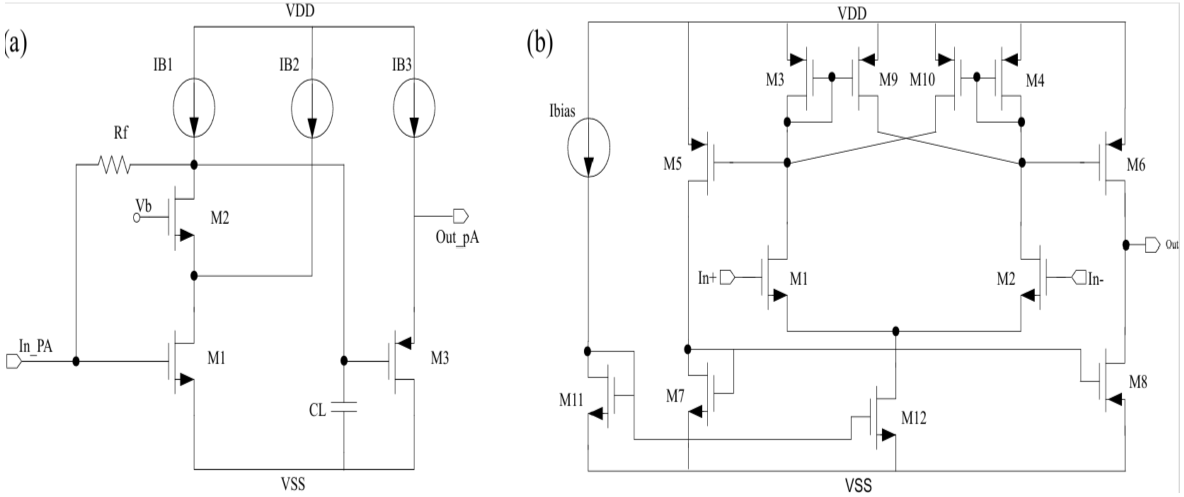
## ■ Self-calibration

- An additional period of CLK_ref is measured for calibration： $LSB_{Cal} = T_{CLK\_ref} / CAL_{code}$;
- $TOA_{time} = LSB_{Cal} * TOA_{code}$;
- $TOT_{time} = LSB_{Cal} * TOT_{code}$.

# Circuits Design

## ■ Front end

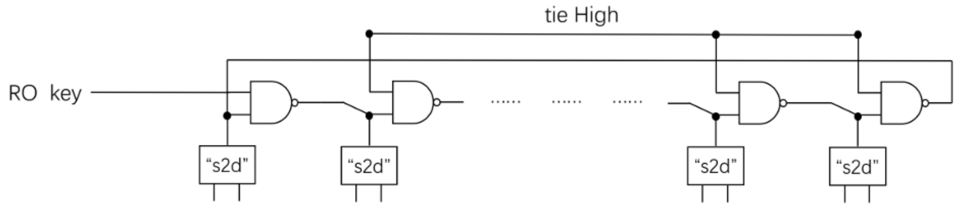
- ➢ A Trans-impedance Amplifier
- ➢ A Discriminator with 2 stage preamplification




Front end circuits: (a)TIA; (b)Discriminator

## ■ TDC core

- ➢ Controller
  - Reference clock, RO control; latch signal generation.
- ➢ Ring Oscillator (RO
  - The RO employs 15 NAND-based delay cells, each providing an average delay of about 30 ps.
  - The S2D converters transform both the rising and falling edges into differential signals for the three groups of SR latches;
  - The symmetric structure of SR latch ensures a consistent response to both rising and falling edges from the delay cells.




15-stage NAND delay chain + s2d block, 30 bit fine phase output

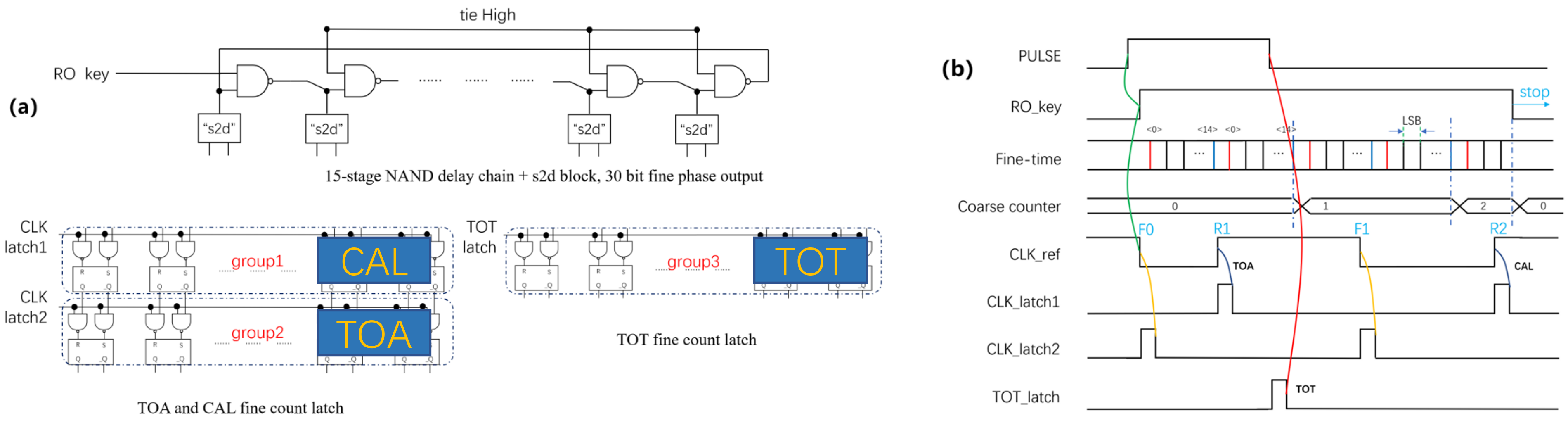
Event-Driven RO

# Quantization Logic

## ■ TDC core

➢ Quantization logic

- When the leading edge of the PULSE signal arrives, the RO is activated, the CLK_ref is enabled, coarse count starts.
- The following two rising edges of CLK_ref after PULSE latches the RO states as TOA and CAL respectively.
- The trailing edge of the PULSE signal latches the RO state as TOT.

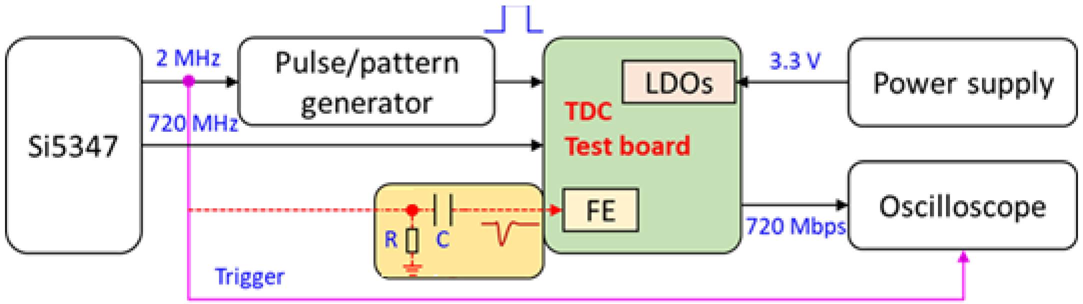


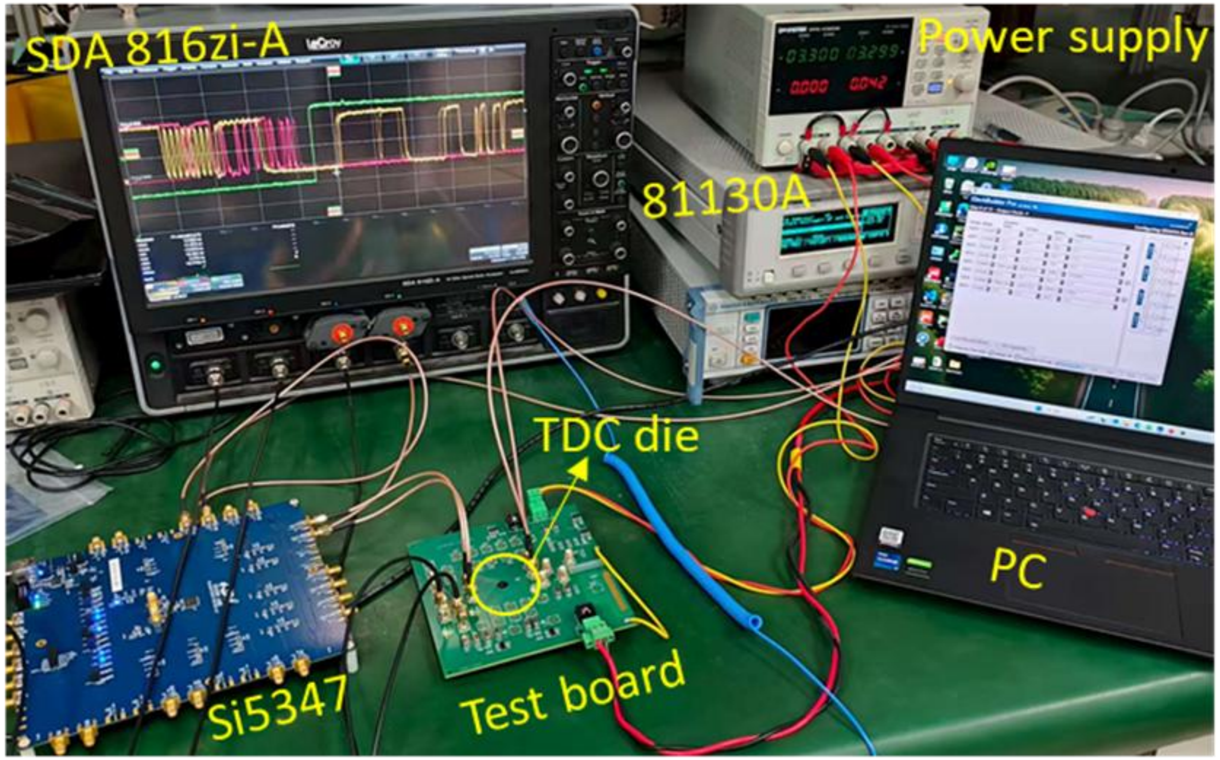

(a) Event-Driven RO & Quantization logic; (b) Quantization timing

# LATRIC0 test results

## Test Setup

- Test-pulse mode
  - A 720-MHz clock (Si5347) for both serializer and TDC.
  - Inside divided down to 18 MHz as the reference clock for measurement.
  - A 2-MHz clock (Si5347) to trigger a pulse/pattern generator (81130A). Scanning TOA and TOT transfer curves by adjusting the pulse delay and width independently.
- FE-mode
  - For functional verification of the FE-TDC integration.



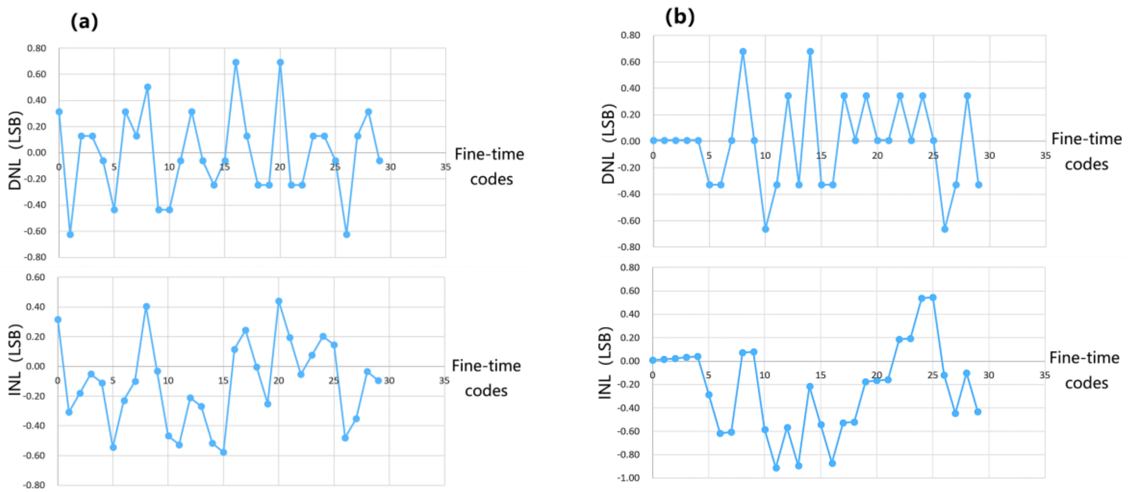




Test setup

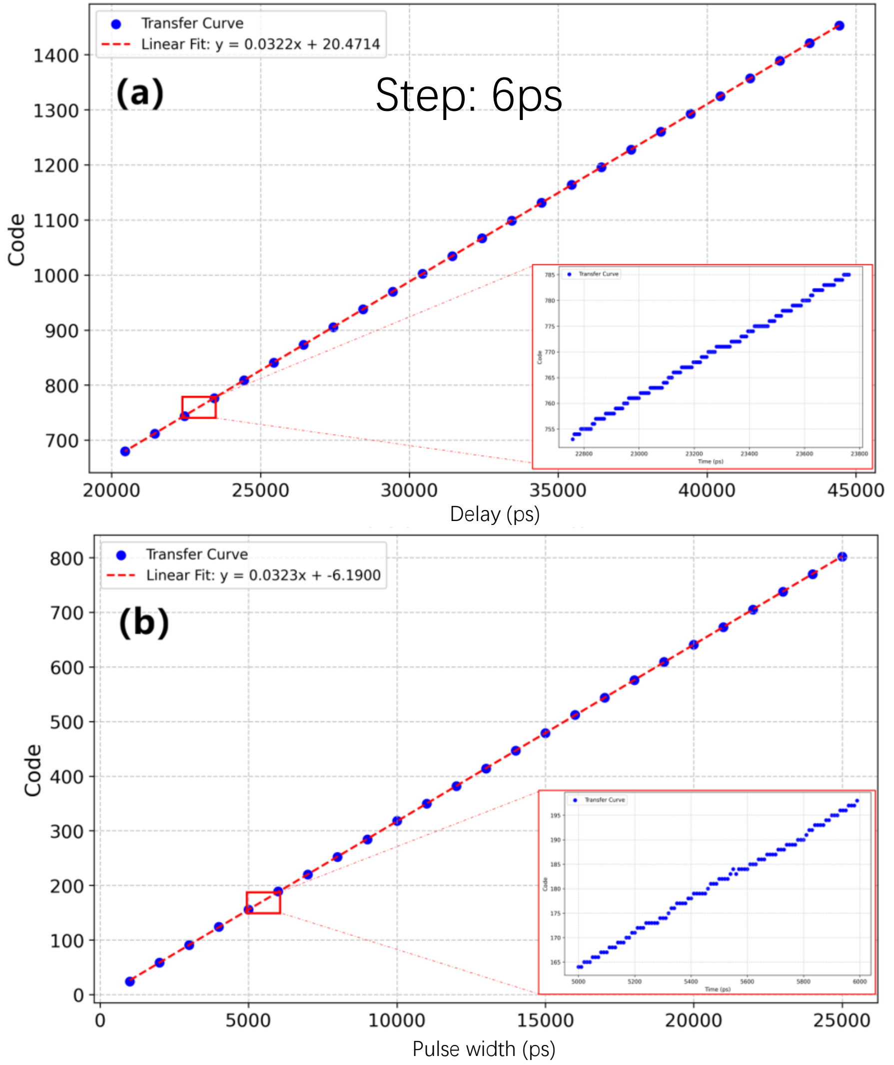
# LATRIC0 Test Results

## ■ Timing performance (test-pulse mode)

- $LSB_{toa} \approx 31.1$ ps;
- The TOA DNL and INL without FE : less than ± 1 LSB;
- $LSB_{tot} \approx 31.0$ ps ;
- The TOT DNL and INL without FE : less than ± 1 LSB;
- $LSB_{cal} \approx 31.1$ps ;
- These three LSB are very close, indicating the effectiveness of the self-calibration.




DNL & INL of: (a) TOA; (b) TOT

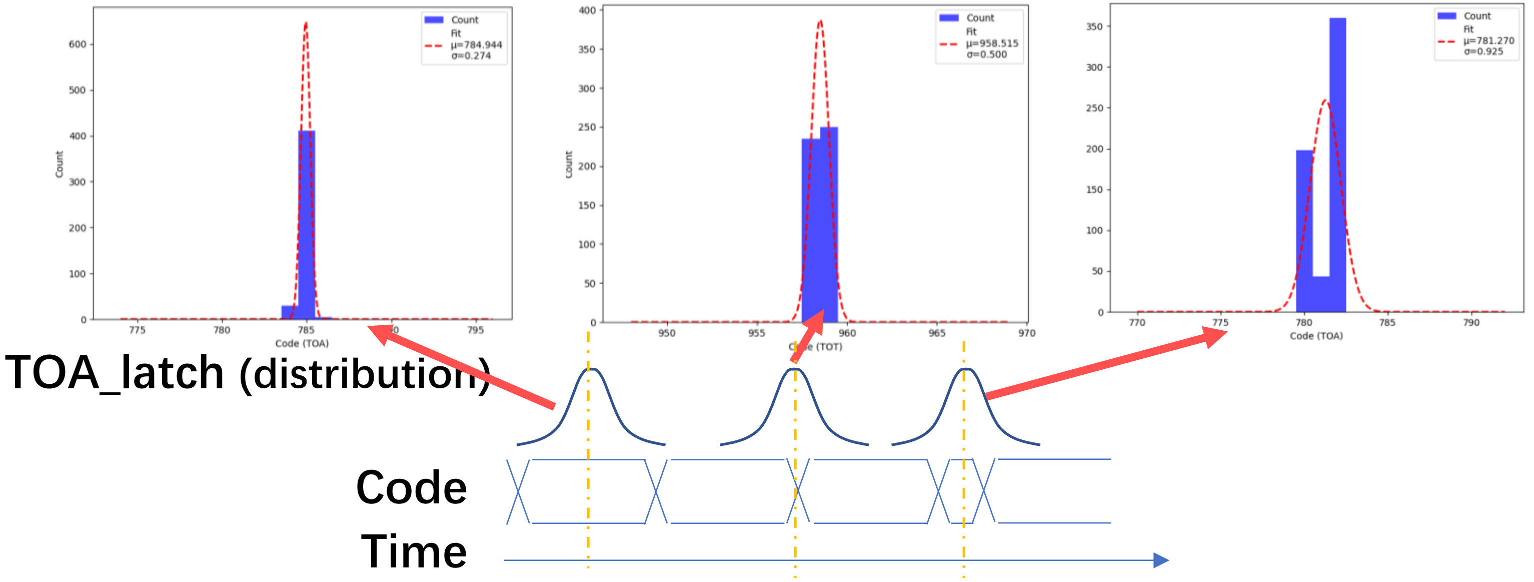


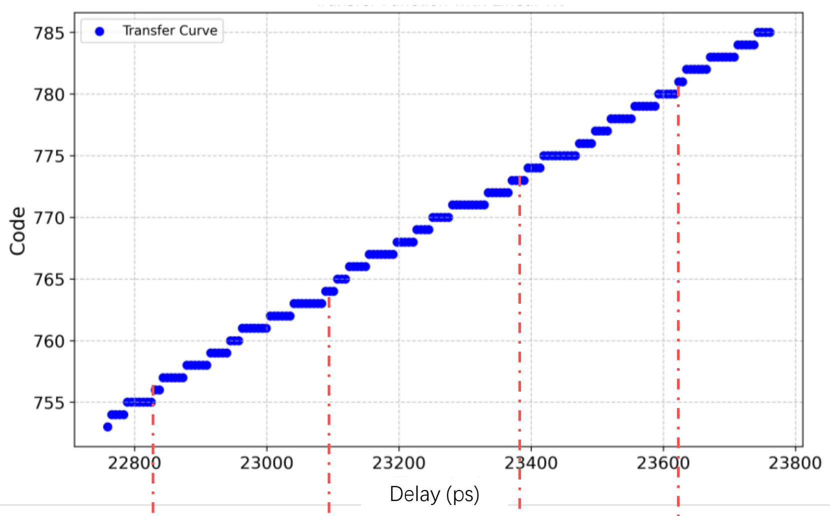

Measured transfer curves of: (a) TOA; (b) TOT

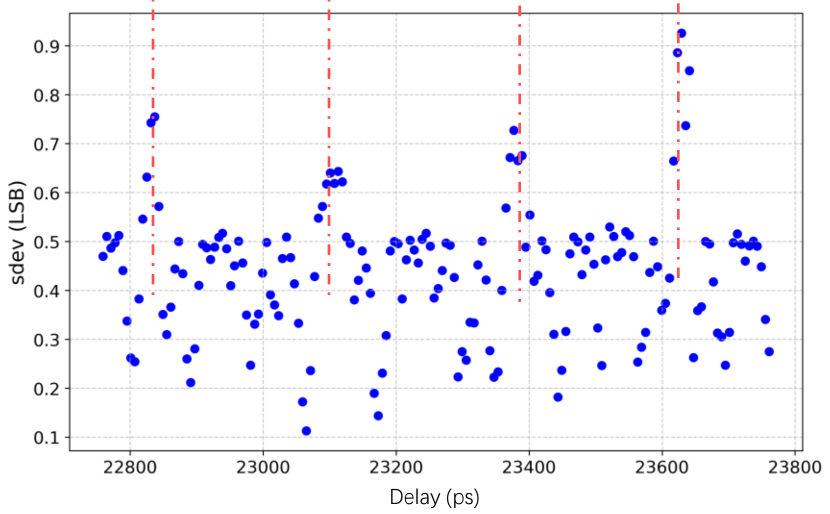
# LATRIC0 Test Results

## ■ Timing performance (test-pulse mode)

- σ < 0.5 LSB for most steps
- For σ > 0.5 LSB:
  - It happens at place with smaller bin width.
  - The code varies more to the jitter of the input for smaller bin width.




The standard deviation of Single Shot Precision

# LATRIC0 Test Results

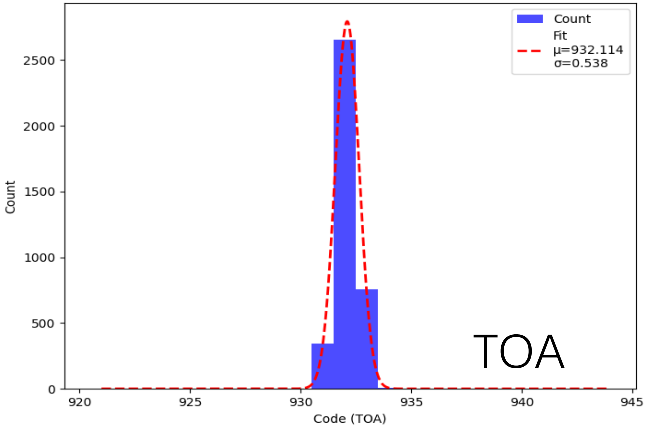
## ■ Timing performance (FE-mode)

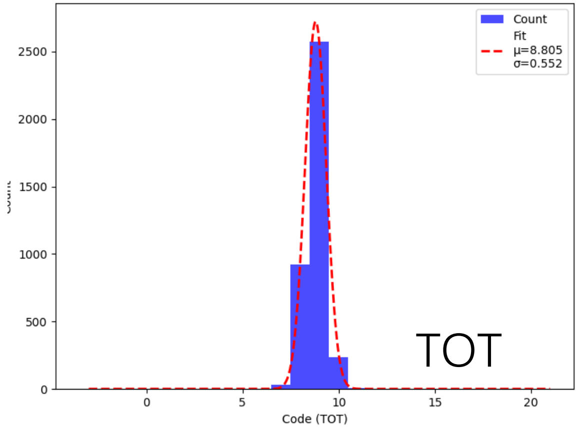
- $\sigma_{FE\text{-}TOA}$ and $\sigma_{FE\text{-}TOT}$ distributions <0.55 LSB for 8 fC injection.

## ■ Power consumption

- The FE consumes 4.9 mA (1.2V).
- The power consumption of the TDC core varies with event rate.
- The total power consumption is measured to be 6.24 mW at an event rate of 1 MHz.

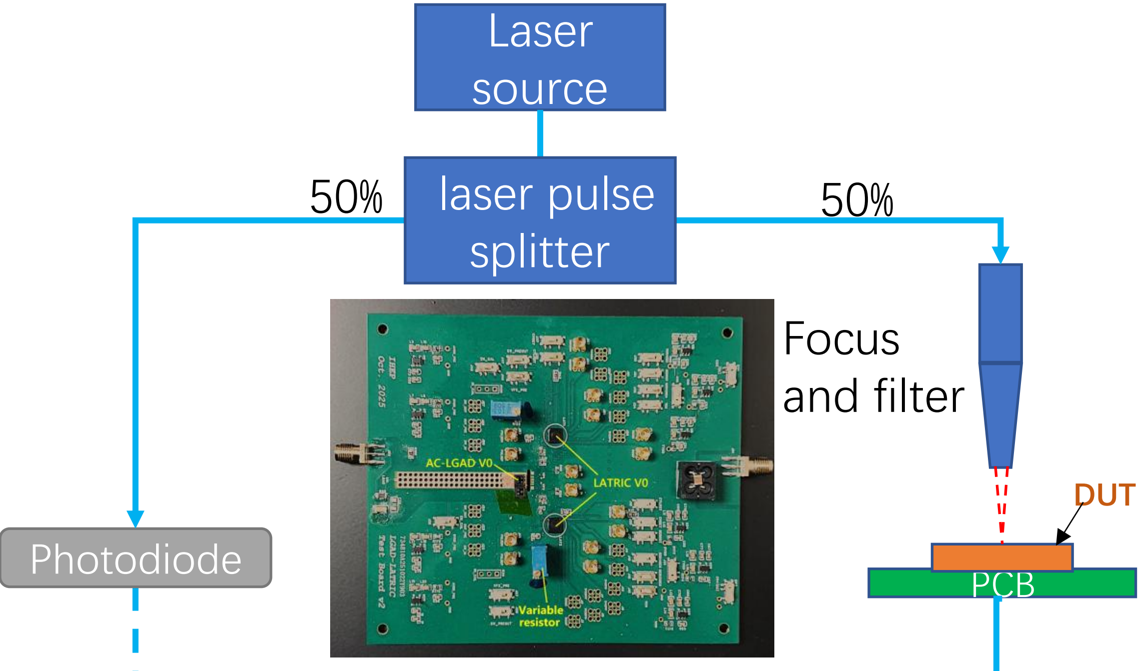
| Blocks | Event rate | Operating current |
|---|---|---|
| TDC part | 2 MHz | ~ 0.5 mA |
| | 1 MHz | ~ 0.3 mA |
| | 500 kHz | ~ 0.1 mA |
| Pre-amplifier | | ~4.9 mA |



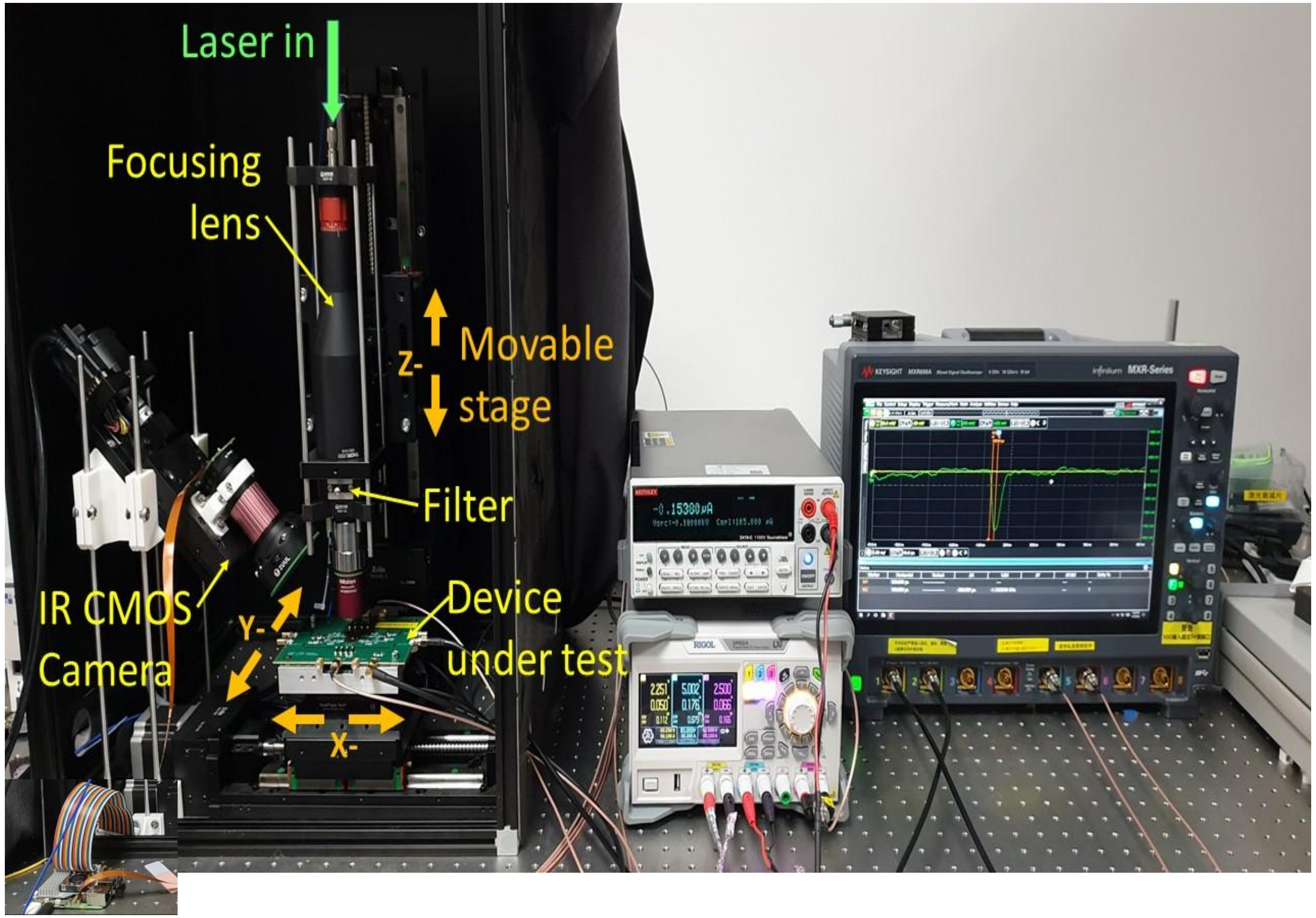




The statistical standard deviation for single shot
（input 8fC，Vth=830mV）

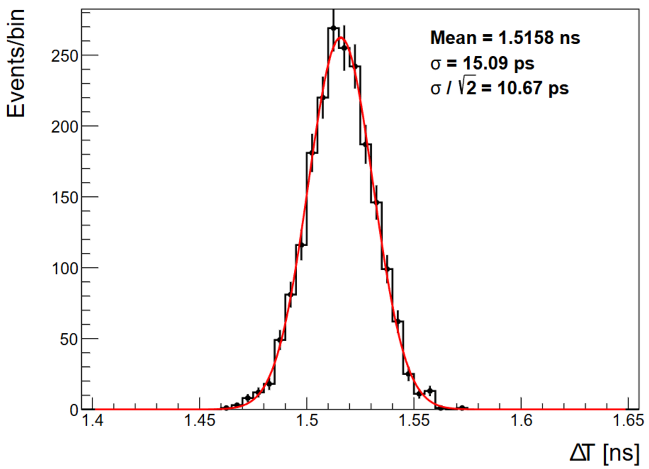
# LGAD+LATIC0 Laser Test



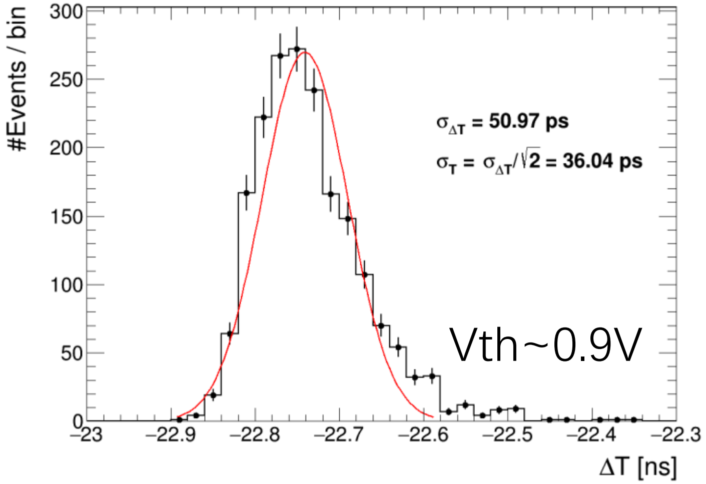

LGAD pixel 2.5mm* 2.5mm



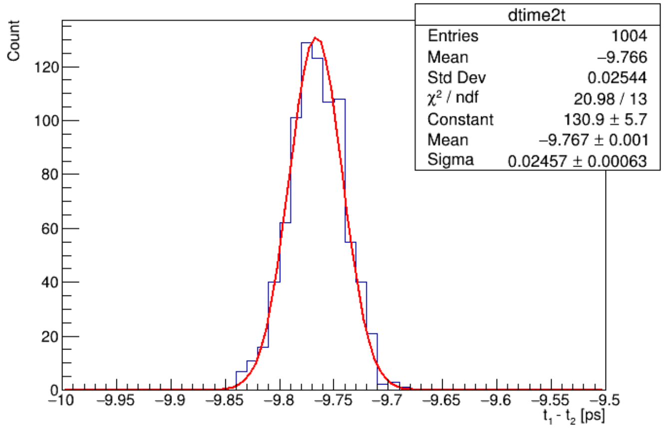
# Coincidence Time (LGAD+LATRIC0)



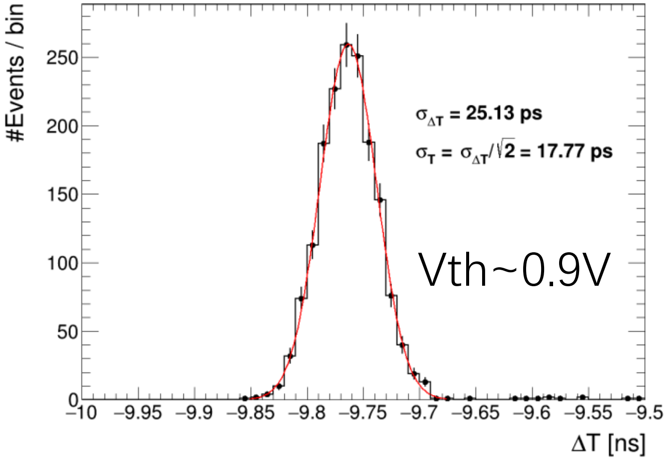

CTR of LGAD @ Laser intensity equivalent to MIP




TOA CTR of LGAD+LATRIC0@ Laser intensity equivalent to MIP




CTR of LGAD @ 100% Laser intensity

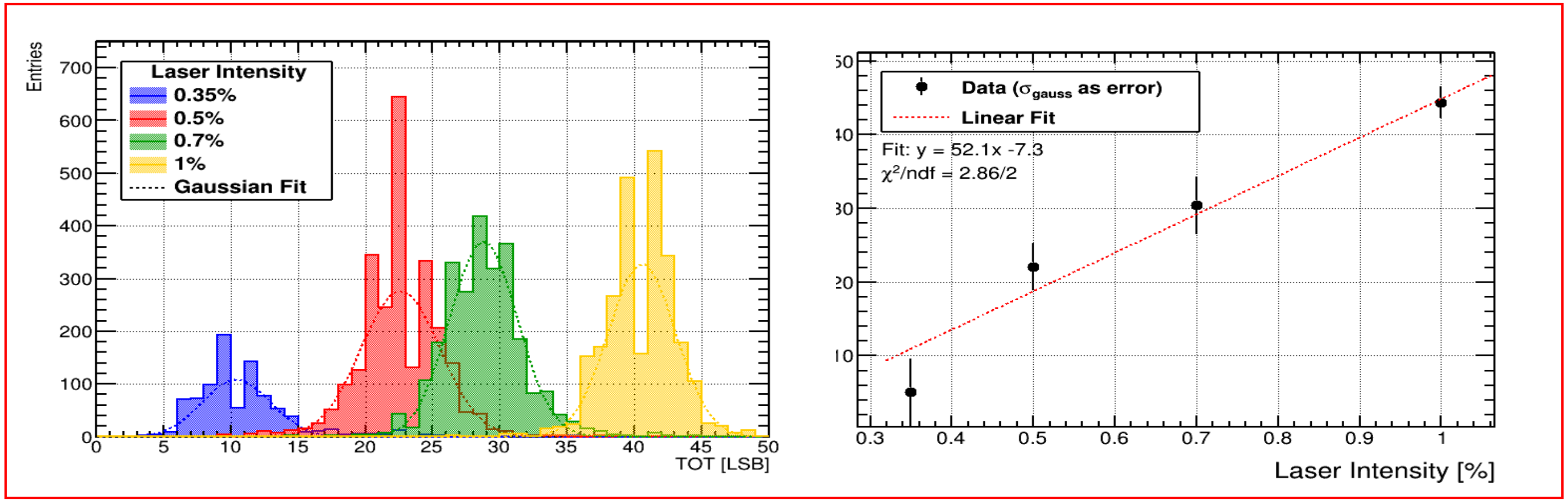



TOA CTR of LGAD+LATRIC0 @ 100% laser intensity

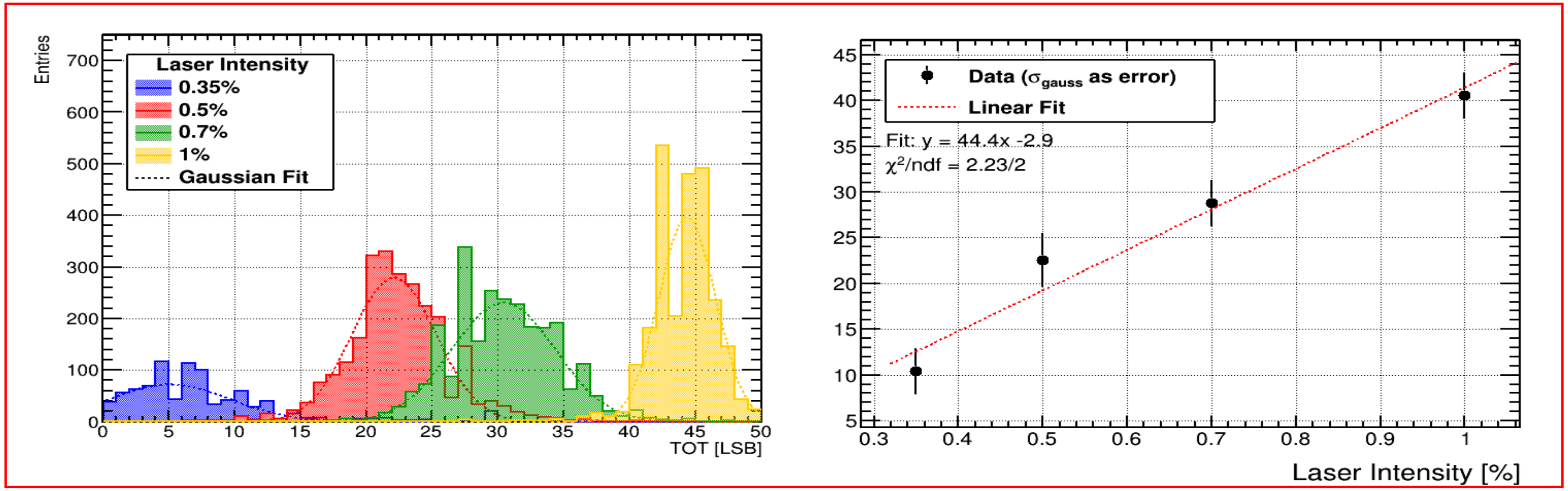
# TOT with Different Laser Intensity

◆ TOT changes with the laser intensity, but bad tot resolution, more study needed

LATRIC0-1

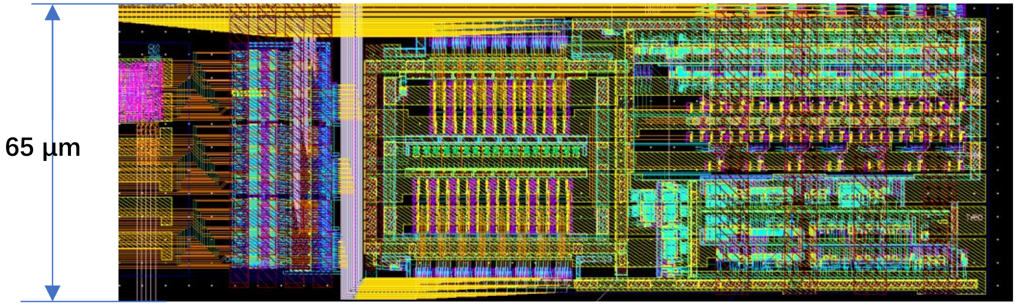



LATRIC0-2

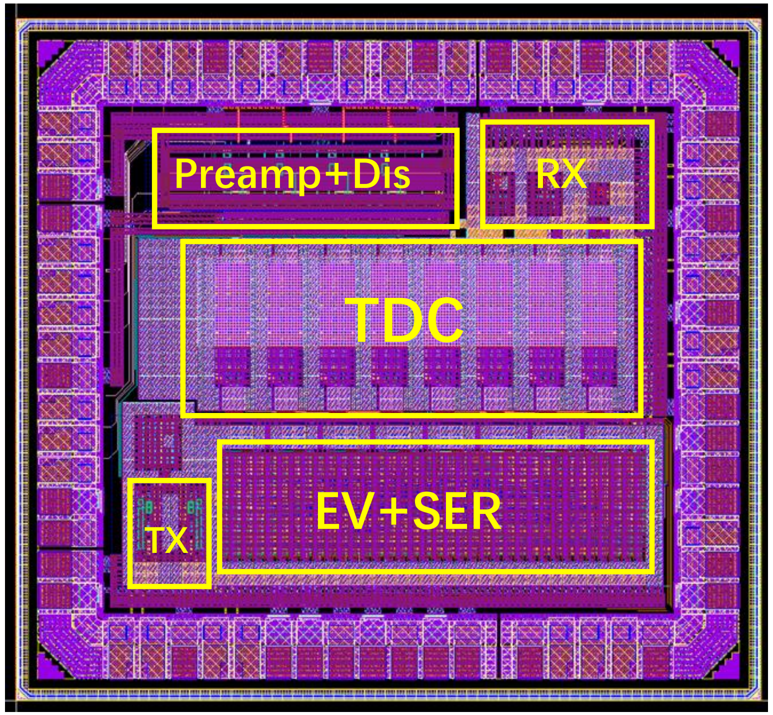


# LATRIC1

- LATRIC1
  - 8 channels; 4 channels with front-end;
  - 2 kinds of delay line,Original / Enlarged
    - CH0,CH1: TDC1
    - CH2,CH3,:   TDC2
    - CH3,CH4: FE+TDC1
    - CH3,CH4: FE+TDC2
  - Increase the gain of preamplifier;
  - Improve the encoder logic;
  - Add event builder and timestamp;
  - 100 µm channel pitch match the LGAD.



TDC single channel layout



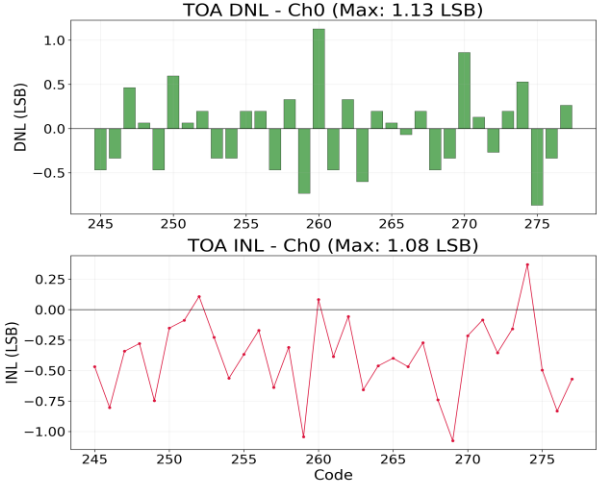
LATRIC1 layout

# LATRIC1 Test -Linearity

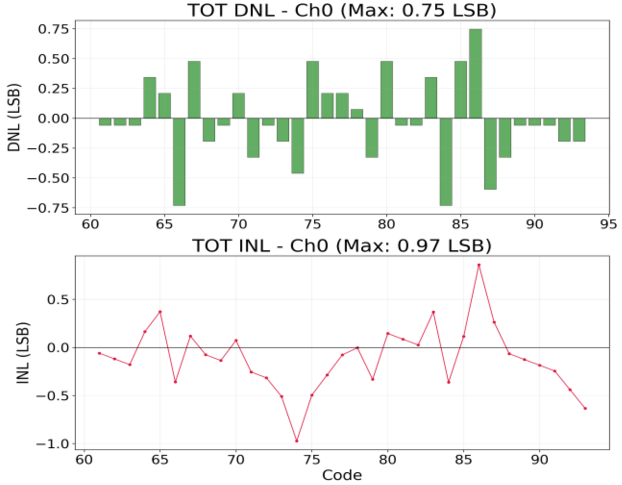
- CH2 has better linearity than CH0, thanks to larger transisitors.
- TOT has better linearity than TOA, because of lighter load for TOT delayline.

| | LSB(ps) | TOA(LSB) | | TOT(LSB) | |
|---|---|---|---|---|---|
| | TOA/TOT | DNL | INL | DNL | INL |
| CH0 | 29.8 ps | 1.13 | 0.97 | 0.75 | 0.97 |
| CH2 | 27.1 ps | 1.06 | 0.93 | 0.62 | 0.79 |

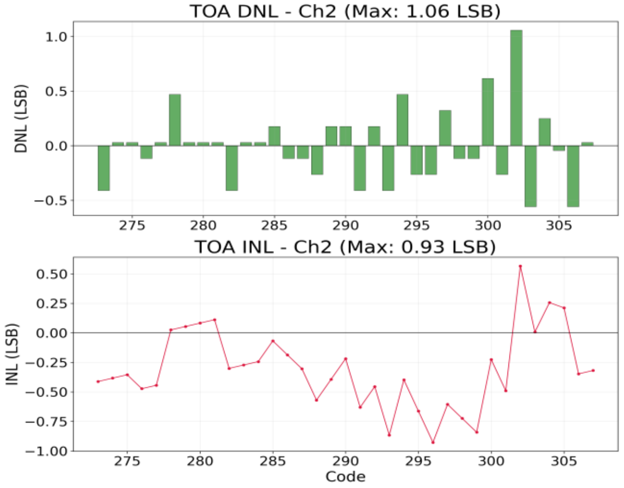
CH0 TOA



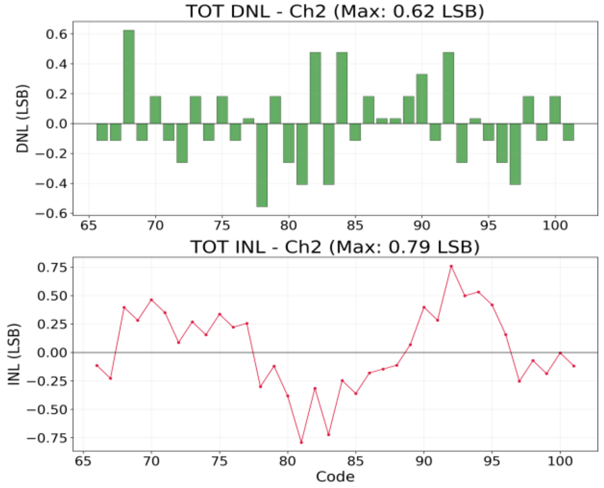

CH0 TOT




CH2 TOA



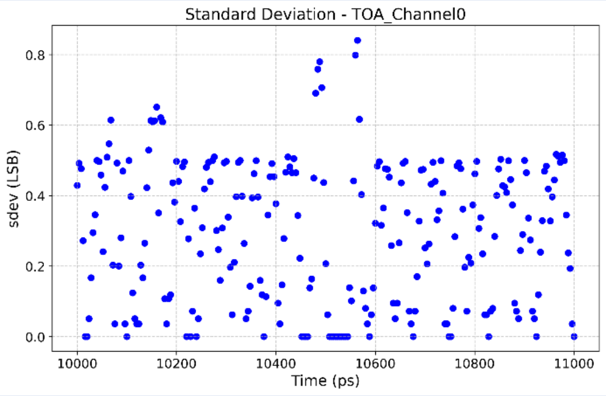

CH2 TOT



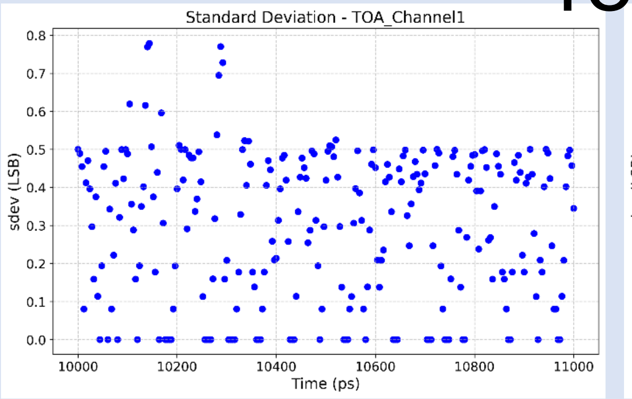
# LATRIC1 Test -Single Shot Precision

- $\sigma_{TOA}$~ 0.5 LSB, $\sigma_{TOT}$~ 0.5 LSB for channels without frontend.

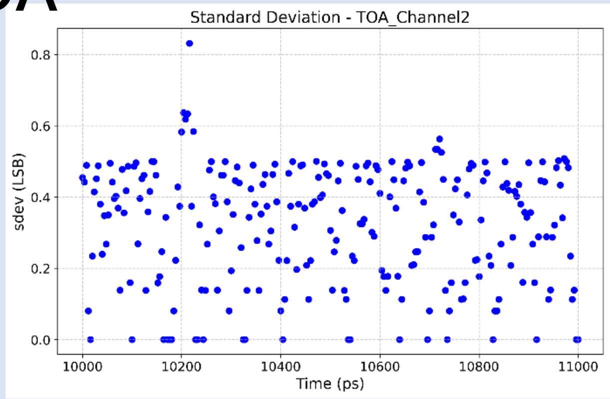
## TOA



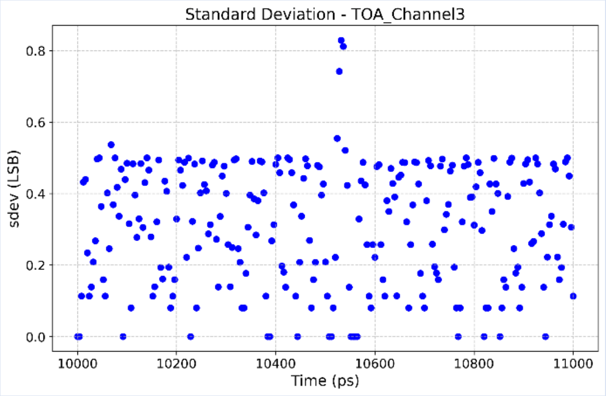

CH0




CH1

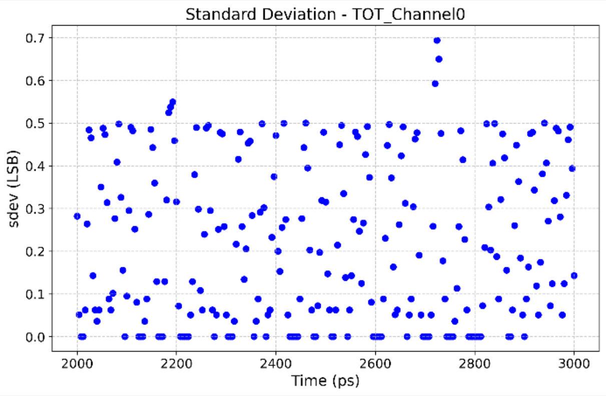



CH2

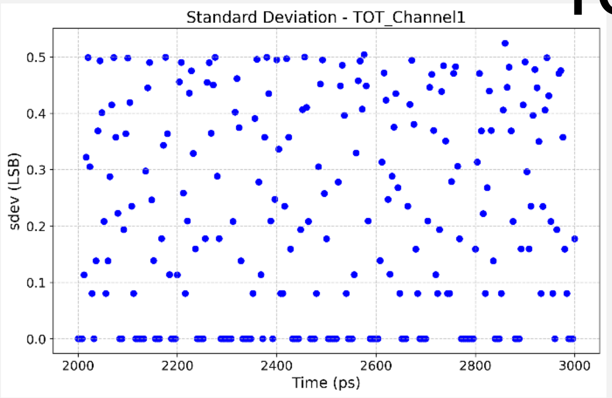



CH3

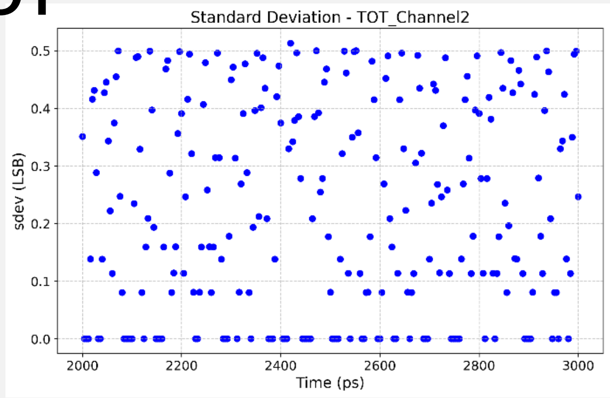
## TOT



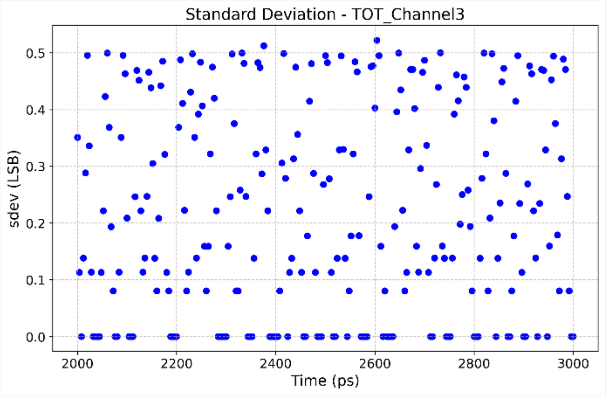

CH0




CH1

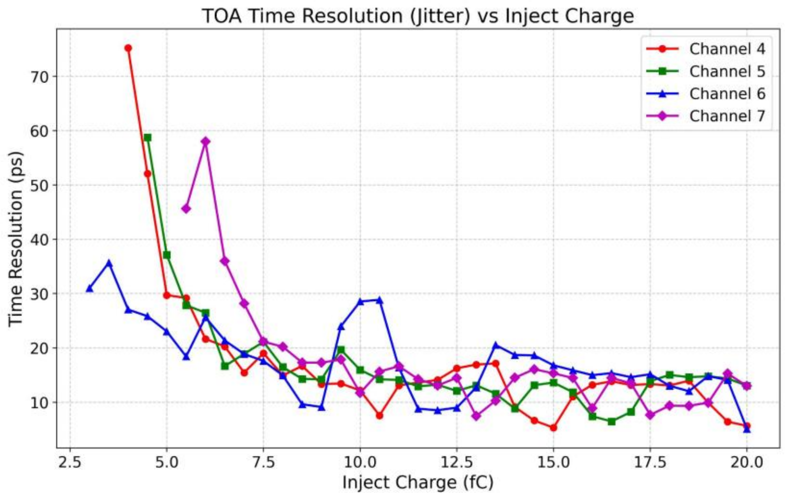



CH2

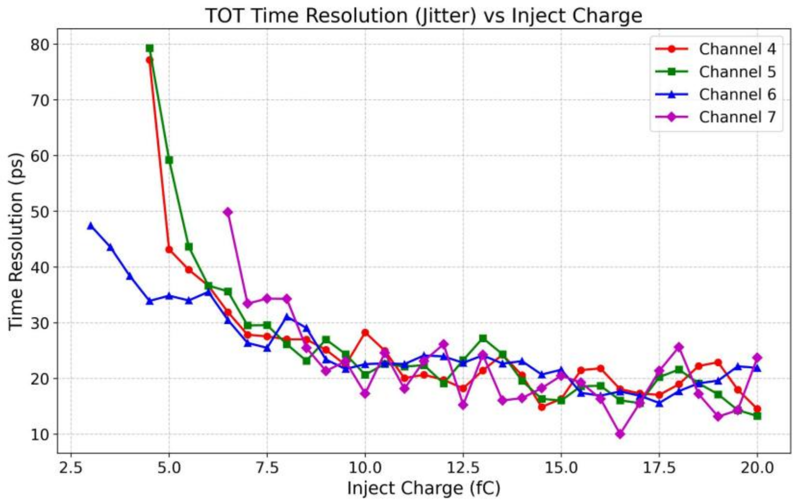



CH3

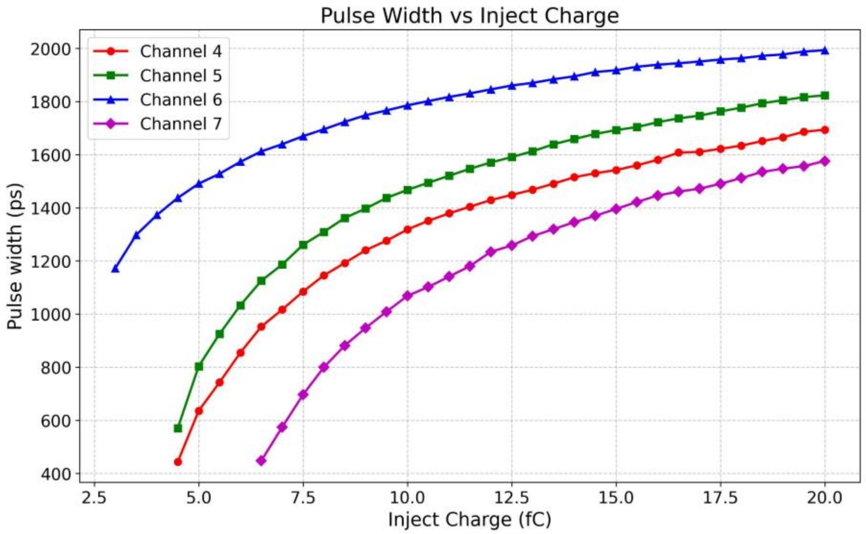
# LATRIC1 Test –Resolution vs. Charge




TOA resolution vs. Charge




TOT resolution vs. Charge




TOT vs. Charge

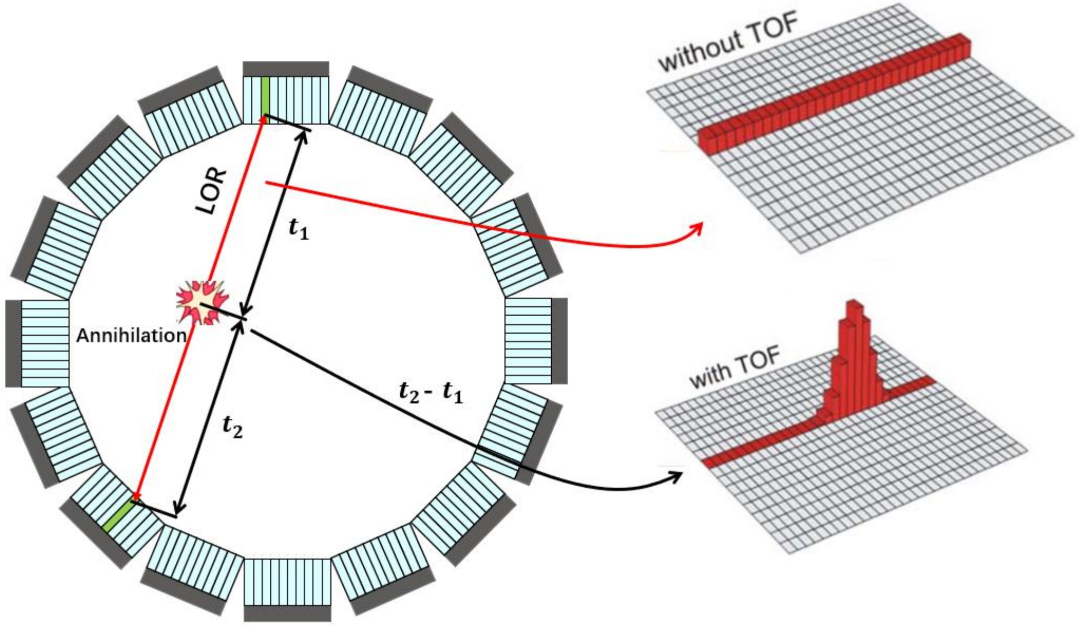
# Conclusion & Outlook for LATRIC

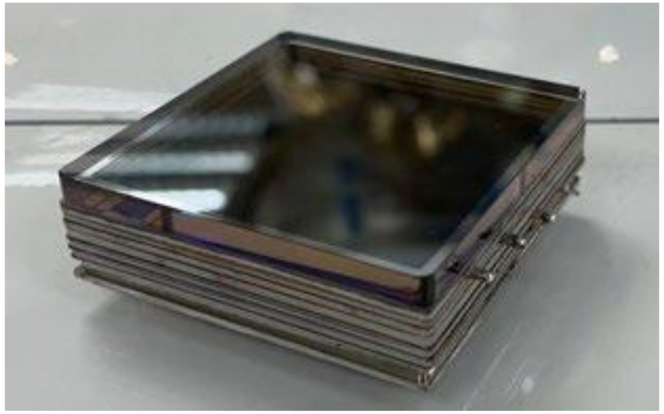
- LATRIC0 time resolution is proved with pixel LGAD by Laser, while performance test by β is ongoing.
- Spatial test system is debugging.
- LATRIC1 time performance is proved preliminarily, need more study, including crosstalk, temperature drift, ….waiting for LGAD strip
- A 32-channel chip is planned to be submitted in the end of 2026.

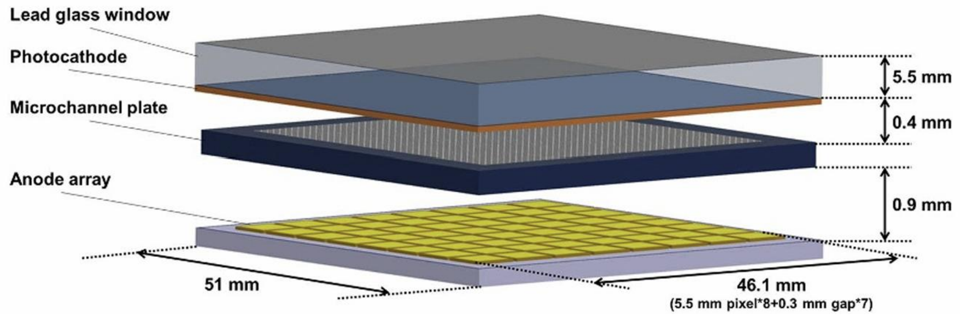
# Outline

- ◆ LATRIC Chip for CEPC OTK
- ◆ FPMROC Chip for ToF-PET

# PET imaging based on MCP-PMTs



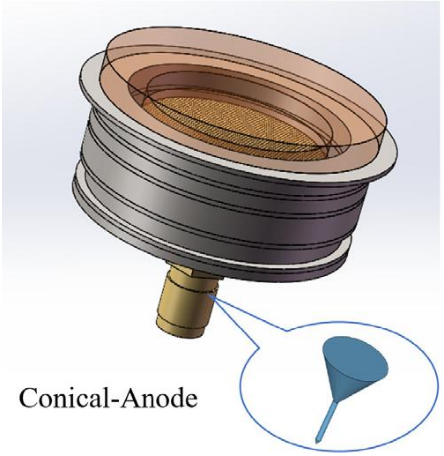



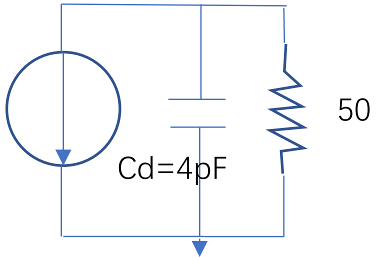


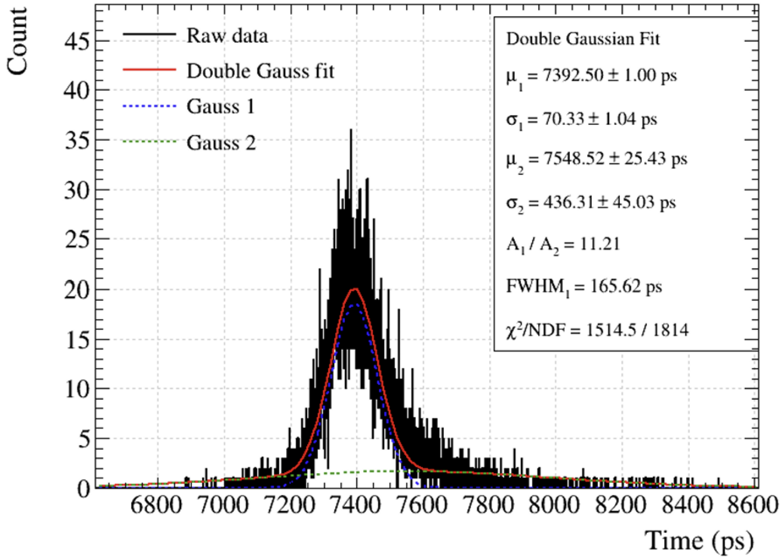

- Achieving a higher signal-to-noise ratio gain or direct positron emission imaging by improving the coincidence time resolution of time-of-flight positron emission tomography (PET) systems is paramount for many advanced clinical PET imaging applications.
- An effective method for enhancing detector time resolution is to use microchannel plate photomultiplier tubes (MCP-PMTs) for prompt Cherenkov photon detection.
- The final goal for the system is FWHM < 100 ps

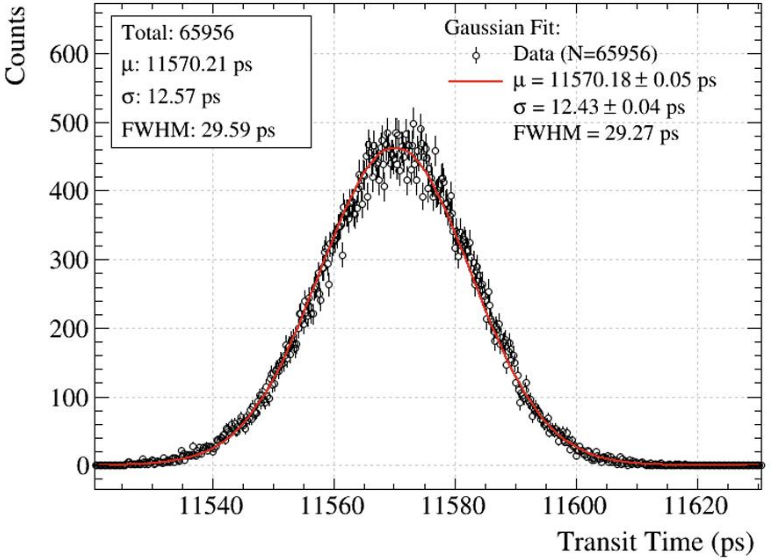
# Single Anode MCP-PMT

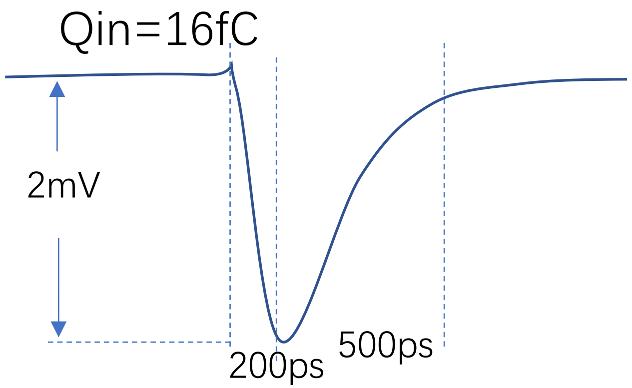
- **The MCP-PMT From NNVT**
  - Features a conical anode
  - Terminates with an SMA connector
  - Transit Time Spread ( early R&D sample )
    - Single-photon: ~70 ps
    - Multi-photon: ~13 ps



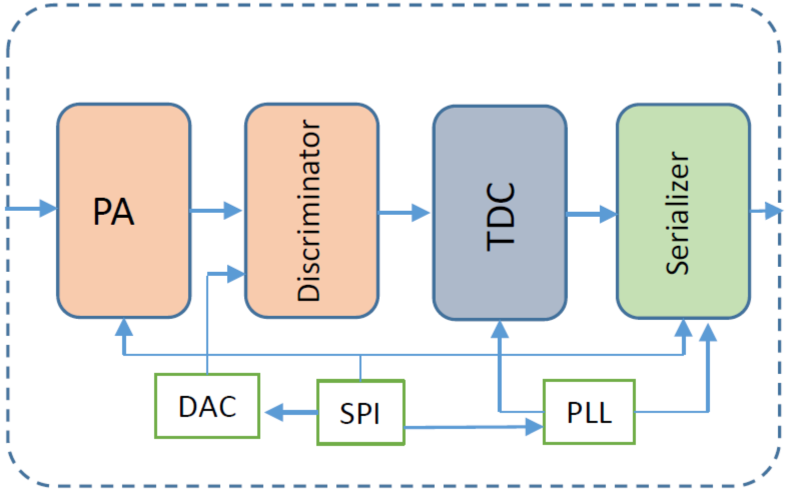



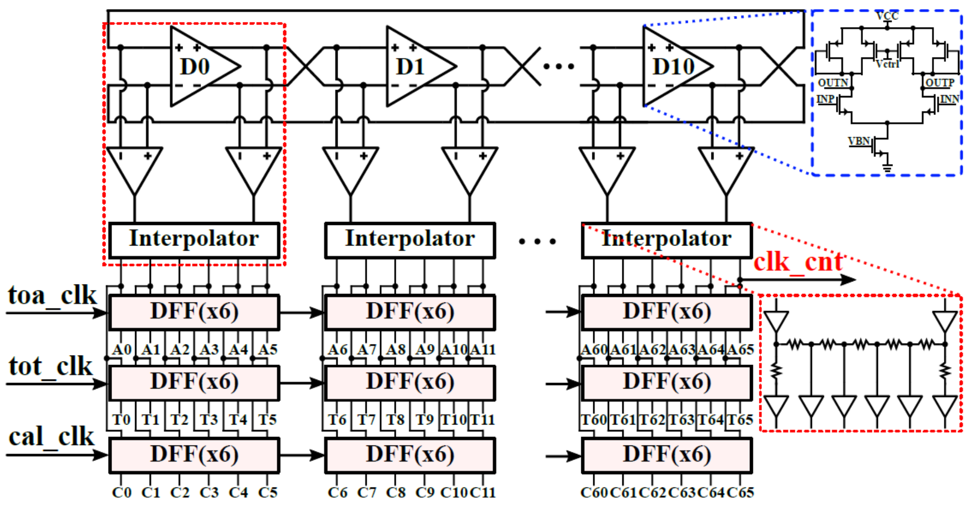



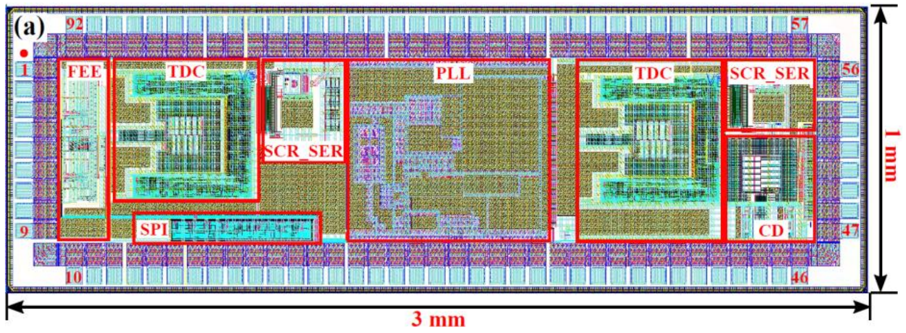



# FPMROC_1CH (Fast MCP-PMT ReadOut Chip)

- Same structure of frontend amplification and discrimination
- Different delay line to LATRIC
  - 11 voltage-controlled differential delay cells
  - A 6-stage passive interpolator for each delay cell
- Measure TOA, TOT, CAL

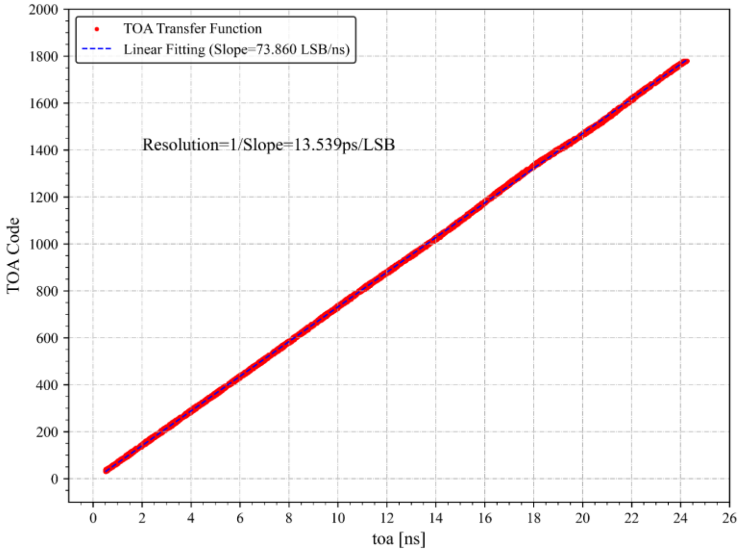


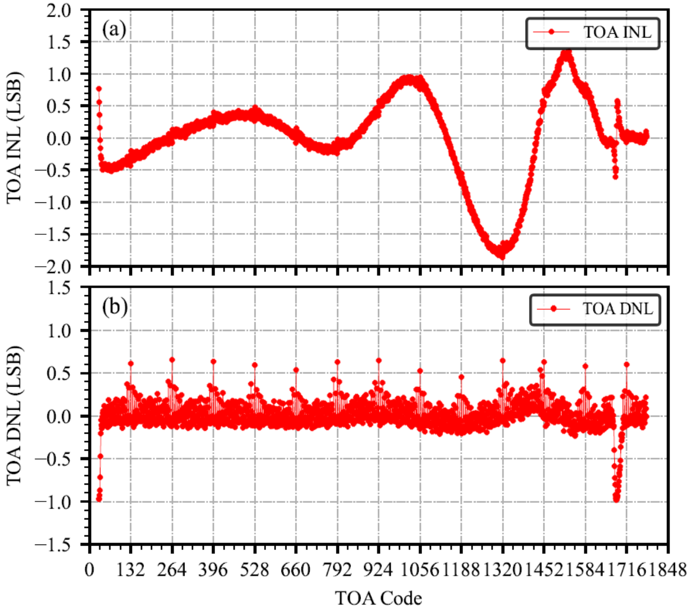



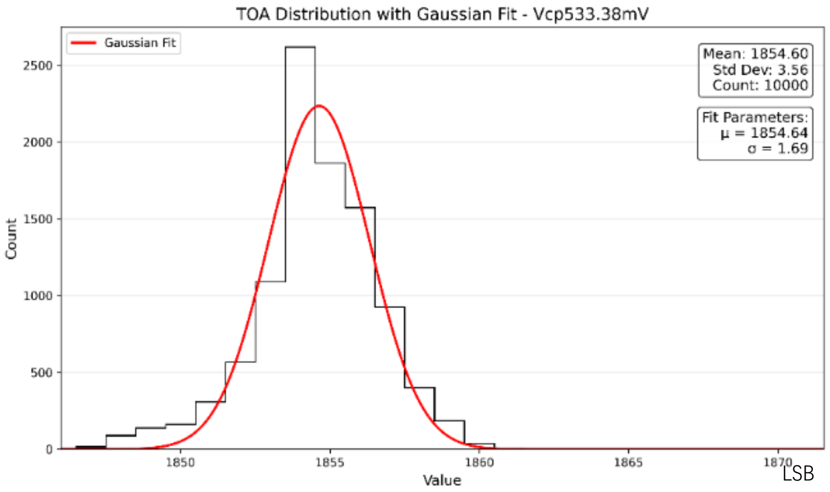
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# FPMROC 1CH test result

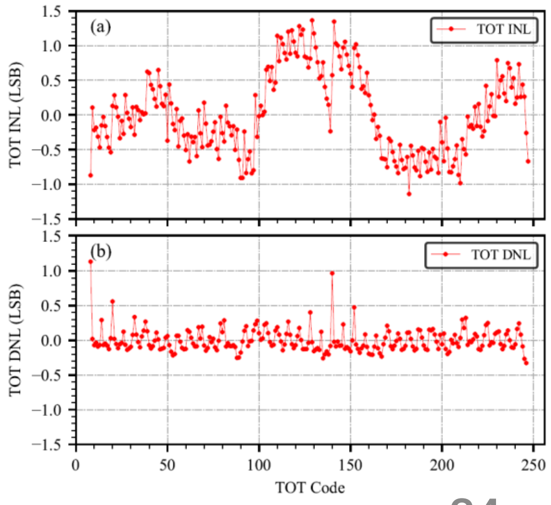



| parameter | performance |
|---|---|
| LSB | 13.6 ps |
| SSP | 23.2 ps |
| TOA DR | 0.2 ns-24.8 ns |
| TOT DR | 0.15 ns- 3.3 ns |
| TOA DNL<br>TOA INL | ±1 LSB<br>±1.9 LSB |
| TOT DNL<br>TOT INL | ±1.2 LSB<br>±1.5 LSB |
| Power | 20mW |



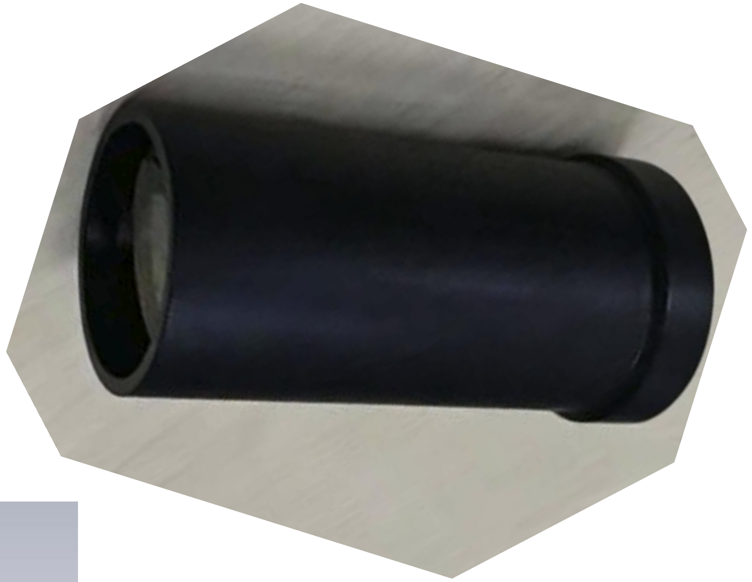



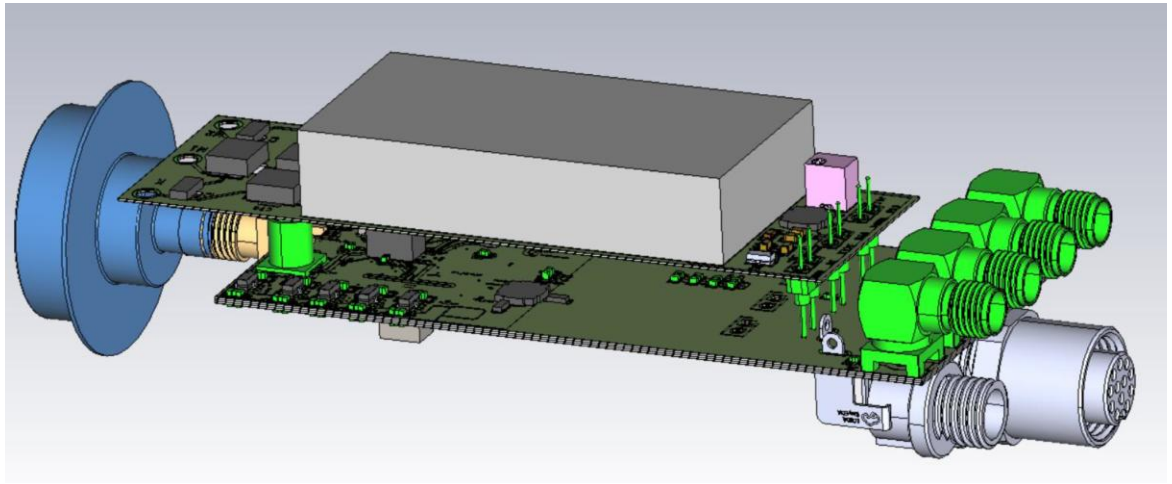

SSP @ Qin=16fC



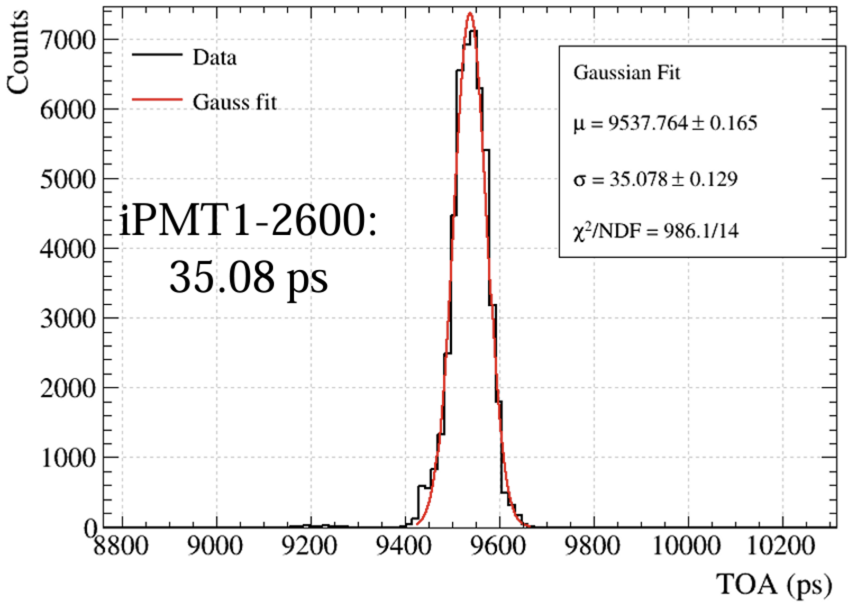
# iPMT

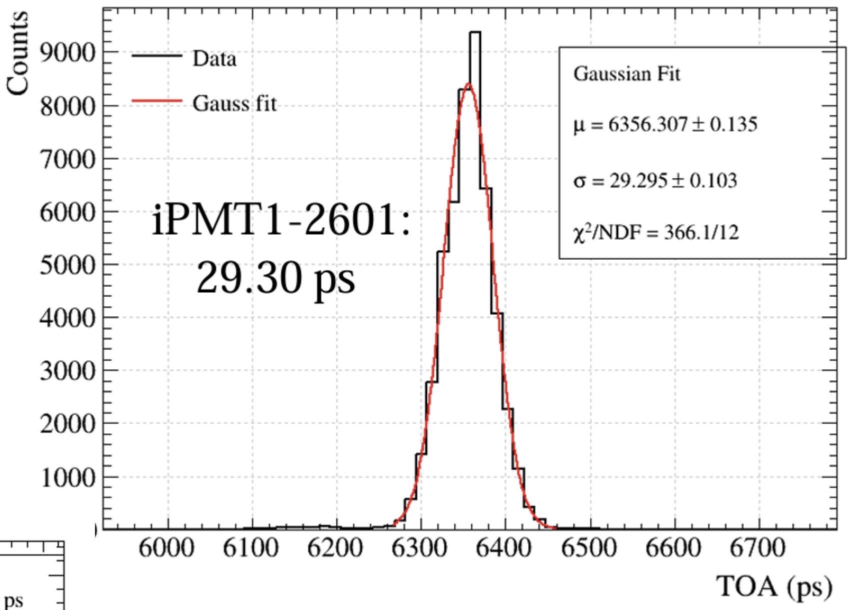
- **iPMT Integration**
  - FPMROC Chip，"Photon in, Data out"
  - High Voltage booster converter
  - Installed in a 40 mm diameter housing
  - The PCB connects directly to the MCP-PMT via SMA
  - Analog signal path merely 20 mm

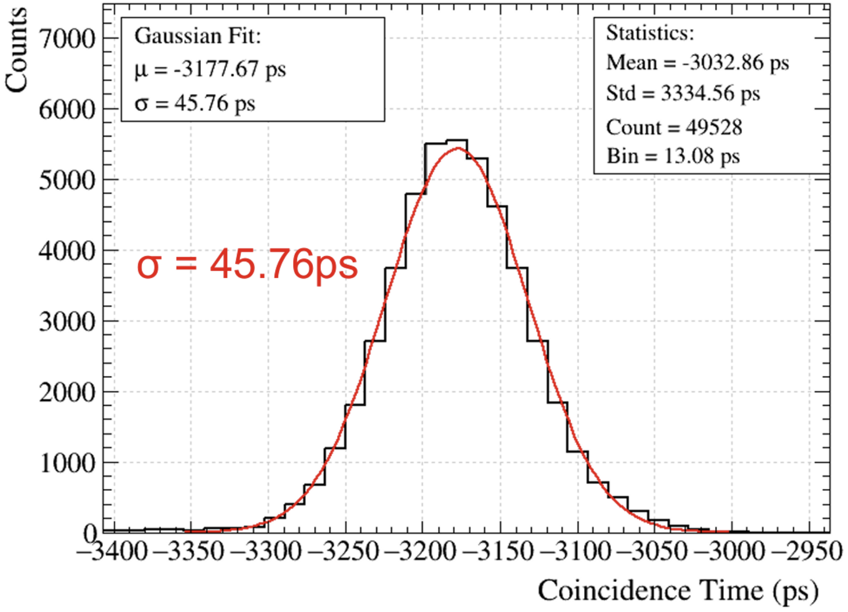




# iPMT coincidence test for multi-photon

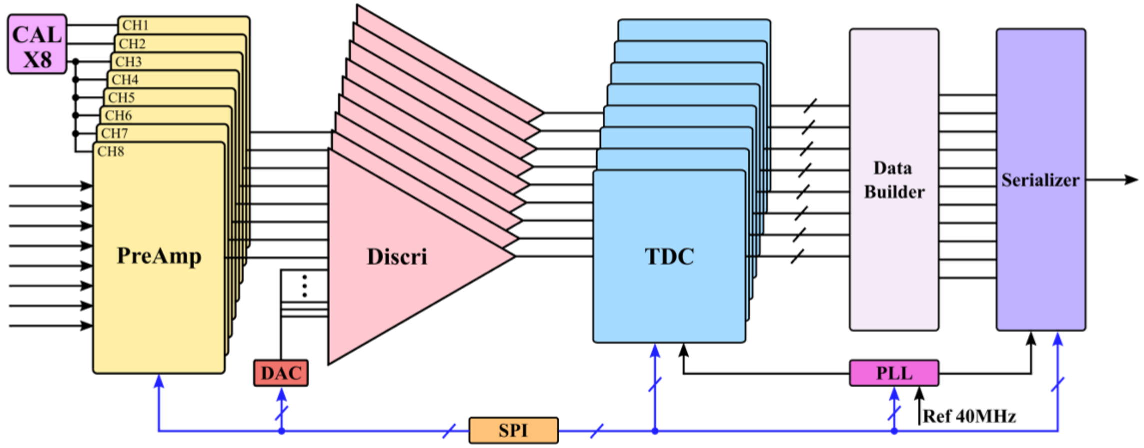


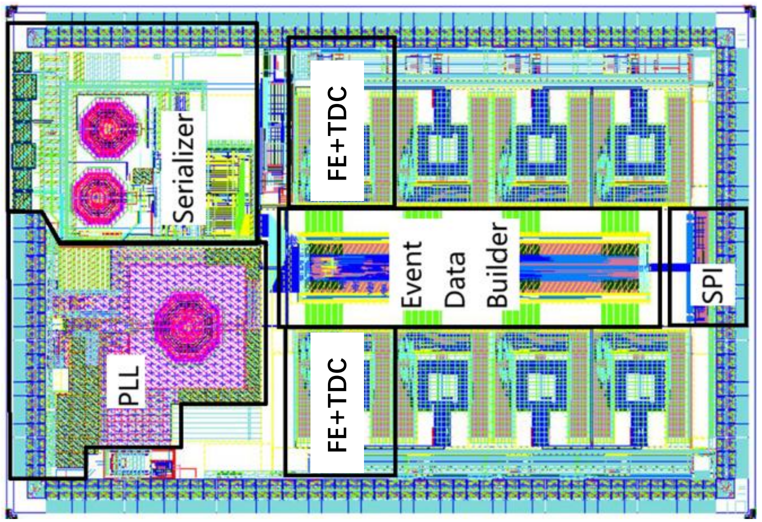



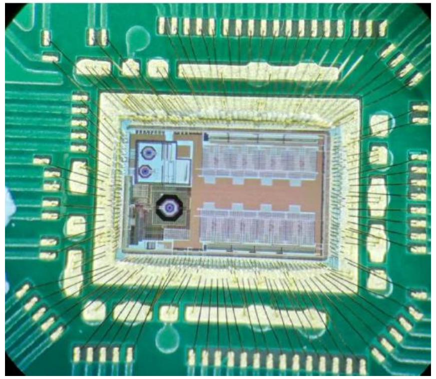
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

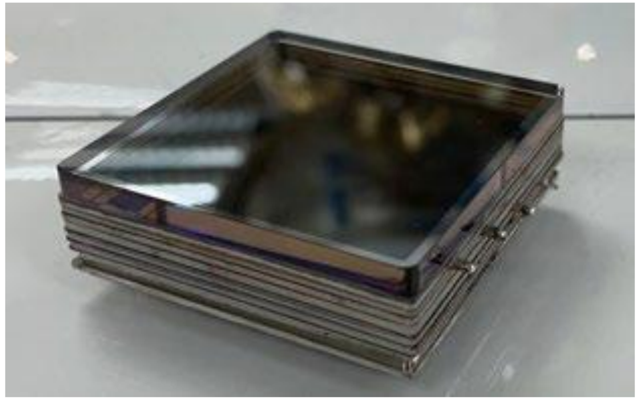
# FPMROC_8CH



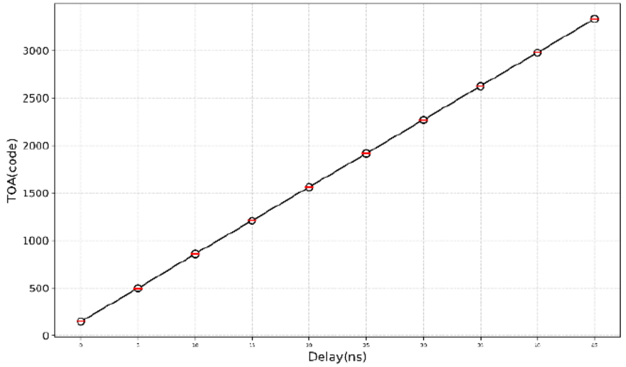




- FE： TIA and dicriminator
- CAL： test pulse injection
- DAC: threshold of each channel
- TDC： measure TOA, TOT, CAL
- PLL: 5.12GHz (40MHz ref CLK)
- Serializer： 10.24 Gbps
- **Event Builder**： combine data, 64B66B

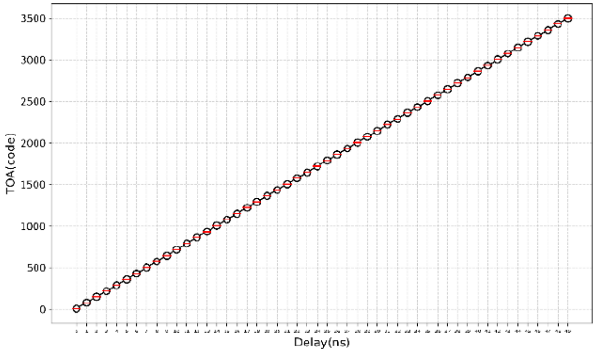




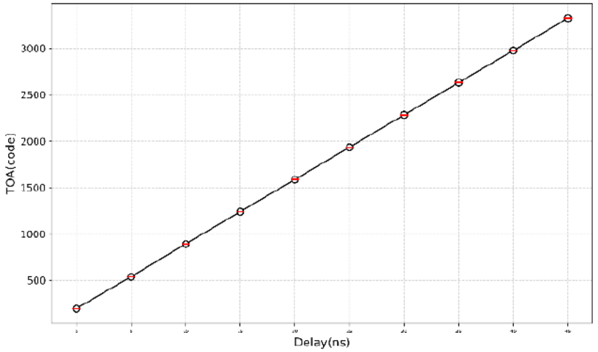
# Preliminary test for FPMROC_8CH



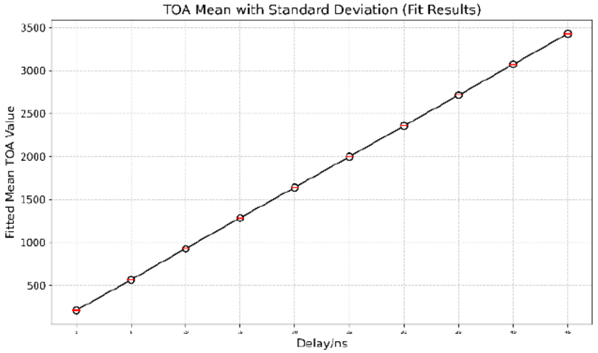

IN0 step: 5ns LSB: 14.14ps



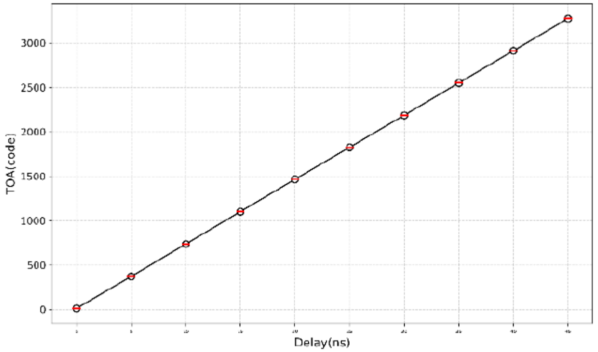

IN1 step: 1ns LSB: 14.04ps



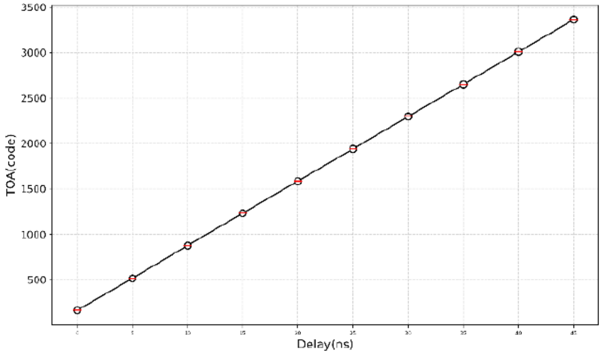

IN2 step： 5ns LSB: 14.30ps



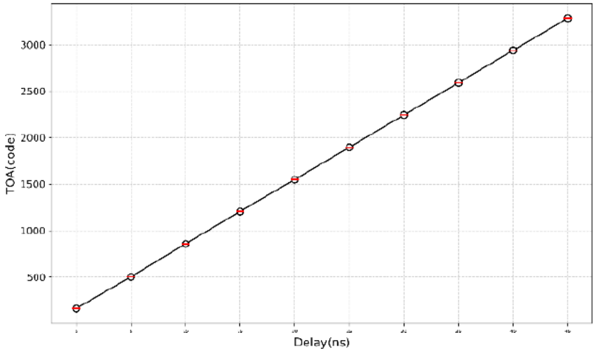

IN3 step： 5ns LSB: 13.96ps



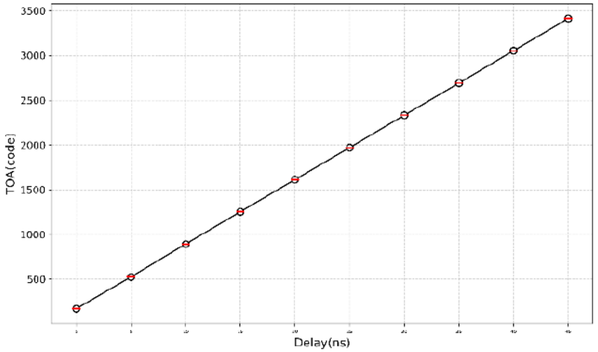

IN4 step： 5ns LSB: 13.78ps




IN5 step： 5ns LSB: 14.07ps




IN6 step： 5ns LSB: 14.41ps




IN7 step： 5ns LSB: 13.87ps

# Conclusion and outlook for FPMROC

- A coincident time resolution of 45.8 ps is achieved with MCP-PMT+ FPMROC chip
- FPMROC achieves LSB <14 ps, but with large SSP (~23 ps), should be improved in future.
- FPMROC_8CH still need more time to test.
- Power consumption is the bottleneck for multi-channel integration of low power application, but 16-channel chip is planned.
- Fast Serializer may not necessary for low event rate application, add choice of slowdown.

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# Thank you for your attention!