

May 21, 2026

Constant Fraction Discriminator Readout Chip (FCFD)

Artur Apresyan
FEE 2026

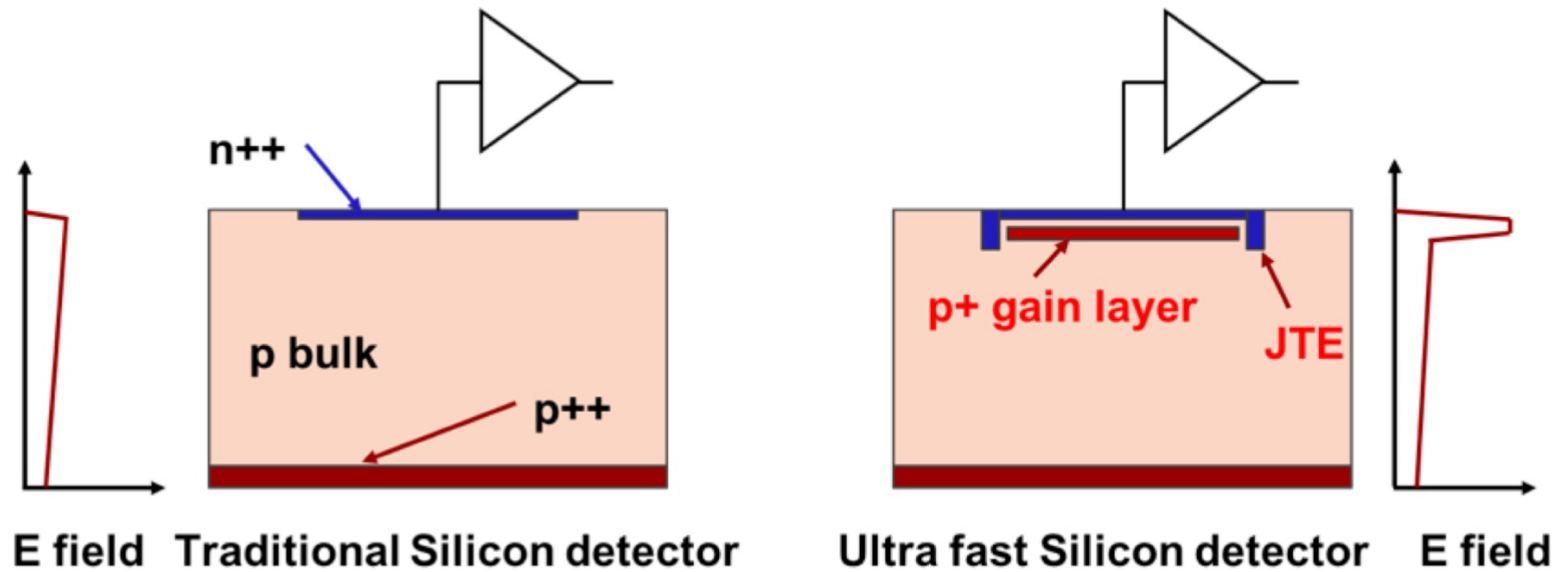


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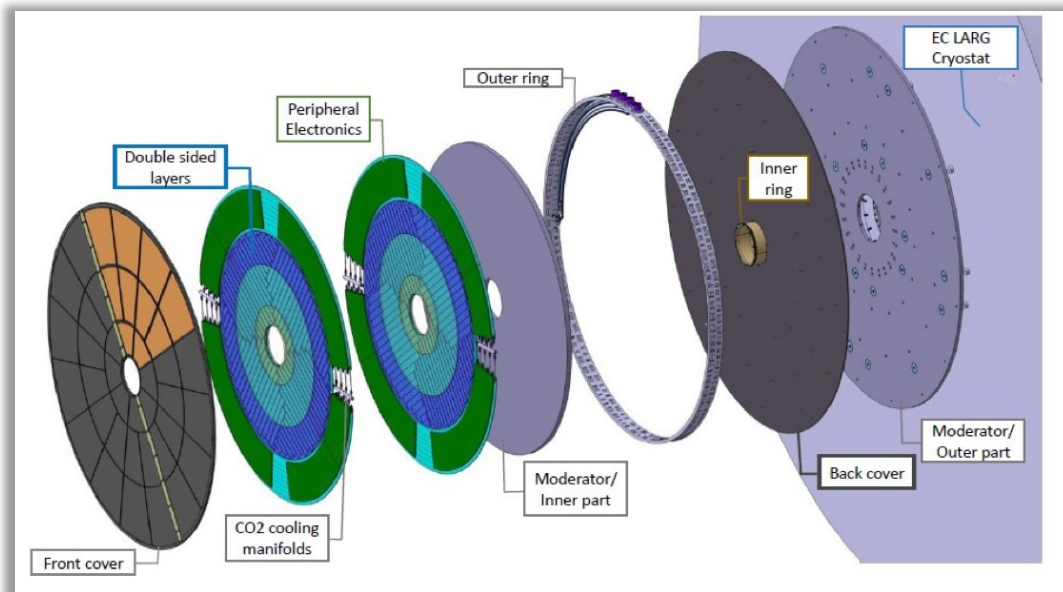
Low-Gain Avalanche Diode (LGAD) sensors

- Breakthrough development of last decade
 - High field in gain region ~ 300 kV/cm, causes avalanche
 - High gain \rightarrow high signal \rightarrow faster rise \rightarrow smaller "jitter"

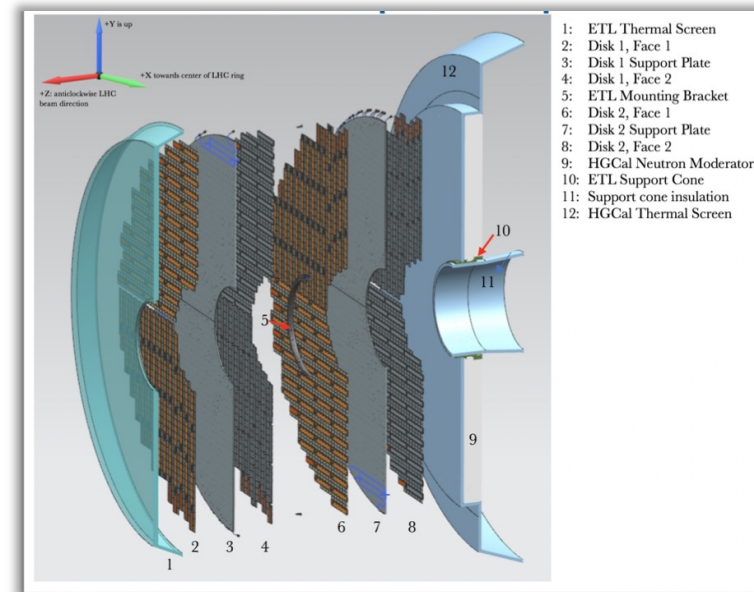


✚ First large-scale application of LGADs

- CMS and ATLAS experiments are building the **1st generation of 4D-trackers**
 - Endcap Timing Layer (**ETL**) and High Granularity Timing Detector (**HGTD**)
- Timing information with 35 ps resolution per track
 - Around **8 million** channels ($1.3 \times 1.3 \text{ mm}^2$) covering **$\sim 10 \text{ m}^2$** surface area
 - **Synchronized** precision timing over tens of thousands of chips, across large area



HGTD at ATLAS



ETL at CMS

Looking into the future

- Improve 4D-trackers to achieve 100% fill factor, and high position resolution
 - CMS/ATLAS LGADs have an irreducible dead-area of 100 μm
- New development: AC-LGADs developed to address limitations of DC-LGADs
 - **100% fill factor**, and **fast timing** performance

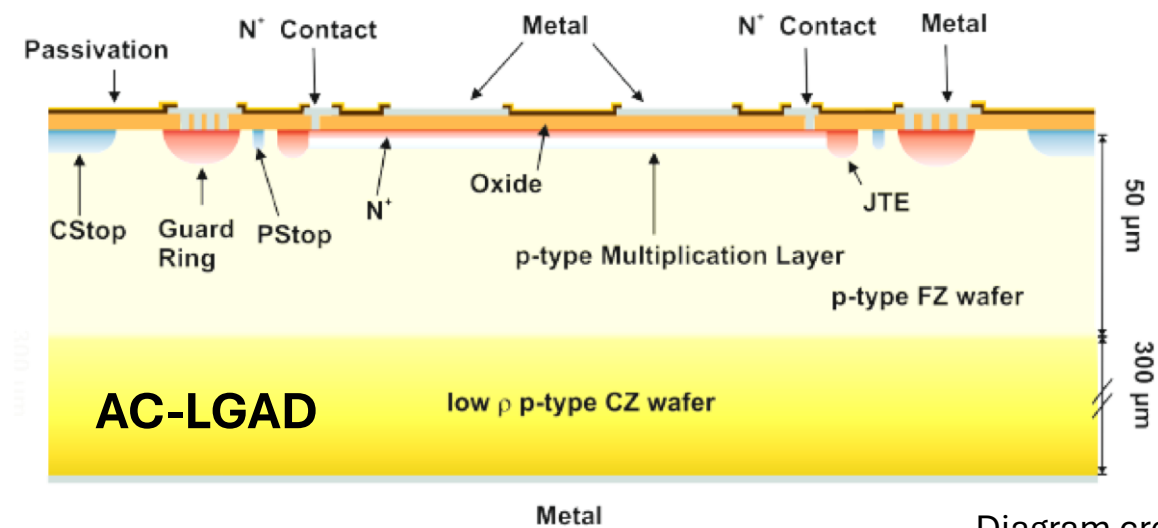
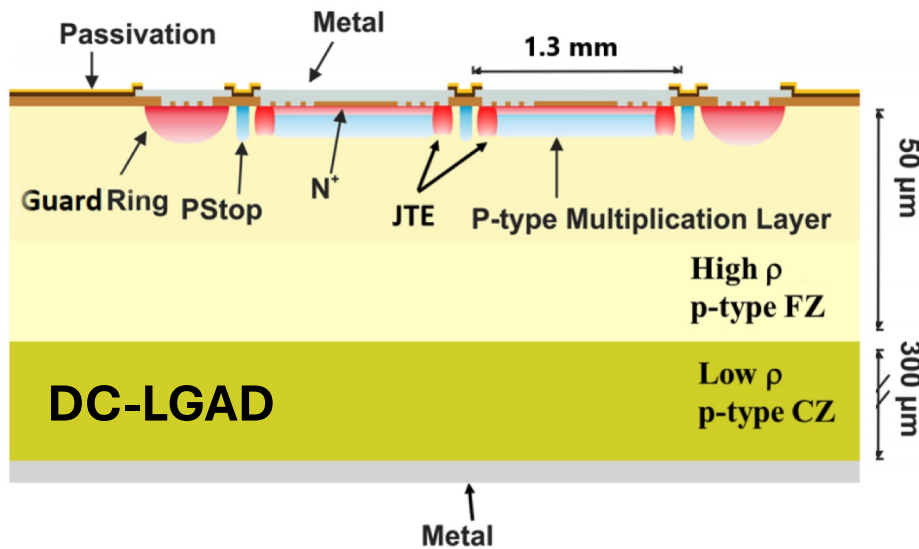
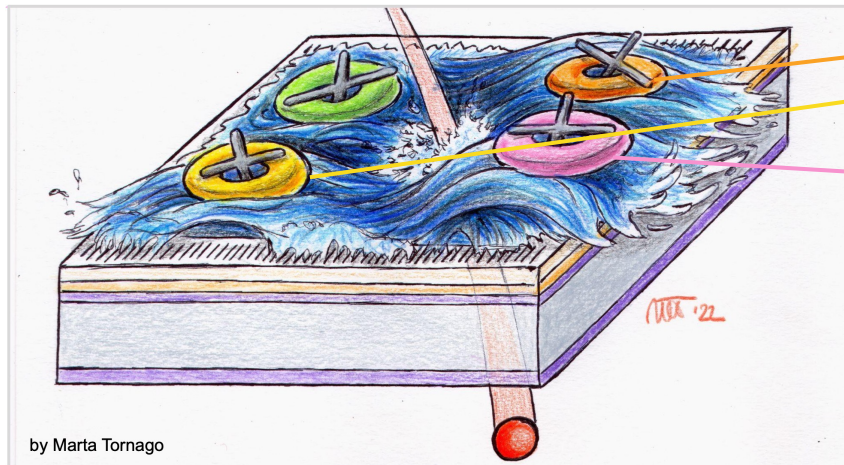


Diagram credit: CNM

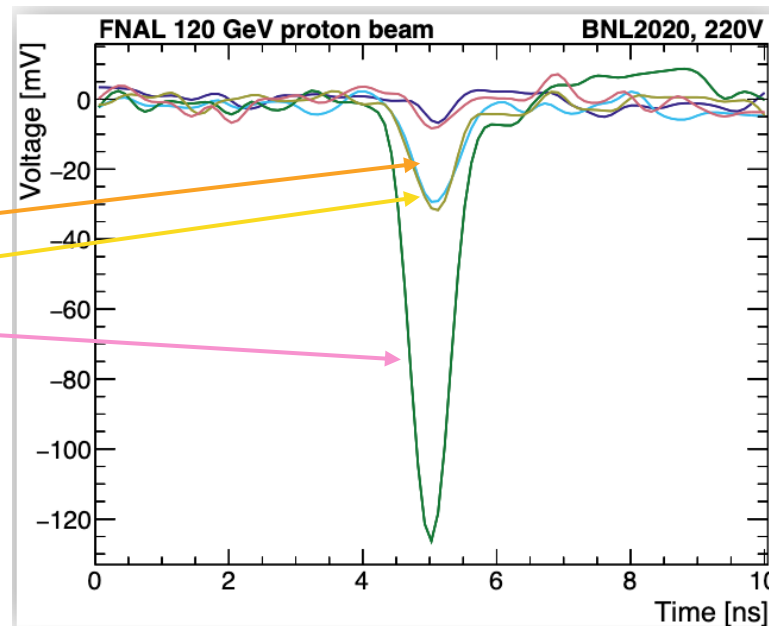
AC-coupled LGADs

- Improve 4D-trackers to achieve 100% fill factor, and high position resolution
 - CMS/ATLAS LGADs have an irreducible dead-area of 100 μm
- New development: AC-LGADs developed to address limitations of DC-LGADs
 - **100% fill factor**, and **fast timing** performance

Artist's impression of an AC-LGAD



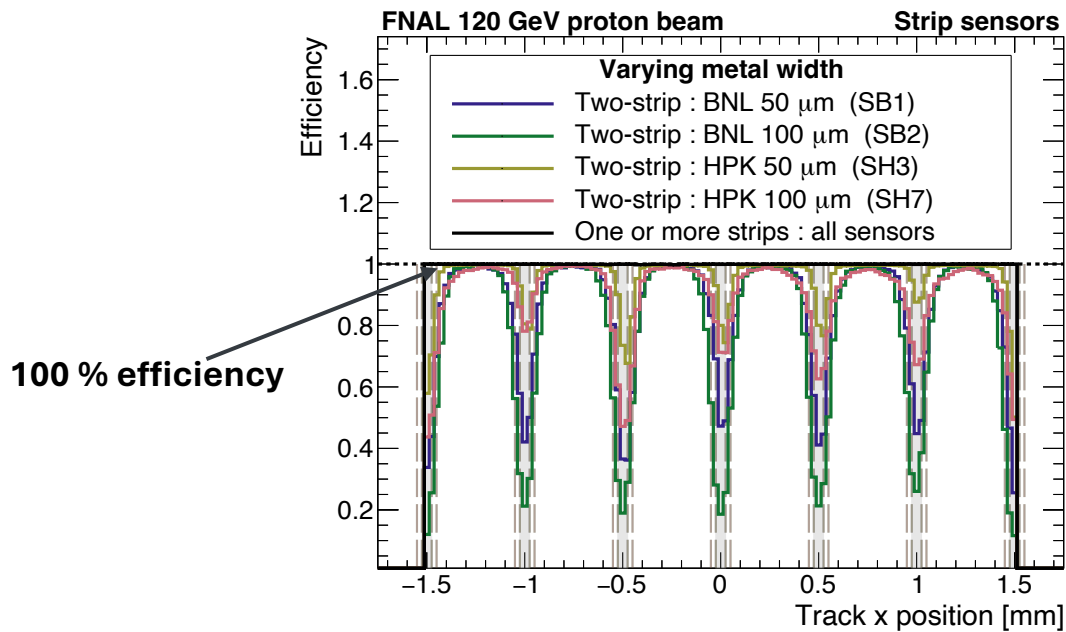
by Marta Tornago



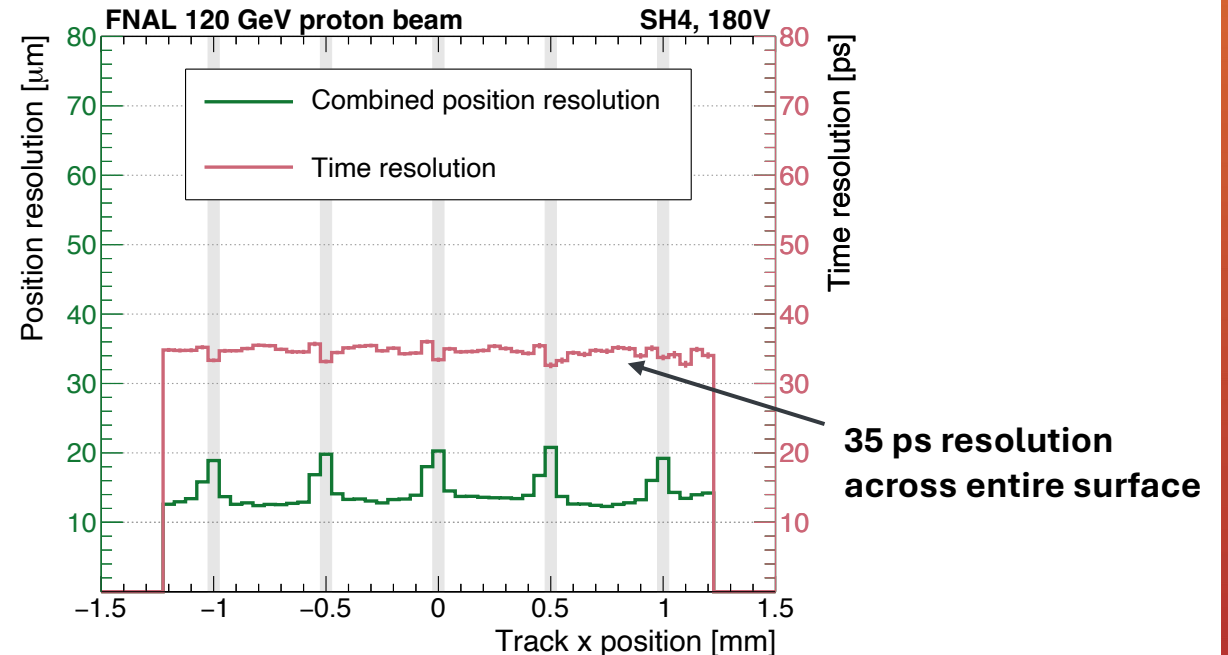
- Large signal in the **primary channel**,
- Shared charge appears in the **neighboring channels**

AC-LGADs sensor optimization

- Position reconstruction
 - Achieve 15-20 μm resolution in 10mm strips, 500 μm pitch
- Excellent time resolution
 - Achieve 30-35 ps for 10 mm strips



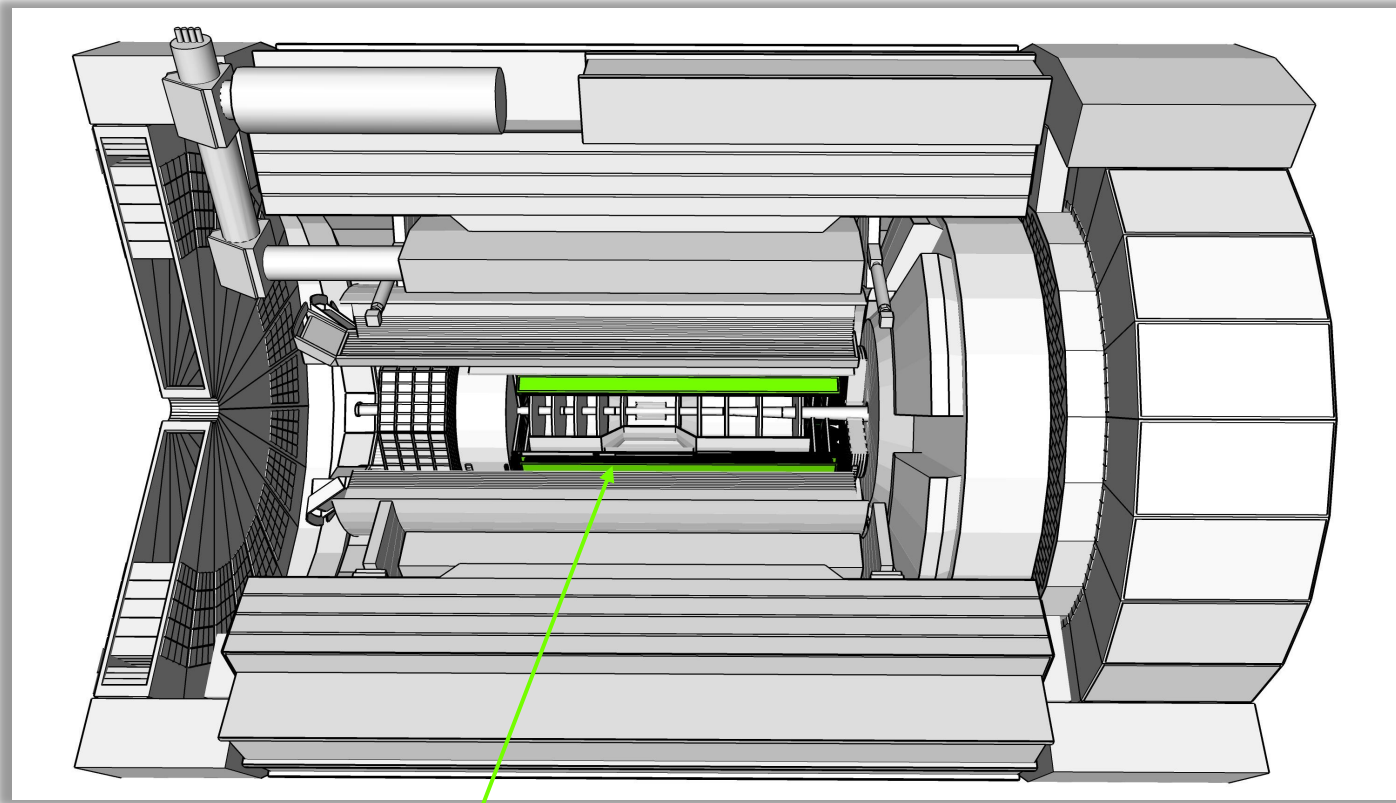
Detection efficiency across surface



Position and Time resolutions across surface

Applications of AC-LGAD sensors

- The ePIC detector is a multipurpose collider detector for EIC
 - Need particle ID down to low energies and across all rapidities
 - First applications of **strip AC-LGADs**; pixel AC-LGAD in the forward region



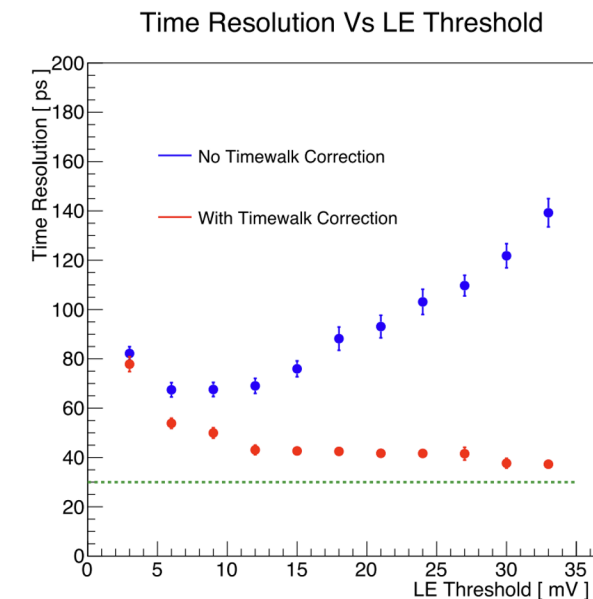
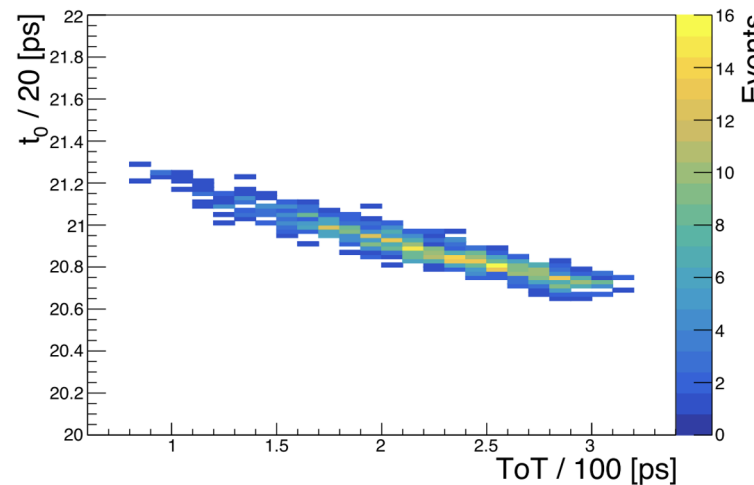
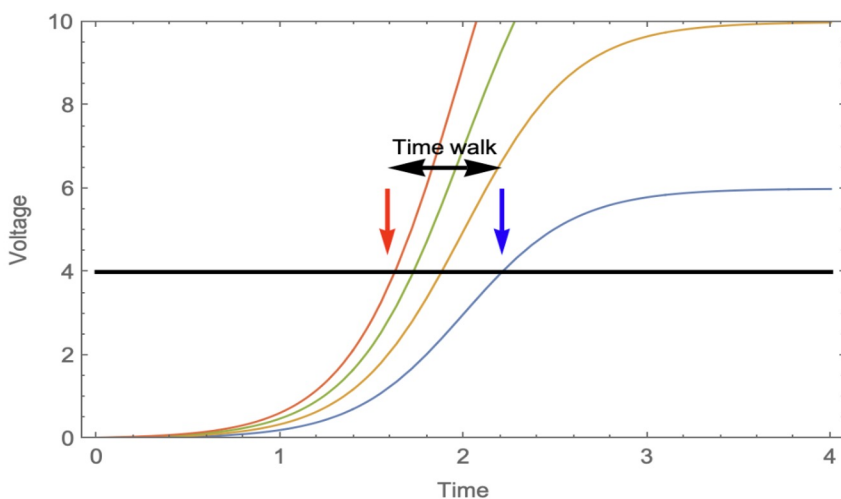
bTOF detector within the ePIC experiment

Constant Fraction Discriminator

- A robust fast-timing measurement technique
- CFD approach achieves excellent performance, especially for low S/N systems, such as LGADs

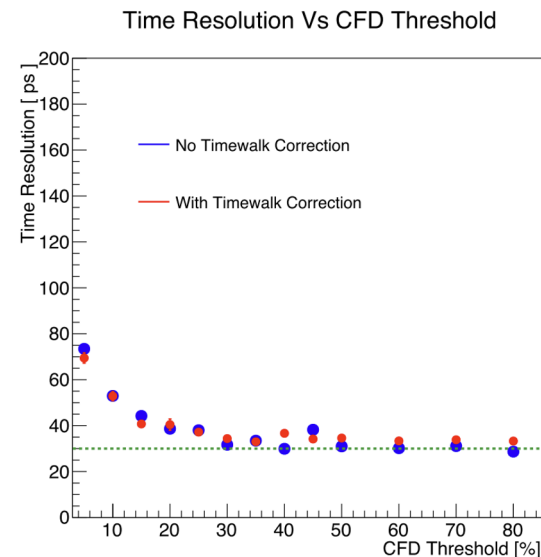
C.Pena et al., **NIM A 940 (2019), pp (119-124)**

- Time-walk effect is well known & must be corrected for best performance
- Conventionally addressed with online or offline corrections via some type of LUT



Constant Fraction Discriminator

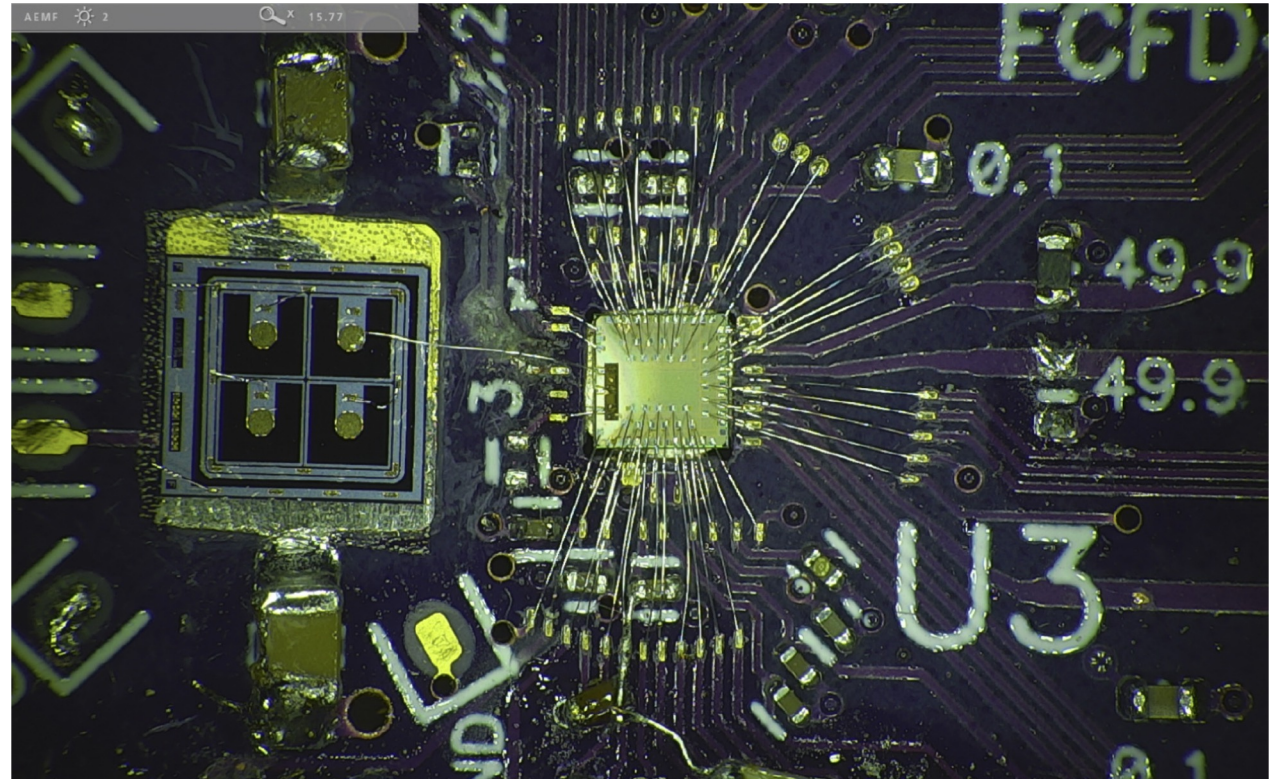
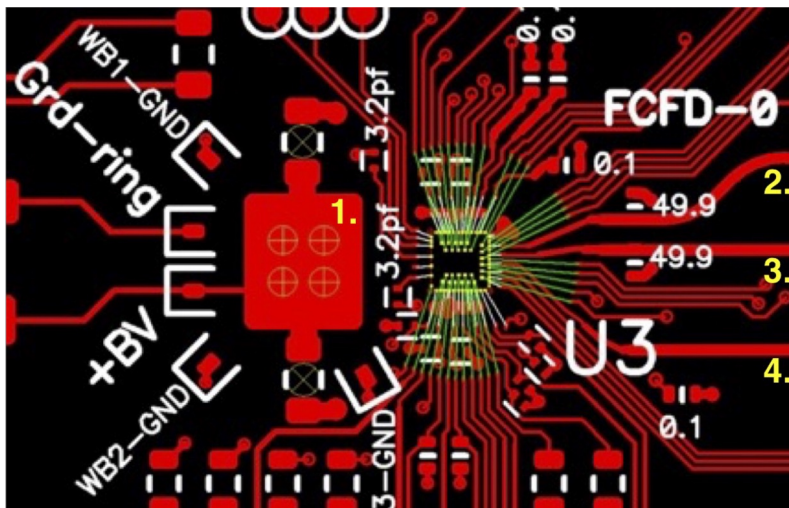
- A robust fast-timing measurement technique
- CFD approach achieves excellent performance, especially for low S/N systems, such as LGADs C.Pena et al., **NIM A 940 (2019), pp (119-124)**
- CFD-based readout is simple in operation and maintenance
- No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc
- A hardware-enabled correction via CFD built into the readout ASIC design offers much simpler solution



FCFD Readout for Timing Detectors

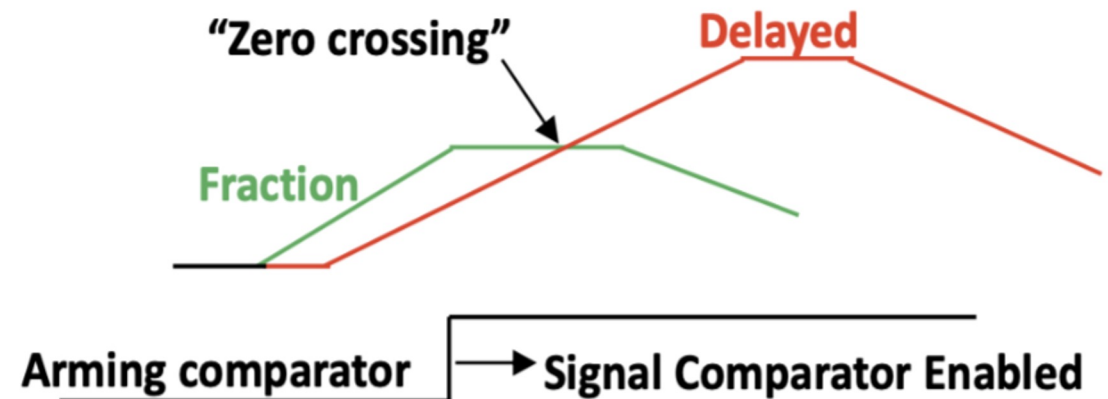
- FCFD readout chip started initial development in 2021
- Originally intended for (AC-)LGAD sensors for MIP signals
- But can be adapted for many types of precision timing detectors

FCFD v0



FCFD Readout for Timing Detectors

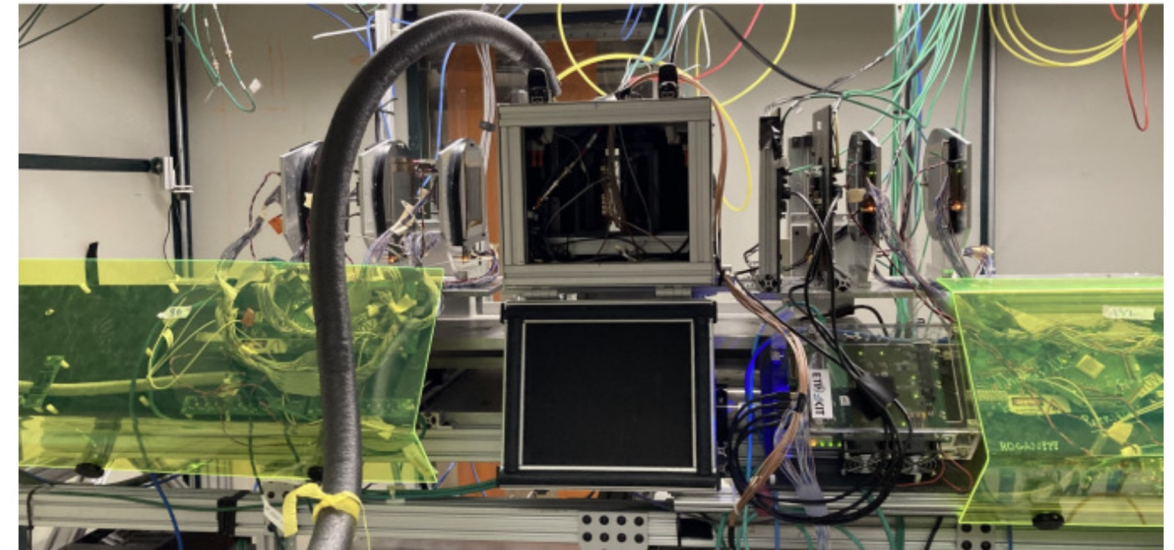
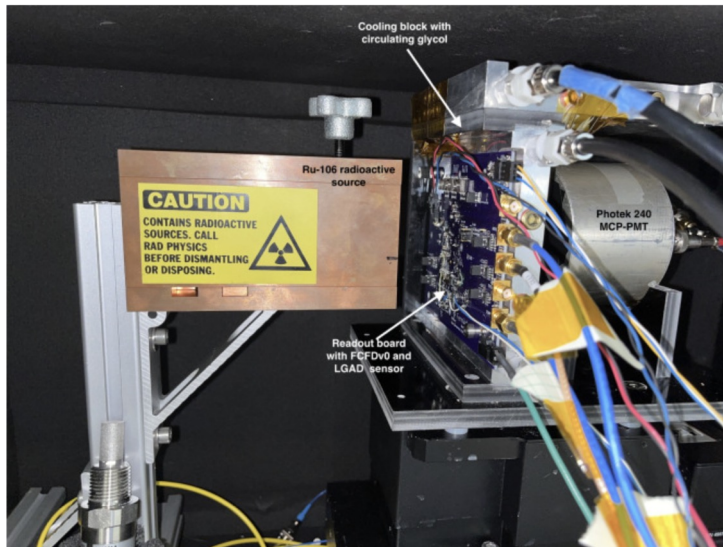
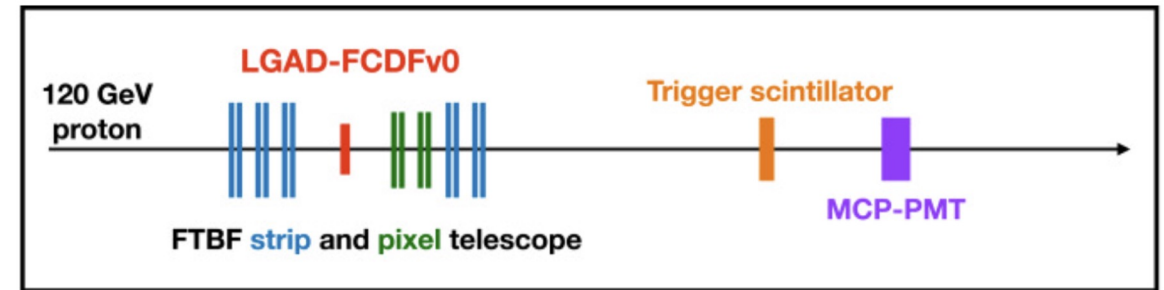
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 - But can be adapted for many types of precision timing detectors
-
- Main features include:
 - Integrator & Follower to create the “fraction” signal
 - Comparator for “arming” and timestamping



S. Xie et. al, *NIM A* 1056, 2023, p168655
<https://doi.org/10.1016/j.nima.2023.168655>

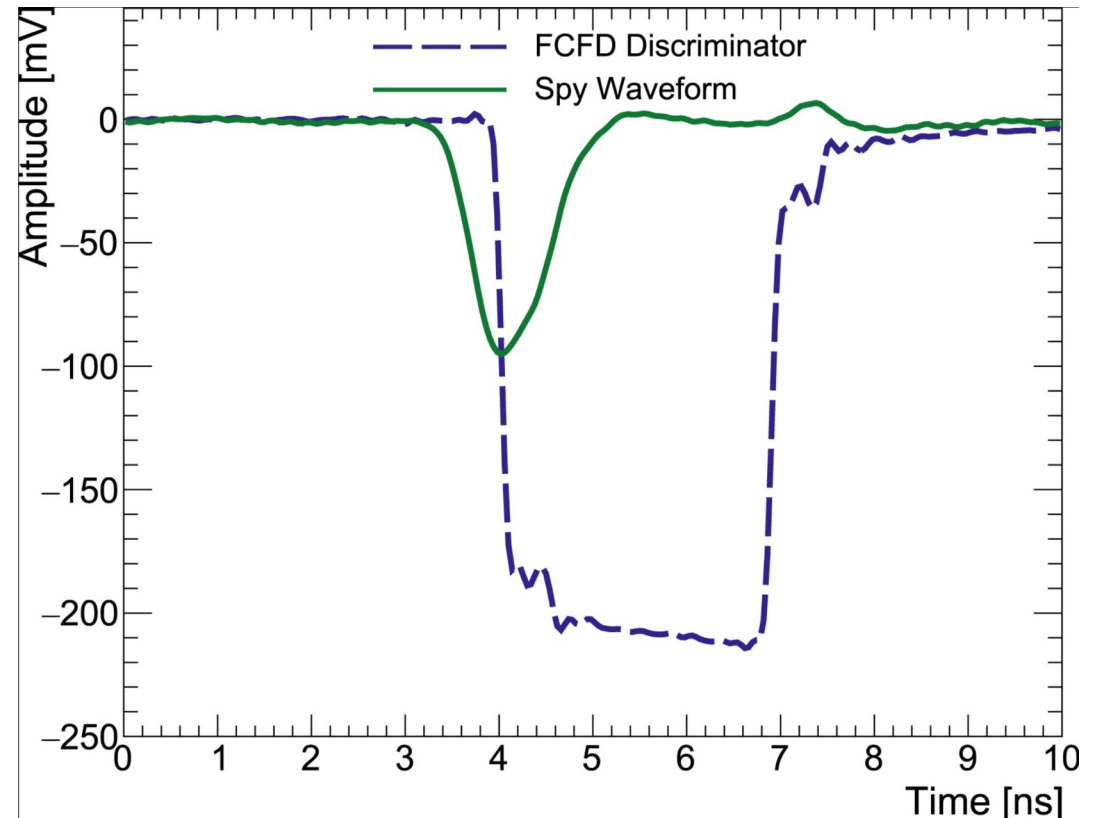
FCFD0 prototype

- FCFD0 performance evaluated using multiple types of signals:
 - Charge-injected signal
 - Picosecond Laser signal
 - Radioactive Source signal
 - Proton Beam signal



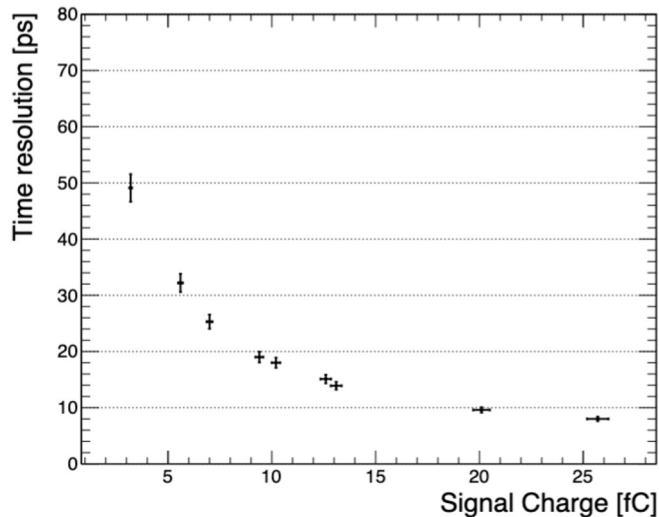
FCFD0 prototype

- FCFD0 performance evaluated using multiple types of signals:
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 - Proton Beam signal
- FCFD0 also featured several integrated characterization and testing functions:
 - A spy waveform
 - Internal charge injection

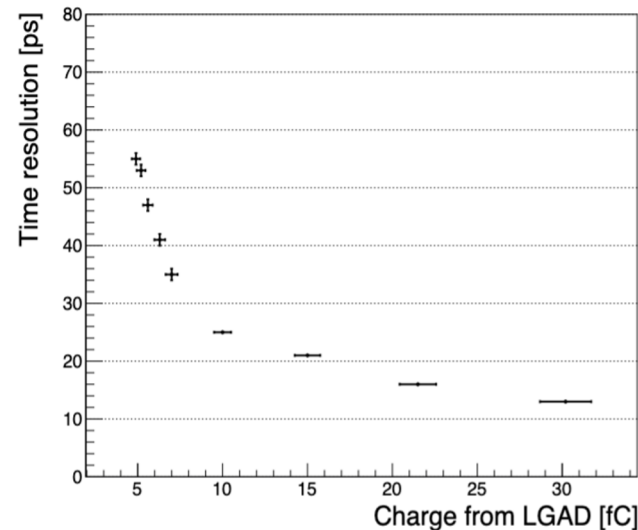


FCFD0 prototype

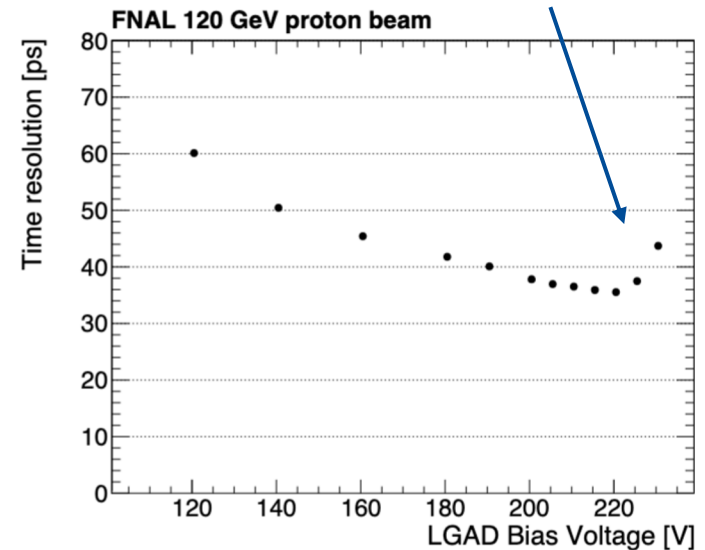
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Charge Injection: intrinsic jitter



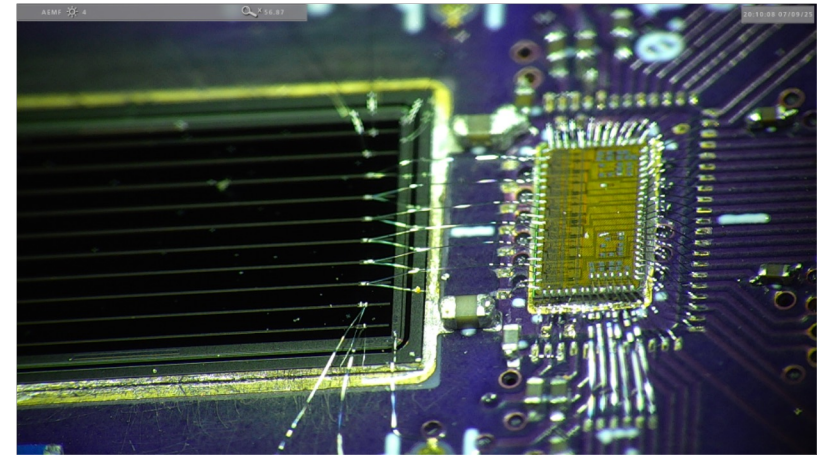
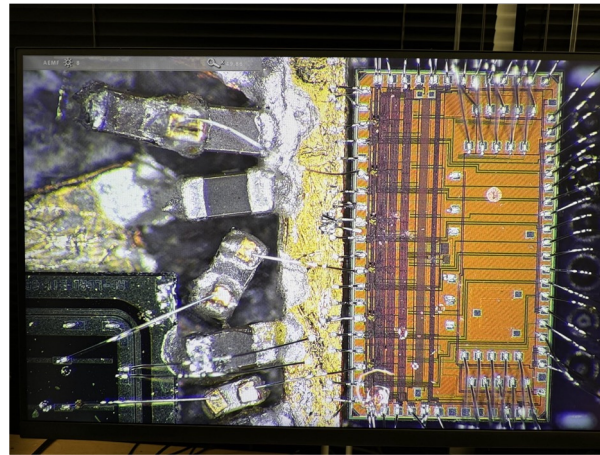
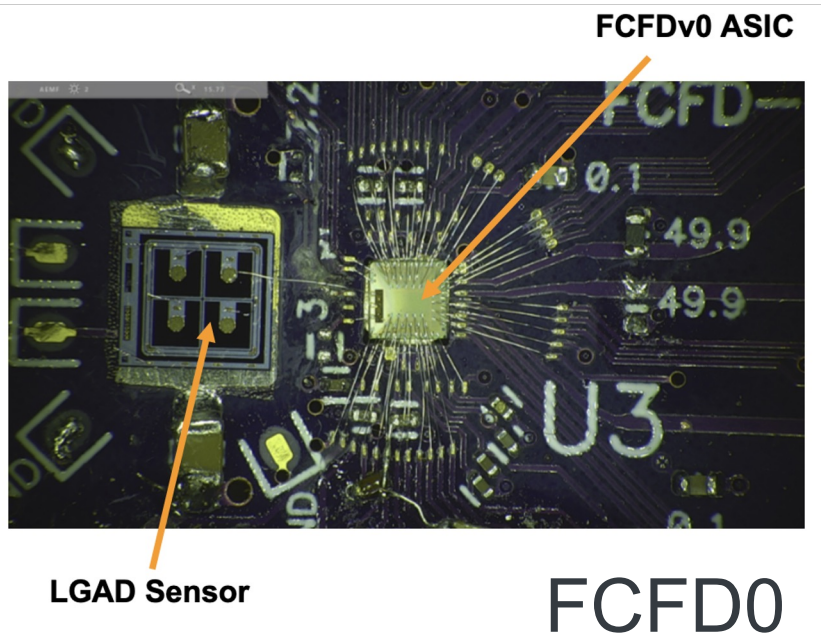
Laser signal on LGADs



Test beam in FNAL

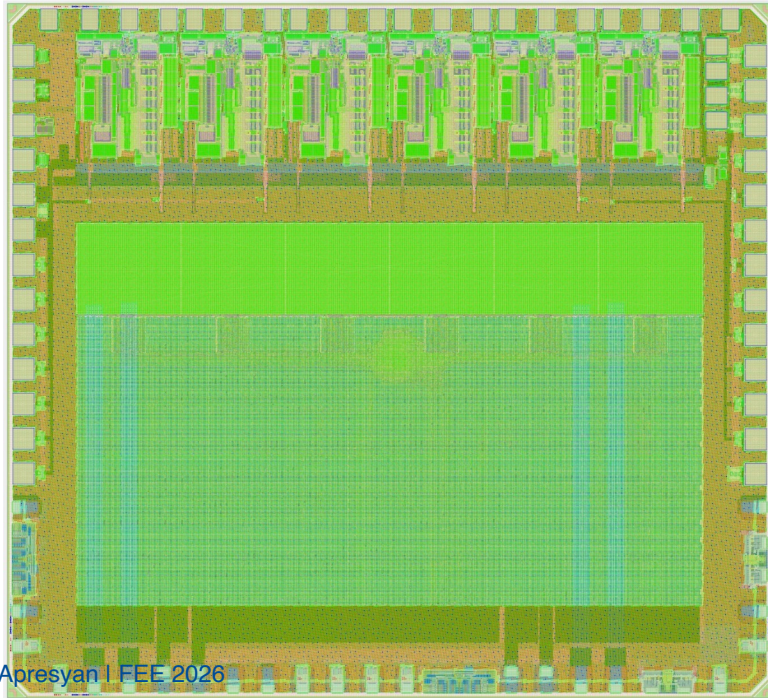
FCFD : A Historical Perspective

- Several versions of the FCFD chip produced, in TSMC 65 nm node
 - FCFD0 : (2021) - first prototype to implement CFD
 - FCFD1 : (2024) - optimized for strip AC-LGAD incl. position reconstruction
 - FCFD1.1: (2025) - optimized for 1-cm AC-LGAD with tunable thresholds



FCFD : A Historical Perspective

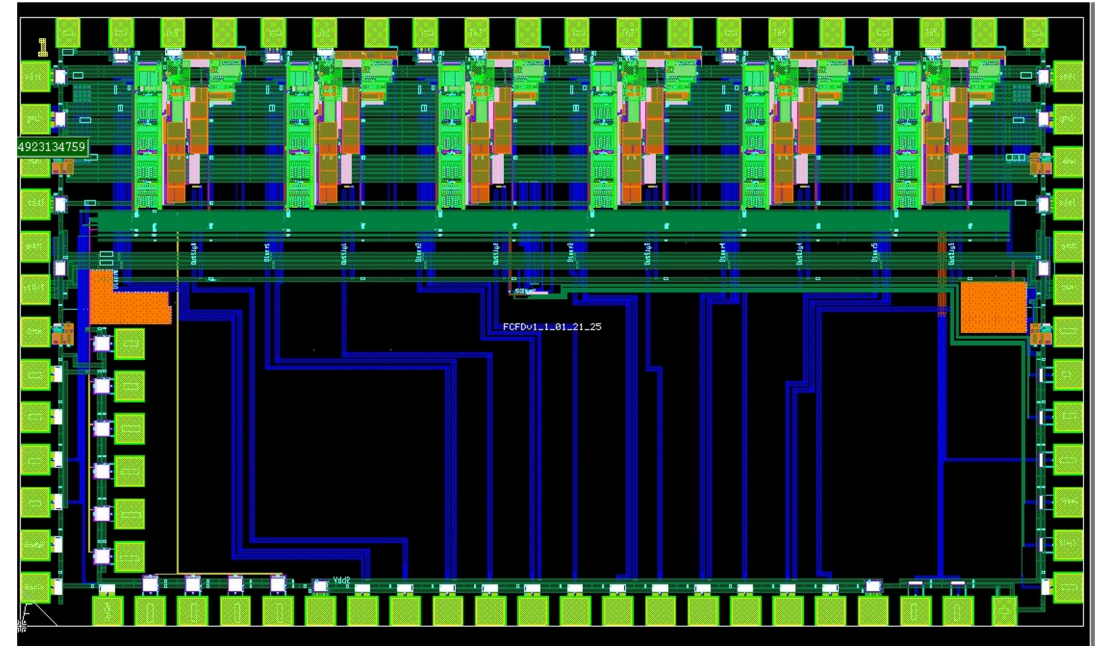
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 - FCFD1.1: (2025) - optimized for 1-cm AC-LGAD with tunable thresholds
 - FCFD1.2: (2026) - first full chip optimized for ePIC Barrel TOF



FCFD1.2 currently in fabrication

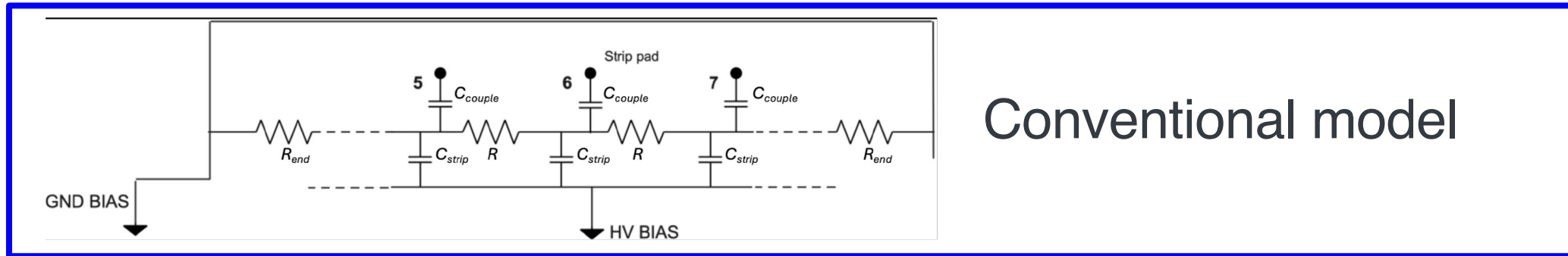
FCFD1.1 prototype

- Co-designed with the following specifications in mind:
 - 50 μm thick AC-LGAD sensor
 - 1cm long strip,
 - 500 μm pitch,
 - 50 μm wide metal strips
 - Signal Characteristics:
 - Signal MPV : 25 fC
 - Dynamic range: 10 - 70 fC;
 - Occupancy: O(10) Hz per channel



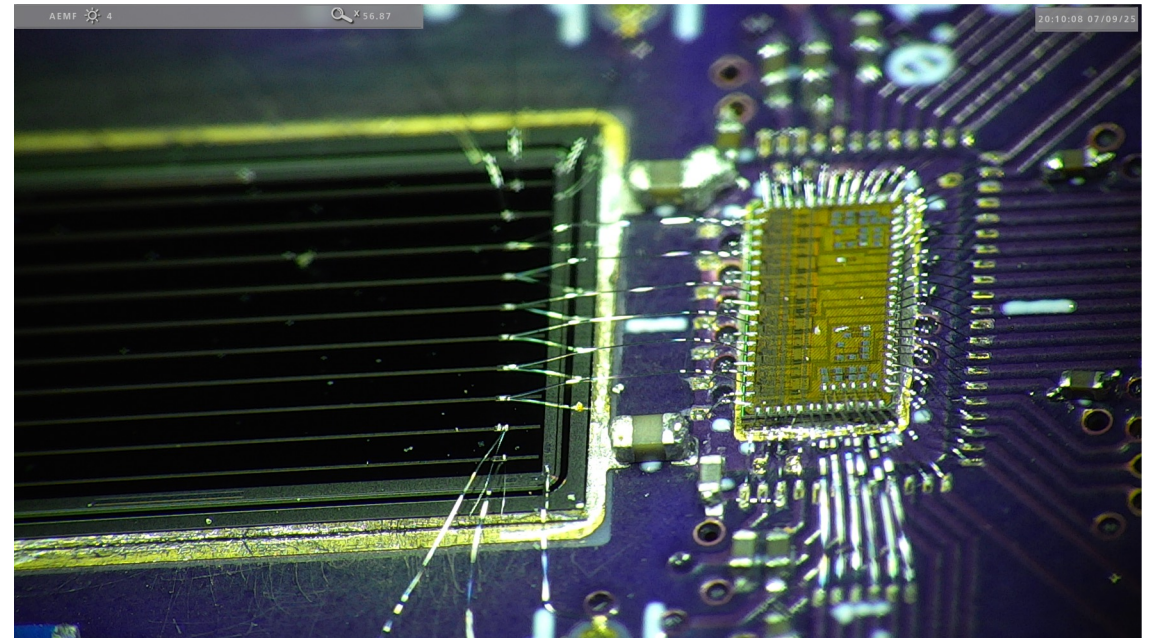
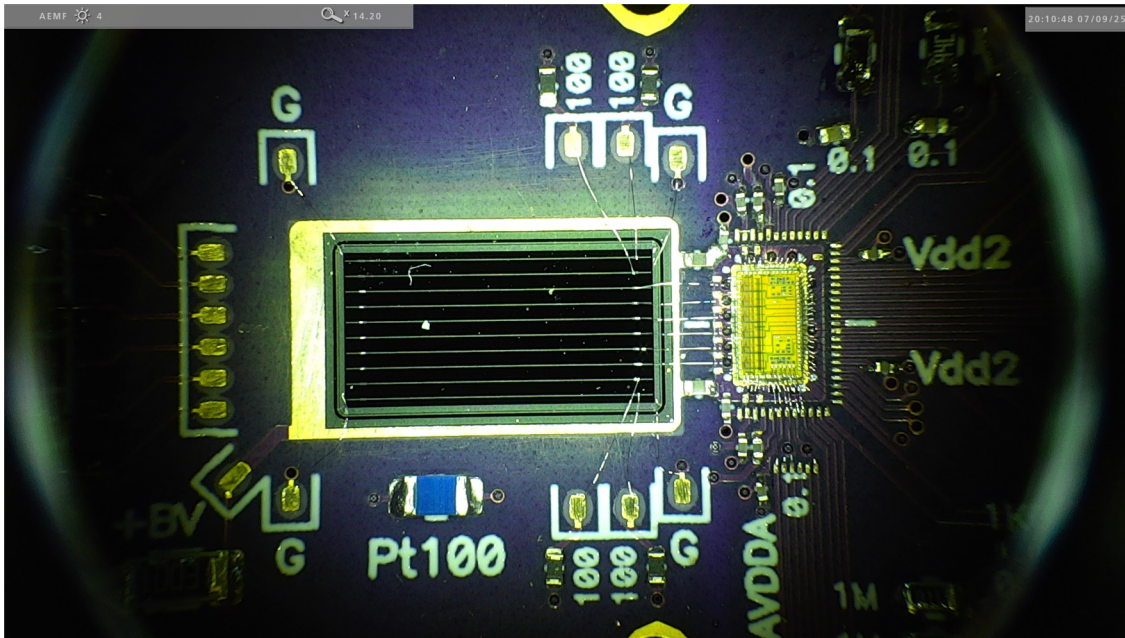
AC-LGAD Sensor Network

AC-LGAD sensors are more complex than conventionally assumed



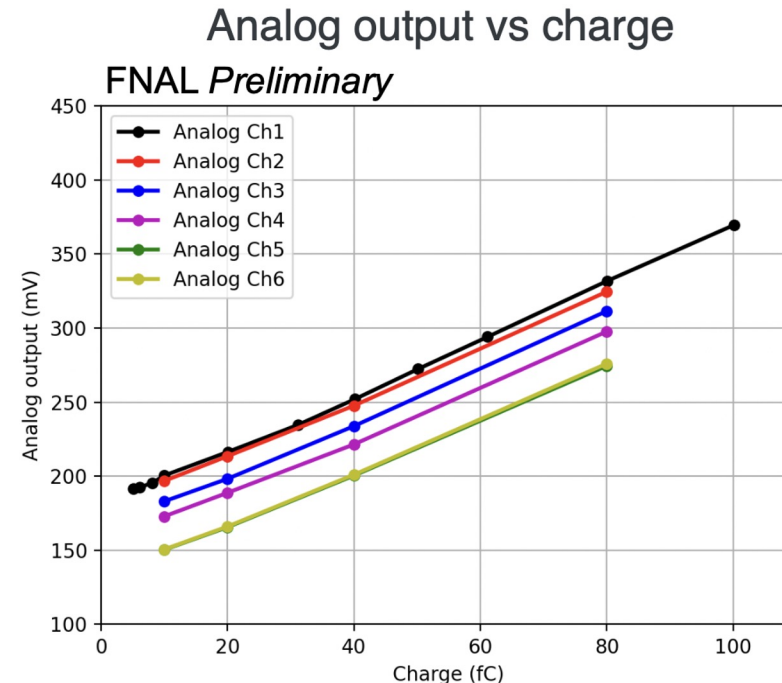
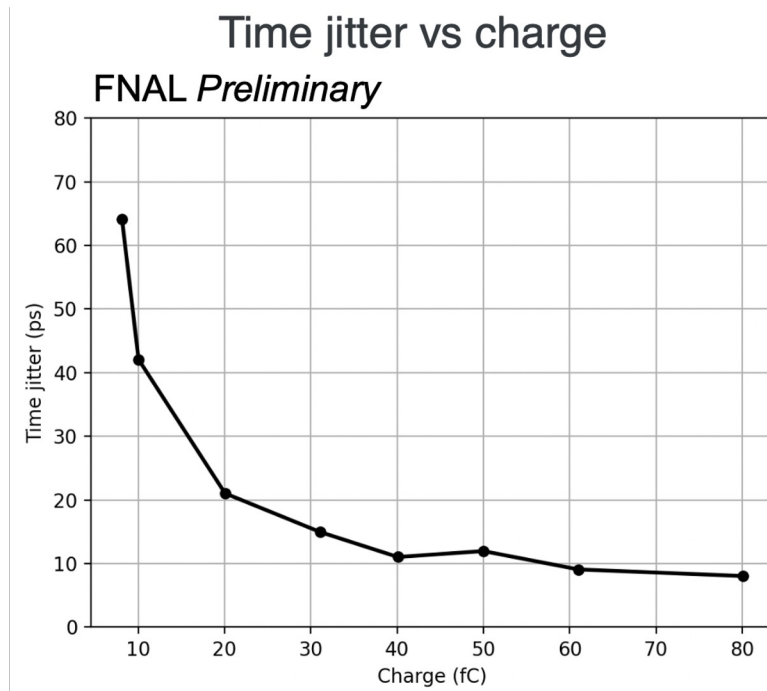
FCFD1.1 prototype

- Fully analog readout: discriminator and amplitude output, read out by oscilloscope
- Design was **submitted on Feb 19, 2025**, received in **June 2025**.
- Wirebonded to a HPK 1-cm strip sensors, 6 strips connected



⚙️ Laboratory Measurements of FCFD1.1

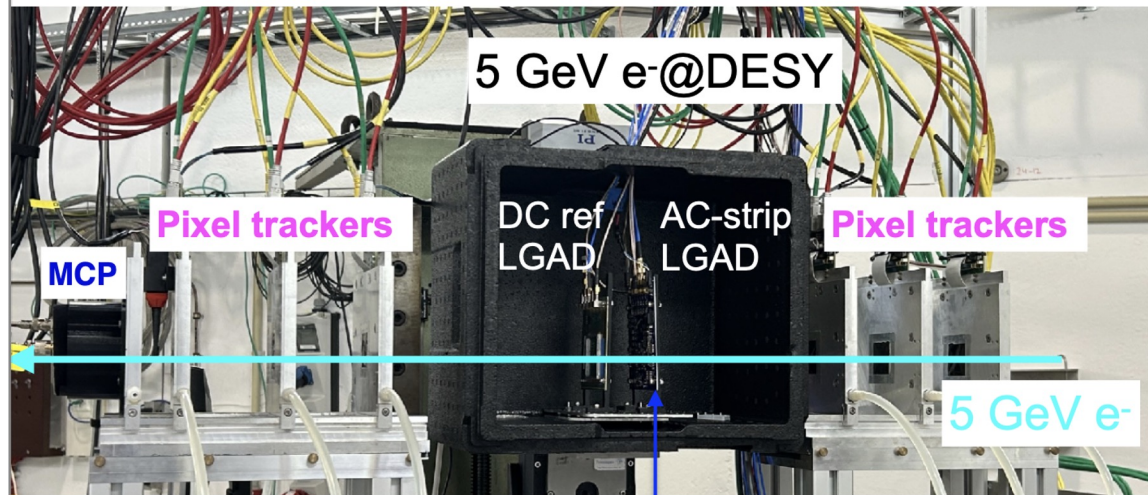
- Charge injection measurements:
 - Jitter measurements consistent with simulation and specs
 - Amplitude measurements: all channels behave as expected, linear in the range



A. Apresyan et al., NIM A 1089 (2026) 171599

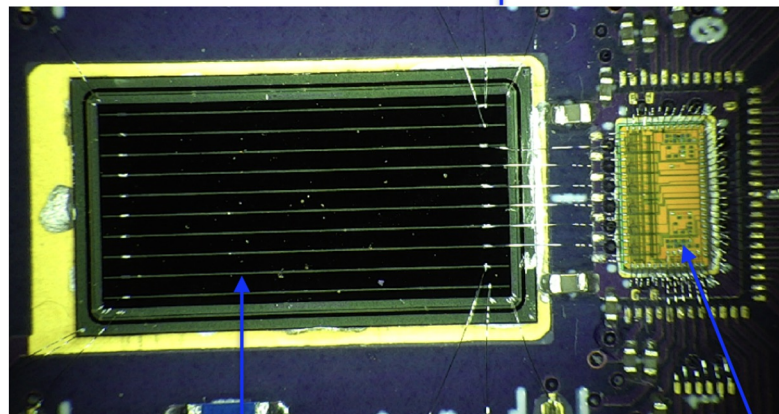
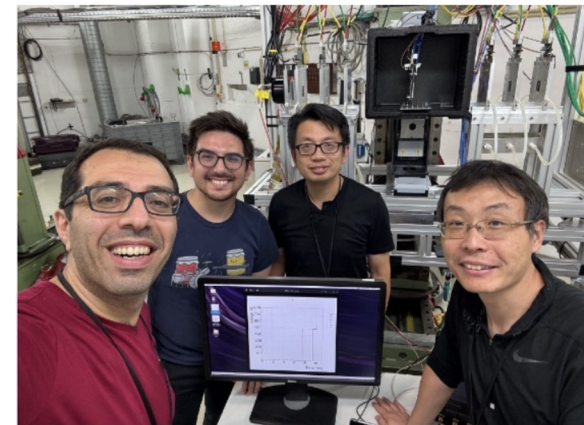
FCFD1.1 Testbeam Measurements

- Test-beams in summer 2025 at DESY (5GeV e-) and CERN (120GeV p)



- Tracking with $\sim 5 \mu\text{m}$ resolution
- Time reference detector with $\sim 10 \text{ ps}$ resolution (MCP)
- DAQ: high bandwidth, high ADC resolution 8-channel scope

crew@DESY (July, 2025)

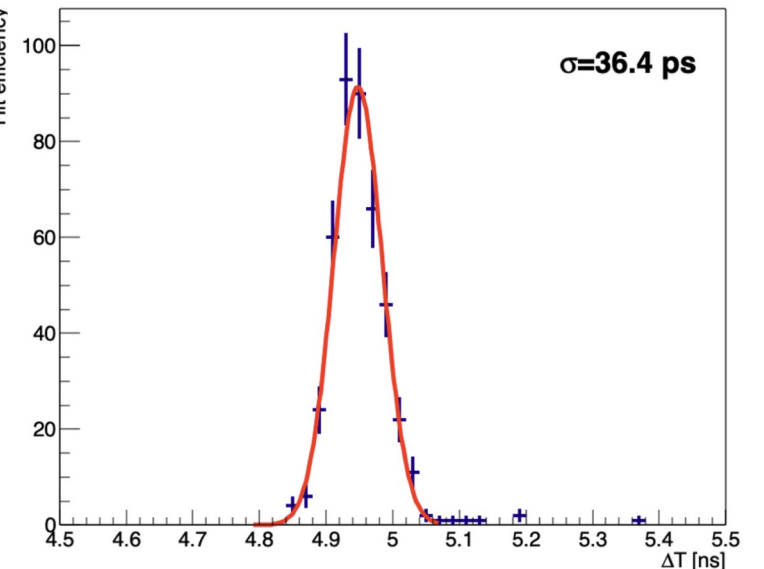
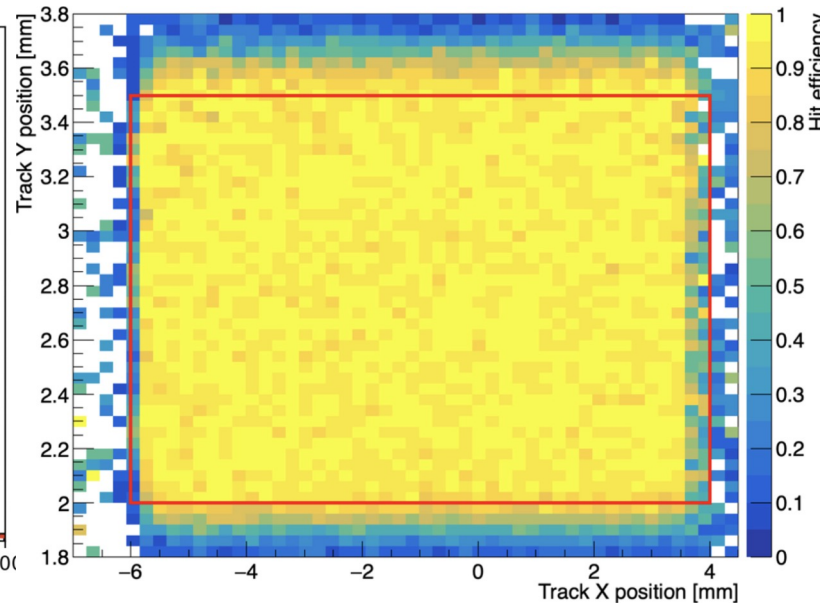
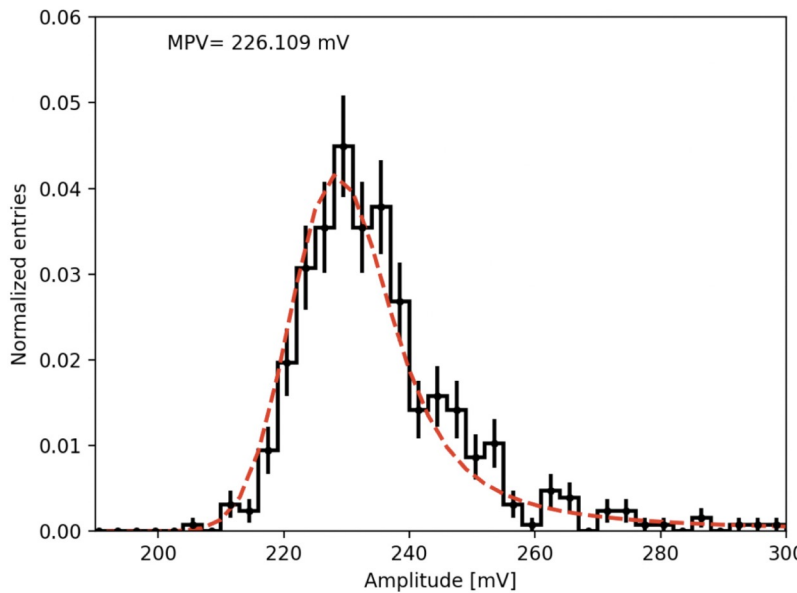


1cm strips, 500um pitch, 50um metal electrode, 50um thick

FCDF-V1.1

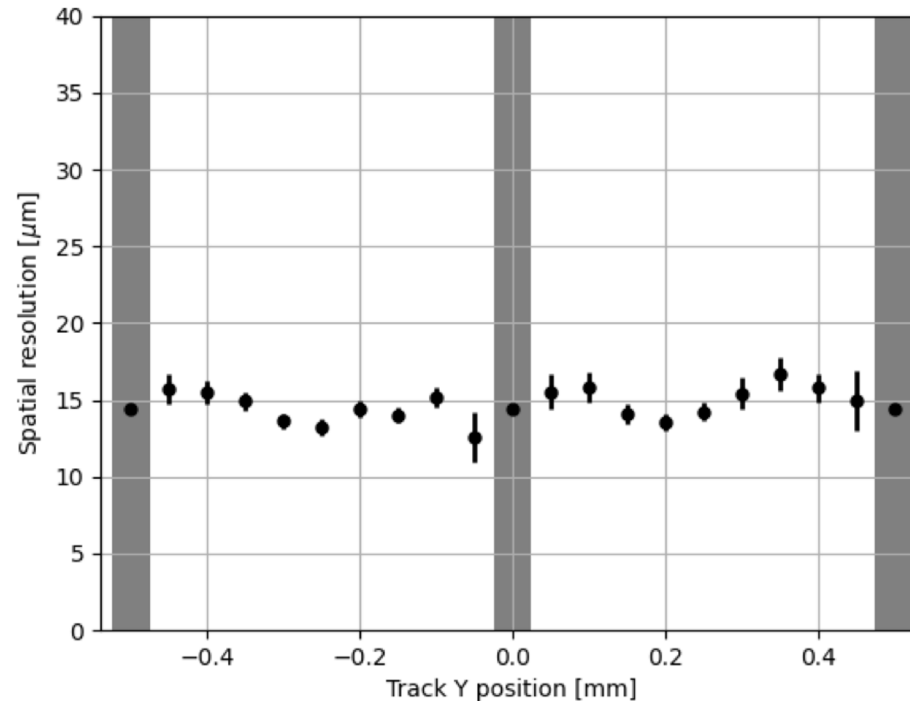
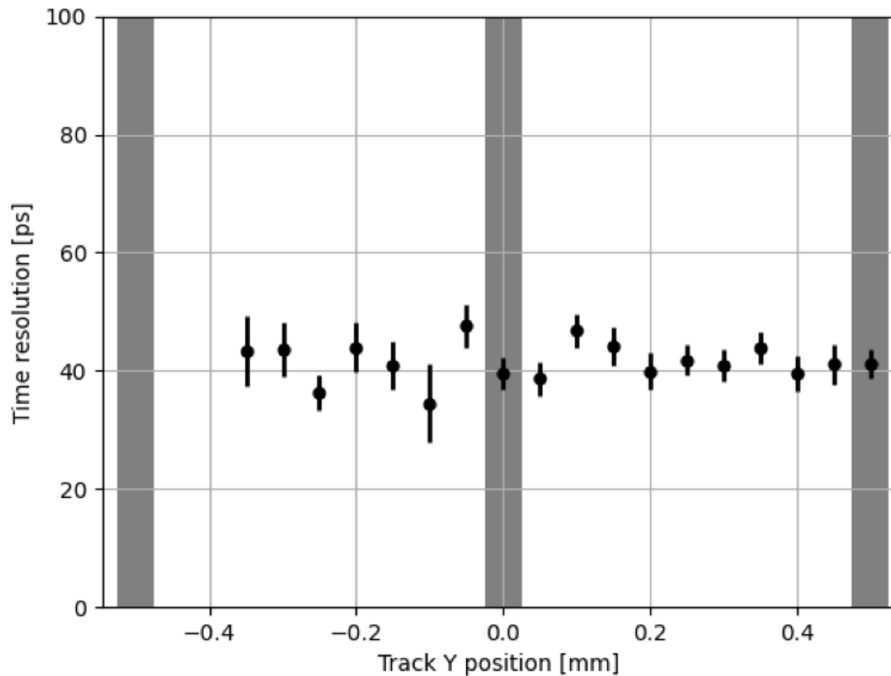
FCFD1.1 Testbeam Measurements

- Validated some basic characteristics
 - Signal amplitude
 - Efficiency
 - Time response



FCFD1.1 Testbeam Measurements

- Characterized timing and spatial measurement performance
 - Measured **time resolution** ~ 40 ps across sensor surface
 - Measured **spatial resolution** ~ 15 - 20 μm



FCFD Next Steps & Development Plan

- FCFD1.2 submitted in April 2026:
 - First full-functionality chip:
 - Implements TDC, ADC, I2C, and simplified readout on a **6-channel** chip
 - Goals: test and verify the new TDC and ADC; enable testing of the full system-chain
- FCFD2 will be the first full functionality, full-size **32-channel** chip
 - Receive near the end 2027
- FCFD3: final version
 - Receive near the end 2028



Timing and Position Resolution Specifications

- Components that go into overall timing:

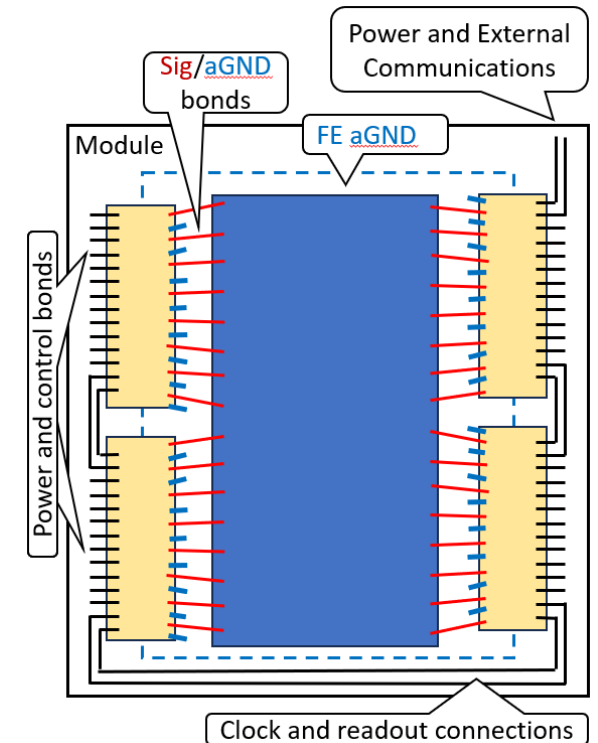
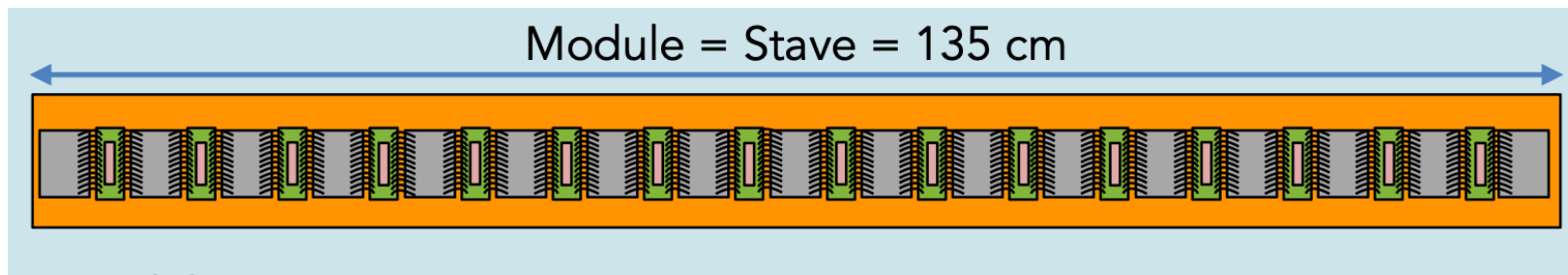
- $\sigma_T^2 = \sigma_{\text{LGAD}}^2 + \sigma_{\text{preamp/disc}}^2 + \sigma_{\text{Internal Clock}}^2 + \sigma_{\text{System Clock}}^2 + \sigma_{\text{TDC}}^2$

Component	Spec
LGAD+ preamp/discriminator	~40 ps
Internal clock distribution	< 10 ps
System clock distribution	< 10 ps
TDC binning	< 10 ps
Total	~ 45 ps

- Time resolution $\sigma_T \sim 45$ ps
- Position resolution:
 - 30 μm in polar angle: **5-bit ADC**

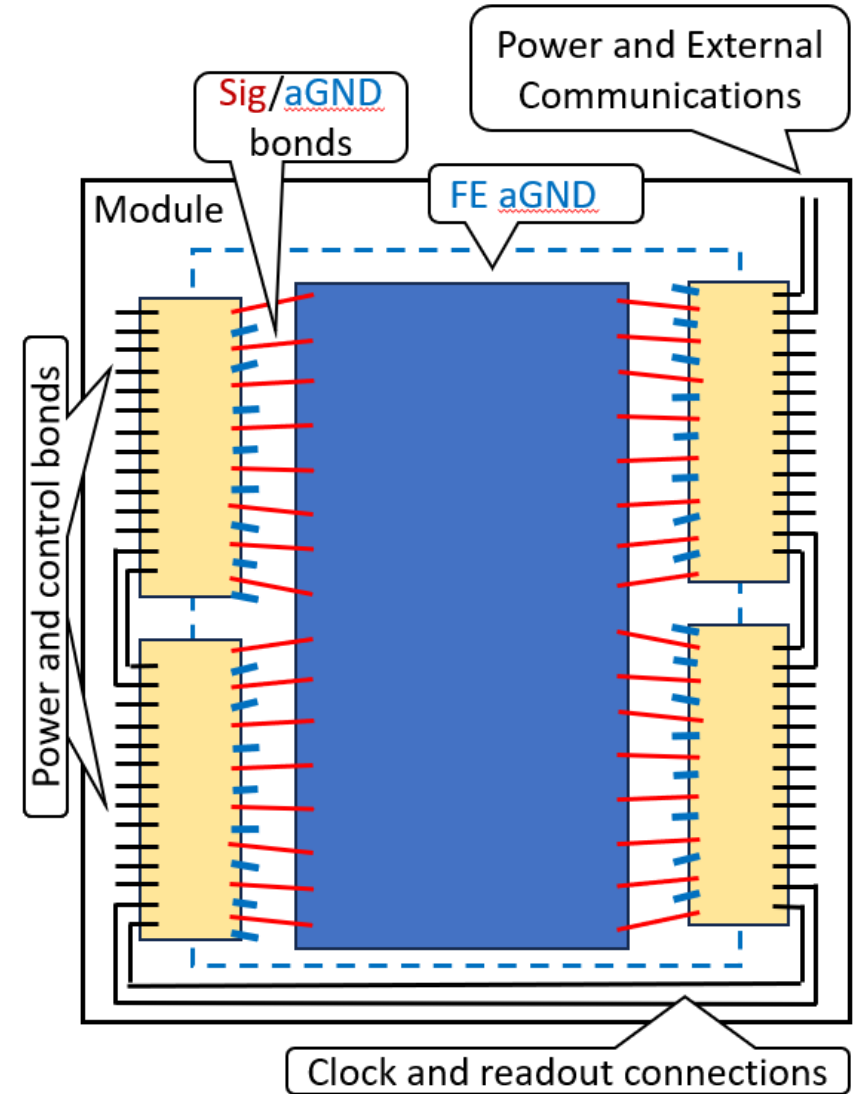
Physical interfaces and constraints

- Each sensor has 64x2 sets of strips, with 500 μm pitch
- Constraint from the system-side is to use single data line per sensor
 - Interface is **one IpGBT elink per 128 channels**
- Each sensor mounted on individual **modules**
- Voltage and current requirements
 - Need **2.5 V** and **1.2 V** voltages for the operation of analog
 - Need **1.2 V** for digital



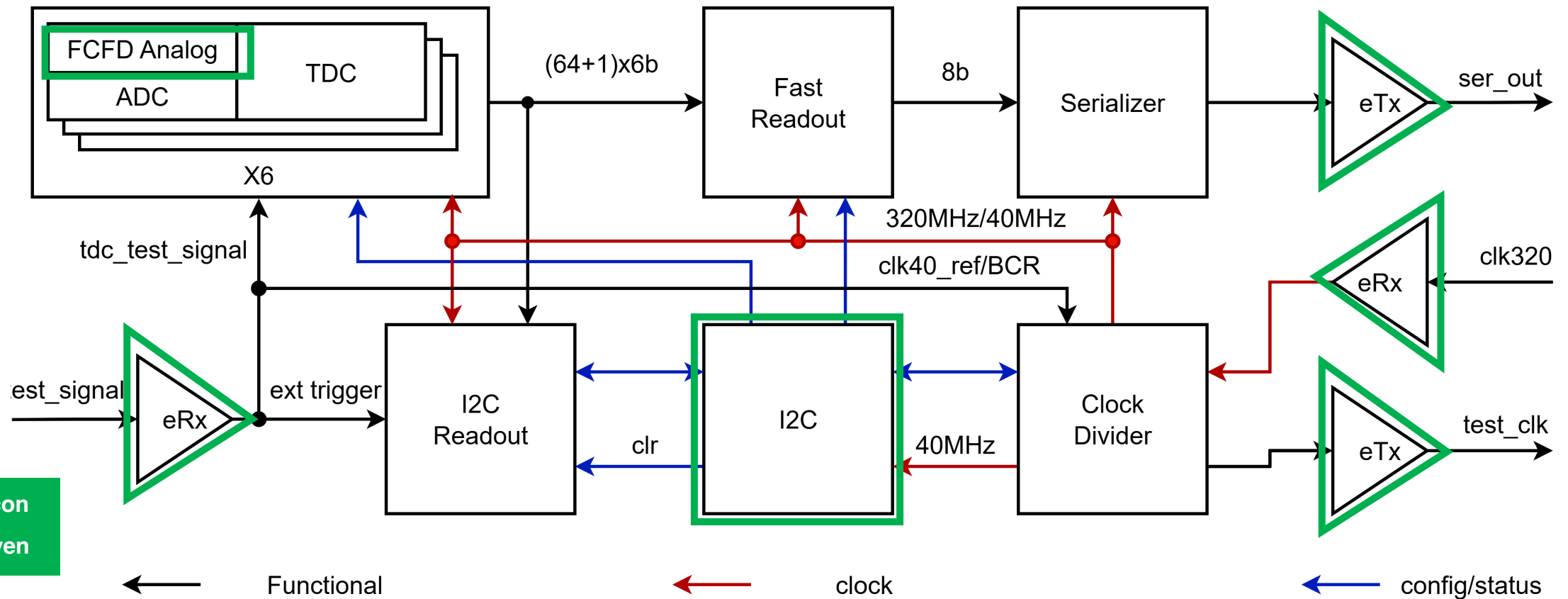
Modules

- **Each sensor has dedicated readout ASICs**
 - Simple modules for testing
 - Easy aGND/dGND separation
 - Plenty of real estate for IO and power
- **FCFD channel counts**
 - Practical chip size and aspect ratio 14-15 by 2-3 mm
 - Direct wire-bonding to the sensor
 - Channel pitch slightly smaller than that of the sensor (0.5mm) so to butt two chips along the sensor.
 - Small fan-out angles (1mm shift for 3-4mm long bonds)
 - All 4 ASICs are connected in a single readout chain



FCFD1.2 prototype

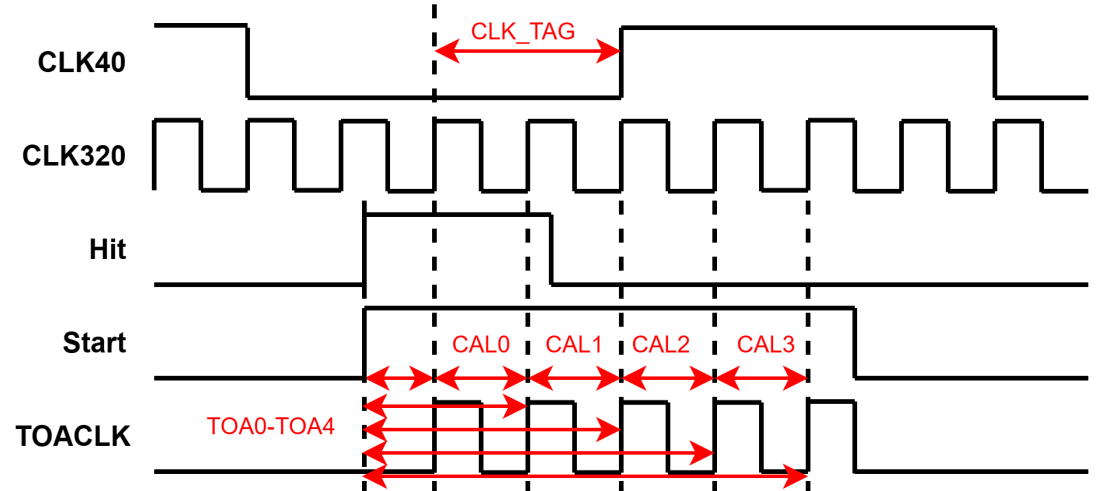
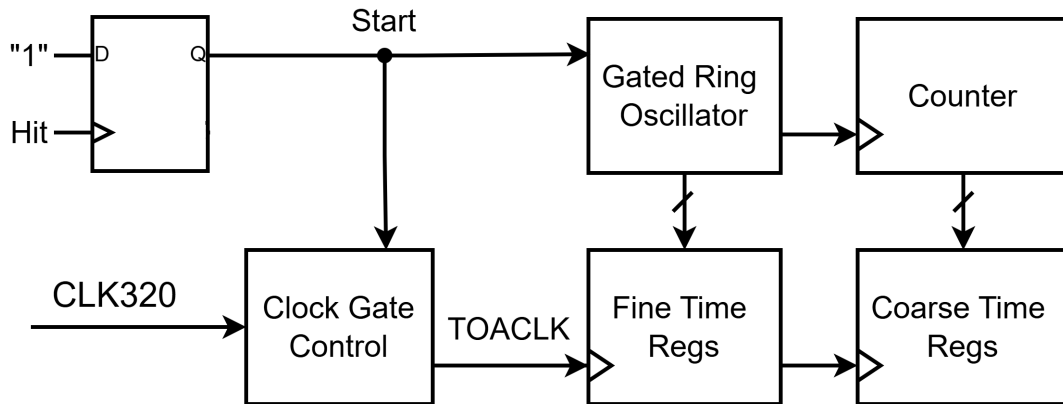
- This prototype will implement and test components beyond the FCFD analog
 - This version focuses on digitization (ADC/TDC), readout (fast/I2C) and configuration (I2C)
 - Fast readout builds data frame; I2C readout uses self/ext trigger



Silicon proven

Self-calibrating multi-cycle TDC

- Requirements:
 - Precise time (<10 ps); Low power (~100 uW); Low occupancy (<100 Hz); No blind timing windows;
- Adopted self-calibrating, multi-cycles TDC architecture.
 - Using regular 320 MHz clock signal; using regular foundry digital standard cells
- Robust against power supply, temperature and mismatch
- The number of timestamps is programmable, up to 64

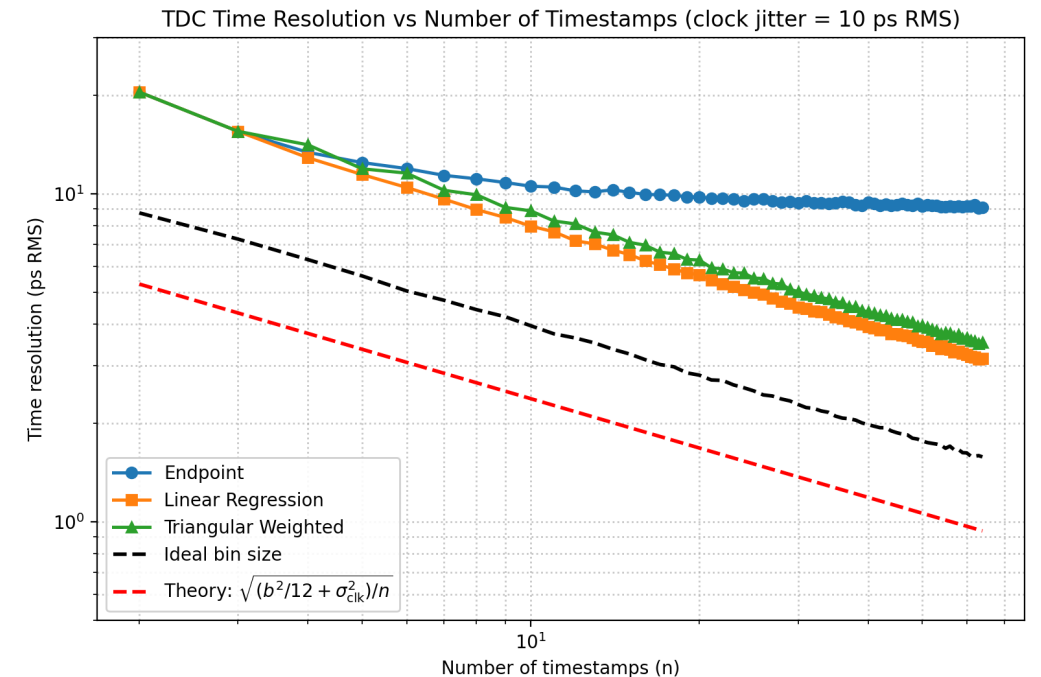
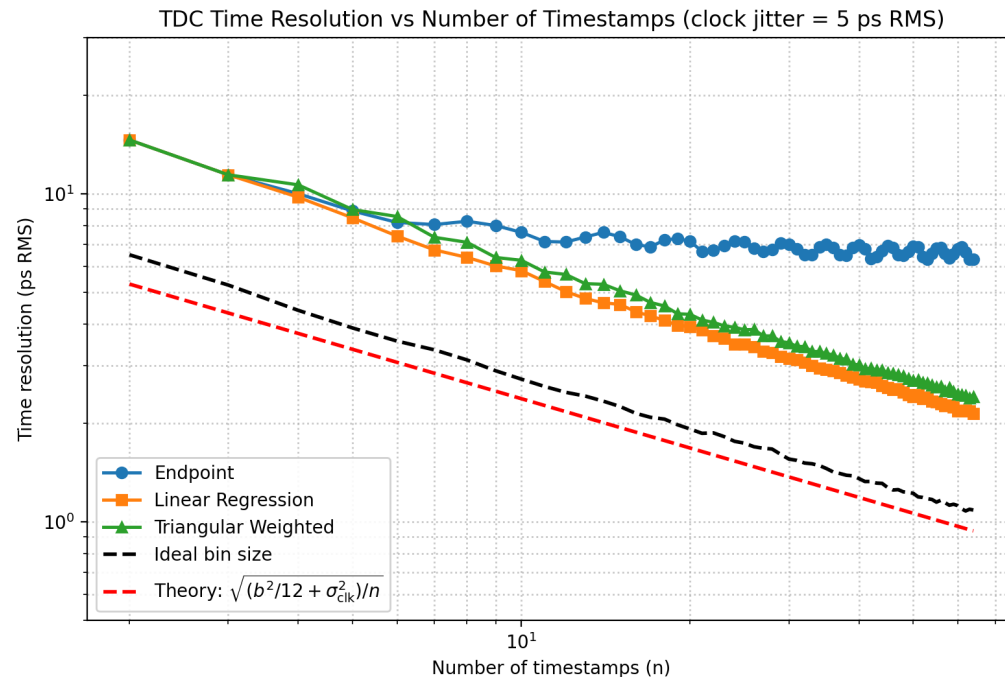
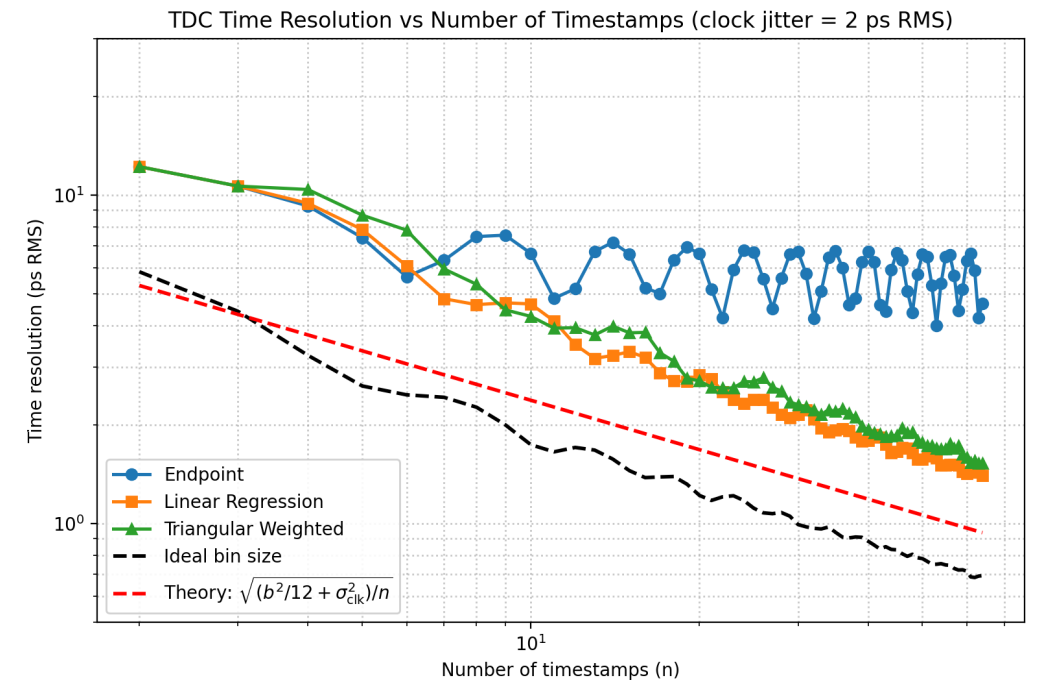




Clock jitter effects

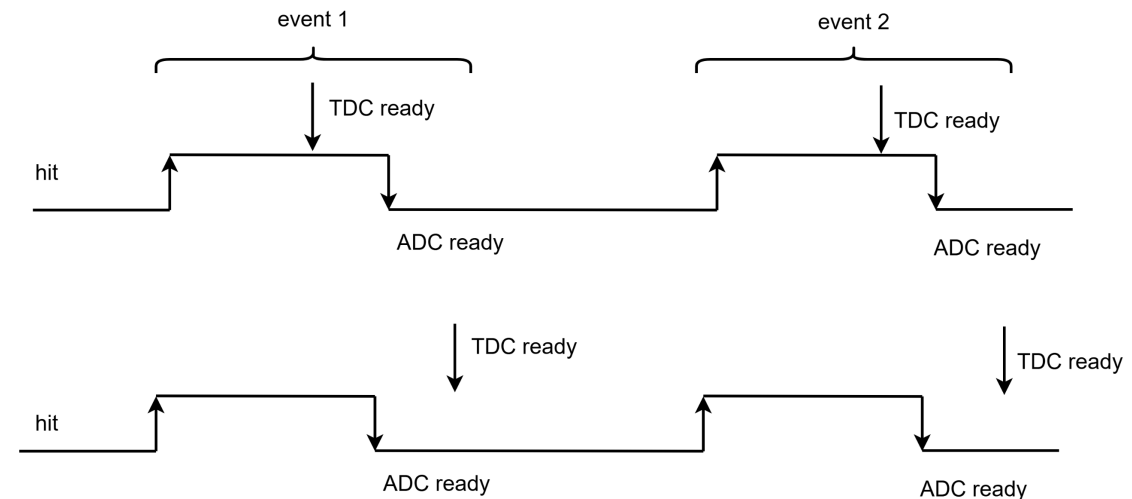
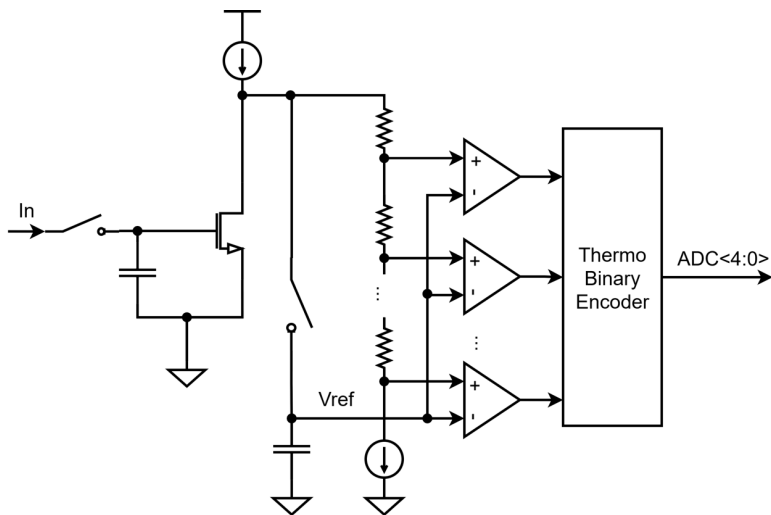
- Multi-cycle averaging suppresses the noise resolution.

Clock Jitter (RMS)	2 ps	5 ps	10 ps
N=16	3.8	4.9	7.0
N=32	2.2	3.4	4.9
N=63	1.5	2.4	3.5



ADC for amplitude readout

- 5 bits flash ADC design
 - The LSB corresponds to 1.5 fF with a dynamic range up to 75 fF
 - ADC data is ready on the falling edge of the hit signal
- Timing-sequencing logic is implemented to maintain ADC/TDC alignment.
 - ADC data are latched on the falling edge of the hit signal.
 - Timeout logic is implemented to recover the TDC from abnormal conditions.



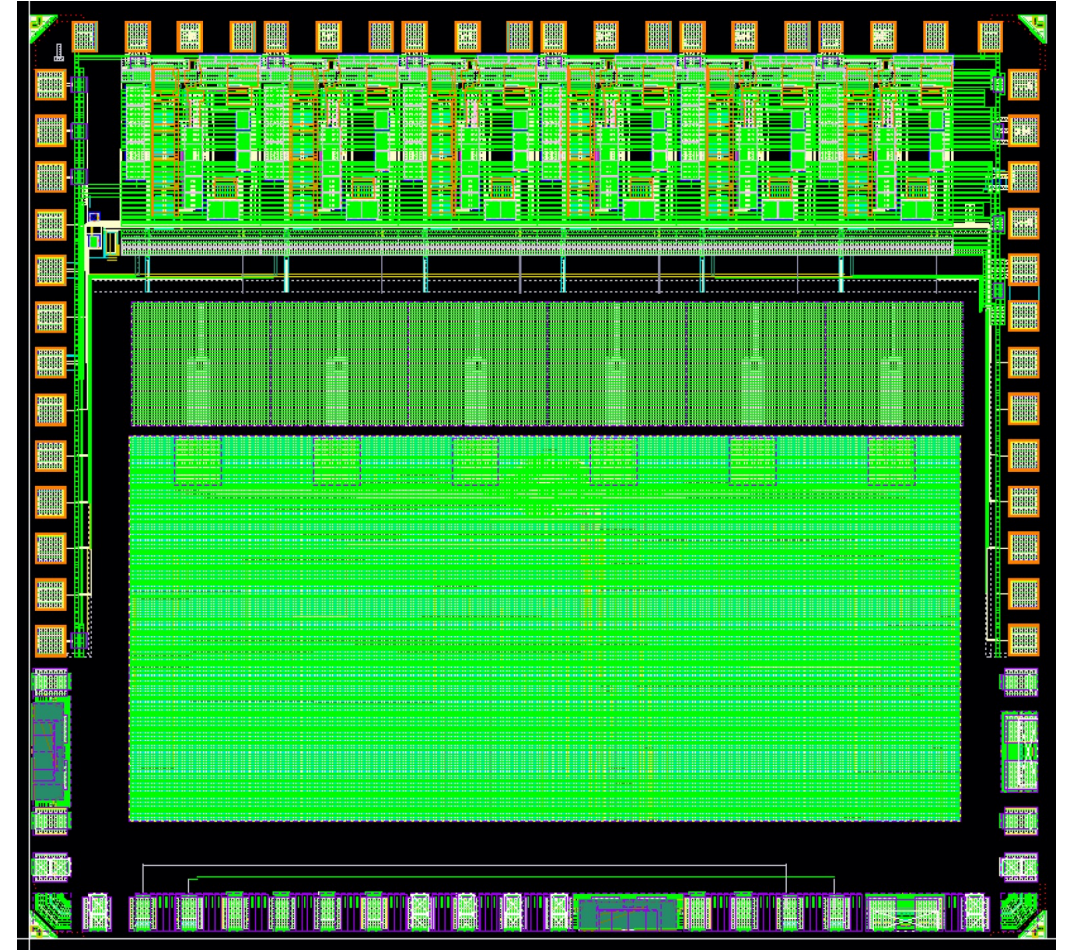
Chip floorplan

- Chip size: 3300x3000 um
- 6 channels, 450 um width per channel
- Analog integration for several large modules: frontend, 6 TDCs, globalDigital and pad ring

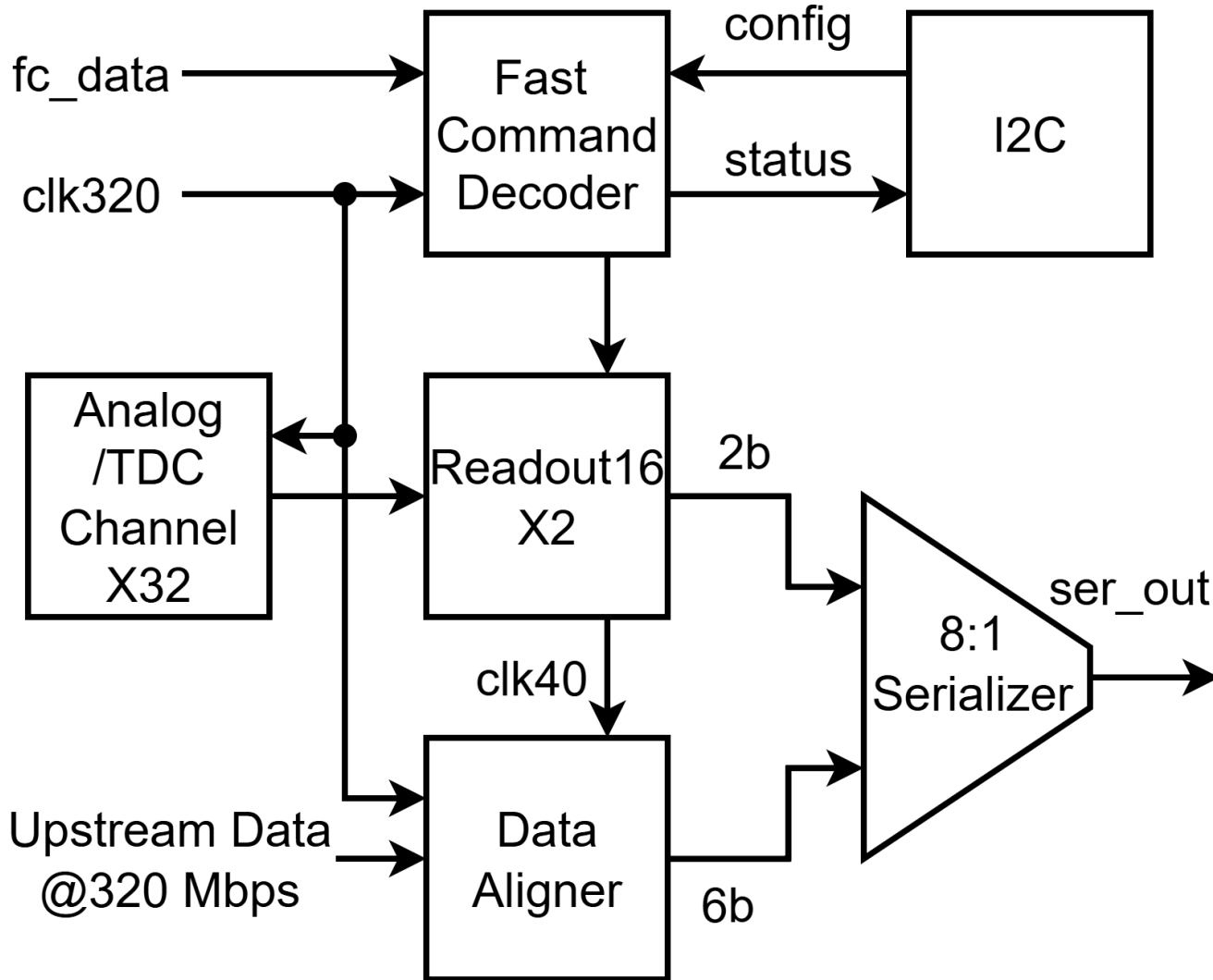


Status of FCFD1.2

- FCFD1.2 was submitted on April 12, 2026
- Expect the chips back from TSMC in middle of July
- Currently working on the design of the test boards and development of the readout firmware
- Extensive testing planned for testing of the all-new ingredients separately, and the whole chip together



Extension to 32-channel FCFD2



Remaining steps for the FCFD2

- Scaling up to the larger chip
- Triplication for radiation protection
- Add a Fast-command decoder
- Expand readout from 6 channels to 16 channels while keep data frame definition.
- Add chaining stage for data alignment logic

Summary

- FCFD readout chip is first hardware-enabled CFD timing chip co-designed with 4D tracking detectors
- Many rounds of prototyping and characterization since 2021 proves its robust performance
- Latest version FCFD1.2 is the next big step towards the bTOF @ ePIC (EIC)



Fermilab

Fermi *FORWARD*



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Power consumption estimation for 32-ch FCFD2

	Unit power(mW) (32-ch)	Units in FCFD32	FCFD32_Power(mW)
analog_front (2.5V)	2	32	64
analog_front (1.2V)	1.6	32	51.2
TDC	0.2	32	6.4
eRx	1	2	2
eTx	2	1	2
Readout16	30	2	60
Serializer	3	1	3
fc_decoder	5	1	5
data_aligner	2	1	2
I2C	2	1	2
Total (mW)			197.6
Total (mW) for 2.5V			64
Total (mW) for 1.2V			133.6