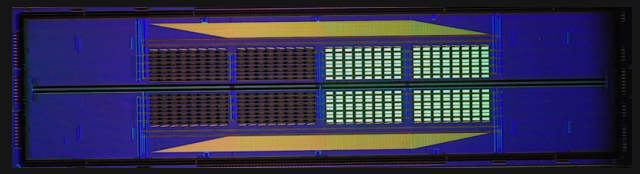
From MADpix to the Alice3 ToF ASIC: Monolithic CMOS LGAD sensors for Timing Applications

XIII FRONT-END ELECTRONICS WORKSHOP 2026

Valerio Pagliarino* on behalf of the INFN Alice3 ToF Collaboration



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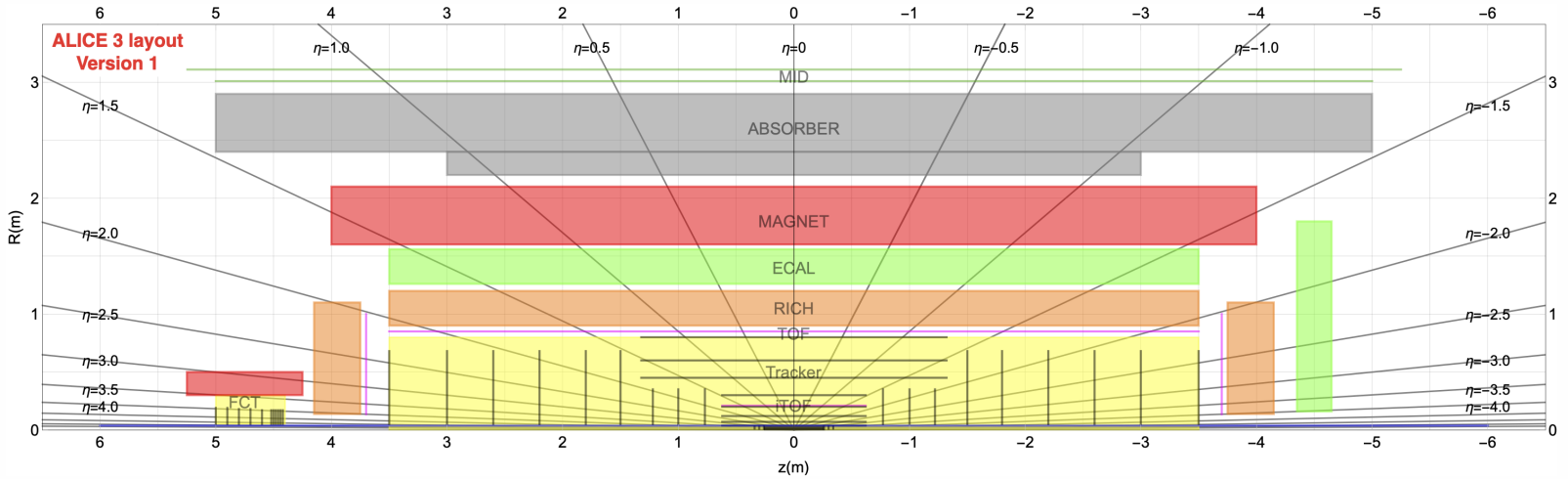
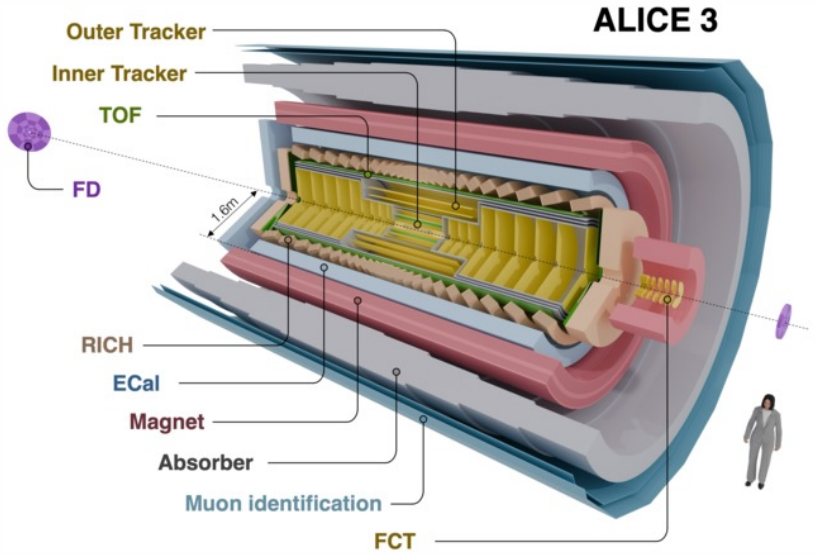
A monolithic CMOS LGAD for the Alice 3 ToF

- Alice 3, scheduled for operations in 2036 will feature unique Particle Identification (PID) capabilities and exceptional pointing resolution
- A crucial role for electron and hadron identification at low energy is played by the **Time-of-Flight detector** expected to cover 45 m^2 with a timing risolution of **20 ps,** tight material budget constraints and a low power density of 200 mW/cm^2



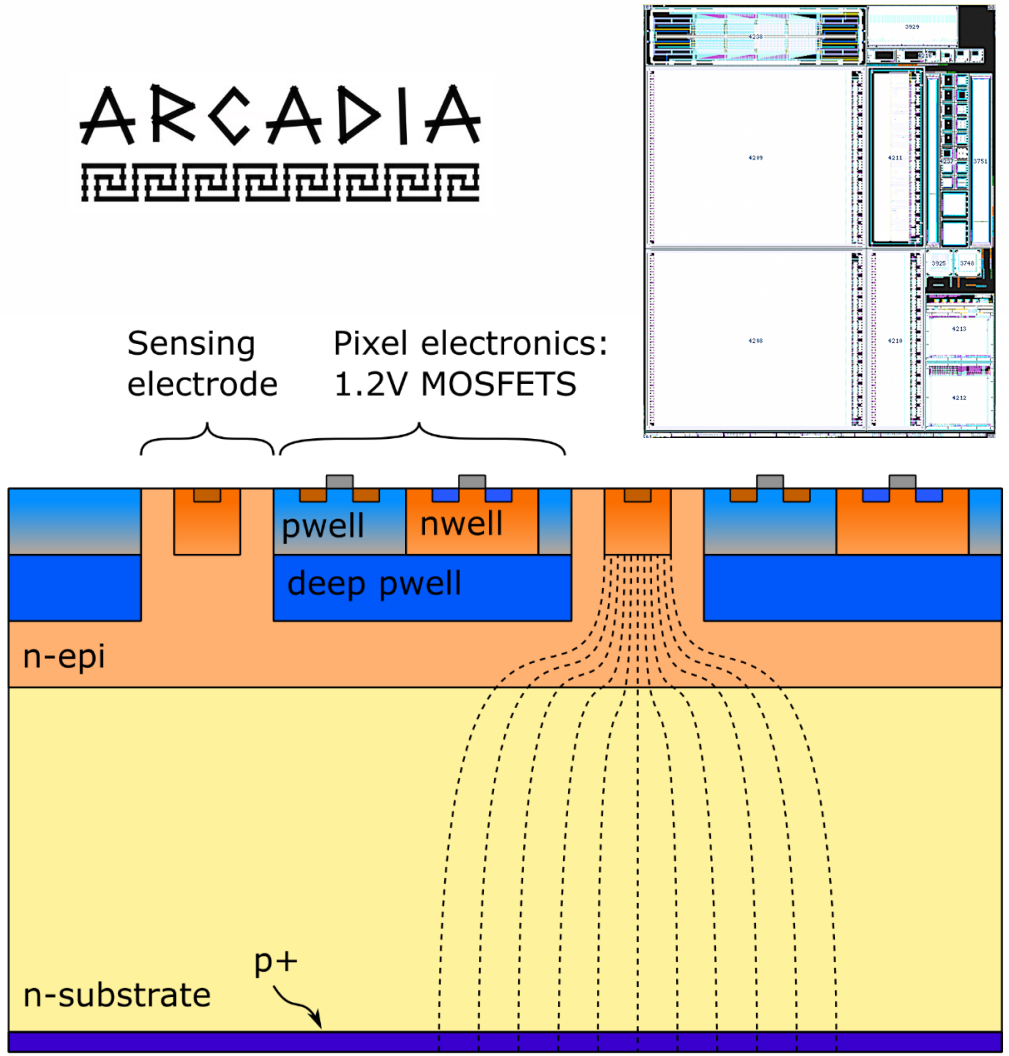
	Inner TOF	Outer TOF	Forward TOF disks
Total area (m^2)	1.5	37	6
Pixel size (mm^2)	1×1	5×5	1×1 to 5×5
Particle hit rate (kHz/cm^2)	200	15	280
Material budget per layer ($\%X_0$)	1 to 3	1 to 3	1 to 3
Power density (mW/cm^2)	200	200	200
Time resolution (RMS) (ps)	20	20	20
Radiation tolerance NIEL (1 MeV n_{eq}/cm^2)	$7 \cdot 10^{12}$	$9 \cdot 10^{11}$	$1 \cdot 10^{13}$
Radiation tolerance TID (rad)	$3 \cdot 10^5$	$2 \cdot 10^4$	$4 \cdot 10^5$



Courtesy of the Alice 3 collaboration

The MadPix Sensing Pixel with Gain

- The current baseline solution is a **Monolithic CMOS LGAD sensor** based on the **ARCADIA** platform: *Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays*
- The Front-End electronics is embedded in the same substrate, reducing the cost and the material budget
- The reverse-biased junction is at the bottom and the **depletion grows from back to top**
- Being a **fully-depleted monolithic sensor the charge collection is fast** by drift, this ensures **good timing performance**
- **For optimal timing performance a very good electric field uniformity is necessary:** a large electrode is used with the drawback of **increasing the capacitance, worsening the Signal-to-Noise Ratio. The current state-of-the-art timing resolution for standard CMOS sensors is ~1 ns**

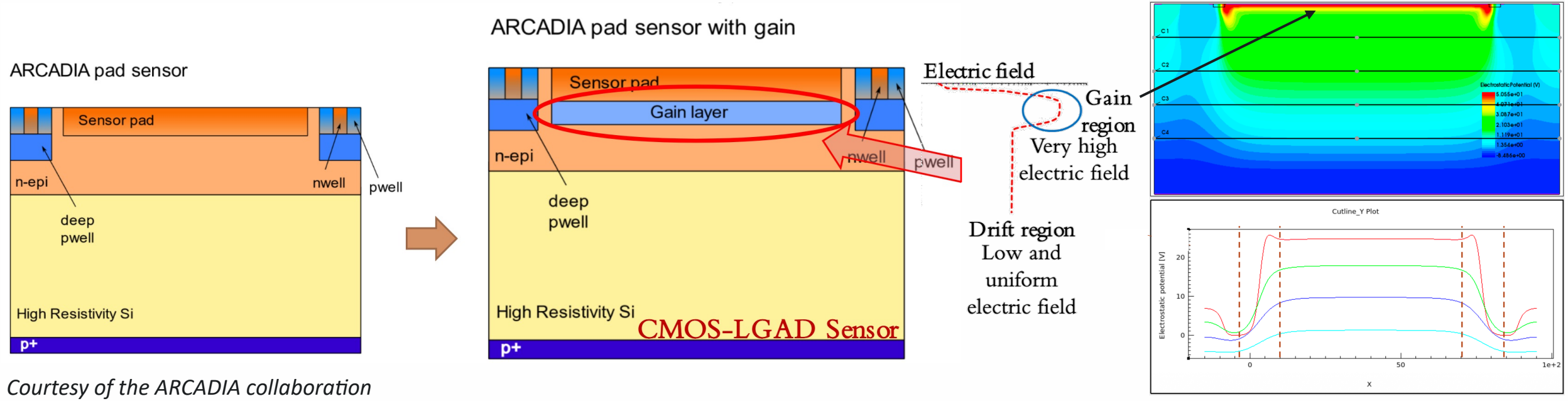


Courtesy of the ARCADIA collaboration

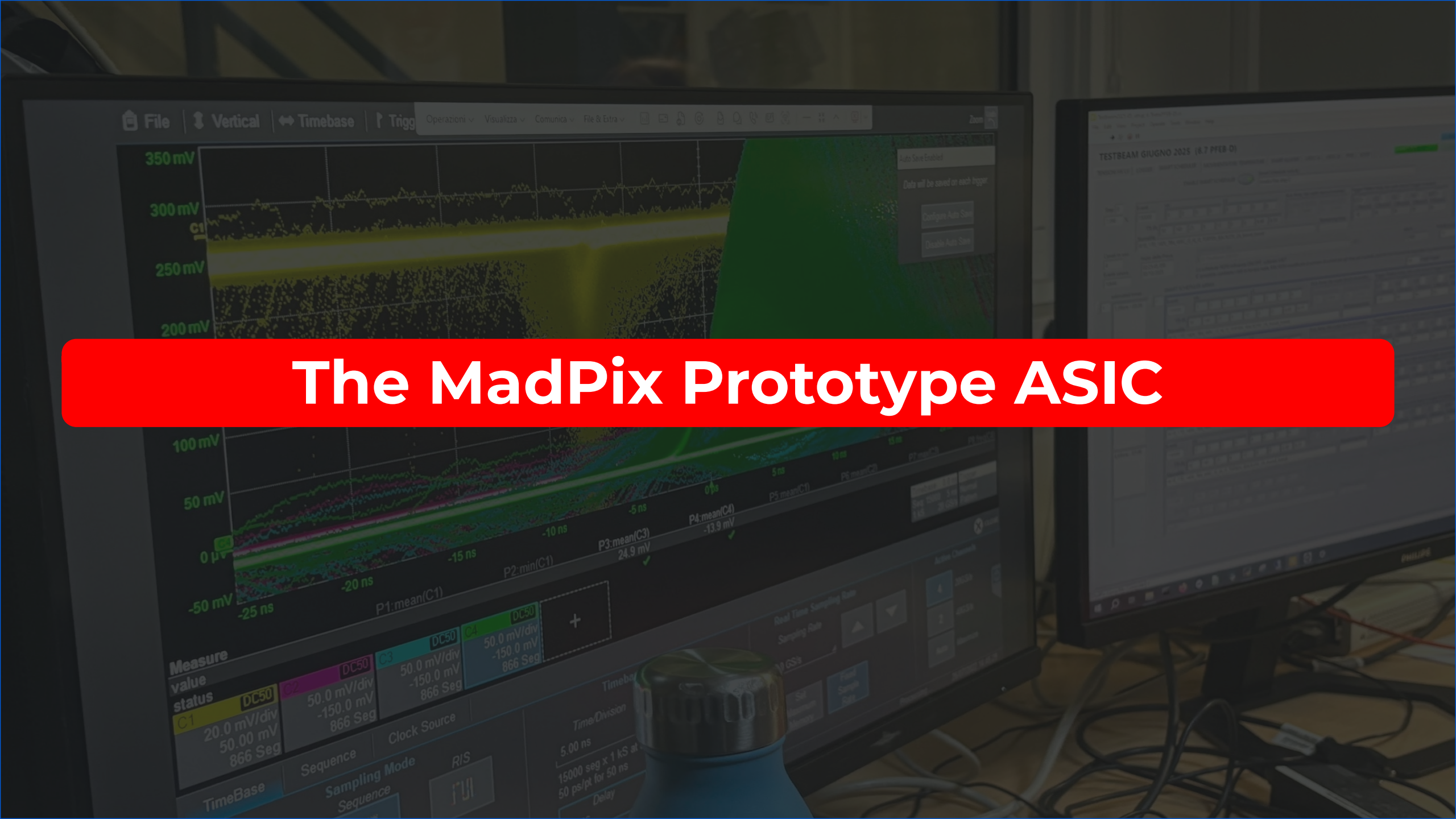
The MadPix Sensing Pixel with Gain

- The solution is the addition of an embedded **low gain layer:** an additional p+ doped layer near the p-n junction which create a very intense electric field
- The drifting charges are accelerated in the gain layer and acquire energy
- If the acquired energy is sufficient, **they ionize atoms producing other e-h pairs undergoing a charge multiplication effect** that is an **avalanche process**
- This final goal of introducing gain is to increase the **Signal-to-Noise Ratio**.
- A larger signal results in a better timing resolution.

Madpix T-CAD Simulation with Ntop
bias = 50V, 70 µm active area, 15 µm sensor tickness.
Courtesy of Matteo Barbagiovanni – from presentation to ALICE mini week, 20/1/2026, Lucio Pancheri.



Courtesy of the ARCADIA collaboration



The MadPix Prototype ASIC

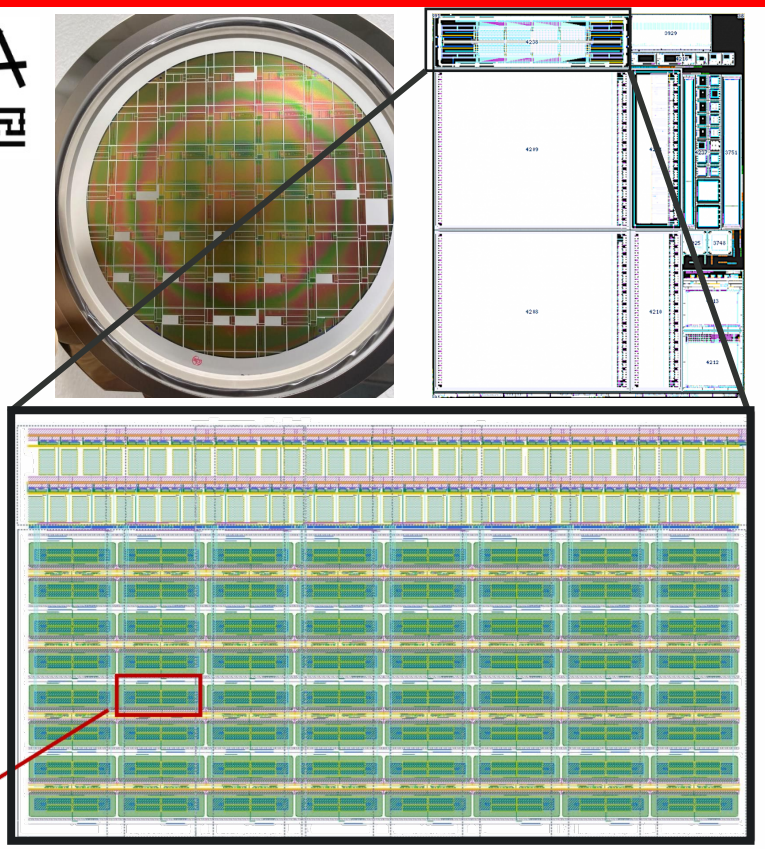
Architecture of the MadPix Prototype

- Within the ARCADIA Platform, the *MaxPix (Monolithic CMOS Avalanche Detector PIXelated Prototype)* prototype has been fabricated, first prototype of CMOS LGAD with **integrated electronics** at 1.2 V and **gain layer** with active tickness of 48 µm

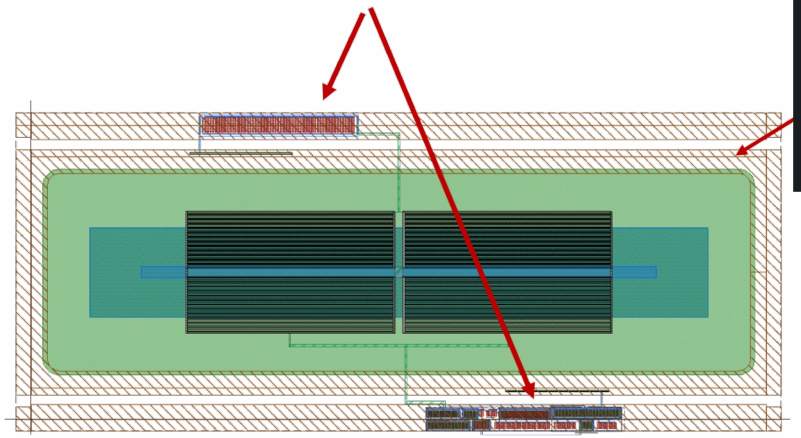
- The backside High-Voltage allows the full depletion
  ↦ -20 V to -40 V

- The topside High-Voltage manages the gain
  ↦ 45 V to 65 V

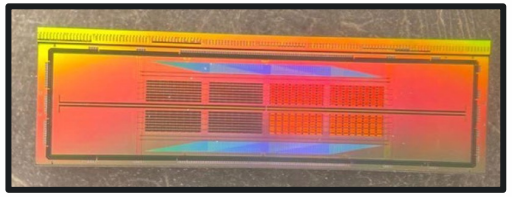
- The MadPix prototype includes 8 matrices of 64 pixels each one with size
  250 µm x 100 µm.
  64 x 2 analog outputs with 3.3 V buffers and 4 flavours



Integrated Front-End electronics



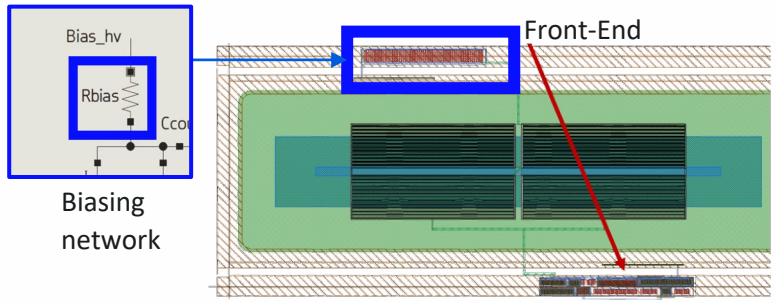
4.4 mm x 16 mm



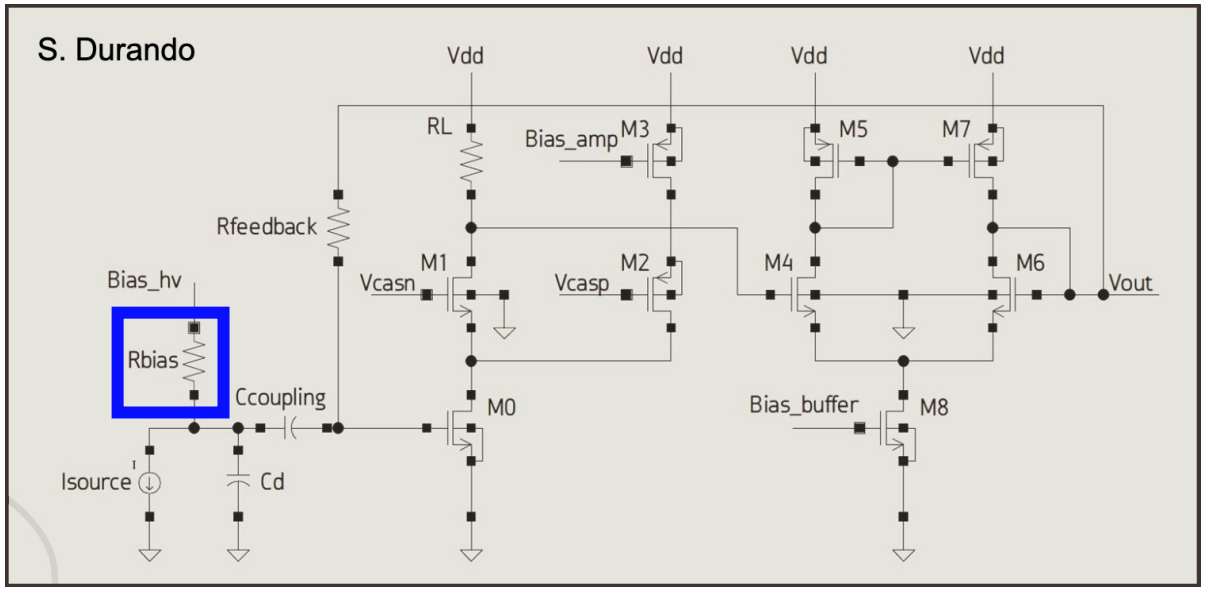
Courtesy of the ARCADIA collaboration and G. Gioachin, C. Ferrero, U. Follo

MadPix in-pixel Electronics

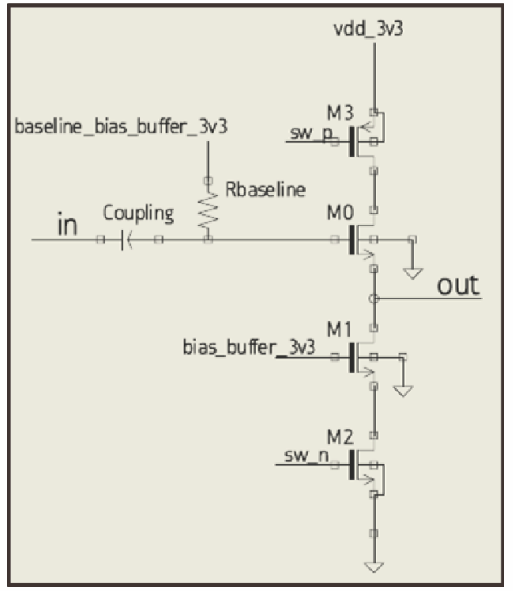
The embedded Front-End Electronics is located on the side of each pixel. With the guard-ring polarized for optimizing the field uniformity (and therefore the timing resolution) charge collection under the electronics is avoided, but changing the guarding polarization a edge breakdown might occur, leading to charge collection also under this region.



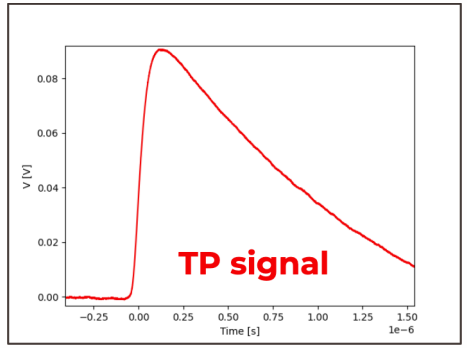
- Cascoded common source with differential buffer operating at 1.2 V
- Front-End AC coupled with the sensor
- Power: 0.18 mW/channel

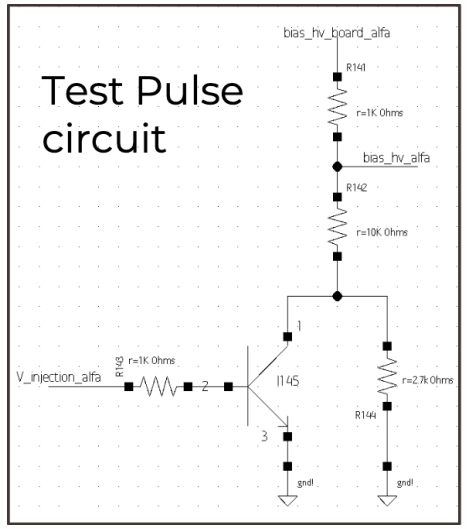


- Source Follower operating at 3.3 V
- AC coupled with the front-end
- Power: 1.65 mW/channel



A test pulser circuit with with linear discharge is available in MadPix.

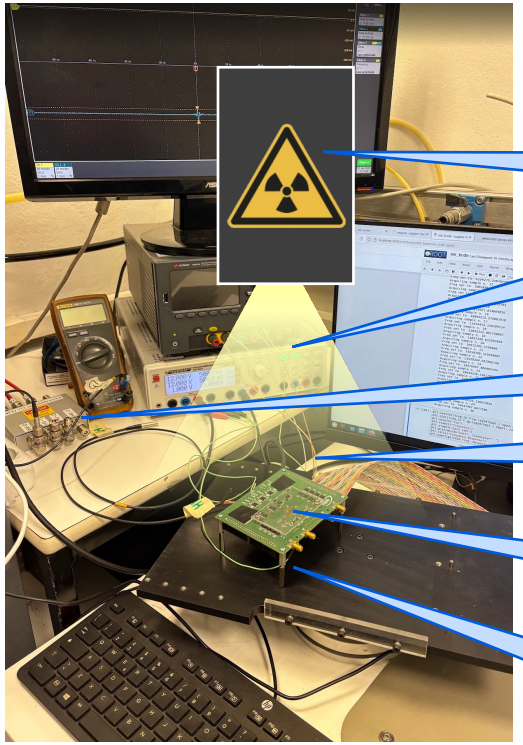




Gain and Timing Resolution Characterization Method

Gain measurement with radioactive source

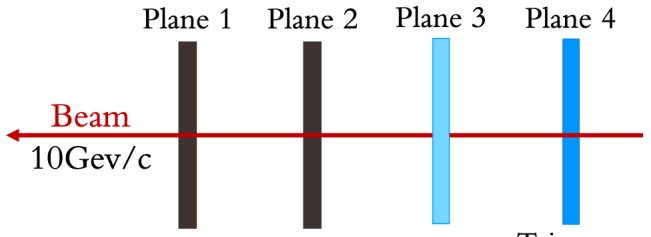
$$\text{Gain} = \frac{MPV_{with\ gain}}{MPV_{without\ gain}}$$



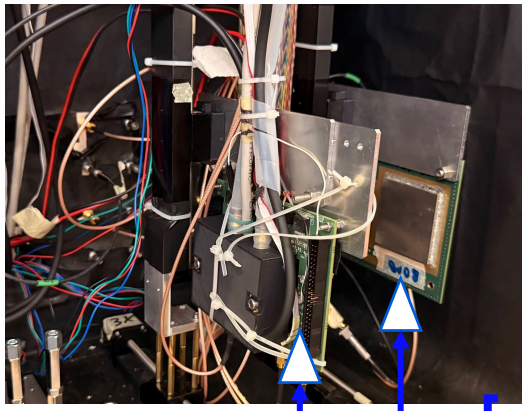
- Fe-55 Radioactive Source
- Low-Voltage PSU
- SHV fanout from HV PSU
- SHV fanout from HV PSU
- MadPix Test Board
- To 25 GSa/s 8.2 ENOB digitizer

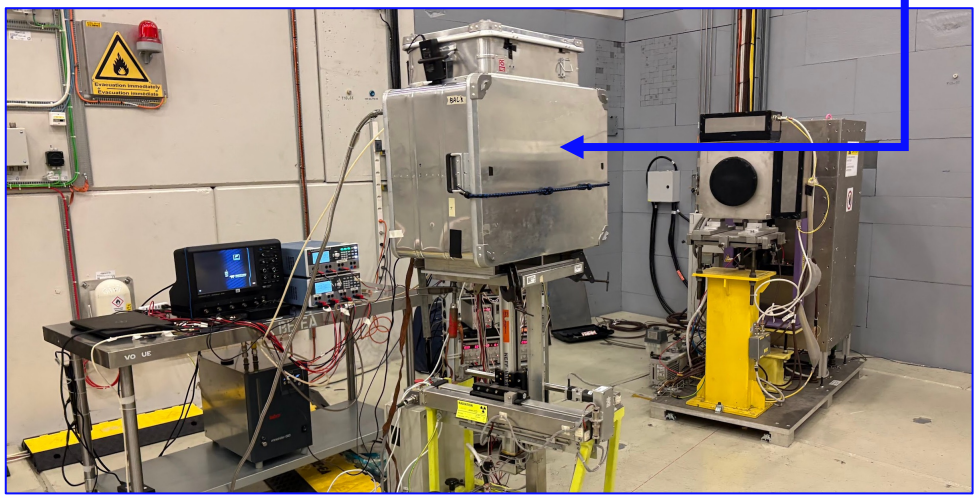
Courtesy of the INFN-To and INFN-Bo Alice 3 Timing Layer Group

Timing Resolution Measurement at CERN PS (T10)



Timing resolution is obtained from the time-of-arrival difference distribution between the DUT and the reference LGAD

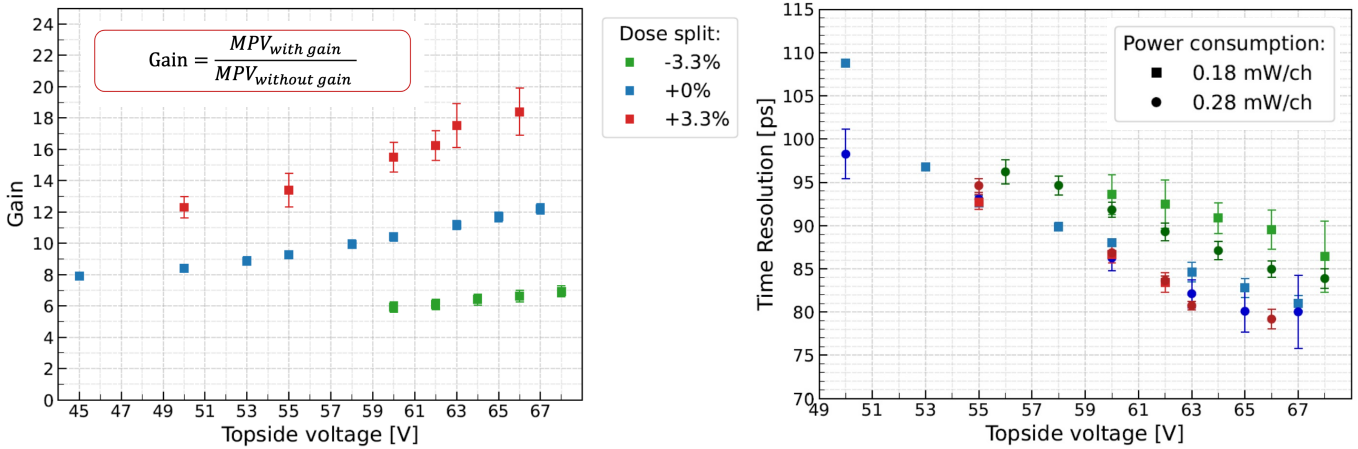


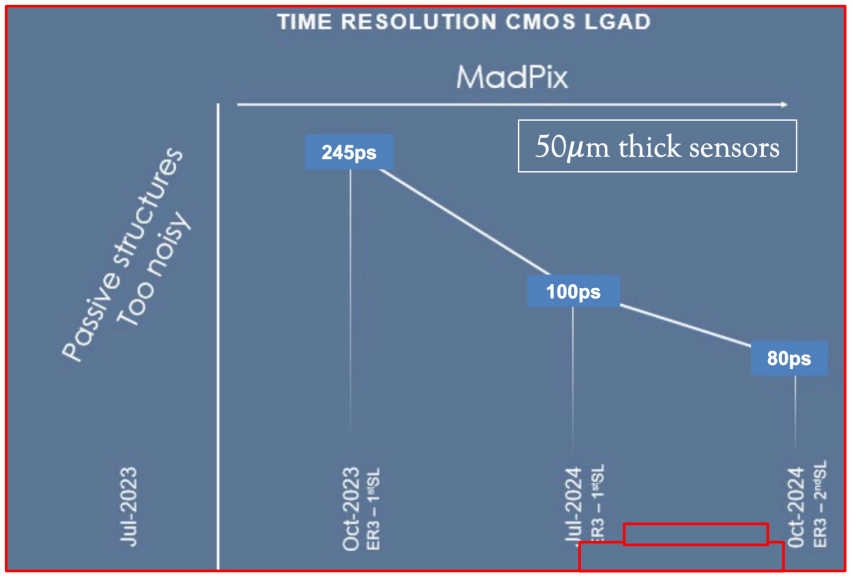


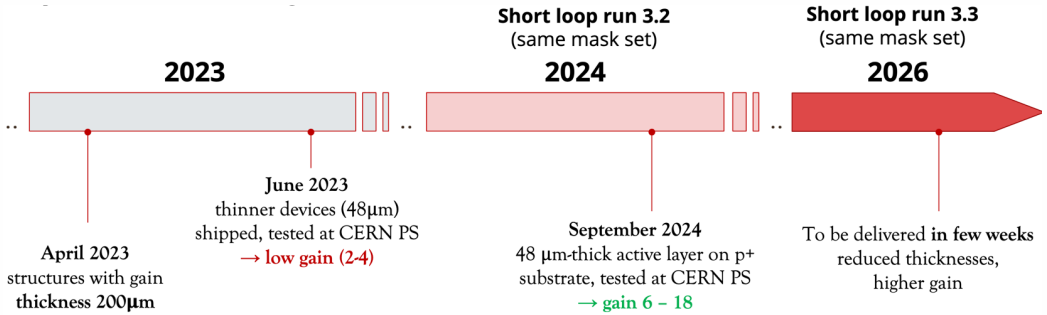
Progress in timing resolution

The path toward 20 ps is a challenging endeavour requiring several iterations. **From the first MadPix test** on ARCADIA ER3 (Engineering Run 3 with Arcadia Project Maskset) **with 245 ps** timing resolution several improvements have been introduced, **reaching 80 ps** for the first time in October 2024

- The maskset include monolithic prototypes with large and small collection electrodes and passive / active structures with gain





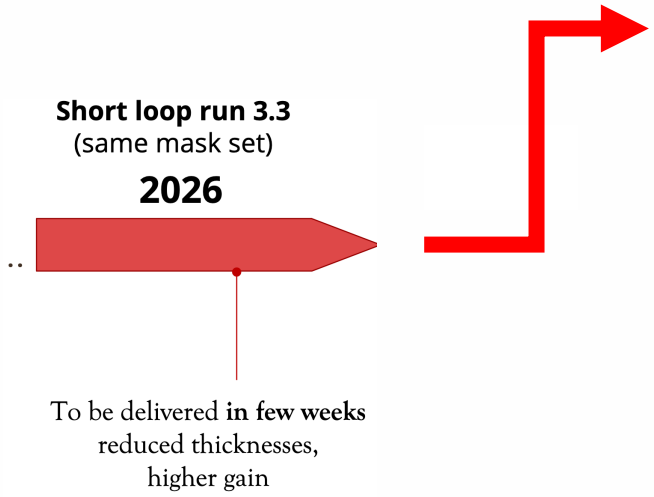


From Test Beam campaing at CERN PS 2024-2025

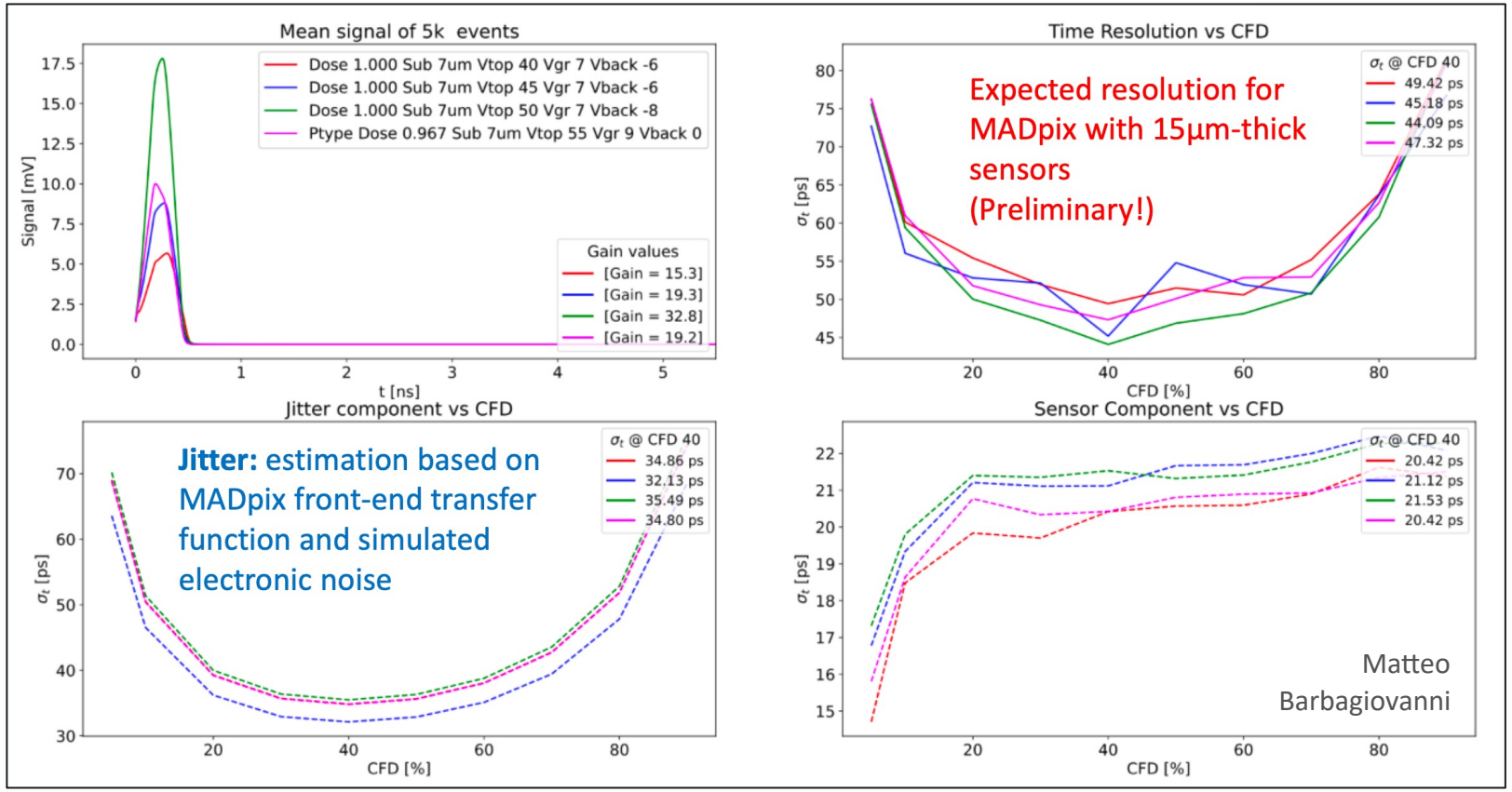
Courtesy of G. Gioachin, C. Ferrero, U. Follo from the Alice 3 Timing Layer Group

Optimization for 20 ps

According to our T-CAD & Garfield Monte-Carlo simulations the timing resolution of 20 ps will be finally achieved with the run 3.3 short-loop that is expected to be delivered in a few weeks, thanks to the reduced tickness of 15 µm and the increased gain.



Expected results according to T-CAD Simulations

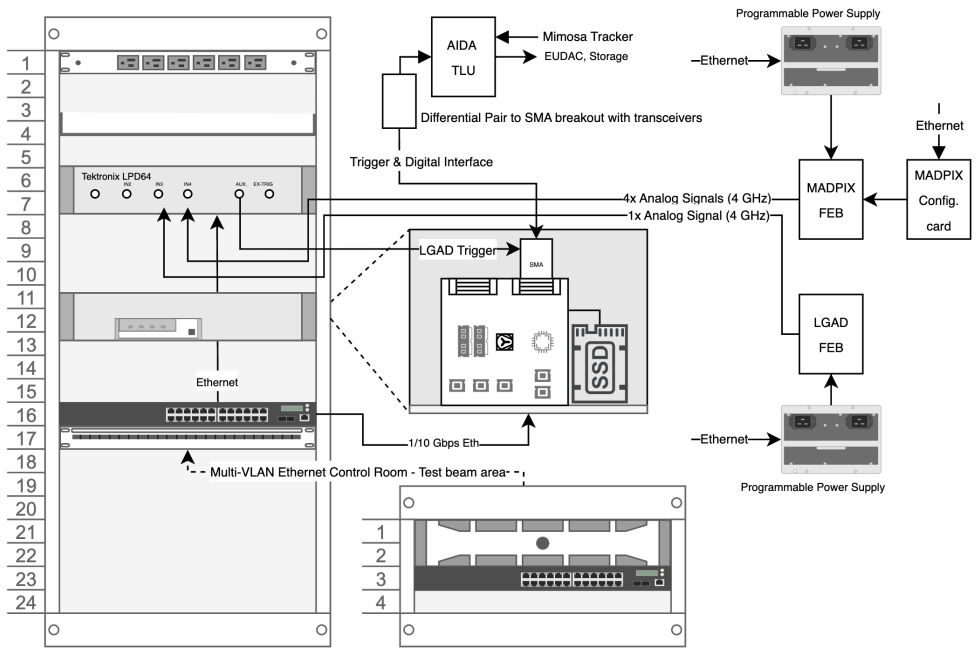


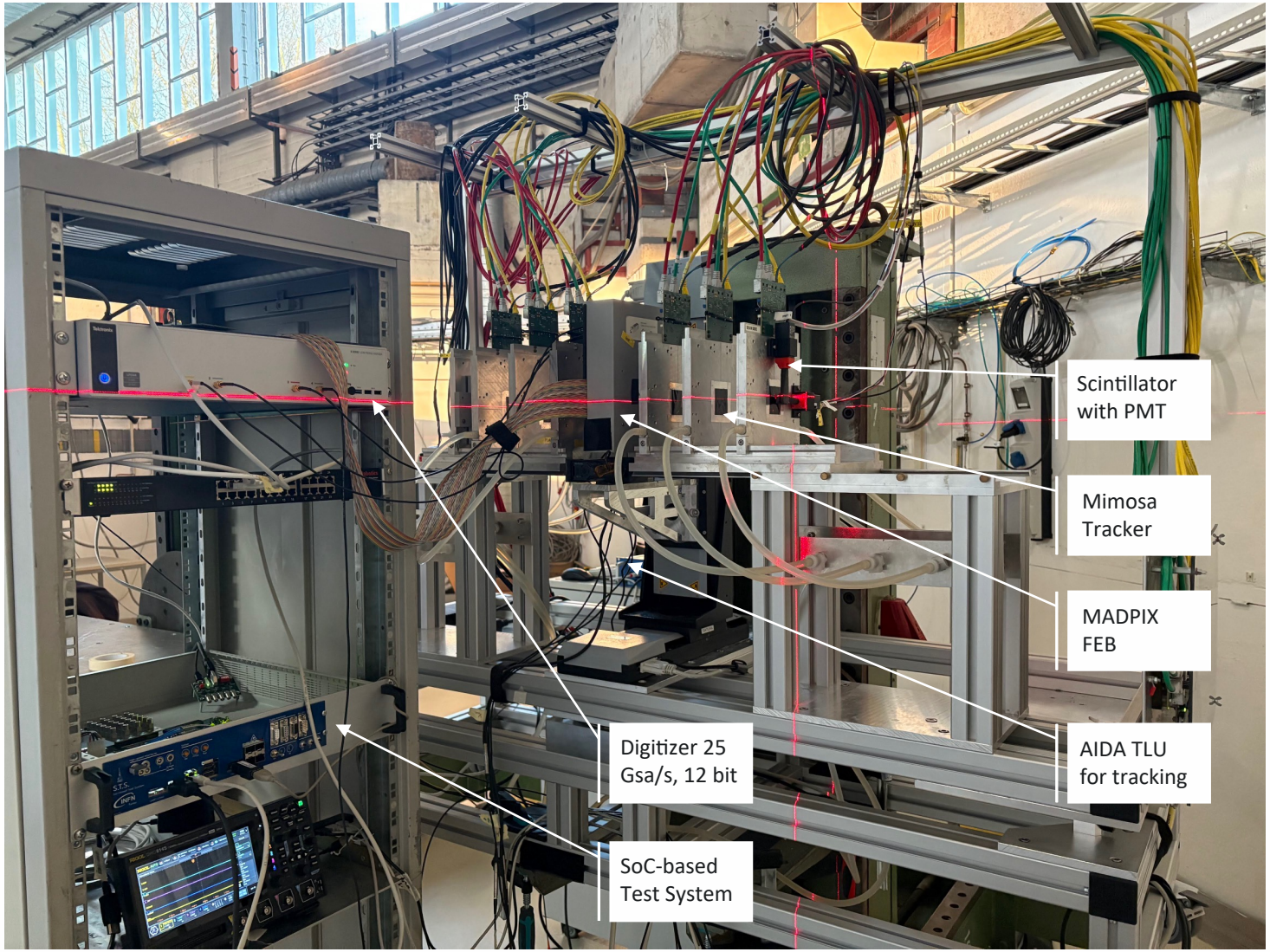
Courtesy of the Alice 3 Timing Layer Group. T-CAD simulations by Matteo Barbagiovanni – from presentation to ALICE mini week, 20/1/2026, Lucio Pancheri.

In-pixel characterization with tracker at DESY

In order to analyze at the sub-pixel level the timing resolution, the efficiency and therefore the characteristicof the electric field, **two Test Beams ad DESY** has been performed, adding to the setup a 6-planes tracking telescope thus **correlating the timing measurement with the interaction poisition of the MIP within the active pixels of MadPix.**

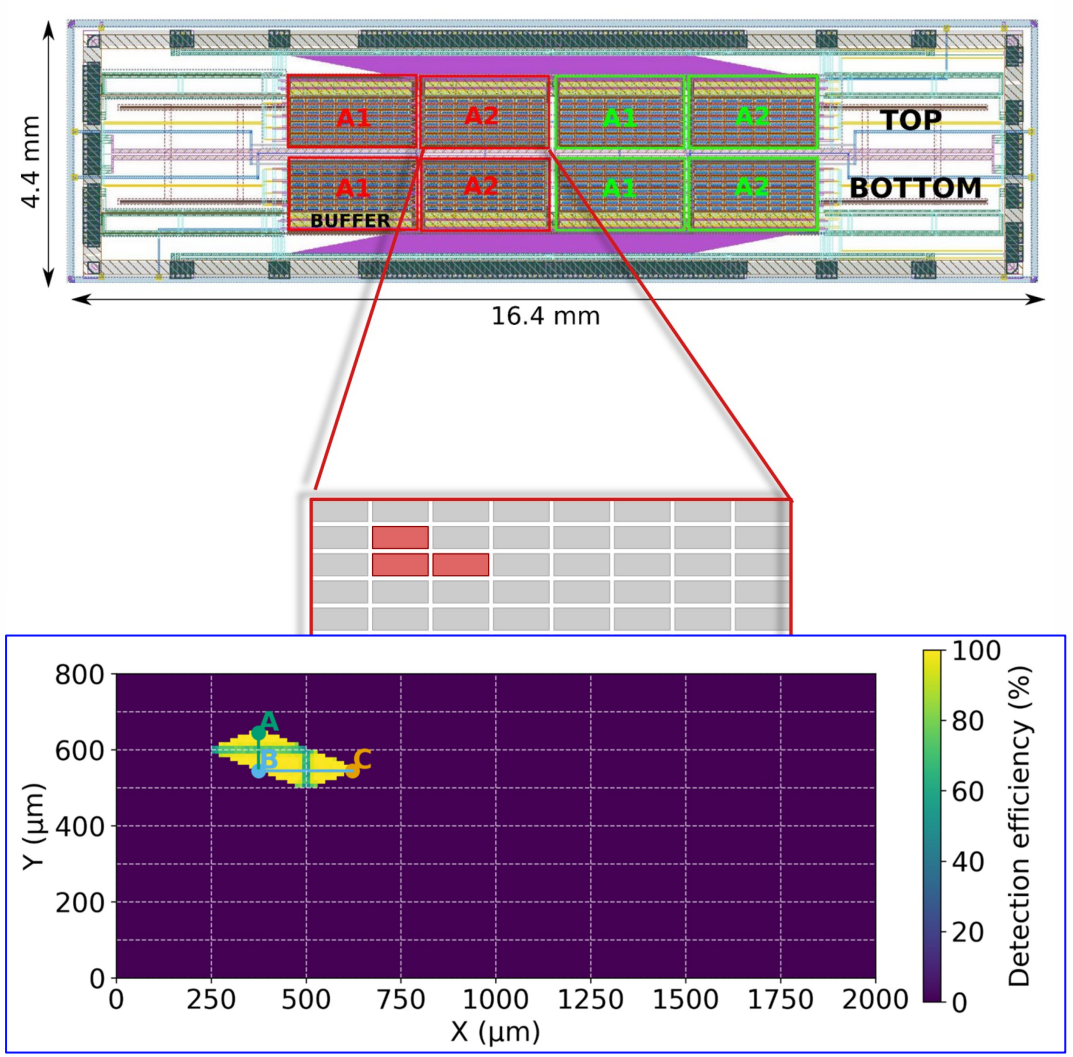
Setup used in March 2025:



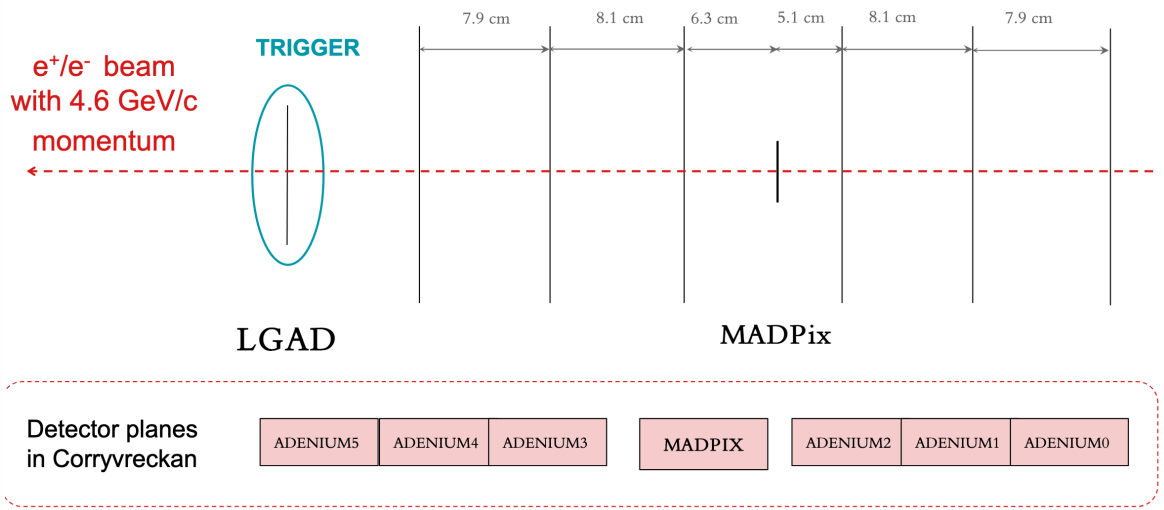


In-pixel characterization with tracker at DESY

In September 2025 the setup was updated replacing the *Mimosa* tracking planes with the *Adenium* tracker and changing the ROI (region of interest) on the DUT that is analyzed in order to investigate the timing resolution and efficiency variations when crossing vertical and horizontal pixel edges on the matrix.



November 2025 Testbeam using Adenium tracking planes:

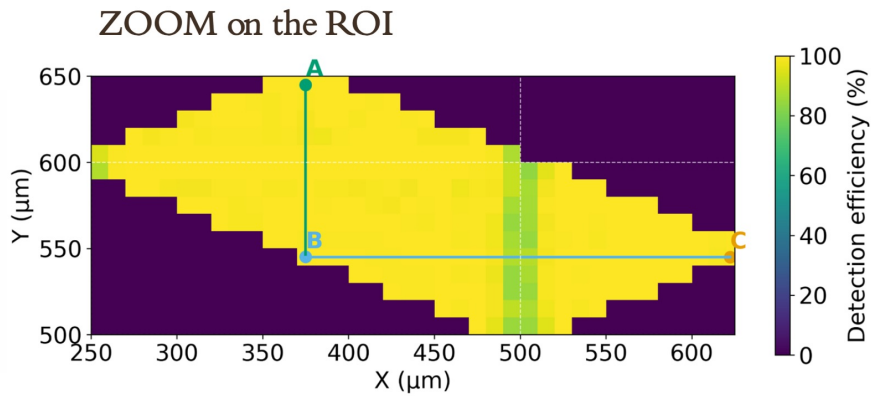


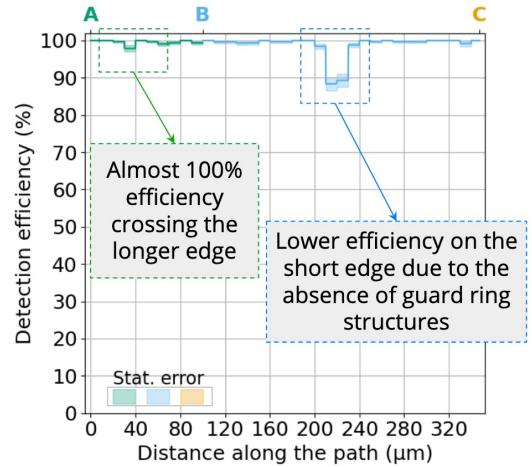
Tracking resolution on the DUT: 4.43 µm (250 µm x 100 µm pixel)

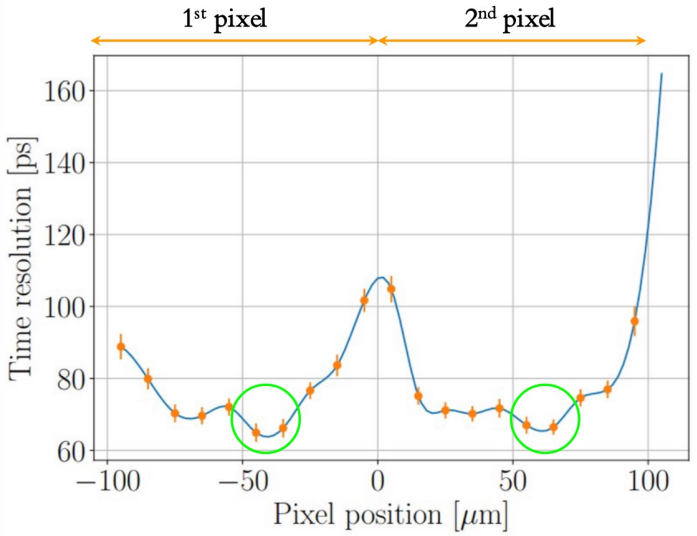
Courtesy of G. Gioachin, C. Ferrero, U. Follo from the Alice 3 Timing Layer Group

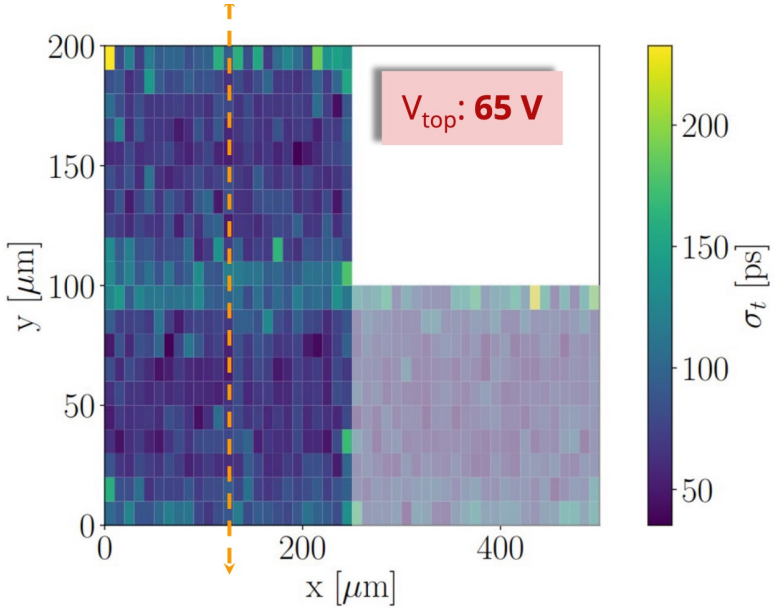
In-pixel Timing Resolution and Efficiency Studies

- The results show the timing resolution and the efficiency variations while moving on the A→B→C path inside the ROI, crossing the two edges.
- The timing resolution reaches less than 70 ps in the center of the pixel, where the electric field uniformity is optimal, while the field distortions at the edges produce an increase above 100 ps.
- These effects are due to the edge breakdown due to the guard ring biasing voltage, that enables charge collection also in this area with very high field distortion. Nevertheless, this configuration maximizes the charge collection efficiency.







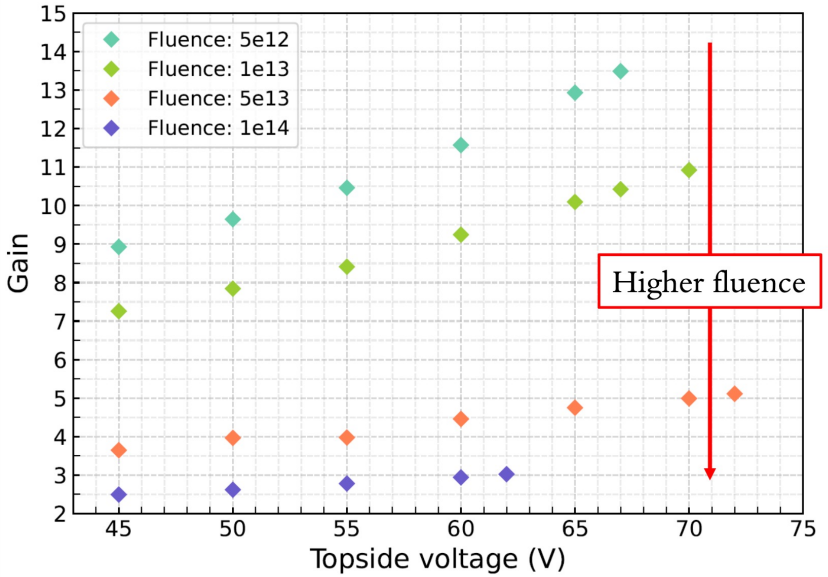


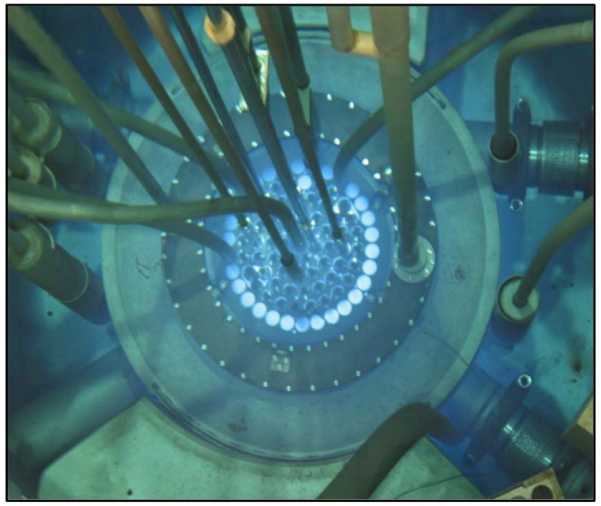
Courtesy of G. Gioachin, C. Ferrero, U. Follo from the Alice 3 Timing Layer Group

Radiation effects on the MadPix Prototype

- The future ToF monolithic sensor for Alice 3 must be capable of tolerating up to 10^{13} 1 MeV n_{eq} / cm^2 irradiation without catastrophic failure or performance drop

- The MadPix prototypes have been irradiated with the TRIGA reactor at the IJS Facility in Ljubljana with 5 different fluences: 5×10^{12}, 10^{13}, 5×10^{13}, 10^{14}, 10^{15} 1 MeV n_{eq} / cm^2 each batch contained MadPix chips and test structures with 4 difference doping profiles of the gain layer.

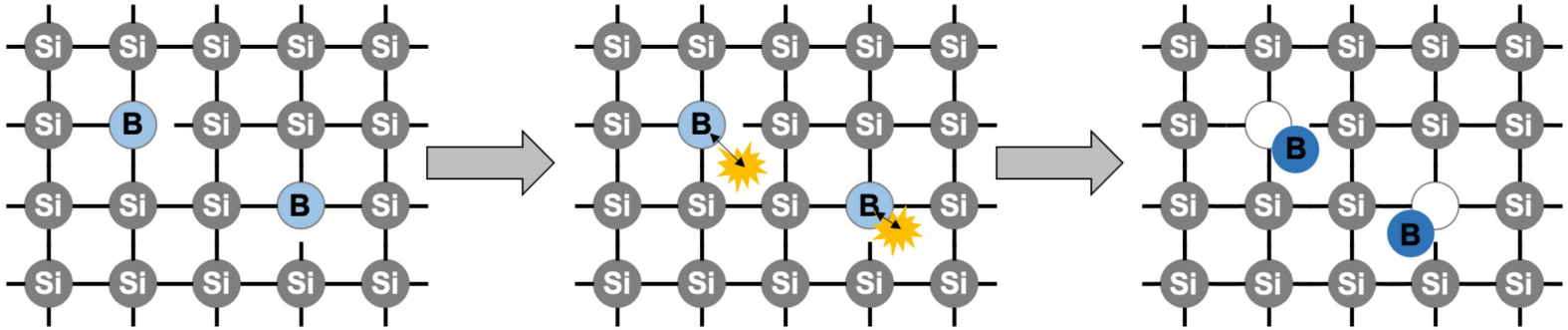




TRIGA reactor @ IJS

- The exposition to radiation has the effect of changing the doping densities through the acceptor removal effect.

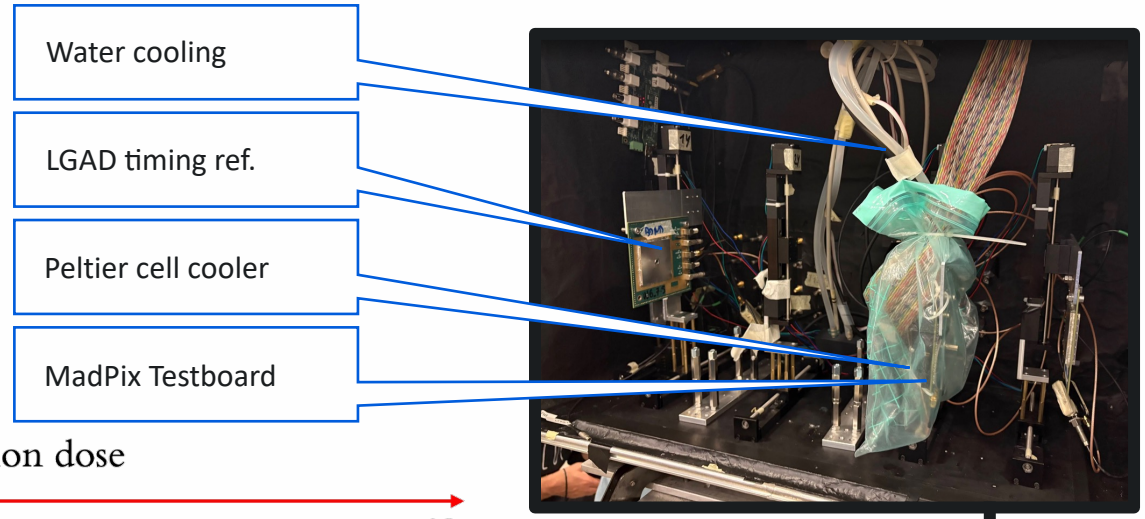
- This causes the deactivation of the gain layer and therefore the loss of gain

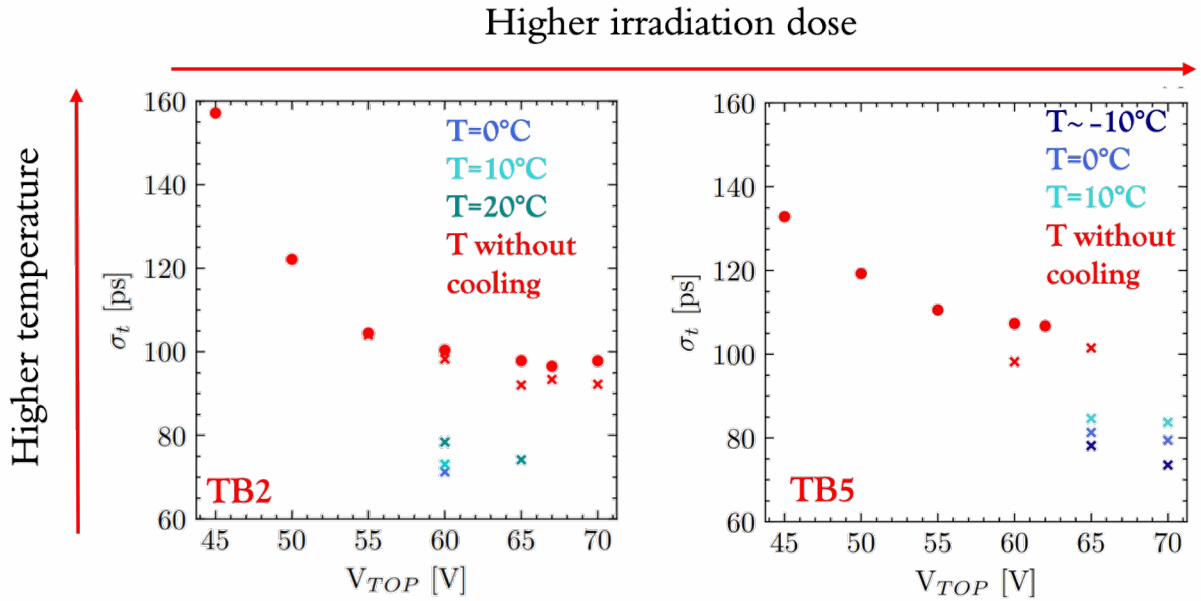


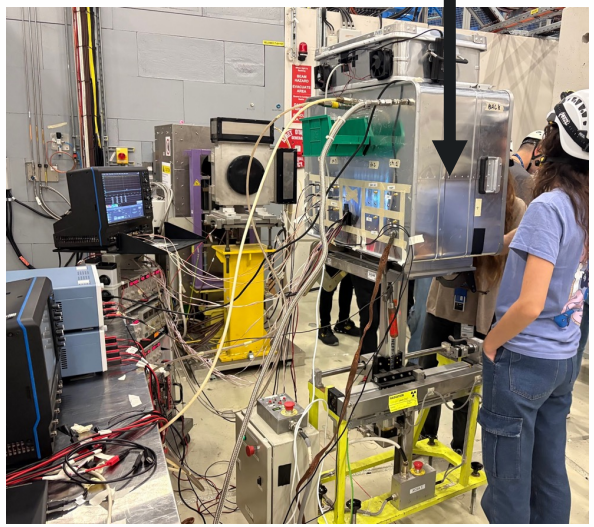
Courtesy of G. Gioachin, C. Ferrero, U. Follo from the Alice 3 Timing Layer Group

Temperature effects: testbeams at CERN PS

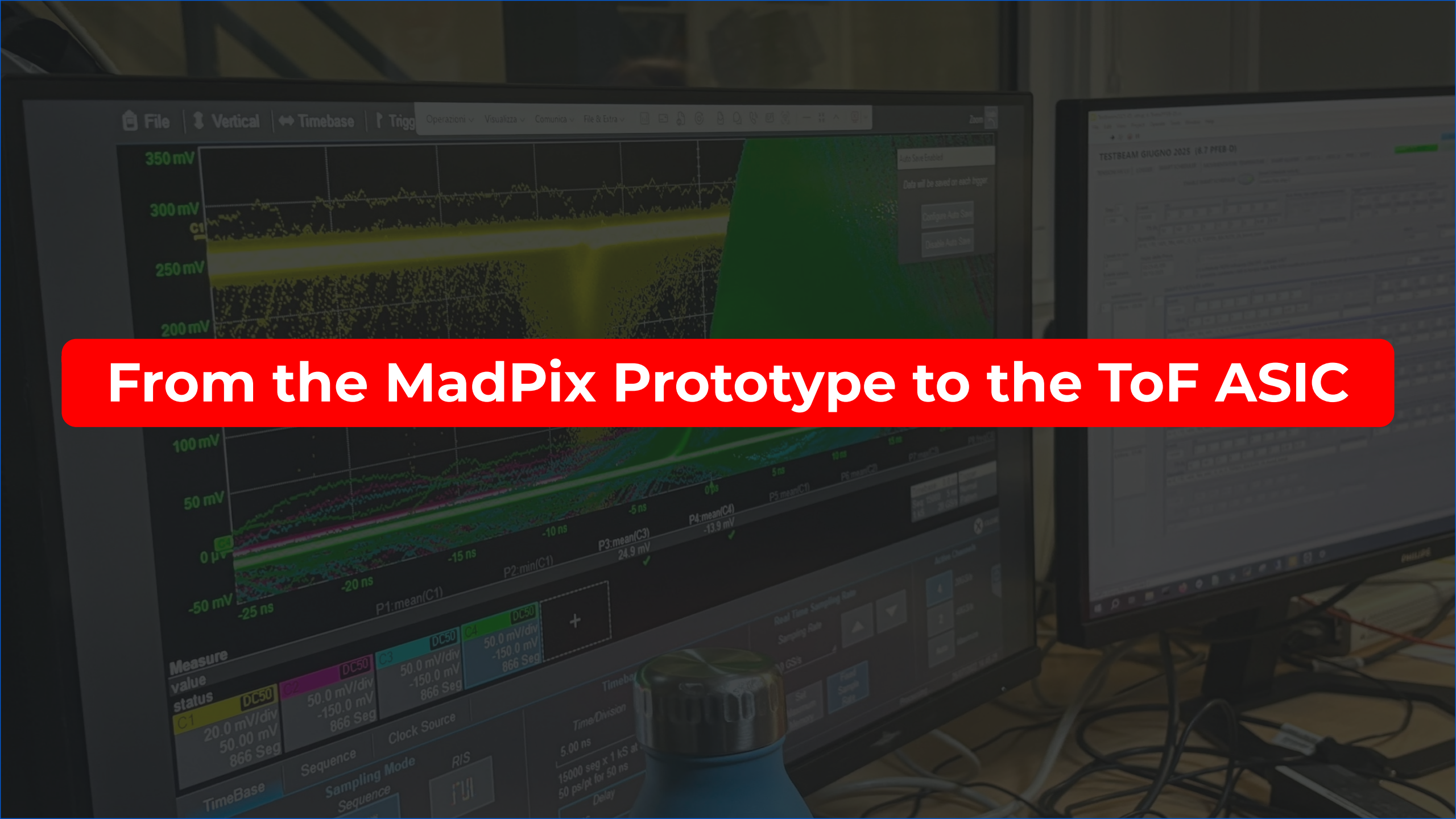
- A possibile mitigation strategy is based on recovering the gain by cooling down the sensor. At low temperature the mean free path of charges increases and this enhance the charge multiplication recovering the gain effect.
- Cooling below 0°C allows to recover a timing resolution between 70 ps and 75 ps after 10^{14} 1 MeV n_{eq} / cm^2 irradiation
- The testing setup used at PS employs a PWM controlled thermoelectric cooler coupled to the MadPix prototype and a water cooling system to remove heat from the TEC cell.







Courtesy of G. Gioachin, C. Ferrero, U. Follo from the Alice 3 Timing Layer Group


From the MadPix Prototype to the ToF ASIC

The timing resolution budget

Evolving from the protorype to the system-grade ASIC new contributions to the timing resolution must be taken into account.

$$\sigma_{preamp} = e_n \frac{C_d}{Q_{in}} \sqrt{t_d} \qquad e_n = \sqrt{\frac{2kT}{g_m}} \qquad g_m = \frac{I_{DS}}{n\phi_T}$$

$$\sigma_t = \sqrt{\sigma_{sensor}^2 + \sigma_{preamp}^2 + \sigma_{TDC}^2 + \sigma_{clk}^2}$$

< 10 ps

Gain and capacitance

Q_{in} proportional to the gain (→ SNR), C_d resulting from a trade-off between field uniformity and its negative impact on SNR.

Front-End Power Budget

The timing resolution of the front-end is the result of a complex trade-off with power consumption. Currently we plan to allocate **up to 200 uW / pixel for the AFE**.

< 18 ps

Sensor field uniformity and Landau noise

High field uniformity required, reduced distortion, minimization of edge effects. **Price to pay: the charge collection efficiency**

< 10 ps

TDC resolution

High-resolution ADCs needed, tight constraints on the jitter of the trigger electronics and of the current steering switches

< 5 ps

Jitter of clock network

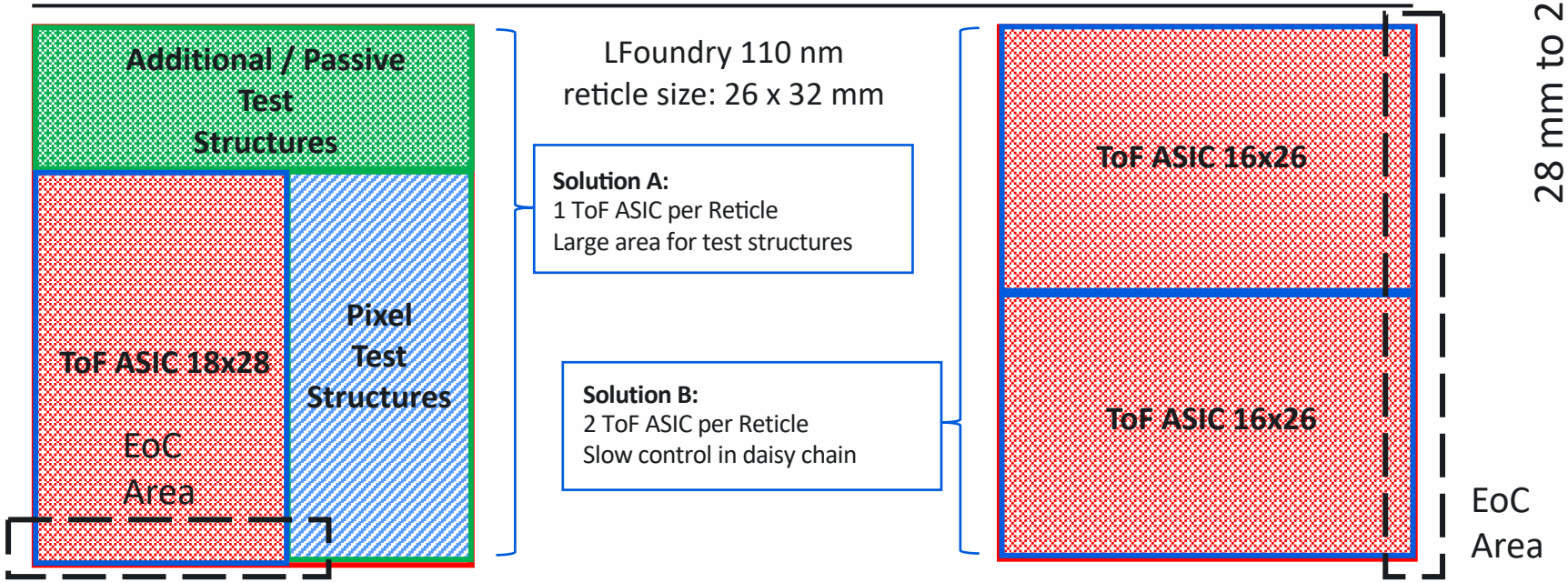
On-chip PLL needed for jitter cleaning, transmission line clock distribution, or **linear distribution topology reduced to a small area of the chip**

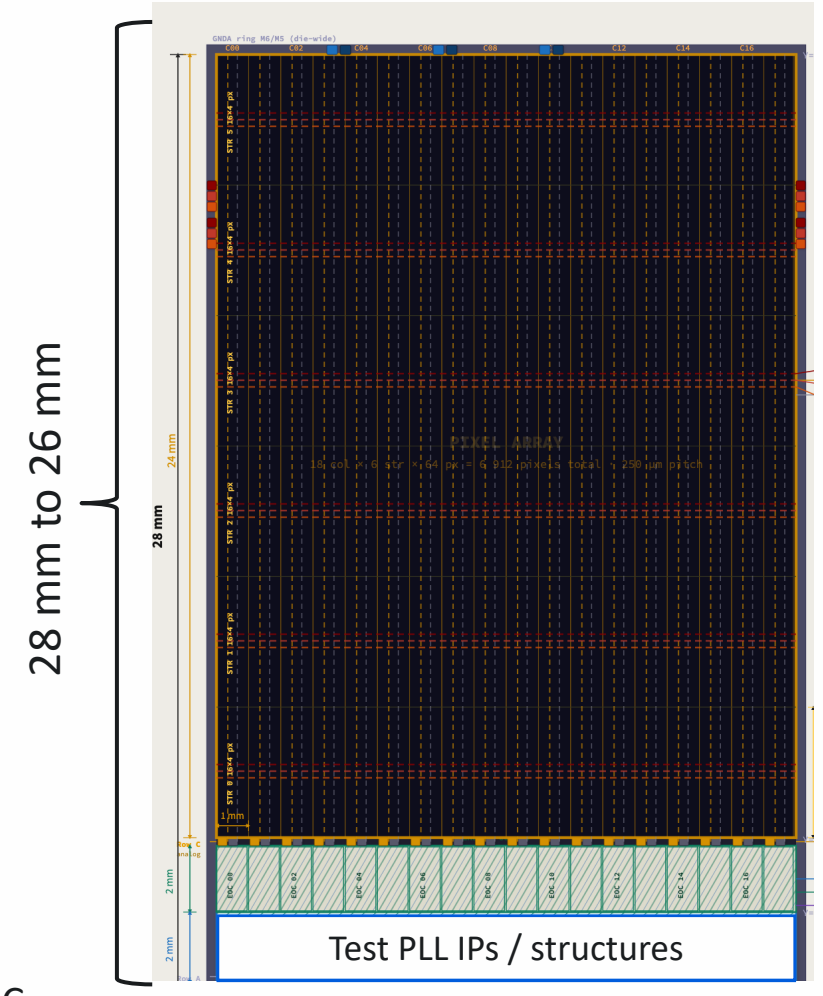
The timing resolution budget shold be allocated to leave large headroom to the sensor.

Proposed Architecture: specifications

- The proposed floorplanning for the system ASIC production foresees to fill the reticle with two ASICs with size **26 mm x 16 mm**, with **1 mm wide columns.** Each column has a sensitive area of **24 mm x 1 mm,** a mixed-signal End-of-Column of **2 mm x 2 mm** including the TDCs, the readout logic and a PLL.

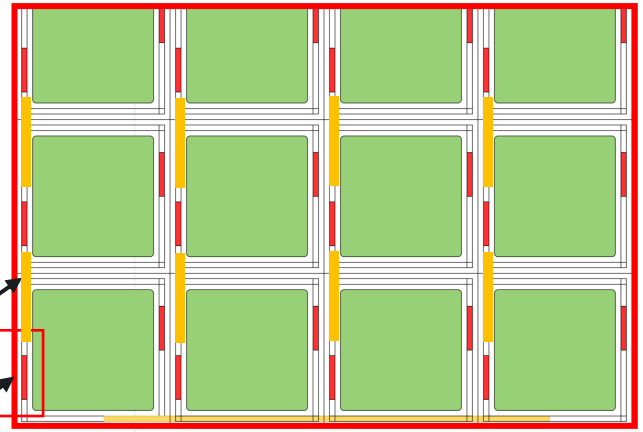
- A larger number of columns and an additional EoC region of **2 mm x 2 mm** could be added during the first run in order to test respectively **multiple pixel configurations** and **multiple PLL / clock distribution IPs** directly connected to the system.



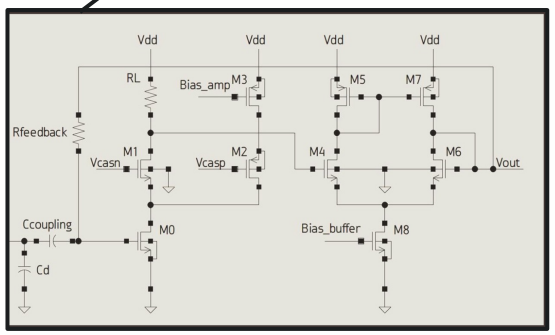


Proposed Architecture: floorplanning

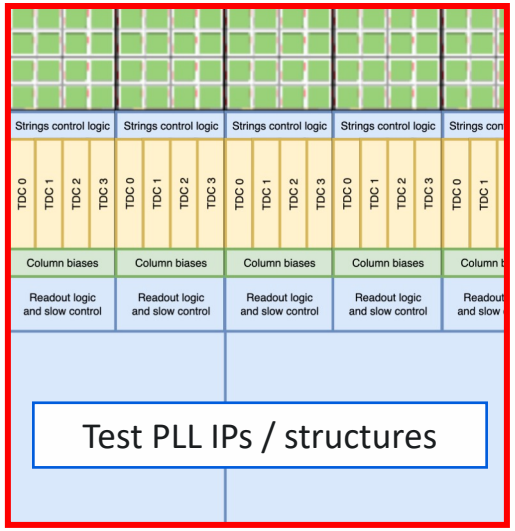
- Each column is divided into **6 pixel strings** containing each one **4 x 16 pixels** with currently investigated size of 250 µm x 250 µm
- Each pixel features an optimized version of the MadPix front-end, a fast asynchronous discriminator an provides an output trigger to the string digital logic
- The string logic extracts the rising and falling edges (for ToA and ToT) and send them to the EoC with the firing pixel address
- In the EoC four TDCs are placed with the readout logic and PLL.

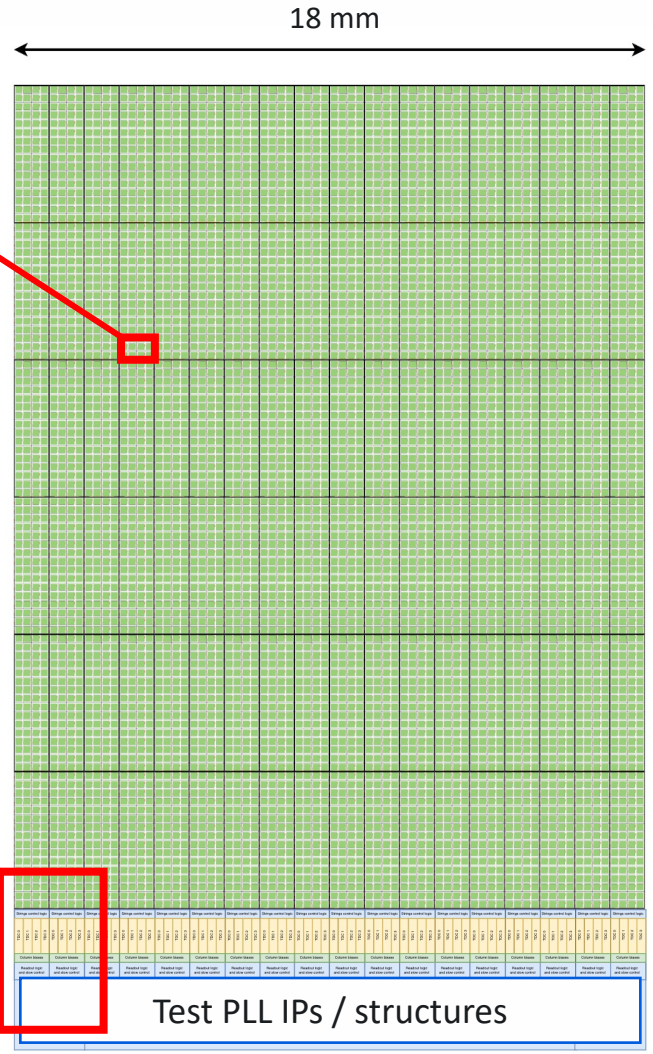


Pixel / String asynchronous digital logic



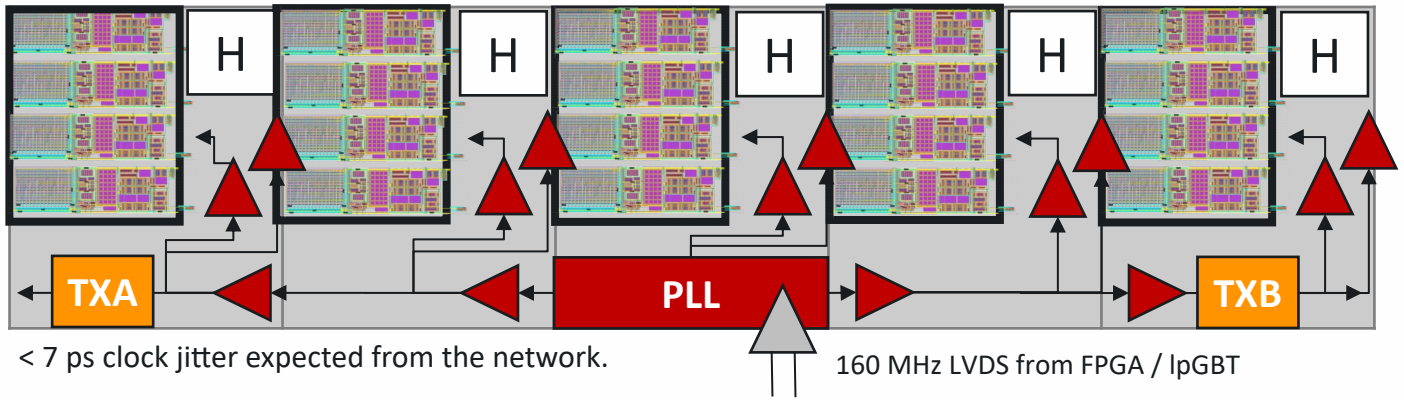
Analog Front—End (1.2 V) adapted from MadPix with minor changes



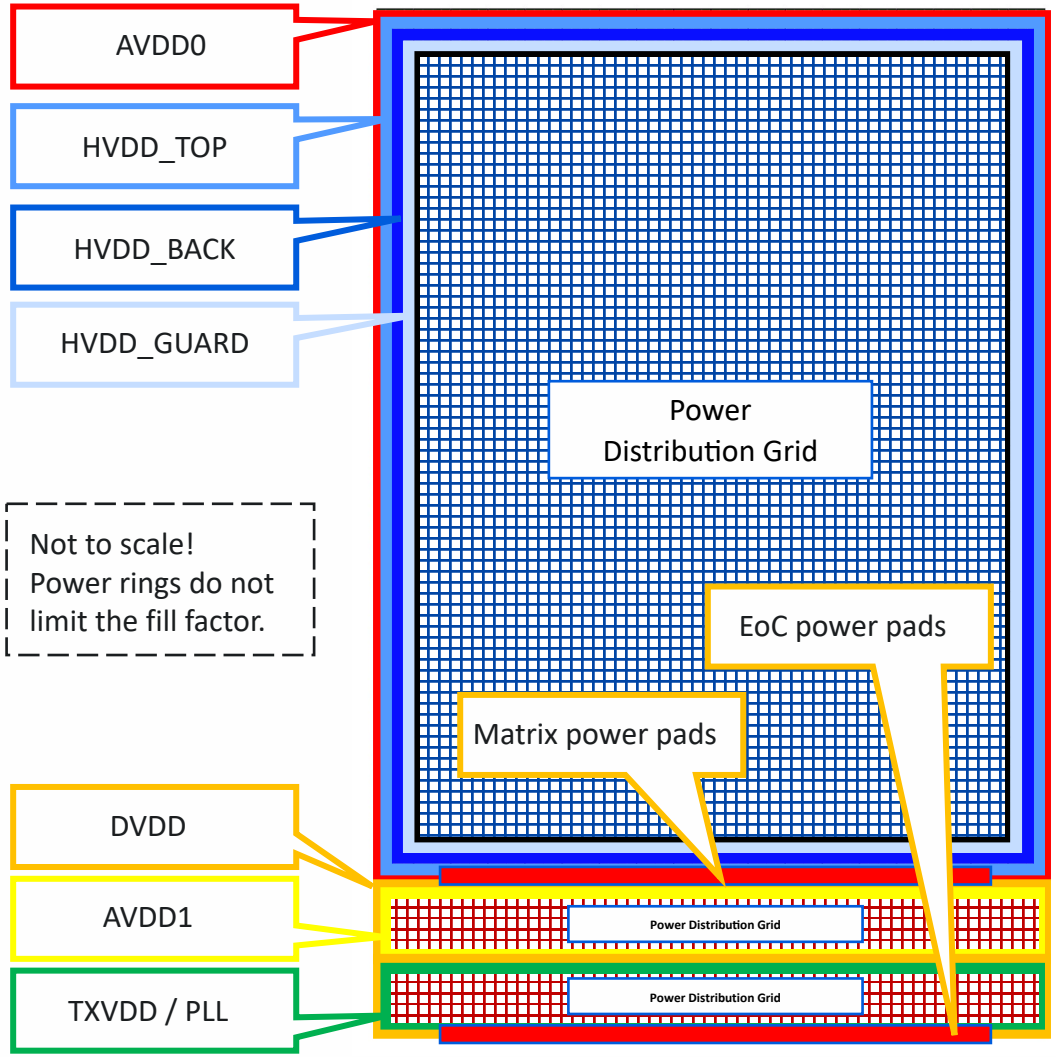


Proposed Architecture: clocking & power planning

- The **160 MHz clock** is not distributed to the large pixel matrix, but is processed by a jitter-cleaning PLL and then distributed with almost constant skew between the EoC blocks. On each block there will be a dedicated clock network for the TDC in addition to the standard logic H tree to reduce the number jitter contributions due to buffers.

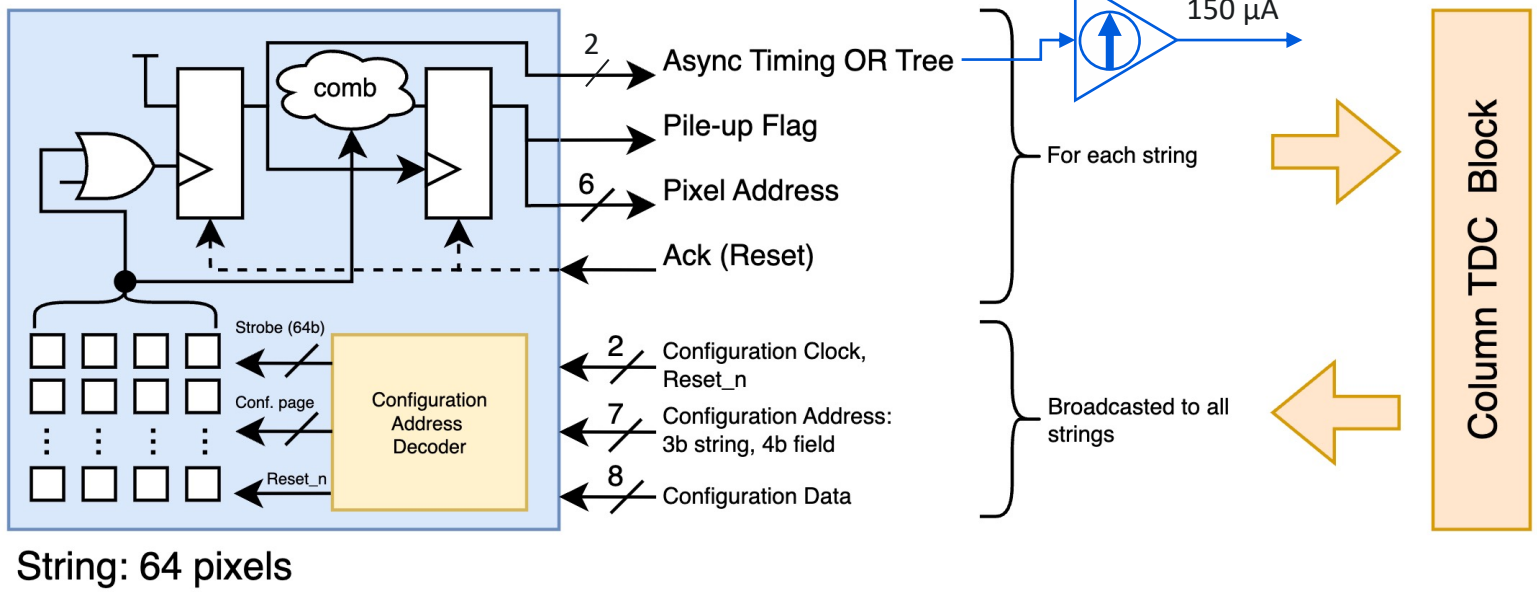


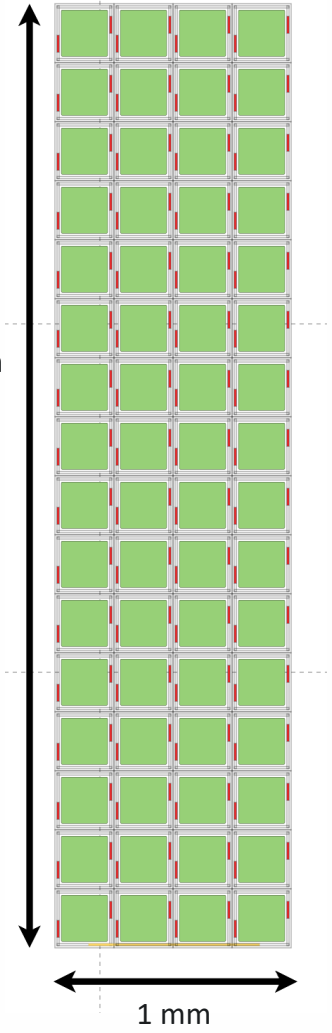
- **On the pixel matrix three sensor polarization power domains** are distributed with an additional analog power domain for the Front-End electronics. Logic gates are connected to the analog domain since they are fully asynchronous and event driven.
  - AVDD0 expected power: about 200 µA / pixel ↦ about 350 mW / cm^2
  - < 50 mV expected IR-Drop, almost fully static
- **On the ASIC periphery:**
  - **AVDD1** expected power 60-80 mW total, almost static dedicated to current-steering time-to-analog conversion
  - **DVDD** expected power 85-100 mW total, dynamic, powering the digital logic
  - **TXVDD / PLL** dedicated to the clock distribution network, serializers and PLL, to be carefully regulated. Power consumption TBD.



Proposed Architecture: logic and readout

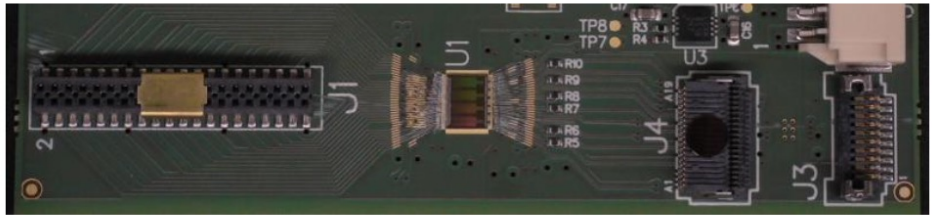
- Each pixel string has a **single core of shared asynchronous control logic**, driven by the output of the 64 discriminators in each pixel.
- A **balanced OR tree** is used for generating a **trigger signal that is latched on its positive** and it trigger the latching of the output of the combinatorial encoder that generates a **6-bit address of the firing pixel**
- This signal enables as well a negative triggered FF that **latches negative edge for ToT measurement.**
- A pile-up flag is asserted if any other pixel fires while these signals have already been latched
- All the FFs are **reset by an asynchronous ACK signal** sent back **from the TDC End-of-Column** block.
- The two timing outputs after latching are transported to EoC **using two current-mode channels** instead of a CMOS digitalsignal that needs several repeaters with strong mistmatch and PVT sensitivity
- The logic manages also the pixel-level adjustable discriminator threshold

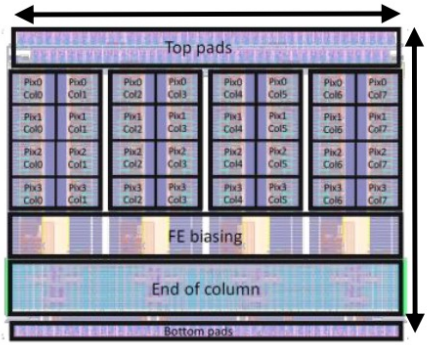


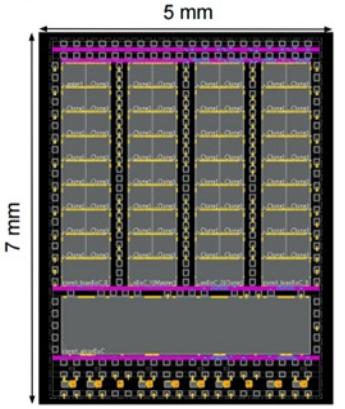


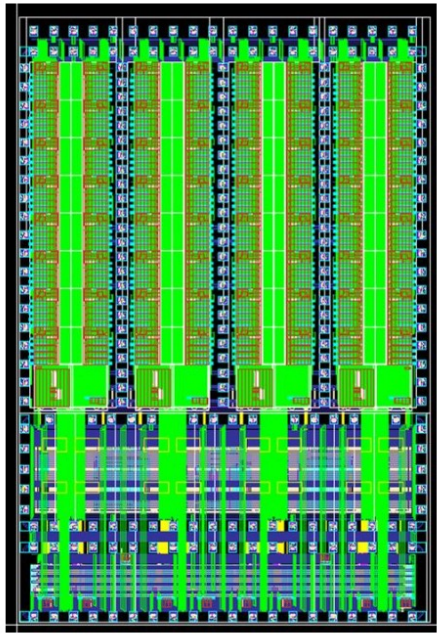
Taking advantage from previous experience: Alcor

- **ALCOR v1:** Mixed-signal ASIC for **SiPM** readout, *Darkside* framework (2019)
  (**A** **L**ow power **C**hip for **O**ptical sensors **R**eadout)
  (PhD Thesis, W. Cheng, Polito: https://iris.polito.it/handle/11583/2842529)
  - UMC 110 nm
  - 32 channels, 4.95 x 3.78 mm^2
  - 440 x 440 μm^2 pixel channel
  - Single-photon time tagging and ToT , compatible with both signal polarities
  - LVDS digital output, 320 MHz DDR Tx links
  - ≈12 mW/channel
  - Tested at room temperature and in liquid Nitrogen
- **ALCOR v2.0/.1 and v3** ASICs for the dRICH EIC Detector at BNL (NY, USA)
  (XII Front-End Workshop, Torino, link : https://agenda.infn.it/event/37033/contributions/228026/)
  - Scaled to 64 channels
  - V2.0: 2023 MPW and engineering run, debugged and optimized for the EIC detector
  - V2.1: 2024 (Jan) Engineerig run, currently under test
  - V3 : Final version, Silicon available in 2025









From 32 to 64 channels

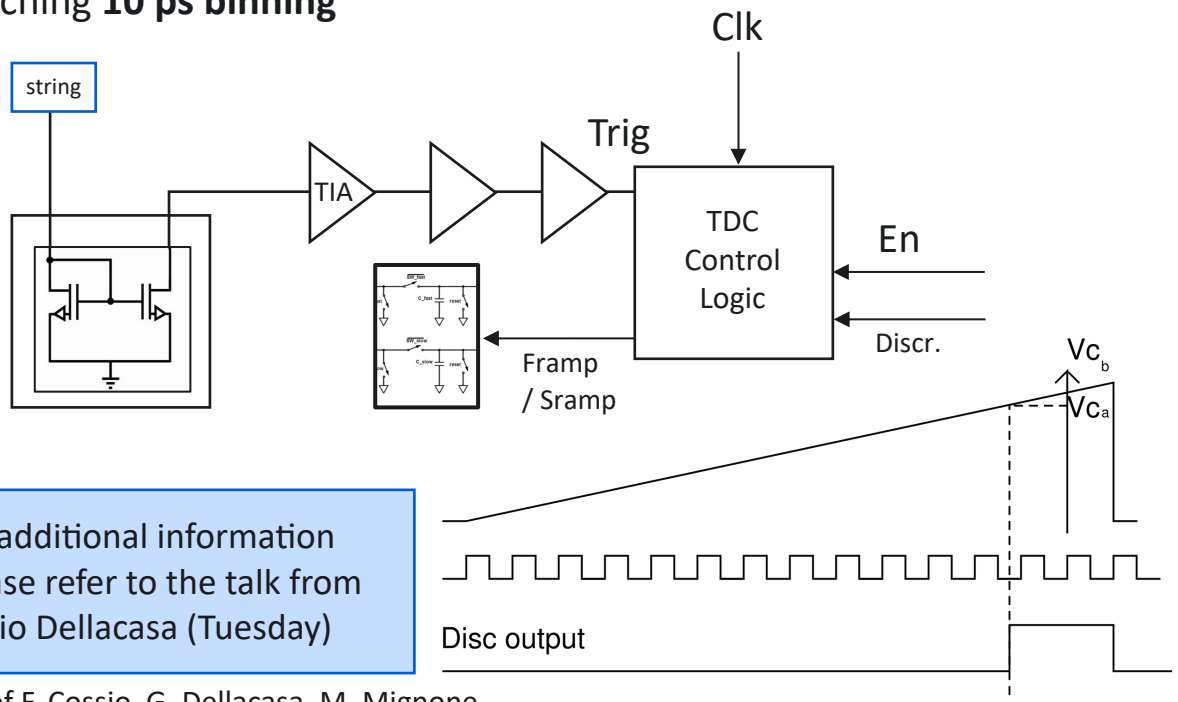
For additional information please refer to the talk by Giulio Dellacasa (Tuesday)

Courtesy of F. Cossio, G. Dellacasa, M. Mignone

Porting the Alcor TDC

- The Time-to-Digital converter from Alcor needs a retuning of MOMCaps and current sources in order to cover the **3.3 ns - 10 ns dynamic range.** The digital switches needs to be controlled by a current source: introducing an **ultra-fast binary TIA.**

- The resolution of the Wilkinson ADC needs to be increased to **10 bits**, reaching **10 ps binning**



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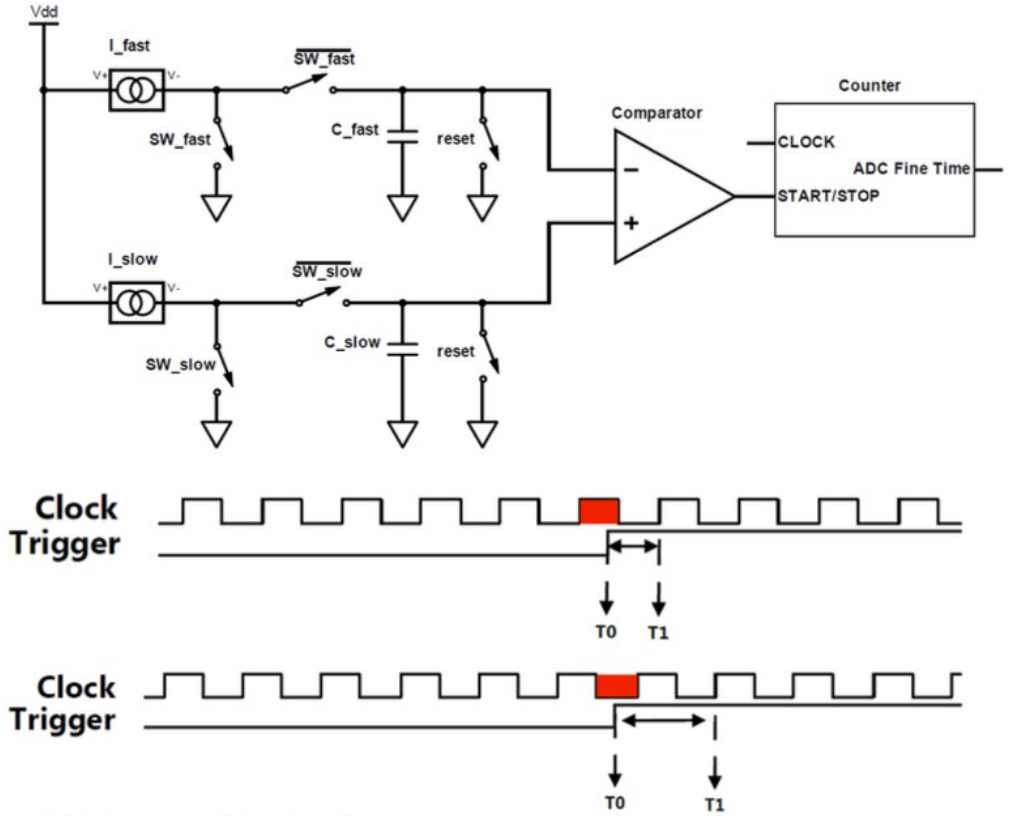
Courtesy of F. Cossio, G. Dellacasa, M. Mignone



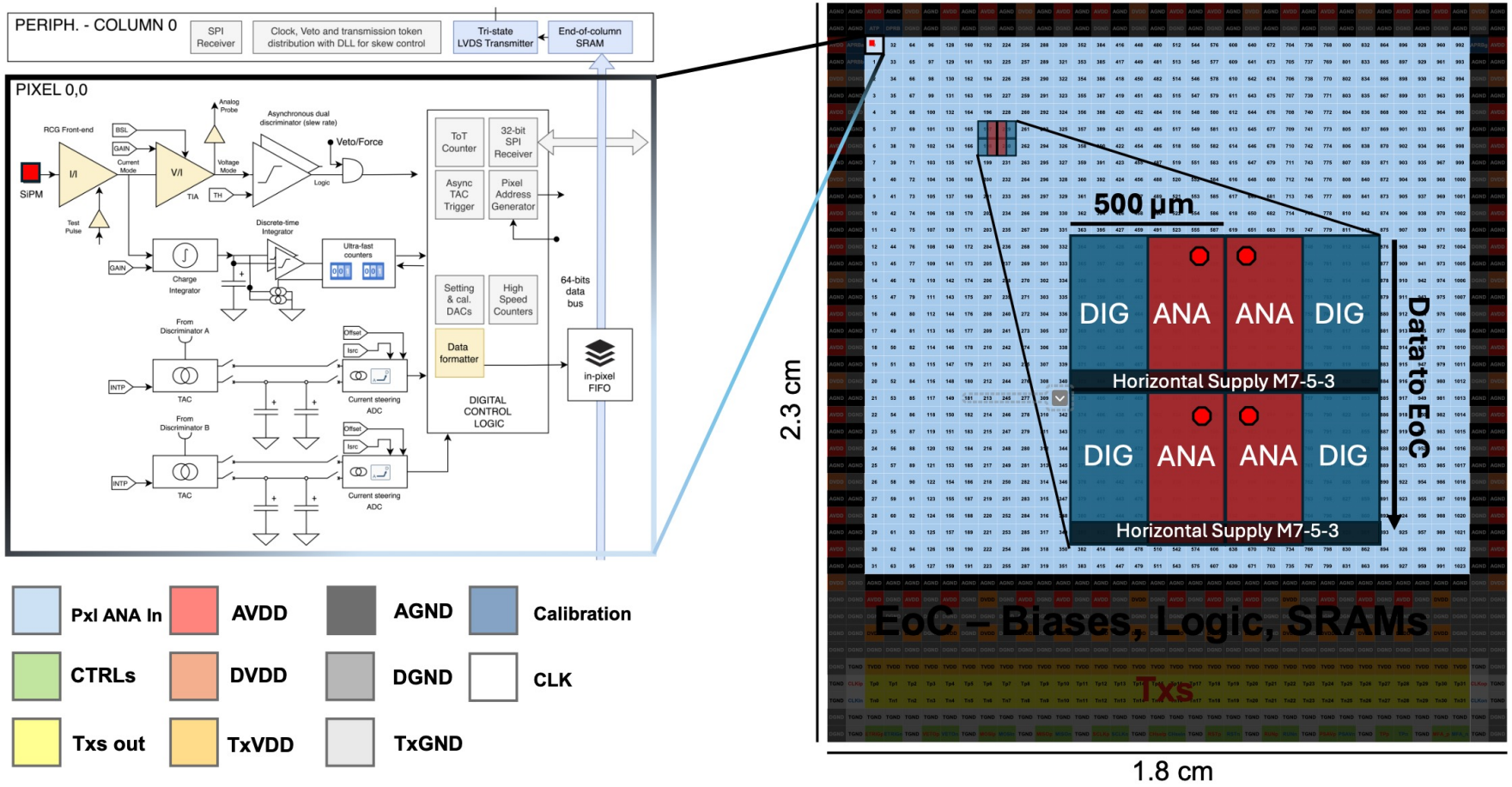
T_0 Before Clock Falling Edge:
If the trigger (T_0) occurs before the clock's falling edge, the fine time is measured between T_0 and the next clock rising edge (t_1).

T_0 After Clock Falling Edge:
If the trigger (T_0) occurs after the clock's falling edge, the fine time is measured up to the *second* rising edge. In this case, the full timestamp is obtained by adding one clock period to the fine time.

Taking advantage from synergies: Deneb

- The readout architecture is based on the previous experience of our design team with the modular logic of the DENEB 1024-channel ASIC
- The TDC EoC block of the Alice 3 ToF ASIC can be easily managed by the DENEB Pixel logic
- The Data Transmission EoC of the Alice 3 ToF ASIC can be implemented porting the DENEB End-of-Column Logic.

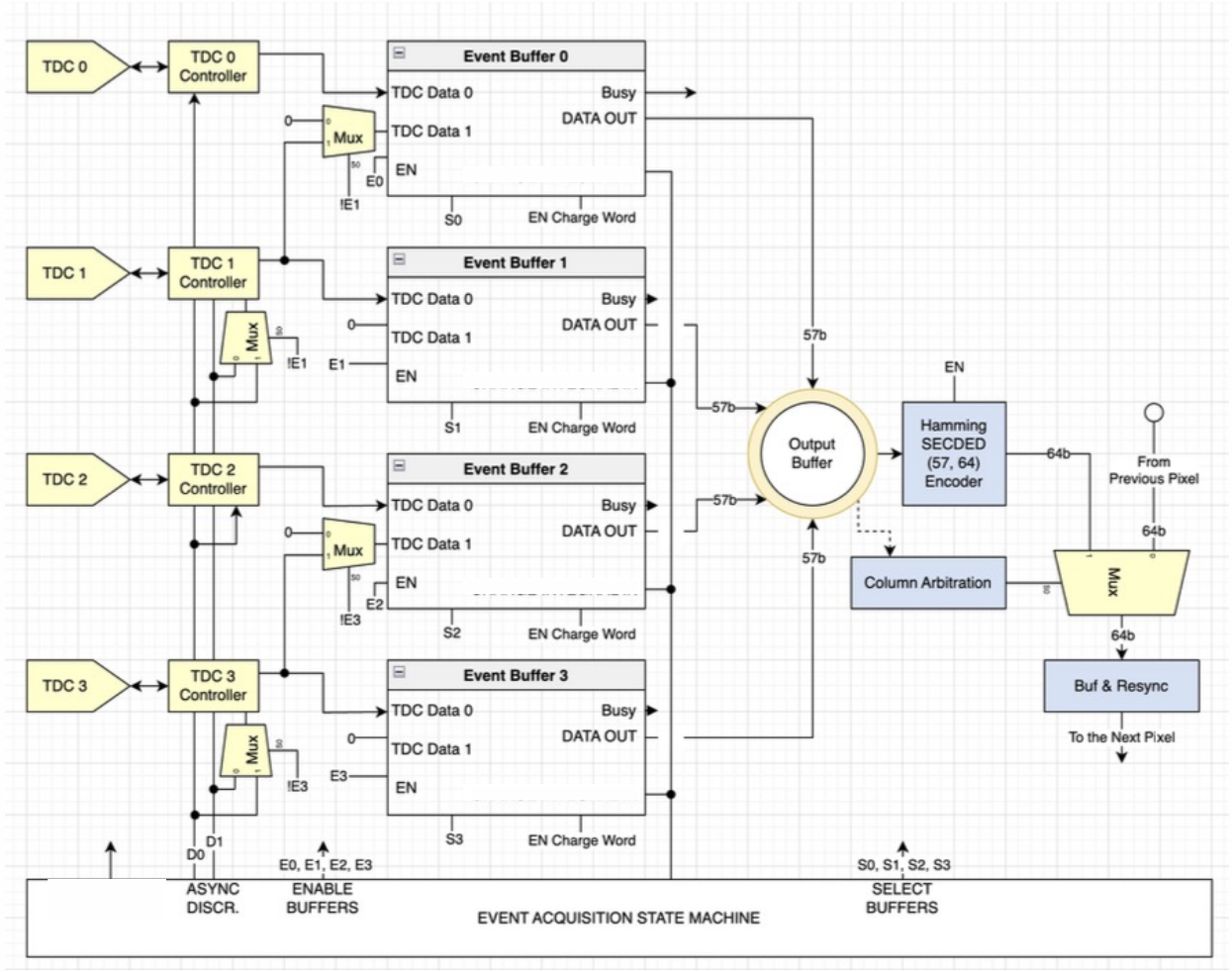
For additional information please refer to the talk from Stefano Durando (Tuesday)



Porting the Deneb Readout Logic to the ToF ASIC

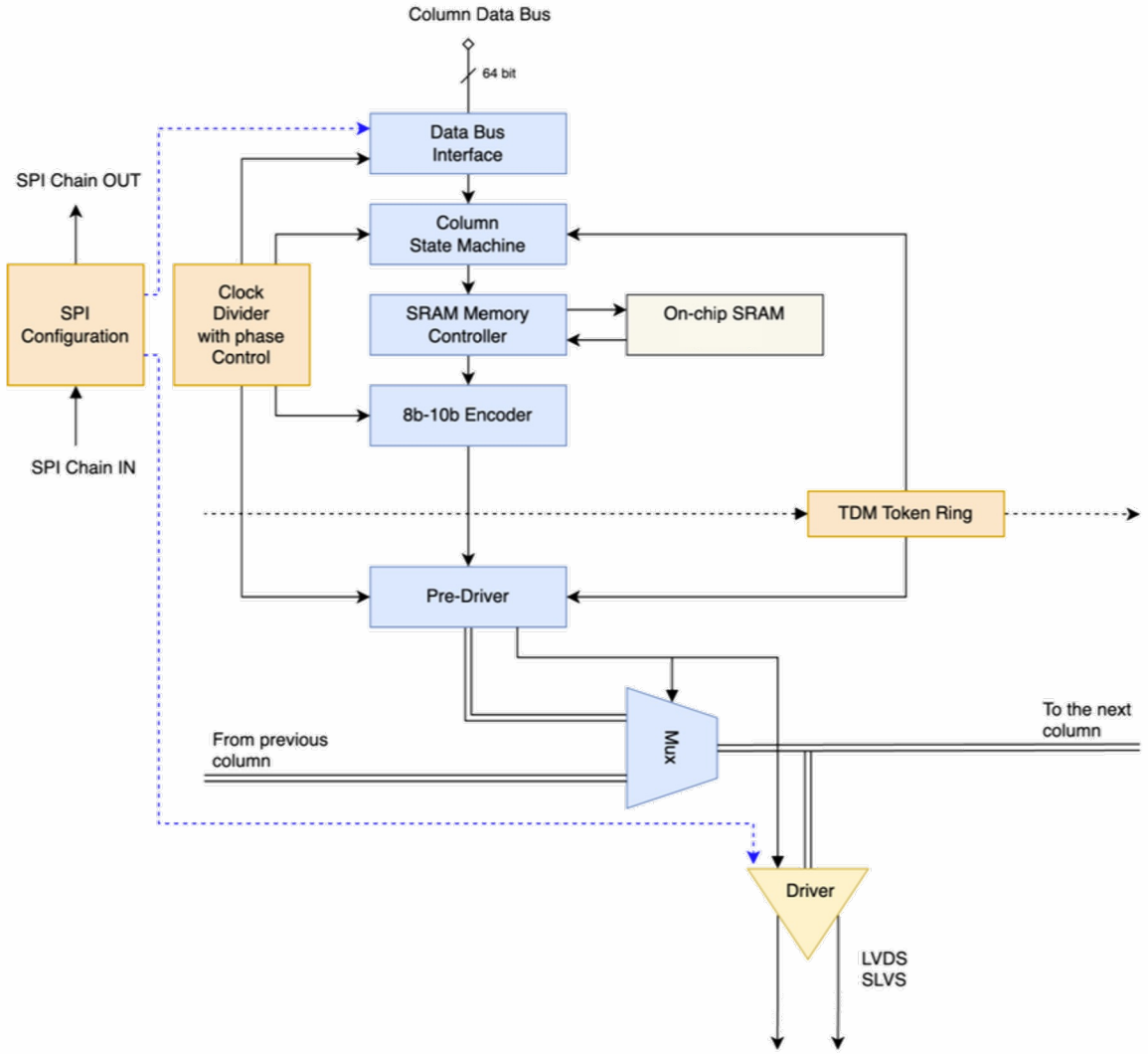
- Each TDC is connected to a dedicated Event Buffer with an internal state machine that monitors the TDC busy status. The output buffer waits for the slowest TDC to assert the valid flag on the data word, that is forwarded to the column arbitration.

Start Bit	Stop Bit	Width	Field
63	34	30	Header + TBD (Lost counter…)
33	30	4	Column Address
29	27	3	String Address
26	21	6	Pixel Address
20	6	16	Coarse Time
5	2	4	Delta Coarse
1	1	1	Lost Event Flag
0	0	1	Pileup Flag



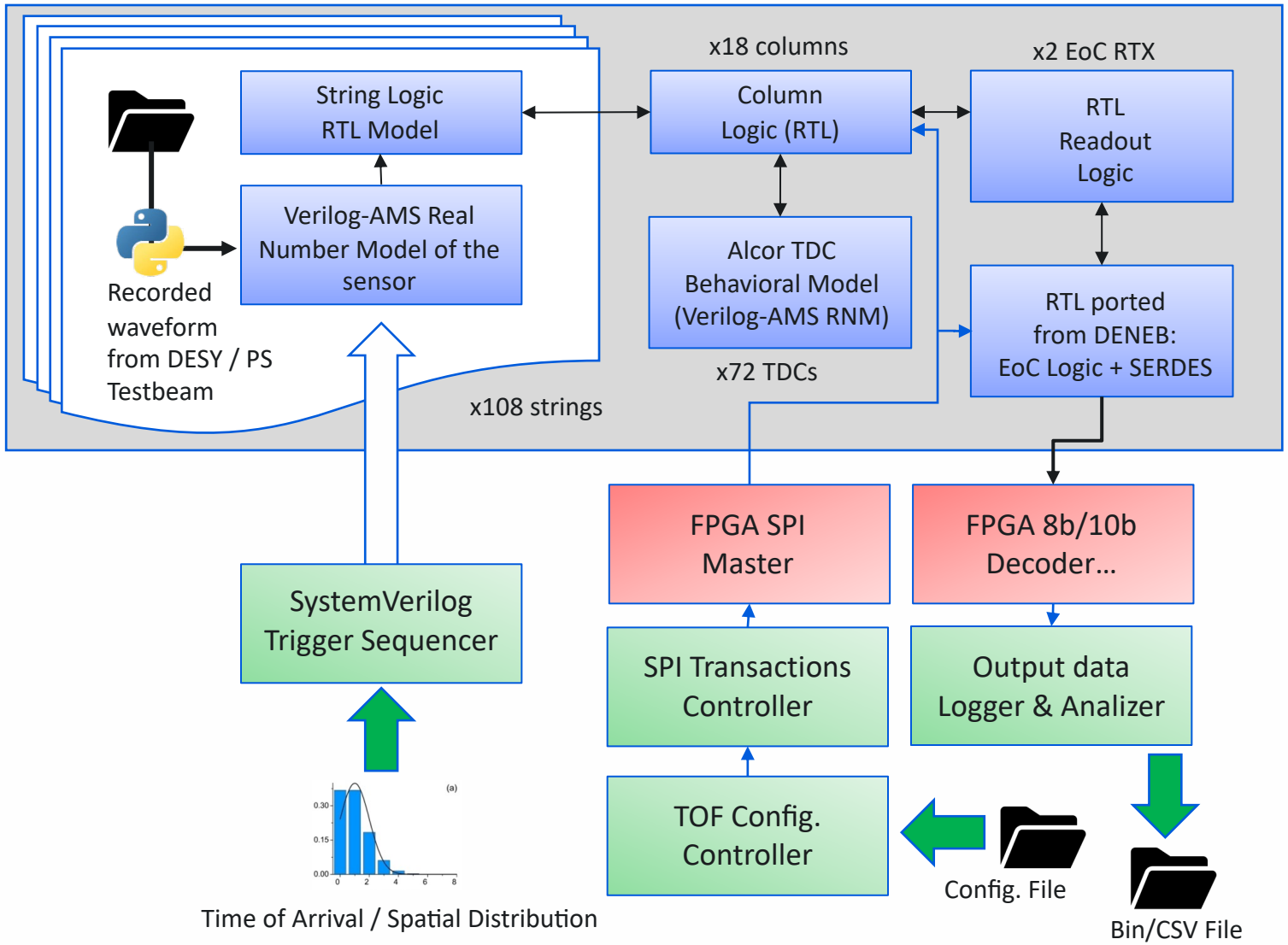
Porting the Deneb End-of-Column Logic

- The 64-bits data words are streamed using a shift-register like approach with local arbitration from each EoC TDC block to the adjacent one, thus simplyfing the timing closure with respect to a direct EoC TDC block to data transmission block communication
- Two data transmission blocks are foreseen (8 column each one) running at 160 Mbit/s SDR supporting 1.6 MHz continuous event rate for each column. (< 1.15 MHz corresponding to 300 kHz / cm^2 hit rate with the current frame data overhead).
- Each EoC data transmission block features a 32 words SRAM FIFO
- Each EoC data transmission block can share the data stream with the block nearby, for reducing the number of necessary links, for readout density limited applications.



System-Level AMS Simulations: flow

- This architecture is being investigated using a mixed SystemVerilog RTL / Verilog AMS simulation environment
- Digitized Waveform from the DESY and CERN PS testbeams are used as stimuli for the discrimininator model, they are replayed by a hit generator sequencer.
- The synthesizable IPs of the SoC-based test system are used as verification IPs for decoding the output data stream
- The great advantage of this hierarchical approach is the possibility to replace single blocks with netlist-level implementations and being able to simulate them within the whole system



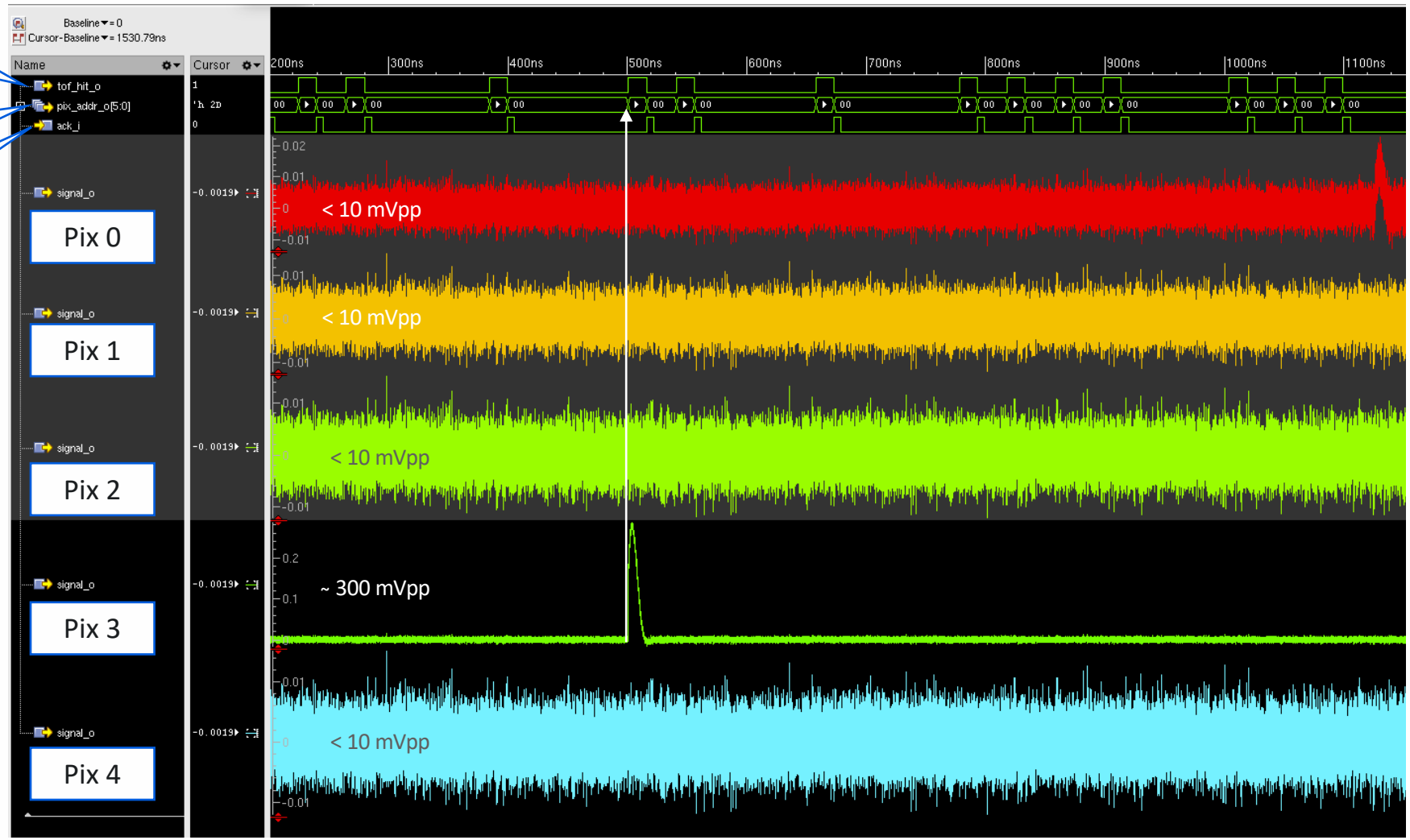
System-Level AMS Simulations: the string

- The waveform of the incoming analog signal from the front-end is produced from recorded data during testbeams

- The superposition of the pulses is driven by a sequencer sampling a parametric poissionian distribution

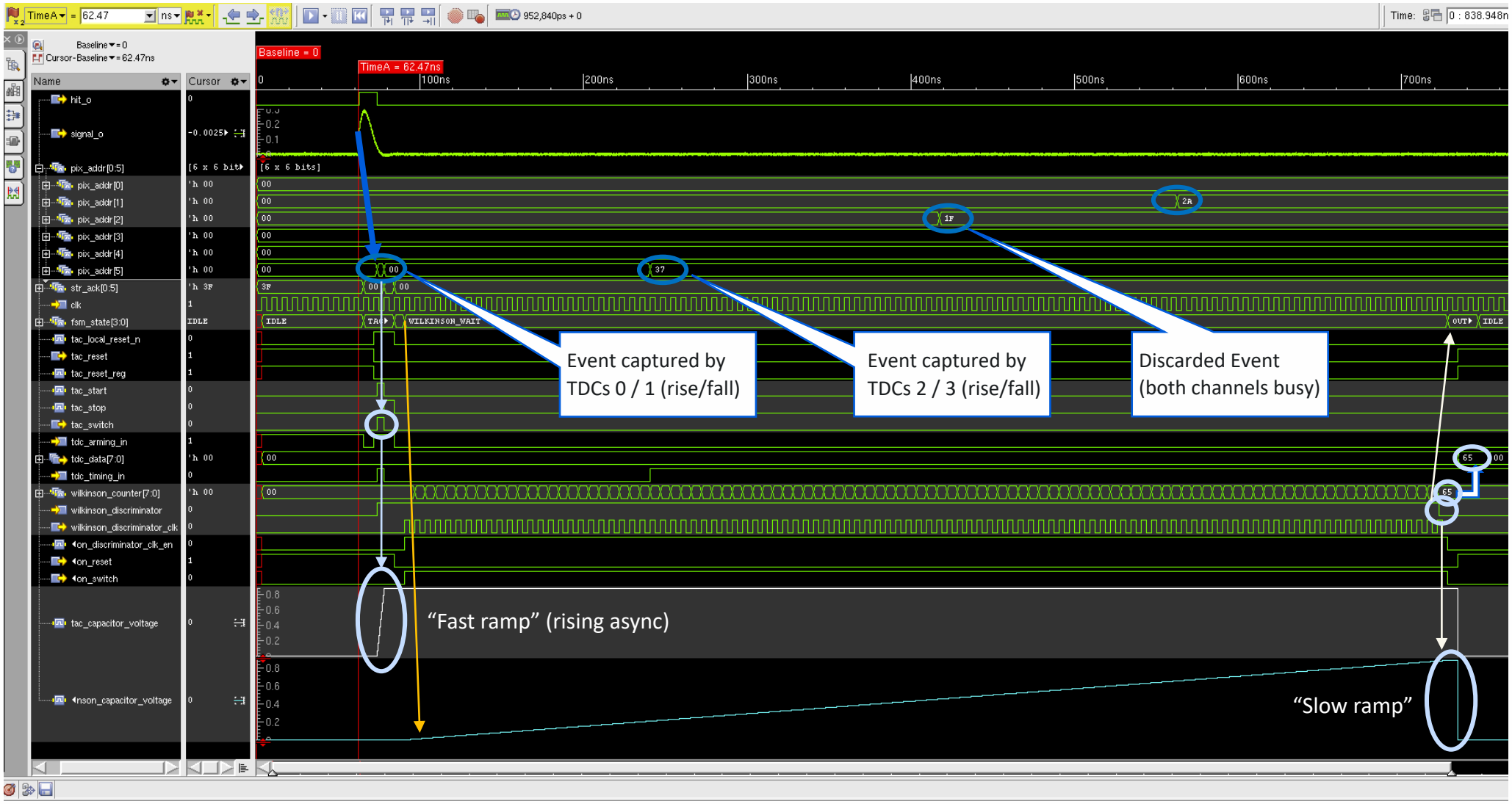
- At the top, some of the digital signals from the pixel string to the End-of-Column logic are shown

- **The pixel string logic is capable of handling more than 5 MHz event rate with < 0.5% fraction of loss events.** That is order of magnitude higher than the expected rate at 300 kHz cm^2



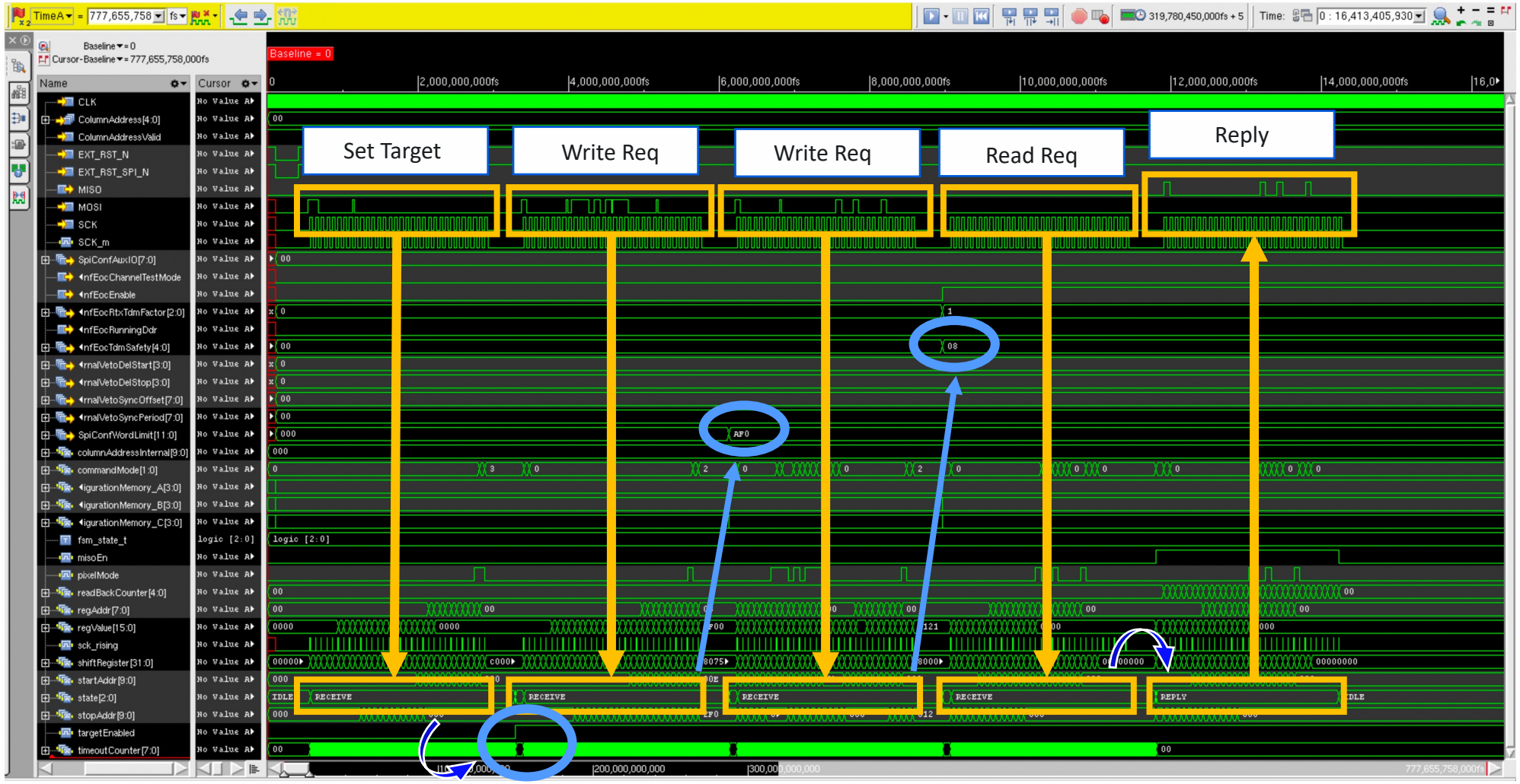
System-Level AMS Simulations: TDCs

- In this Verilog AMS model the behaviour of the TDC is analyzed
- The limiting factor on the peak event rate of the ASIC is the dead time of the TDC.
- Nevertheless, with two TDC pairs (ToA, ToT) per column for derandomization with 10 bit resolution, the efficiency is well above 95.5% with 300 kHz / cm^2 hit rate.



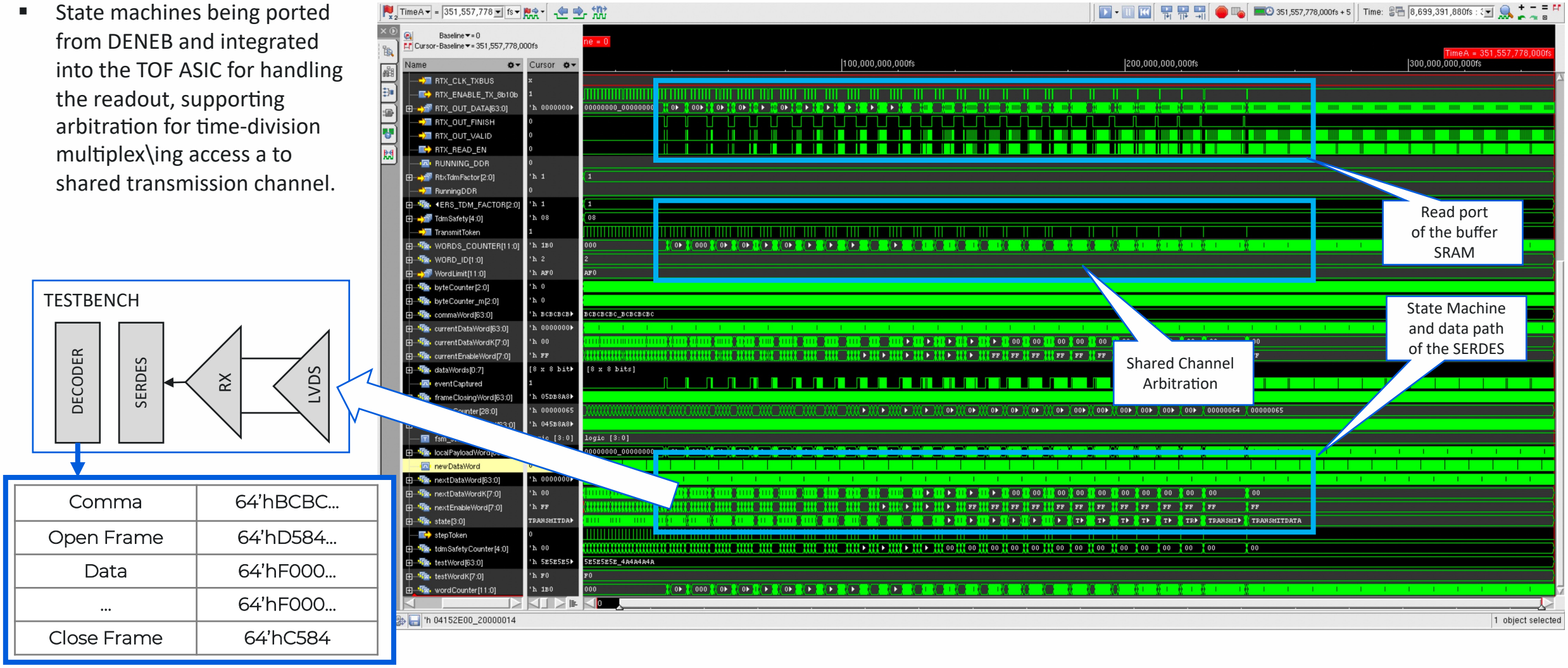
System-Level AMS Simulations: SPI configuration

- Simulation of the SPI slow control system being ported from the DENEB ASIC
- It is based on a unicast / multicast configuration architecture optimized for large ASICs with pixel-level SPI receivers that can handle multicast / broadcast packets for reducing the configuration time.



System-Level AMS Simulations: End-of-Column

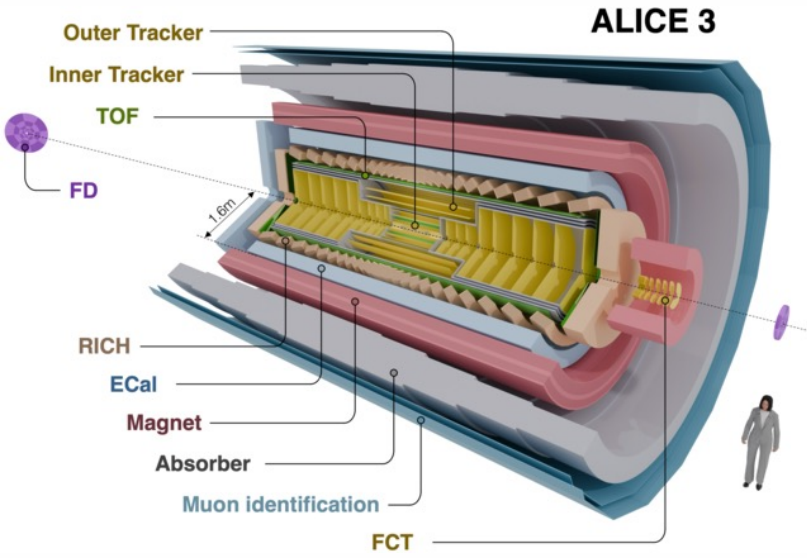
- State machines being ported from DENEB and integrated into the TOF ASIC for handling the readout, supporting arbitration for time-division multiplex\ing access a to shared transmission channel.



Comma	64'hBCBC...
Open Frame	64'hD584...
Data	64'hF000...
...	64'hF000...
Close Frame	64'hC584

Conclusions

- A roadmap for producing a 110 nm monolithic CMOS LGAD for timing applications started in 2023, embedded into the ARCADIA platform.
- The MadPix prototype allowed to validate with measurements the feasibility of reaching **up to 80 ps** timing resolution on the whole pixel and **up to 65 ps** timing resolution in the central uniform field region.
- Radiation and temperature effects has been investigated and seems not to be critical for achieving the required TID tolerance
- The targeted resolution of **20 ps** is expected to be reached with the 3.3 shortloop that will be tested in some weeks, according to the TCAD simulations.
- In the meanwhile, the **system-level design and simulation of the system-grade ASIC started**, leveraging **a strong synergy with other 110 nm projects** such as ALCOR and DENEB to reuse silicon-proven IPs.



Thank you!