XIII FEE Workshop 2026 - Paris

A Low-Power Fully Depleted Monolithic CMOS Pixel Detector with Time and Charge Measurement for Space-Based Compton Imaging

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Politecnico di Torino

Space Compton Telescope

Science Driver

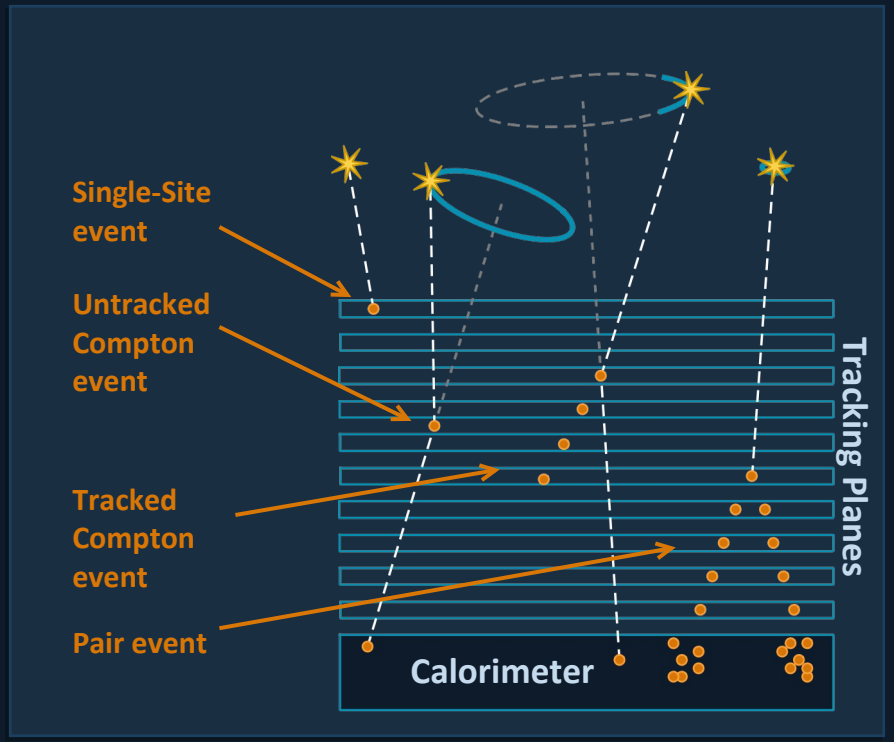
MeV Gap

Target the MeV gap (100 keV – 1 GeV) currently invisible to Fermi-LAT (20 MeV – 300 GeV) → AMEGO-X
Needed for studying extreme accelerators and multimessenger sources, including supermassive black hole jets (**blazars**), **binary neutron star mergers** (gravitational wave counterparts), and **Galactic supernovae**

Detection Principle

Characterize gamma-rays:

- **Single-site (< 100 keV)**
  - Increases sensitivity for low-energy transients, just triggers one pixel (Photo-electric effect)
- **Compton Scattering (< 10 MeV)**
  - Measures the energy and position of the interaction to determine the initial scatter angle (ϑ)
- **Pairs Production (> 10 MeV)**
  - Tracks the electron-positron pair to reconstruct the incident photon's direction



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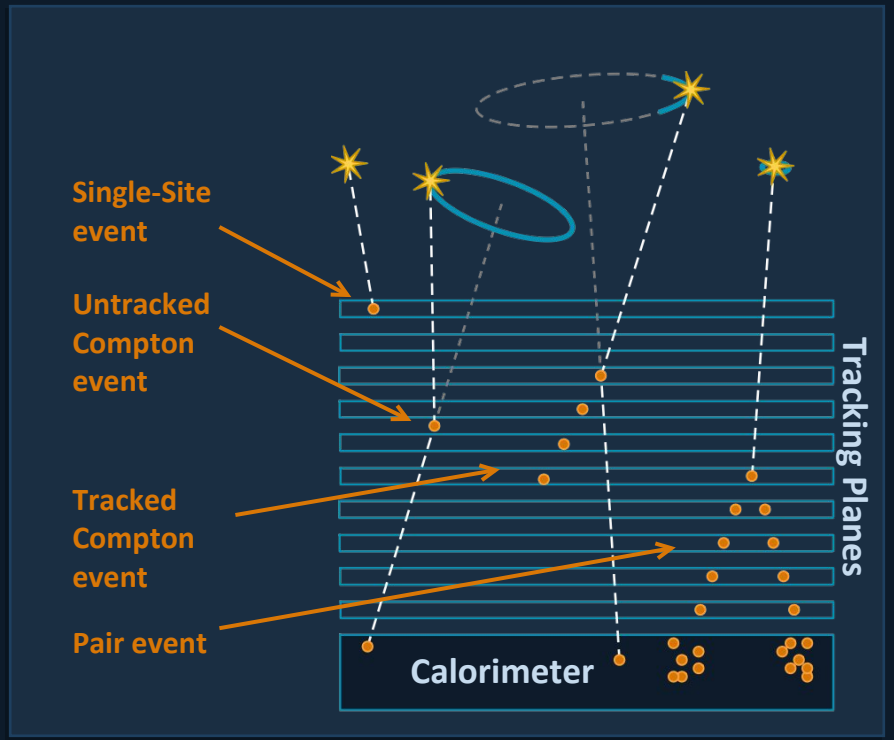
Requirements:

- Low power consumption **< 10 mW/cm^2**
  - **6.25 µW/channel @ pitch 250 µm**
- High input energy dynamic range **[10^1, 10^9] keV**
- **Low rate 10 Hz/cm^2**
- Low noise **SNR > 10 & ENC < 200 e$^-$**
- Timing Resolution **200 ns rms**
- Energy Resolution **10% @ 60 keV**
- Space graded working range **[-35, 50]°C**



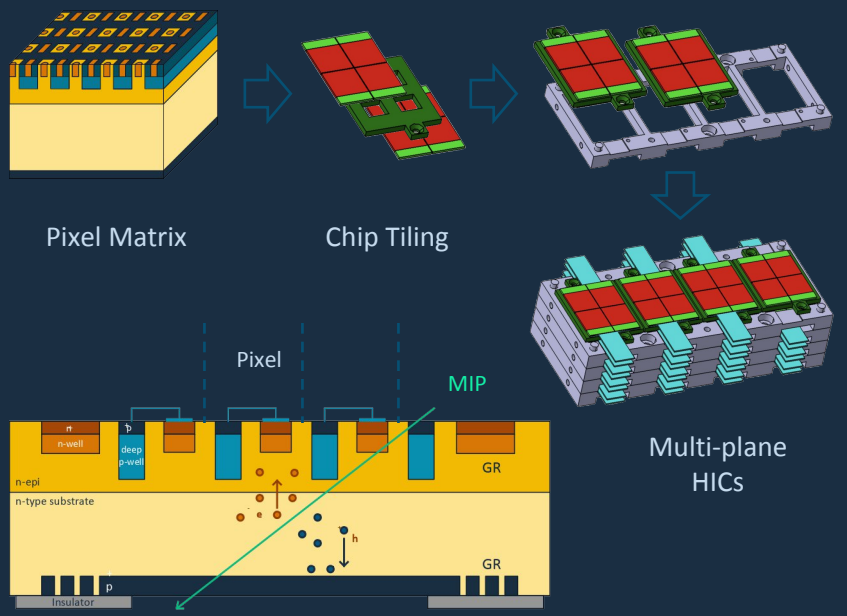
Why a MAPS for space-borne γ-ray detection?

ARCADIA FD-MAPS

Monolithic integration
- **Sensor + Readout on same wafer**
- **Electronics buried in deep p-wells**

ARCADIA heritage
- **110 nm** CMOS custom process (LFoundry)
- N-type high resistivity active region
- Backside reverse biased juction
  - Fully Depleted (FD)
  - Depletion grows up to the top
- N-type epitaxial layer to limit punch-through current
- Proven up to 400 µm FD substrates

>500 µm - thick FD-MAPS
- Increase the interaction probability (**stopping power**)
- Maintain low power consumption



ARCADIA Collaboration

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays · INFN CSN5

Technology Platform

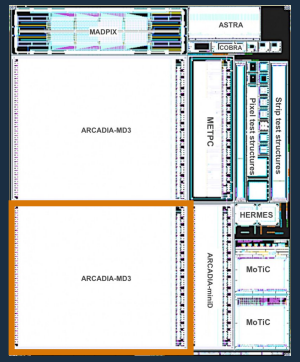
R&D in semiconductor sensor technology IP-core design, mixed-signal ASICs, and advanced DAQ systems all on the INFN-LFoundry 110 nm CIS process

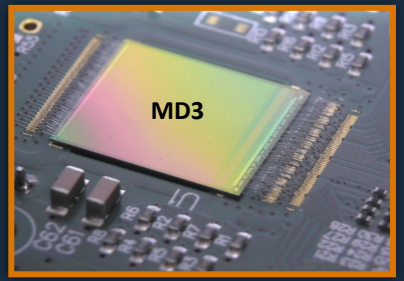
Applications

High-energy particle physics (vertex & tracking), astroparticle physics in space, medical instruments, nuclear imaging & dosimetry

Key Achievements

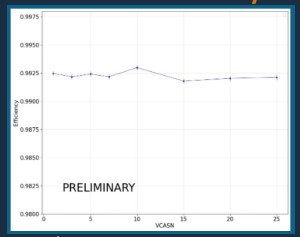
- High-granularity MAPS down to **5 µm** spatial resolution
- System-ready MD3 demonstrator
  - **512×512** pixels, 1.64 cm²,
  - **17 mW/cm²** in low-rate mode
- **CMOS LGAD** targeting timing performances better than **20 ps rms**
- Monolithic strip sensors with embedded electronics for space-borne applications





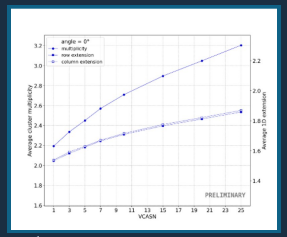
- Test beam at FNAL with 120 GeV protons
- Single-point resolution **~ 4.7 µm**
- average efficiency **99.23%**

Detection Efficiency



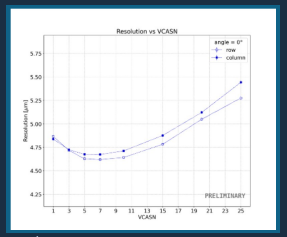
V_{th}

Cluster Size



V_{th}

Resolution



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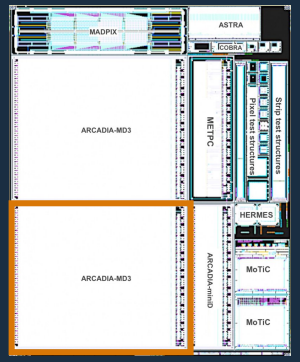
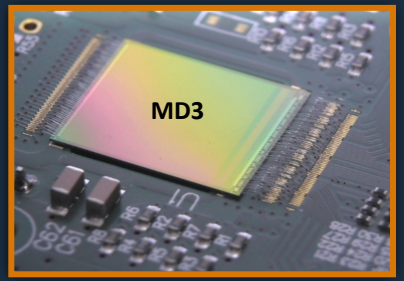
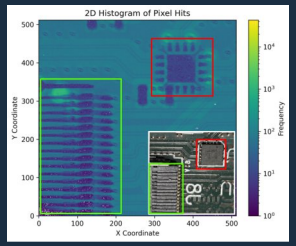
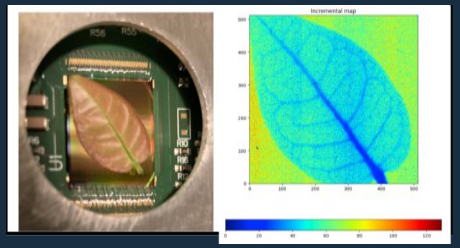




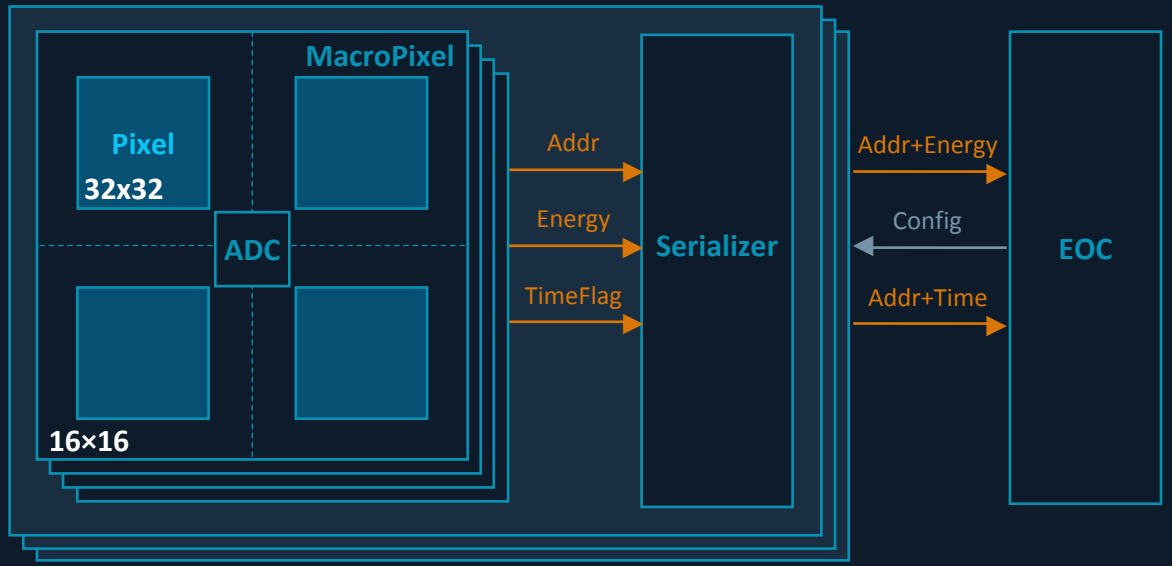
- Molybdenum $K_{\alpha 1}$ and $K_{\alpha 2}$ X-rays (17 keV)
- X-ray microfocus (up to 140 keV) for radiography and CT setups





System Architecture

Top-level block diagram



Grouping
- Macropixels composed of 2x2 pixels
  - Low Hit occupancy
  - Cluster size
- Resource sharing
  - Wilkinson ADC
  - Common Logic

EOC
- Sparse Readout
- Timestamping
  - Global coarse timestamp
  - Local fine-time
- Final data 24 bit words
  - Address
  - Fine Time
  - Energy Value

Pixel
250×250 µm²
CSA
PDH
Discriminator

→

MacroPixel
2×2 pixels
Shared ADC
FE Logic
*Serializer

→

Serializer
24-bit words
DDR - 12 CLK
16 ser./chip

→

EOC
Time reconstruction
Sparse readout
Configuration

Data flow →
← Configuration (token ring)

Macropixel Event Handling

Word Transmission

24-bit words in DDR, same line for charge and time

Async trigger storage

Event fires → pixel stores arrival word position (0-11) and word counter at arrival (0-5), pixel is immediately blocked

Round Robin scan

Two indipendent pointers scan all 4 pixel registers looking for valid events

- Priority TIme > Charge

Pixel release

After both time and charge are transmitted the pixel is unblocked and ready for the next hit

Pixel Register State

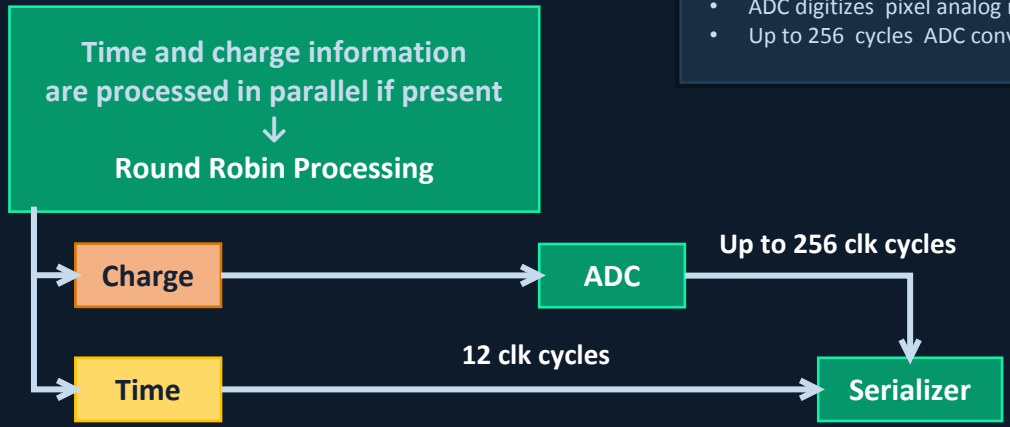
Pixel	Arr. word pos.	Word Ctr.	Time	Charge
00	bbbb	bbb	1	1
01	bbbb	bbb	1	1
10	bbbb	bbb	1	1
11	bbbb	bbb	1	1

Time Path

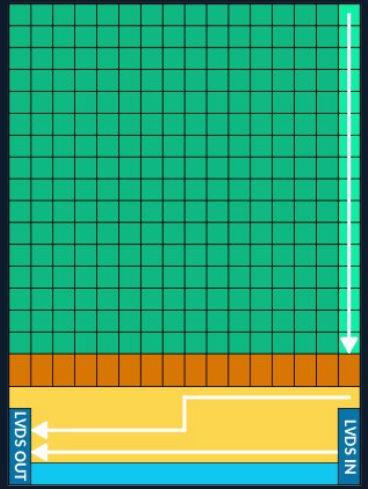
- 12 clk cycles per word
- Transmit counter (0-11) encodes sub-word phase
- Word counter (0-5) encodes inter word delay

Charge Path

- ADC digitizes pixel analog memory
- Up to 256 cycles ADC conversion



Timing Reconstruction in EOC



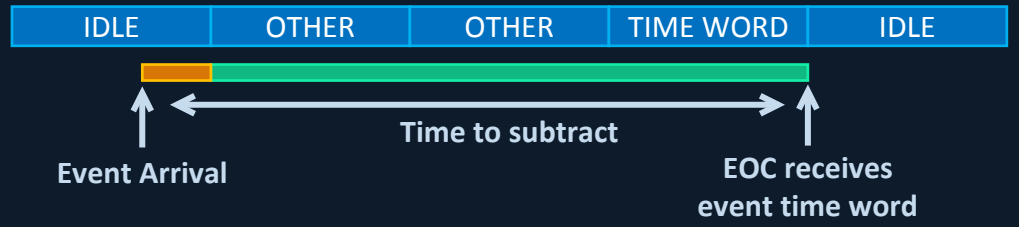
MacroPixel
Base Column - Deserializer
EOC
PAD: power, test, config ...
Differential Transmission
Data Flow

EOC timing reconstruction

$$T\_event = T\_global - (N\_words\_waited + 1) \times T\_word - (12 - transmit\_counter)$$

Word arrives with fixed delay (calibration routine at startup) on a dedicated wire (Macropixel to EOC)

1. Global timestamp is latched at EOC on time word arrival
2. Transmit count track position within the current word
3. Word counter counts how many words elapsed since event

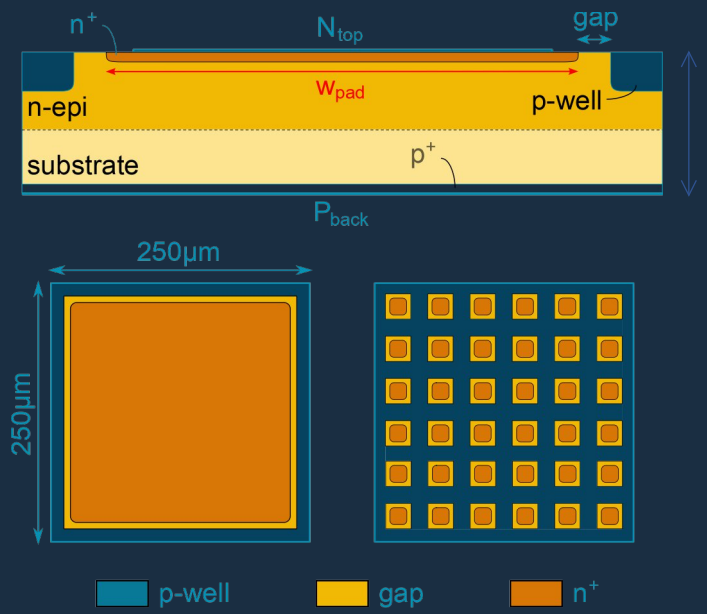


Sensor Design

Fully depleted n-on-n sensor structure

Synopsys TCAD Sentaurus simulations — 110 nm LFoundry process

Cross-section schematic



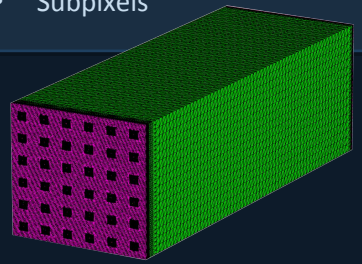
Design choices

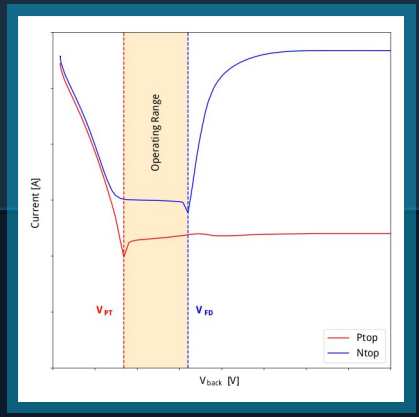
Pitch → 250 µm → 6.25 µW/channel
- Limit the number of channels for power constraints
- No sacrifice on reconstruction capabilities

Thickness → 715 µm
- Electrical Characterization
- On going tests on new substrates

Capacitance → < 250 fF
- gap optimization
- p-well/n⁺ ratio

Pixel Layout
- Single pad
- Subpixels





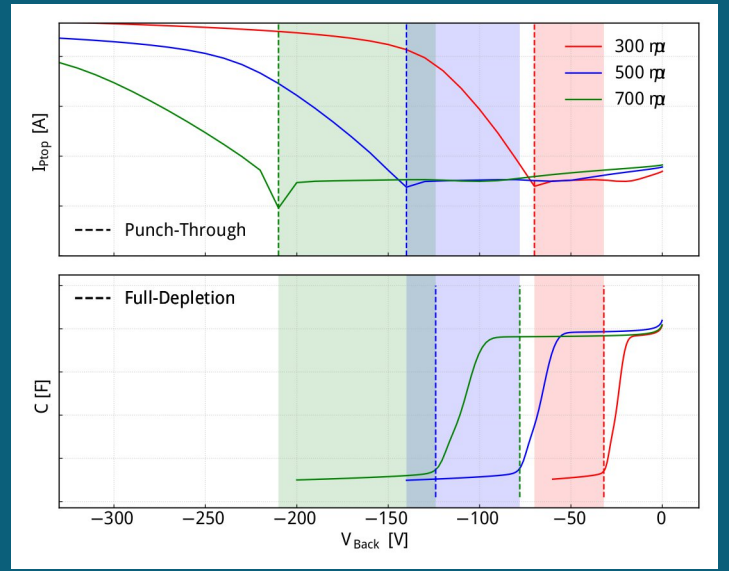
Sensor Layout Optimization

Key figure of merit: lateral n⁺/p-well junction capacitance

Electrical Characterization

PT shifts with thickness but remains accessible across 300-700 µm.
C(V) identified FD as capacitance plateau; well-defined working range also for 700 µm.

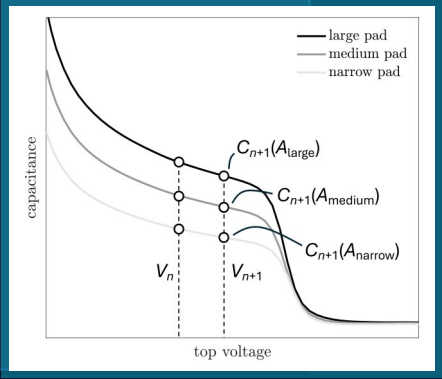
Thickness [µm]	$V_{Full\ Depletion}$ [V]	$V_{Punch\text{-}Through}$ [V]
300	30	70
500	80	140
700	125	210

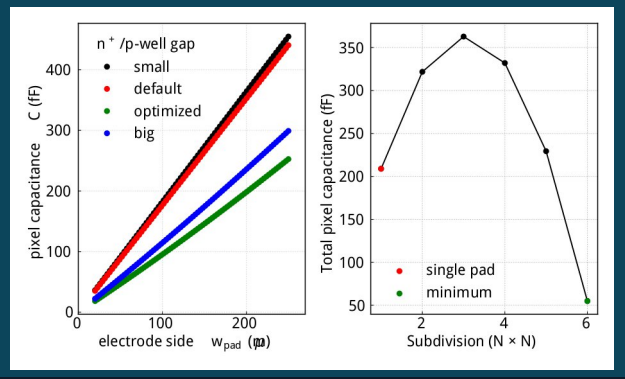


Predictive Capacitance Modeling

Developed geometry-based models to accelerate layout optimization

- Main capacitance contribution is the lateral one for the
- n⁺/p-well junction
- Gap optimization leads to half of the capacitance wrt default value
- Segmented pixels increase perimeter capacitance until 6×6 sub-pixel layouts improve scaling — but routing complexity and parasitic capacitance grows





Sensor MC Testing

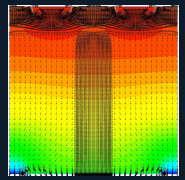
TCAD

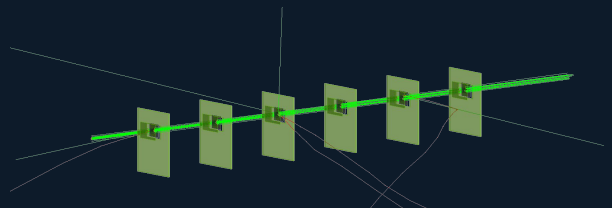
Device layout and simulation → export following maps

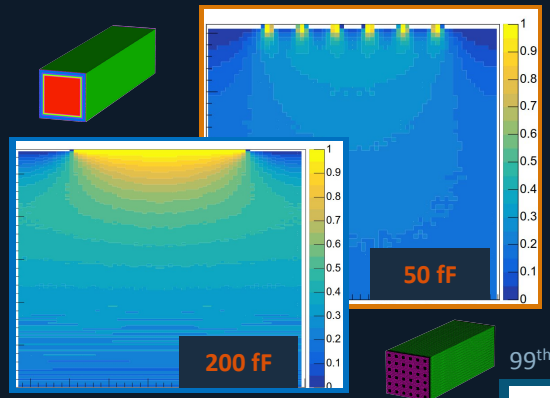
- Doping Concentration
- Electrostatic Potential → Weigthing Potential
- Electric Field

Monte Carlo Framework

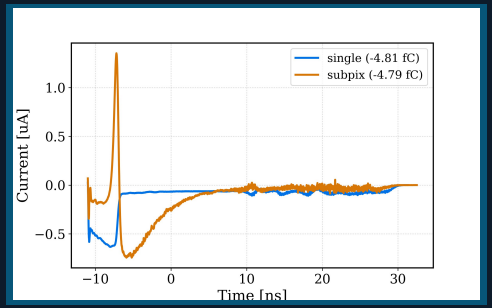
- Particle transport and interactions simulations
- Energy deposition and ionization modeling
- Charge carrier drift and signal induciton computations





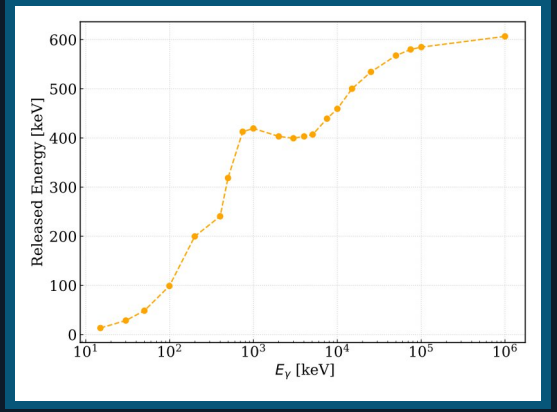


Allpix signals for 30 ke⁻ released at 100 µm Depth at the center of one pixel



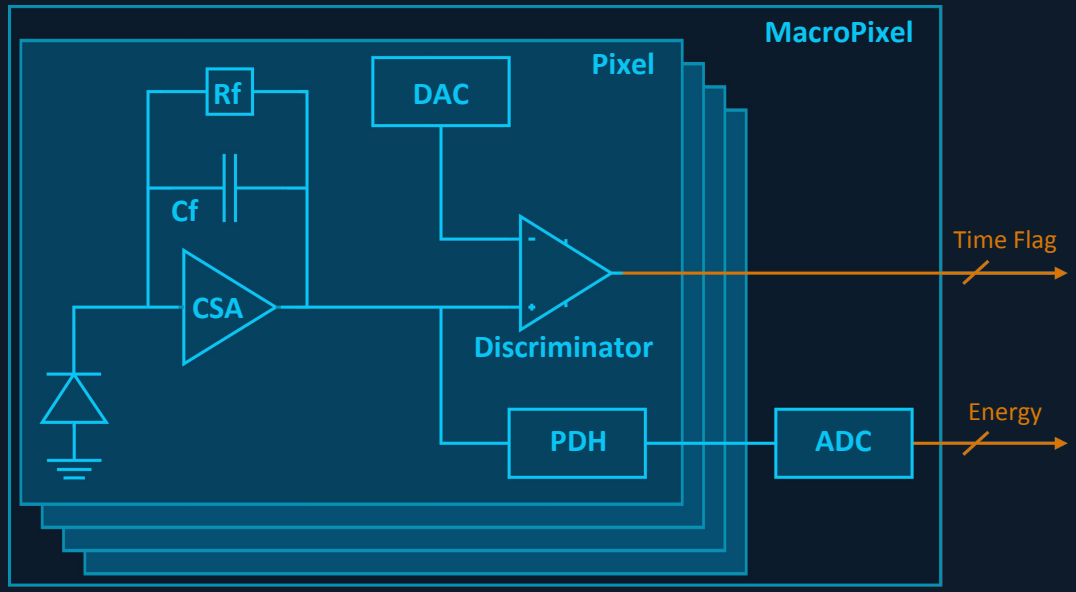
E_γ [keV]	99th percentile [keV]
1e1	10 → 3k e⁻
1e3	400 → 110k e⁻
1e4	450 → 125k e⁻
1e5	570 → 160k e-

99th percentile of Energy released in one pixel



Front-End Implementation

Pixel Architecture Overview



Sensor Capacitance
- Single pad layout → 200 fF

Dynamic Range
- 3k - 160k electrons in sensor
- Focus on 3k - 100k electrons

Temperature Range

Space grading → [-35,50] °C

PreAmplifier
- CSA
- TP injection

Energy Branch
- Peak Detector and Hold circuit
- Shared Wilkinson ADC

Time Branch
- Timing Discriminator

Pixel
250×250 µm²
CSA
PDH
Discriminator

→

MacroPixel
2×2 pixels
Shared ADC
FE Logic
*Serializer

→

Serializer
24-bit words
DDR - 12 CLK
32 ser./chip

→

EOC
Time reconstruction
Sparse readout
Configuration

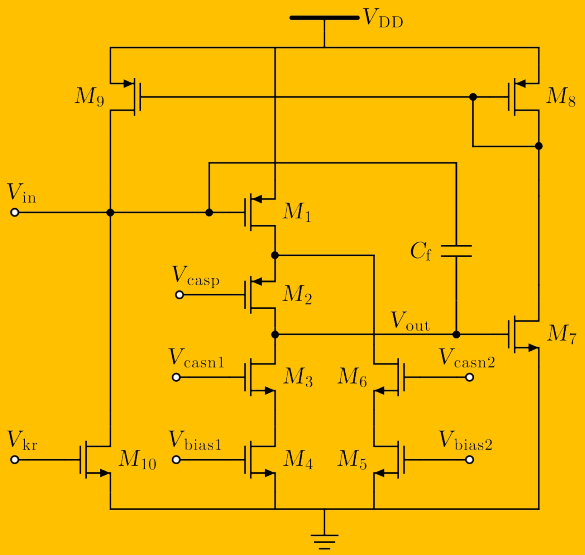
Data flow →
← Configuration (token ring)

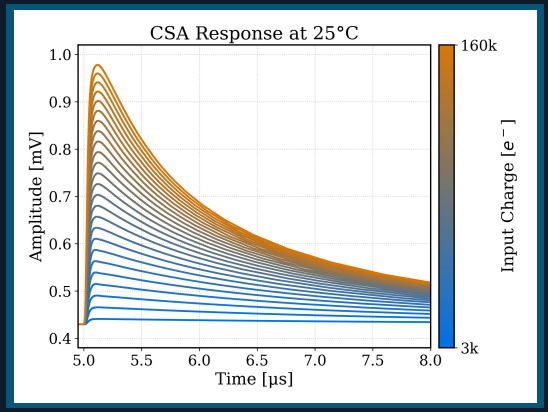
Charge Sensitive Amplifier

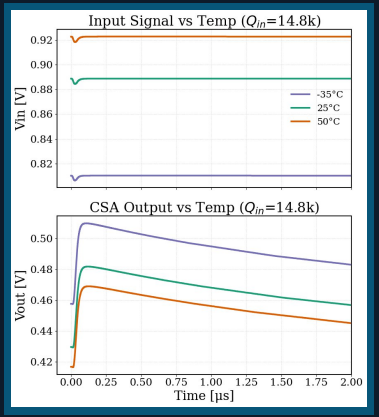
1.2 µW

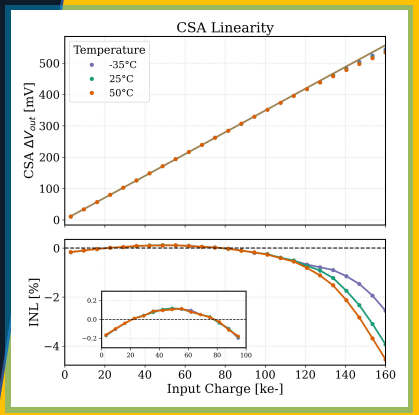
CSA Features

- Telescopic cascode with split bias current branch and PMOS input transistor
  - $C_{Detector}$ = 200 fF
  - $C_{Feedback}$= 45 fF → expected gain 22 mV/fC
  - [3, 160] kelectrons input → [10, 570] mV output swing
- Sensor cathode needs at least 0.7 V bias
  - Active feedback network to give enough room for the output
    - τ_{RC} = 3.5 µs
    - Peaking Time = 150 ns









CSA Simulations

DC Levels:

- V_{in} > 0.8 V
- V_{out} ~ 450 mV
- V_{out} ~ 40 mV change
- Need for baseline holder

Linearity:

- 21.8 mV/fC measured gain
- INL ± 0.2% @ [3-100] ke^-

Peak Detector and Hold

1.8 µW

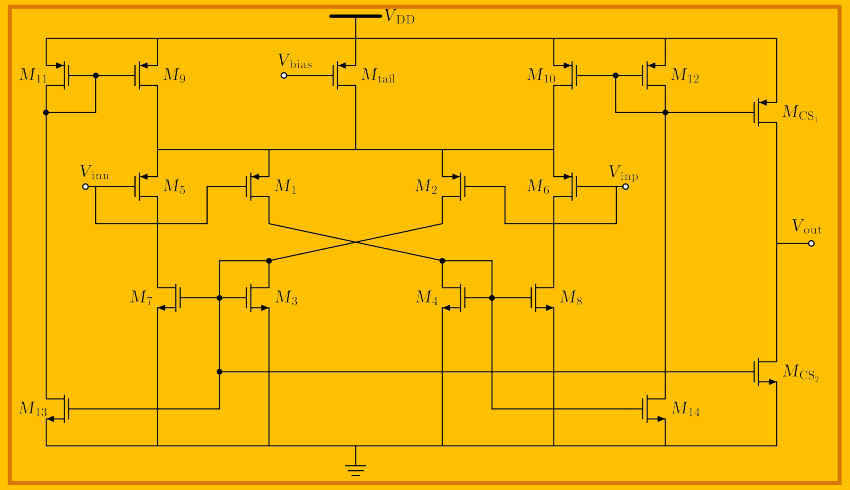
PDH Features

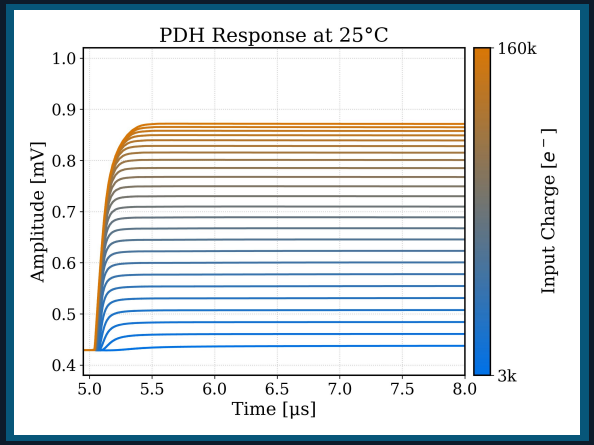
Class AB OTA

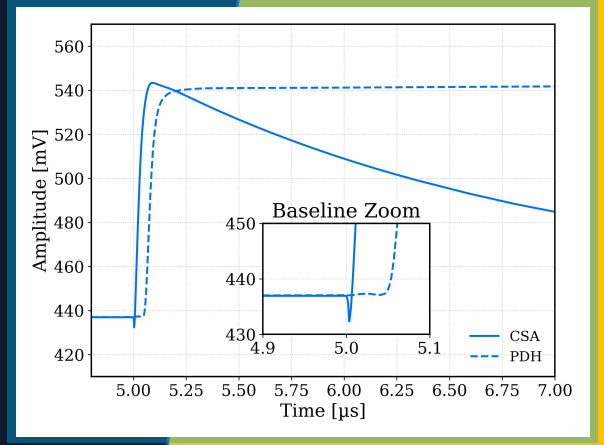
- Adaptive Biasing via Positive Feedback
  - Boost current during pulse edges
- Enhanced Slew-Rate/Power Ratio
- Weak-Inversion Quiescent Operation

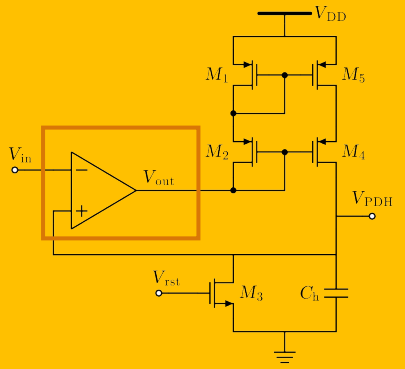
Cascoded rectifing current mirror

- Prevent voltage drop and leakage
- Limit baseline pedestal









[1] Ah-Reum Kim et al. "Low-power class-AB CMOS OTA with high slew-rate," *2009 International SoC Design Conference (ISOCC)*, Busan, 2009, pp. 313-316, doi: 10.1109/SOCDC.2009.5423790

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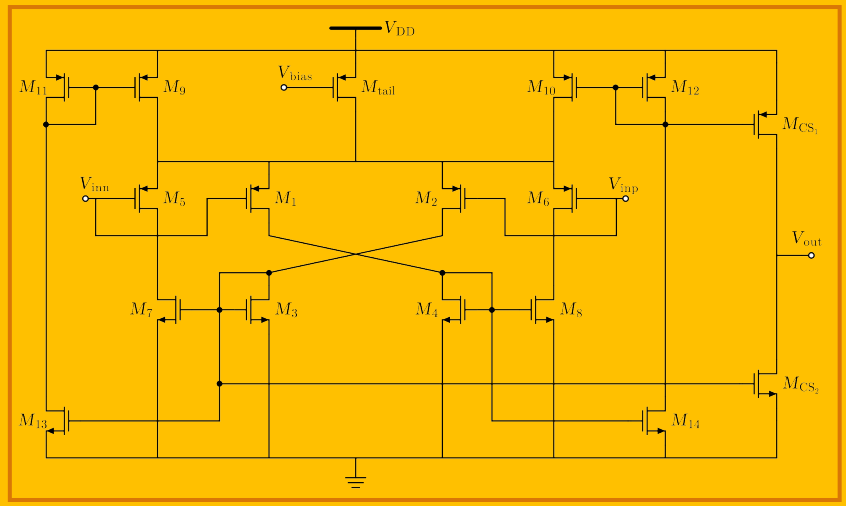
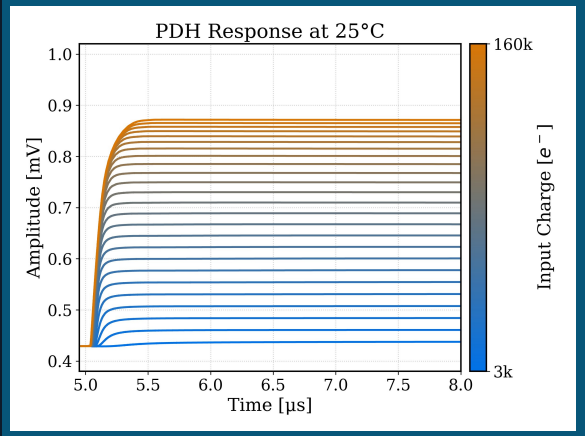
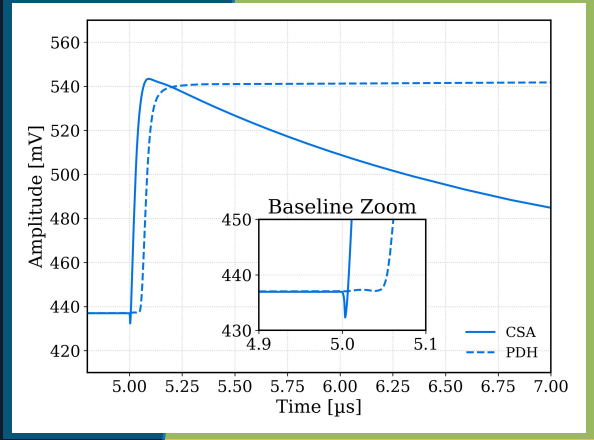






PDH Simulations

I_{tail} = 40 nA

C_h = 300 fF

- Pedestal < 2 mV
- Settling time ~ 0.5 µs

Linearity

- PDH/CSA ± 3% @ [3, 100] ke⁻
- Strong dependence on temperature for more energetic events

[1] Ah-Reum Kim et al. "Low-power class-AB CMOS OTA with high slew-rate," *2009 International SoC Design Conference (ISOCC)*, Busan, 2009, pp. 313-316, doi: 10.1109/SOCDC.2009.5423790

Peak Detector and Hold

1.8 µW

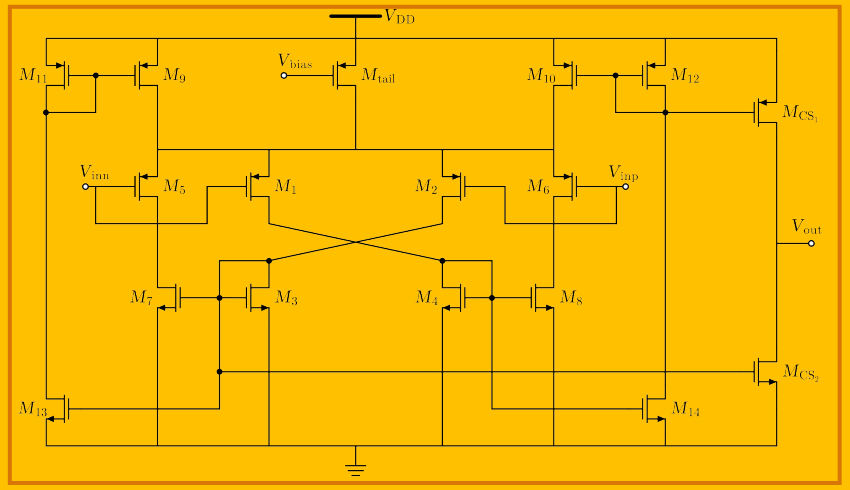
PDH Features

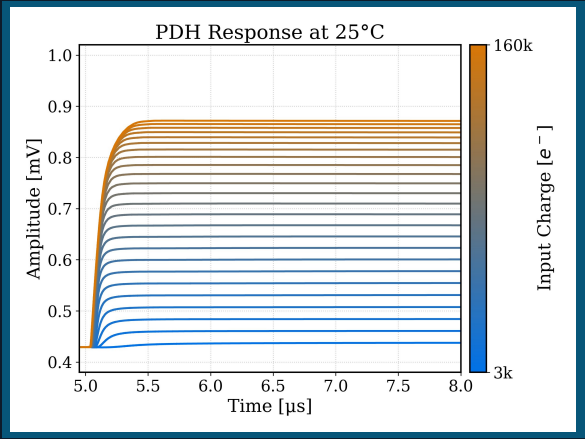
Class AB OTA

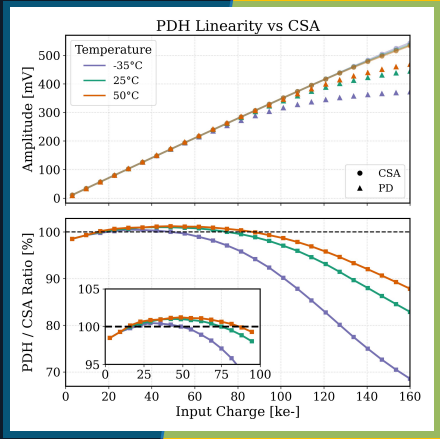
- Adaptive Biasing via Positive Feedback
  - Boost current during pulse edges
- Enhanced Slew-Rate/Power Ratio
- Weak-Inversion Quiescent Operation

Cascoded rectifing current mirror

- Prevent voltage drop and leakage
- Limit baseline pedestal







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Timing Discriminator

DiscriminatorFeatures

Dual stage cascoded leading-edge discriminator

- Cells connected with active biasing network
- Minimal quiescent current

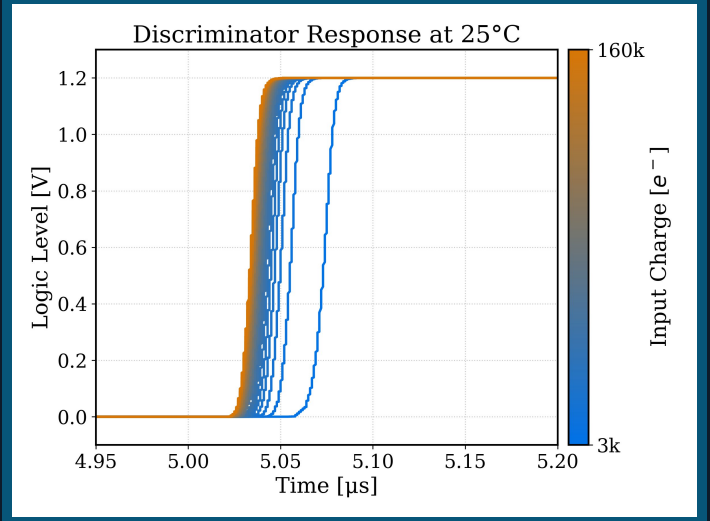
Boost tail current of the second stage

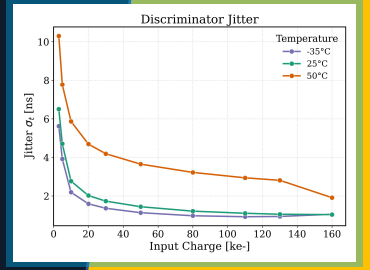
- Fast recovery limiting voltage swing

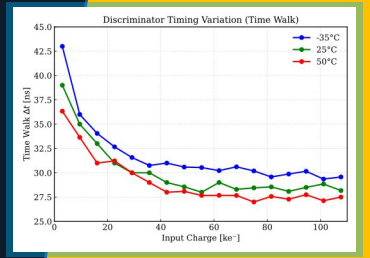
1.5 µW

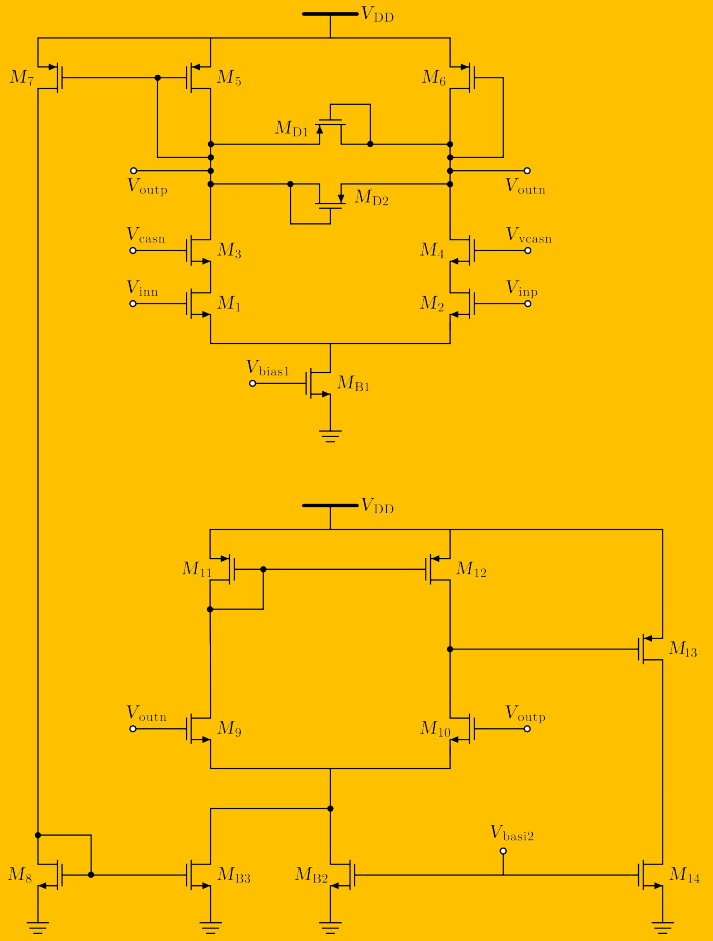
Discriminator Simulations

- Jitter < 10 ns
- Timewalk < 45 ns





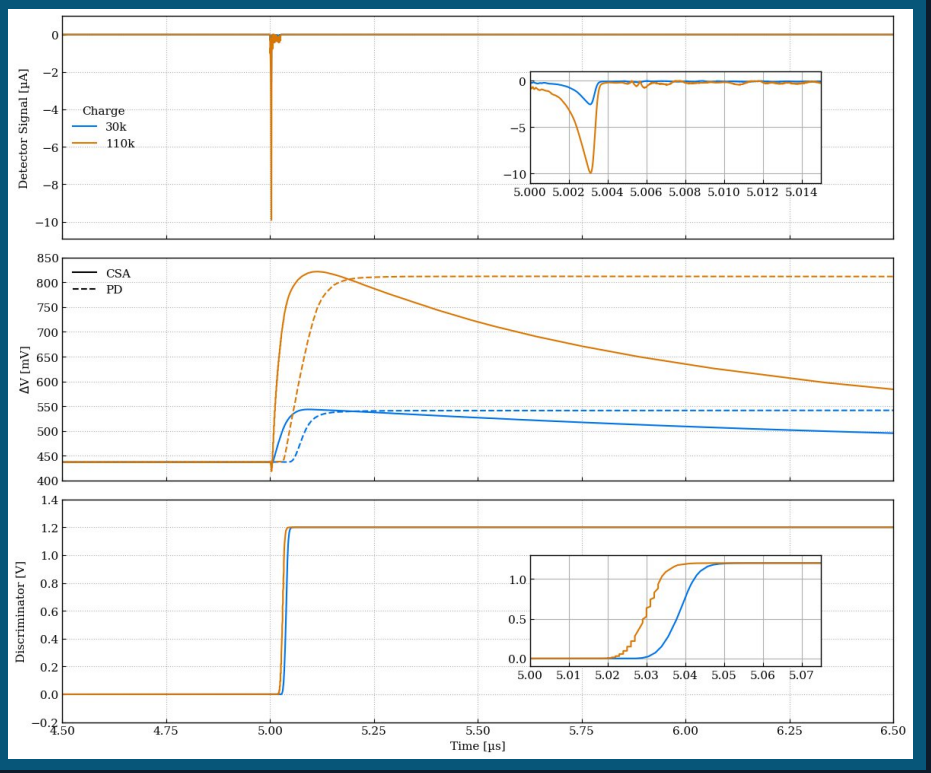




[2] Menouni, Mohsine. "Low Power Discriminator for ATLAS Pixel Chip," 2009. doi:10.5170/CERN-2009-006.606.

Front-end simulated results

Front end response to Allpix² signals



Power Consumption:
- 10 mW/cm²
- 250 µm pitch
  → 6.25 µW/channel

Timing Resolution:
- 200 ns r.m.s.

Temperature Range
- Space Application
  → [-35, 50]°C

Dynamic Range
- Main focus on 3k - 100k electrons

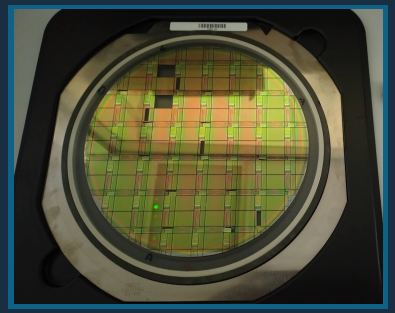
Technology	LFoundry 110 nm CIS
Power Supply	1.2 V
$N_{Channels}$	32 x 32 Pixels / 16 x 16 MP
Input Polarity	Negative
C_{Sensor}	200 fF
ENC	< 200 e^-
SNR @ 3 ke^-	17
FE Power Consumption	4.5 µW/channel

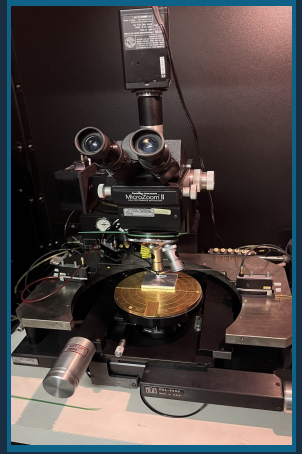
Substrates Characterisation

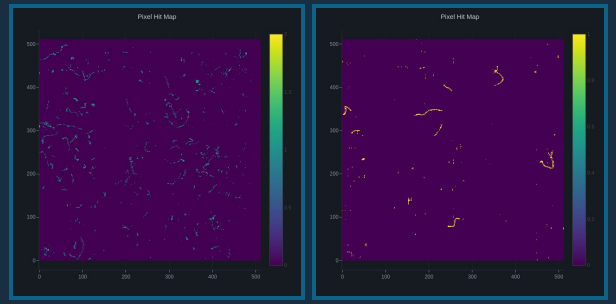
First test results

Substrate Characterisation

- ✓ IV Characterisation at the MicroProbing station (passive structures)
  - 500 µm – thick substrates
  - 700 µm – thick substrates
- ✓ Testing of ARCADIA MD3 on thicker substrates

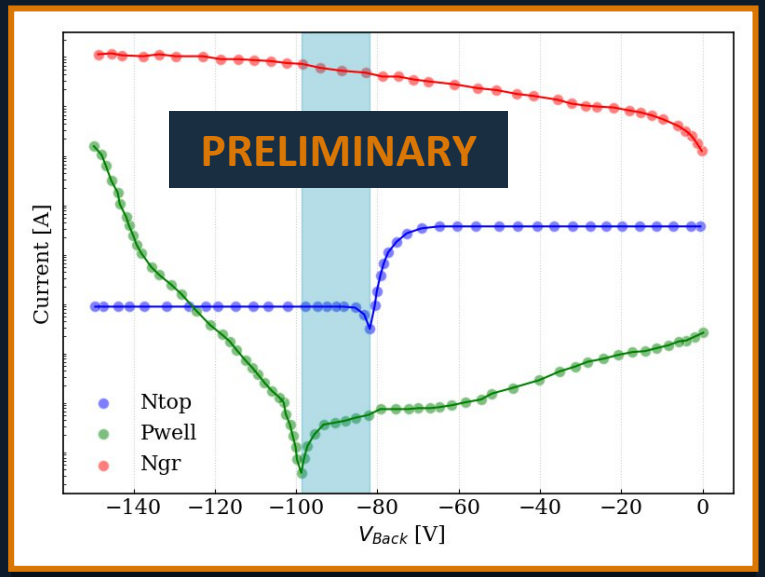


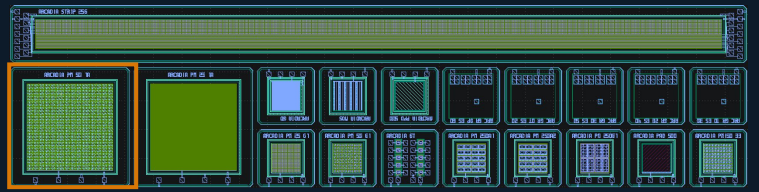




500 µm 700 µm

- Uranium cup used as source
- Hitmaps: number of hits showed relatively to the 512x512 pixels MD3 matrix





Status and Outlook

A Low-Power FD-MAPS for Space Compton Imaging

Sensor

700 µm n-on-n TCAD pixel optimised at 250 µm pitch

- single-pad layout selected for field uniformity
- 200 fF capacitance achieved
- full depletion at ~80 V on real 700 µm substrates

Digital

MacroPixel async event storage

- time-priority round-robin arbitration
- EOC sub-word timestamp reconstruction validated in simulation
- 24-bit DDR serialisation implemented

Front-End

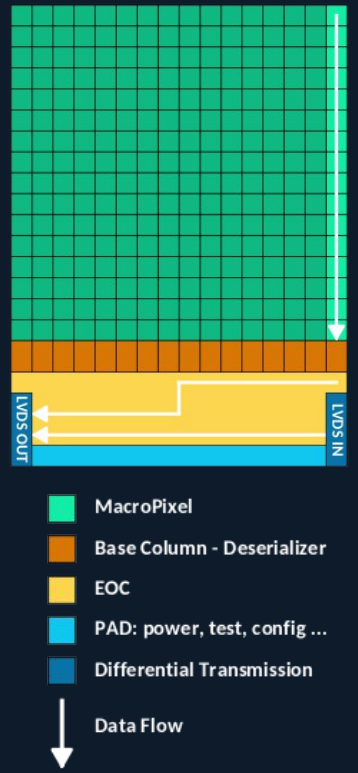
-35 to 50 °C

- CSA
  - 150 ns peaking
  - Output swing 10 - 600 mV
  - ±0.2% INL
- PDH
  - 0.5 us settling time
  - 2 mV pedestal
- Time Discriminator
  - timewalk < 45 ns
  - Jitter < 10 ns

4.5 µW

Ongoing work

- Wilkinson ADC design: ramp linearity and power optimisation in progress
- Full analog–digital integration: floor-planning and mixed-signal verification upcoming
- Complete thick substrate qualification on 700 µm samples under way
- Module integration with multiple HIC options under study (PCB, FPC, FLEX)



Thank you for your time!

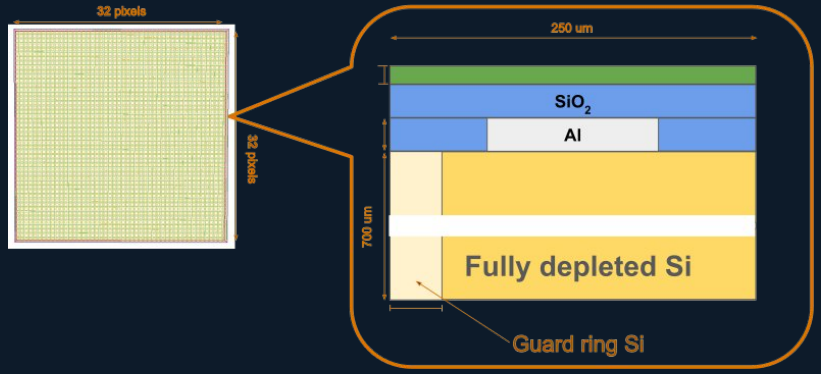
Design, Simulation and Test Group

M. Barbagiovanni, L. Baldini, M. Da Rocha Rolo, A. Di Salvo,
E. Posteraro, A. Frassà, L. Latronico, M. Mandurrino,
U. Savino, C. Sgrò, E. Trossarello

INFN ARCADIA Politecnico di Torino 1859 ASI AGENZIA SPAZIALE ITALIANA SPACE IT UP!

Backup Slides

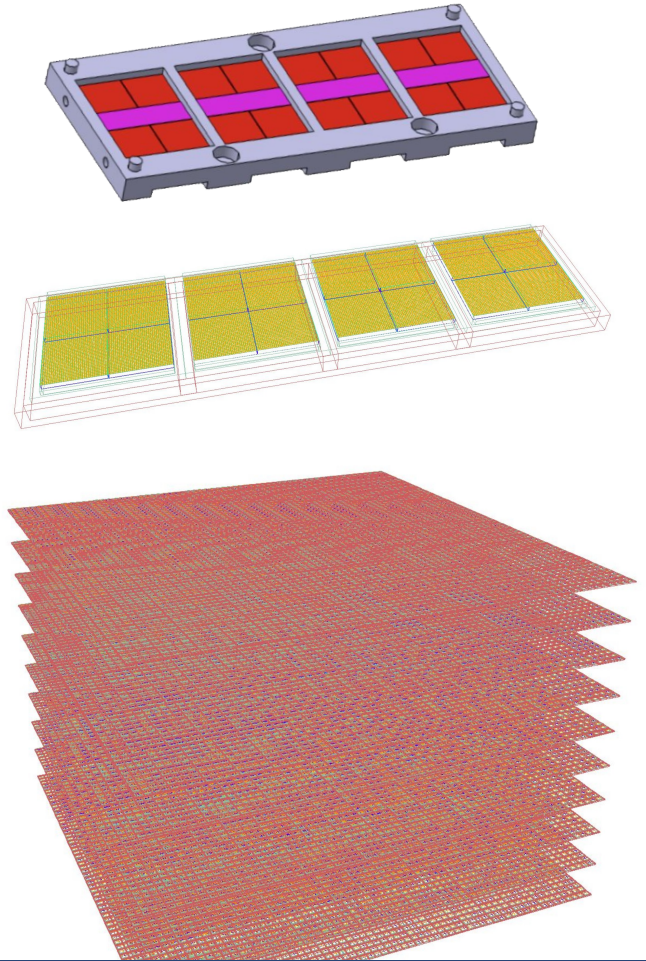
GEANT Simulations



Tracker simulation details

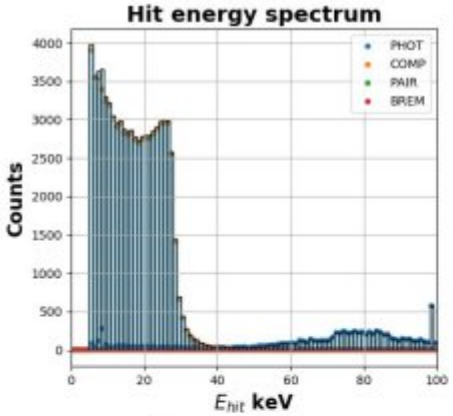
- Detector
  - simulated with worst case single block of all metallization on top of sensor
  - 32x32 pixels
  - EOC
- Hybrid Integrated Circuit
- Multiplane tracker
  - 1 m^2 chip planes
- Monocromatic source
  - 100 keV - 1 GeV

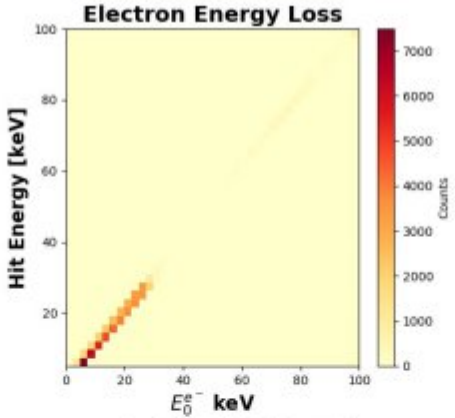
Courtesy of A. Frassà

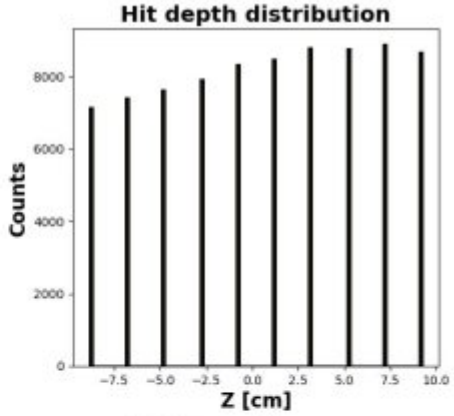


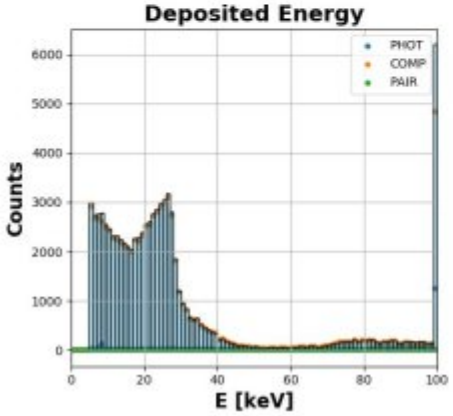
Courtesy of A. Frassà

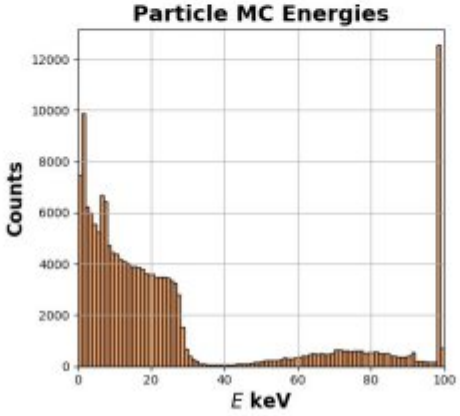
GEANT - E_γ = 100 keV, E_{thr} = 5 keV

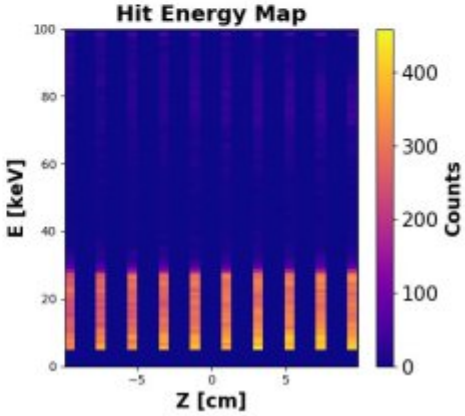












Courtesy of A. Frassà

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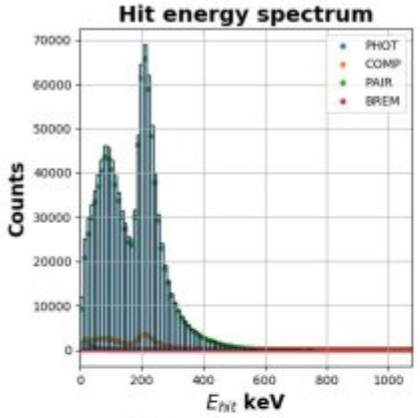
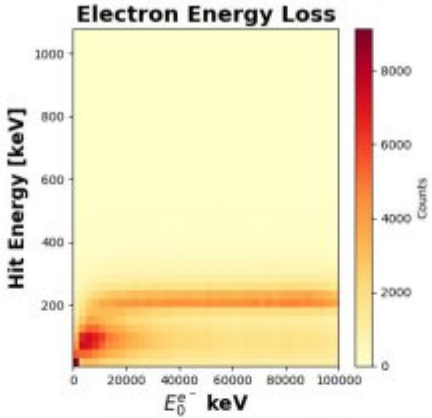
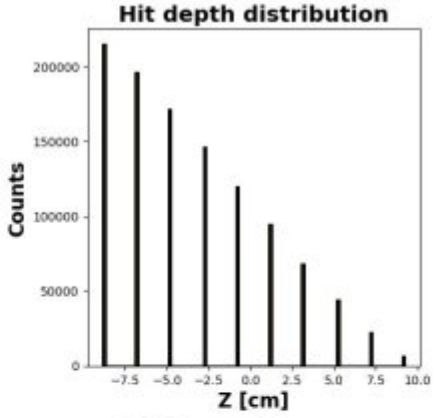
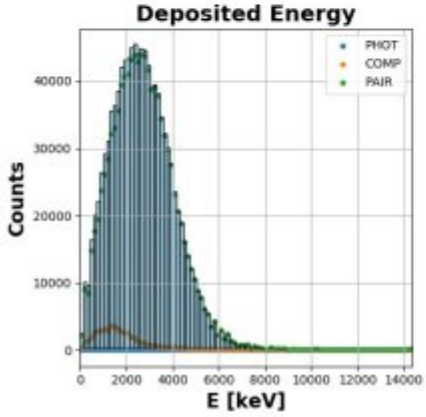
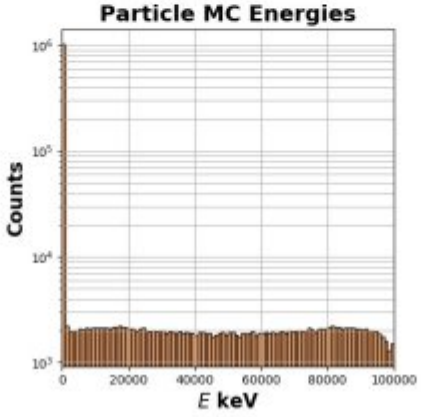
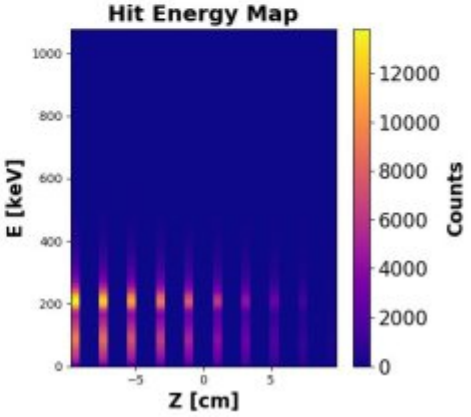










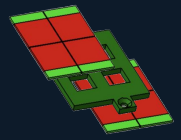


Module assembly options

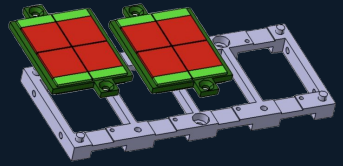
PRELIMINARY
Courtesy of U. Savino

PCB
Printed circuit board

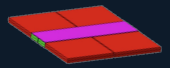
2x2 chips layout

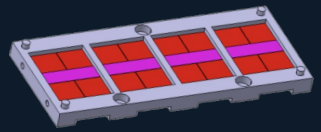


Hybrid Integrated Circuit



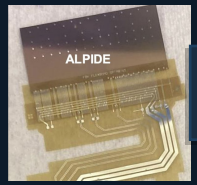
HICs on Al Frame





FPC
Al flexible printed circuit

Flex embed
Al Chip embedded in flex printed circuit



FBK flex demonstator
spTab bonded to ALPIDE chip

Thermal Performances
Steady-state thermal simulation

- 32 chips (16 per side)
  - Dissipated power/chip 13mW
- ideal thermal contact and a wall temperature fixed at 15°C

Maximum global variations:

- PCB → 4.5°C
- FPC → 2.5°C

Higher thermal drain for FPC