MightyPix: A HV-CMOS Pixel Chip for LHCb's Mighty Tracker

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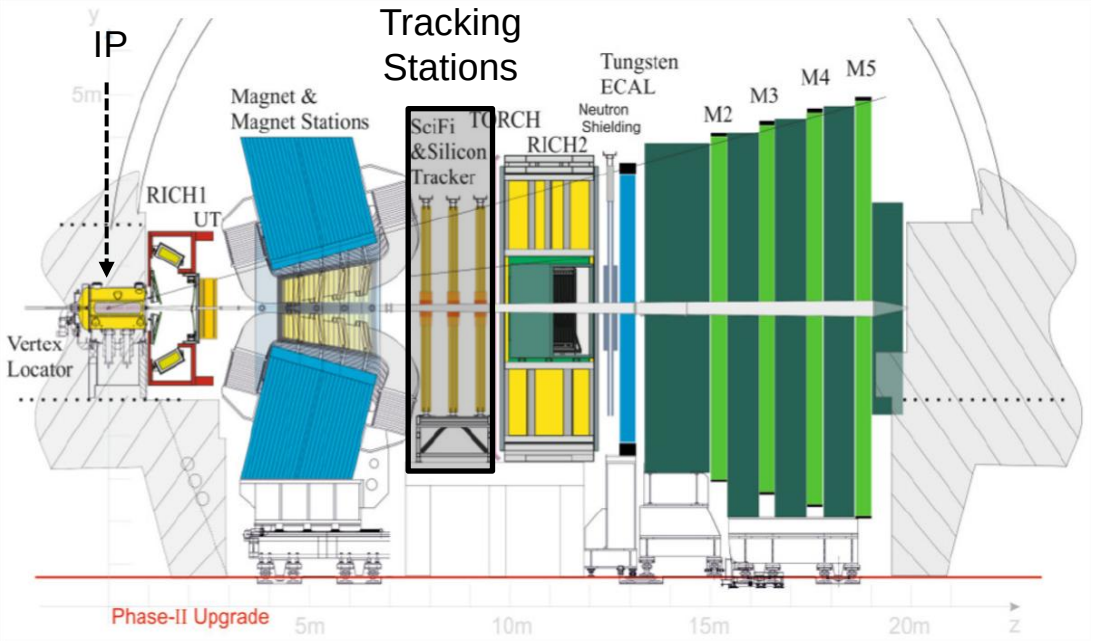
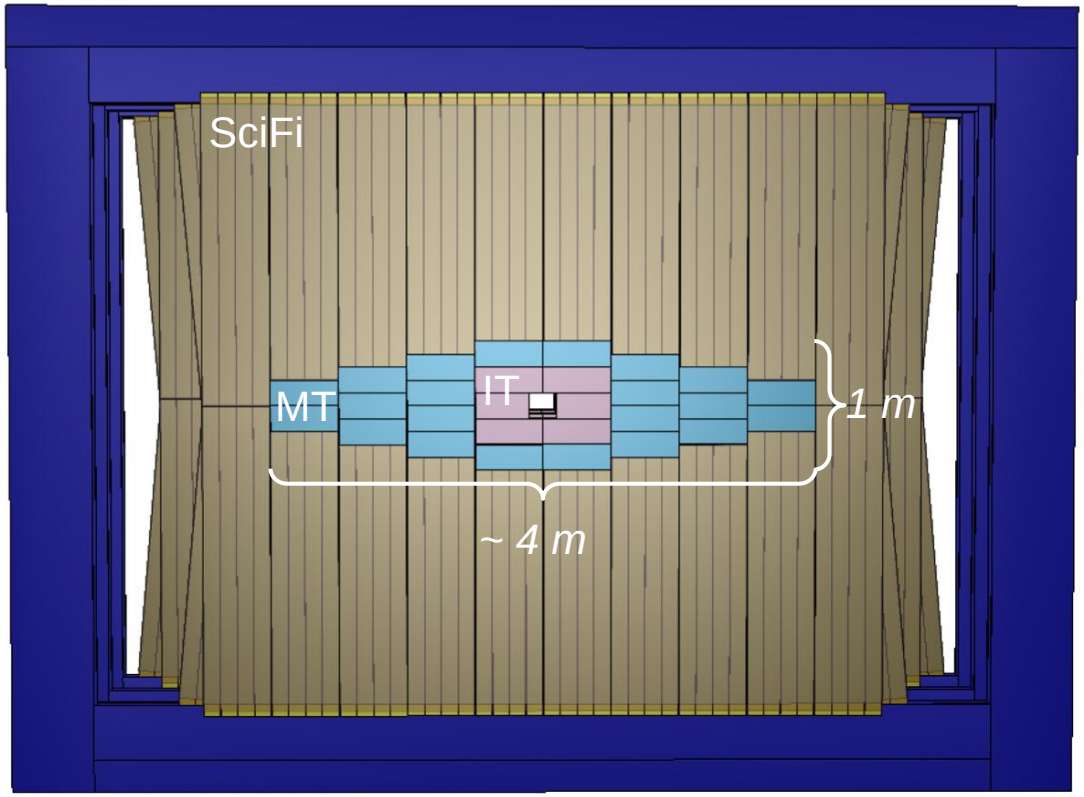
Ivan Peric*

- **LHCb Experiment**
- Forward-arm spectrometer at the LHC
- Precision flavour physics:
  - CP violation
  - beauty and charm decays
  - hadron spectroscopy
  - rare decays
- ~9 fb^{-1} recorded in Run 1 and Run 2



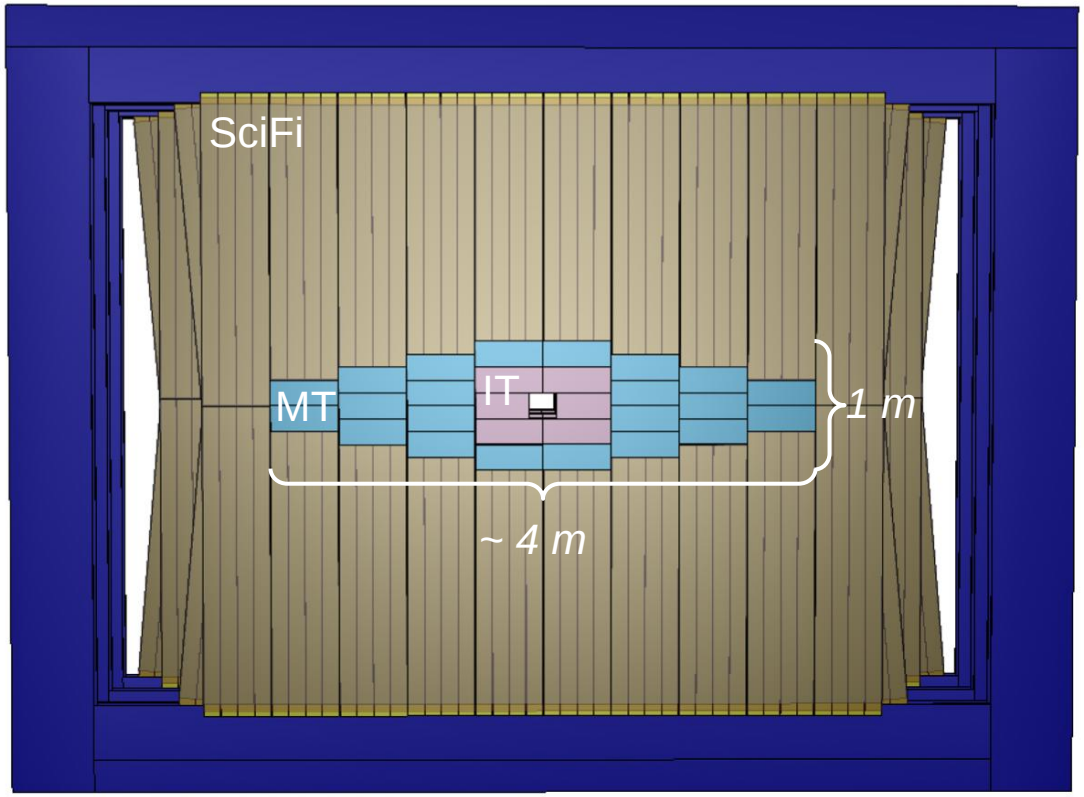
Schematic side view of the Upgrade II LHCb detector. [1]

- **LHCb Upgrade II**
- Higher luminosity operation
- Increased:
  - radiation dose
  - particle multiplicities
  - hit rates
- Upgrade of downstream tracker:
  - **Mighty Tracker**



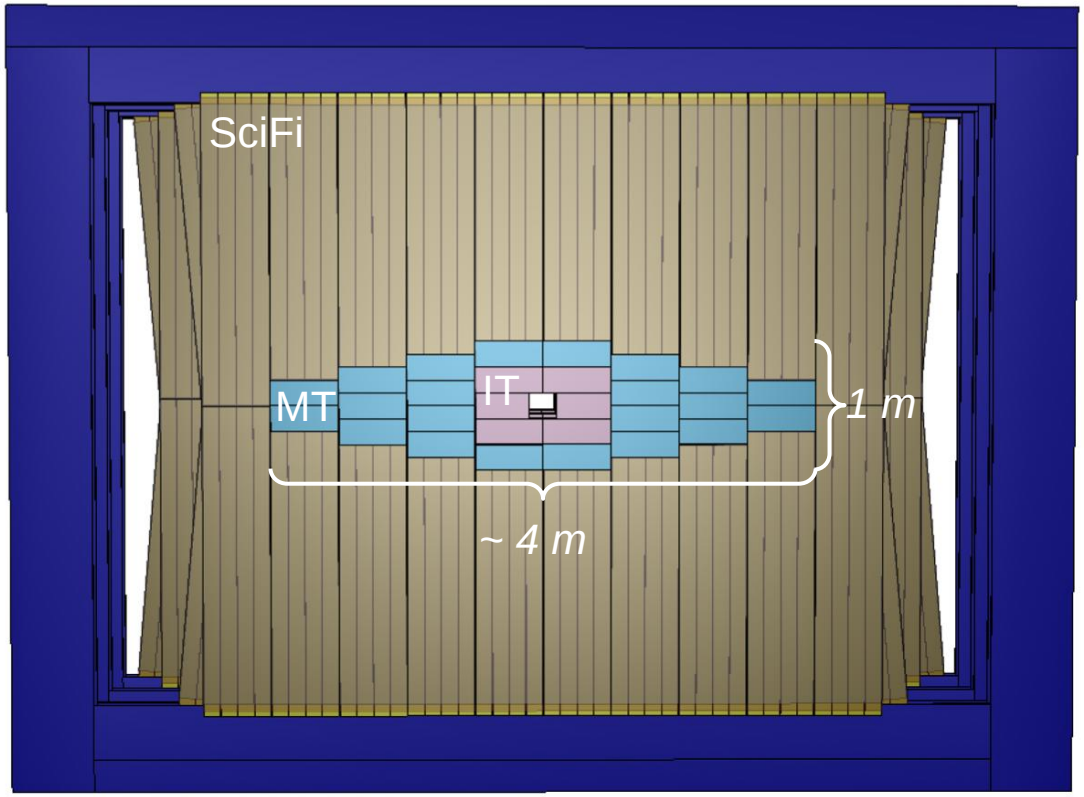
Schematic of one layer of the Mighty Tracker. [1]

- **Mighty Tracker**
- Hybrid tracking detector:
  - SciFi Tracker
  - Inner Tracker
  - Middle Tracker
- Technology:
  - Scintillating fibres + HV-MAPS
- Advantages:
  - High granularity
  - Fast timing
  - Radiation hardness



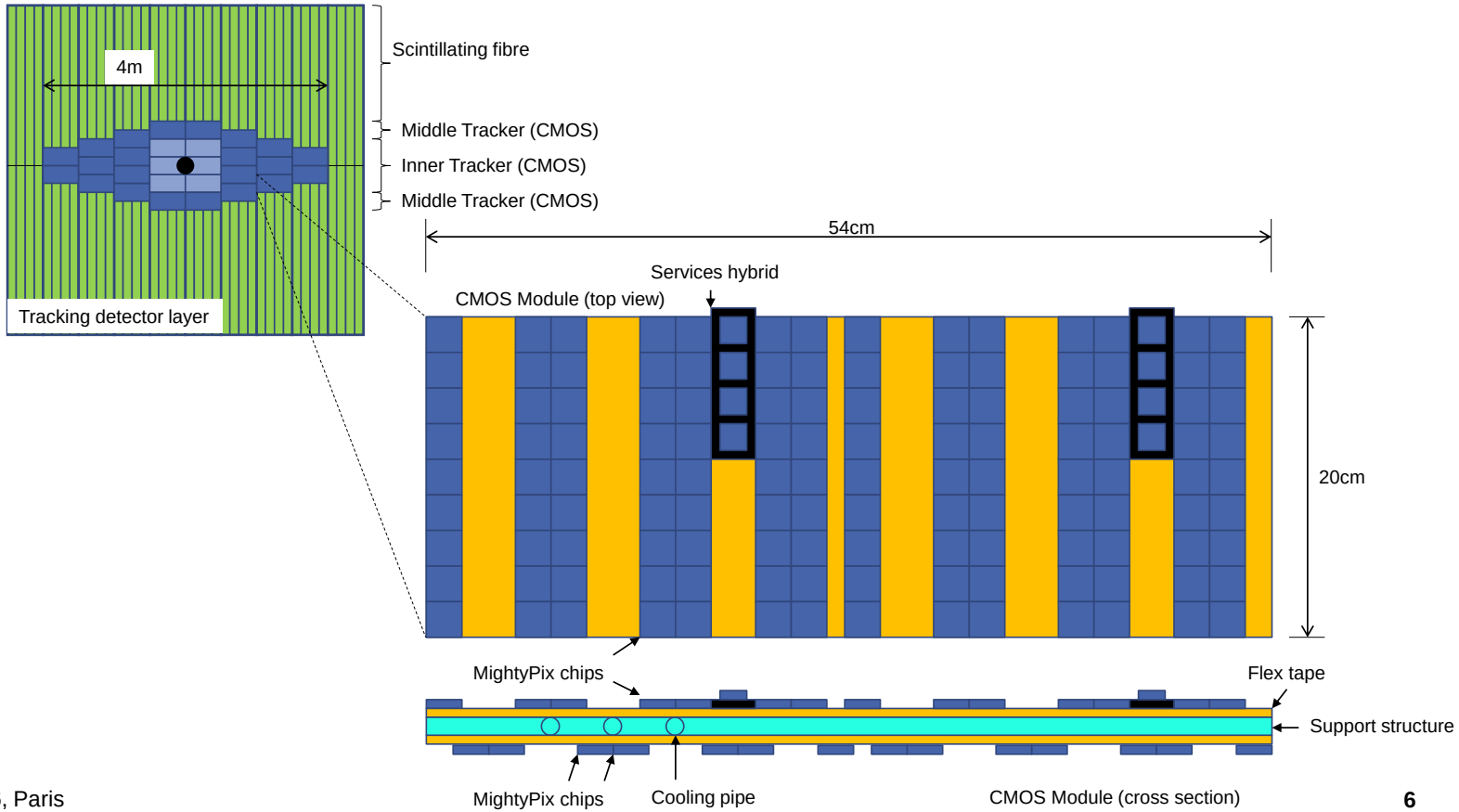
Schematic of one layer of the Mighty Tracker. [1]

- **MightyPix Detector Scale**
- Baseline technology:
  - HV-CMOS pixel chip **MightyPix**
- 46,000 silicon sensors
- Total silicon area:
  - ~18 m²



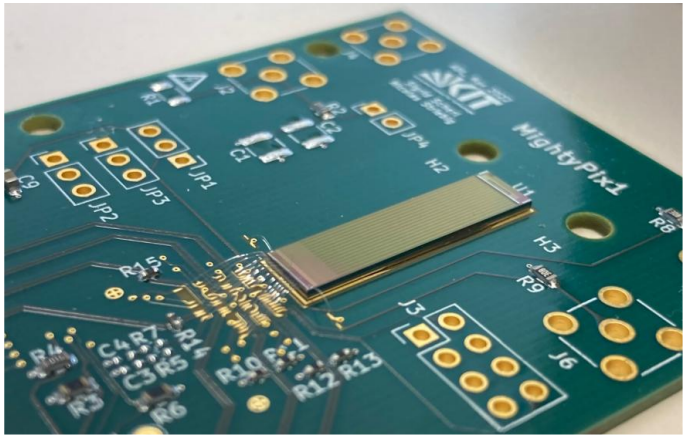
Schematic of one layer of the Mighty Tracker. [1]

- Module structure:
- 28 modules/layer, 6 layers
- Module size: 20 cm × 54 cm
- **Mighty Tracker Module**
- HV-MAPS mounted on both sides
- Cooling pipes integrated into support structure
- Continuous active coverage

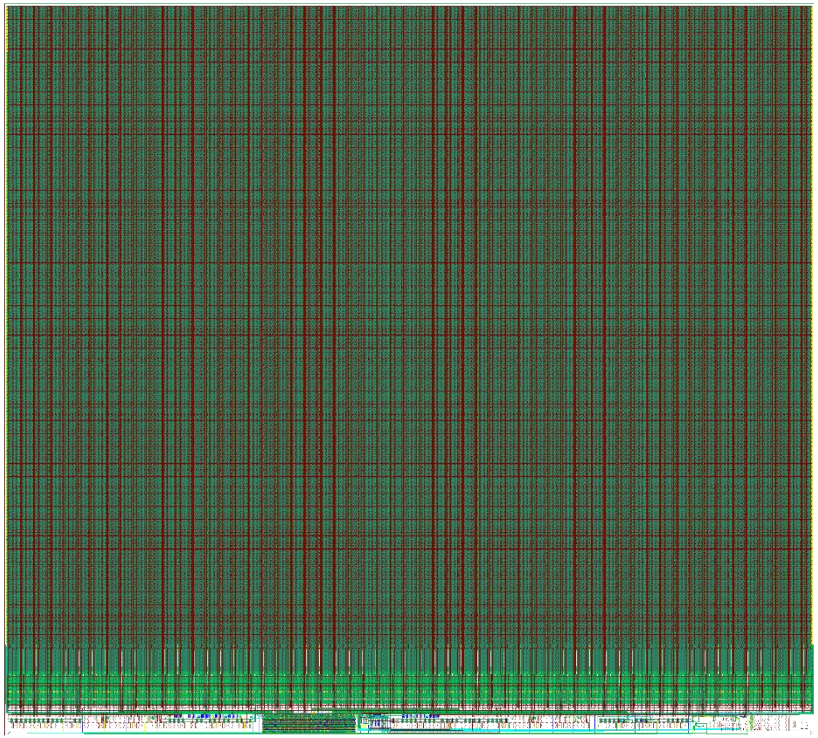


- **MightyPix Requirements**
- Pixel size:
  - < 100 µm × 300 µm
- Hit-rate capability:
  - 30 MHz/cm²
- In-time efficiency:
  - 99% in 25 ns
- Radiation hardness:
  - 6×10^{14} neq/cm²
- Power:
  - < 150 mW/cm²
- 4 × 1.28 Gbps data links

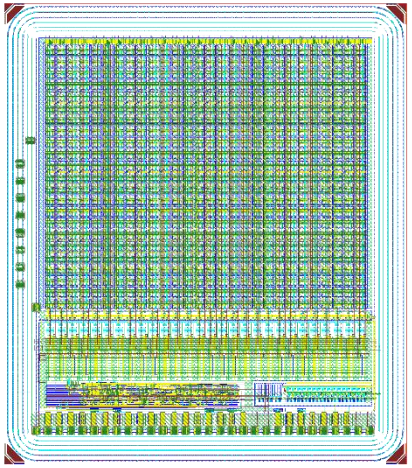
- **MightyPix Development**
- MightyPix1
  - first prototype
- MightyPix2
  - near-full functionality
- MightyPix3
  - final prototype
- Parallel development:
- LF-MightyPix
  - 150 nm CMOS backup technology



MightyPix1

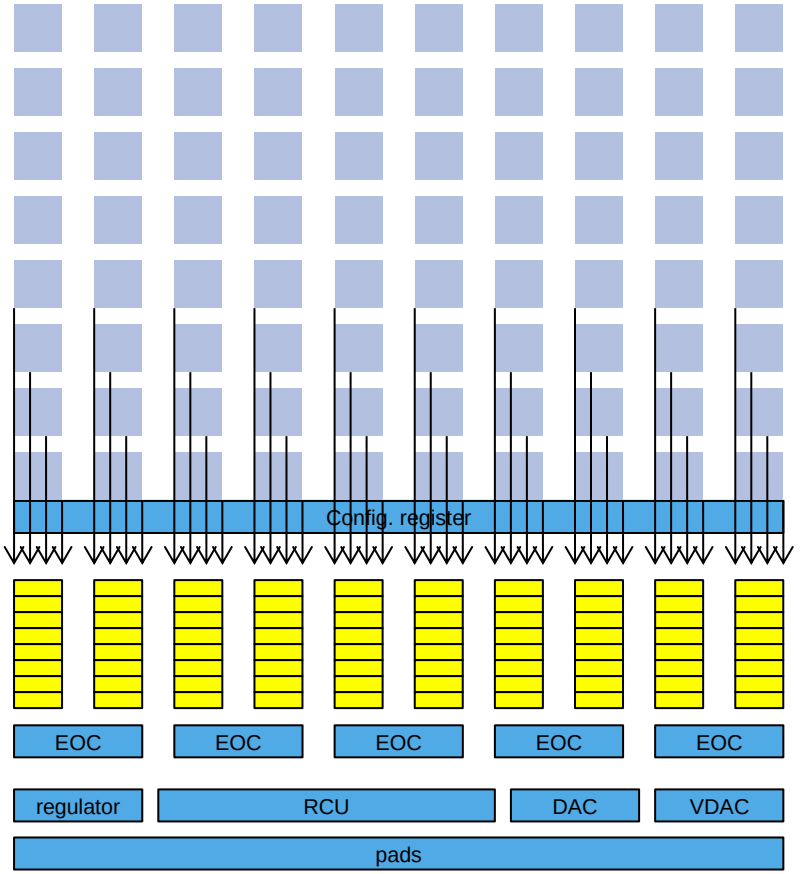


MightyPix2



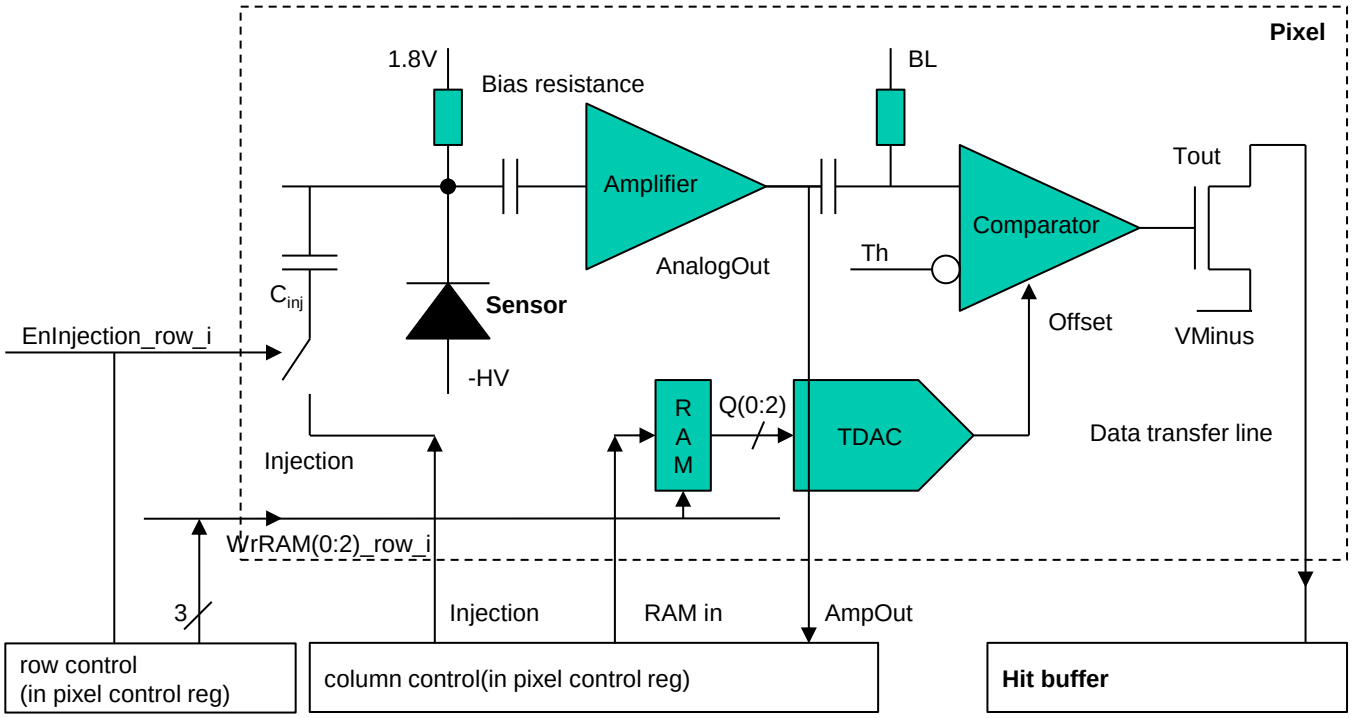
LFMightyPix

- **MightyPix Chip Architecture**
- 122 double columns
- 2 × 194 pixels per double column
- Chip periphery includes:
- Hit buffers
- End-of-Column (EoC) circuits
- Readout Control Unit (RCU)
- DACs
- I/O pads



Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer



Source: Ivan Perić

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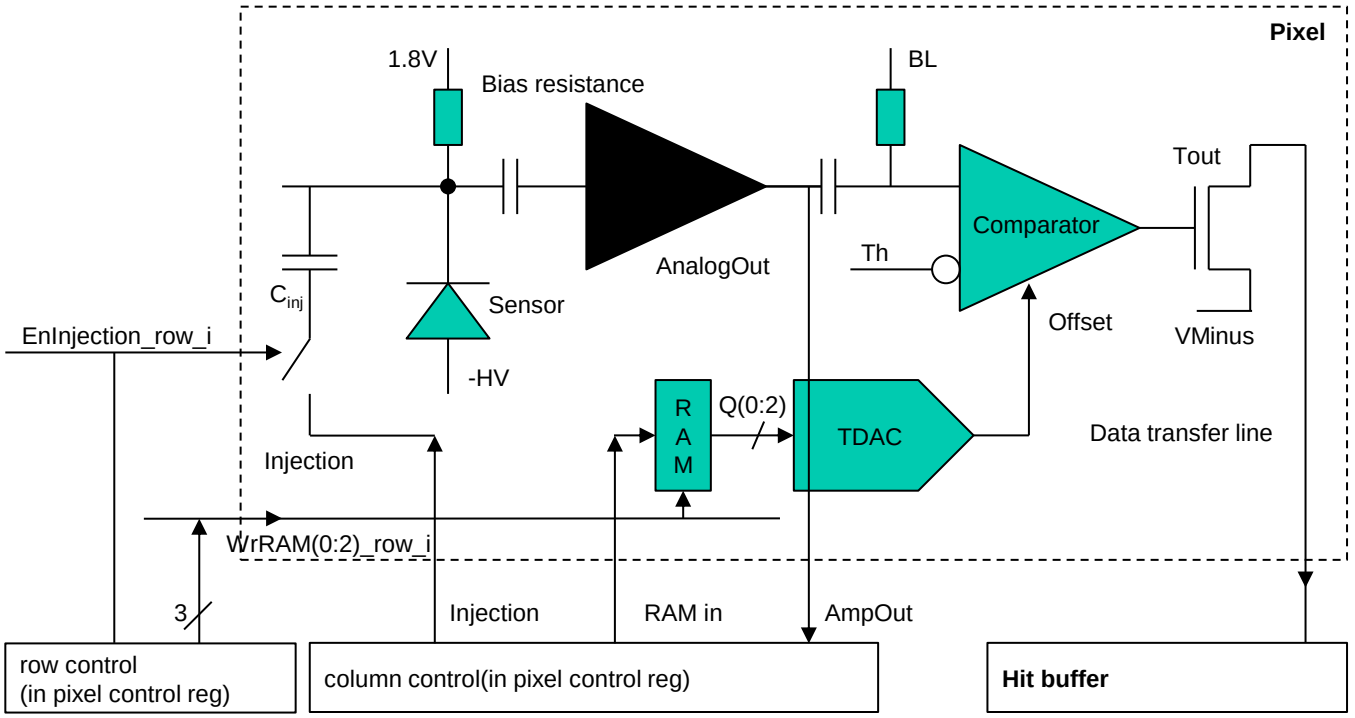

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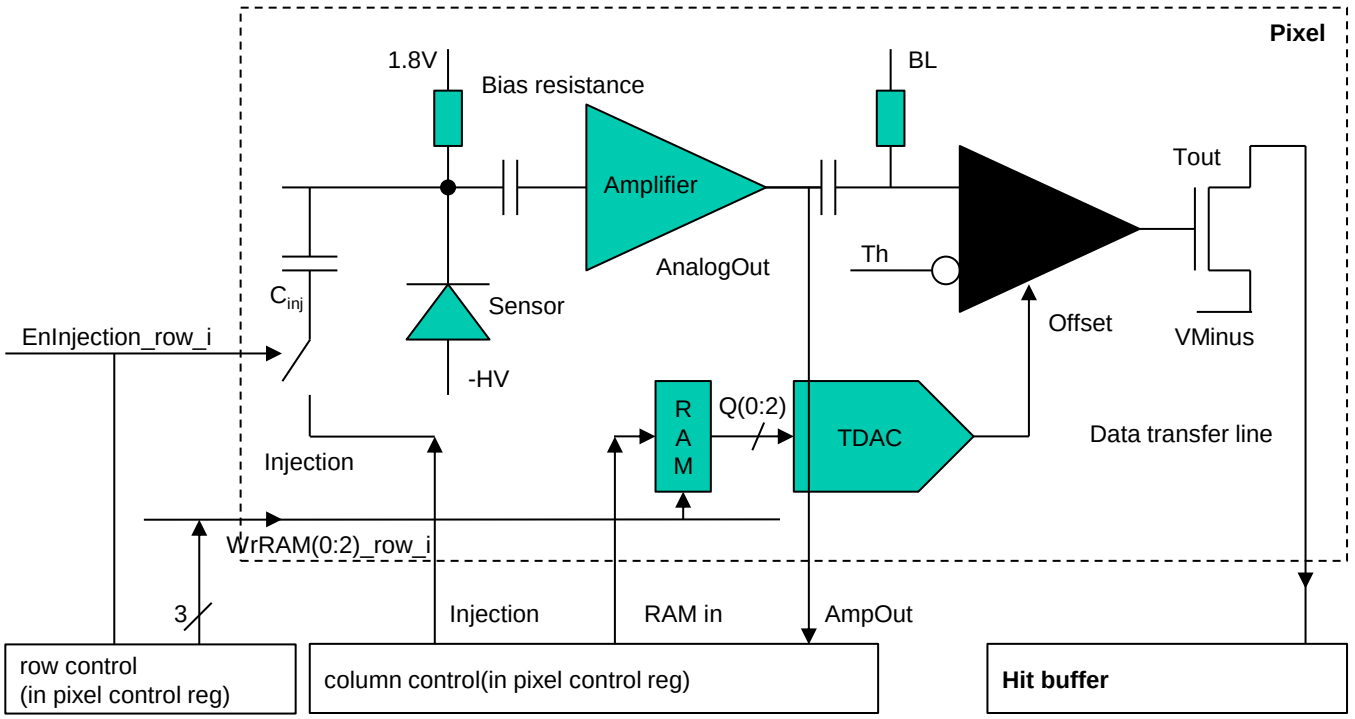

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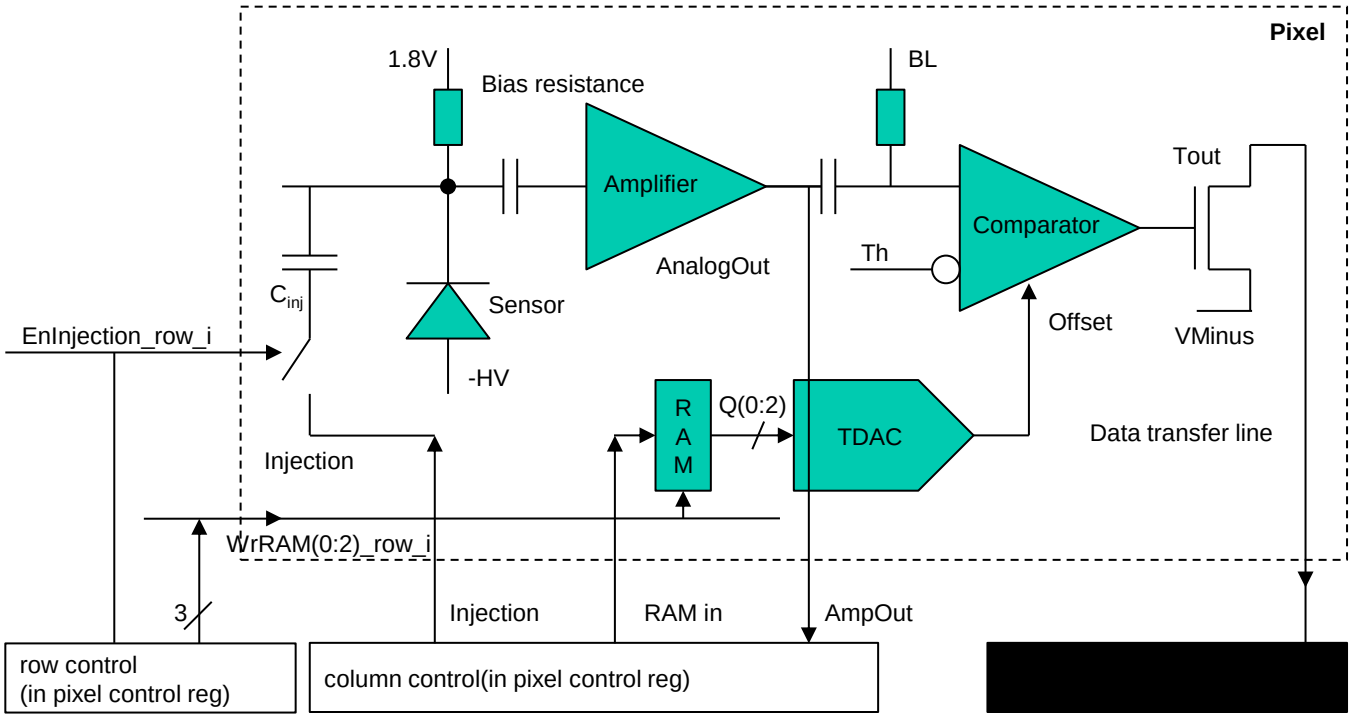
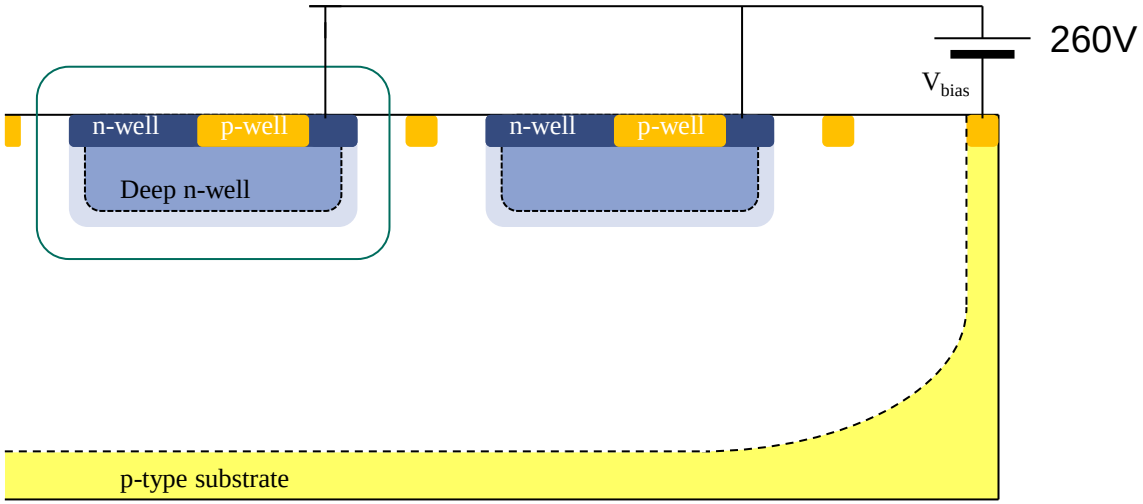
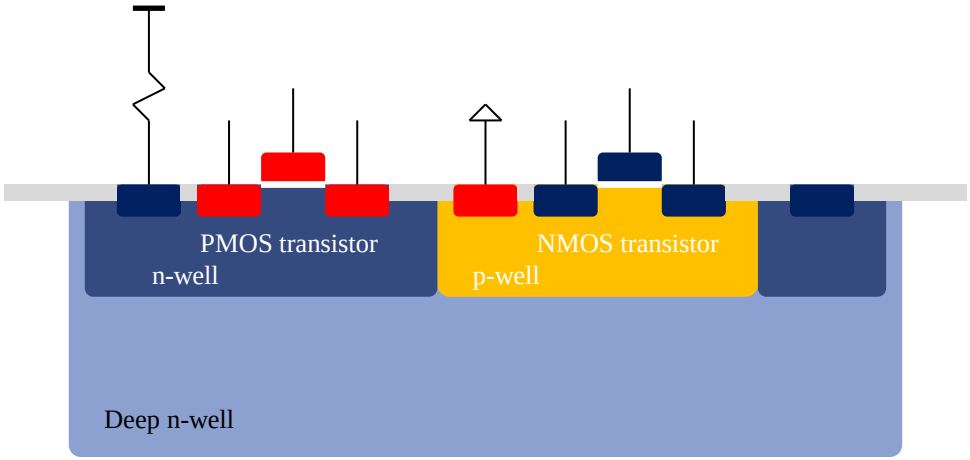


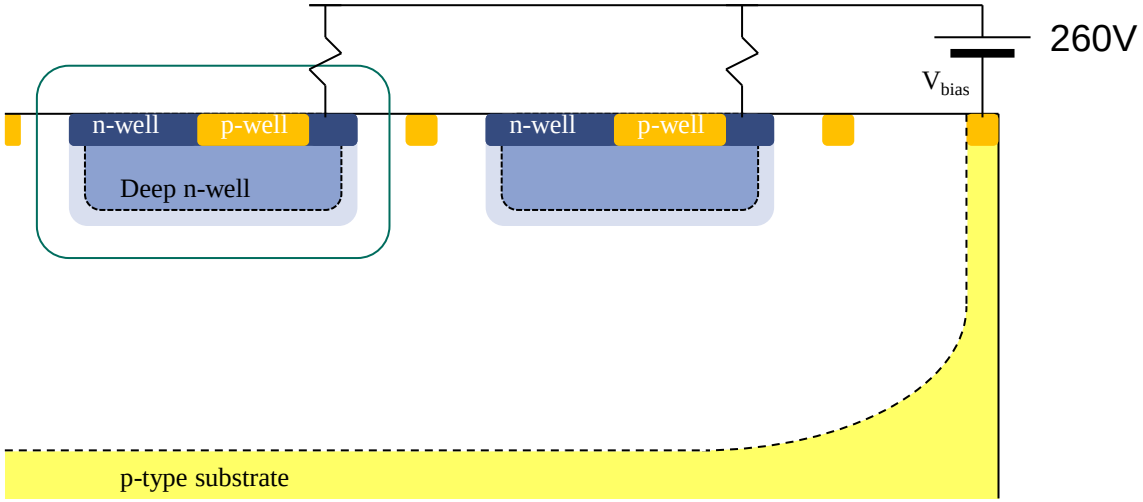
Source: Ivan Perić

- Deep n-well in high-resistivity substrate
- Reverse bias up to ~260 V
- Depletion depth:
  - ~90 µm
- Charge collection by drift

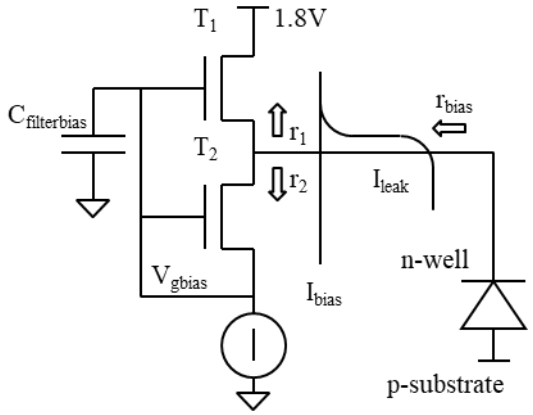




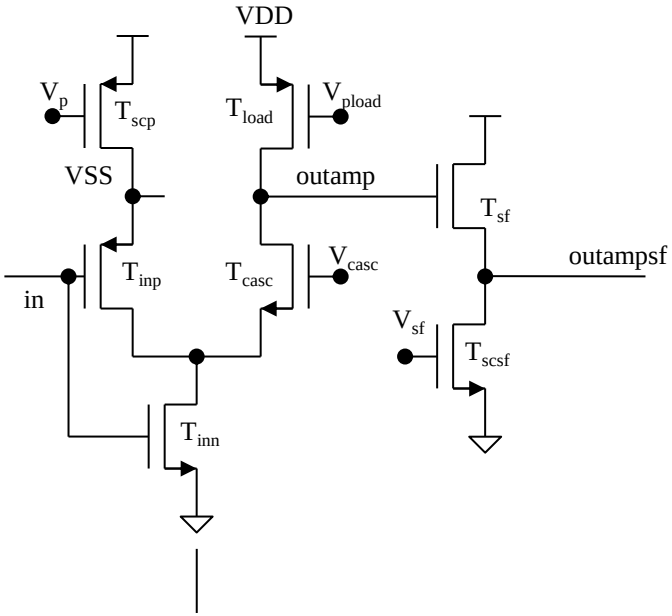
- **Sensor Biasing**
- Deep n-well biased through high-ohmic device
- Maintains correct DC potential
- Avoids low-impedance path for signal charge



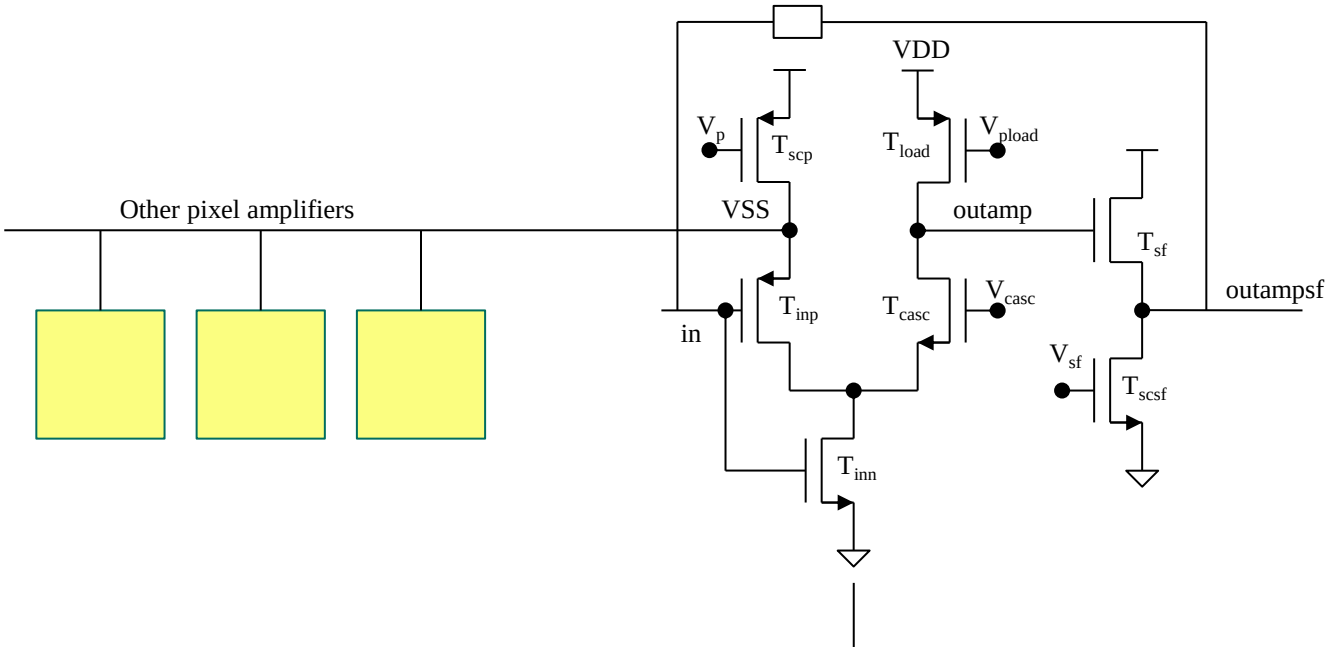
- Bias device implementation:
- Operation:
- T2 provides bias resistance
- T1 carries leakage current



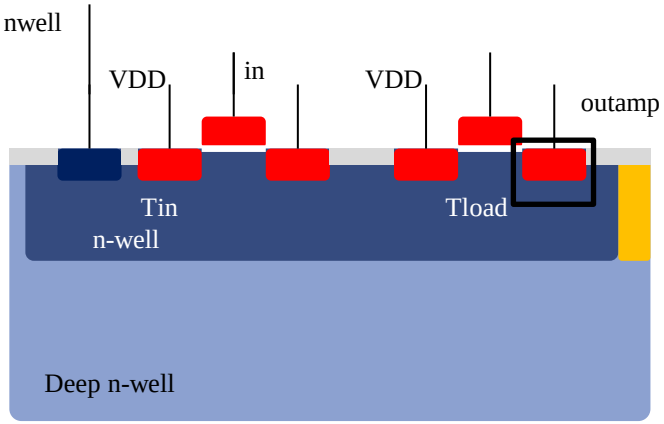
- **Charge Sensitive Amplifier**
- Cascode amplifier architecture
- Combined:
  - NFET input
  - PFET input
- Enhanced transconductance:
  - gm = gm,NMOS + gm,PMOS

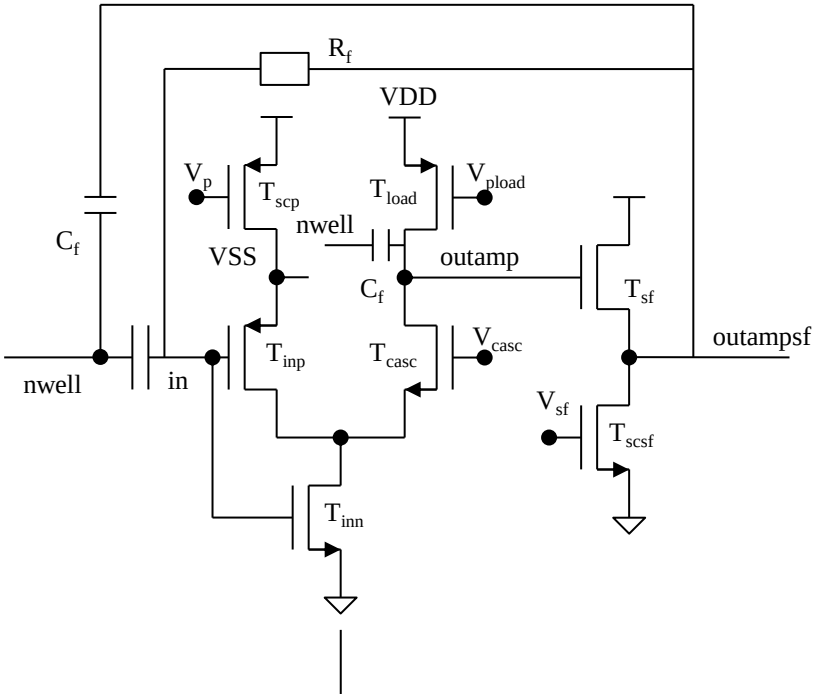


- **CSA Operating Principle**
- NMOS gate controlled by DC feedback
- Current source defines bias current
- PMOS and NMOS share same current
- VSS node:
  - large capacitance
  - AC ground behavior
- AC currents add constructively
- Increased effective gm

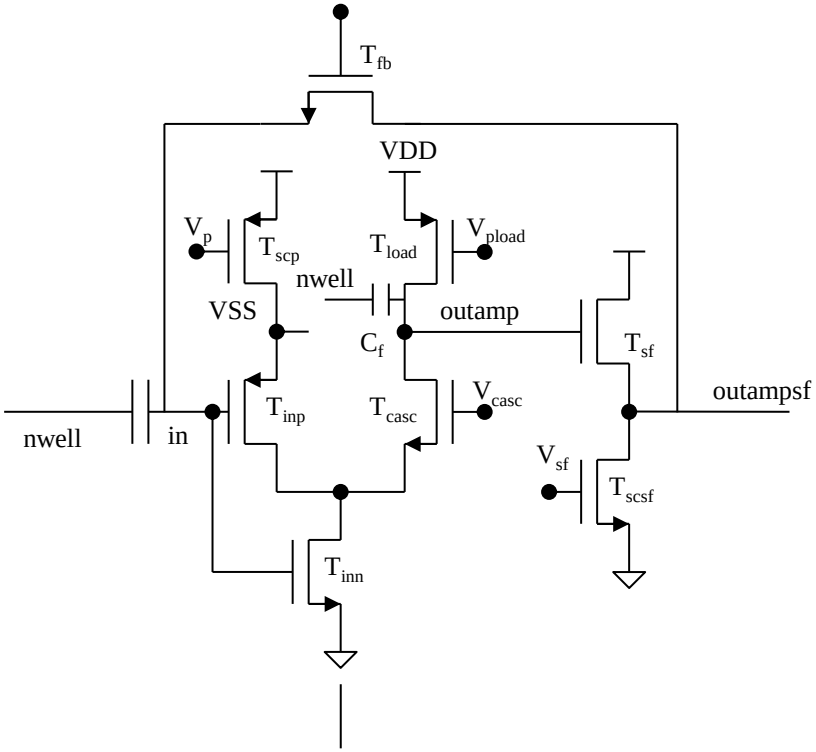


- *Feedback Capacitance (C_f)*
  Realized using **parasitic drain diffusion capacitance** of a MOSFET

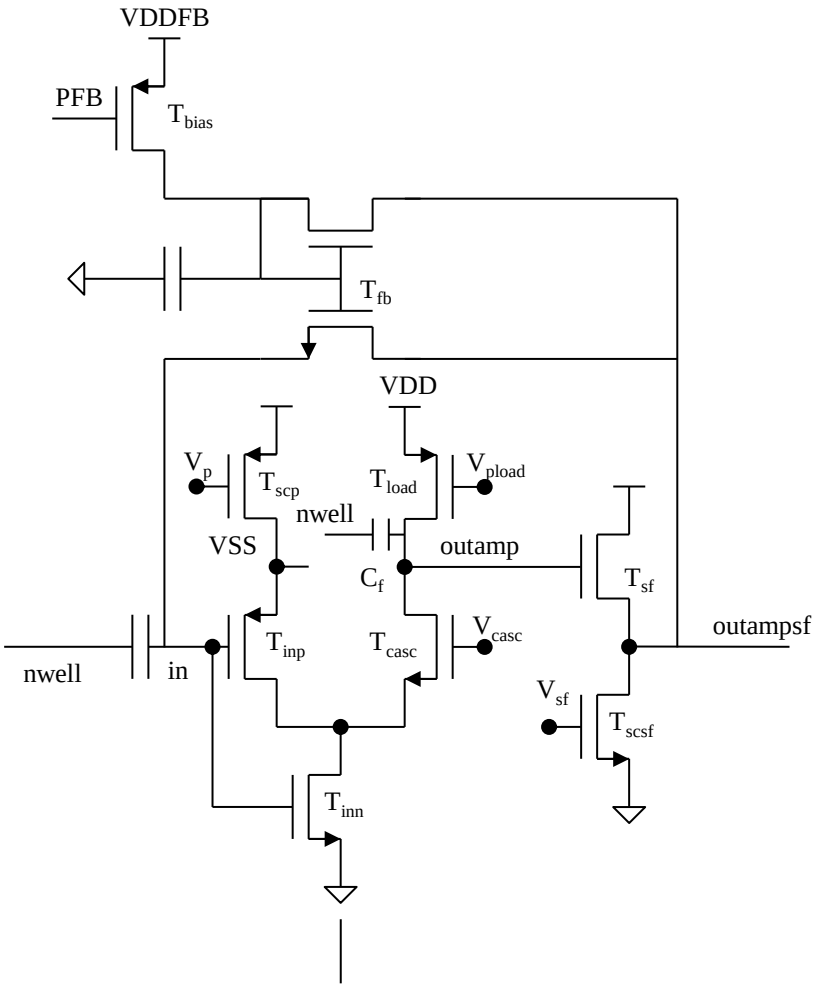




- **Feedback Resistor Implementation**
- Feedback resistor Rf implemented using MOSFET
- Simple implementation:
- Common gate bias generated off-matrix



- **Improved Feedback Biasing**
- Local bias-current generation using Tbias
- Tbias generates small current:
  - ~100 pA
- Current generates gate voltage for Tfb
- PFB generated off-matrix by bias DAC



Optimizing Amplifier Rise Time for Minimum Time Jitter

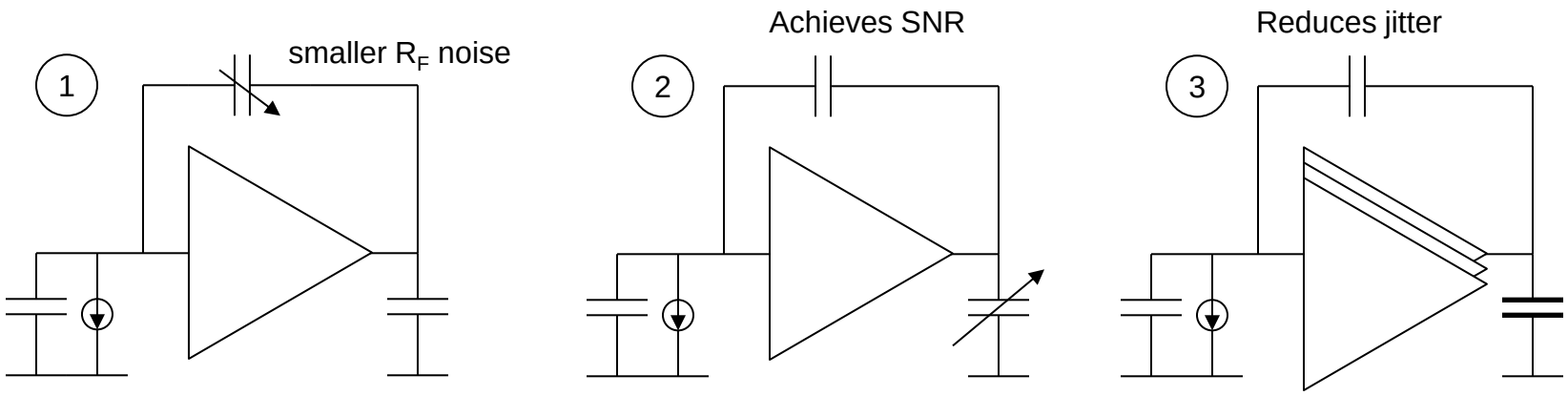
- **Time Jitter Formula:**
- $\mathrm{TJ} \approx T_r \cdot \frac{N}{V_{\mathrm{sig}} - V_{\mathrm{TH}}}$,
- **Noise dependence:**
- $N = \frac{A}{\sqrt{T_r}}$ where $A = \frac{1}{2} \cdot \frac{C_{det}}{C_f} \sqrt{\frac{4kT\gamma n}{g_m}}$
- **Threshold dependence:**
- $V_{\mathrm{TH}} = m\,N = \frac{m\,A}{\sqrt{T_r}}$
- **Combined Expression:**
- $\mathrm{TJ} \approx T_r \cdot \frac{N}{V_{\mathrm{sig}} - m\,N} = T_r \cdot \frac{\frac{A}{\sqrt{T_r}}}{V_{\mathrm{sig}} - \frac{m\,A}{\sqrt{T_r}}}$
- Time jitter **depends nonlinearly** on Tr.
- Small Tr → higher noise. Large Tr → slower signal.
- Optimal **Tr minimizes TJ**: trade-off between **noise** and **signal timing**.

Optimizing Amplifier Rise Time for Minimum Time Jitter

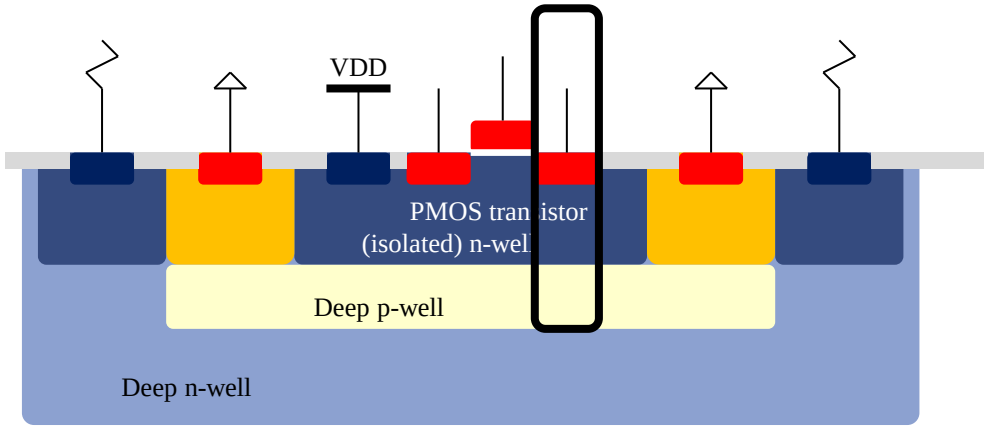
- **Optimal Rise Time:**
- $T_r = \left(\frac{2\,m\,A}{V_{\text{sig}}}\right)^2;\; A = \frac{1}{2}\cdot\frac{C_{det}}{C_f}\sqrt{\frac{4kT\gamma n}{\frac{I_{bias}}{nU_T}}} = nU_T\frac{C_{det}}{C_f}\sqrt{\frac{e\gamma}{I_{bias}}}$
- **At optimum:**
- $N = \frac{V_{\text{sig}}}{2\,m} \Rightarrow\; SNR = \frac{V_{\text{sig}}}{N} = 2m \Rightarrow\; \sigma_J \approx \frac{T_r}{m}$

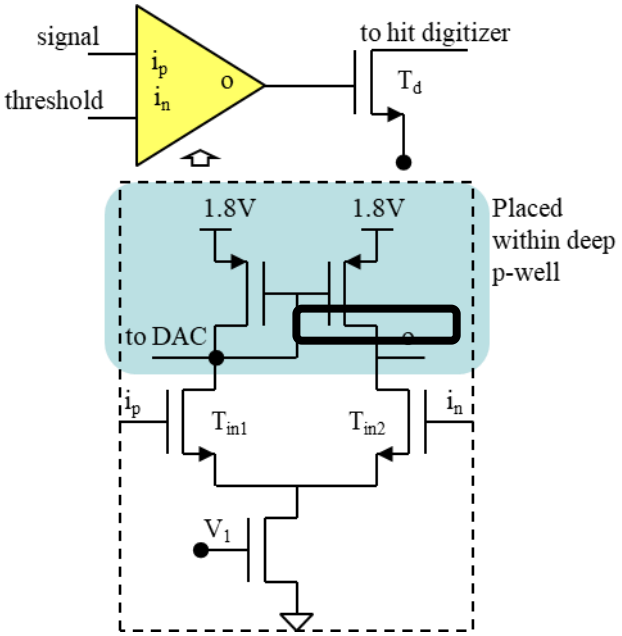
Optimizing Amplifier Rise Time for Minimum Time Jitter

- **Step 1:** First, we scale down C_f until the R_f - noise contribution becomes small enough.
- **Step 2:** Adjust rise time Tr (via output capacitance Co) to achieve SNR = 2m
- **Step 3:** Multiply transistors to increase bias current Ibias
  - Keeps SNR optimal
  - Decreases Tr → reduces timing jitter
- **Trade-off:** Increasing Ibias raises power consumption
  → balance time resolution vs. power efficiency
- **Assumption:** Charge collection time ≪ Tr

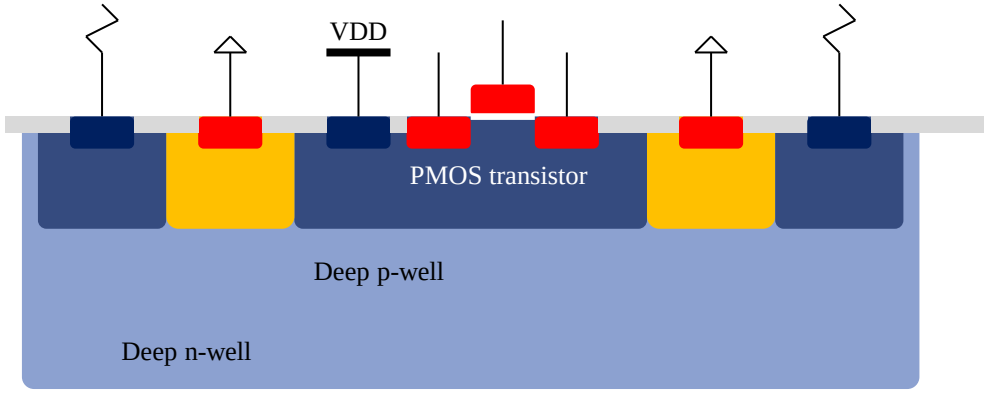


- **Comparator Architecture**
- Challenge:
- Large signals on PMOS diffusion contacts can cause parasitic charge injection into sensing deep n-well
- Solution: Isolated n-well
- Isolated n-well available in:
- AMS aH18
- TSI 180 nm HV-CMOS
- LFoundry 150 nm

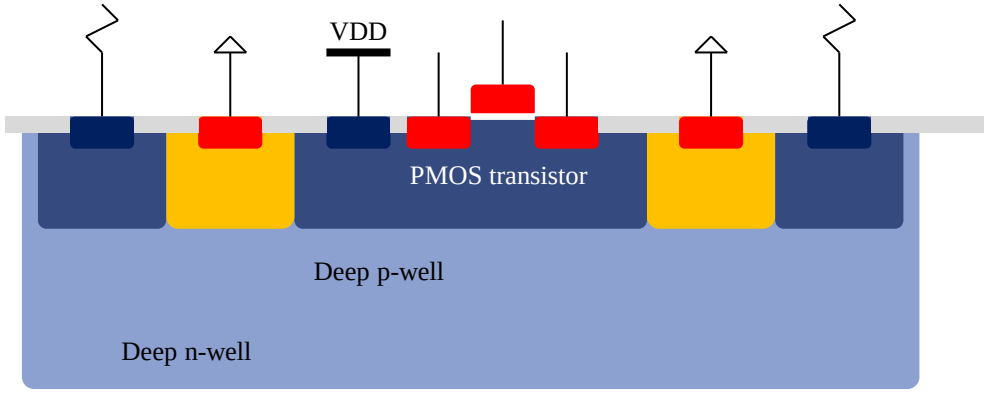


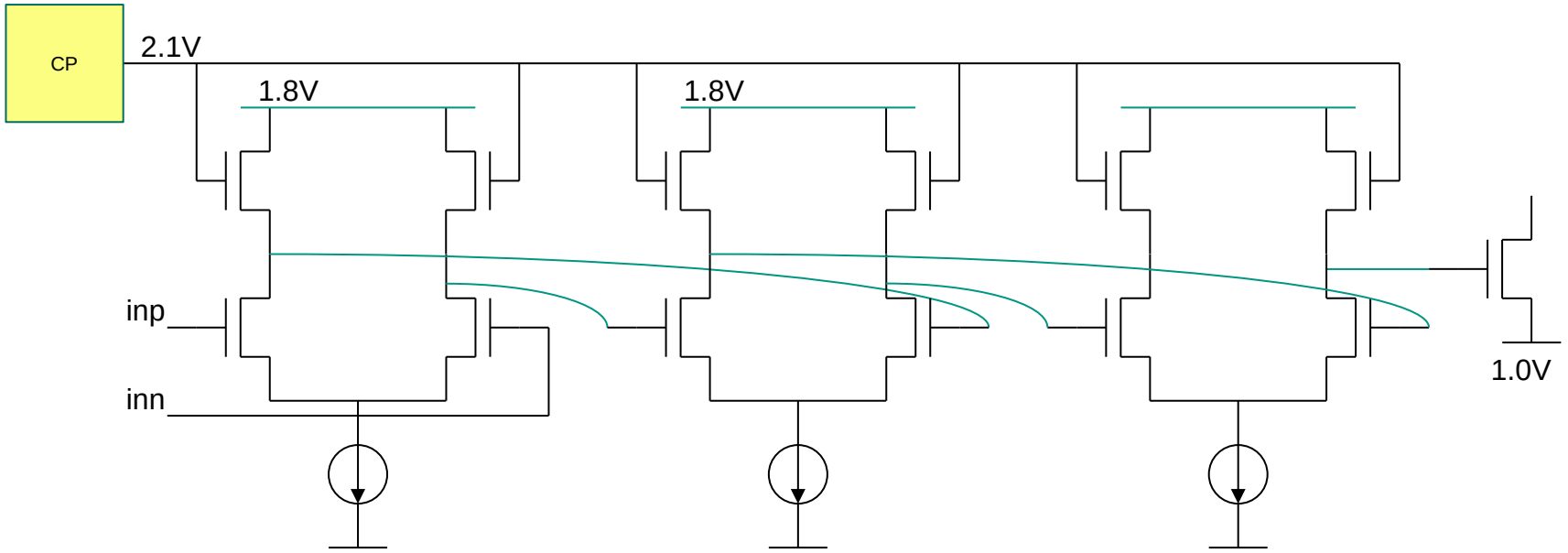


- MightyPix2:
- no isolated PMOS option available



- MightyPix2:
- fully NMOS-based comparator
- Three-stage cascade
- NFET differential amplifiers, NFET loads
- No PFET loads:
- avoid parasitic charge injection





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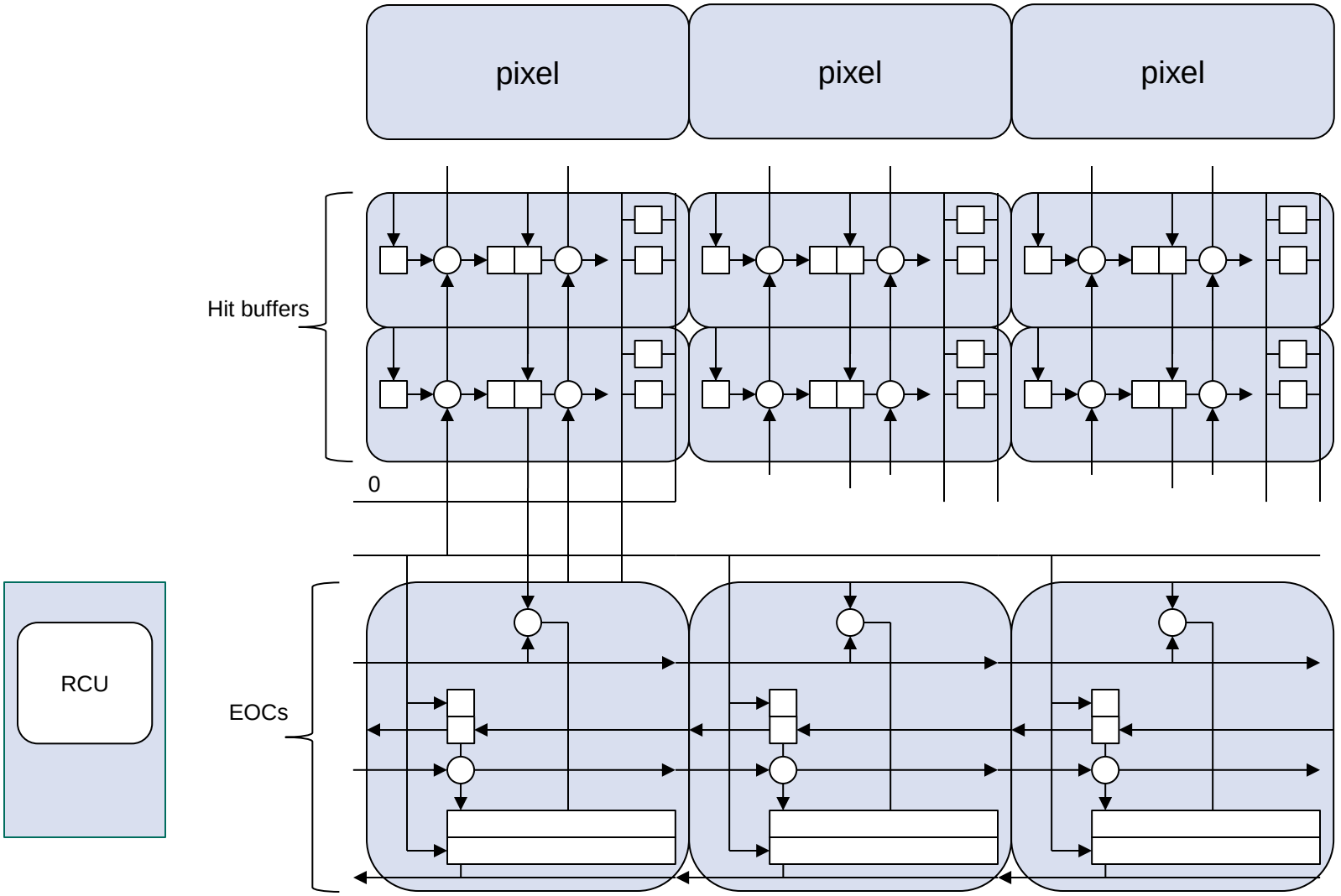

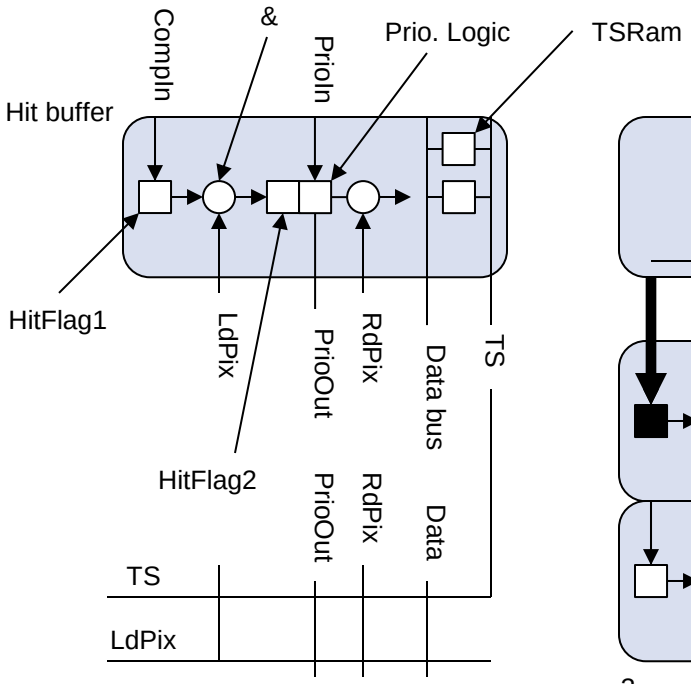
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PrioIn
Prio. Logic
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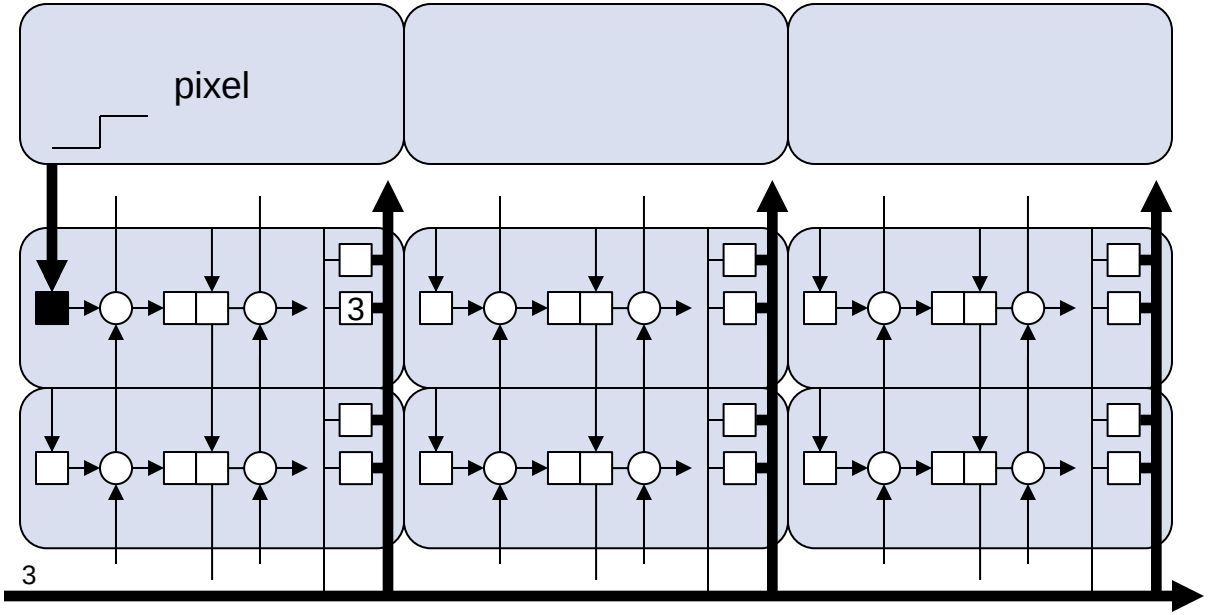
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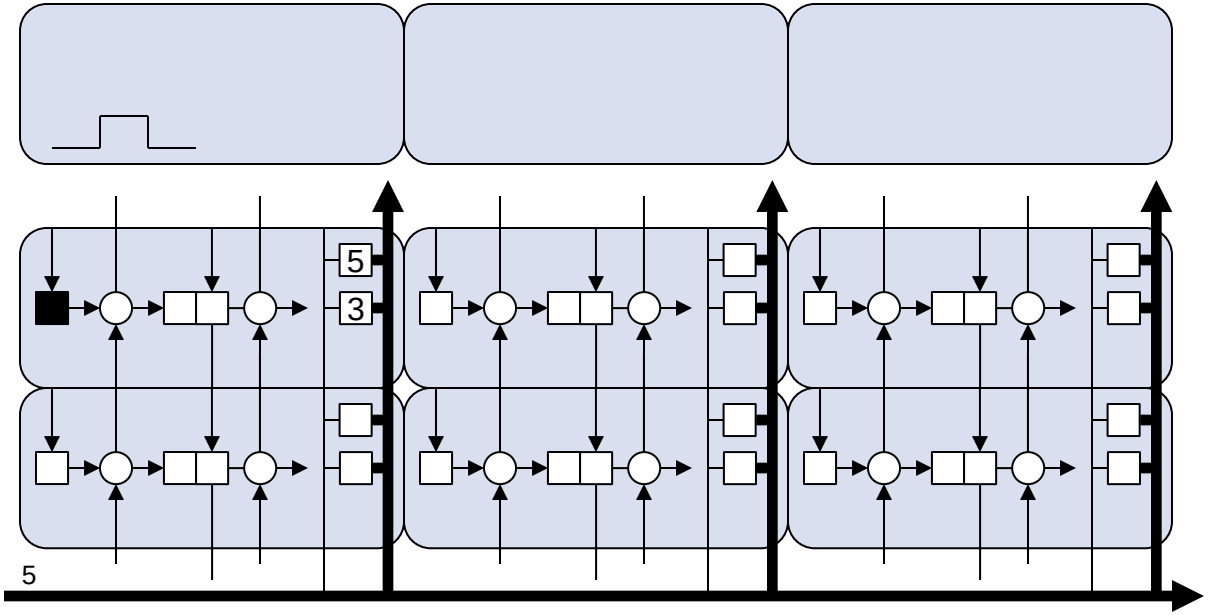
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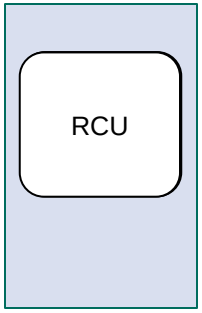
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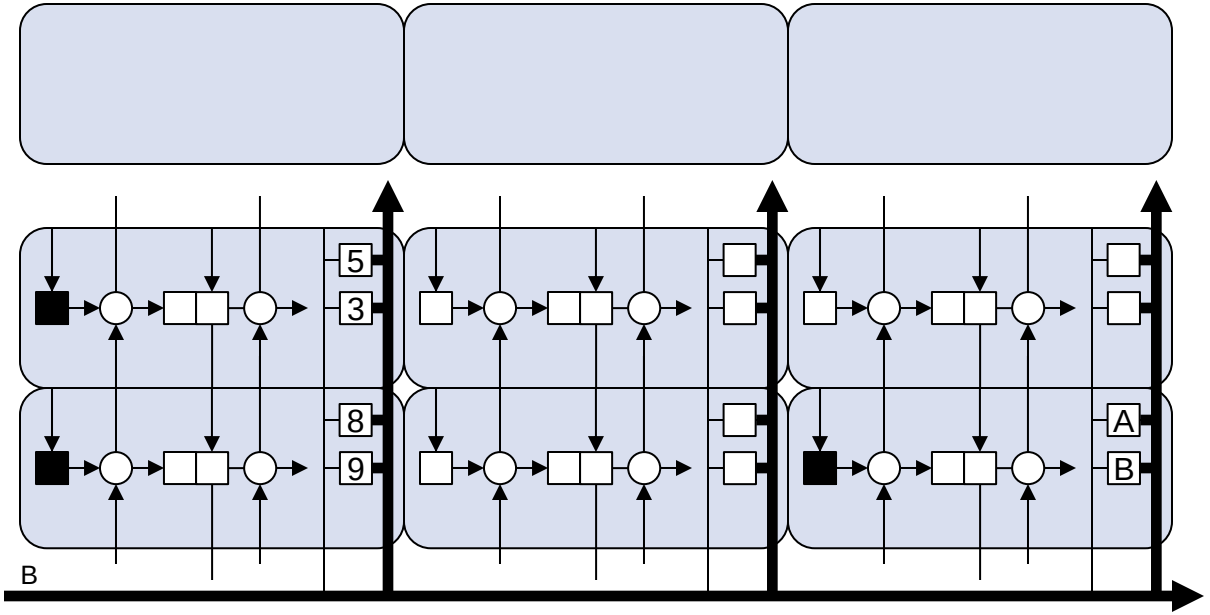
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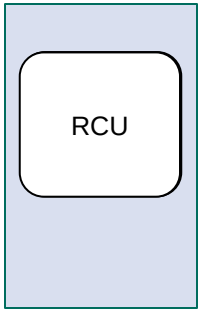
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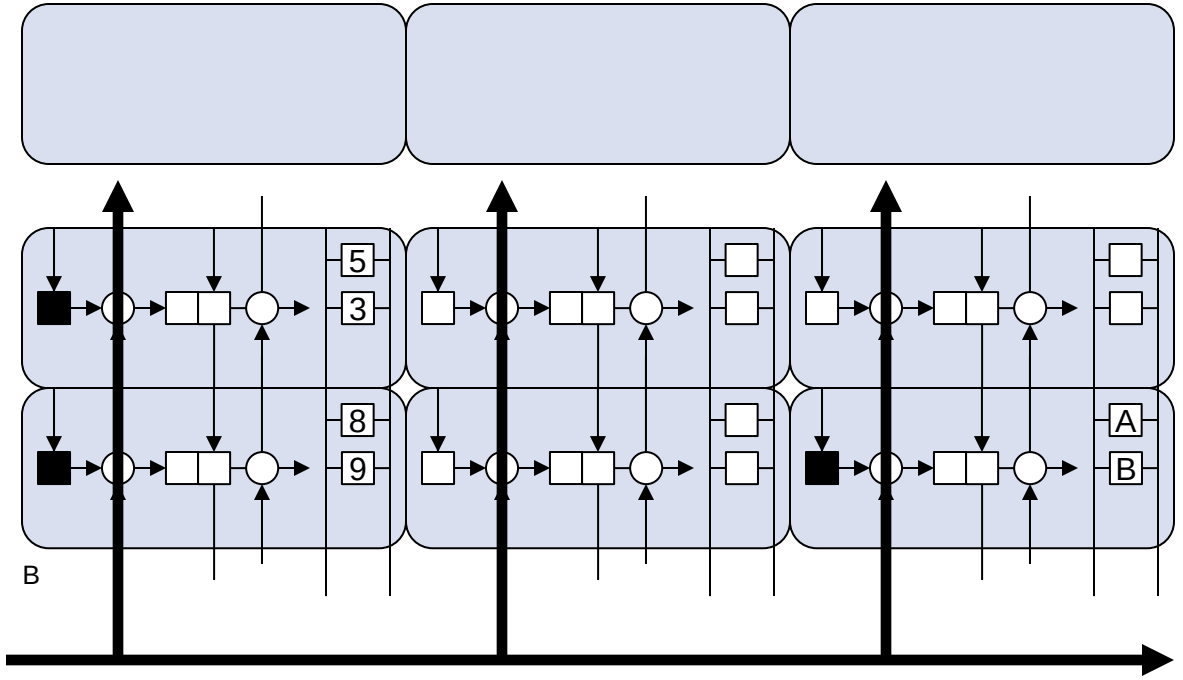
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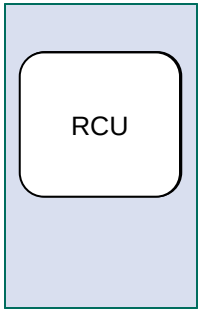
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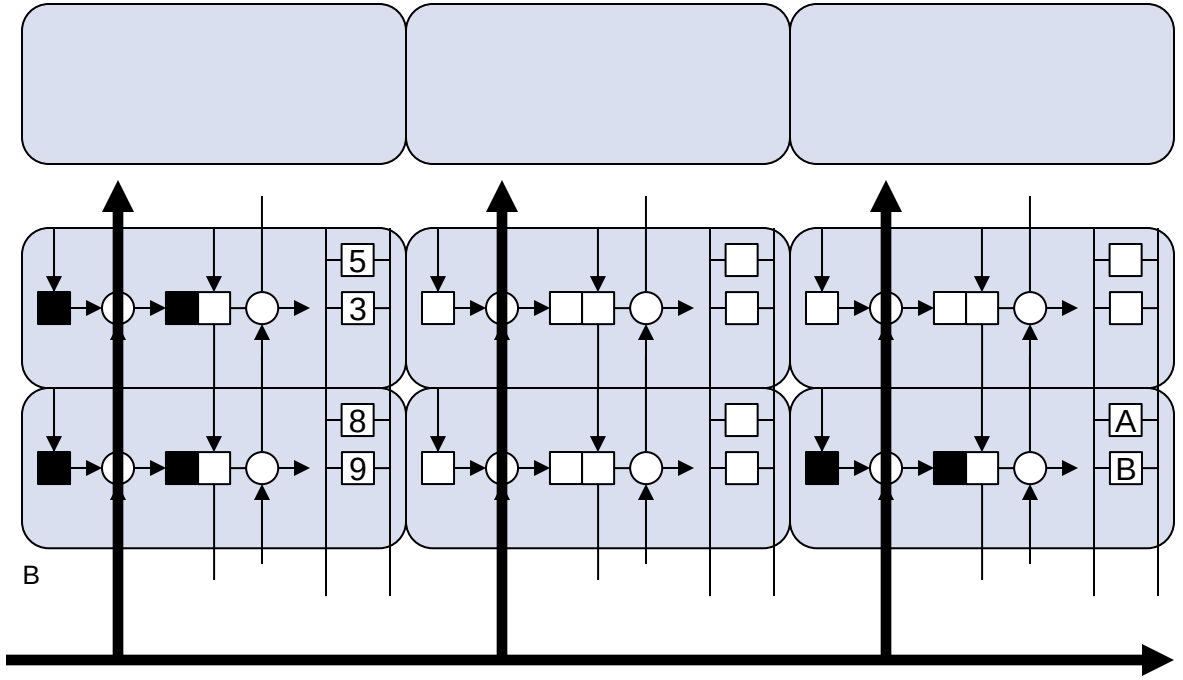
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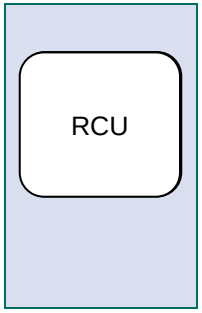
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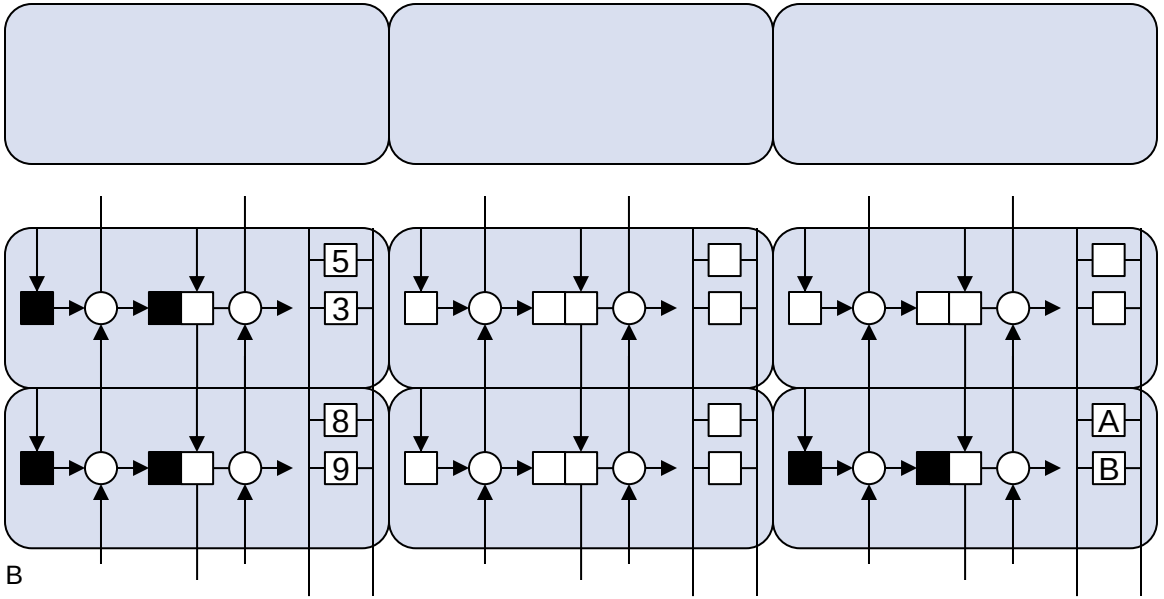
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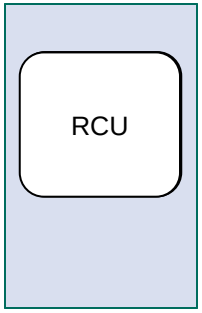
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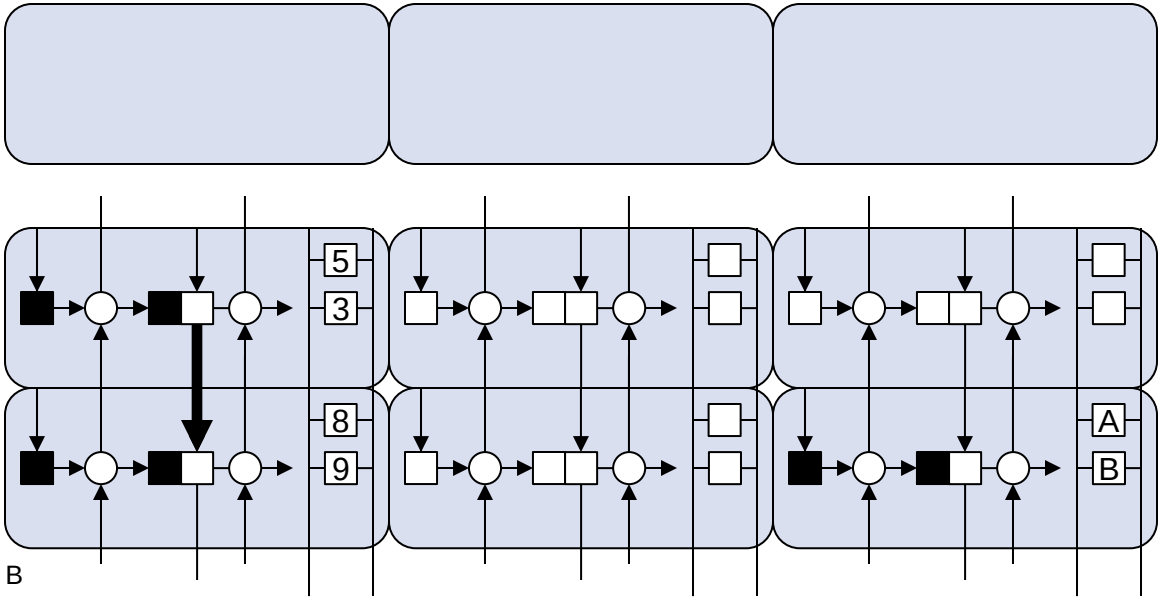
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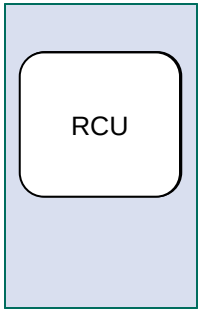
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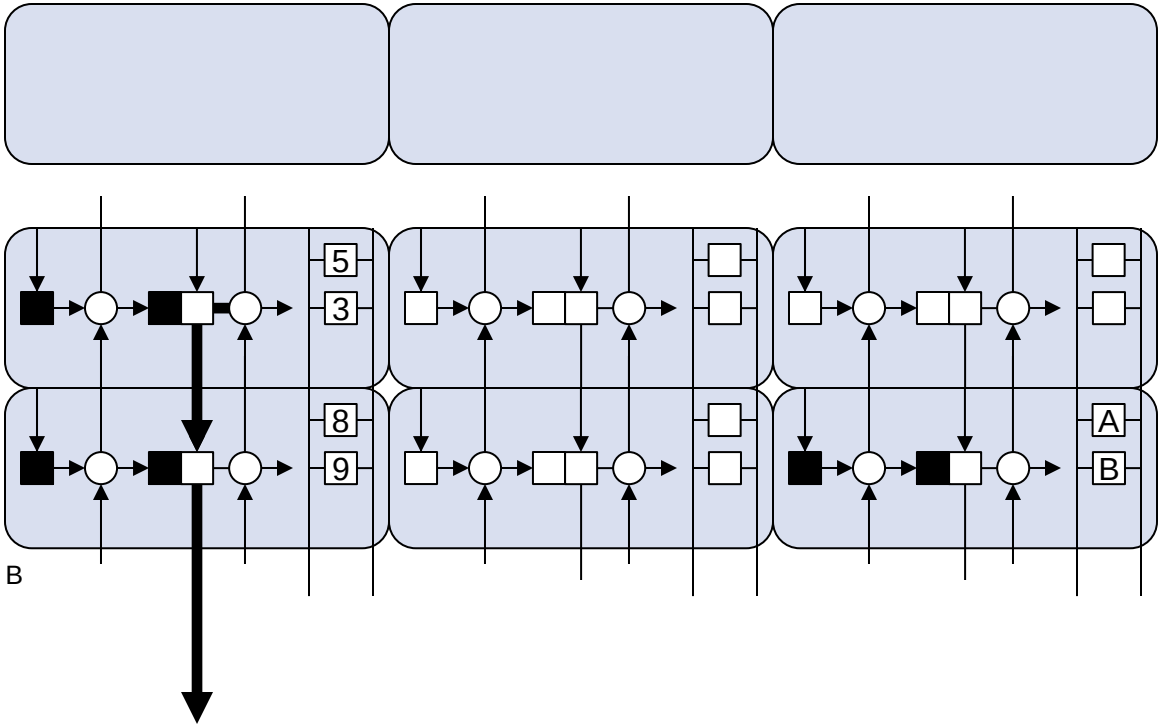
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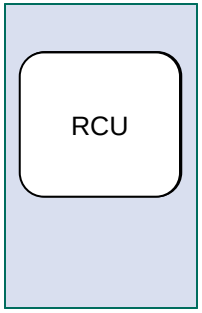
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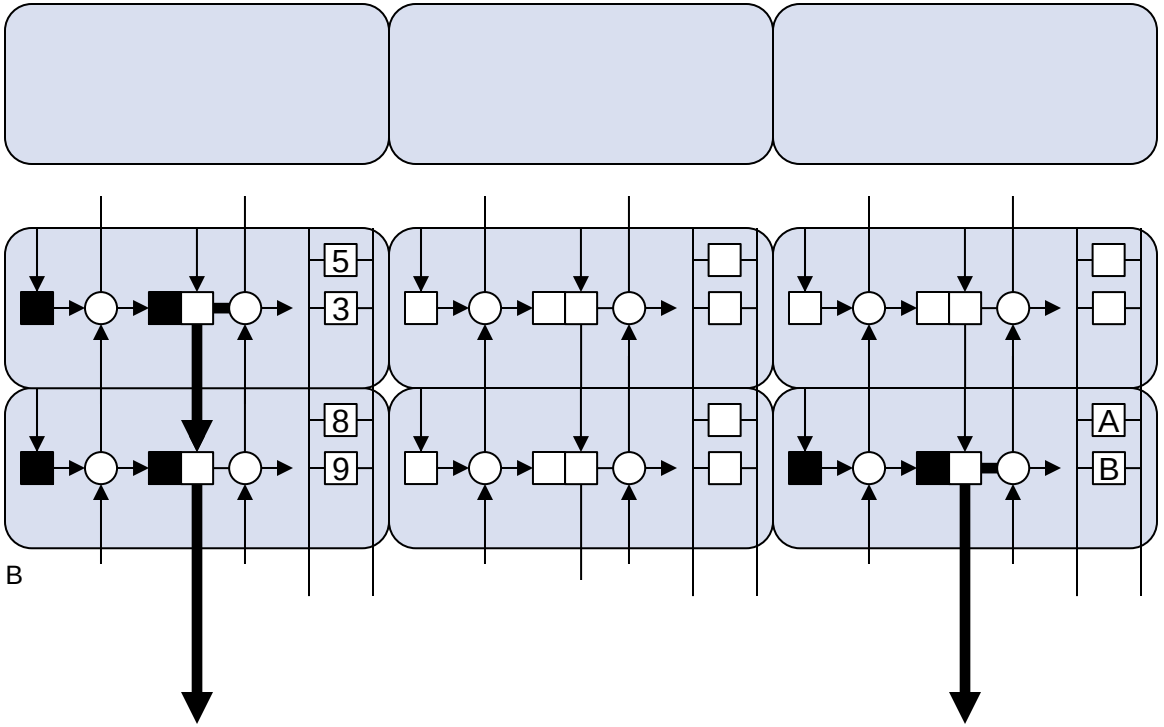
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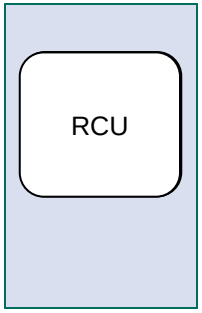
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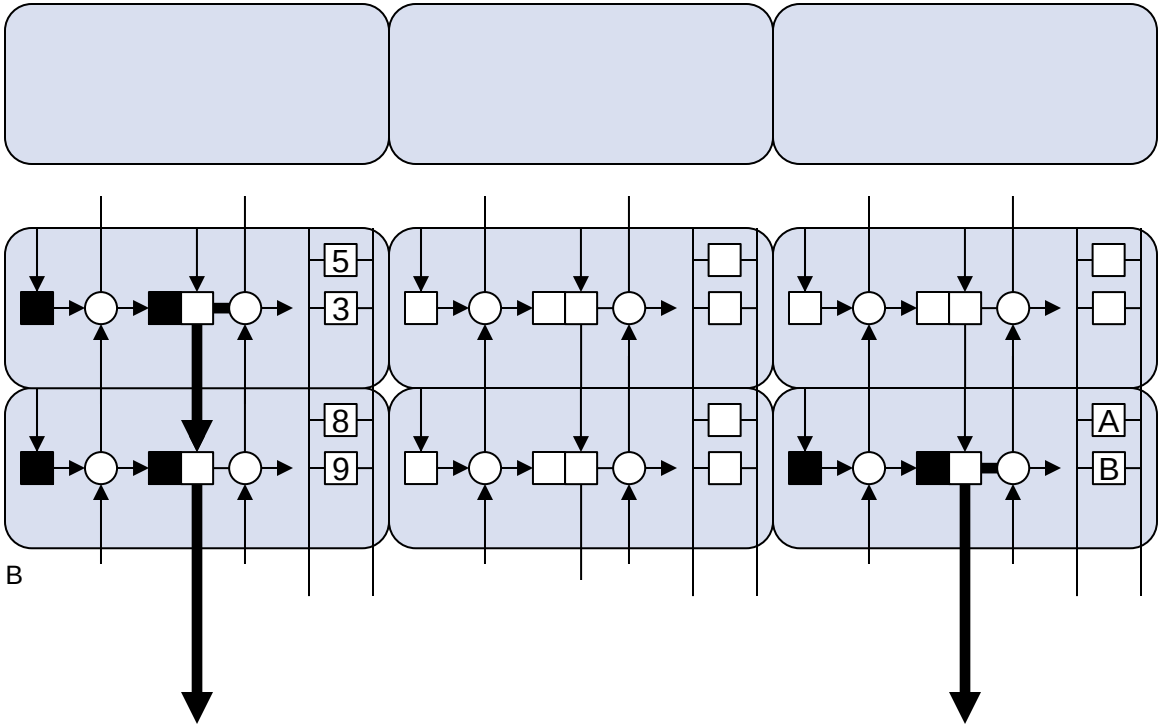
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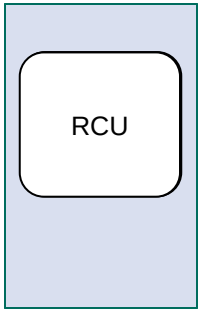
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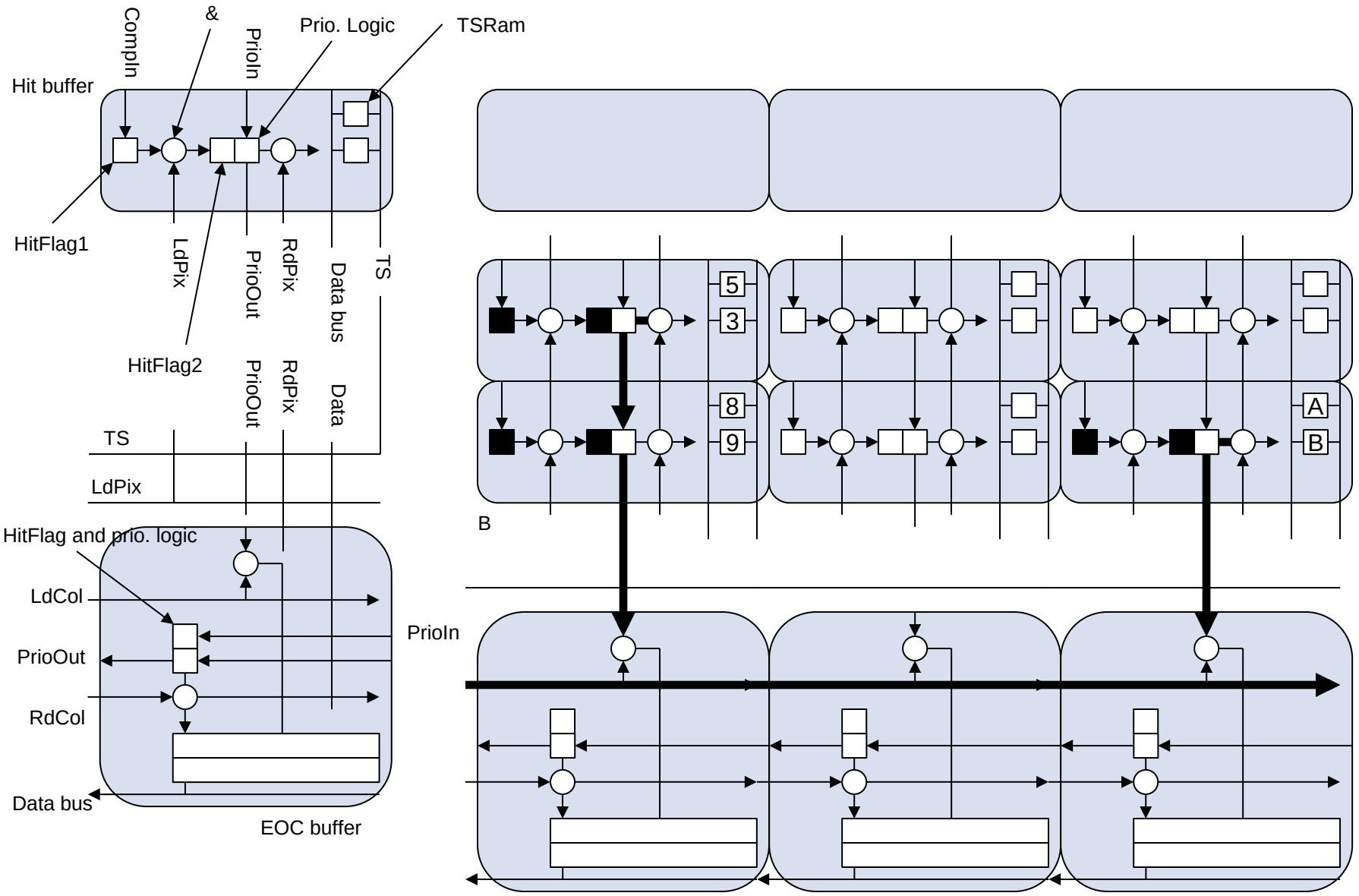
CompIn
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Prio. Logic
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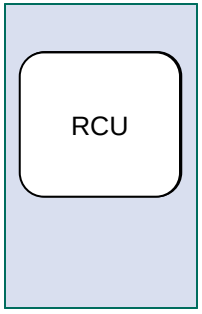
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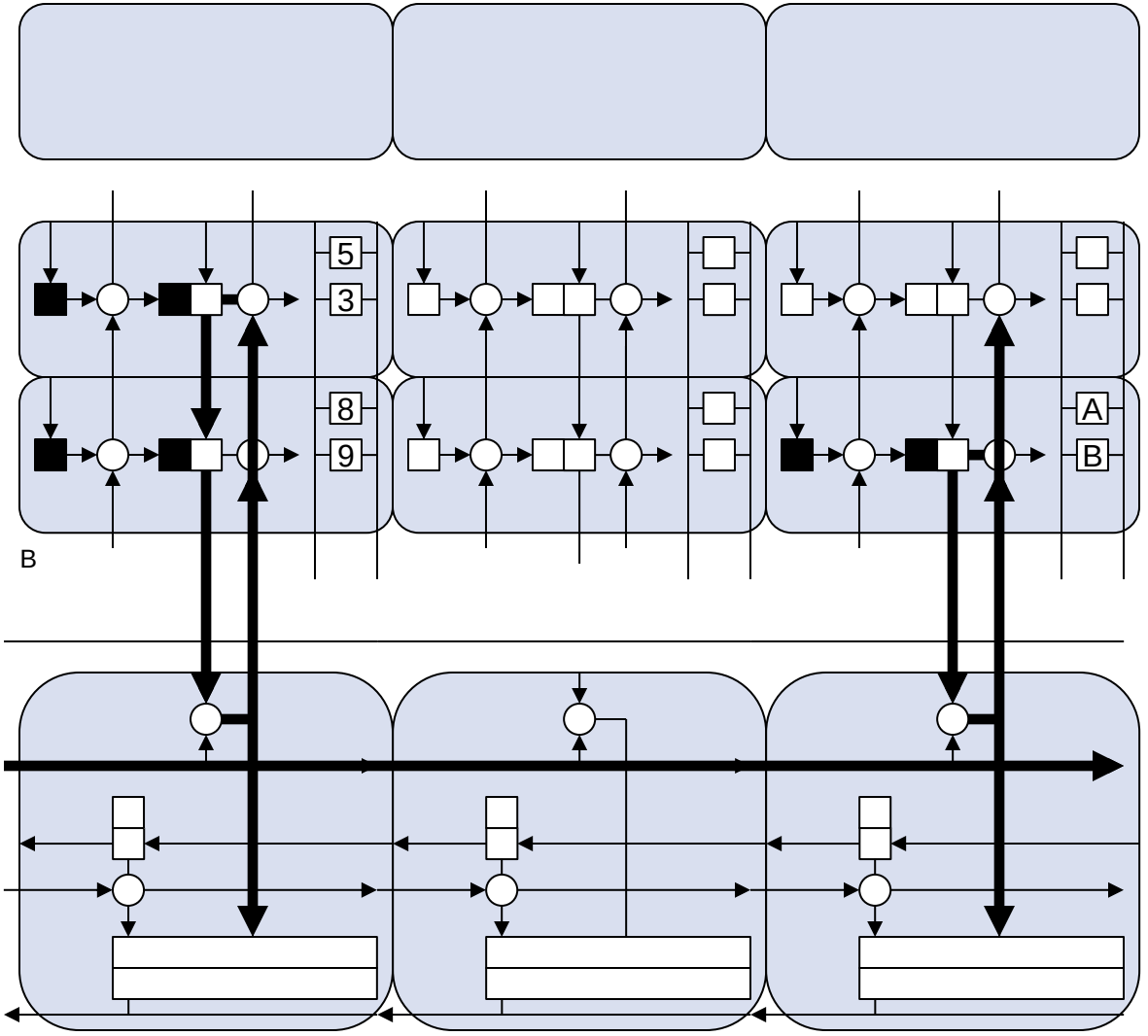
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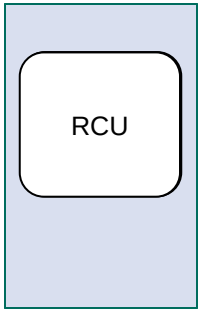
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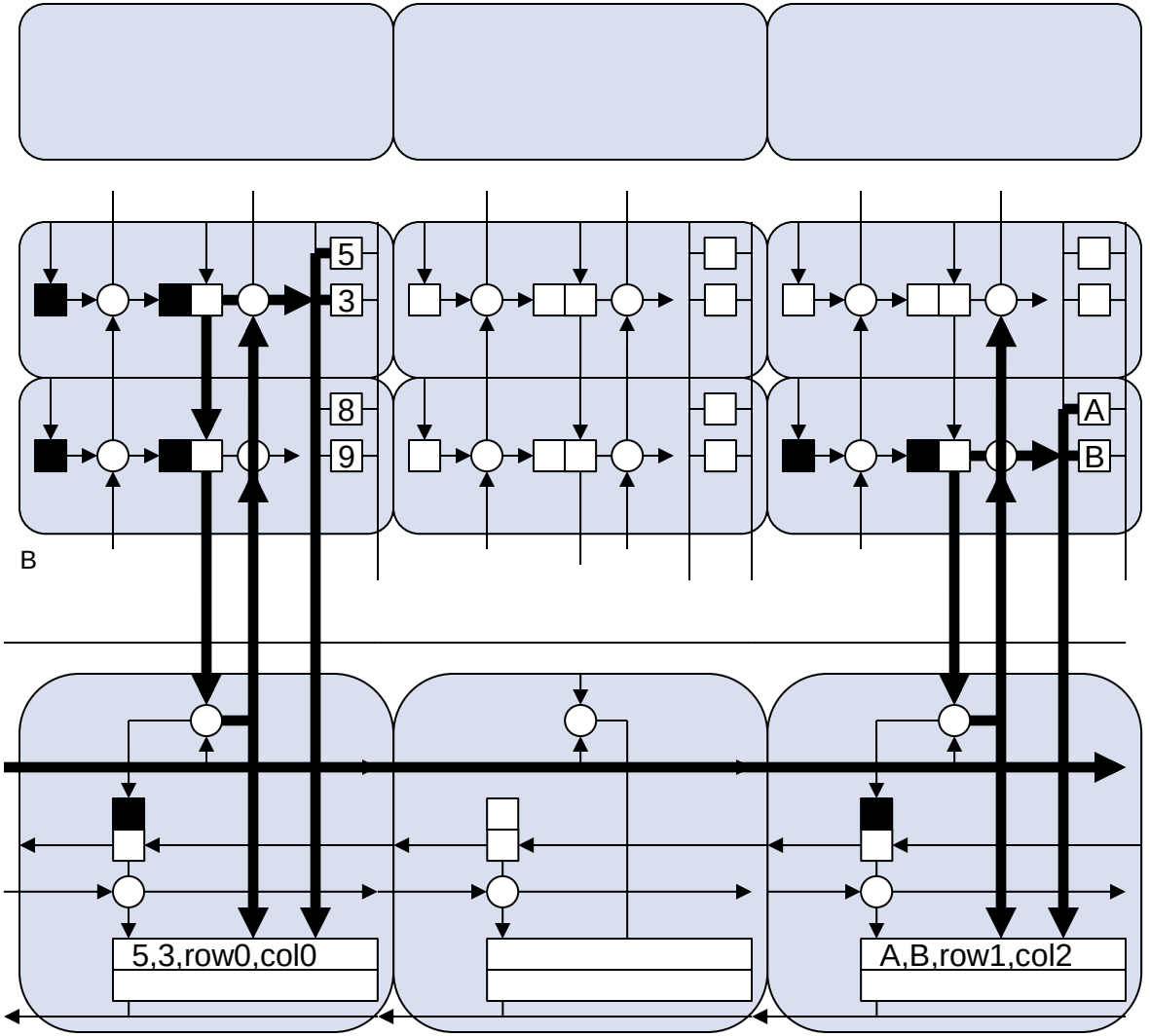
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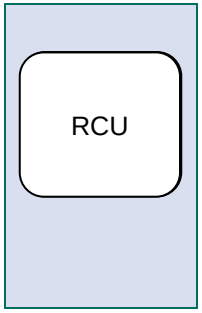
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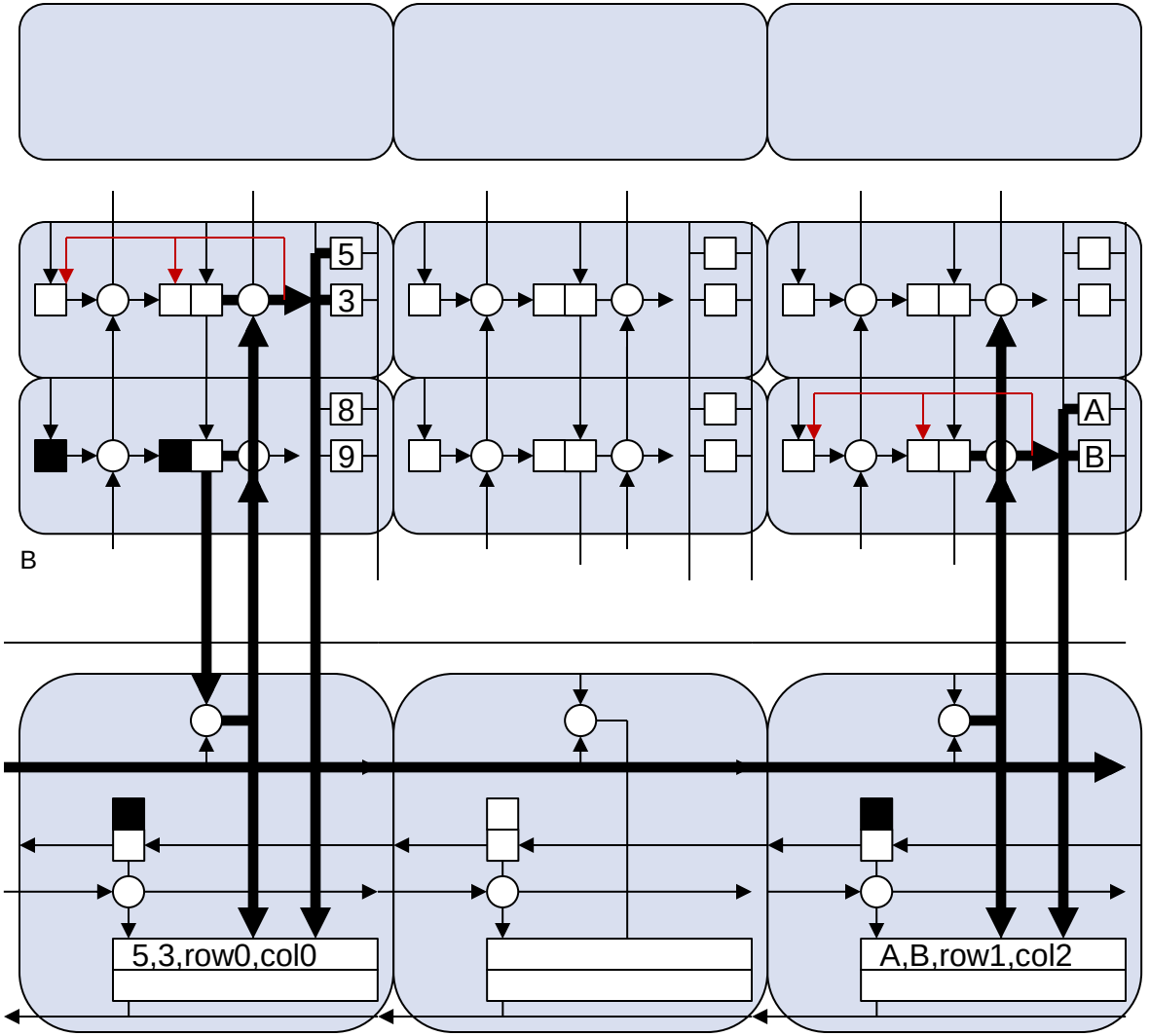
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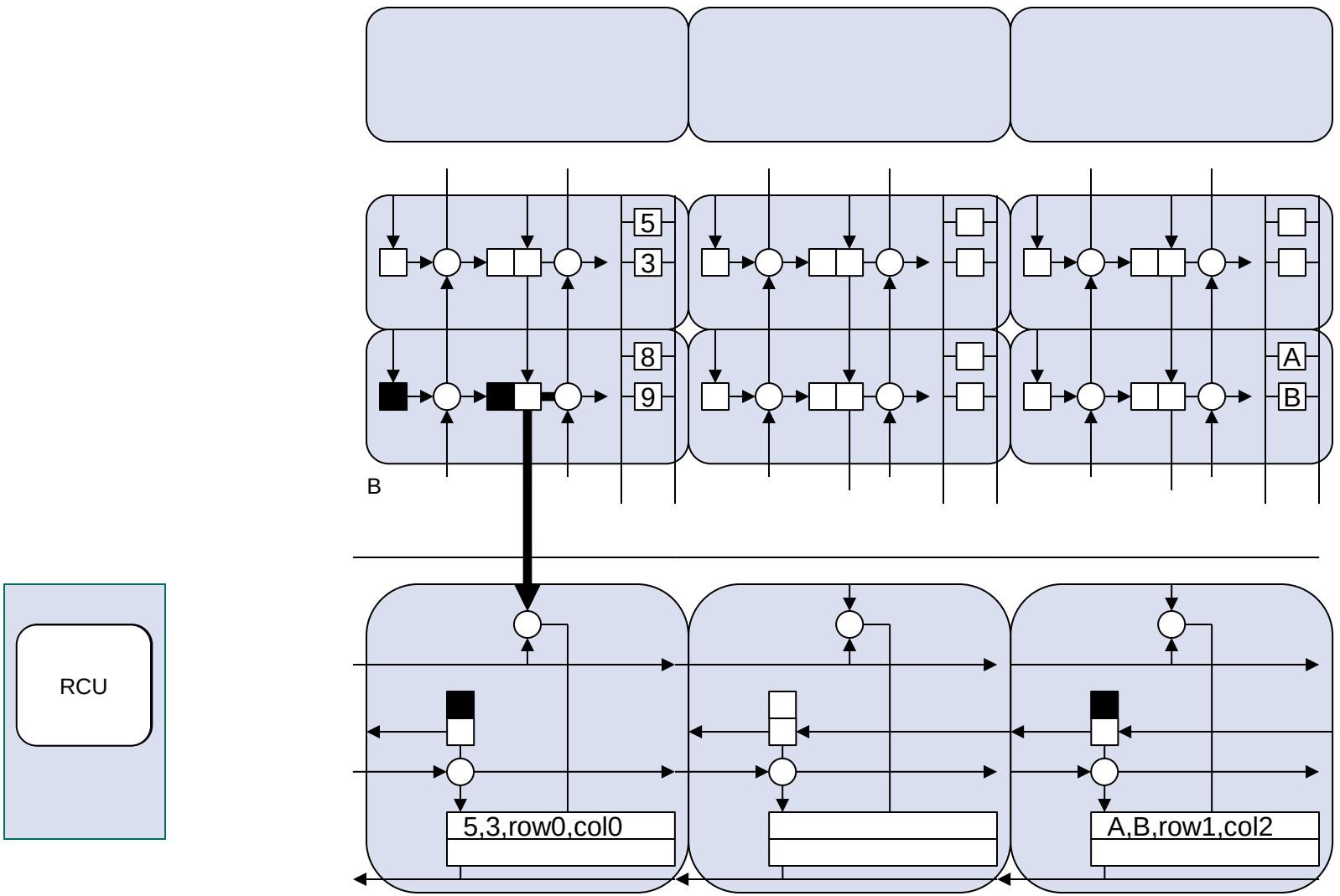
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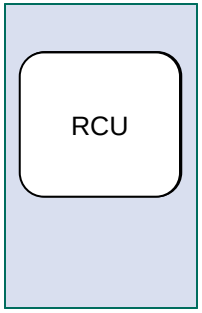
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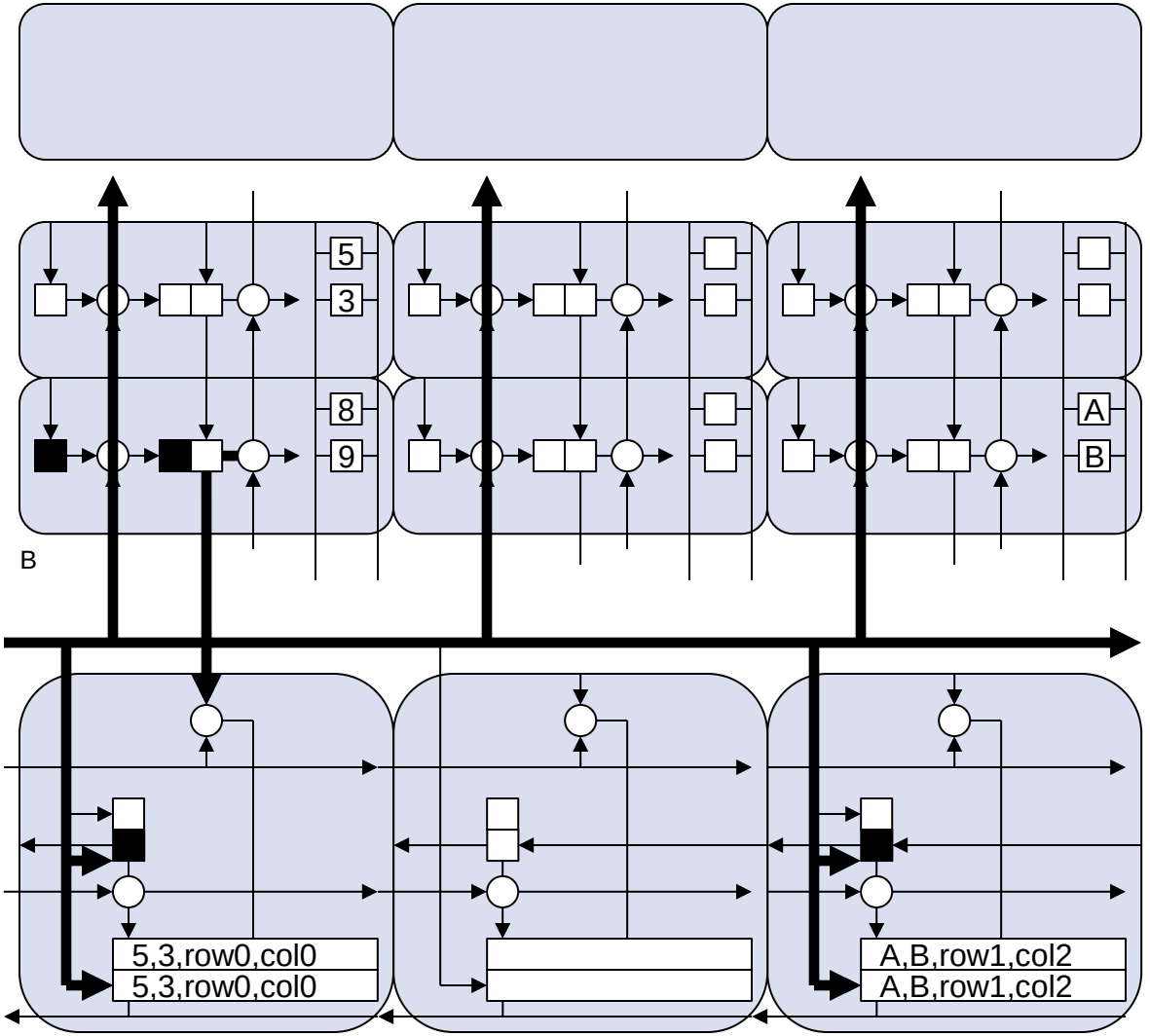
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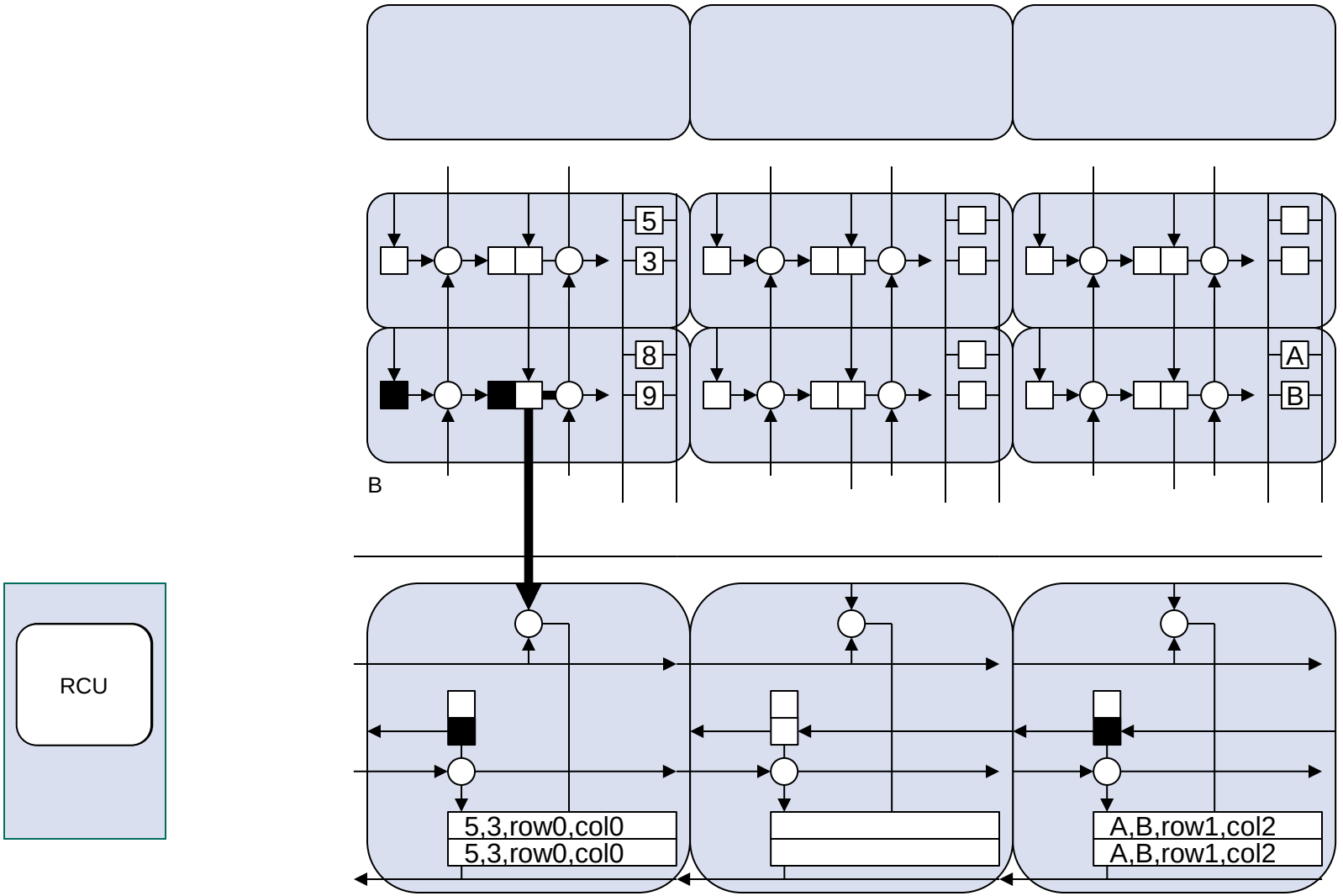
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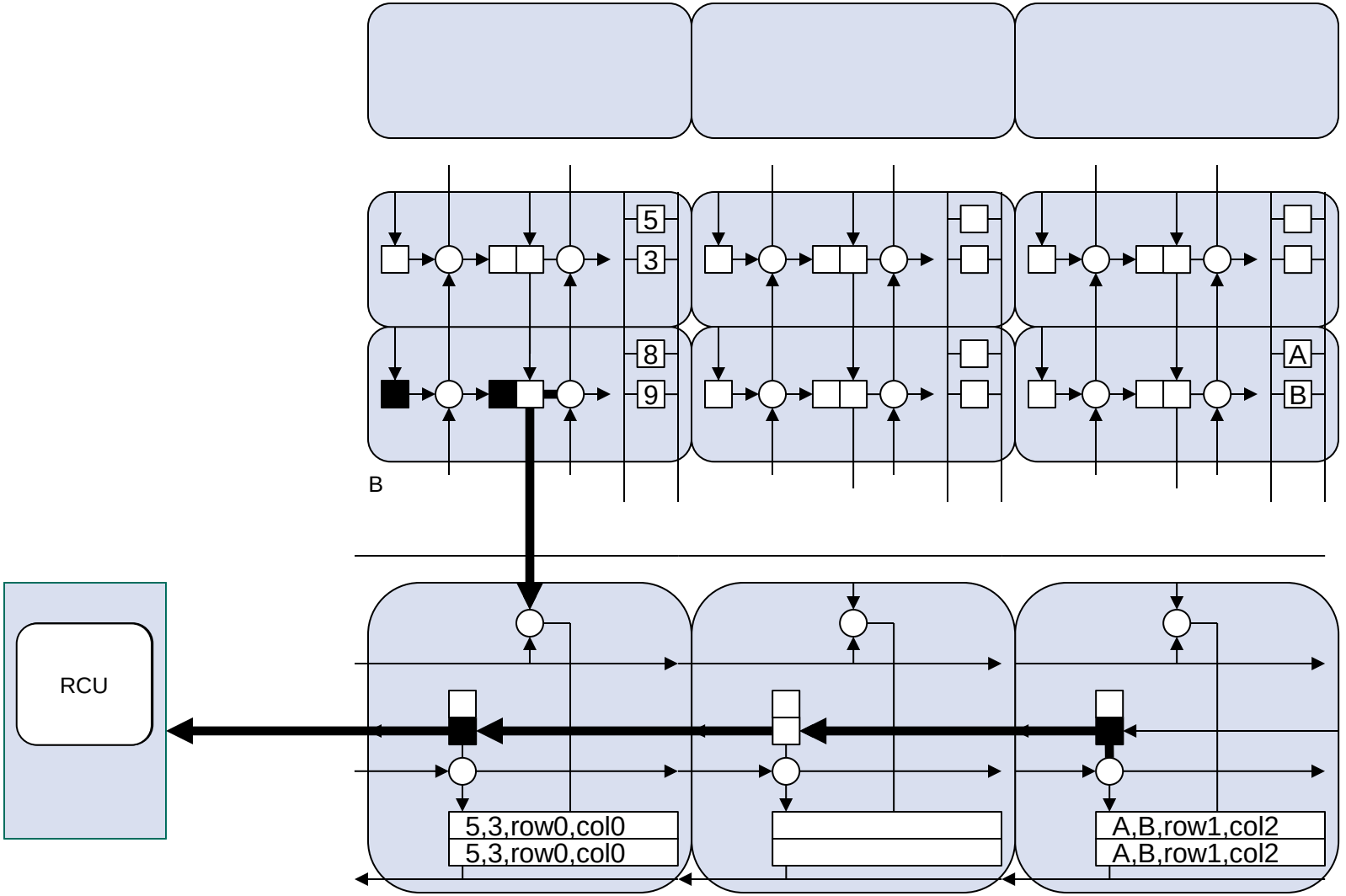
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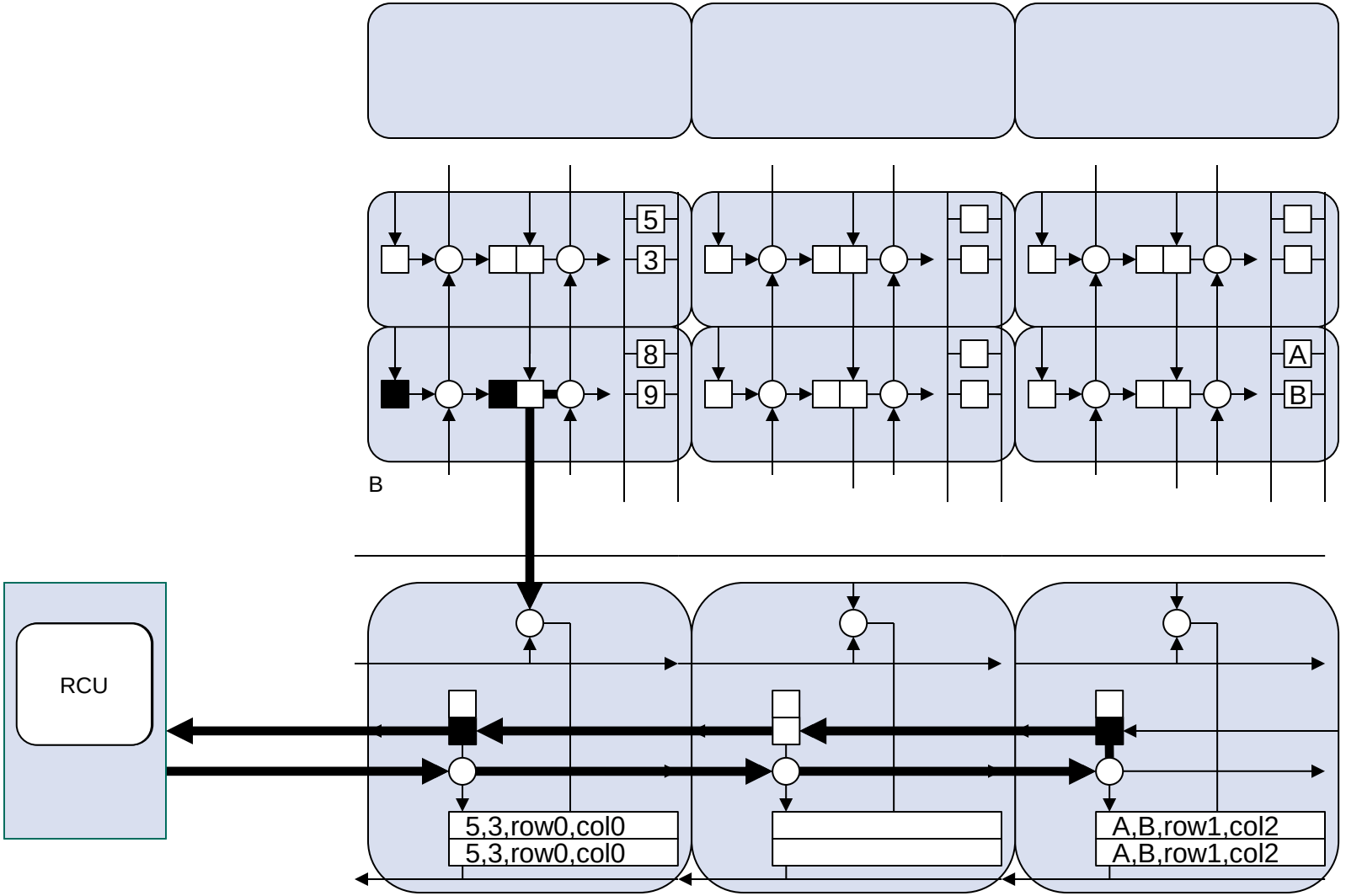
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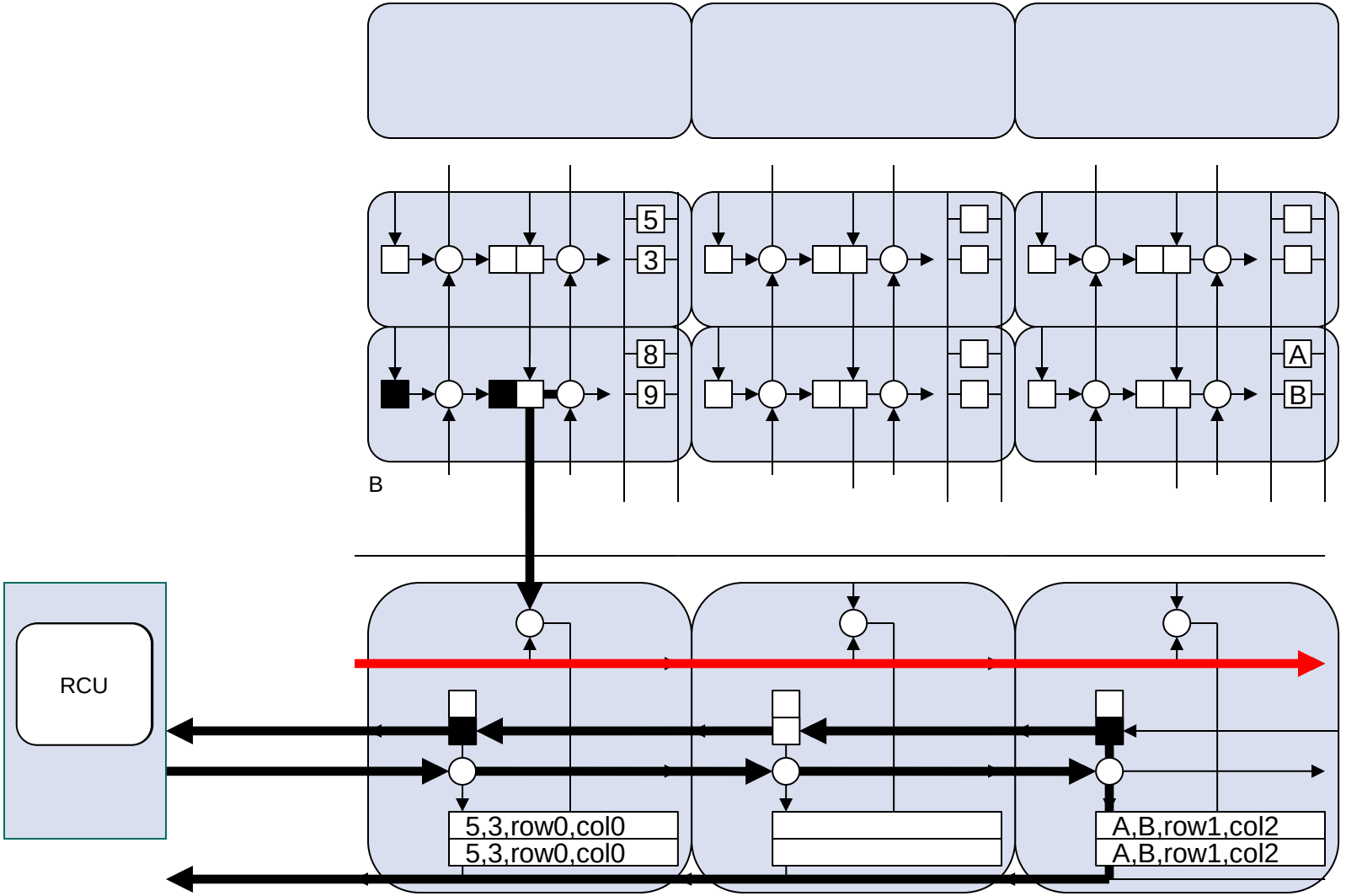

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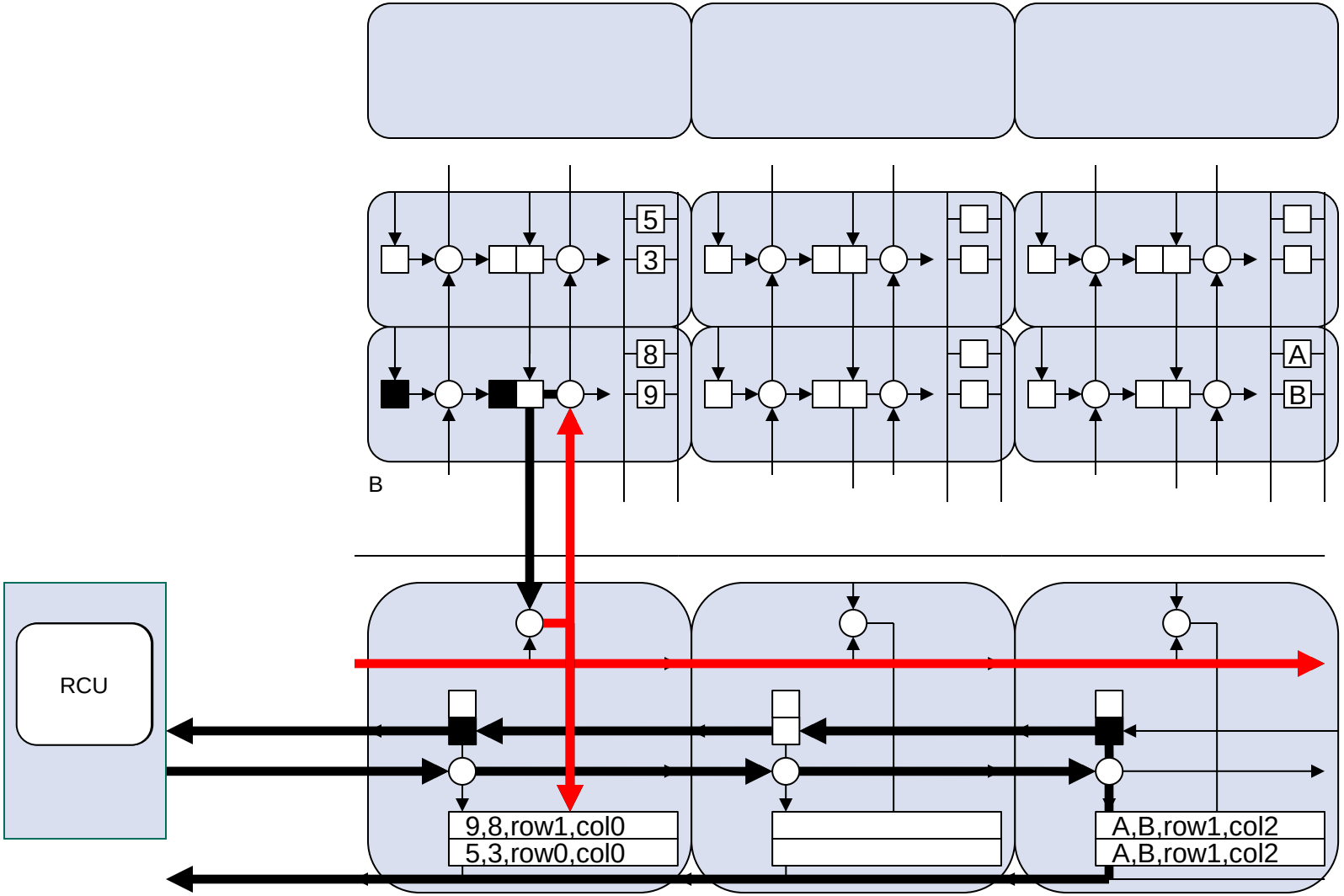

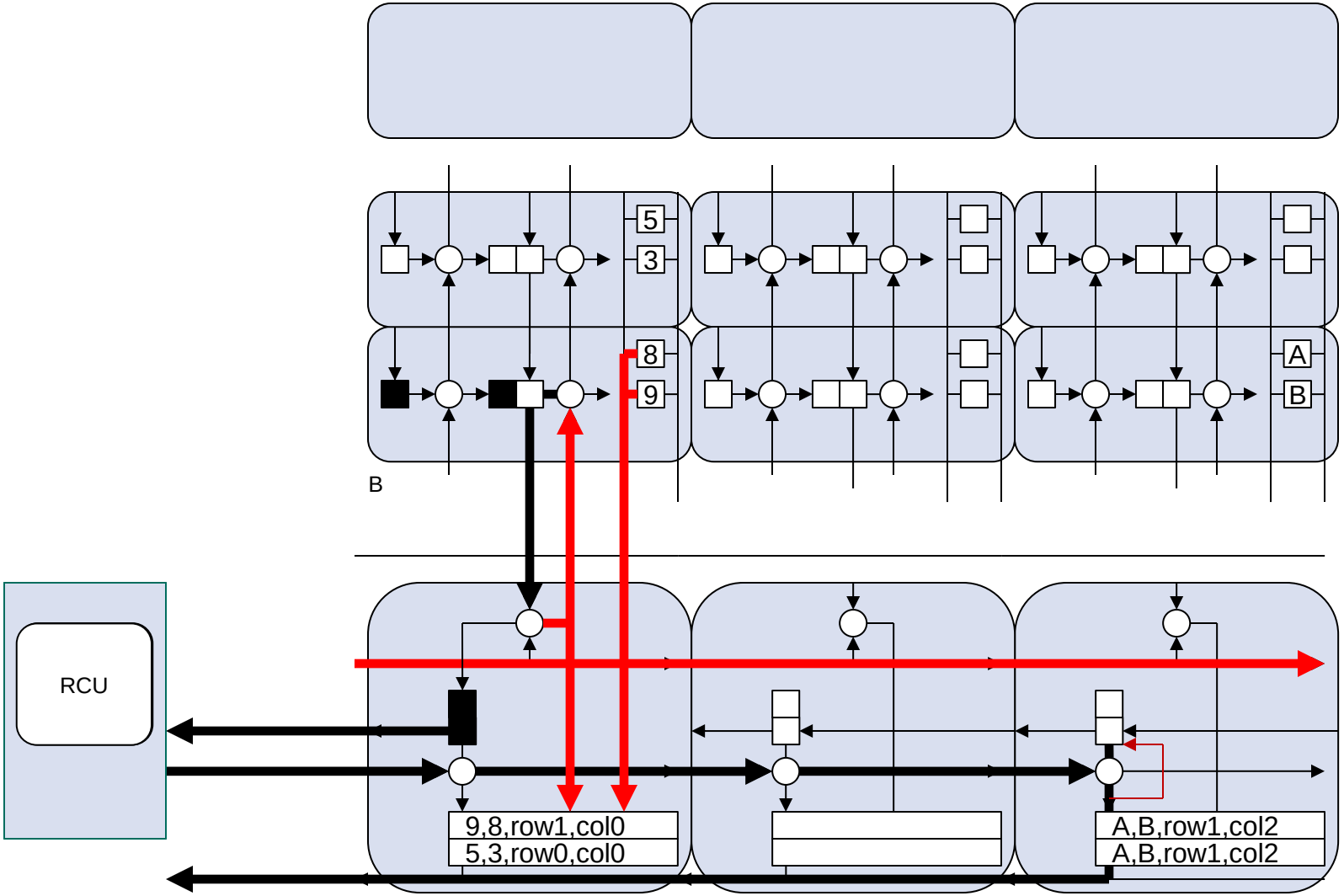
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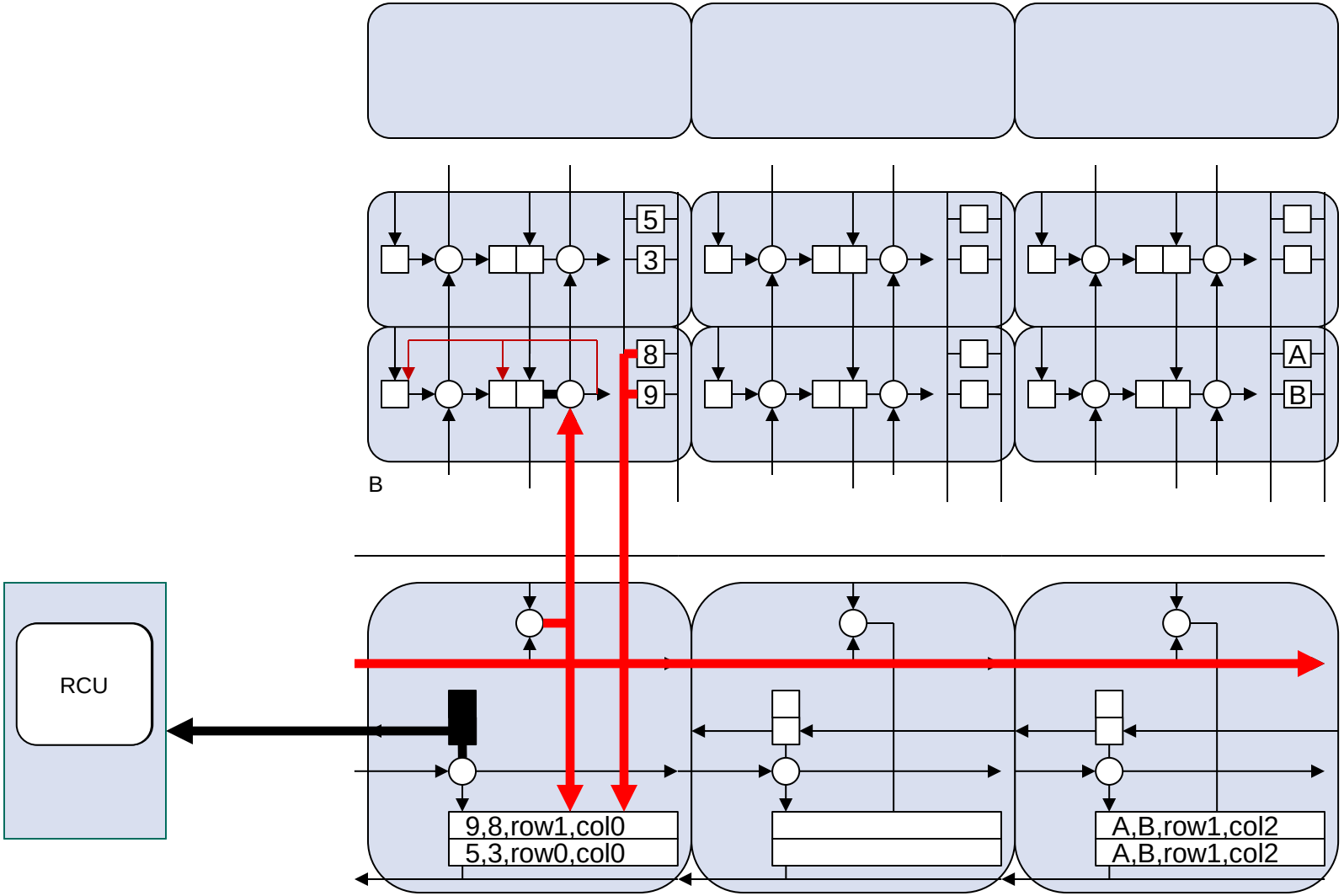
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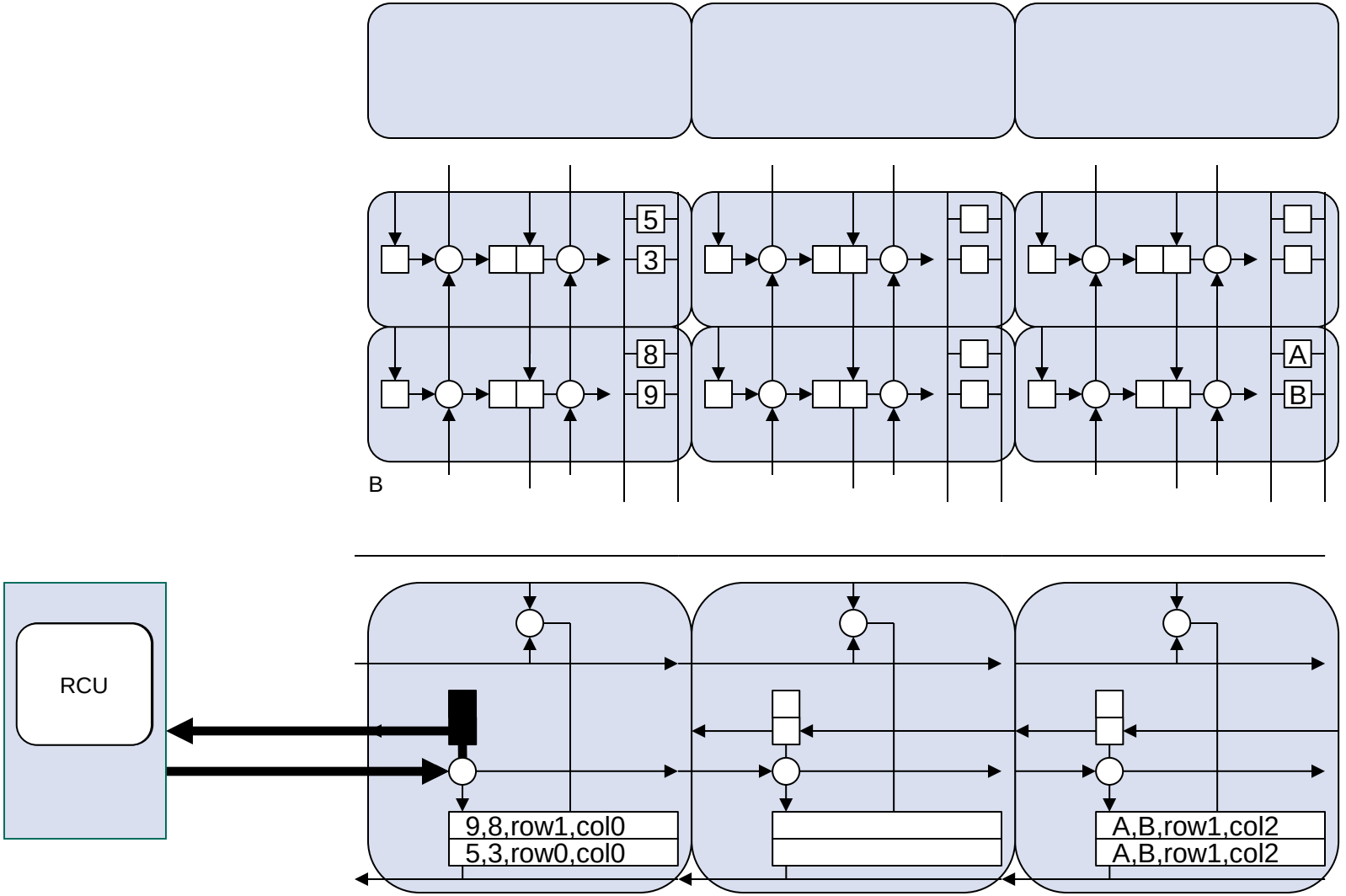
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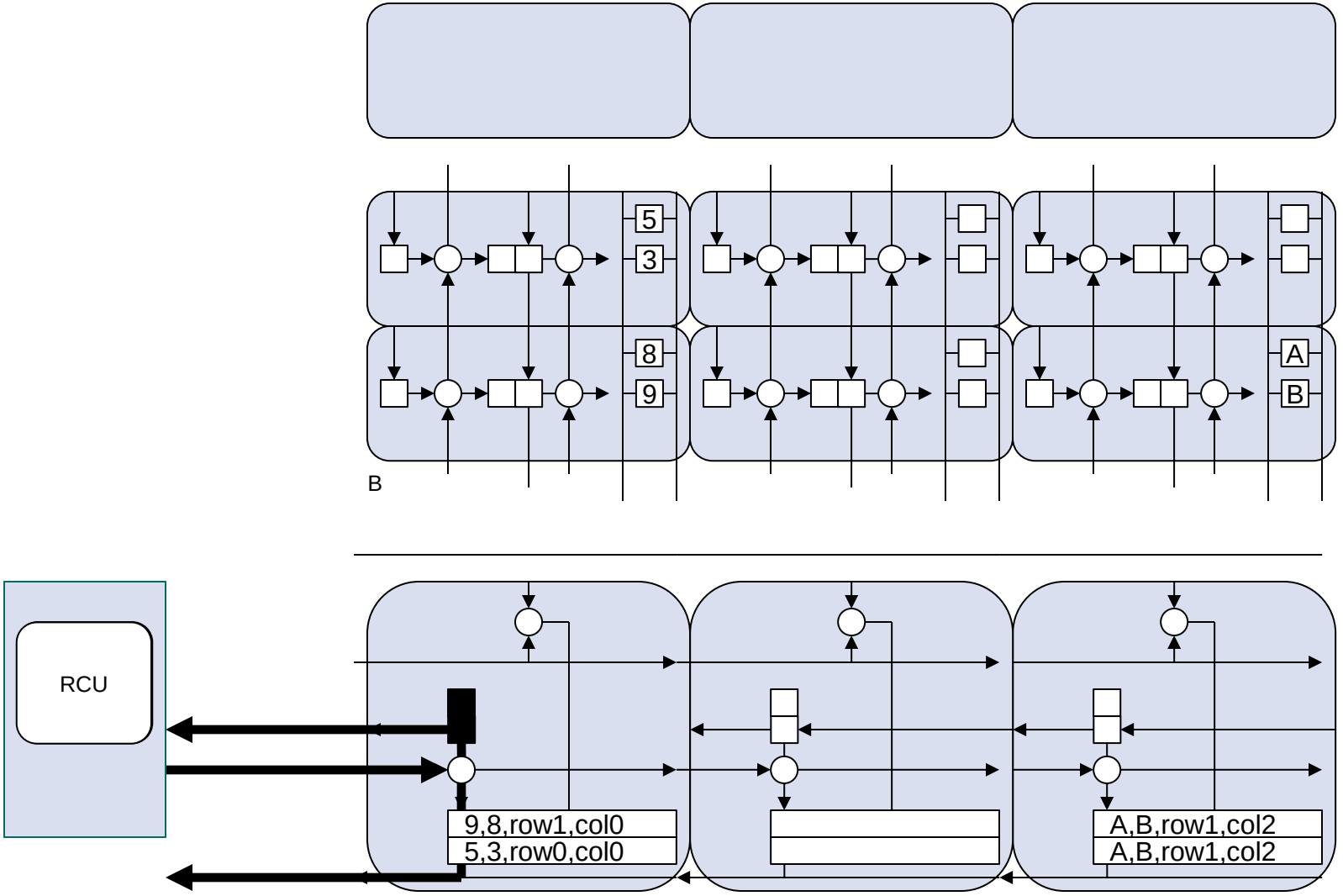
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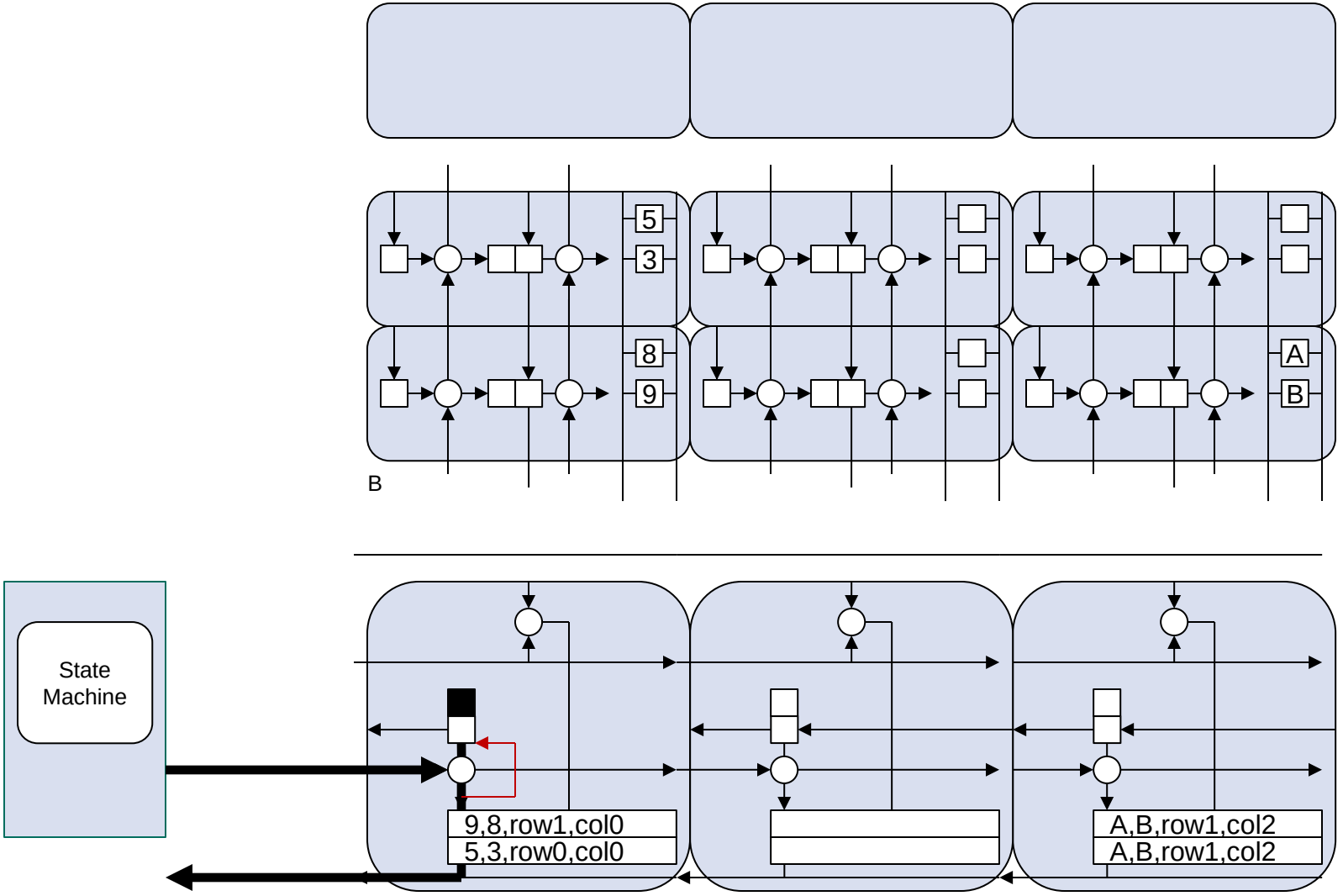
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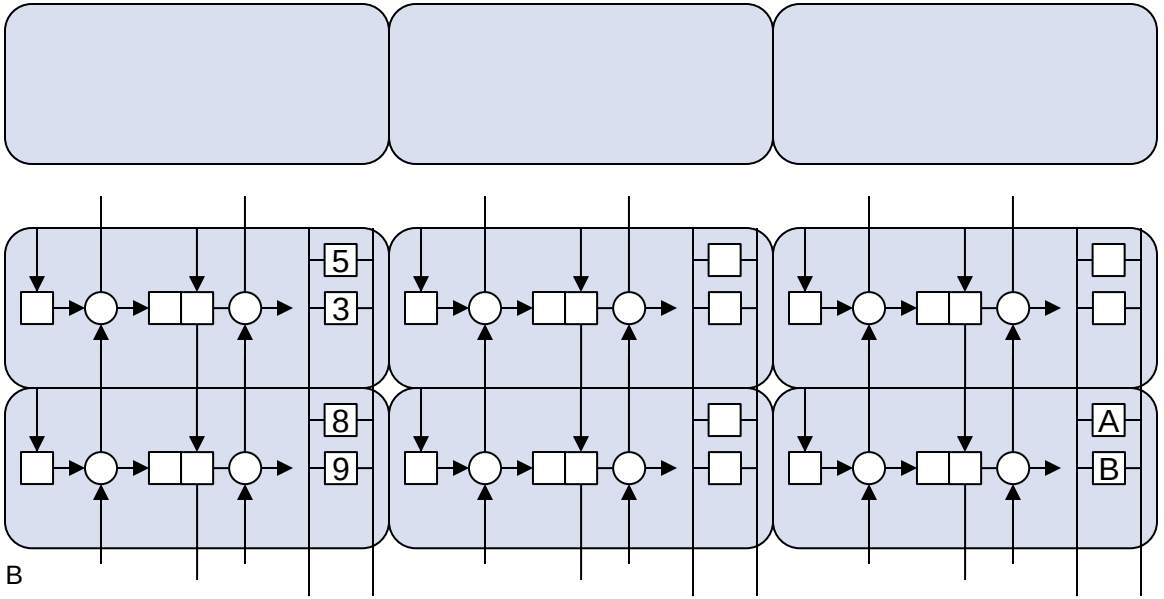

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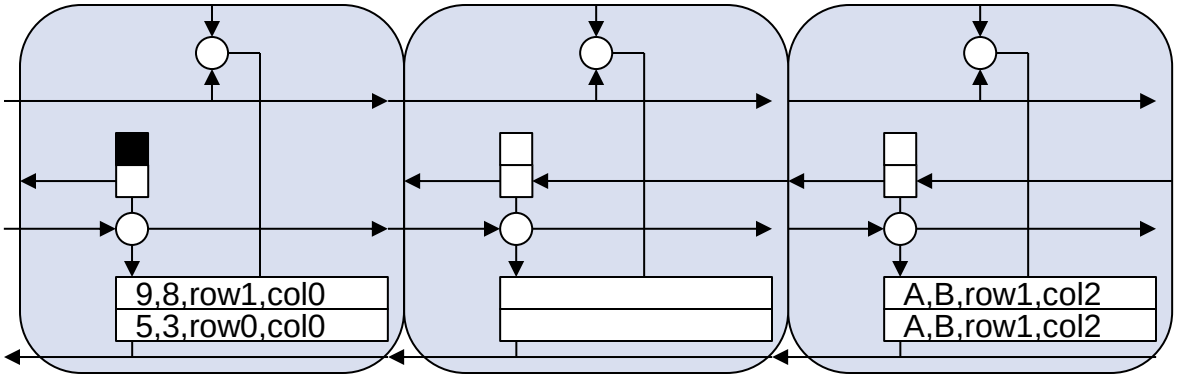

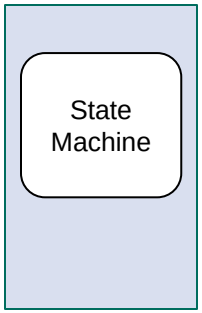
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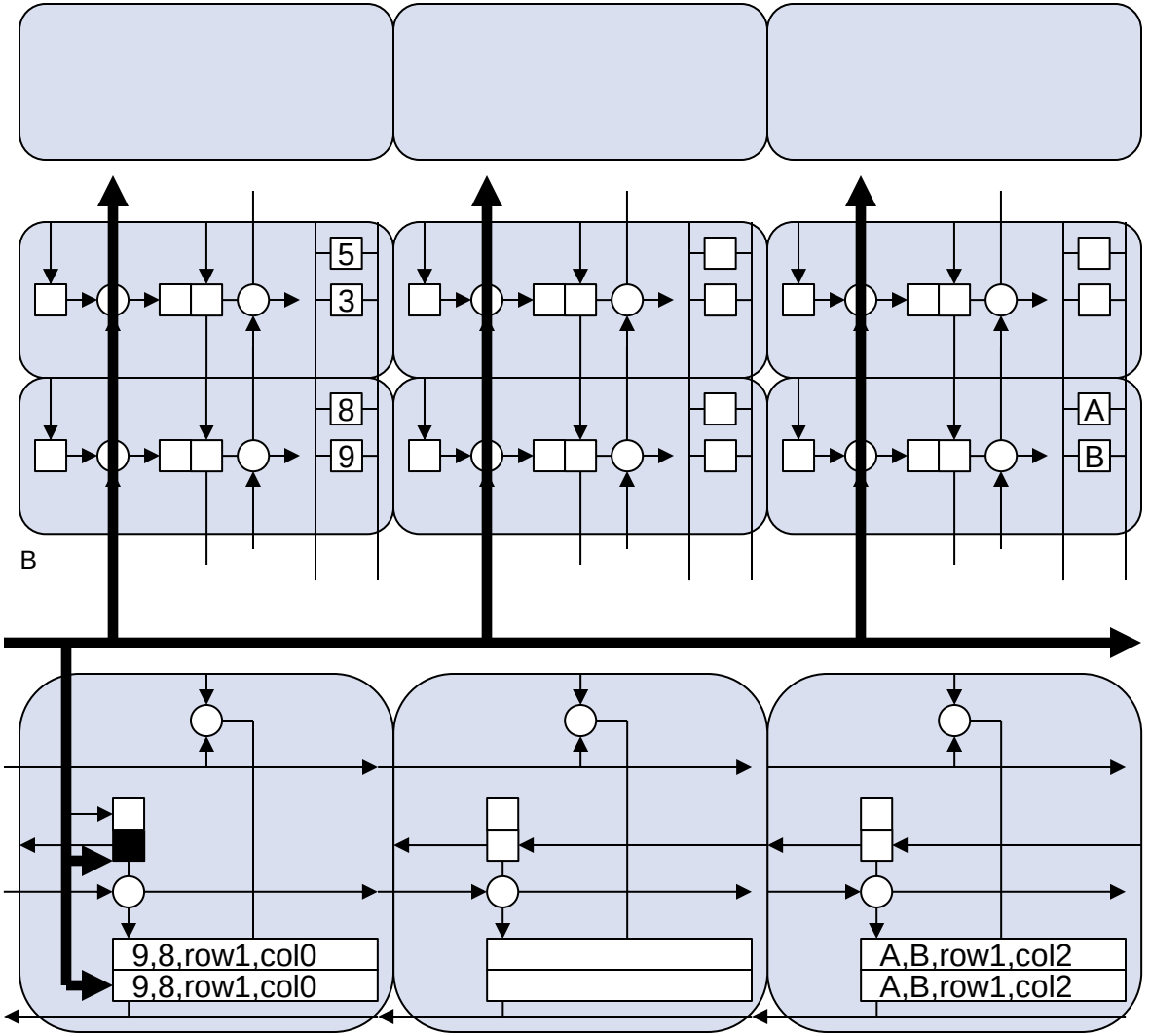
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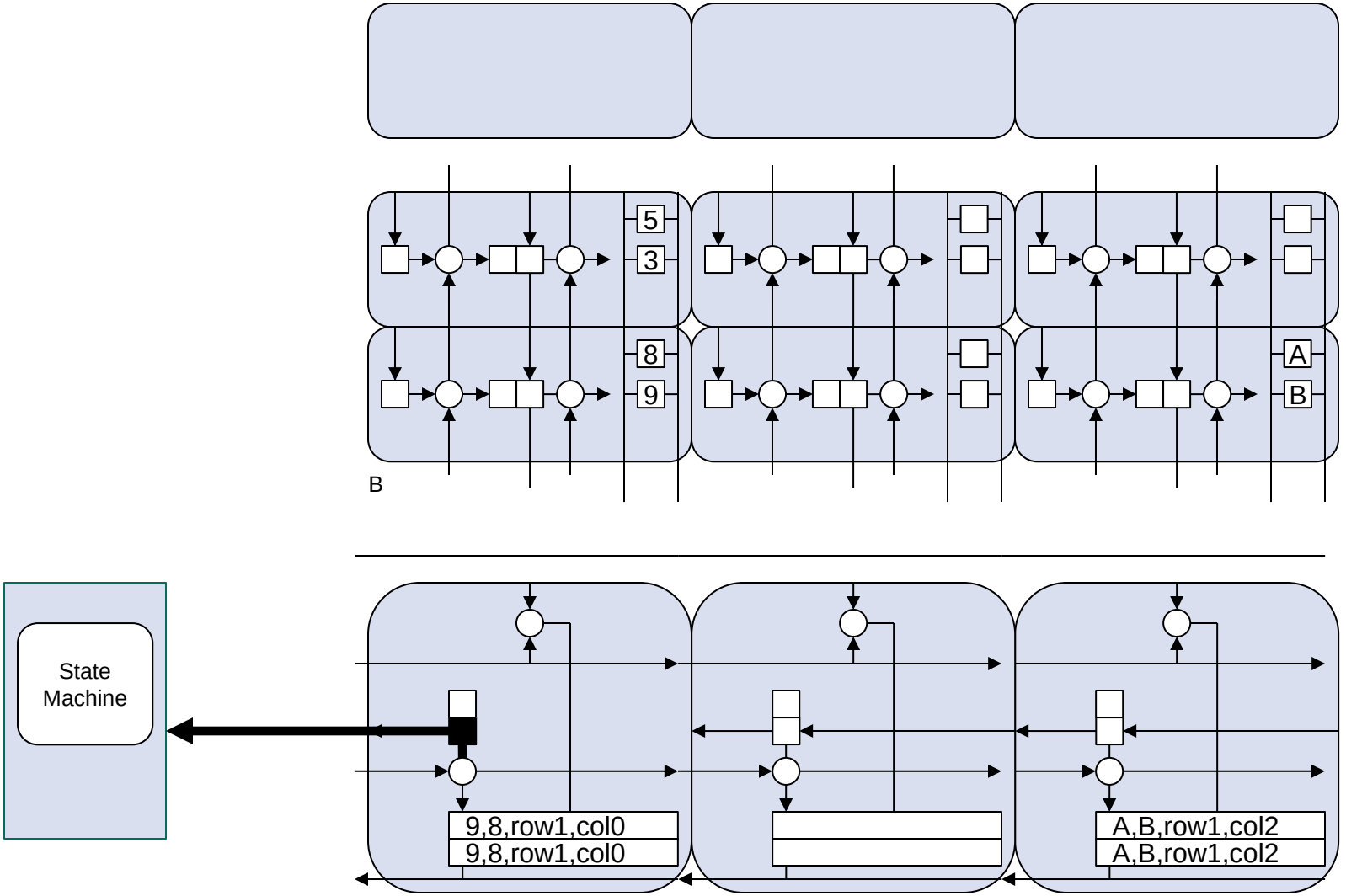
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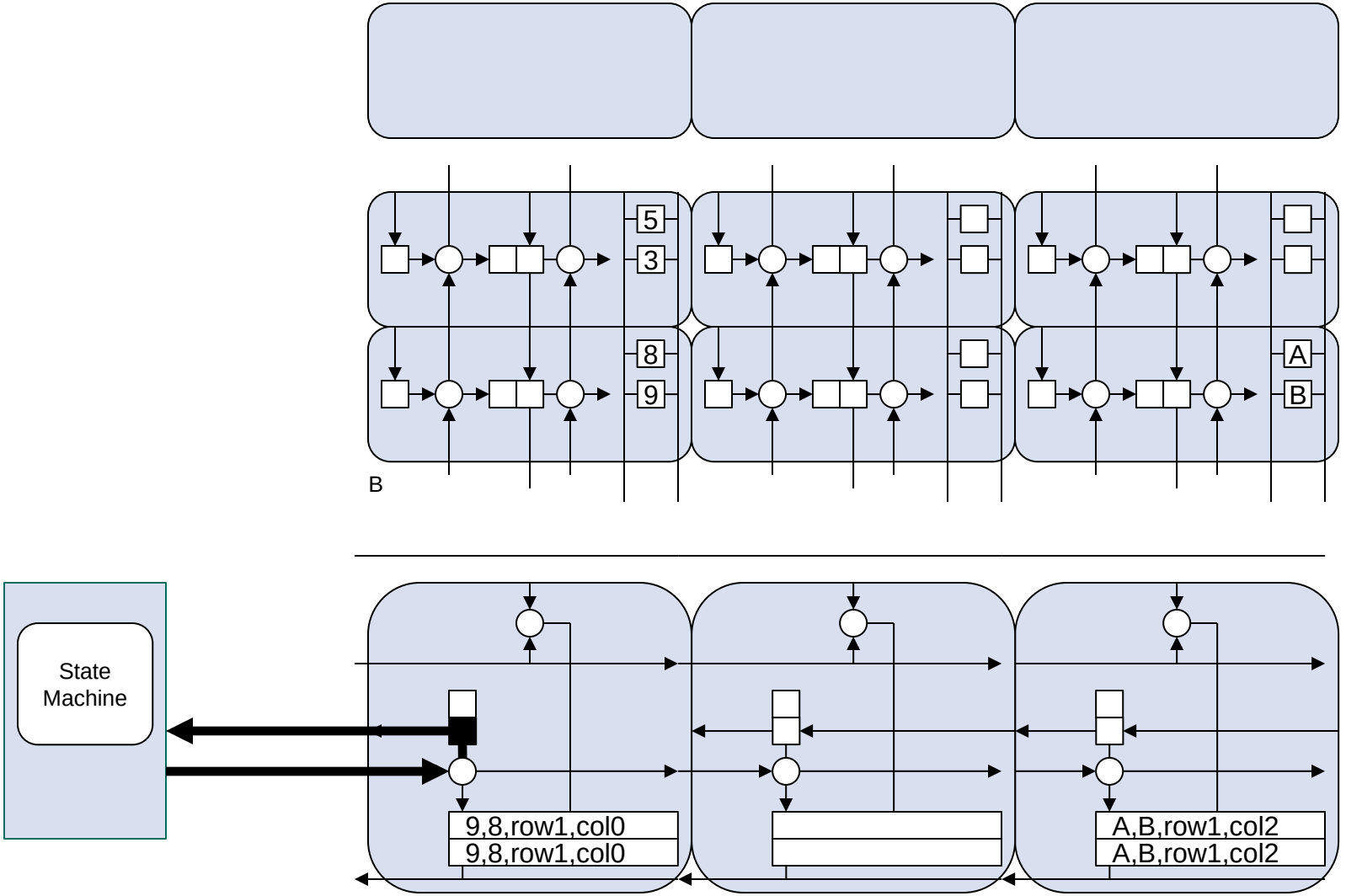
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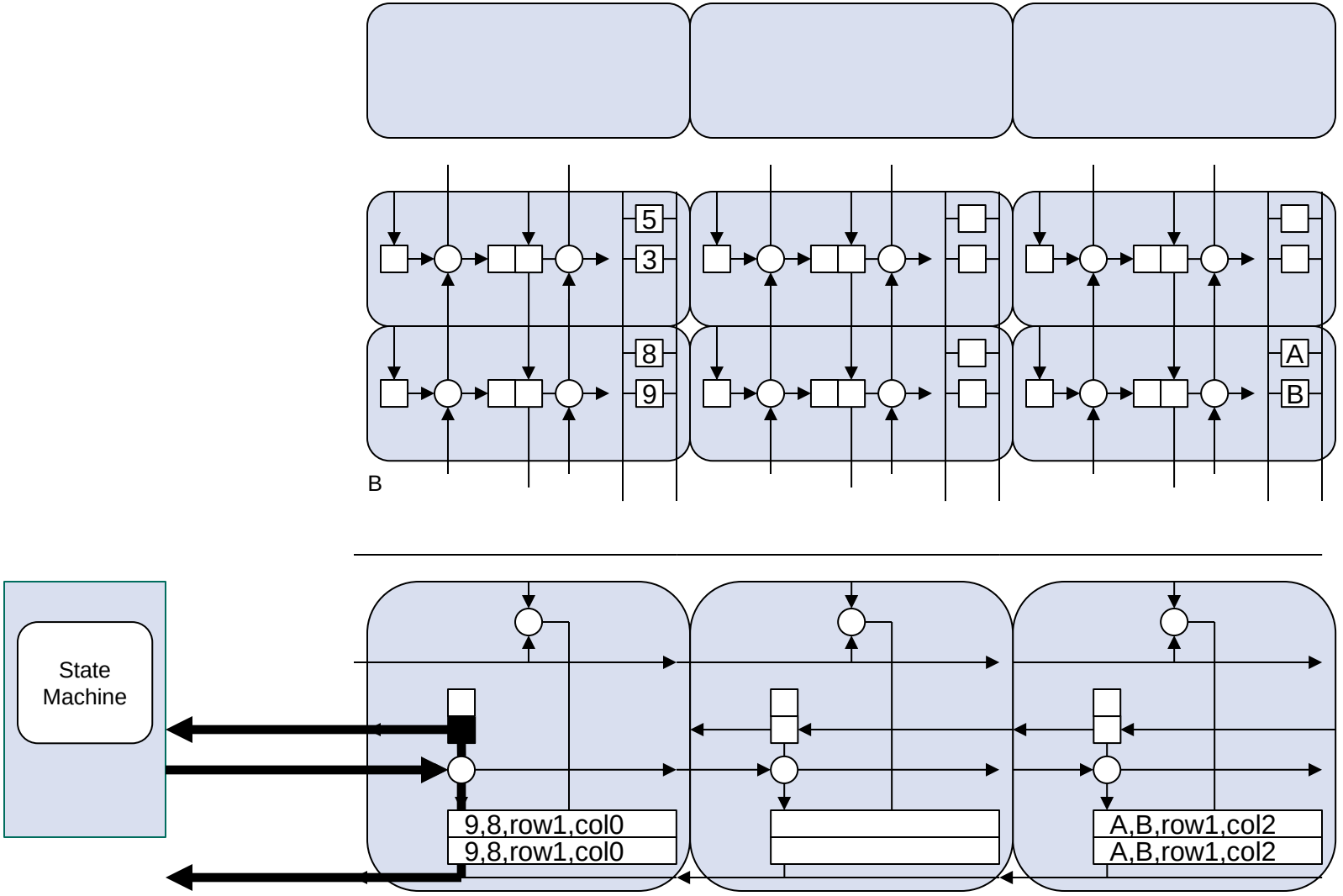
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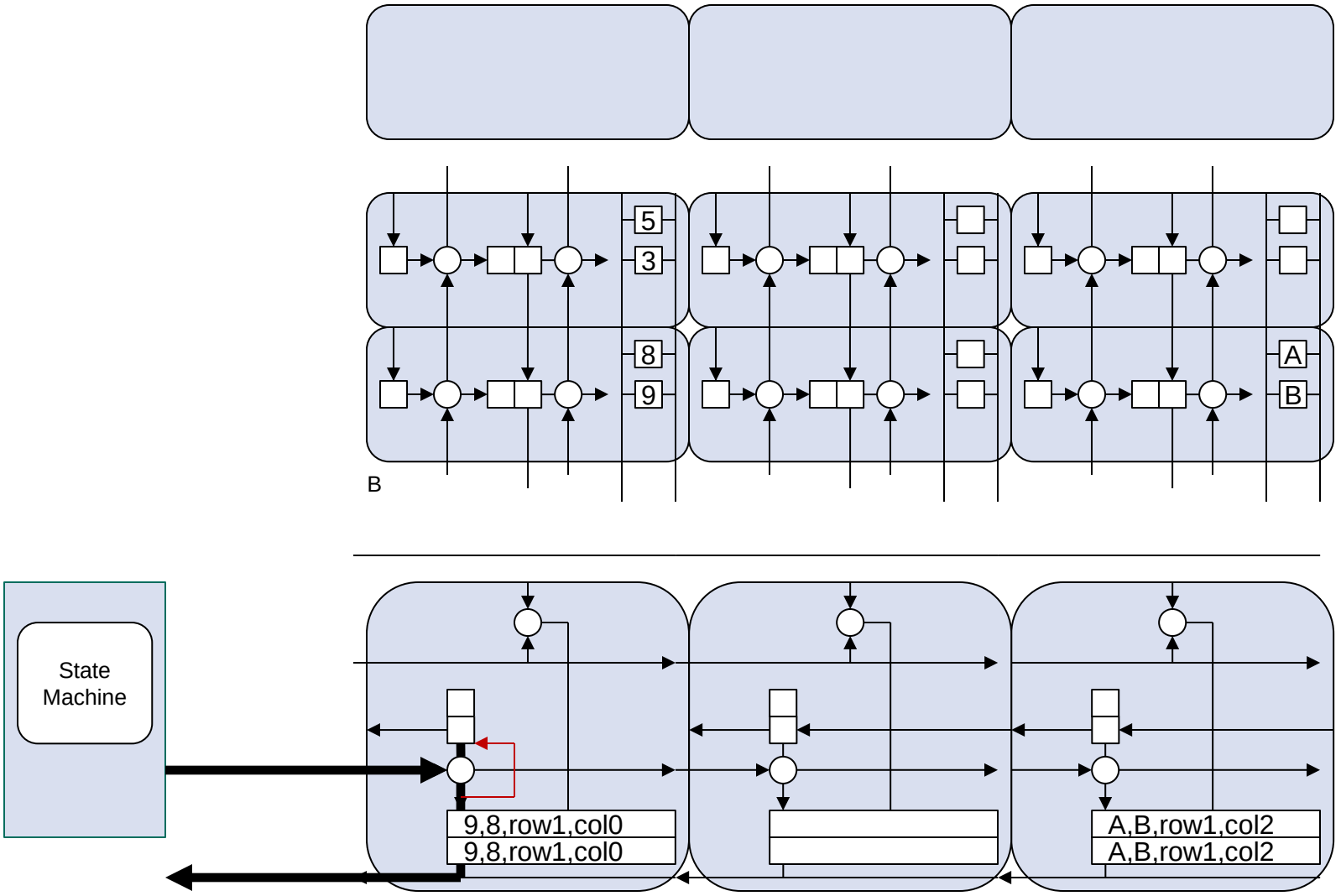
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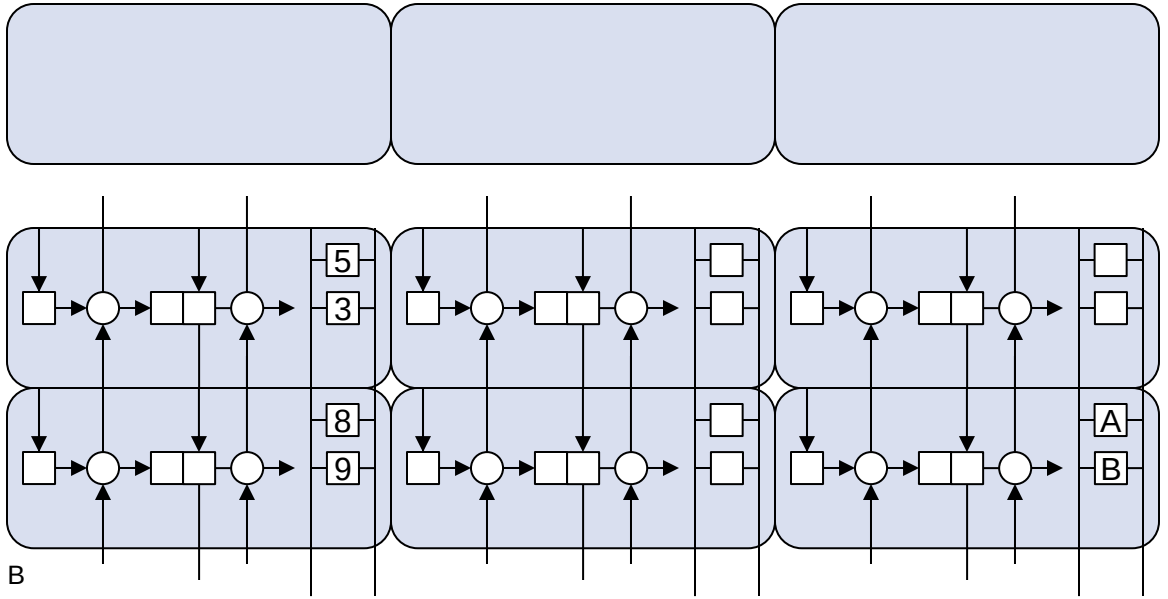

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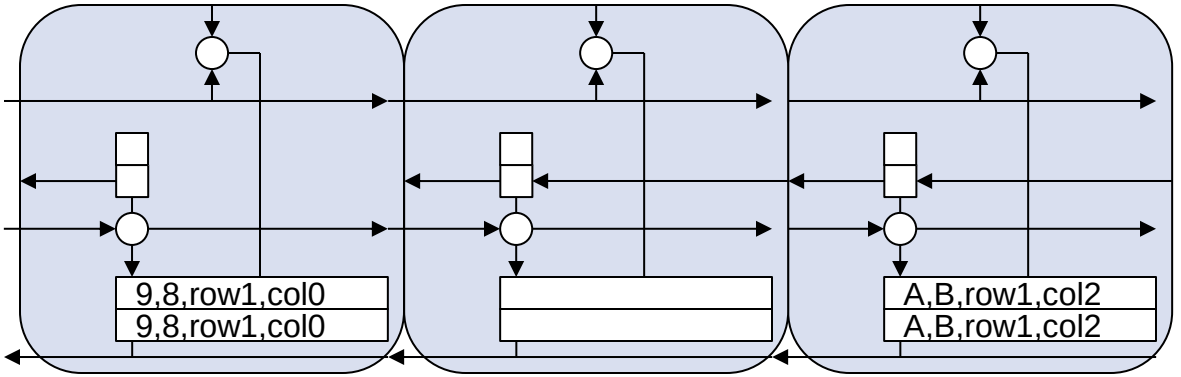

Readout Control Unit (RCU)

- **Readout Control Unit (RCU)**
- Main digital readout block
- Contains:
  - Readout FSMs
  - Asynchronous FIFOs
  - Readout multiplexer
  - Round-robin arbiter
  - Gearbox
  - Scrambler
  - Serializer
  - DDR output stage
- **Slow Control Interfaces**
- Used for:
  - Chip configuration
  - Monitoring
  - Status register readback
  - On-chip ADC readout
- Main interface:
  - ECS downlink
  - 10 Mbps serial link
  - 8b/10b encoded

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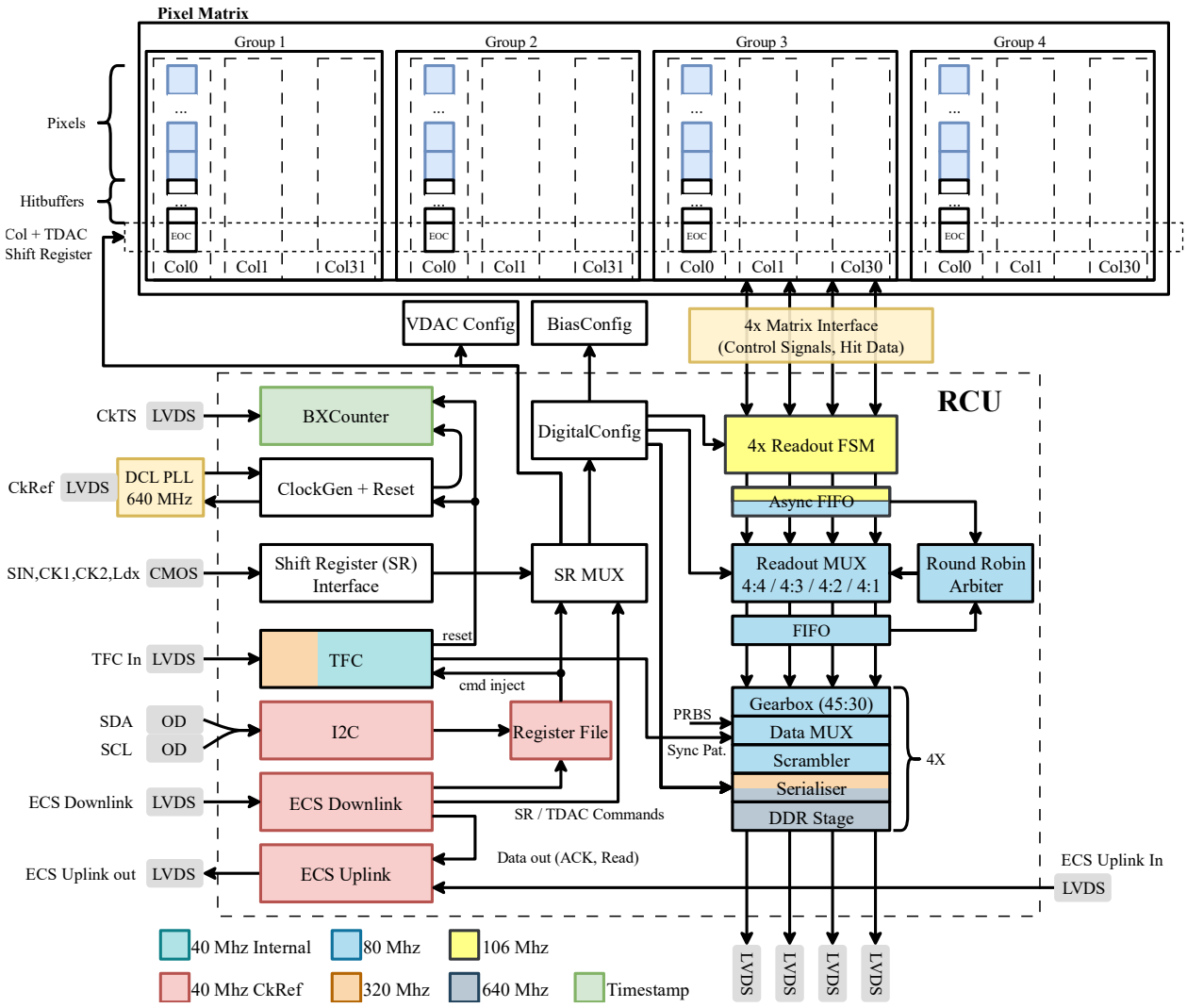
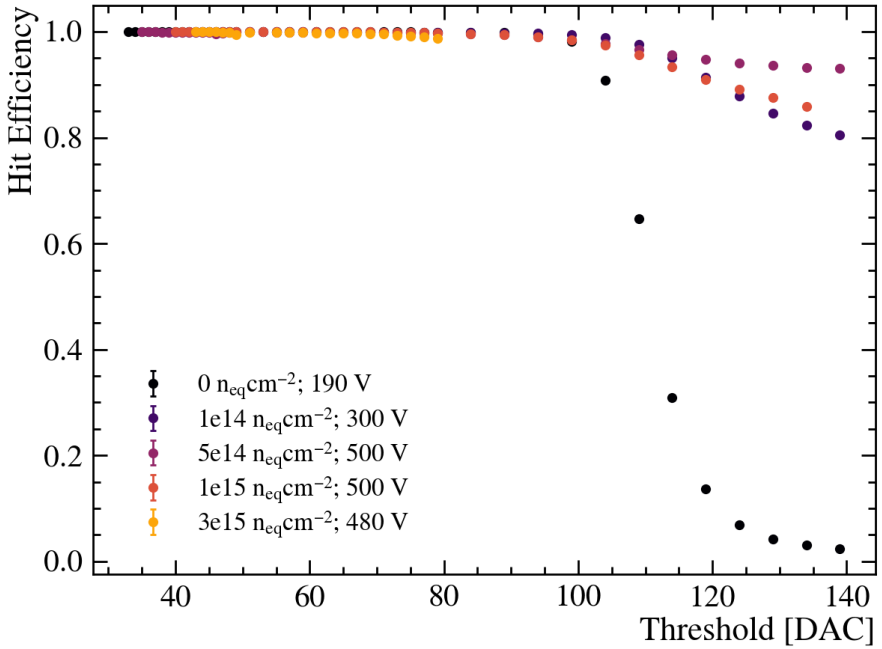


- **Test Results**
- Measured prototypes:
  - MightyPix1
  - LF-MightyPix
- Focus:
  - Radiation hardness
  - Hit efficiency
  - Timing performance

- **DESY Test Beam**
- Measurements performed after irradiation
- Scans:
  - Threshold scans
  - Bias voltage scans
- Conditions:
  - Up to 3×10^{15} neq/cm^2
  - High-voltage operation up to 480 V

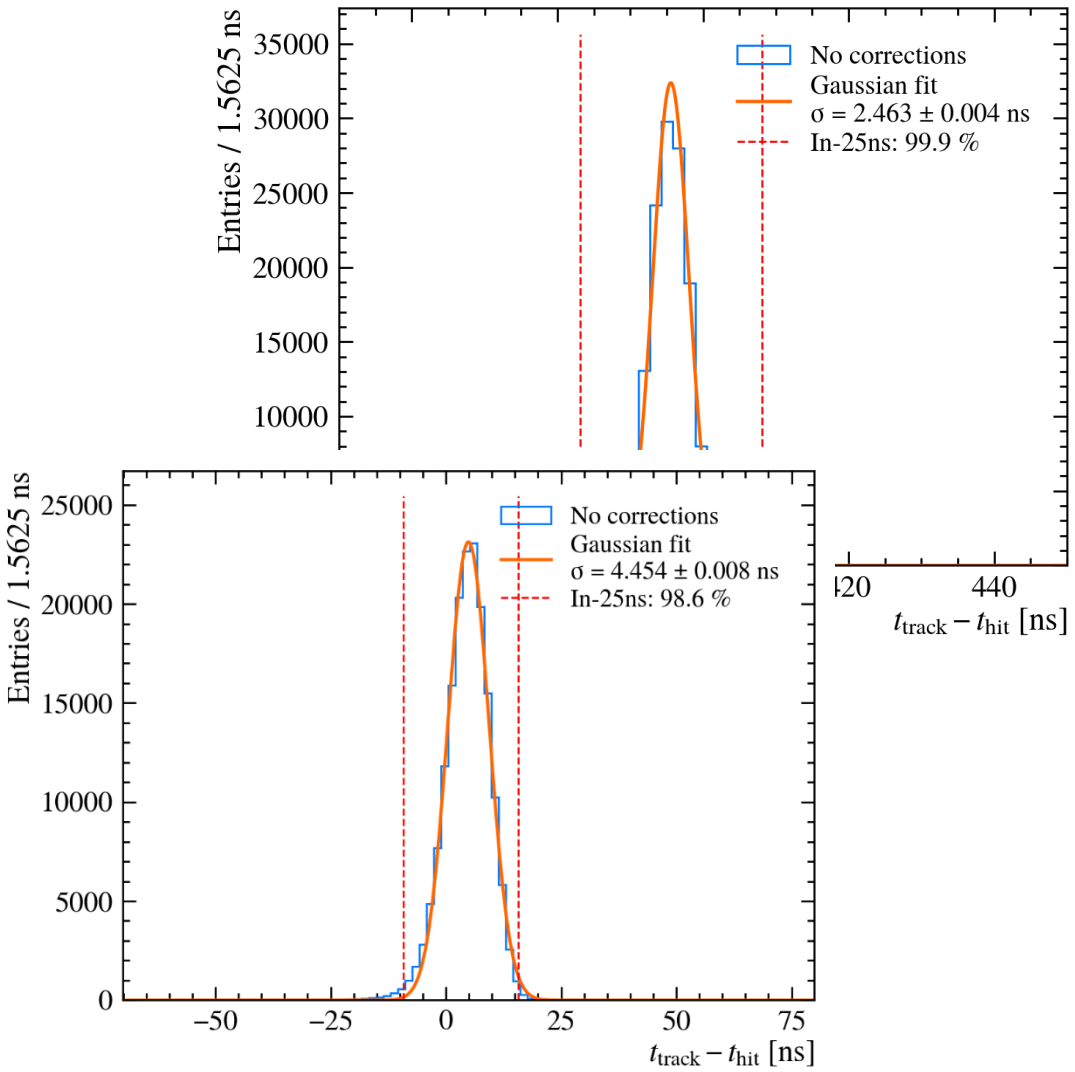
- **Radiation Hardness**
- LF-MightyPix achieves:
  - 99% hit efficiency
  - up to 3 × 10^{15} neq/cm²
- Operation voltage:
  - up to 480 V



Measurements: Lucas Dittmann (U. Heidelberg)

- **Timing Resolution**
- Without timewalk correction:
- ~2.5 ns
  - up to 1 × 10¹⁵ neq/cm²
- ~4.5 ns
  - at 3 × 10¹⁵ neq/cm²

- **In-Time Efficiency**
- LHCb requirement:
- 99% within 25 ns
- Measured:
- fulfilled up to 1 × 10¹⁵ neq/cm²
- 98.6% at 3 × 10¹⁵ neq/cm²



Measurements: Lucas Dittmann (U. Heidelberg)

- **Conclusion**
- MightyPix demonstrates:
  - high-rate capability
  - fast timing
  - strong radiation hardness
- HV-CMOS is a strong candidate for:
  - LHCb Mighty Tracker
- Next steps:
- MightyPix2 measurements
- MightyPix3 development