Analog front-end channels in 28nm CMOS for HEP and photon science

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XIII Front-End Electronics Workshop

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Outline

- Introduction

- Radiation effects on a 28 nm CMOS technology

- Front-end channels for HEP
    - Flash-ADC based front-end
    - Time-over-Threshold based front-end

- A proof-of-concept front-end for photon science

- Conclusions

Bergamo/Pavia activities with 28 nm CMOS

- Since 2021 the group is working with the 28 nm CMOS technology (3 mini@sic chip submitted)

Falaphel

Development and integration of **Silicon Photonics** modulators with high speed, rad-hard **electronics in 28 nm**

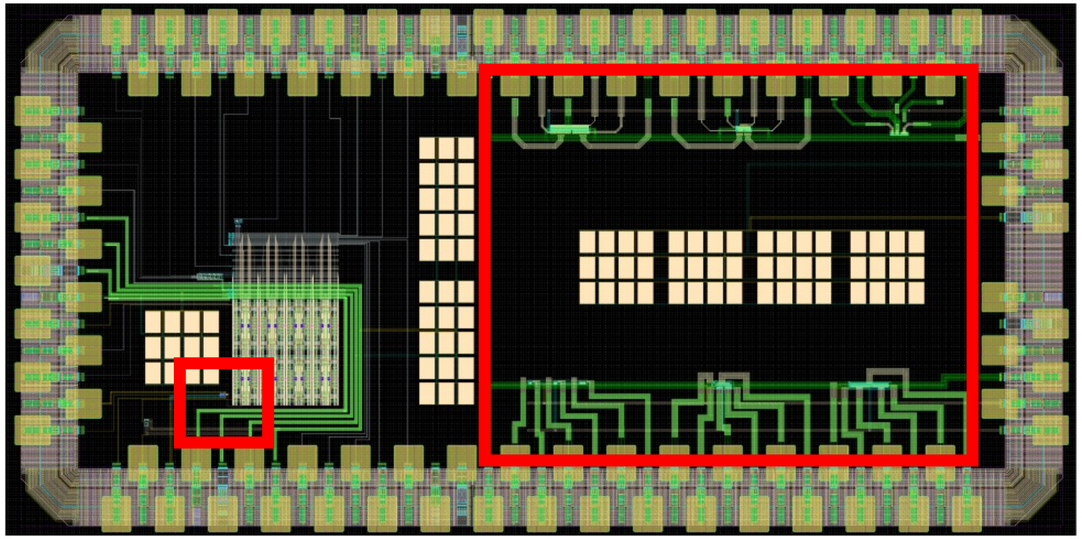
  - INFN Padova, Pavia, Pisa, Scuola Superiore S. Anna di Pisa, UniPisa, UniMilano. (P.I. Fabrizio Palla)

PiHEX
PRIN 2022

Development of **front-end channels in a 28 nm CMOS process** for Pixel detectors in future High Energy physics colliders and advanced X-ray imaging instrumentation

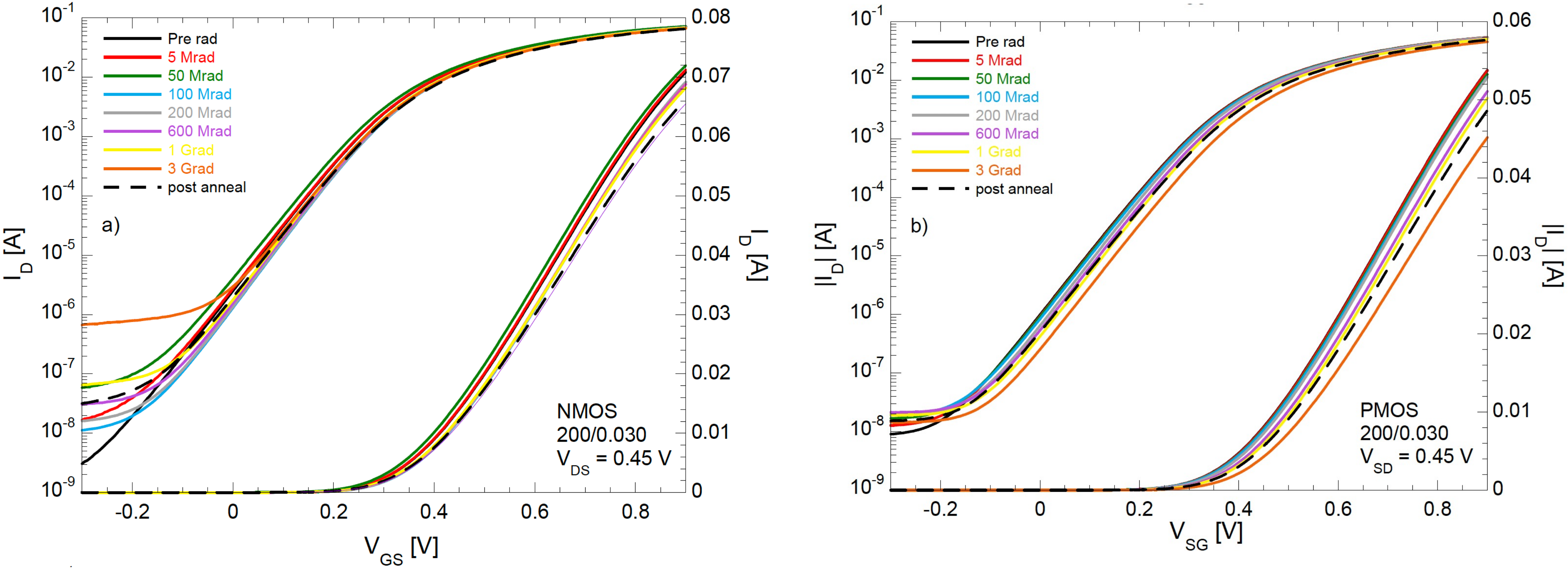
  - University of Bergamo and University of Padova (P.I. Luigi Gaioni)

Radiation effects on a 28 nm CMOS technology



- **First submitted chip includes:**
  - **standalone NMOS and PMOS** transistors for static and noise characterization
  - **a standalone charge sensitive amplifier (CSA)** for the evaluation of main analog performance parameters
- **Technology features**
  - High Performance Computing (HPC+) flavour
  - V_{DD} = 0.9 V
- **Investigated devices**
  - Standard Vth NMOS and PMOS (W = 100, 200, 600 µm / L = 30, 60, 180 nm)
  - Standard open structure interdigitated layout (W_F = 2.5 µm)
- **Irradiation conditions**
  - X-ray machine with an average energy of 10 keV
  - TID up to 3 Grad - dose rate of 1.5 krad/s
  - Irradiation at room temperature

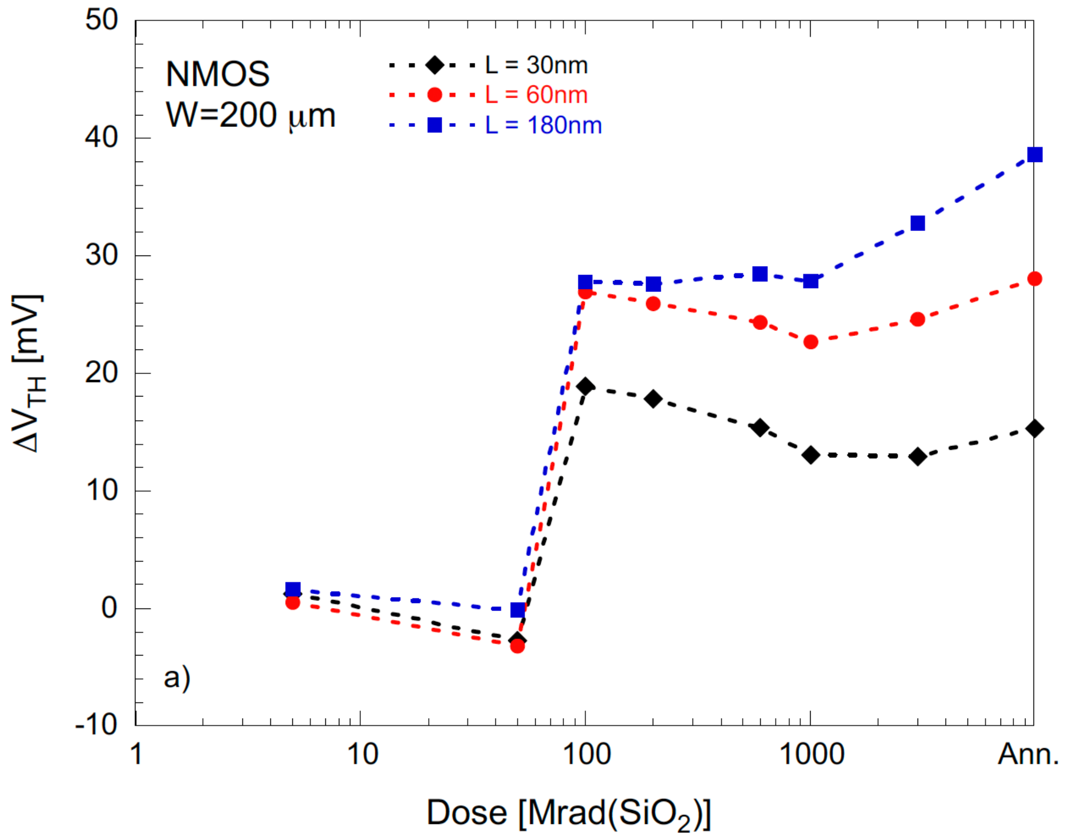
Static characteristics

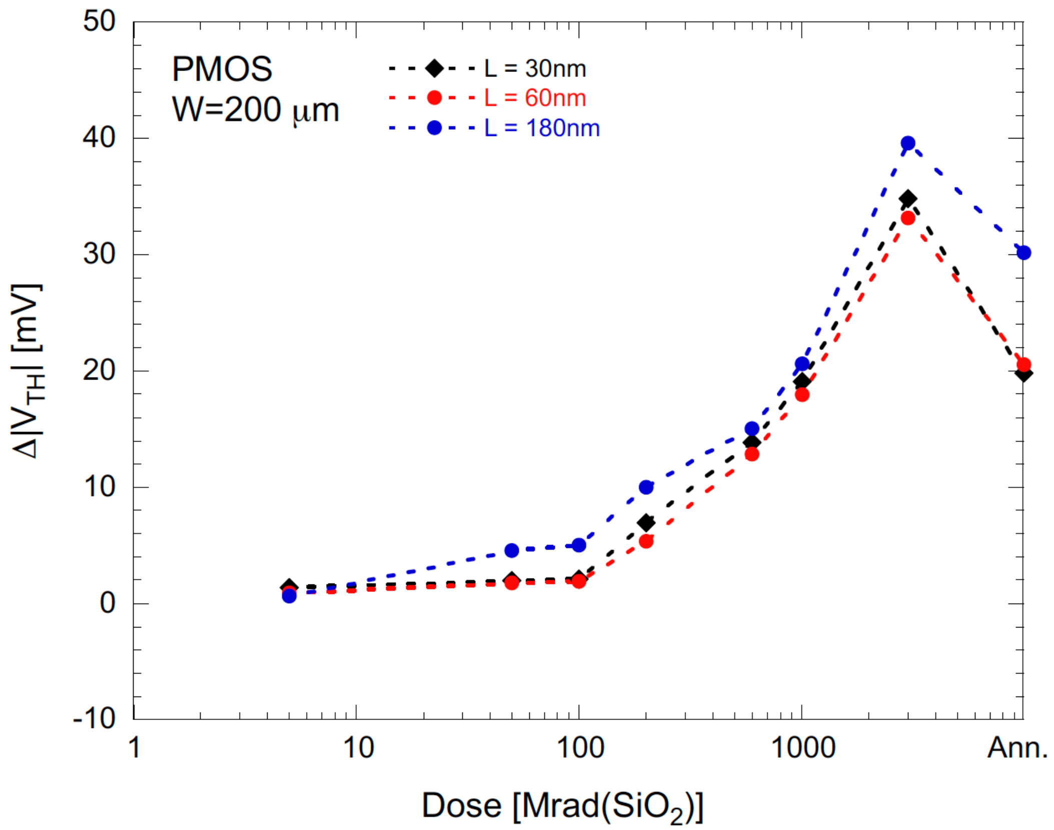


- Moderate **increase in drain leakage** current after irradiation for **NMOS** (significant **recover** after annealing)
- **Limited increase** in **PMOS** leakage current but more affected at maximum drive current

G. Traversi et al., **Ionizing Radiation Effects of 3 Grad TID on Analog and Noise Performance of 28nm CMOS Technology**, IEEE Transactions on Nuclear Science, 10.1109/TNS.2025.3542230

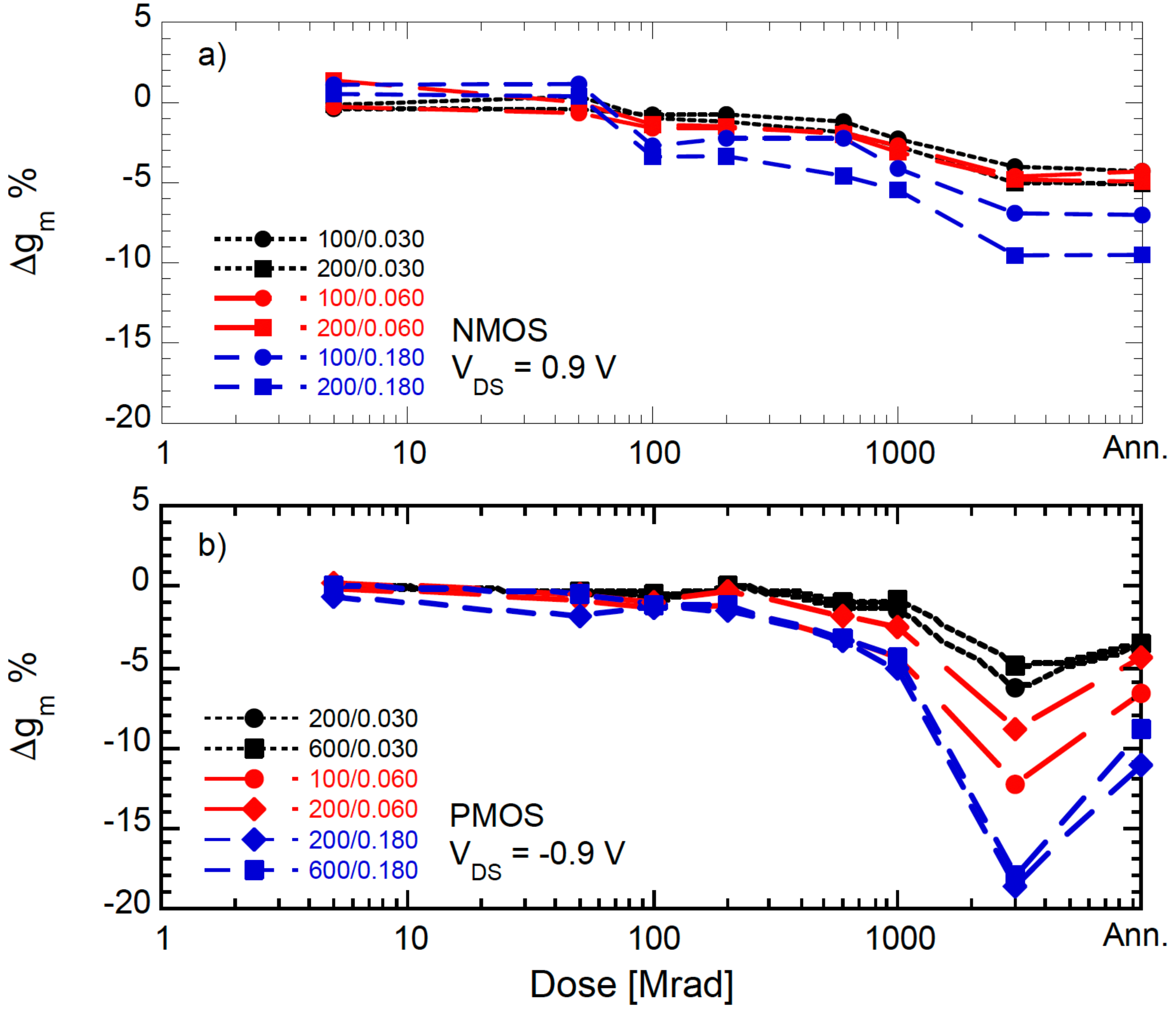
Threshold voltage





- **NMOS →** trapped charge (+) in STI decreases V_{TH} at 50 Mrad, then the interface trapped charge (-) induces a large positive shift
- 100 Mrad - 3 Grad: the effects of the charge trapped in the STI prevails for shorter devices
- **Annealing** removes the charge trapped in the oxide more than the charge trapped at the interface
- **PMOS →** monotonic variation of V_{TH} (partial recovery after annealing)

Transconductance variation

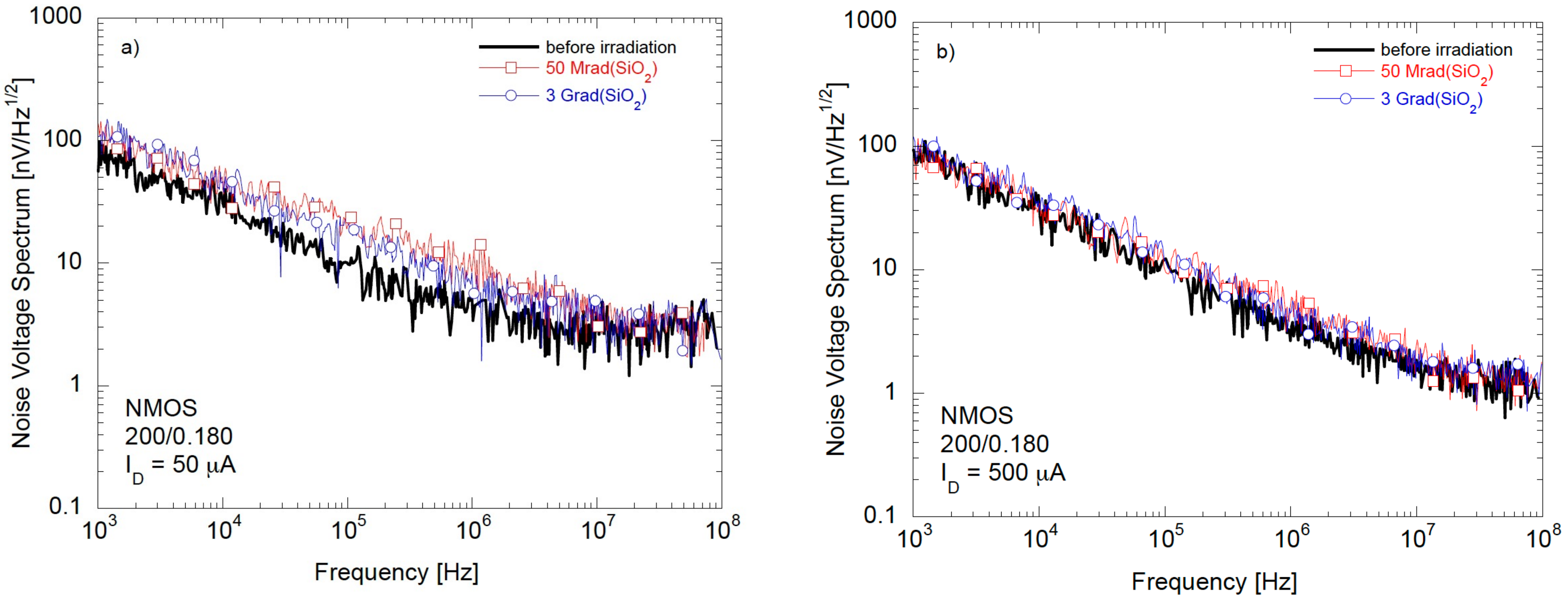


- Percentage variation of the **transconductance** as a function of the TID for NMOS and PMOS devices.

- All devices have limited transconductance degradation → less than 10% for NMOS and 20% for PMOS up to 3 Grad

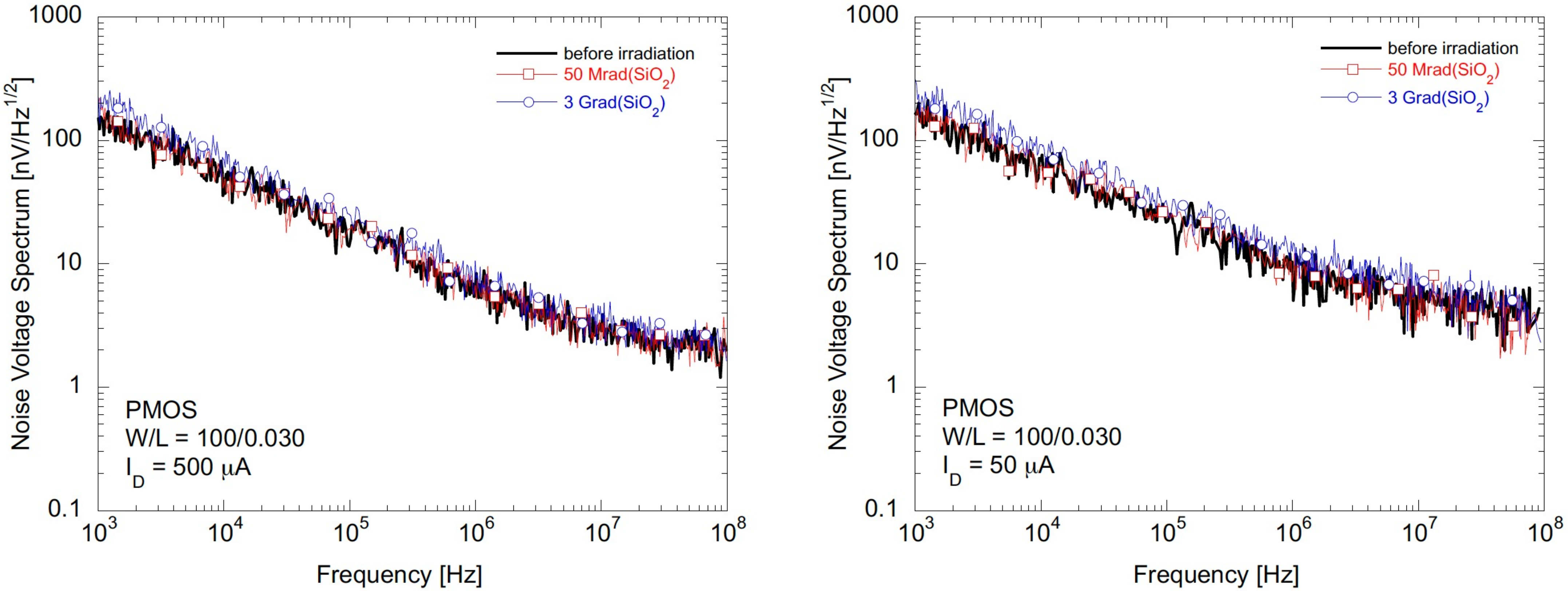
- **Shorter devices** are more radiation tolerant

Noise in NMOS devices



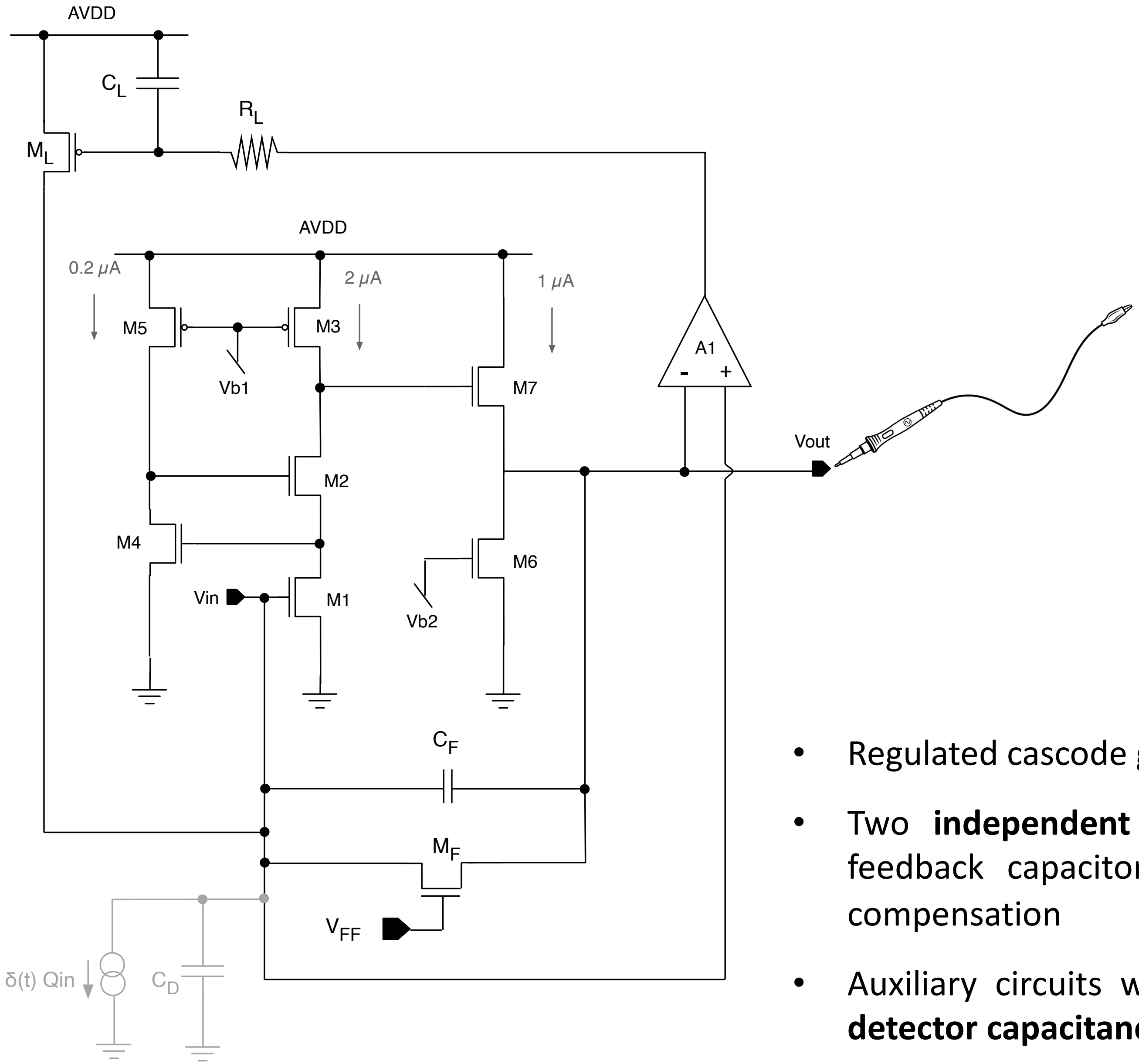
- **1/f noise** at 50 Mrad higher than at 3 Grad for low drain current density
- At **higher current density** almost no variation in the 1/f noise
- Very small variation of the **white noise**, consistent with the variation of the transconductance

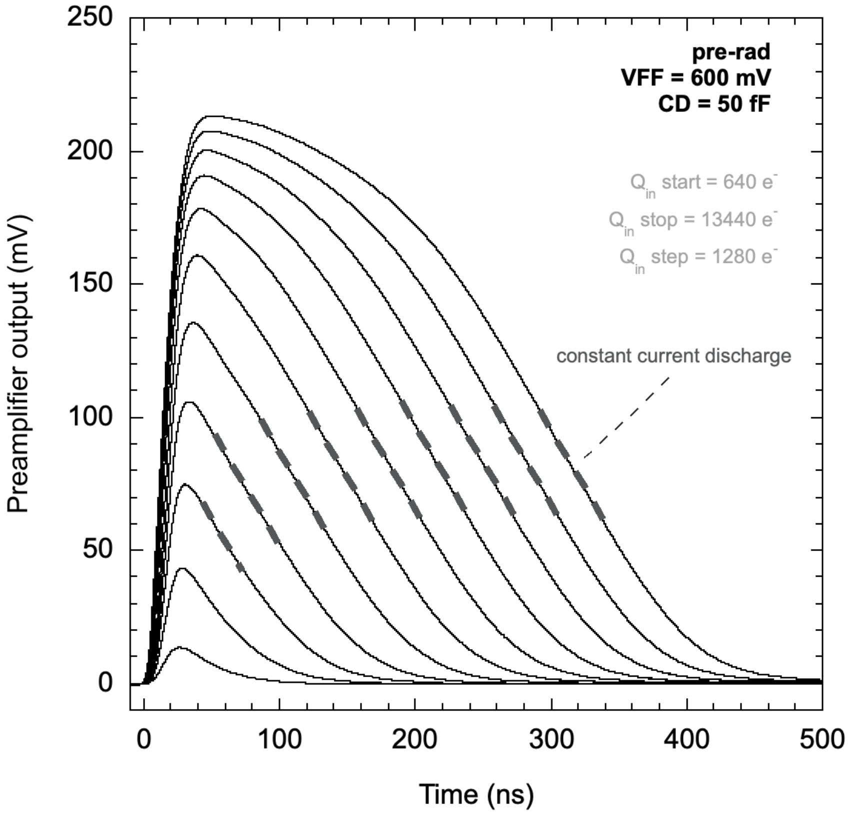
Noise in PMOS devices



- Compared to NMOS, no increase of the **1/f noise** at 50 Mrad
- Limited variation of 1/f noise **at 3 Grad**
- **High tolerance** to ionizing radiation

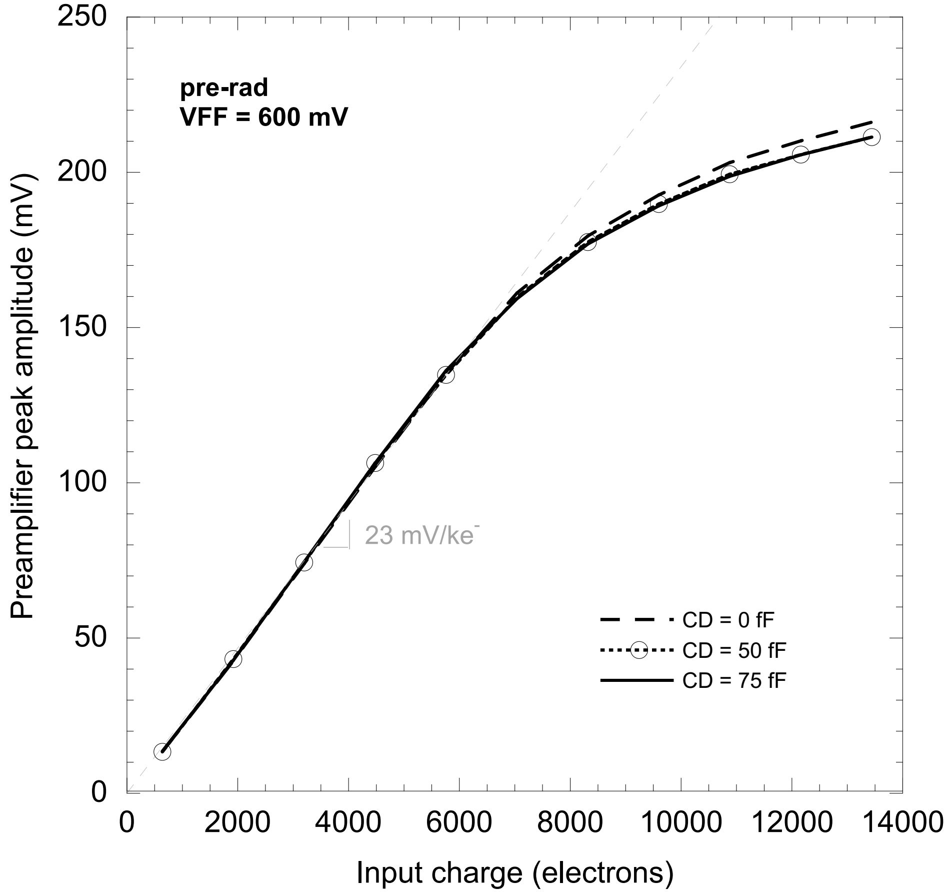
Charge sensitive amplifier design

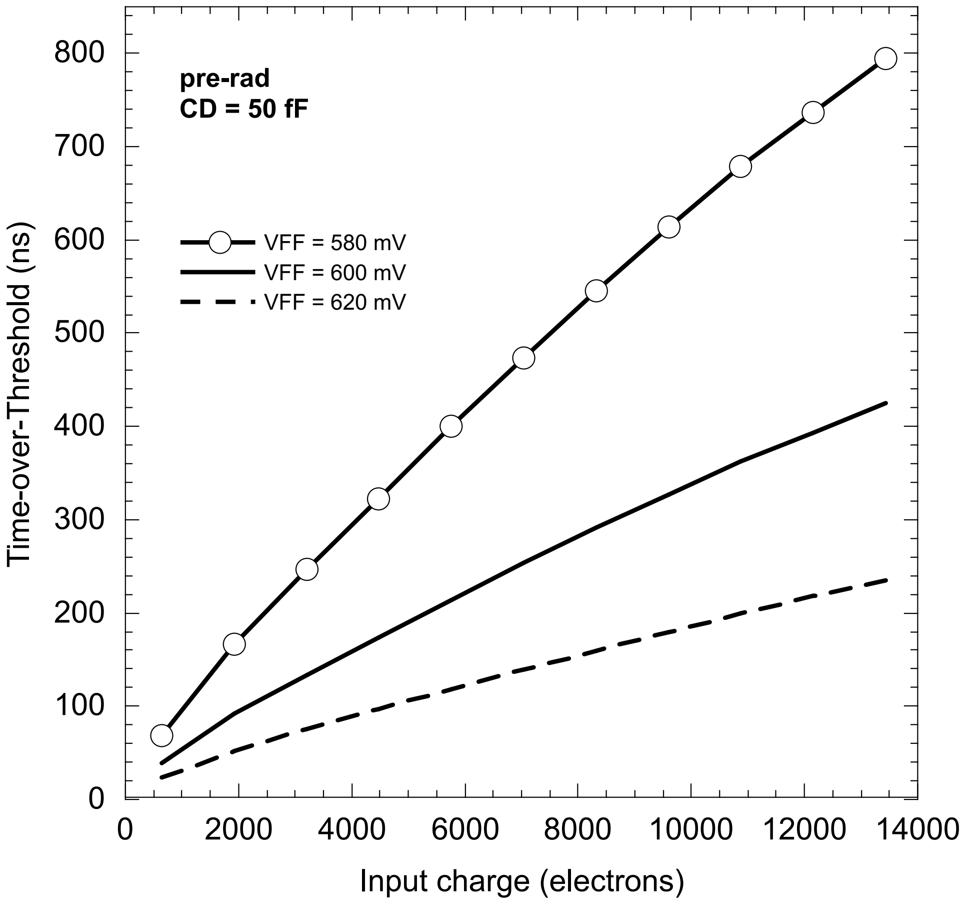




- Regulated cascode gain stage + source follower
- Two **independent feedbacks**, one for the discharge of the feedback capacitor and the other for the detector leakage compensation
- Auxiliary circuits were integrated to emulate the presence **of detector capacitance** and **leakage current**

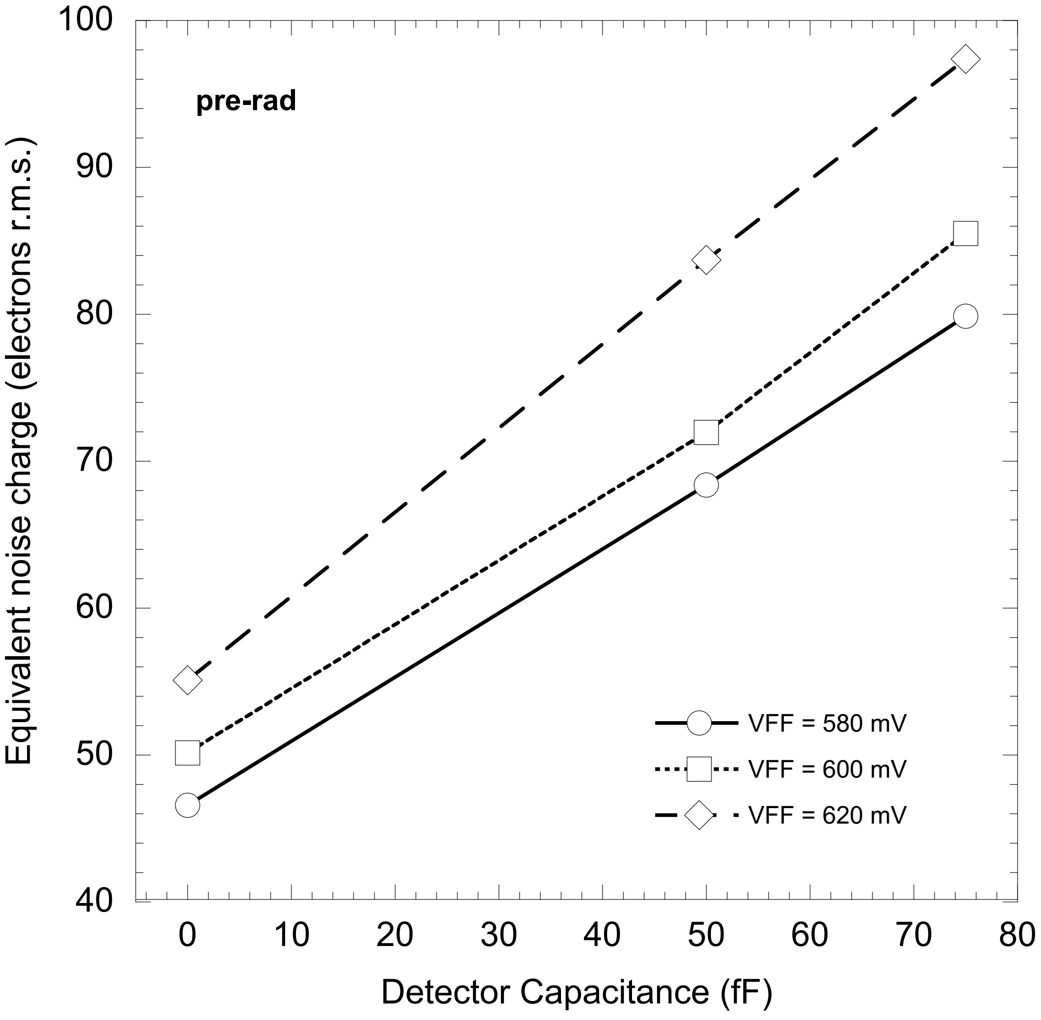
Charge sensitive amplifier – Test results

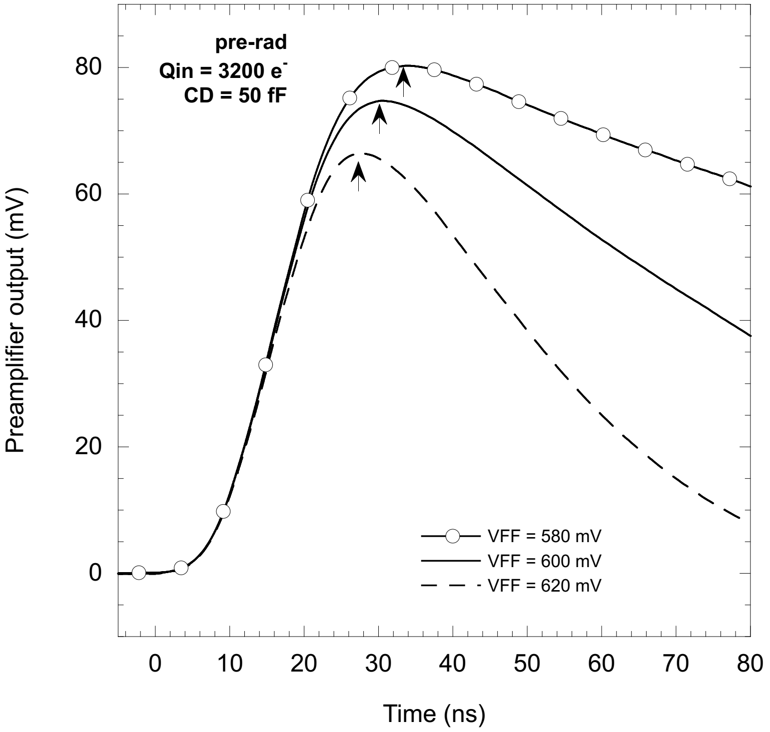


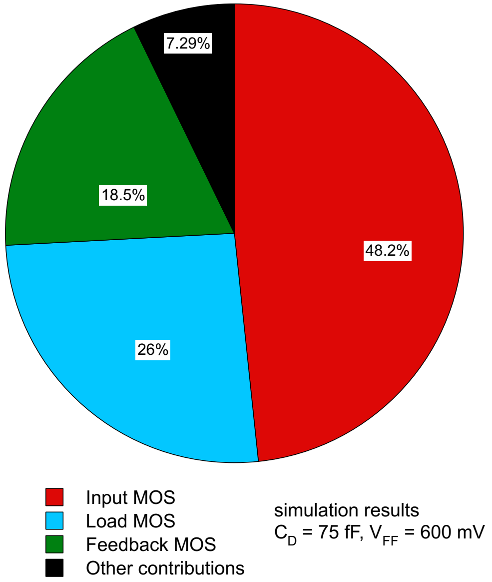


- CSA **peak amplitude** as a function of input charge → linear behavior up to ~7000 electrons. The behavior is evaluated for different detector emulating capacitances
- **Time-over-Threshold** as a function of input charge, for different VFF → linear behavior up to ~13000 electrons (max INL ~3.1% for VFF=600 mV)

Charge sensitive amplifier – Test results



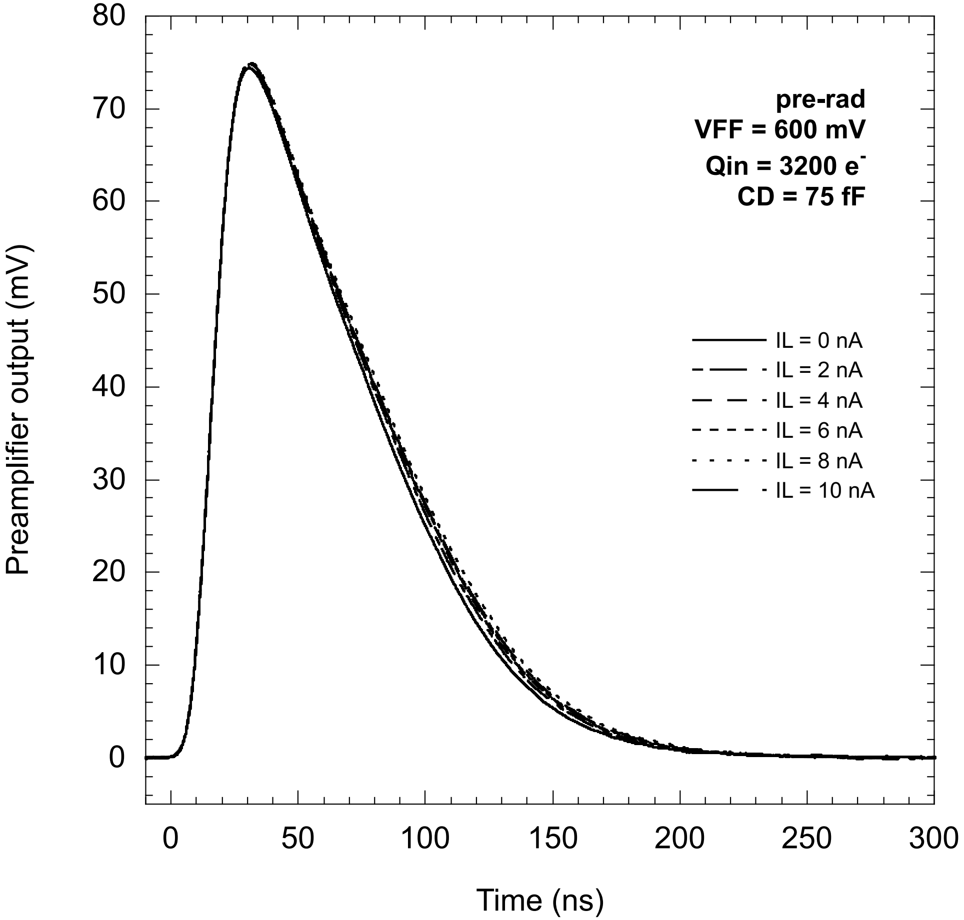


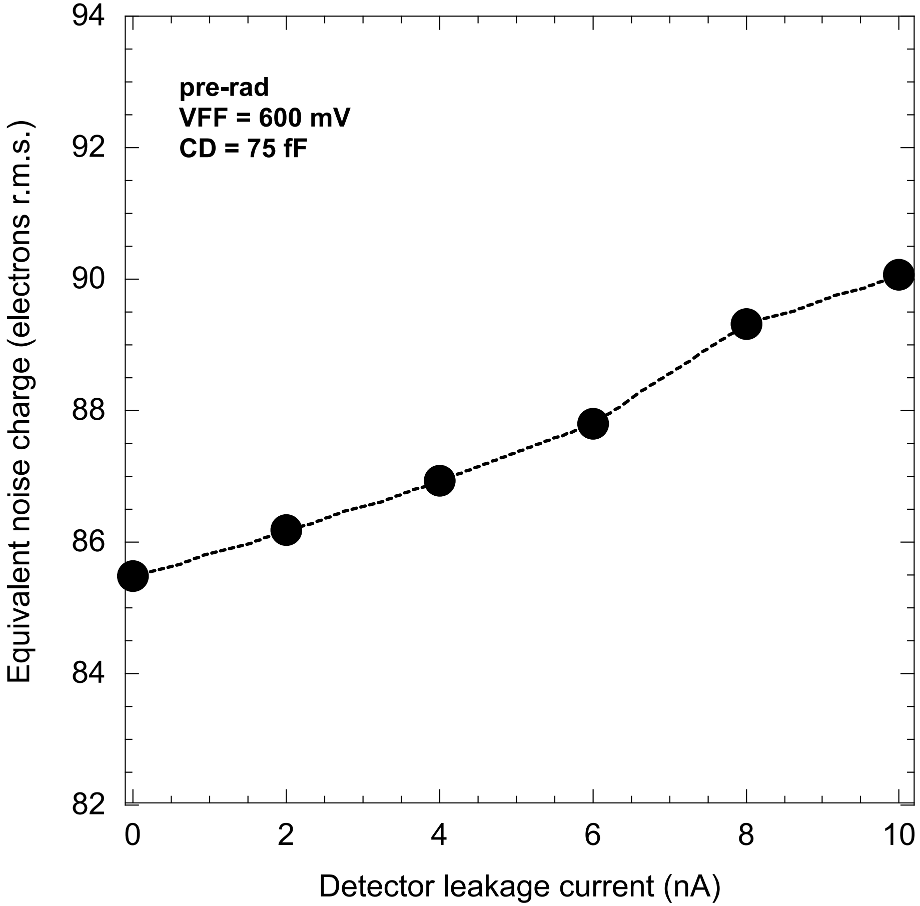


- **Measured ENC** as a function of the **detector emulating capacitance**, for different V_{FF} → ENC ≈ 70 e r.m.s @ CD=50fF
- **Noise increases** for larger V_{FF} (larger C_F discharge current): larger parallel noise contribution and faster preamp output signal (increased contribution from input MOS channel thermal noise)
- Main **contributors** to the noise: preamp input MOS, load and feedback transistors

L. Gaioni et al., **Design and characterization of a 28 nm CMOS charge sensitive amplifier for harsh radiation environments ,** Nuclear Inst. and Methods in Physics Research, A 1083 (2026) 171177

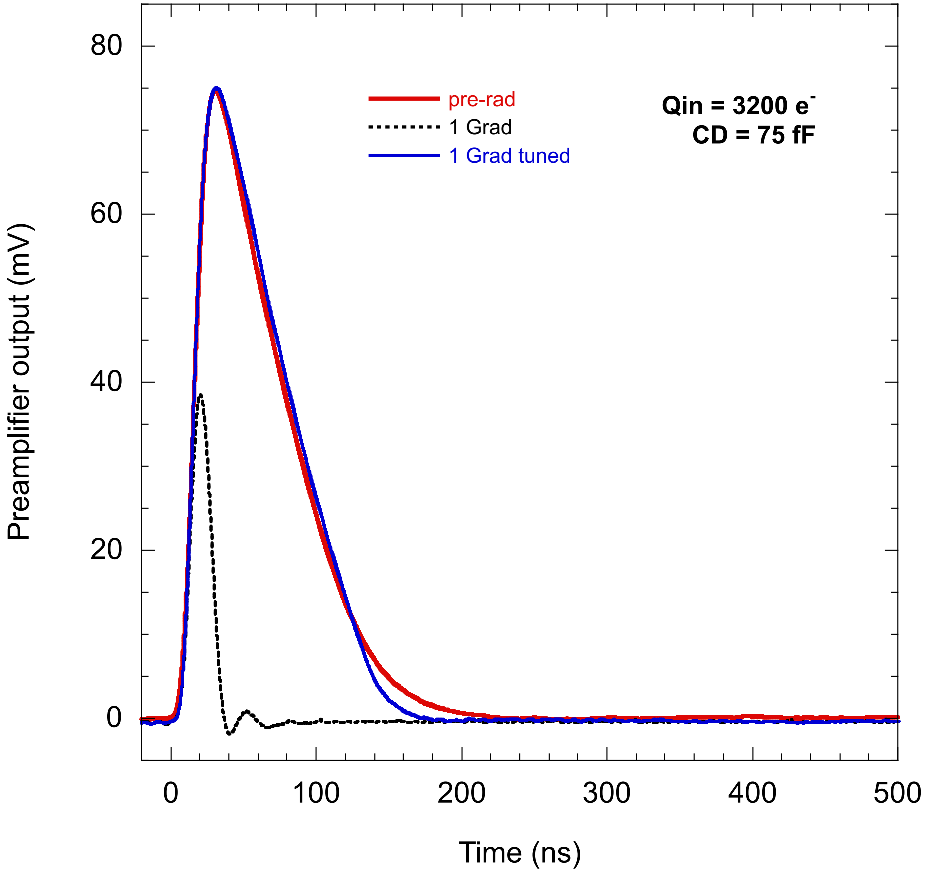
Charge sensitive amplifier – Test results

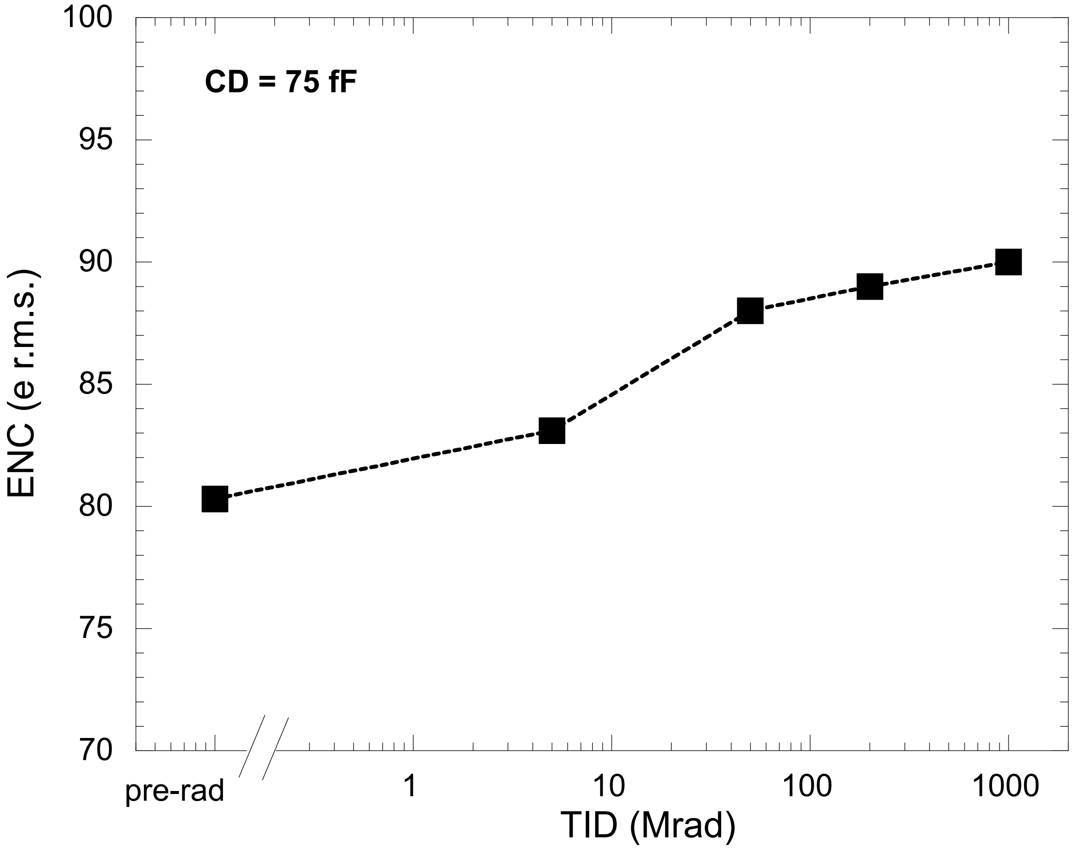




- CSA output signal in the presence of detector **leakage current** (emulated): both peaking time and amplitude are preserved, together with pulse duration
- **ENC** as a function of the detector **emulated leakage current:** slight increase in the ENC was detected for an increasing current (ML contribution)

Charge sensitive amplifier – Radiation effects





- One sample of the prototype chip has been exposed to a **TID up to 1 Grad** with a 10 keV X-ray source
- **CSA output** as a response to an input signal of 3200 electrons before irradiation (red) and at 1 Grad (dashed black) → pulse duration and amplitude significantly reduced (ML leakage) → retuning of VFF (from 600 mV to 490 mV) partially restores the waveform (blue)
- Moderate increase (~12%) of the **ENC at 1 Grad**

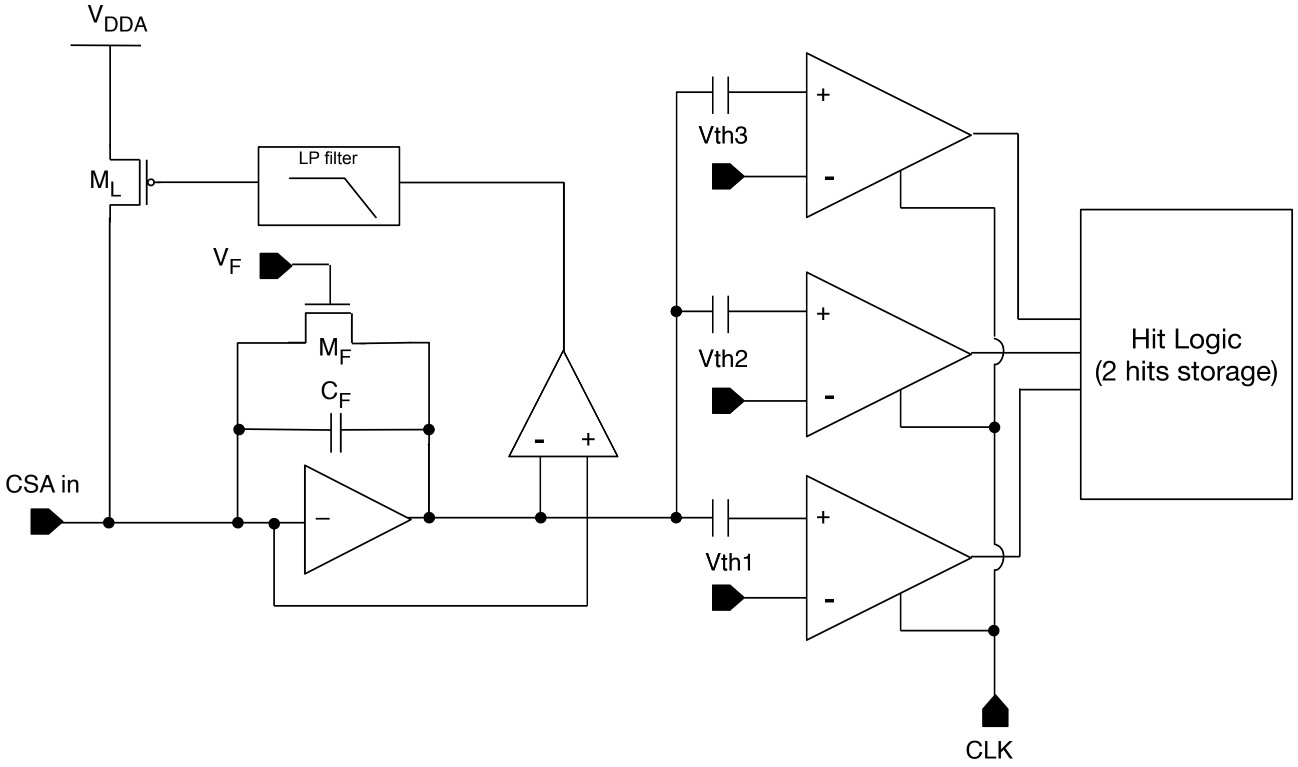
Front-end design for HEP applications

- Leveraging the CSA architecture described in the previous slides, **two front-end channels** have been devised:

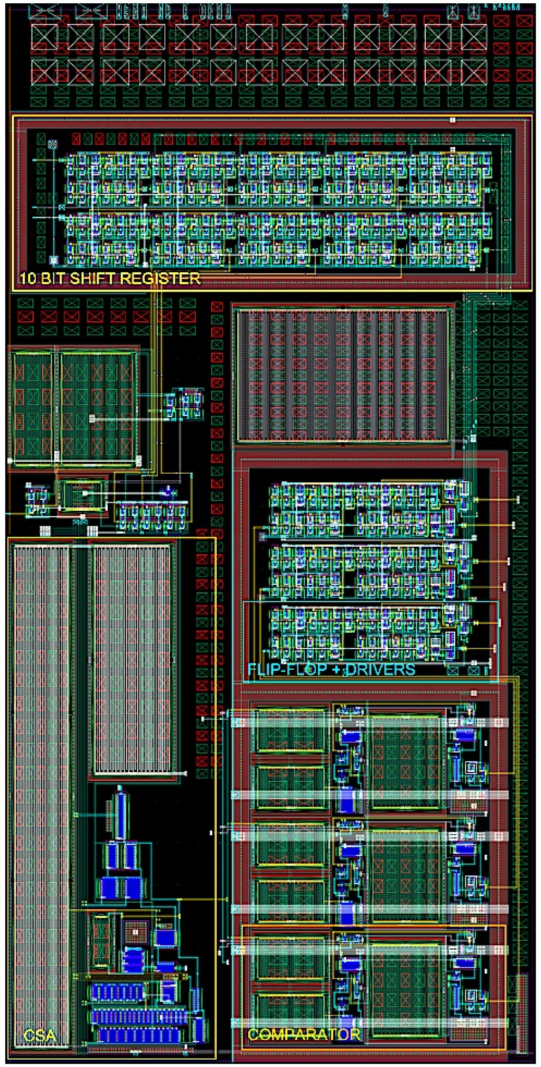
- **Flash ADC** based front-end → preamp + AC coupled bank of comparators implementing a 2-bit flash A/D conversion
    - **Zero dead-time analog channel for high-rate applications** (non negligible probability of having hits in adjacent bunch crossings)

- **Time-over-Threshold (ToT)** based front-end → preamp + DC coupled comparator, with ToT A/D conversion of the signal + threshold tuning DAC
    - Specs mostly **derived from RD53, but targeting operation at a lower threshold**

Flash ADC based front-end

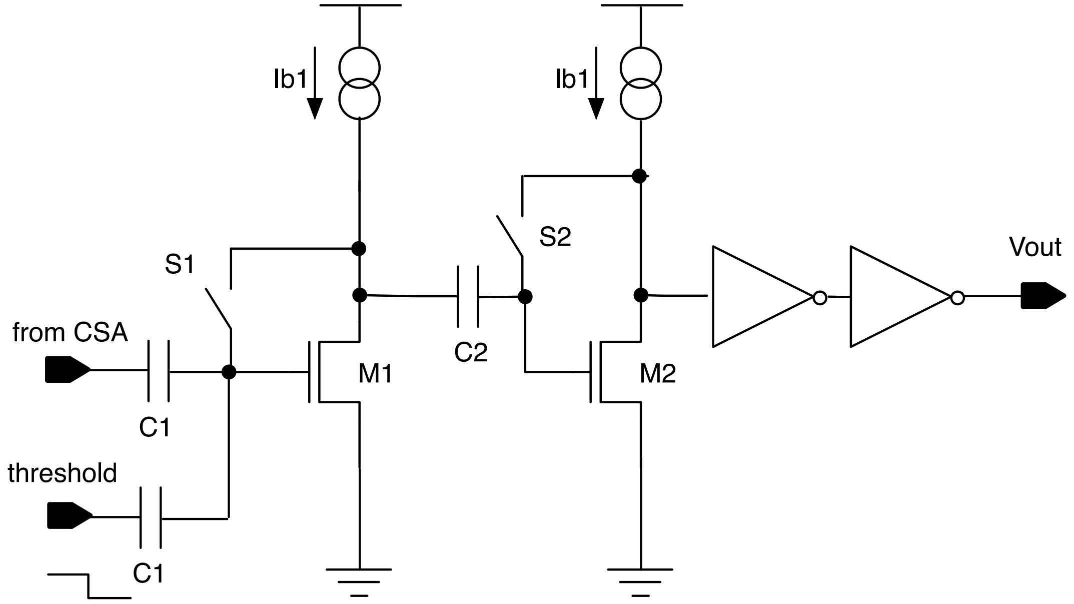


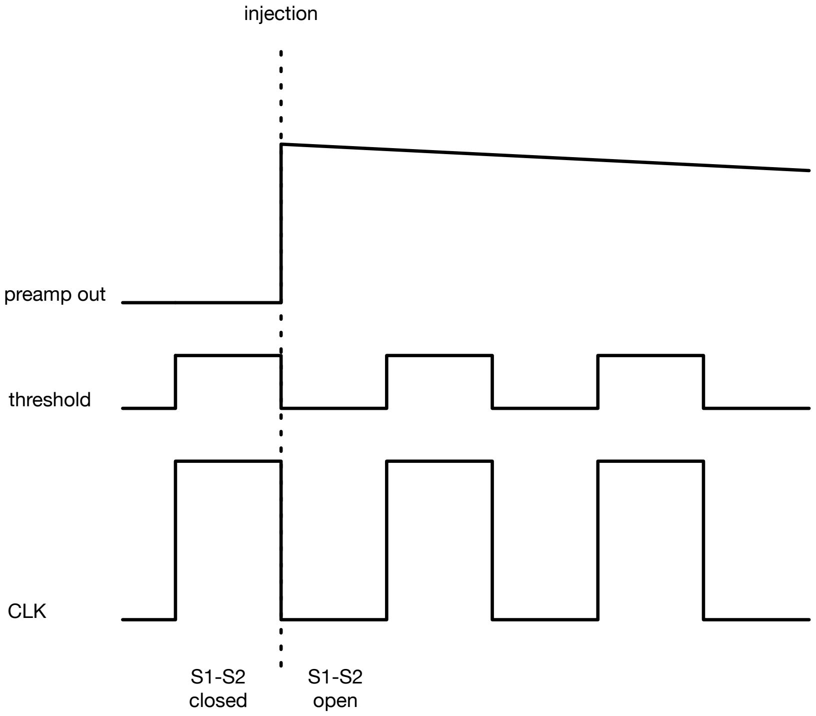
- Preamp (**regulated cascode**) two independent feedbacks
- Ancillary blocks for **detector emulation**



- **AC coupled, auto-zeroed comparators**, operated with 40 MHz clock, implementing a **2-bit flash ADC.** The design is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required
- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ V_{DD}=0.9 V
- Elementary cell size: 25 x 50 µm^2 (analog+digital)
- Integrated in an **8x4 matrix**

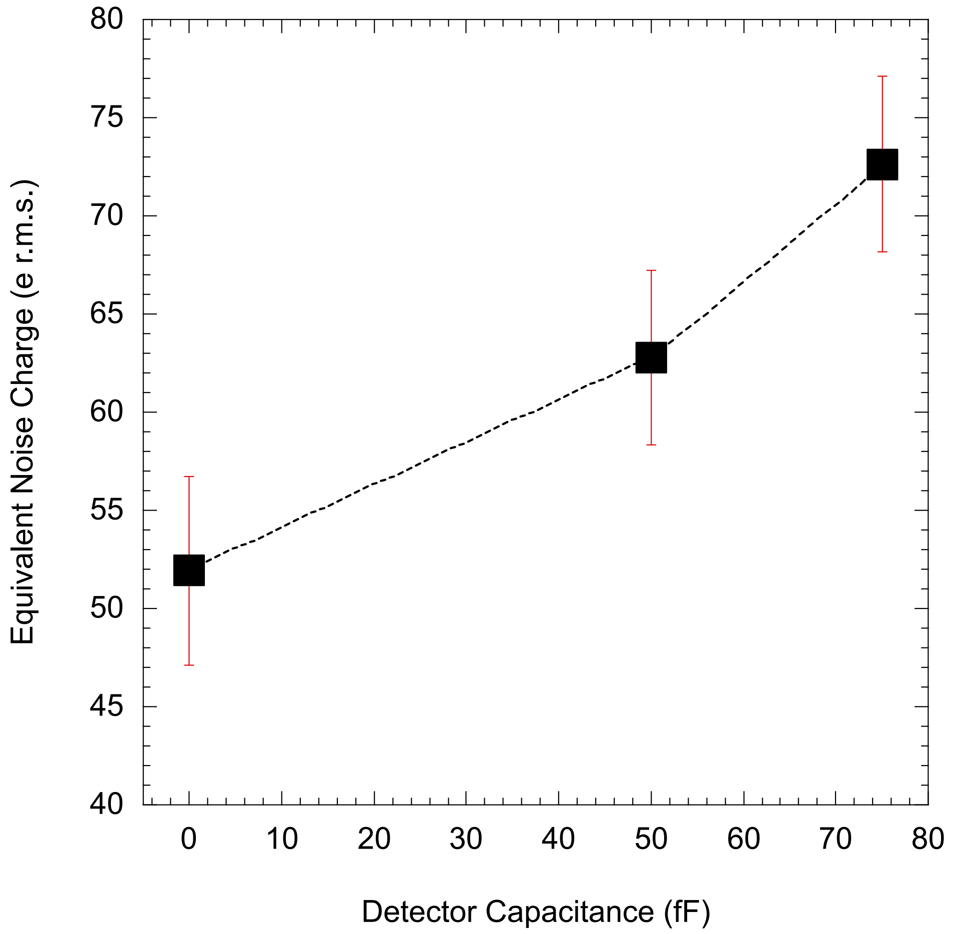
Clocked comparator

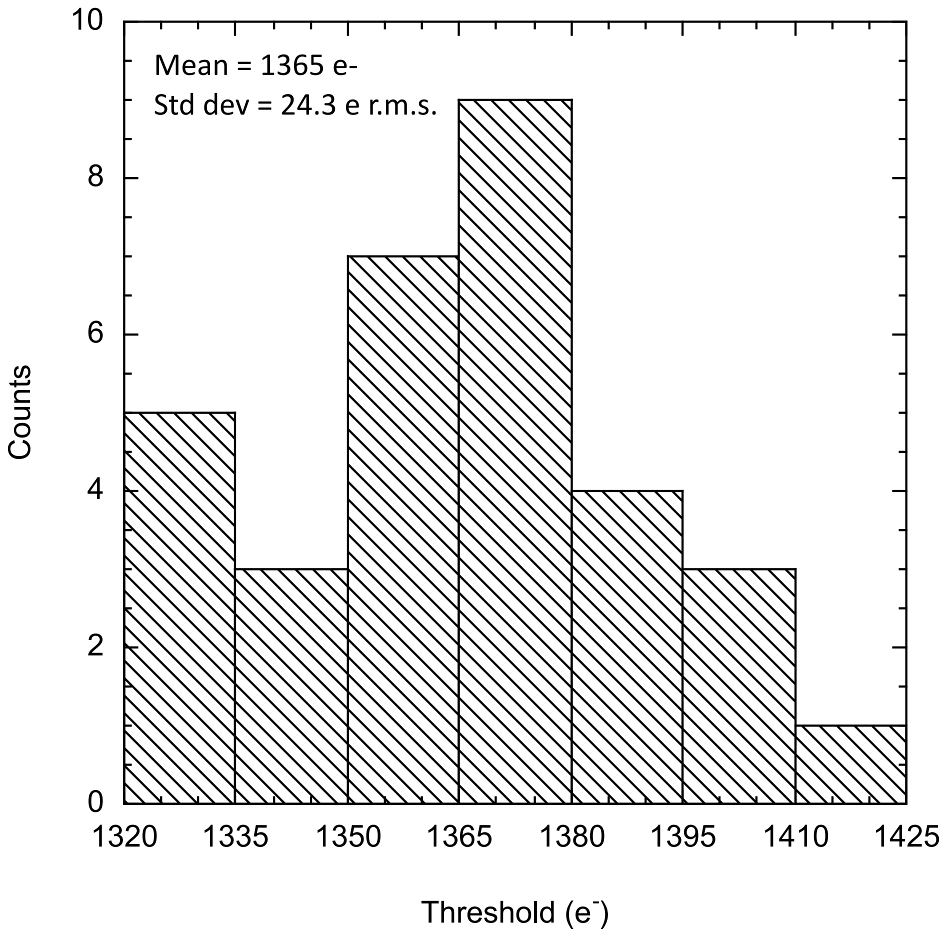




- Clocked, **auto-zeroed** comparator featuring low power consumption (700nW)
- Two phases operation: Reset phase (S1, S2 closed) and Comparison phase (S1, S2 open)
- Signal from CSA and threshold injected at the gate of the input transistor M1, **synchronous with CLK** (controlling S1 and S2)
- CSA signal larger than the threshold → positive going signal at M1 gate, amplified by two common source stages and fed to output inverters that consolidate the output logic
- **Low threshold dispersion** (signal and threshold injected at the gate of one single transistor)

Flash ADC front end - Test results



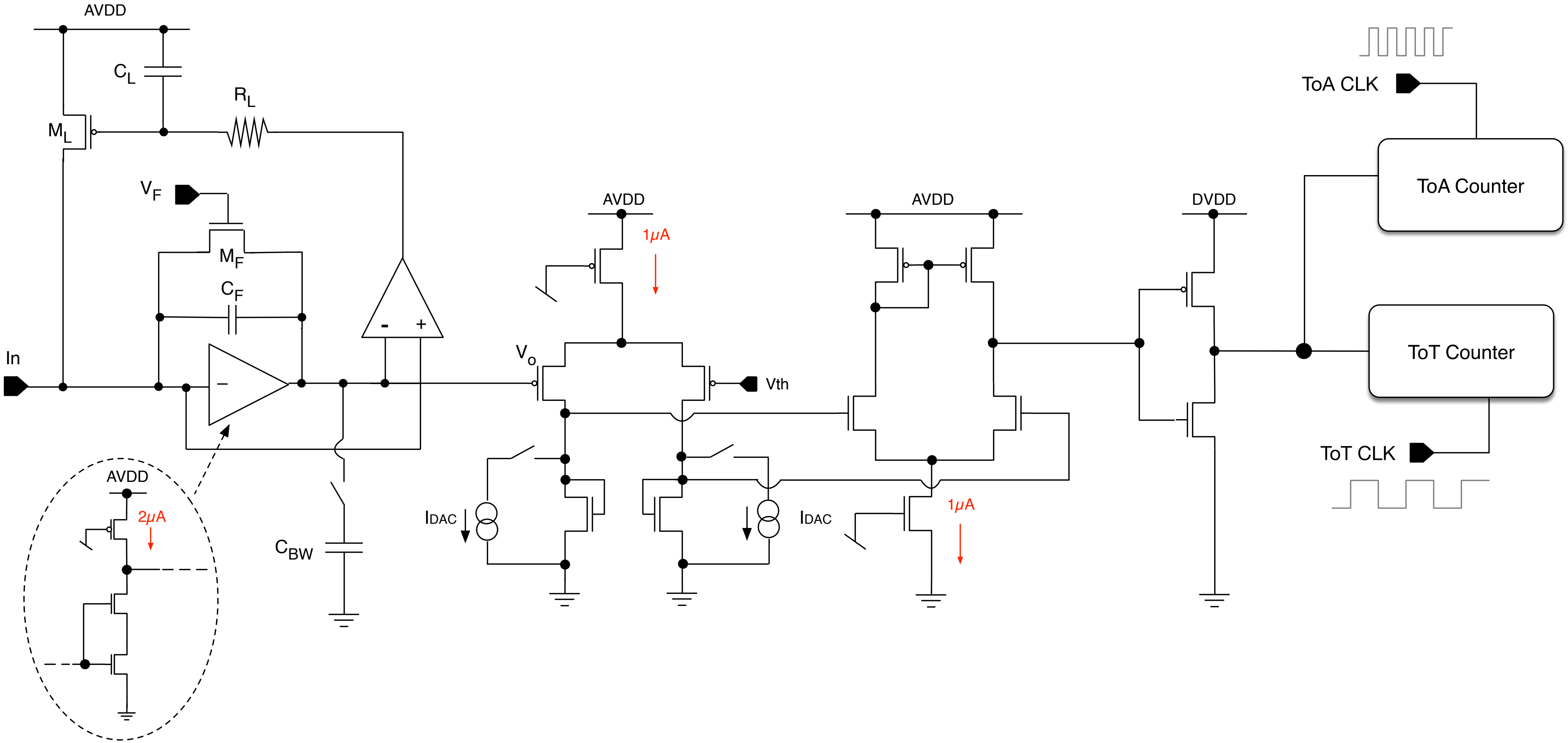


- **ENC** as a function of the simulated detector capacitance --> ENC ≈ 63 electrons r.m.s. @ CD=50 fF
- **Threshold distribution** → dispersion close to 24 electrons r.m.s.

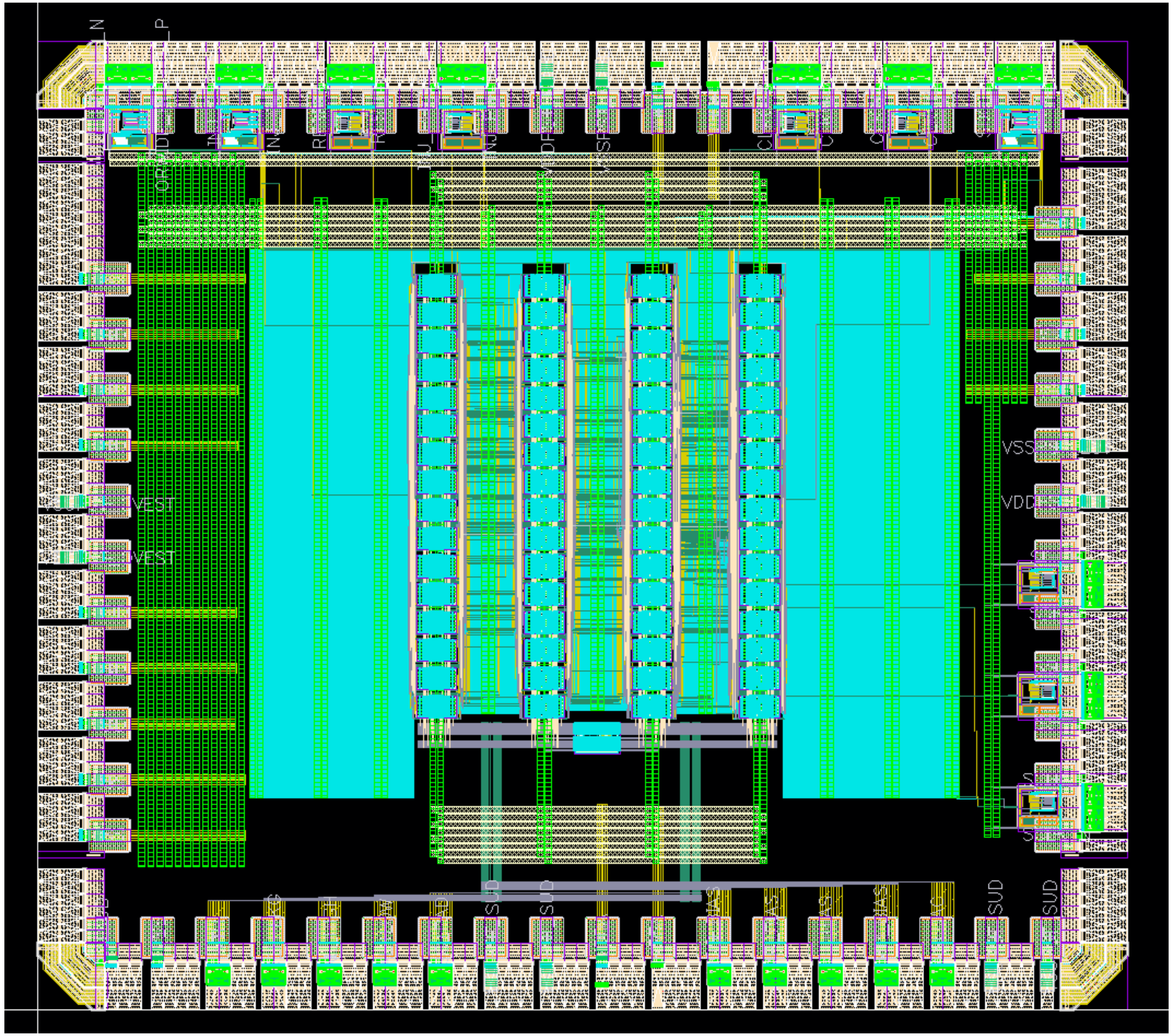
L. Gaioni et al., **A 28 nm CMOS front-end circuit with in-pixel flash ADC for high-rate hybrid detectors,** Nuclear Instruments and Methods in Physics Research A 1080 (2025) 170655

ToT-based front-end

- **A front-end architecture (optimized for low thresholds)** has been developed, based on **Time-over-Threshold (ToT)** → preamp + DC coupled comparator + 5–bit threshold tuning DAC
  - Self-cascode preamp gain stage
  - Differential comparator architecture to improve the immunity to interferences



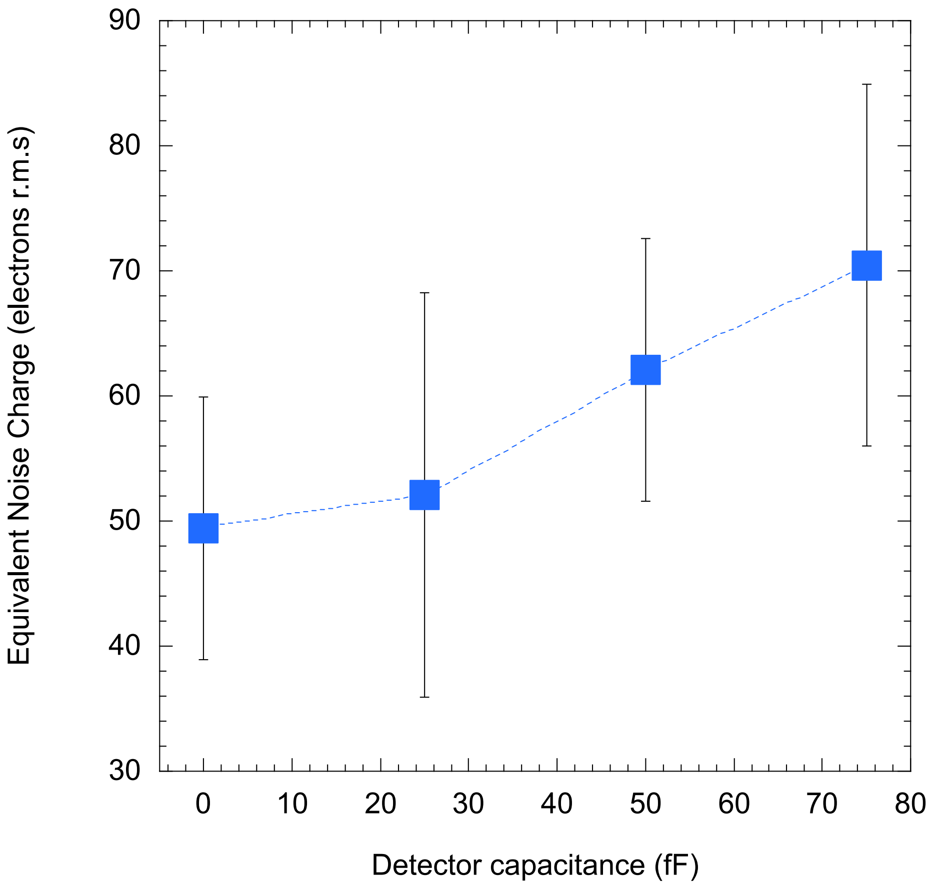
ToT-based front-end: chip layout

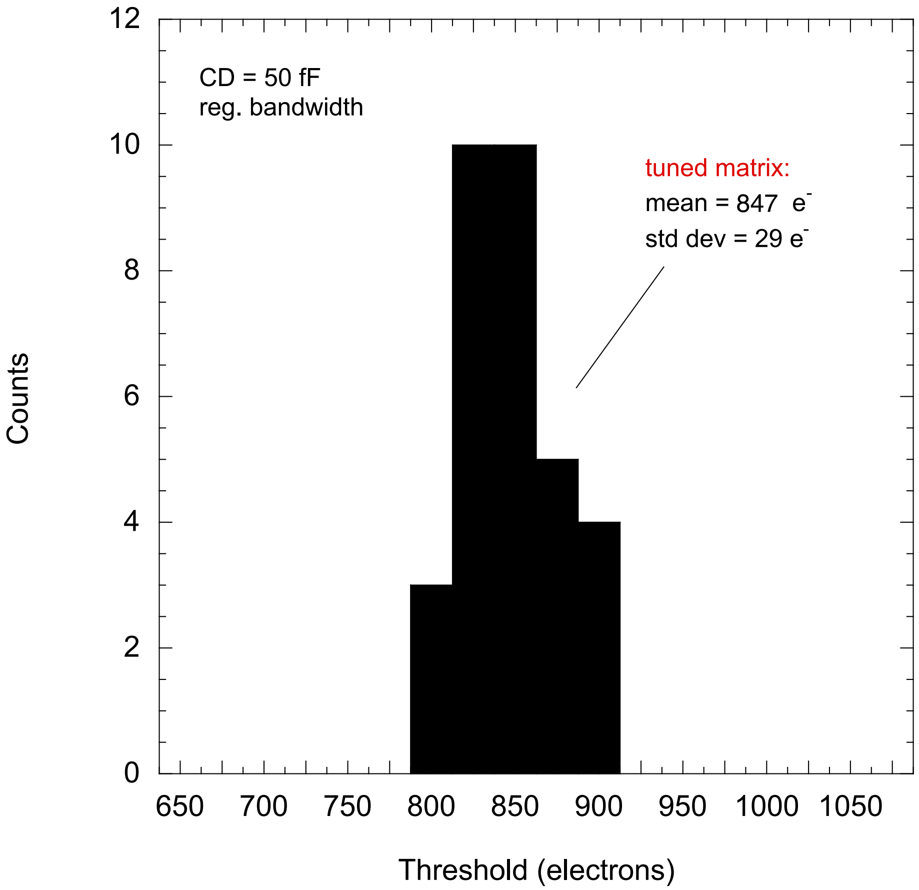


- 8x32 matrix of readout channels
- 100 x 25 μm^2 pixels
- Shared 8-bit Time of Arrival Counter (640 MHz)
- Shared 5-bit Time-over-Threshold Counter (40 MHz)
- SPI controller

- Developed with **INFN MI** and **INFN BO**

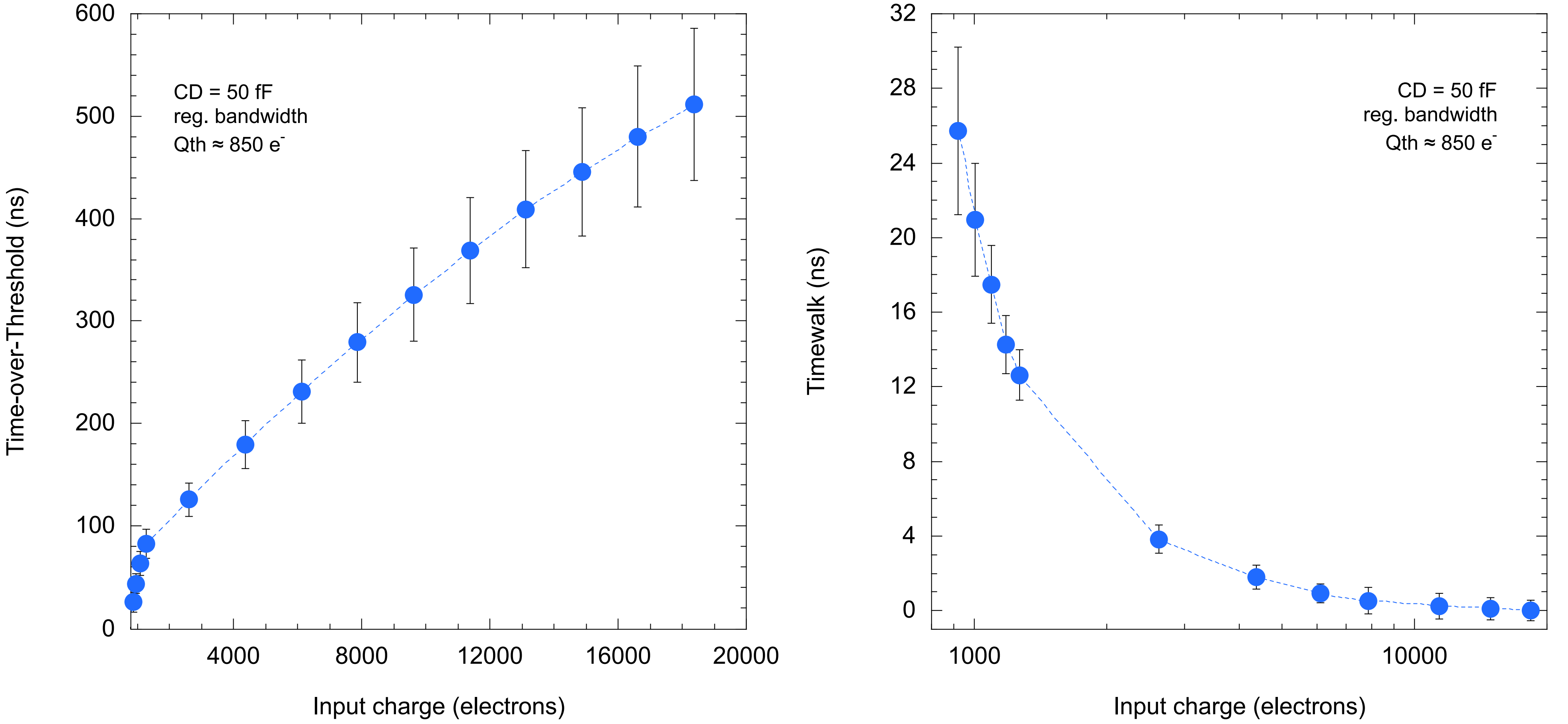
Test results: noise and threshold





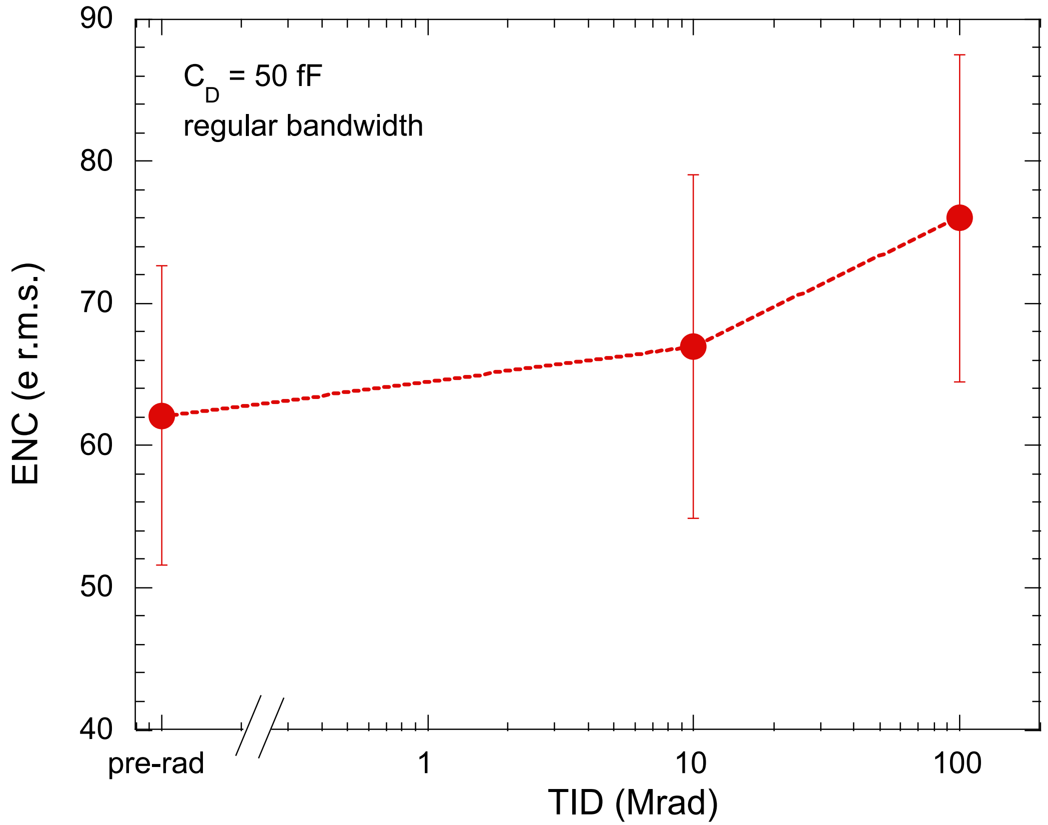
- Data obtained on a sub-matrix region including 32 pixels
- A mean **ENC ≈ 62 e r.m.s.** measured @ C_D = 50 fF (regular bandwidth option)
- **Tuned threshold** below 1000 electrons, with a dispersion of 29 e r.m.s. (pre-tuning ~260 e r.m.s.)

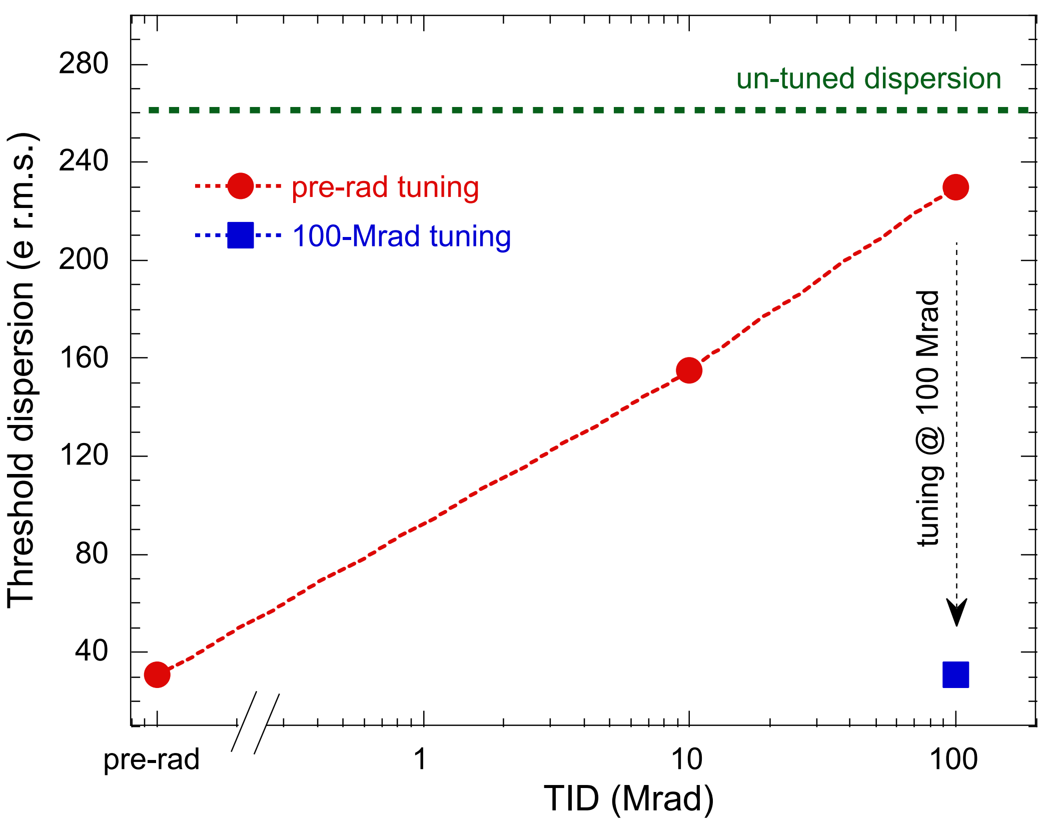
Test results: Time-over-Threshold and Time-walk



- **Non-linearity** in the lower range of the ToT characteristic –> time-walk effects + feedback MOS M_F in triode for small signals
- **INL ≈ 3.8%** from ~1.2ke- up to 15 ke-
- **Time-walk** ~26ns (slightly exceeding LHC bunch period) for 50 e- overdrive

Preliminary results: radiation effects





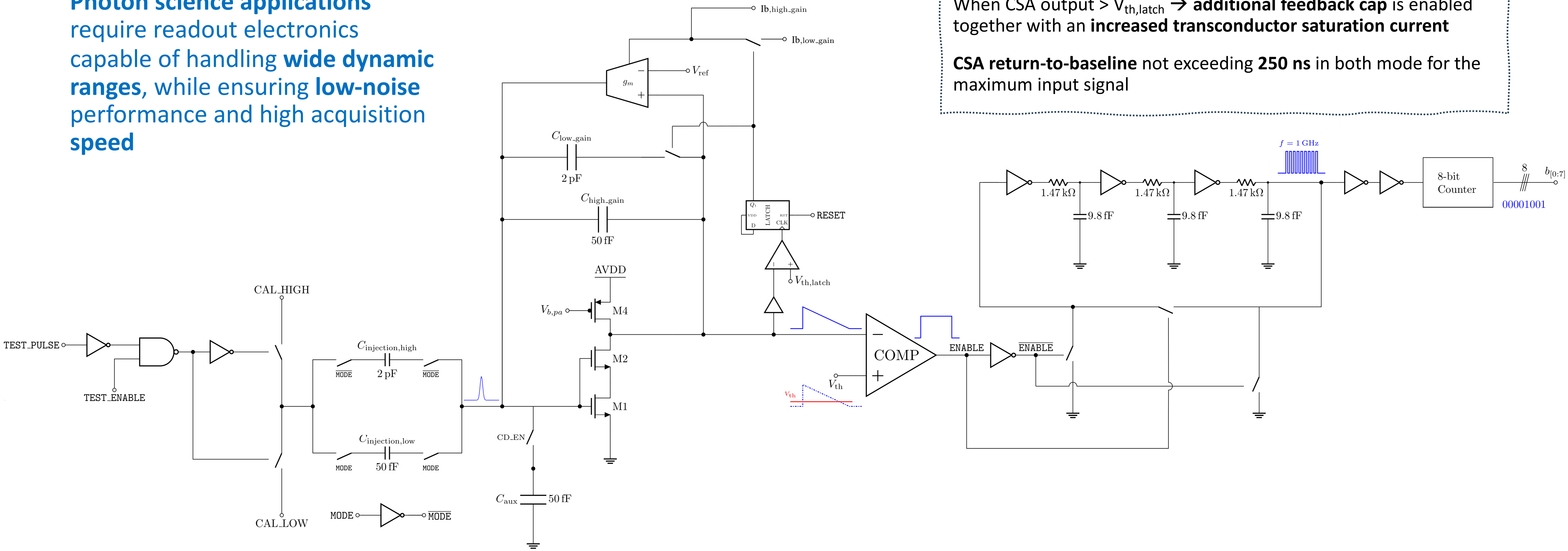
- One sample irradiated up to TID **100 Mrad** (dose rate ~1 Mrad/h)
- **ENC increase** at TID = 100 Mrad of the order of 20%
- Significant **de-tuning** with TID –> full recovery at TID=100 Mrad after threshold trimming

Proof-of-concept channel for photon science

Photon science applications require readout electronics capable of handling **wide dynamic ranges**, while ensuring **low-noise** performance and high acquisition **speed**

When CSA output > $V_{th,latch}$ → **additional feedback cap** is enabled together with an **increased transconductor saturation current**

CSA return-to-baseline not exceeding **250 ns** in both mode for the maximum input signal

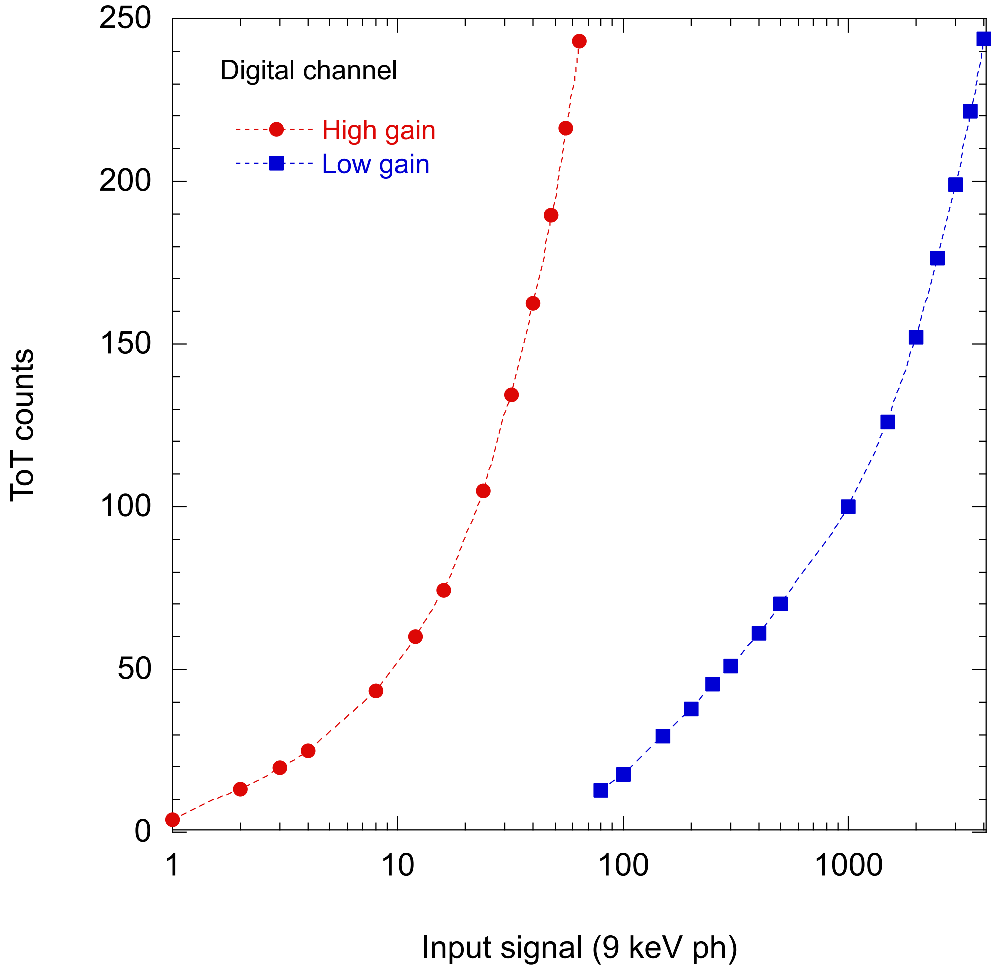


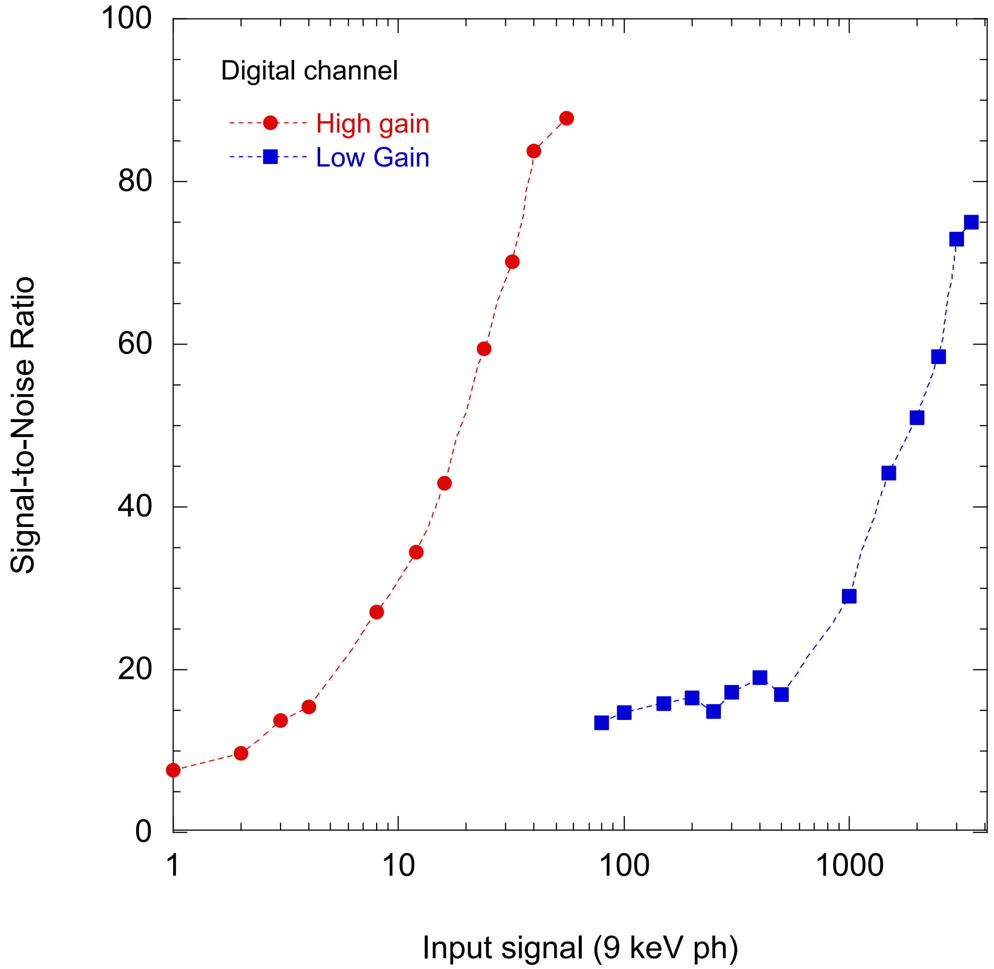
The proposed channel features **dual gain architecture**, enabling:

- **High gain mode** for weak signals (1 – 50 photons @ 9keV)
- **Low gain mode** for large signals (50 – ~4x10^3 photons @ 9keV)

- **8-bit ToT** + **1bit flag** for gain mode
- The channel fits an **area of 110 µm x 55 µm** (including very large injection mom capacitors)
- A **mini@sic chip** including standalone channels has been submitted and preliminarily tested

Preliminary test results





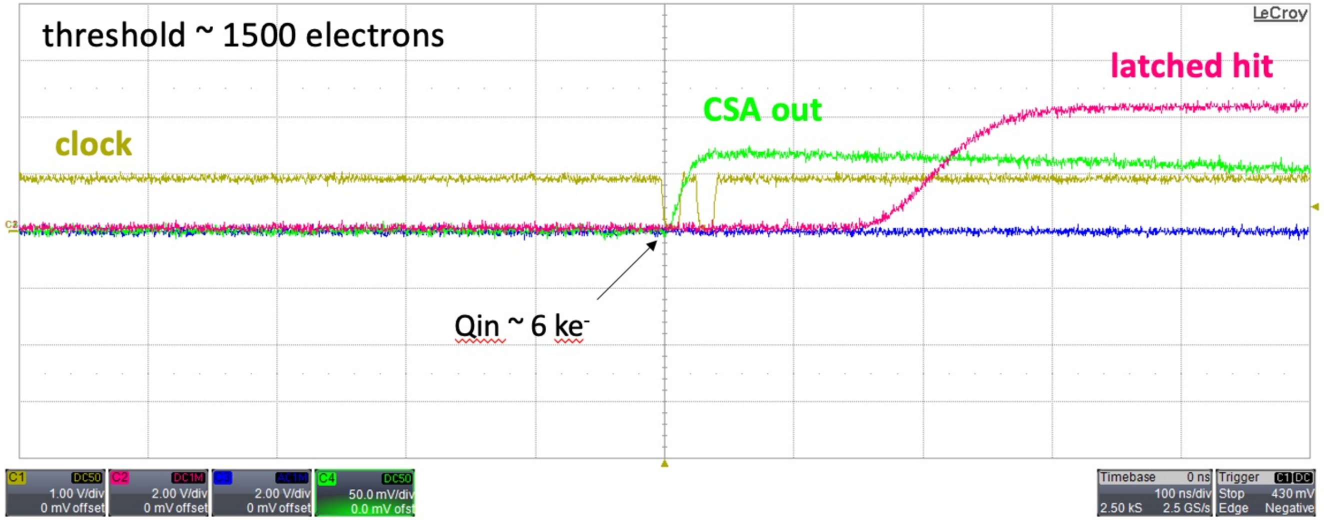
- 1 ToT count = 1 ns (nominally)
- **Minimum SNR** (as obtained from ToT dispersion) ~8 in high gain mode (~15 in low gain mode)

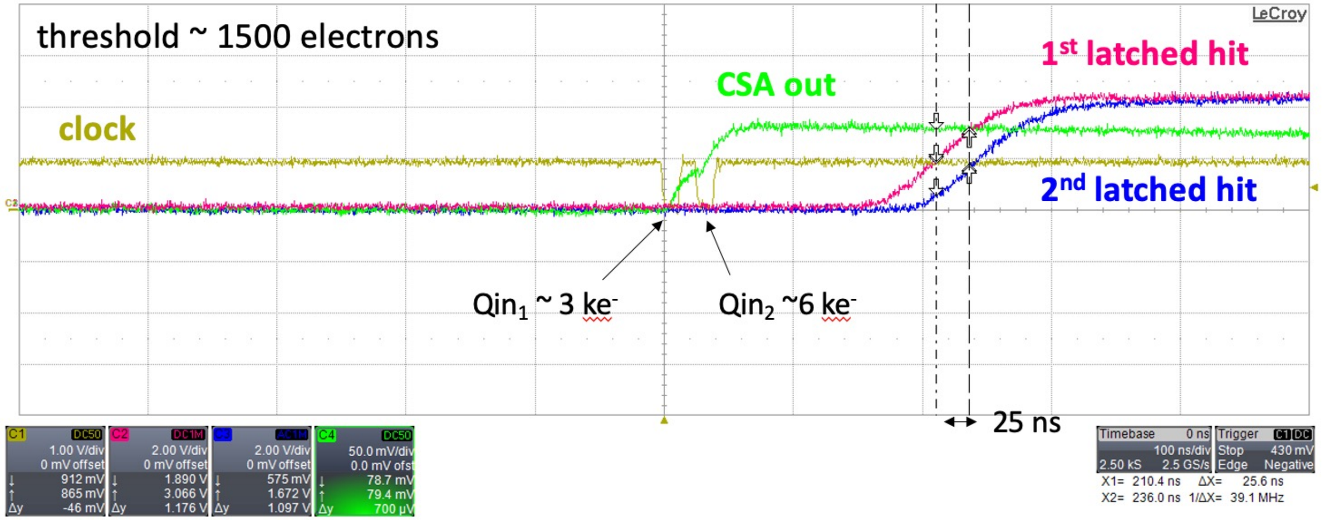
Conclusions and future steps

- Test on single devices and analog building blocks confirm the **high degree of tolerance to ionizing radiation** of the 28 nm CMOS technology, in particular from the standpoint of noise performance
- Different analog **front-end architectures** has been designed in a 28 nm CMOS technology and successfully tested
- Test results for the **ToT-based** front-end point to analog performance comparable to the one obtained in 65 nm design (e.g. RD53 chips), but enabling much **denser readout logic**
- Results for **Flash-ADC based** front-end are promising, showing good results in terms of noise and threshold dispersion
- A **proof-of-concept channel** for photon science applications has been developed, enabling single photon sensitivity while being able to cope with ~72dB input dynamic range (with a conversion time not exceeding 250 ns)
- Future steps
  → **radiation qualification** of the developed demonstrators in the Grad regime
  → Investigating **FinFET technology** in future projects

Backup

Flash ADC front end - Test results

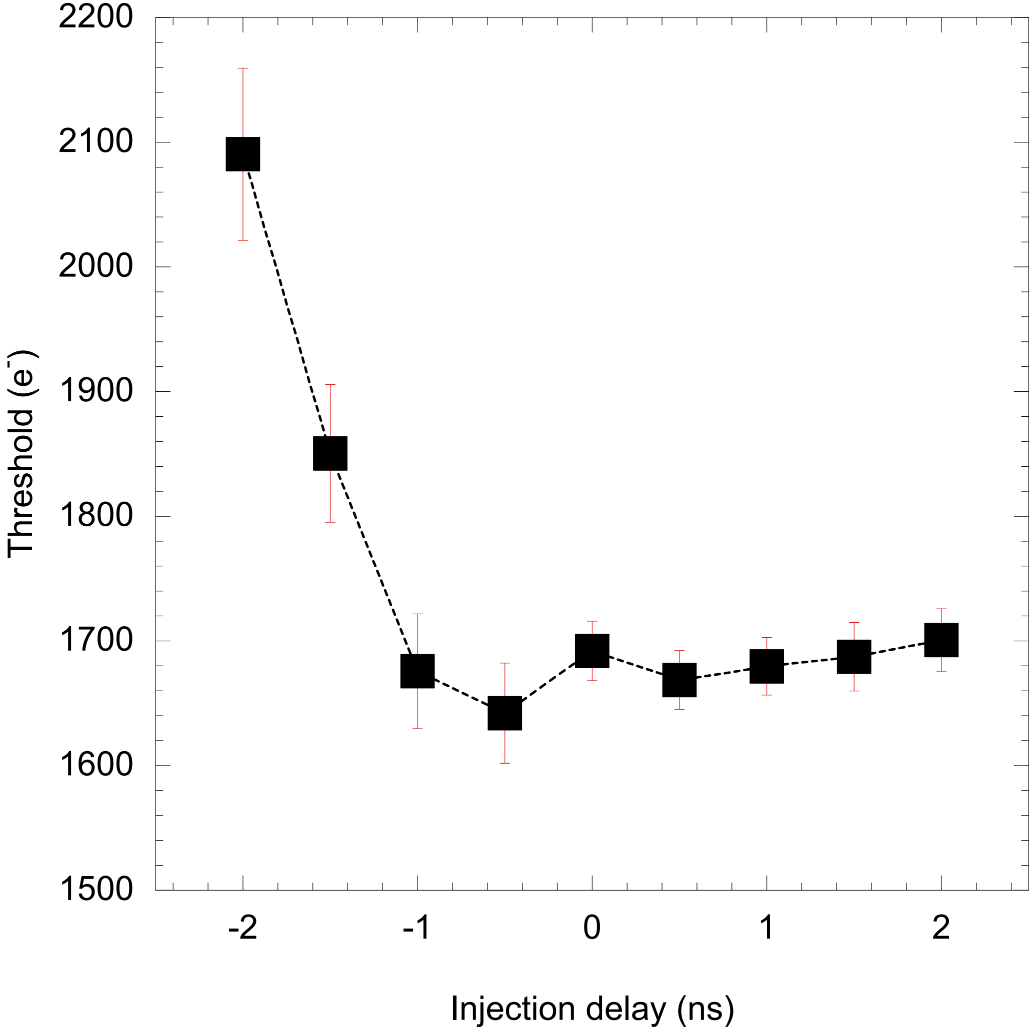


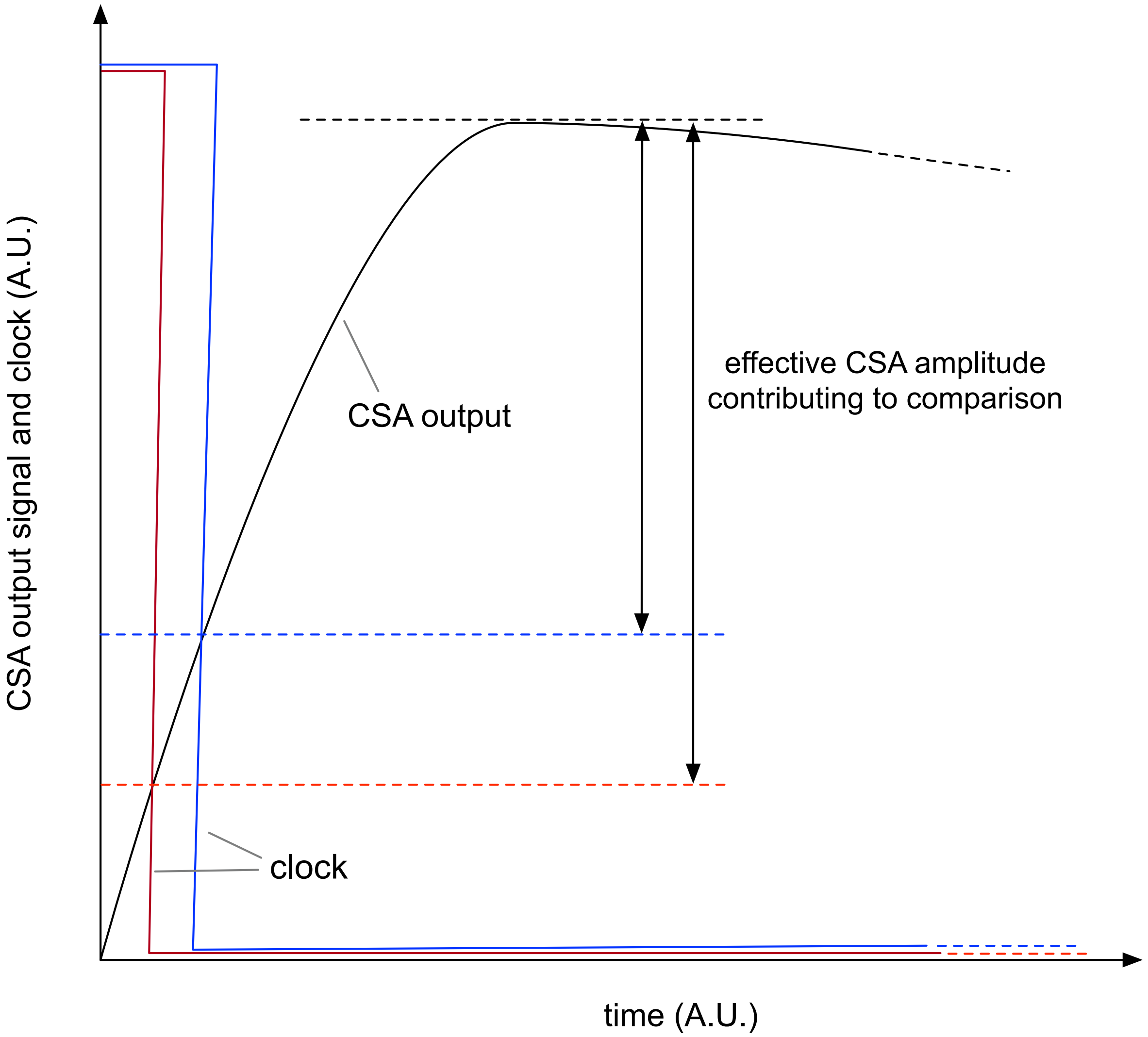


☺ the FE can successfully process hits in **adjacent buckets** (25 ns)

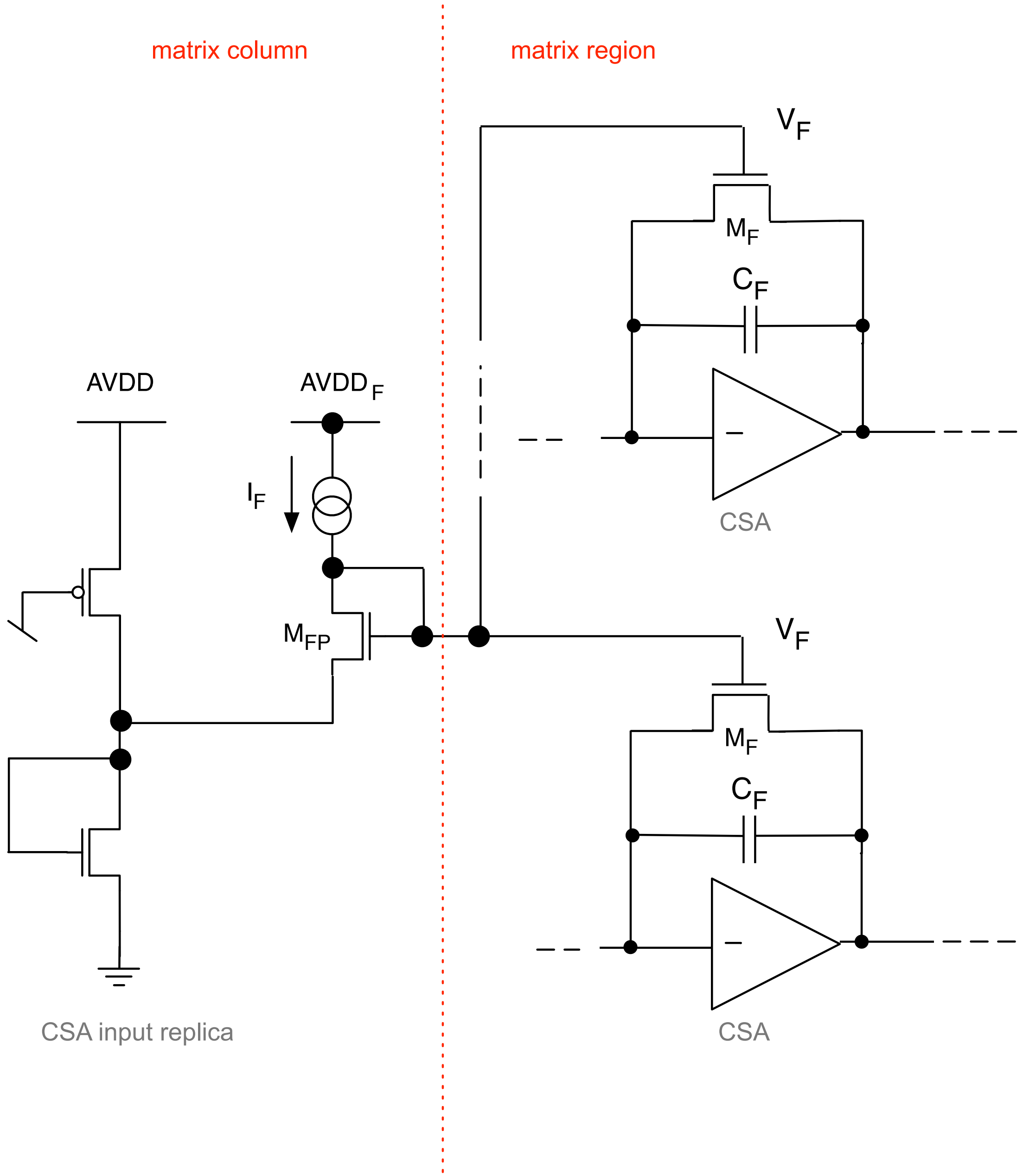
L. Gaioni et al., **A 28 nm CMOS front-end circuit with in-pixel flash ADC for high-rate hybrid detectors,** presented at the 2025 Vienna Conference on Instrumentation (VCI)

Flash ADC front-end

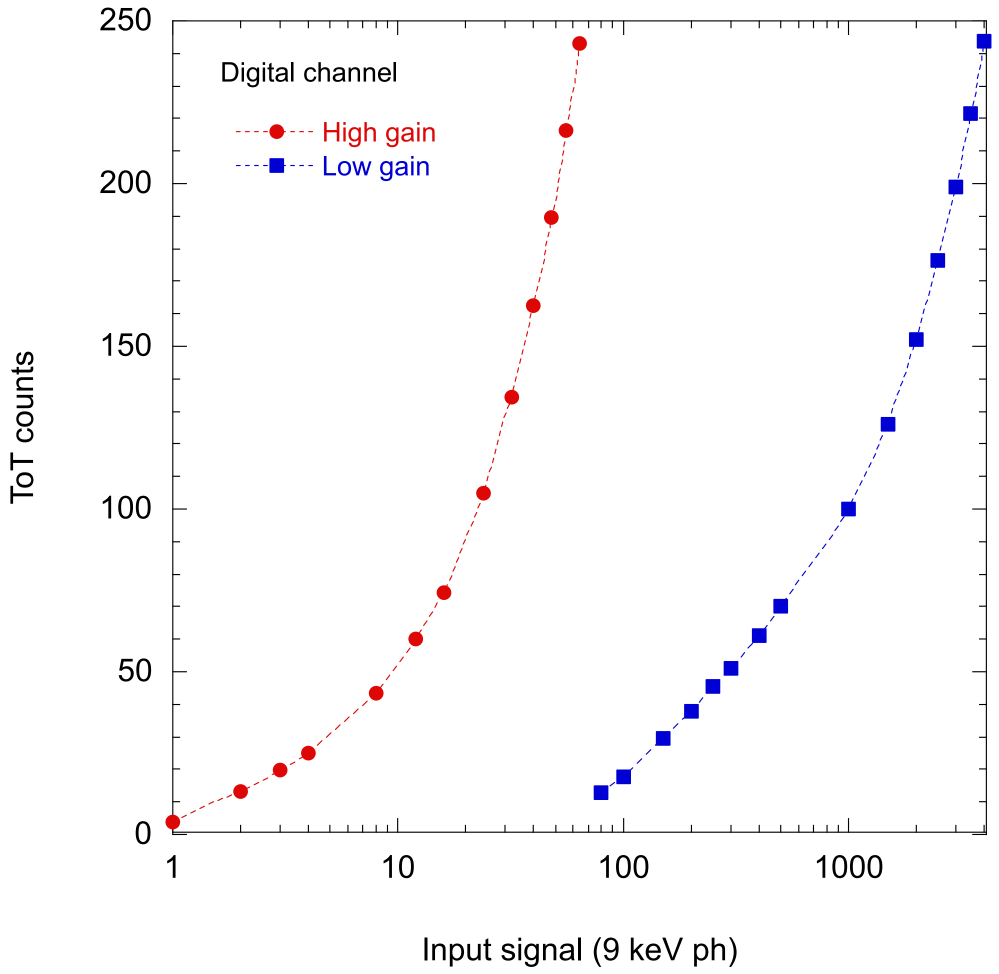




ToT-based front-end: VF bias



Noise for the dual-gain front-end



$$\sigma_N = \frac{\sigma_{ToT}}{d(ToT)/dN}$$

CSA radiation test: VFF variation