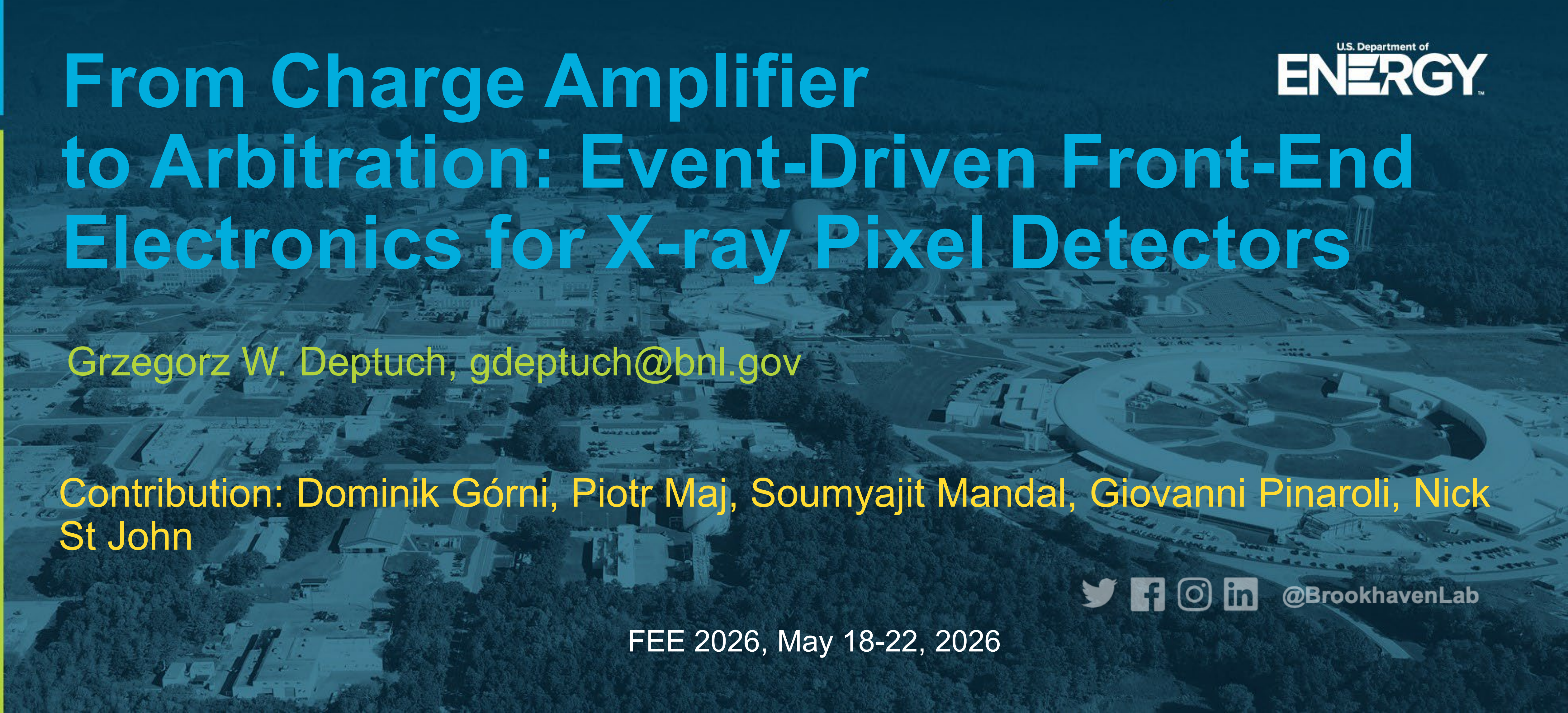

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U.S. Department of ENERGY

From Charge Amplifier to Arbitration: Event-Driven Front-End Electronics for X-ray Pixel Detectors

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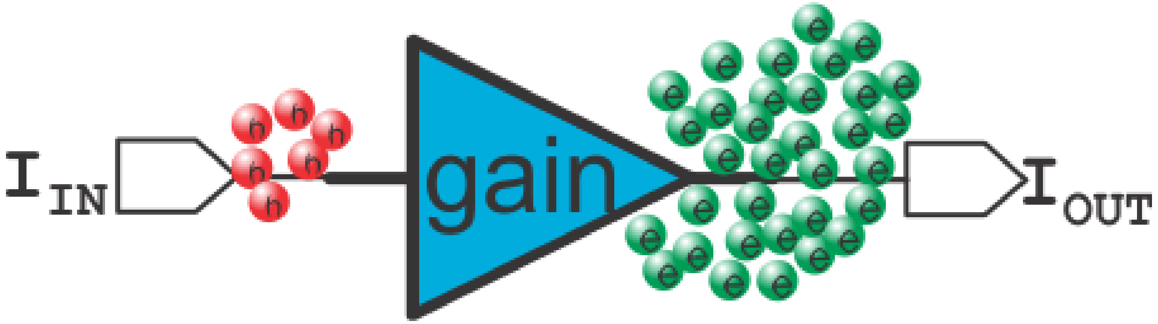
Contribution: Dominik Górni, Piotr Maj, Soumyajit Mandal, Giovanni Pinaroli, Nick St John

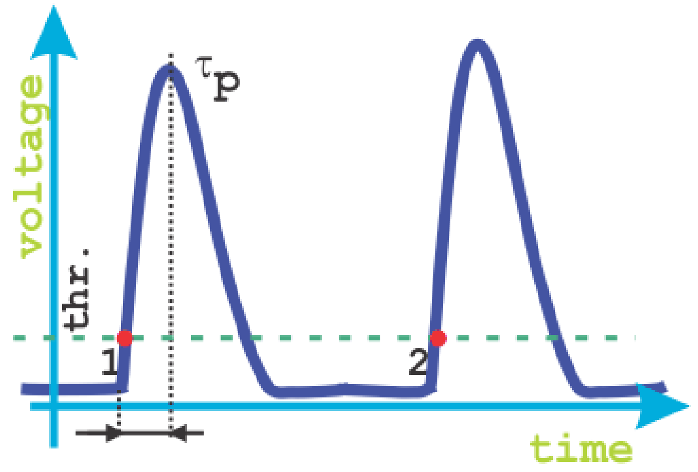
@BrookhavenLab

FEE 2026, May 18-22, 2026

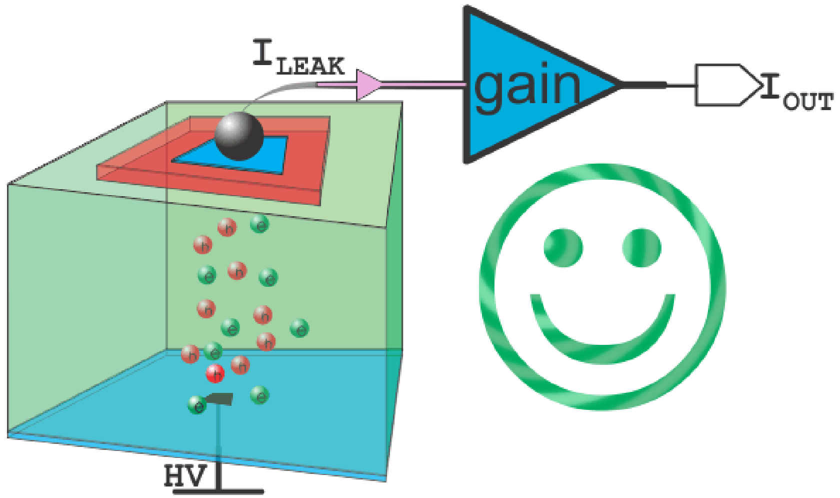
Desired Features of Analog Front-End



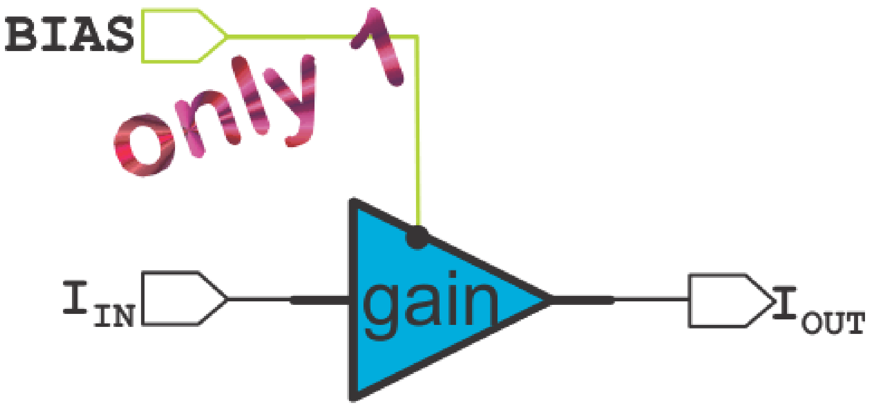
converts linearly small input charge to large output charge (⇨ linearity and low noise)



yields high precision pulses while operating at SNR optimized bandwidth (⇨ amplitude/timing resolution)

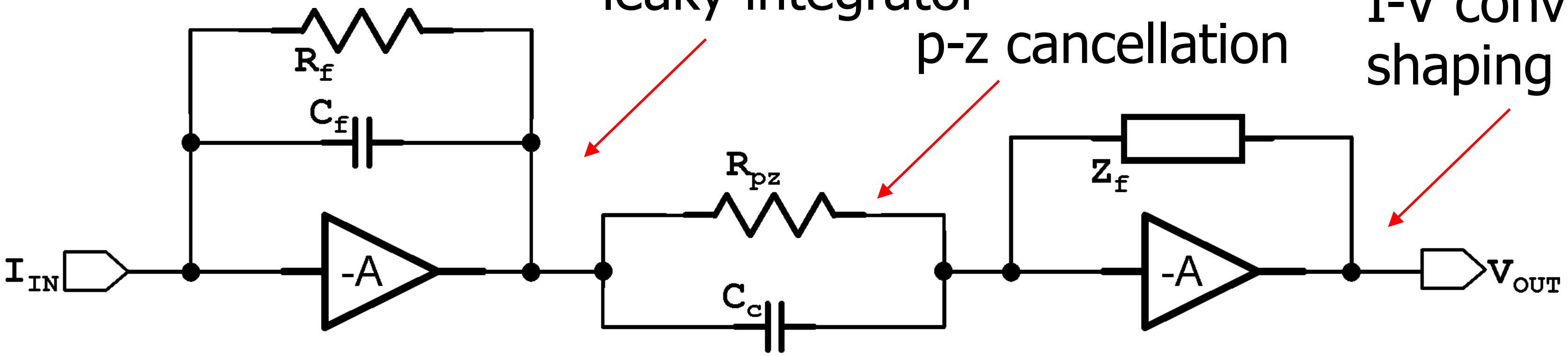


handles adaptatively sensor’s dark current (⇨ stability)



requires simple bias (⇨ calibration and low power)

Magic of p-z Cancellation



leaky integrator

p-z cancellation

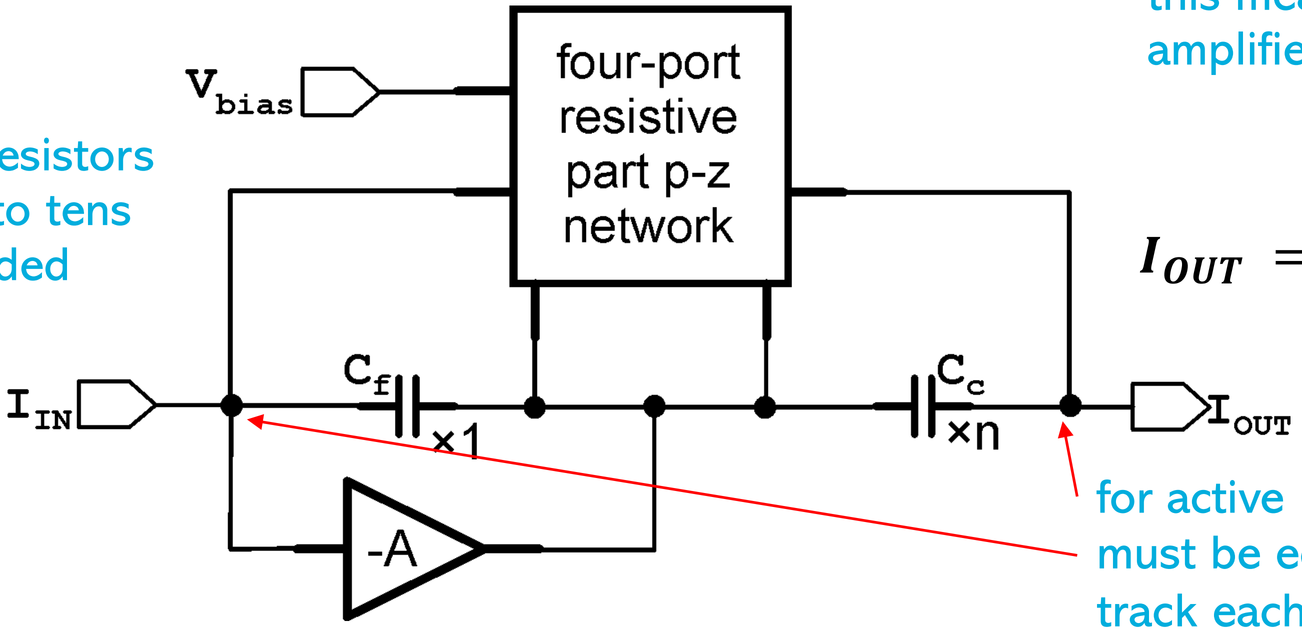
I-V converter / shaping filter

$Z_{f\mathrm{CSA}} = R_f||1/(sC_f) = R_f/(1 + sR_fC_f)$ $\mathrm{V_{out}}(s)/I_{in}(s) = Z_f\mathrm{Y_{p-z}}Yp - z\, Z_{f\mathrm{CSA}}$

$Y_{p-z} = 1/R_{pz} + sC_c = (1 + sR_{pz}C_c)/R_{pz}$ if $R_{pz}C_c = R_fC_f$, then $\mathrm{V_{out}}(s)/I_{in}(s) \approx \boldsymbol{R_fZ_f/R_{pz}}$

this means that output pulse is amplified copy of input current pulse

typically, passive resistors are not used due to tens of MΩ values needed

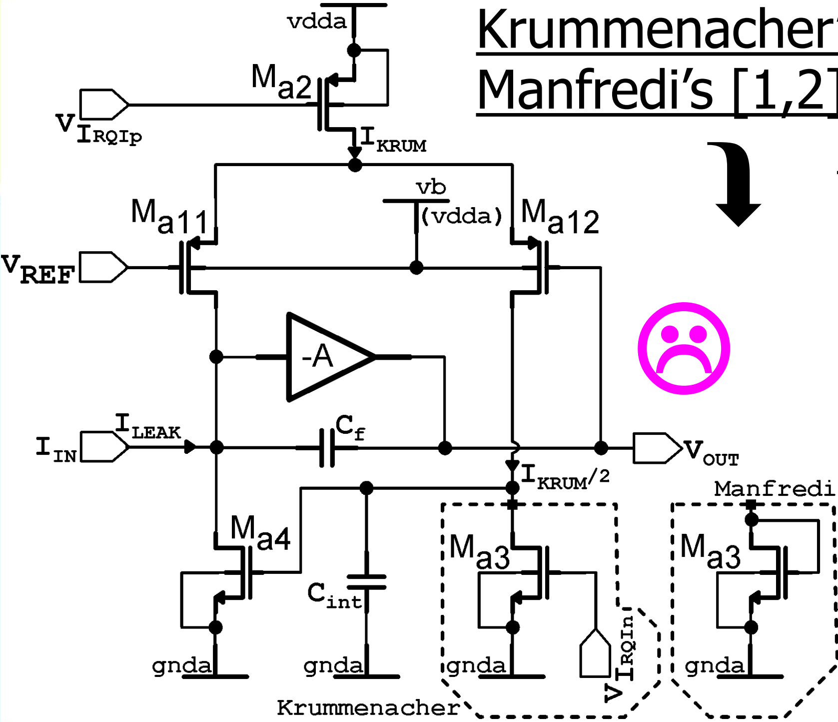


$\boldsymbol{I_{OUT} = n \times I_{IN}}$

for active resistors, terminal potentials must be equal to have R_{pz} and R_f track each other

Commonly Used Solutions

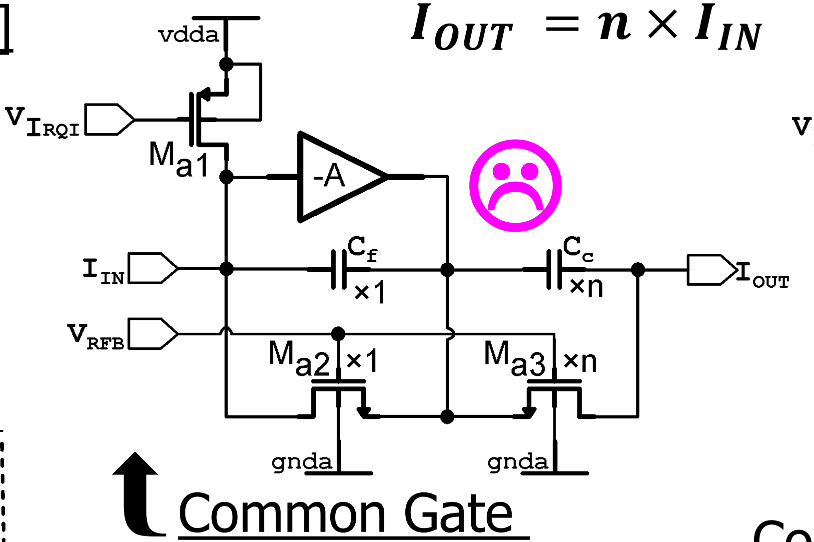
Krummenacher's / Manfredi's [1,2]



- feedback resistance ∝ current source^{-1},
- I_{KRUM} must exceed I_{LEAK}, ⇒ parallel noise,
- too large I_{LEAK} ⇒ loss of stability [3],
- requires large (~pF) C_{int},
- not connectable in p-z cancellation.

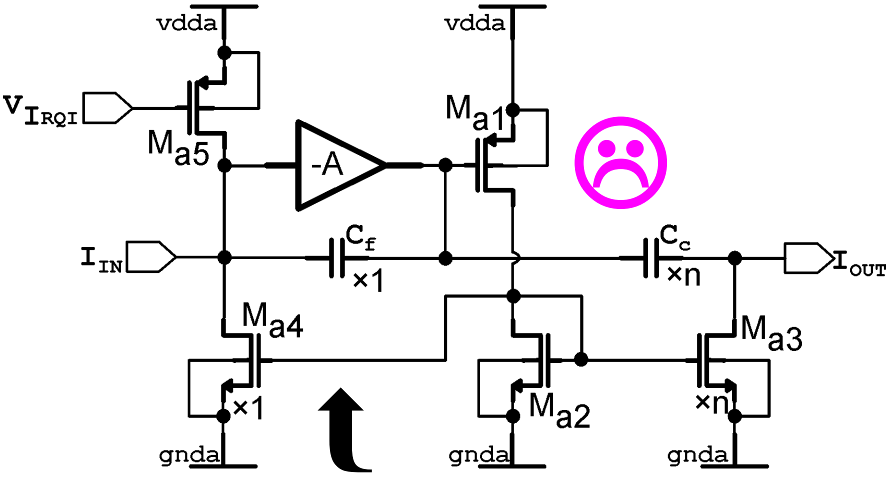
input charge signal multiplication

$$I_{OUT} = n \times I_{IN}$$



Common Gate Feedback (CGF) [4]

- operates in p-z cancellation,
- one-fit-all V_{RFB} is needed,
- Reset Quiescent Current (RQI) is optional; if used, multiplied RQI to next stages ⇒ shift of baseline.



Common Source Feedback (CSF) [5]

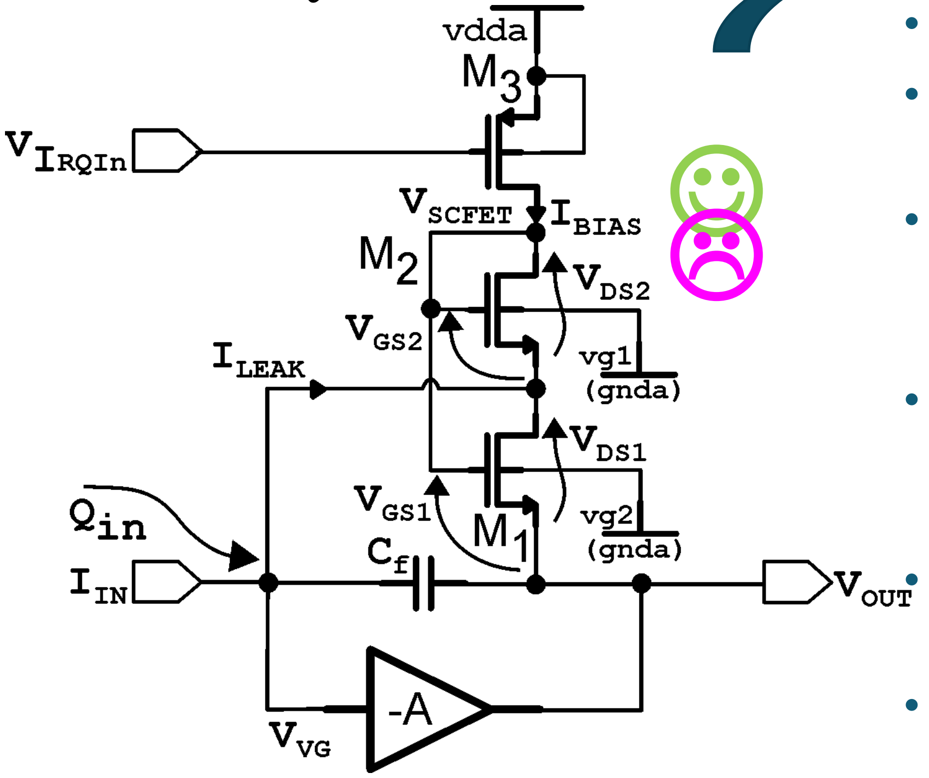
- operates in p-z cancellation,
- RQI (typ. at some pAs) is required, but difficult to control and match,
- larger I_{LEAK}+RQIs ⇒ loss of stability,
- multiplied both RQI and sensor I_{LEAK} to next stages ⇒ shift of baseline.

[1] F. Krummenacher, Nucl. Instrum. Methods Phys. Res., vol. A305, pp. 527-532, 1991,
[2] P.F. Manfredi, et al, Nuclear Physics B - Proceedings Supplements, Vol. 61, Is. 3, February 1998, 532-538
[3] Y. Hu, et al, in IEEE TCAS I, vol. 48, no. 8, pp. 1022-1030, Aug. 2001
[4] G. De Geronimo et al., Nucl. Instr. Meth. A 421 (1999) 322-333
[5] G. De Geronimo et al., IEEE Trans. Nucl. Sci Vol. 51, No. 4, August 2004 1313-1317

all shown for holes

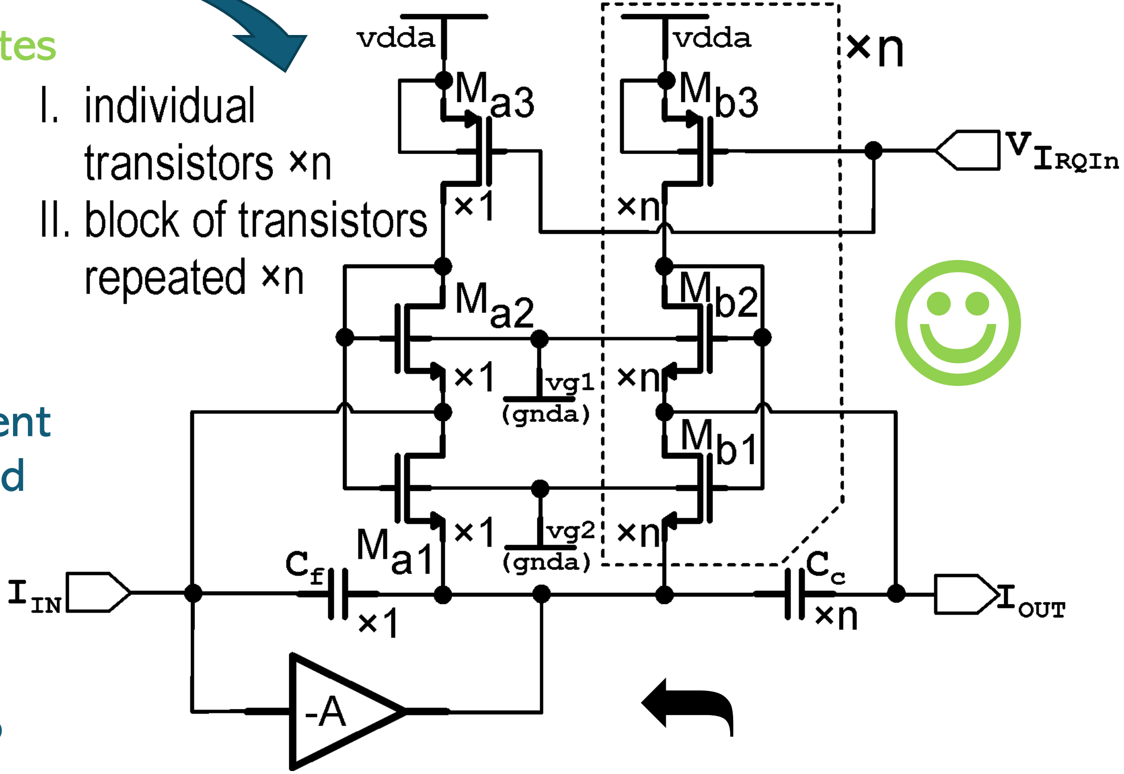
Analog Front-End with SCFET Network (1)

$I_{RQI} =$ a few tens of pA



CSA with Self-Cascoded Field-Effect Transistor (SCFET) feedback network;

- feedback self-regulates
- configurable to p-z cancellation,
- no increase in order of feedback loop ➲ stable
- reset quiescent current (RQI) is not multiplied to next stages
- no stabilization capacitance needed
- V_{DS1} almost equal to zero



I. individual transistors ×n

II. block of transistors repeated ×n

CSA with (SCFET) configured in pole-zero cancellation, ➲ multiplication (gain) of input charge × **n**;

$$V_{DS1} \approx \frac{kT}{q} \cdot \ln\left(1 + \frac{\left({}^{W}/_{L}\right)_{M_2}}{\left({}^{W}/_{L}\right)_{M_1}} \cdot \frac{I_{DS,M_1}}{I_{DS,M_2}}\right)$$

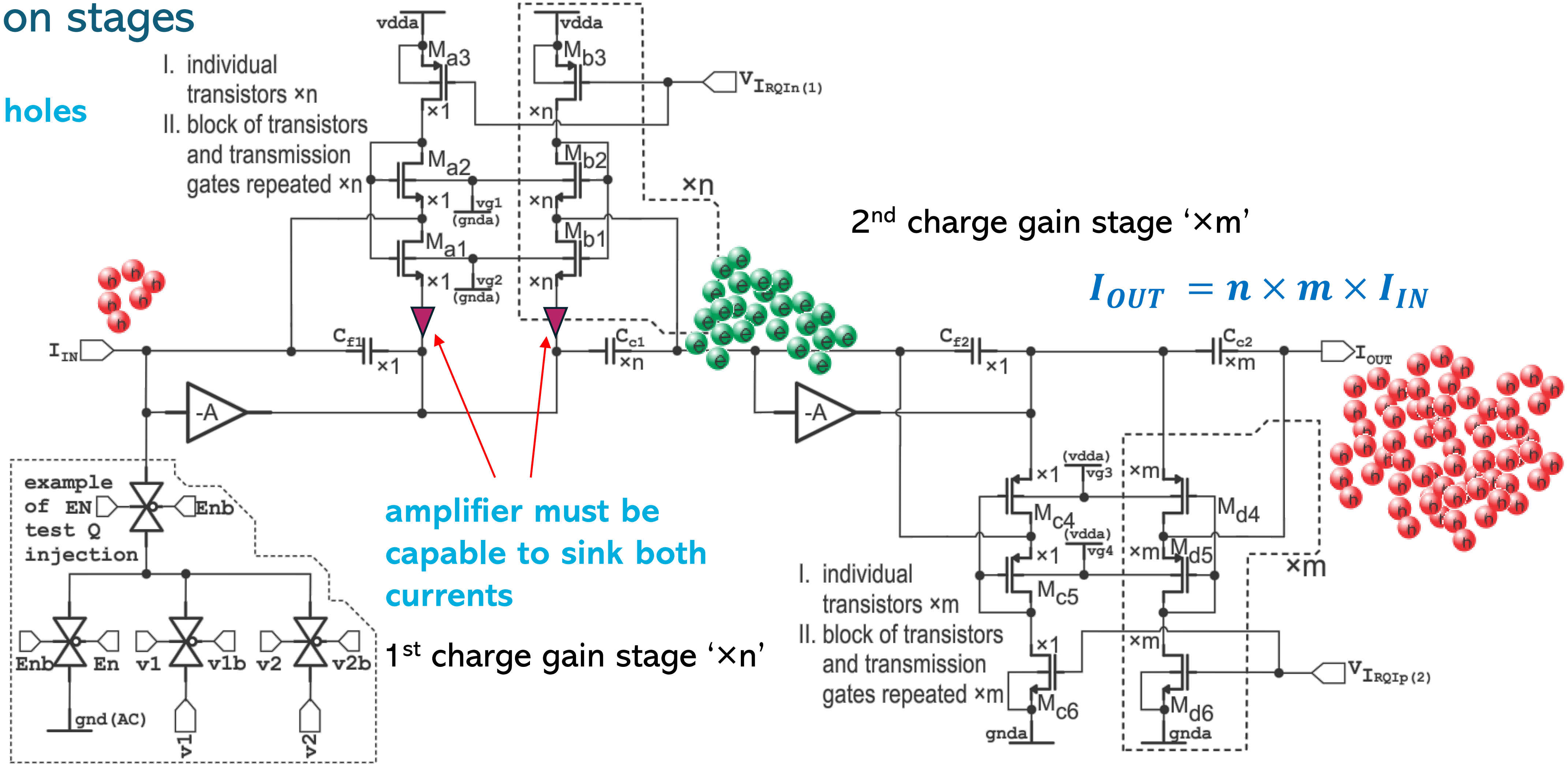
temperature dependence cancels in p-z;

all shown for holes

Analog Front-End with SCFET Network (2)

cascading of charge multiplication stages

input charge: holes



I. individual transistors ×n

II. block of transistors and transmission gates repeated ×n

×n

2nd charge gain stage '×m'

$$I_{OUT} = n \times m \times I_{IN}$$

amplifier must be capable to sink both currents

1st charge gain stage '×n'

I. individual transistors ×m

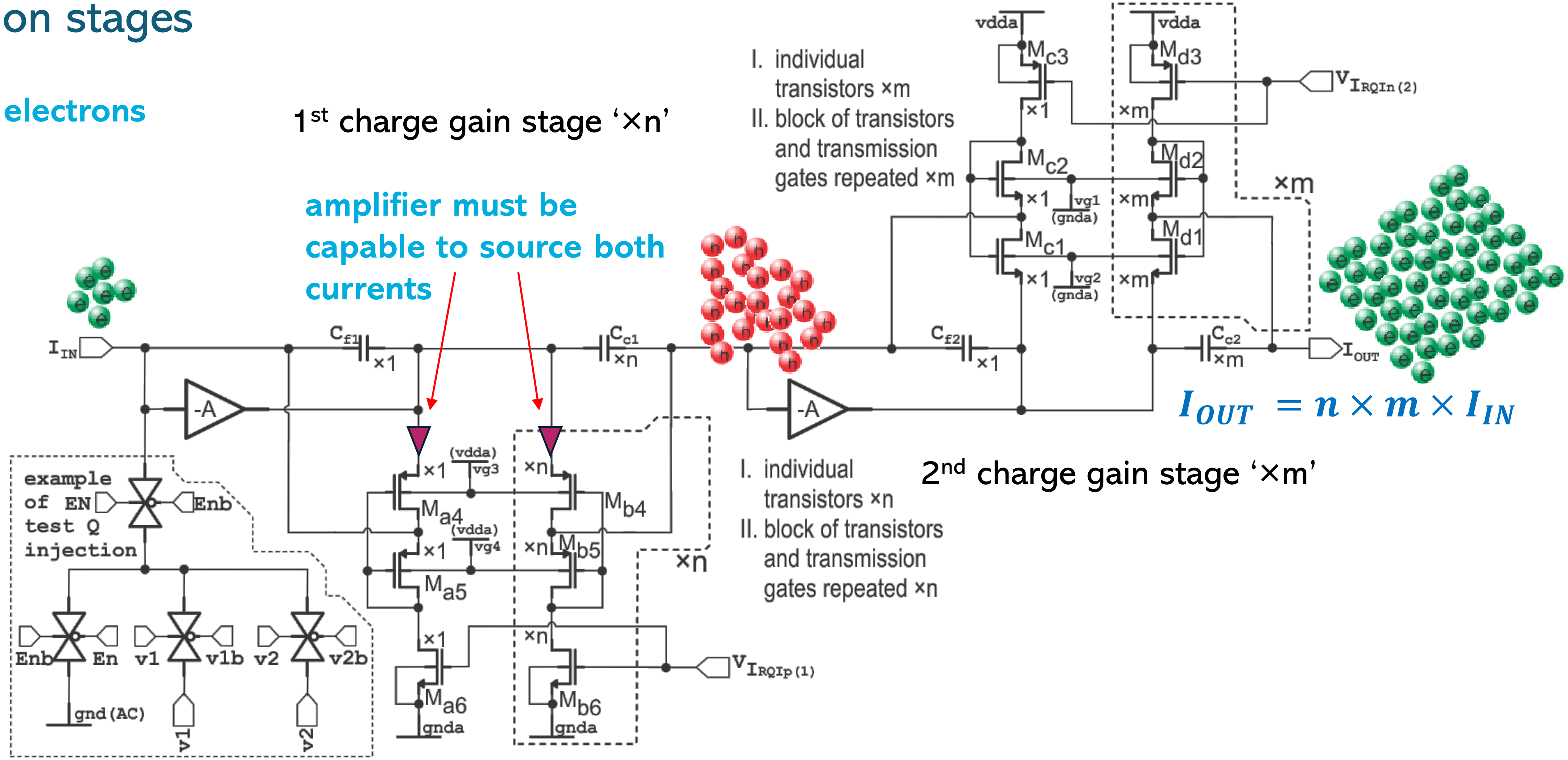
II. block of transistors and transmission gates repeated ×m

×m

Analog Front-End with SCFET Network (3)

cascading of charge multiplication stages

input charge: electrons



1st charge gain stage ‘×n’

amplifier must be capable to source both currents

I. individual transistors ×m
II. block of transistors and transmission gates repeated ×m

I. individual transistors ×n
II. block of transistors and transmission gates repeated ×n

2nd charge gain stage ‘×m’

$$I_{OUT} = n \times m \times I_{IN}$$

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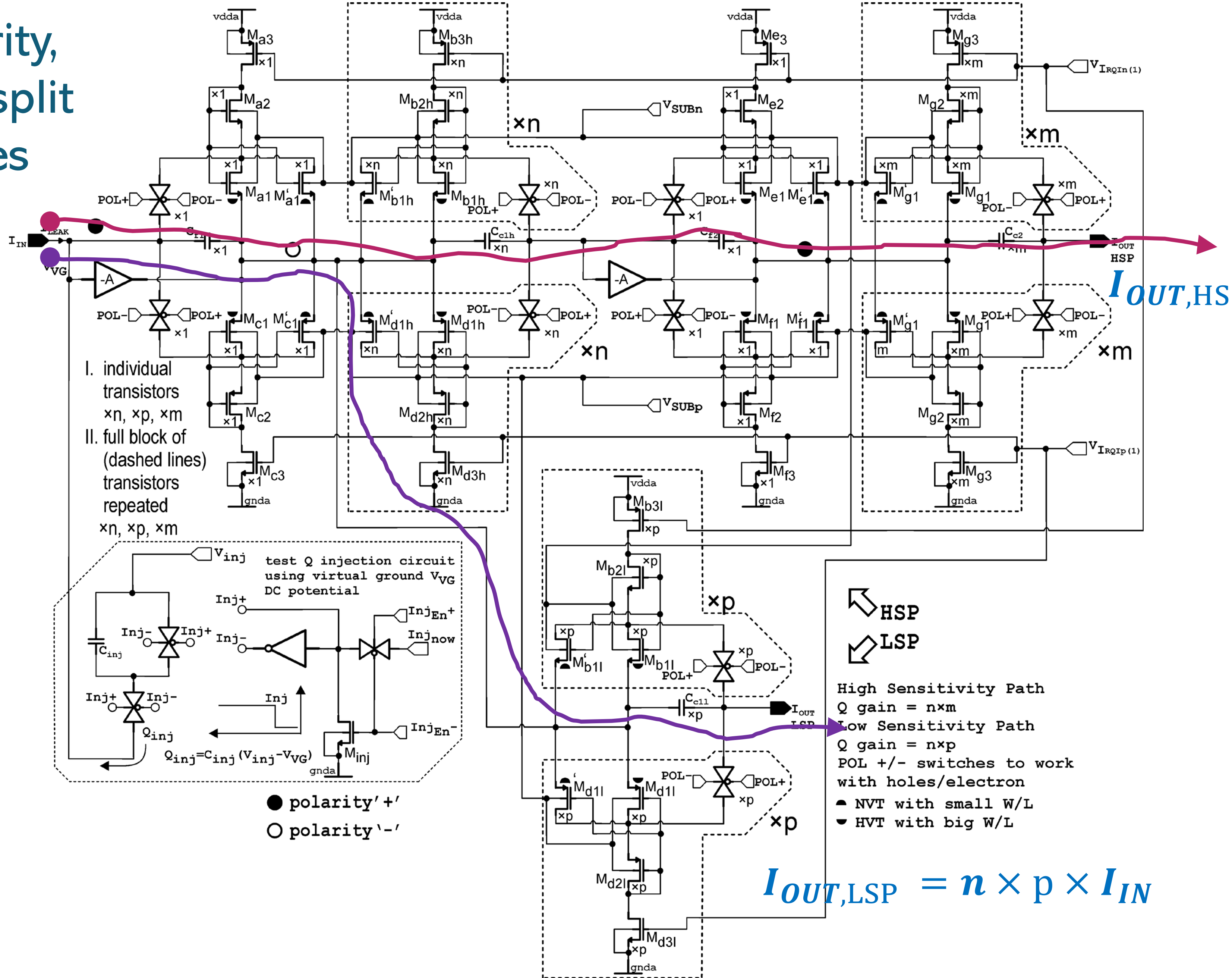
Analog Front-End with SCFET Network (4)

selectable polarity, cascading and split sensitivity stages



I. individual transistors ×n, ×p, ×m
II. full block of (dashed lines) transistors repeated ×n, ×p, ×m

test Q injection circuit using virtual ground V_{VG} DC potential

$Q_{inj}=C_{inj}(V_{inj}-V_{VG})$

● polarity'+'
○ polarity'-'

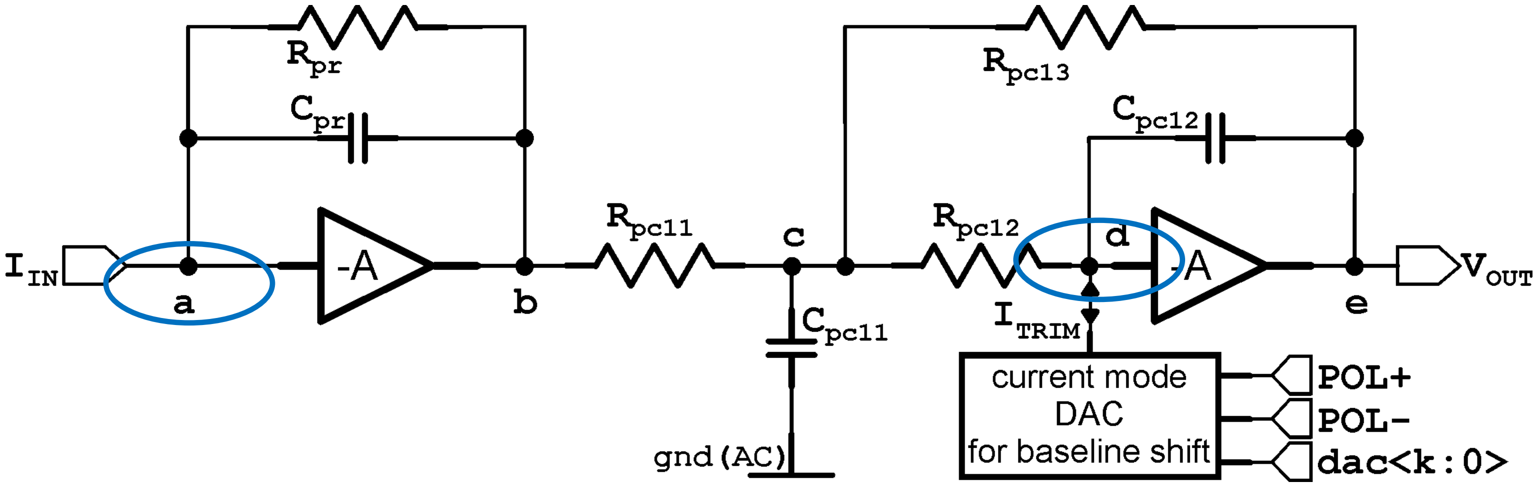
HSP
LSP

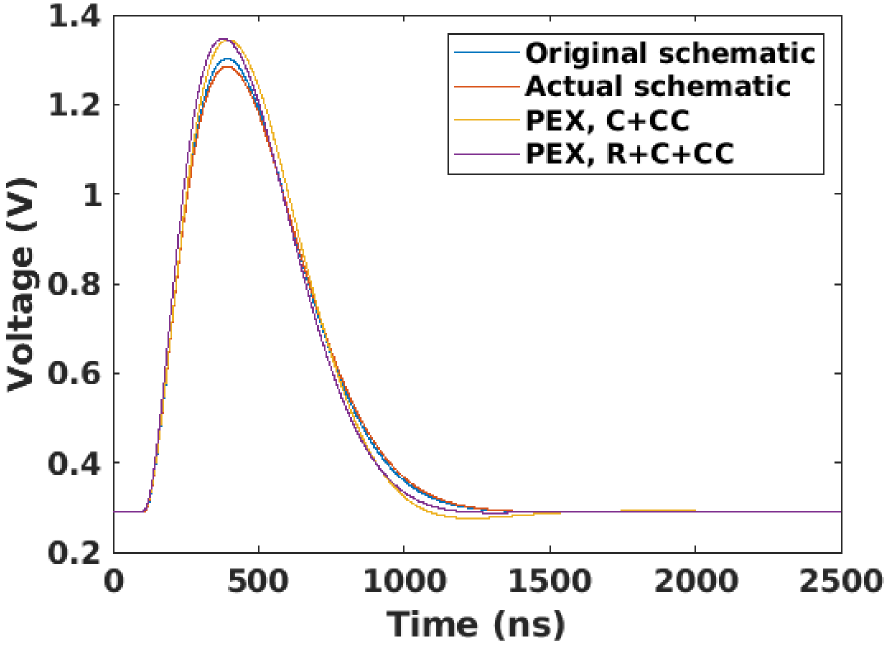
High Sensitivity Path
Q gain = n×m
Low Sensitivity Path
Q gain = n×p
POL +/- switches to work with holes/electron
NVT with small W/L
HVT with big W/L

$$I_{OUT,\mathrm{HSP}} = n \times m \times I_{IN}$$

$$I_{OUT,\mathrm{LSP}} = n \times \mathrm{p} \times I_{IN}$$

Analog Front-End with SCFET Network - Filtering





- 3rd order, 1-real + 2-complex conjugate poles [6], τ_p=300 ns
- baseline adjustment via current-mode DAC (7.5 bit equiv. +1 bit for polarity setting DAC – k=8)
- DAC current is injected into node ‘d’ for noise performance
- IR drop across $R_{pc12} \Rightarrow$ shifts of baseline.

$$H_t(s) = \frac{1}{s}\frac{-sC_cR_{pr}}{sC_{pr}R_{pr}+1}\frac{1}{s^2C_{pc11}C_{pc12}R_{pc12}R_{pc13}+sC_{pc12}R_{pc12}\left(1+\frac{R_{pc13}}{R_{pc11}}+\frac{R_{pc13}}{R_{pc12}}\right)+1} = \frac{-sC_cR_{pr}}{sC_{pr}R_{pr}+1}\frac{-A_v}{\frac{s^2}{\omega_0^2}+\frac{s}{\omega_0 Q}+1}$$

C_c is coupling capacitance for the last stage of the CSA

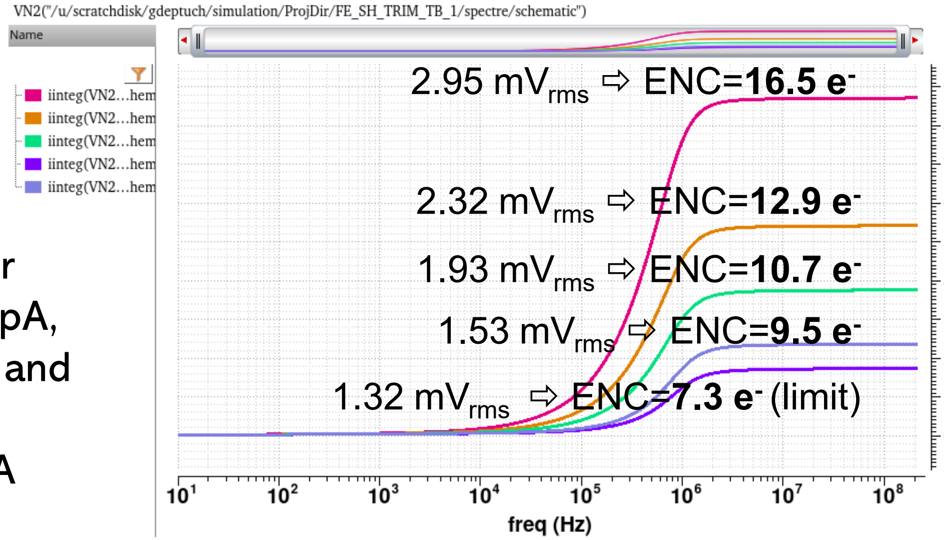
R_{pr} = 571.6 kΩ, C_{pr} = 304.0 fF, R_{pc11} = 183.2 kΩ /7 = 26.17 kΩ, C_{pc11} = 4.52 pF, R_{pc12} = 183.2 kΩ, C_{pc12} = 304.0 fF / 2 =152.0 fF, R_{pc13} = 183.2 kΩ,
I current DAC = ±250 nA (baseline) + 1 μA (polarity)

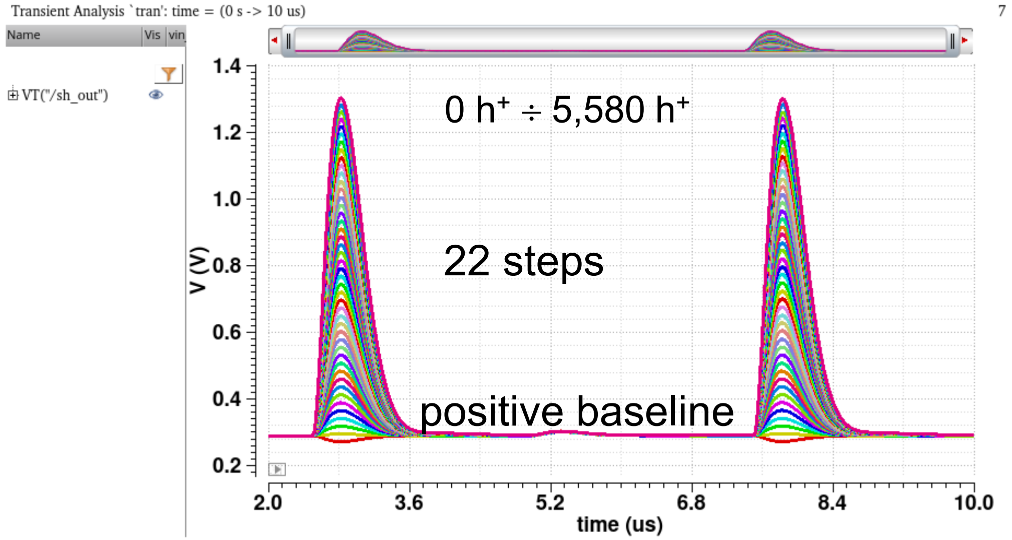
[6] G. De Geronimo and S. Li, in IEEE Transactions on Nuclear Science, vol. 58, no. 5, pp. 2382-2390, Oct. 2011

Simulation Results

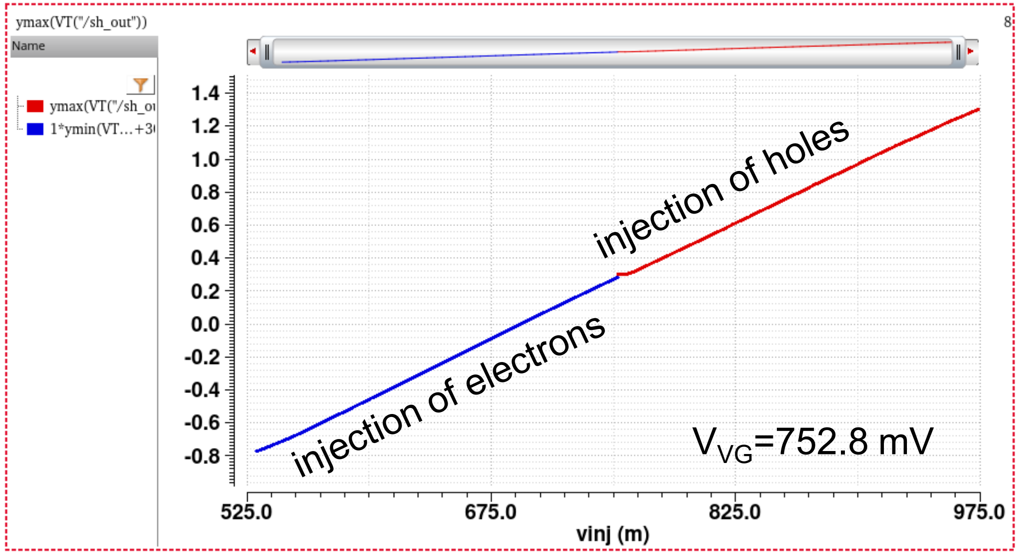
two-stage CSA ➲ charge multiplication $I_{OUT}=12\times12\times I_{IN}$, with $C_{f1}=4$ fF, $C_{c1}=12\times4$ fF, $C_{f2}=40$ fF and $C_{c2}=12\times40$ fF and semigaussian shaping filter (1RP2CCP) $\tau_p=300$ ns; C_{DET} = 50 fF, VDDA=1.5 V, I_{bias}=~50 μA/OTA stage.

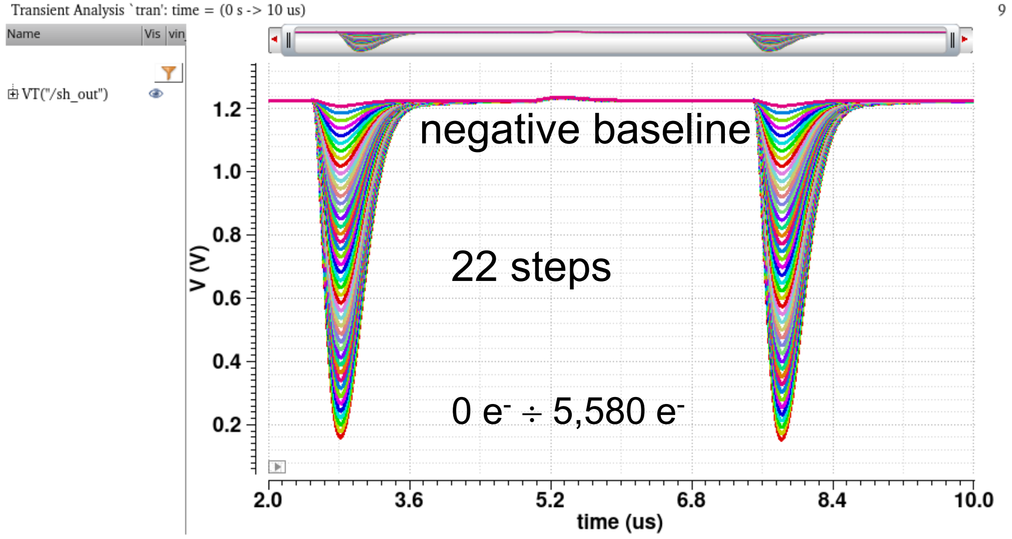
AC noise simulation for positive polarity for 0 pA, 2 pA, 12.5 pA, 25 pA and 50 pA current biasing SCFET feedback in CSA





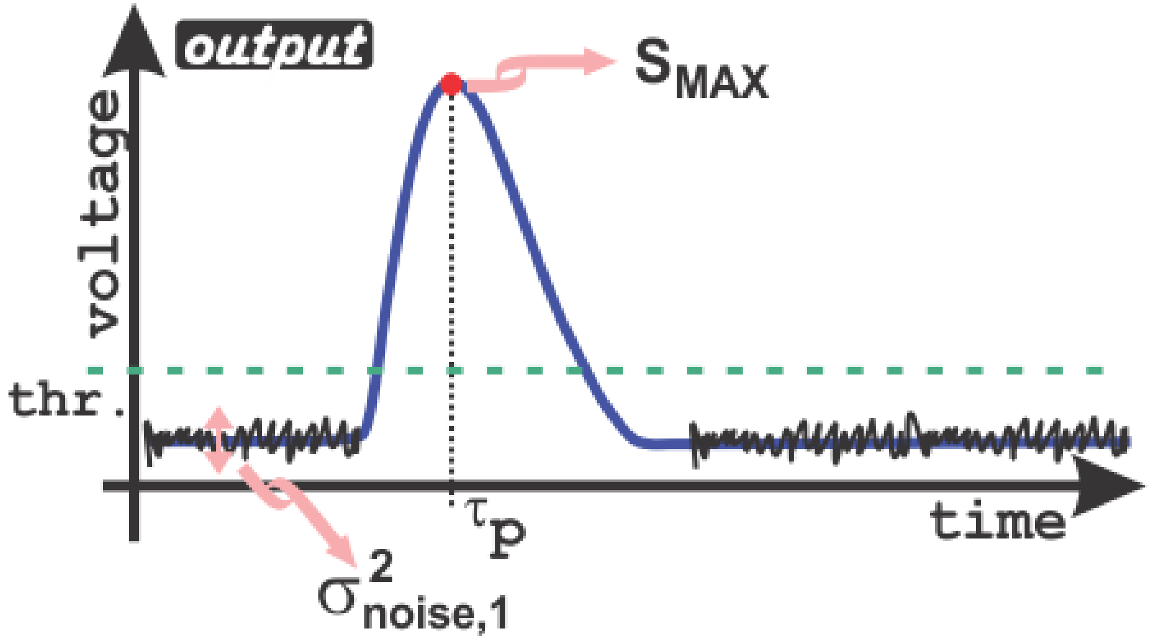
linearity for positive and negative signals obtained separately

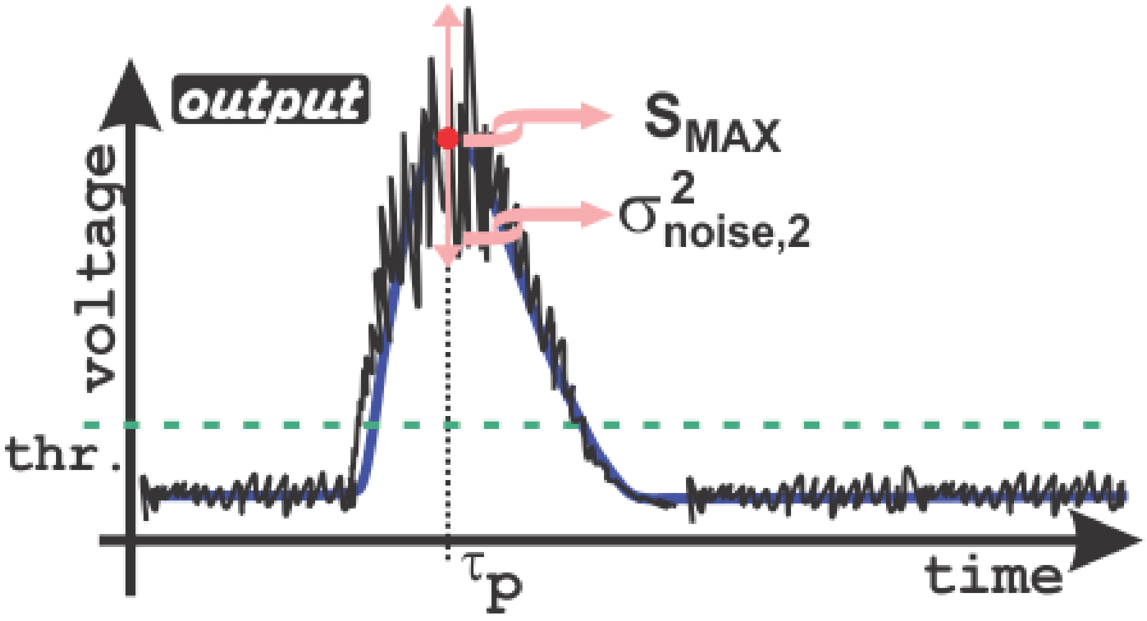




Reporting of Noise for CSA with Active Circuitry in Feedback (1)

SNR REPORTING





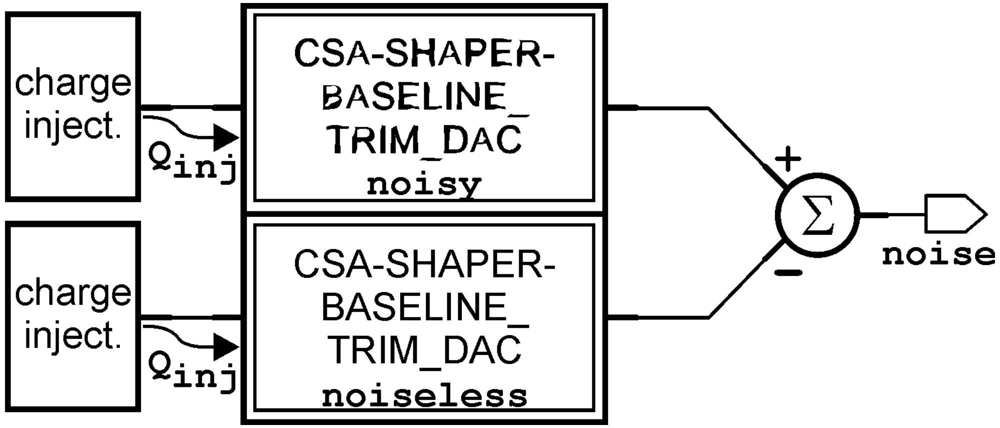
$$\mathrm{SNR}_1 = \mathrm{S_{MAX}}/\sqrt{\sigma^2_{\mathrm{noise},1}} > \mathrm{SNR}_2 = \mathrm{S_{MAX}}/\sqrt{\sigma^2_{\mathrm{noise},2}}$$

often lower SNR measured,
assigned to poor simulation
models, charge collection inefficiency…

Which one is correct, honest?

Reporting of Noise for CSA with Active Circuitry in Feedback (2)

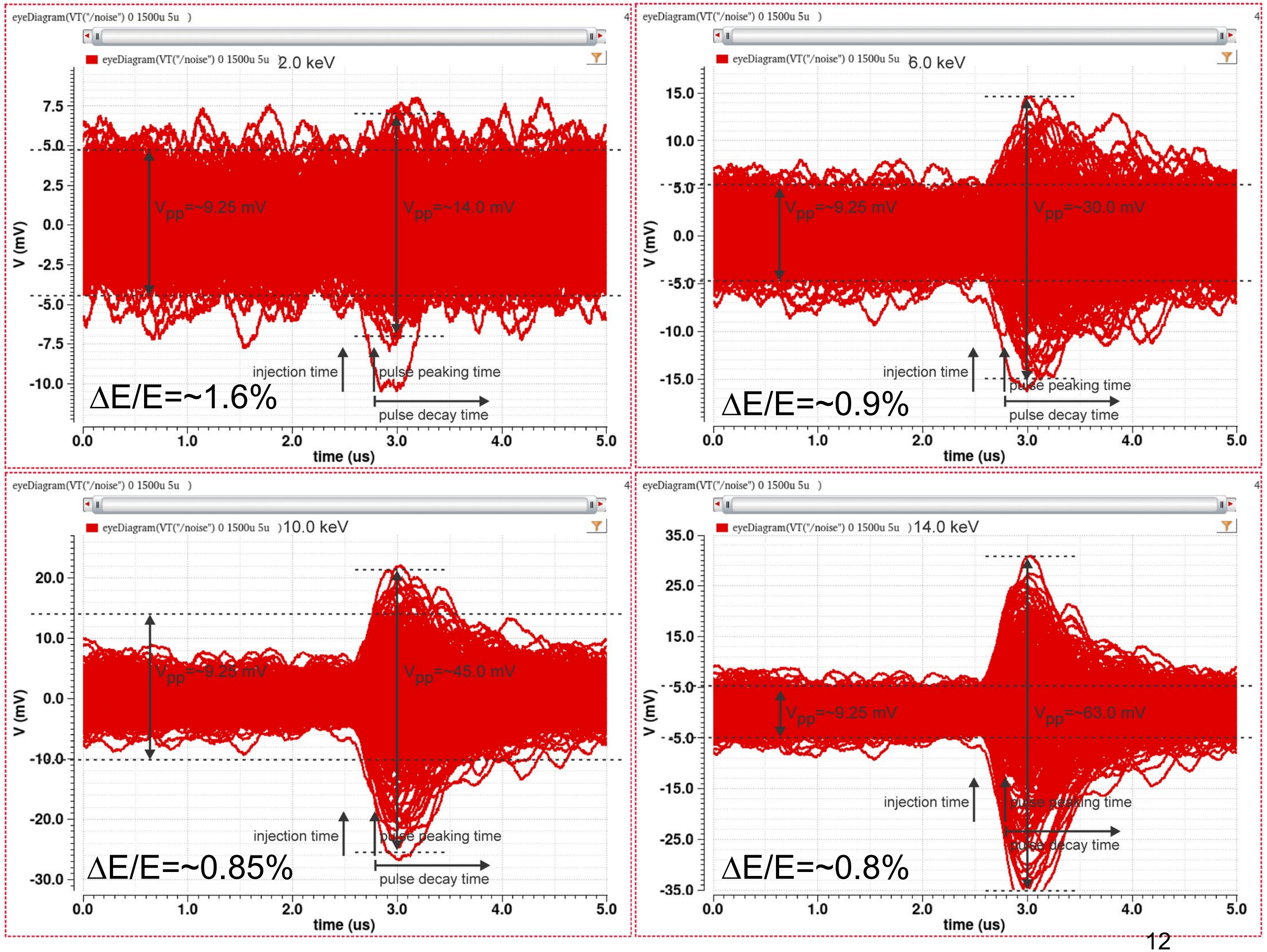
Often SNR is incorrectly reported as
As ratio of pulse amplitude (transient sim.)
to rms at not signal (AC noise sim.)



Simulation test setup for estimation
of noise (SNR and DE/E)

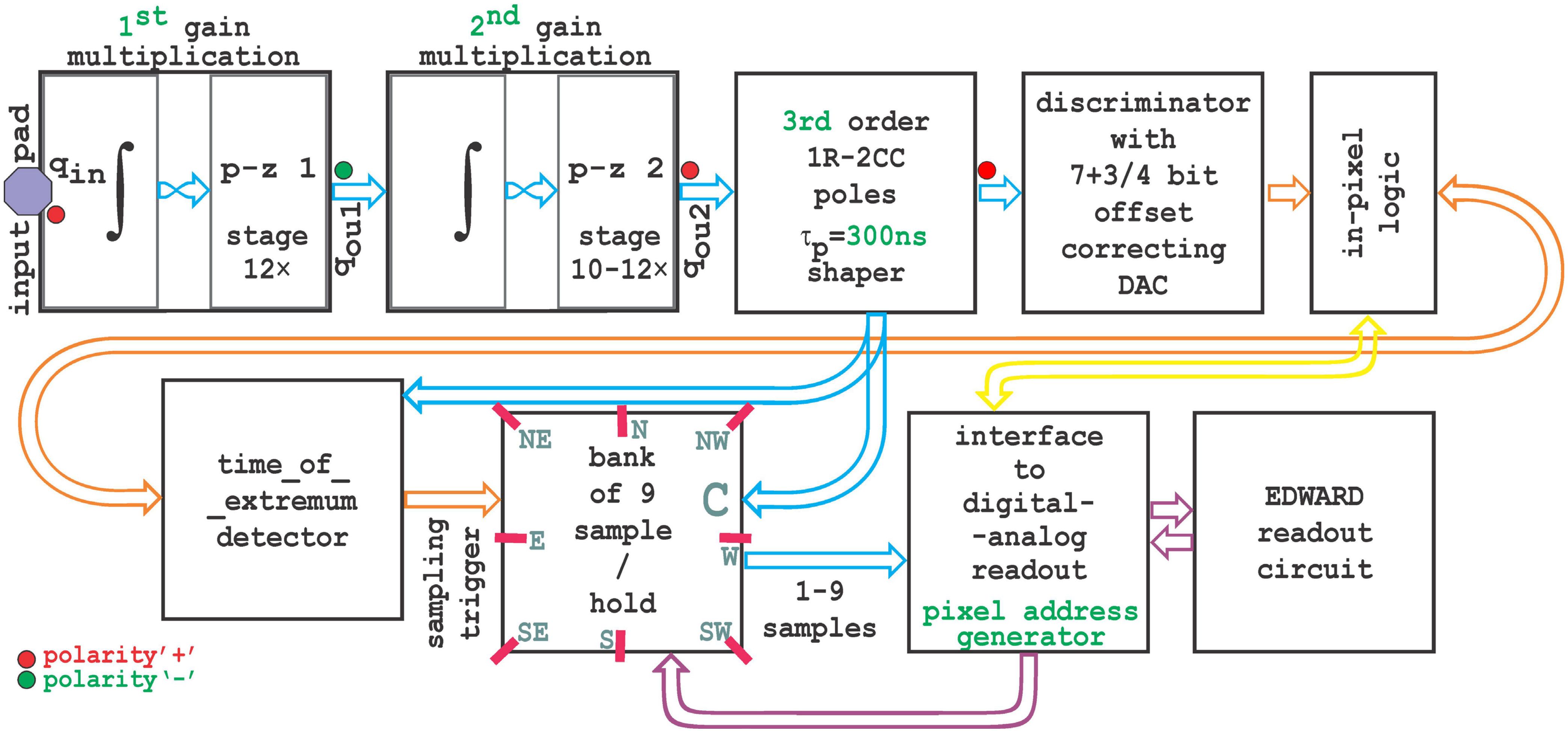
- feedback path of CSA: passive, i.e., capacitors, and active, i.e., transistors (bias << transient currents).
- FE circuit transfer function is non-nonstationary ➲ noise (variance at specific points of time series data) needs to be assessed using transient noise simulation,

1.5 ms long simulations - injections every 5 ms
(max noise frequency 250 MHz)
presented in ‘eyeDiagram’ mode with period of 5 ms

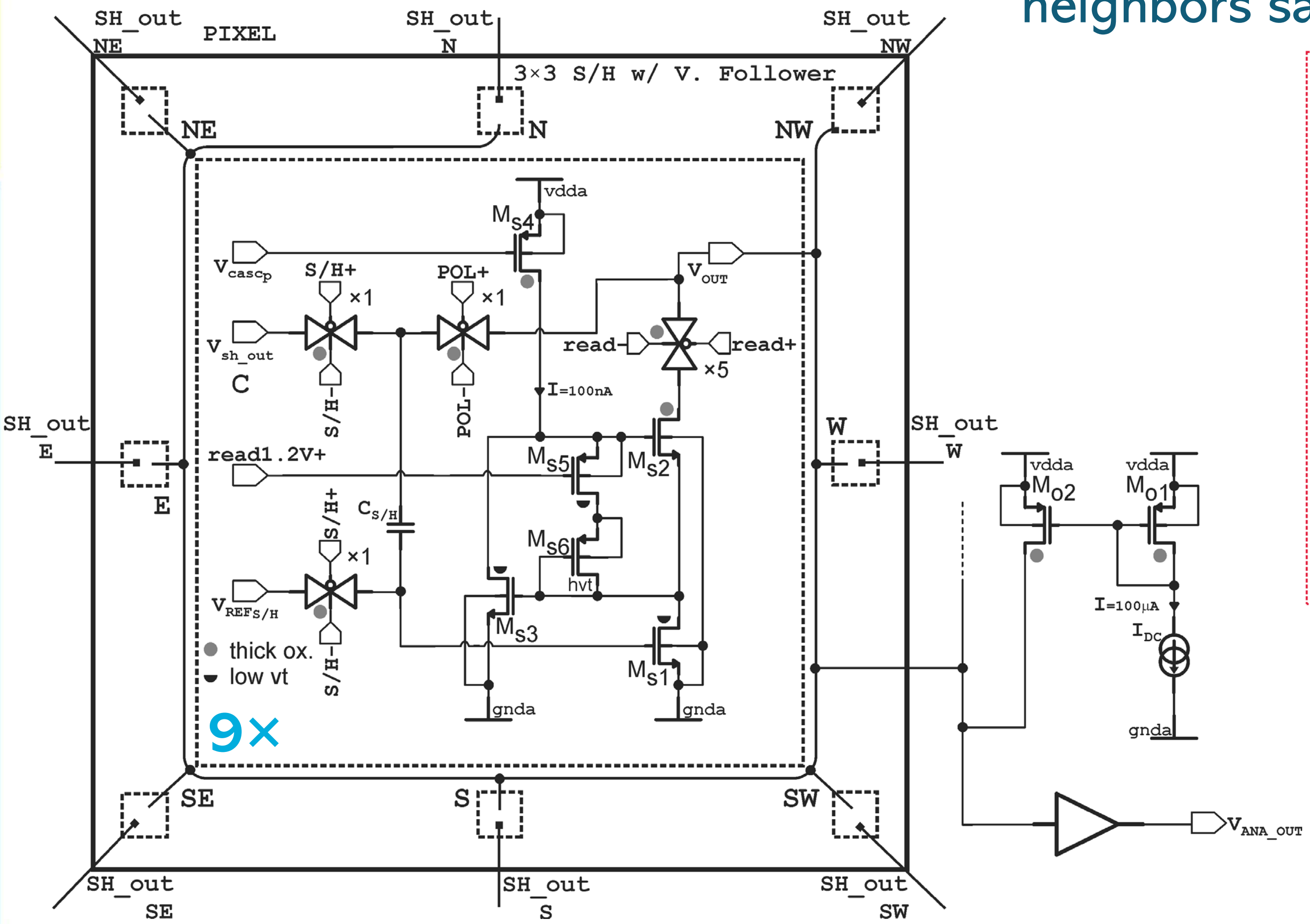


Processing Chain

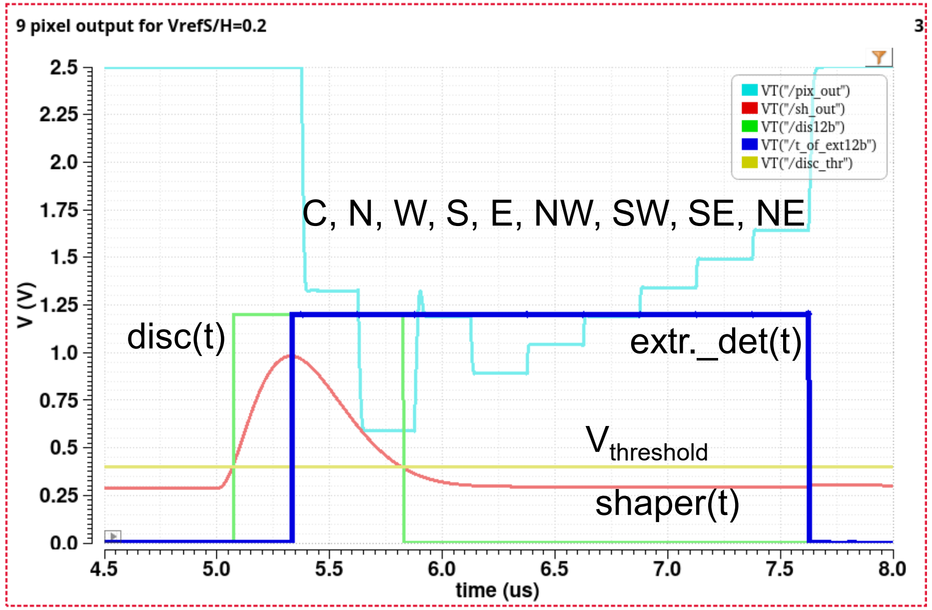
Pixels with AMPlitude and Event-Driven readout

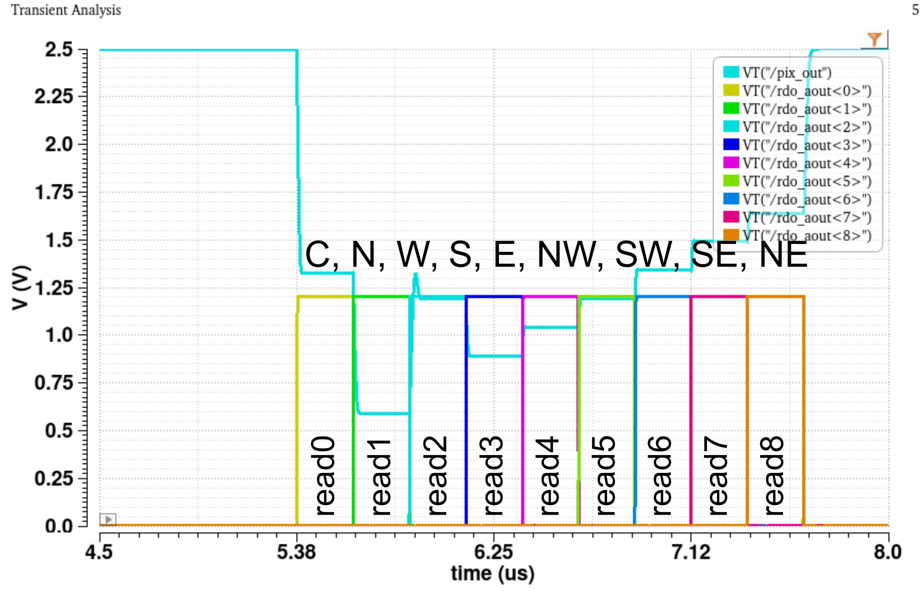


Bank of 9 Sample and Hold Circuits



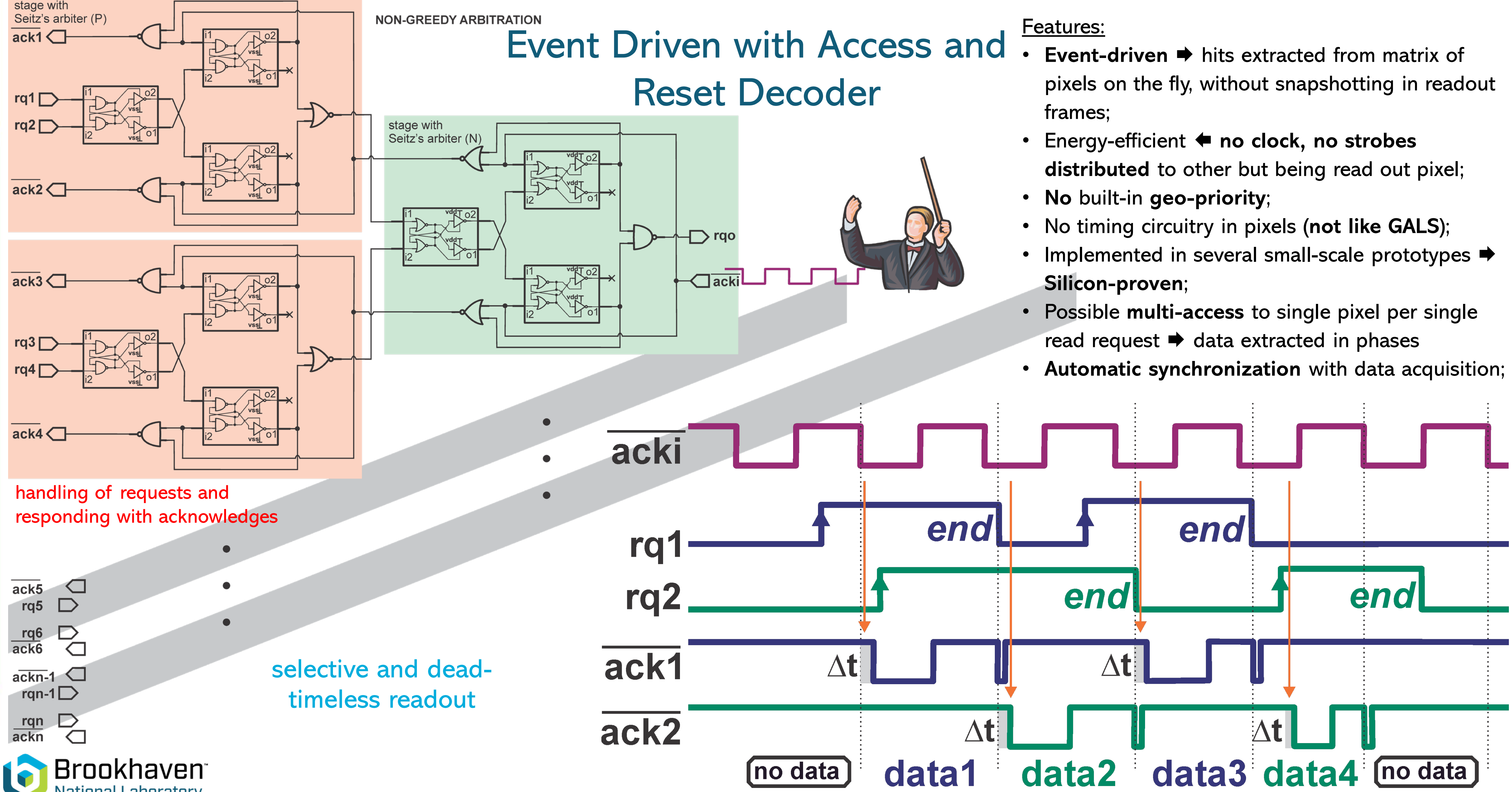
neighbors sampled together with peaked central pixel





- source follower = variable gain, typically <1, unless complicated architectures [US Patent No 11,108,981 B2]
- CommonSource with the S/H capacitor in feedback path is used.

Event Driven Readout – Suitable for Fluorescence Imaging



NON-GREEDY ARBITRATION

Event Driven with Access and Reset Decoder

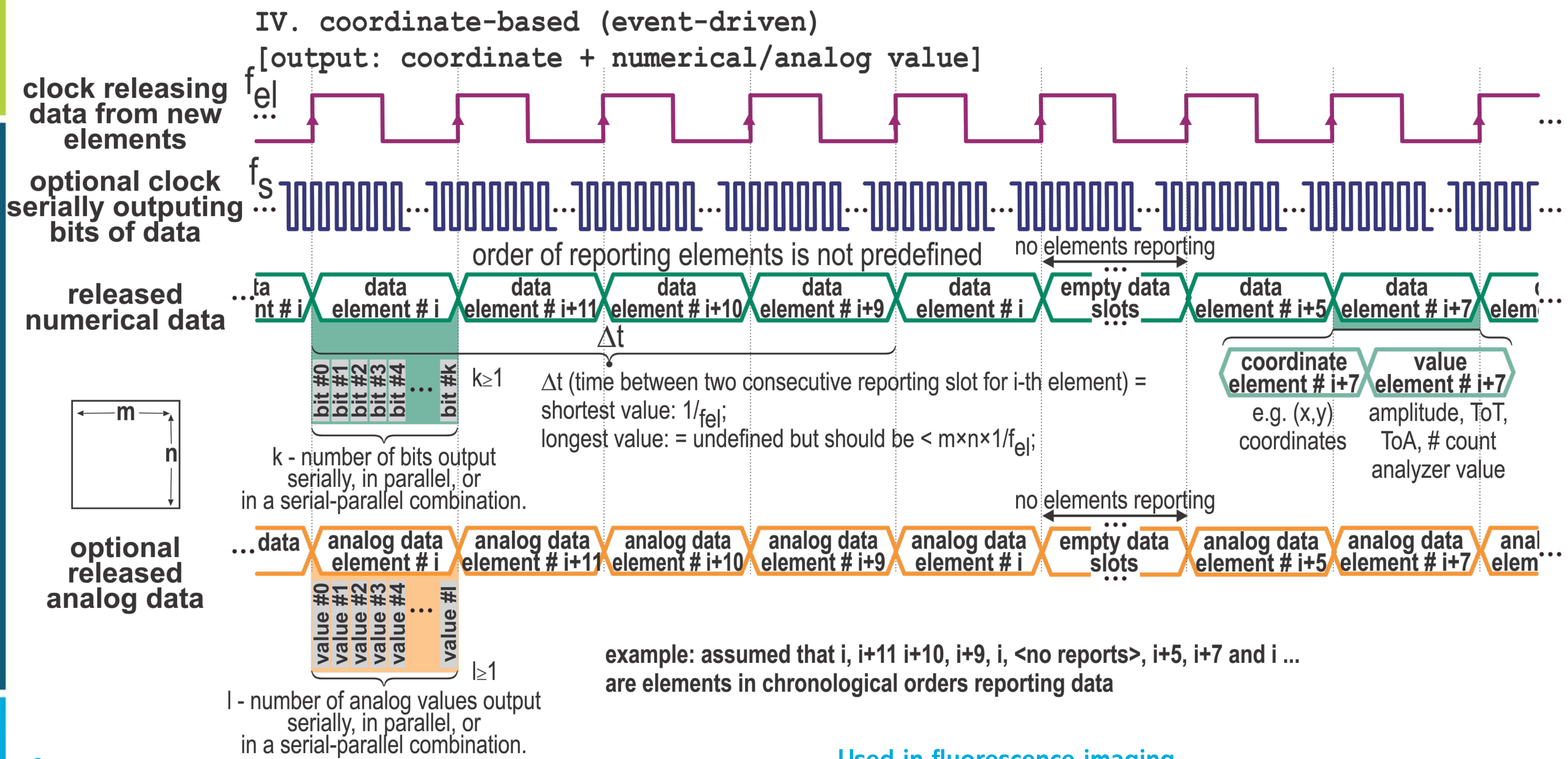
handling of requests and responding with acknowledges

selective and dead-timeless readout

Features:

- **Event-driven** ➡ hits extracted from matrix of pixels on the fly, without snapshotting in readout frames;
- Energy-efficient ⬅ **no clock, no strobes distributed** to other but being read out pixel;
- **No** built-in **geo-priority**;
- No timing circuitry in pixels (**not like GALS**);
- Implemented in several small-scale prototypes ➡ **Silicon-proven**;
- Possible **multi-access** to single pixel per single read request ➡ data extracted in phases
- **Automatic synchronization** with data acquisition;

Comparison: Event Driven with All Data



k - number of bits output serially, in parallel, or in a serial-parallel combination.

Δt (time between two consecutive reporting slot for i-th element) =
shortest value: $1/f_{el}$;
longest value: = undefined but should be < $m \times n \times 1/f_{el}$;

l - number of analog values output serially, in parallel, or in a serial-parallel combination.

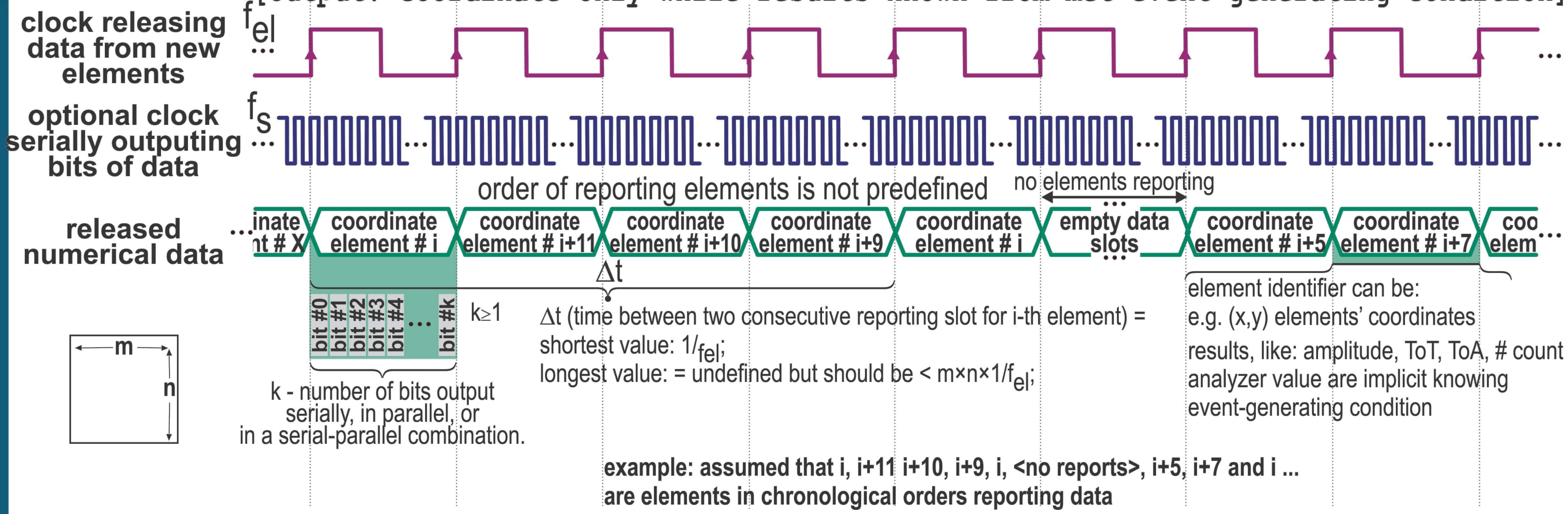
example: assumed that i, i+11 i+10, i+9, i, <no reports>, i+5, i+7 and i ...
are elements in chronological orders reporting data

Used in fluorescence imaging

Comparison: Even Driven without Data

V. coordinate-based (event-driven)

[output: coordinate only while results known from met event-generating condition]



order of reporting elements is not predefined

Δt (time between two consecutive reporting slot for i-th element) =

shortest value: $1/f_{el}$;

longest value: = undefined but should be < $m \times n \times 1/f_{el}$;

k - number of bits output serially, in parallel, or in a serial-parallel combination.

element identifier can be:

e.g. (x,y) elements' coordinates

results, like: amplitude, ToT, ToA, # count analyzer value are implicit knowing event-generating condition

example: assumed that i, i+11 i+10, i+9, i, <no reports>, i+5, i+7 and i ... are elements in chronological orders reporting data

May be used in photon counting: identifier of an even tells all about data

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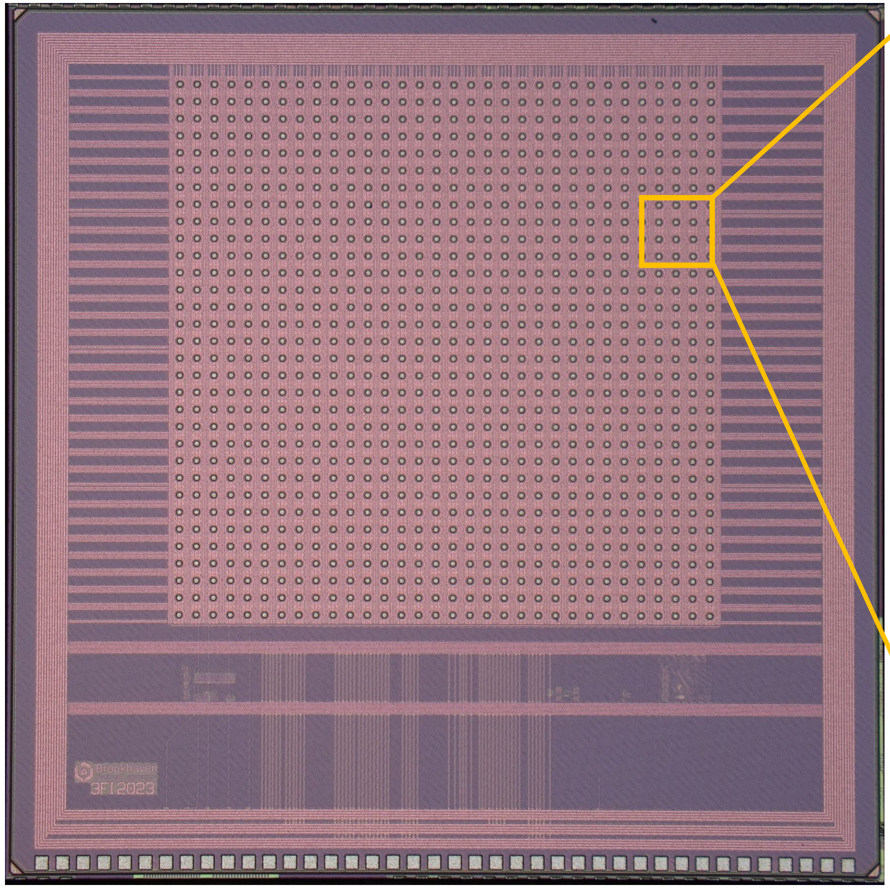
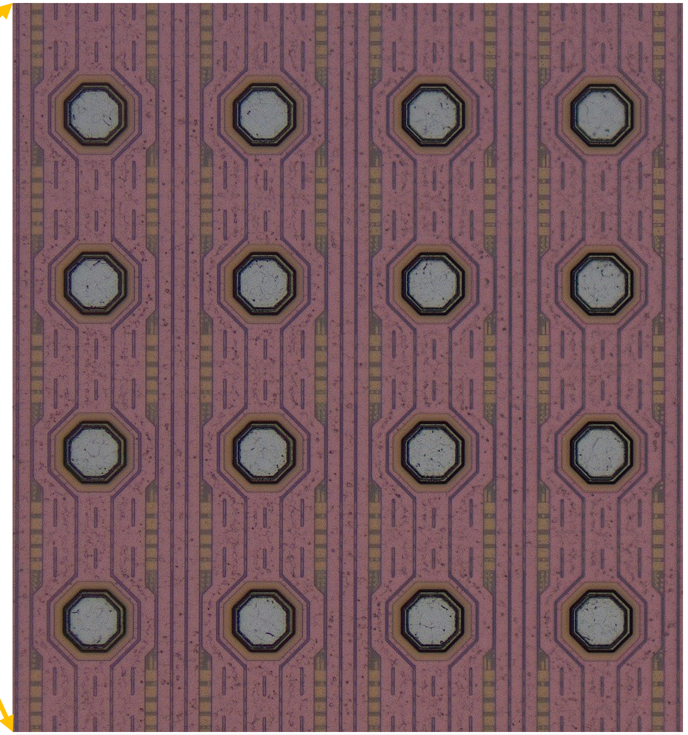
Prototype ASIC – 3FI



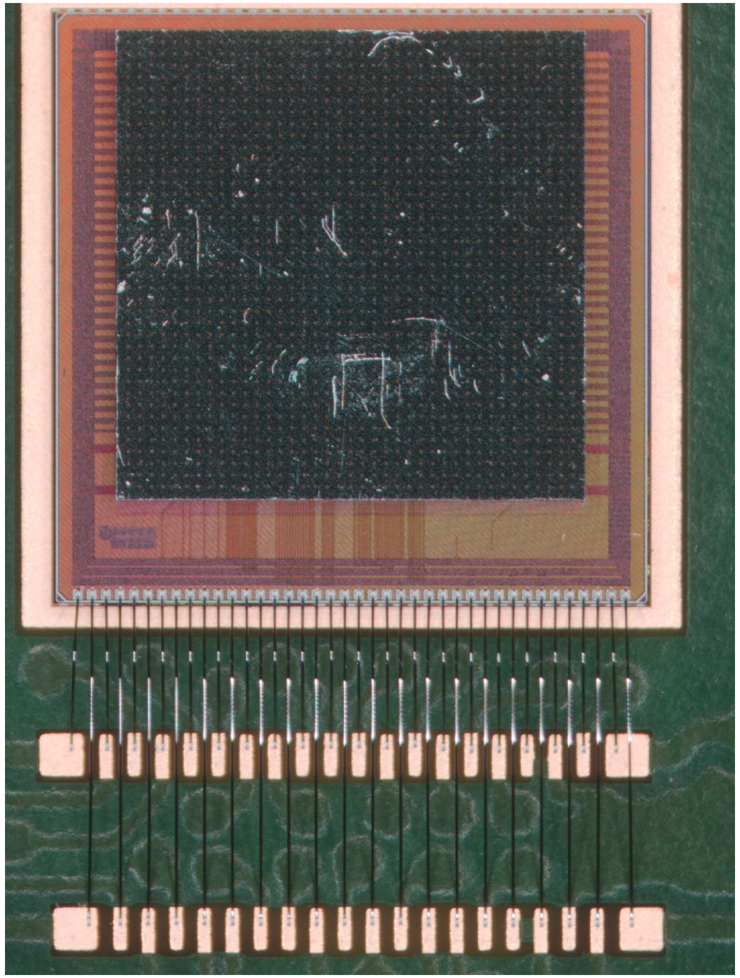
Full Field Fluorescence Imaging - 3FI ASIC:
Tender X-ray Spectroscopy
100×100 μm^2 square pixels
2 keV – 16 keV single gain path
32×32 pixels 65 nm CMOS process
Silicon sensor



30 μm bump-bonding pads on 100 μm pitch

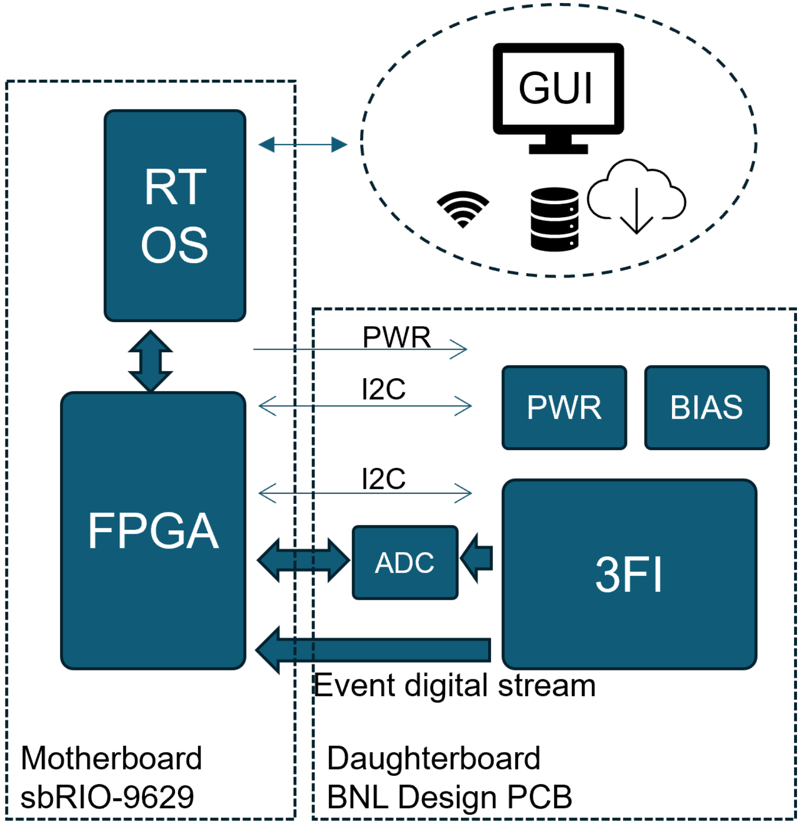
Power supplies:

- analog FE = 1.5 V
- analog discriminator, extremum (peak) detector and S/H = 2.0 ÷ 2.5 V
- digital (event driven readout) = 1.2 V



3FI ASIC with bump bonded Si sensor

Measurement Results – Test Setup


GUI

RT OS

FPGA

PWR

I2C

I2C

PWR

BIAS

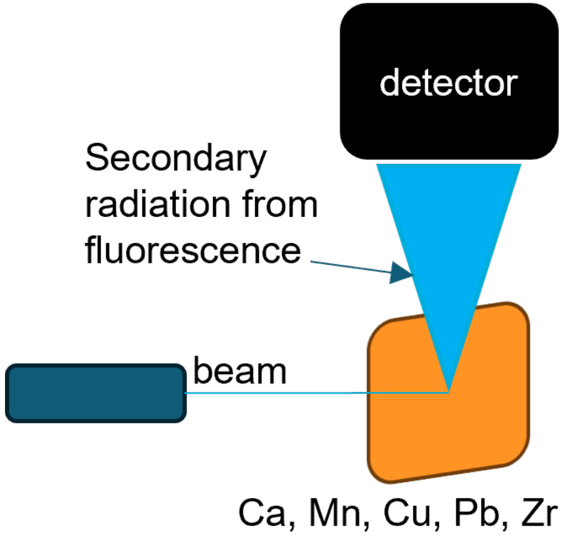
ADC

3FI

Event digital stream

Motherboard
sbRIO-9629

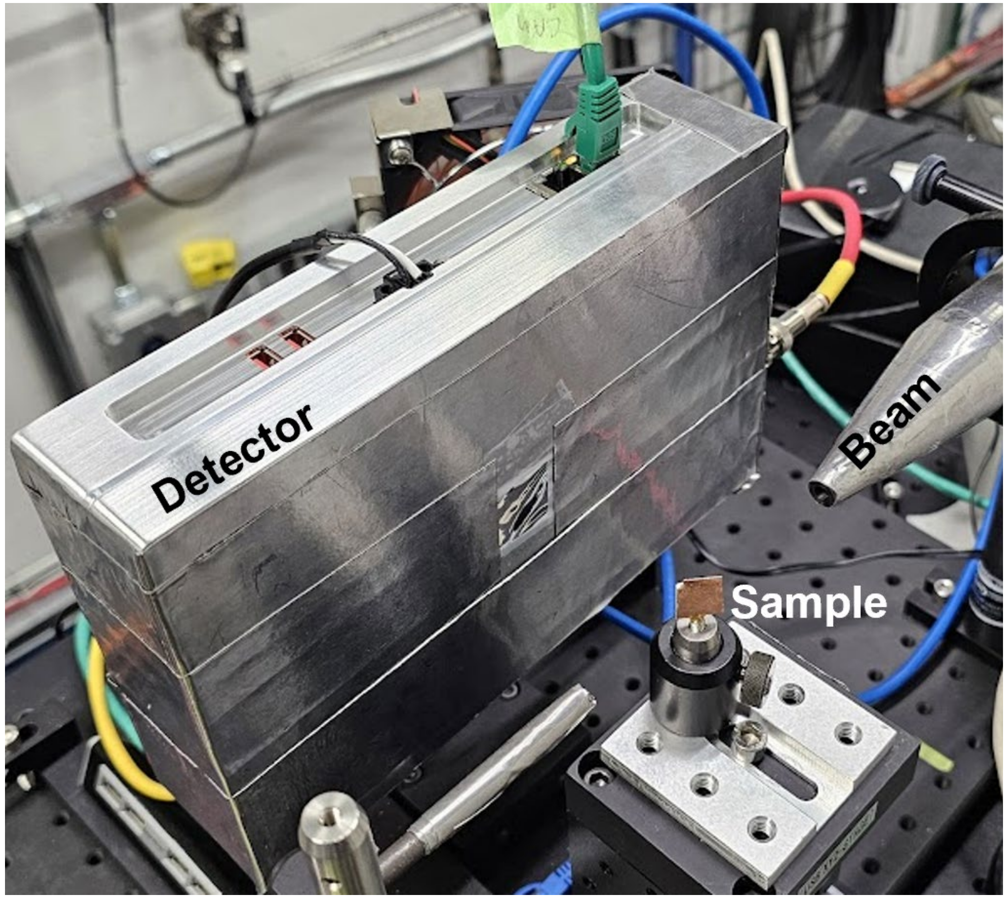
Daughterboard
BNL Design PCB


detector

Secondary radiation from fluorescence

beam

Ca, Mn, Cu, Pb, Zr



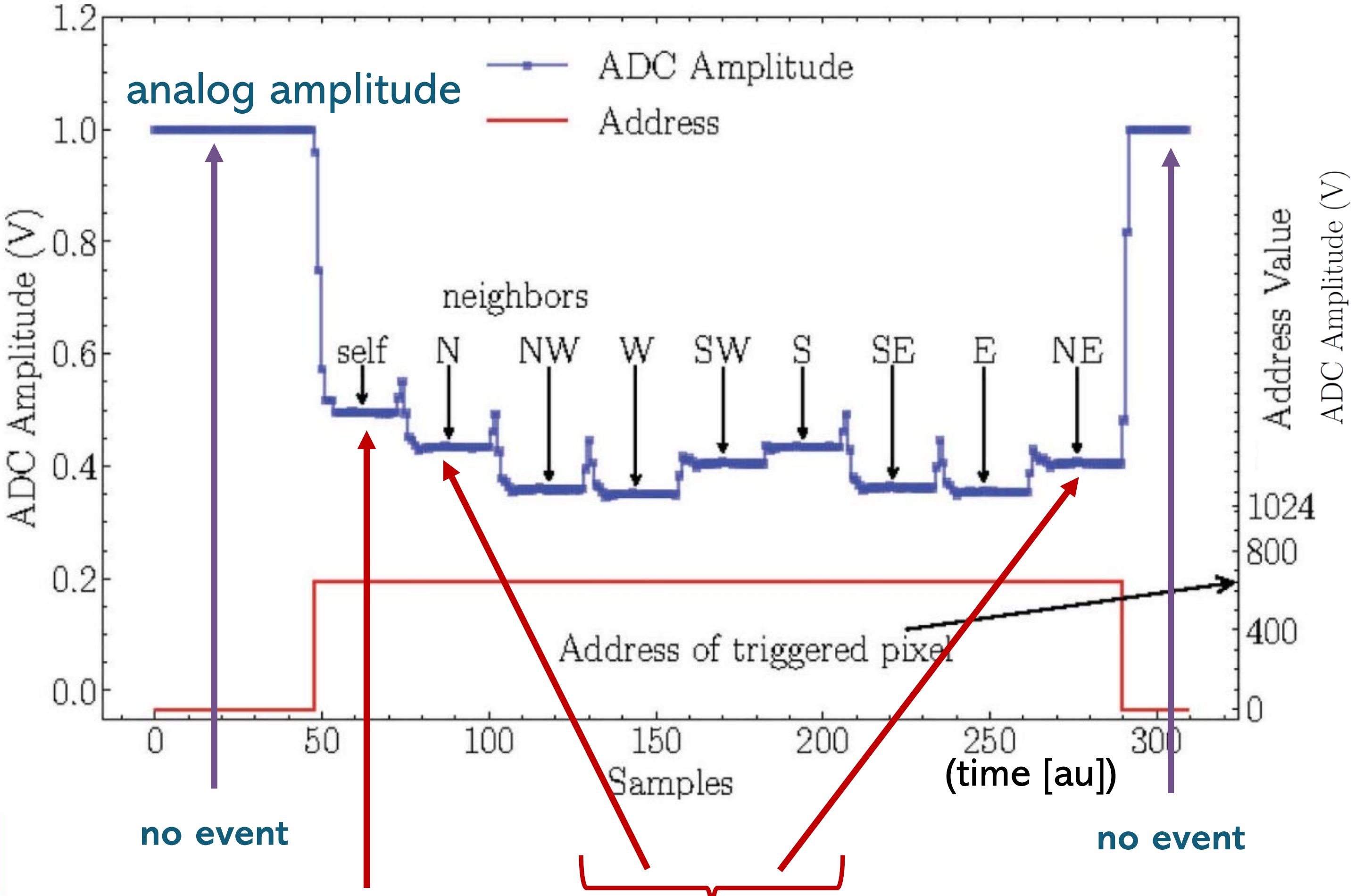
test setup and data processing/acquisition NI / LabView

illumination of detector with fluorescence X-rays

setup on 17-BM of NSLS-II

Measurement Results (1)

central pixel and neighbors (for each event)



no event

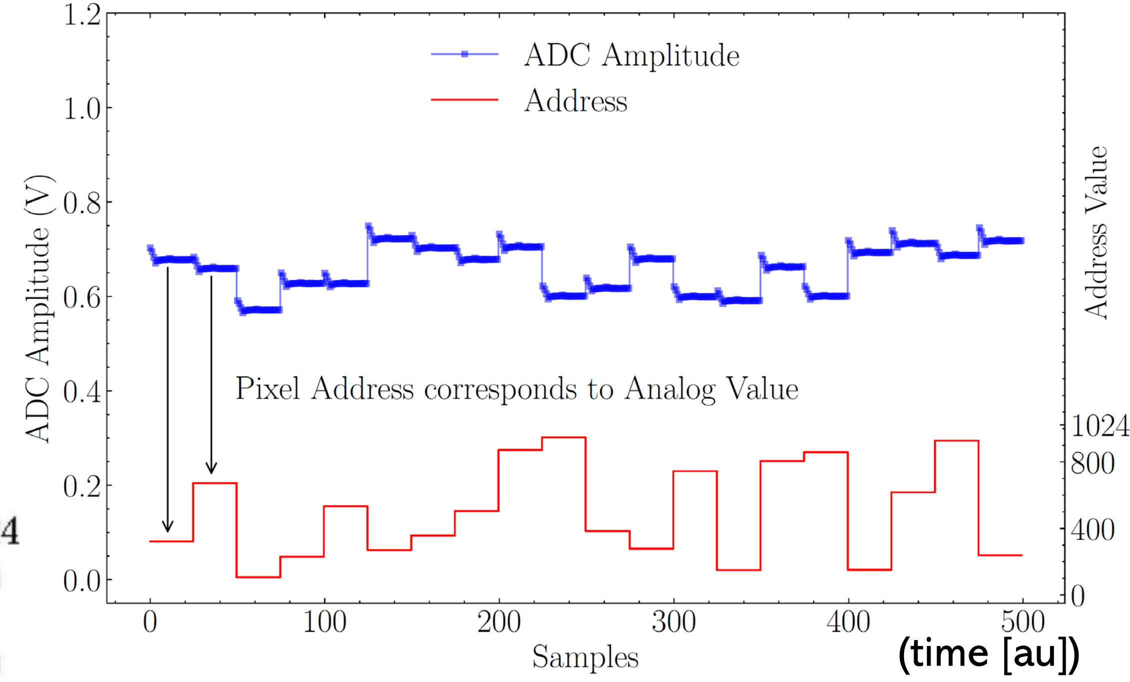
central pixel

8 neighbors

no event

Full Readout Mode

only central pixel (for each event)

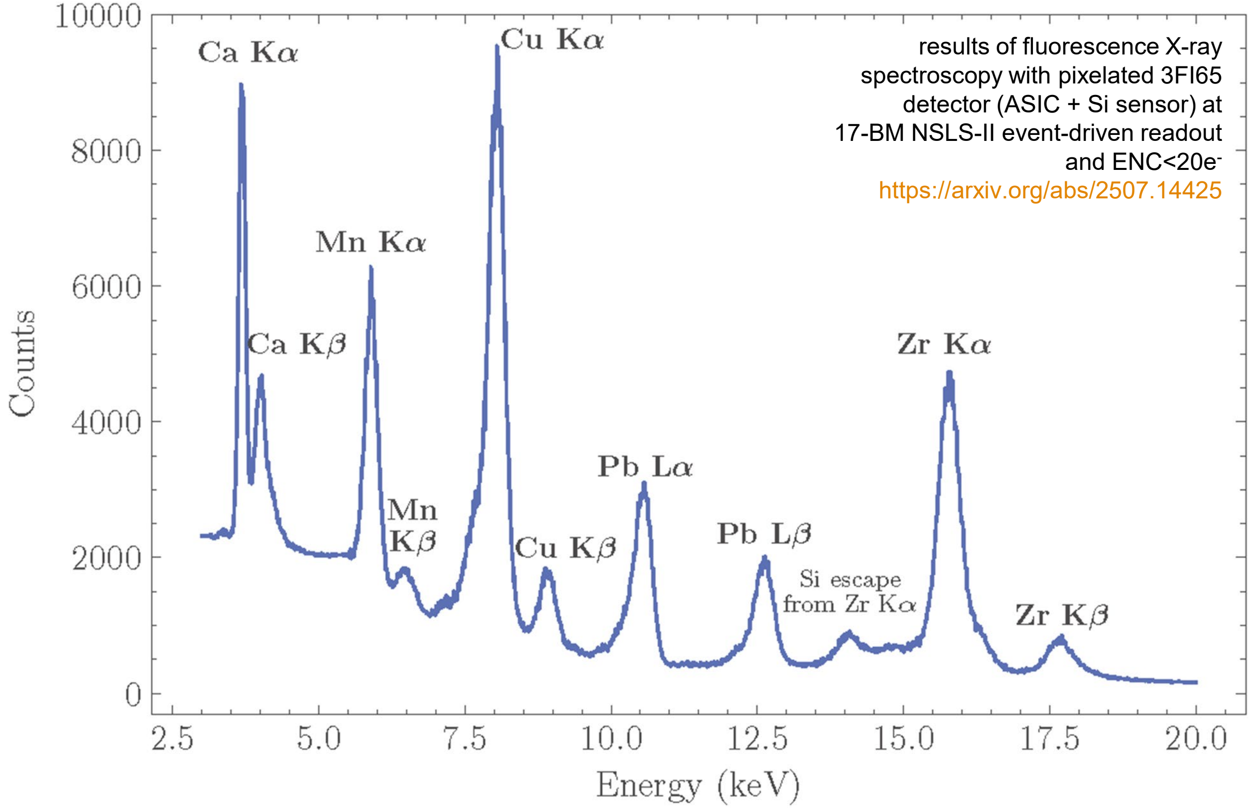


High Throughput Mode

➡ full complete signals from fractions shared among neighbors

Measurement Results (2)

3FI65 with Si-pixelated sensor bump-bonded



results of fluorescence X-ray spectroscopy with pixelated 3FI65 detector (ASIC + Si sensor) at 17-BM NSLS-II event-driven readout and ENC<20e^-
https://arxiv.org/abs/2507.14425

Maj, P., Deptuch, G. W., Gorni, D., et al. (2026). Evaluation of an event-driven 3FI ASIC for spectroscopic X-ray detection with synchrotron radiation. J. Synchrotron Rad. 33, 145-161 (https://doi.org/10.1107/S1600577525010501).

Characteristic X-ray Lines and Measured Energy Resolutions

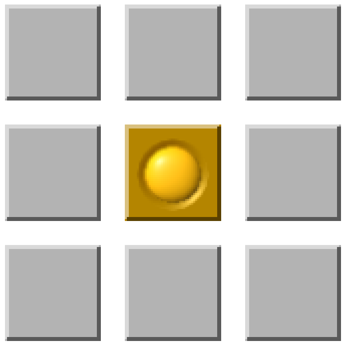
Element	Energy (keV)	FWHM (eV)	σ (eV)	ΔE/E ×100% (σ-based)
Ca (Kα)	3.691	138	58.6	1.59
Mn (Kα)	5.898	249	105.7	1.79
Cu (Kα)	8.047	308	130.8	1.63
Pb (Lα)	10.551	339	144.0	1.36
Zr (Kα)	15.775	469	199.2	1.26

Conversion used: $\sigma = \mathrm{FWHM} / 2.355$

Relative resolution: $\Delta E/E \times 100\% = \sigma/E \times 100\%$

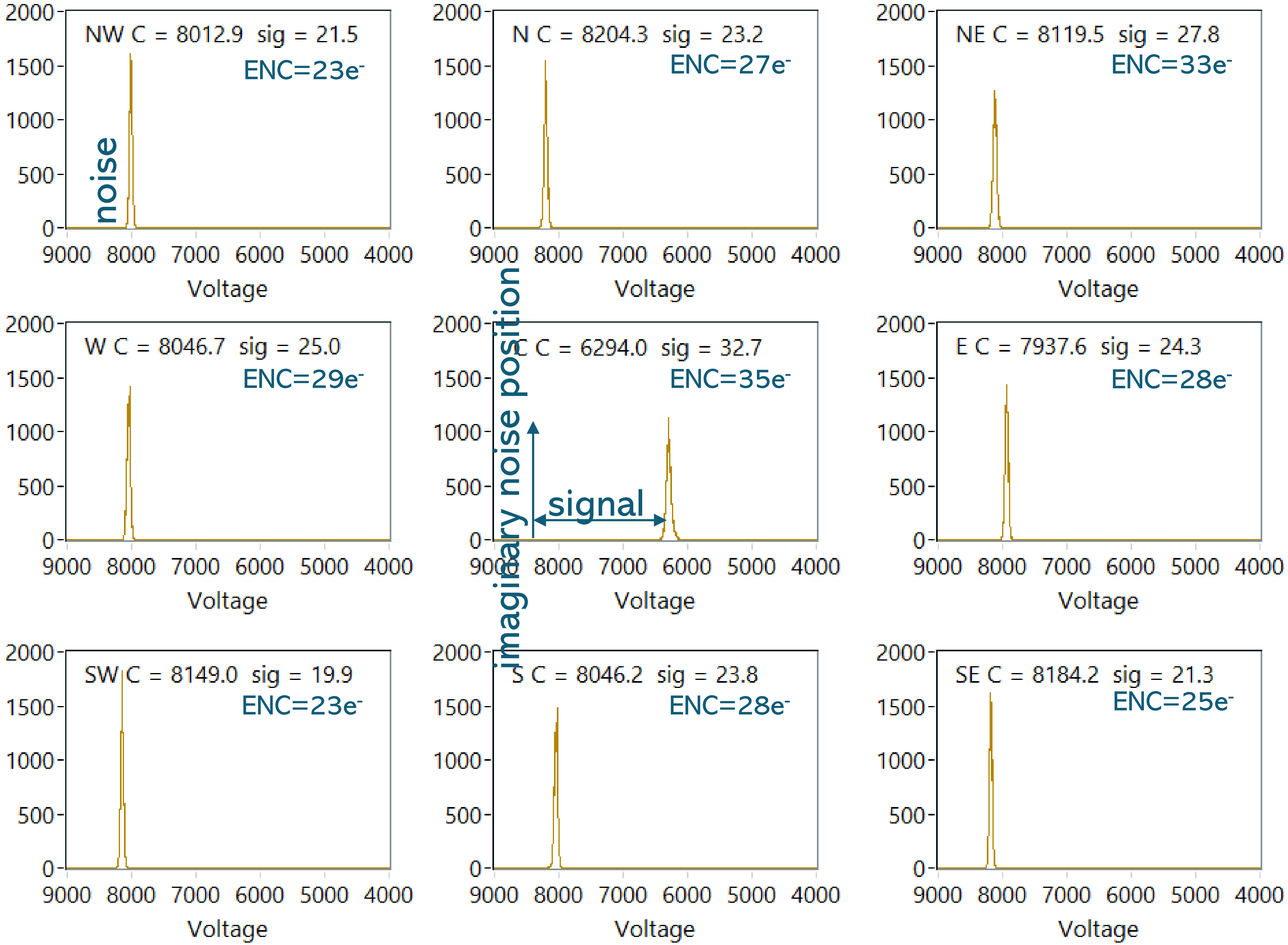
observed evolution of ΔE/E with energy reflects signal-dependent and non-stationary nature of front-end noise in CSA with active feedback.

Measurement Results (3)



- beam is focused on center of one pixel.
- Full Readout Mode, i.e. central pixels peaks its neighbors are sampled too.
- this methods allows to measure baseline noise

(Voltage=ADCu)



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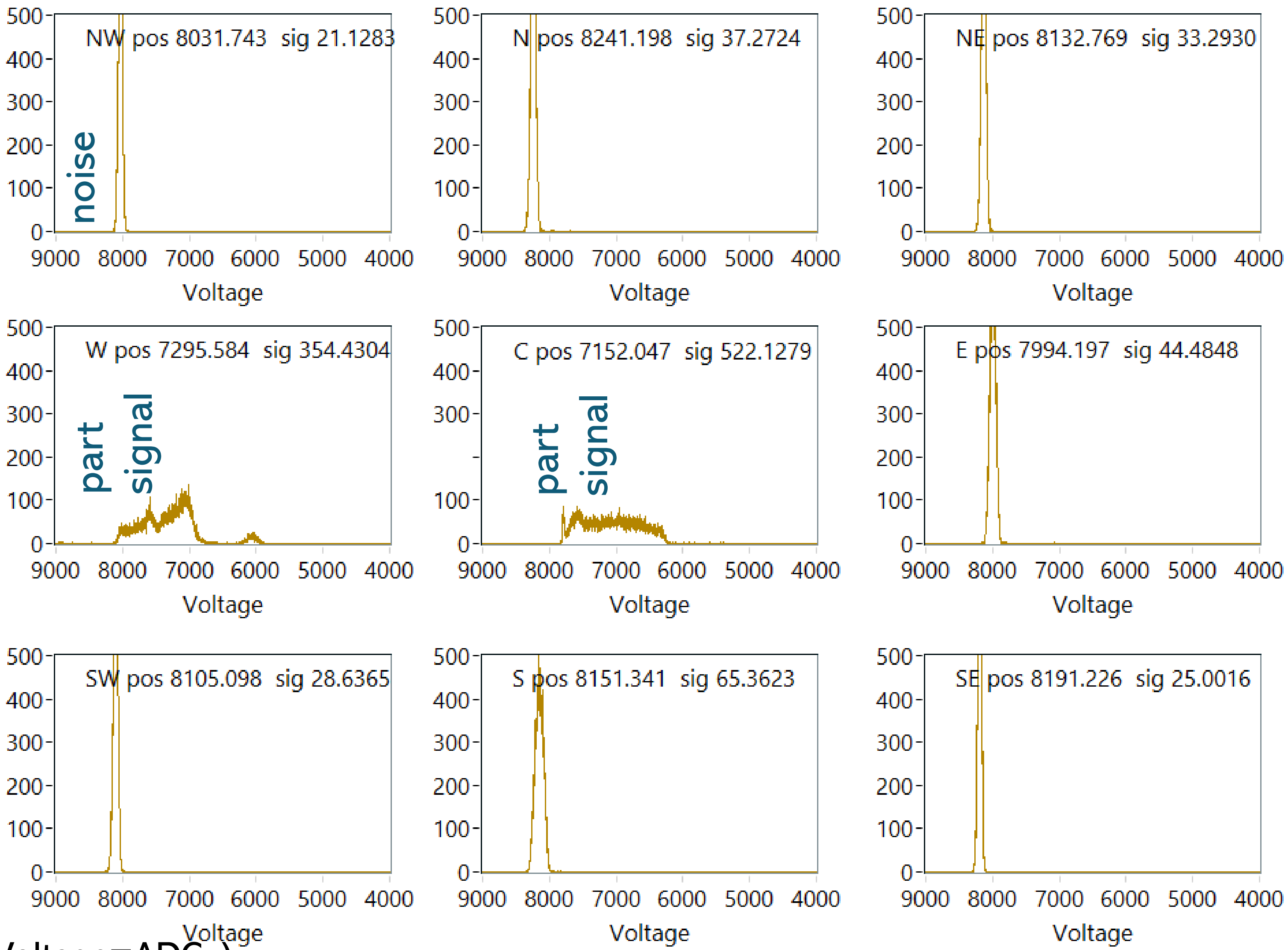
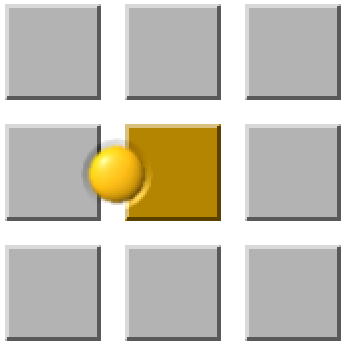
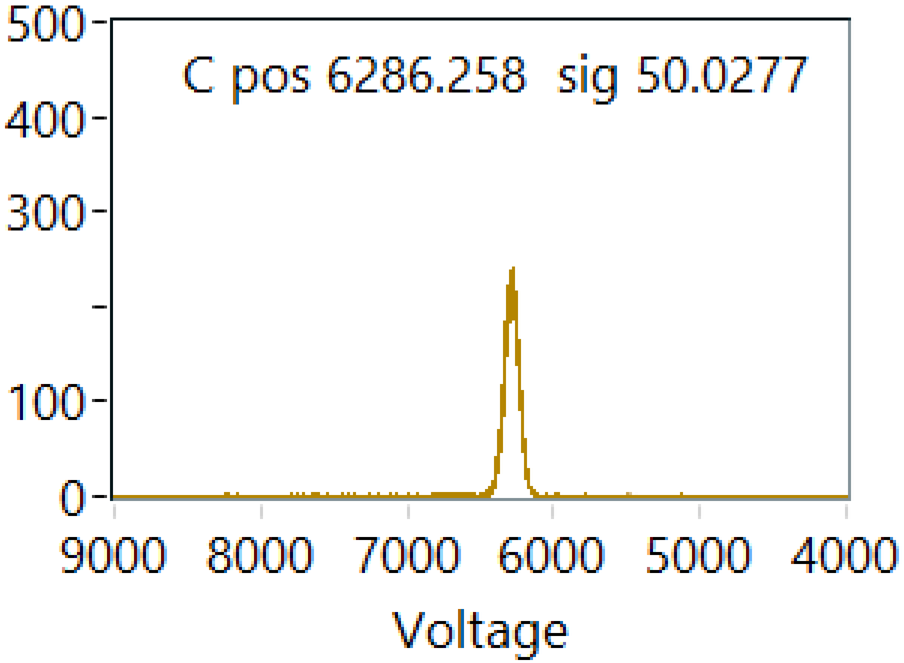
Low Power Supply Design (4)





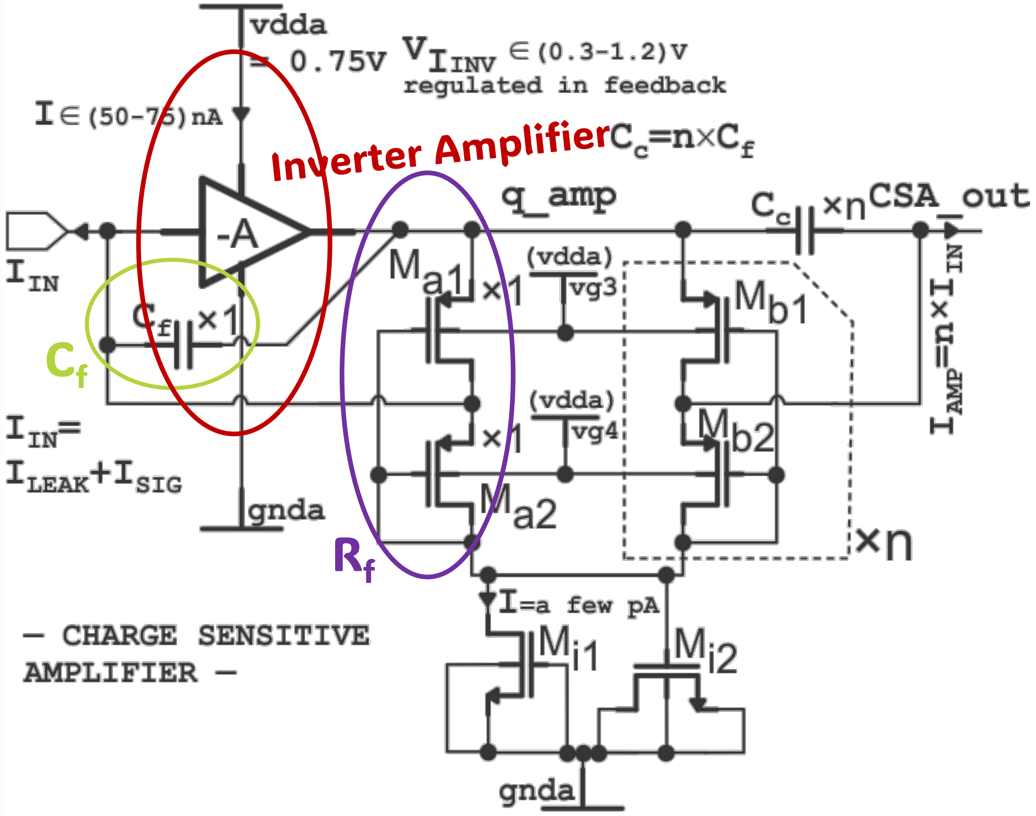
- beam is focused between pixels.
- Full Readout Mode, i.e. central pixels peaks its neighbors are sampled too.
- combined signal is calculated

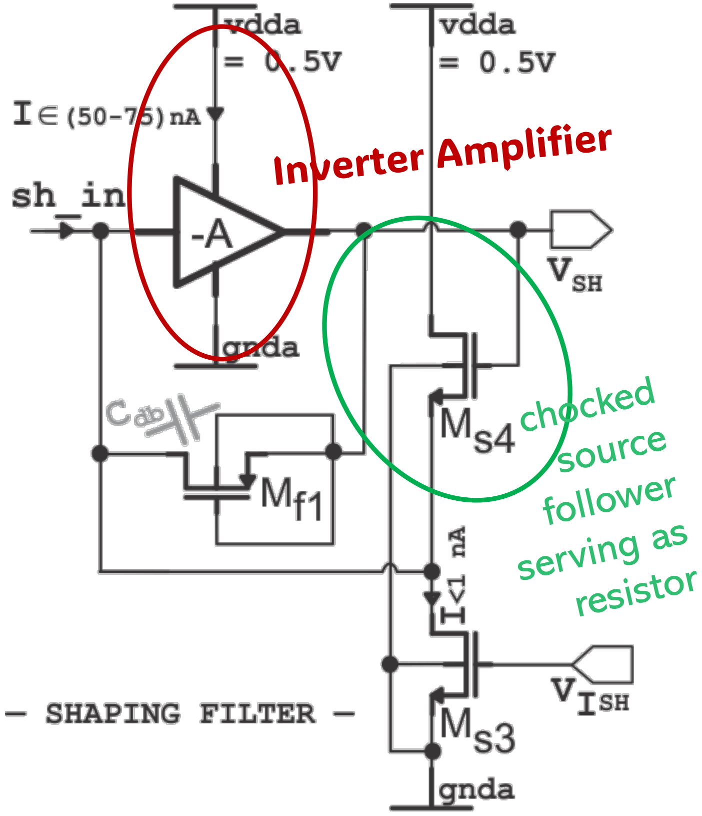


(Voltage=ADCu)

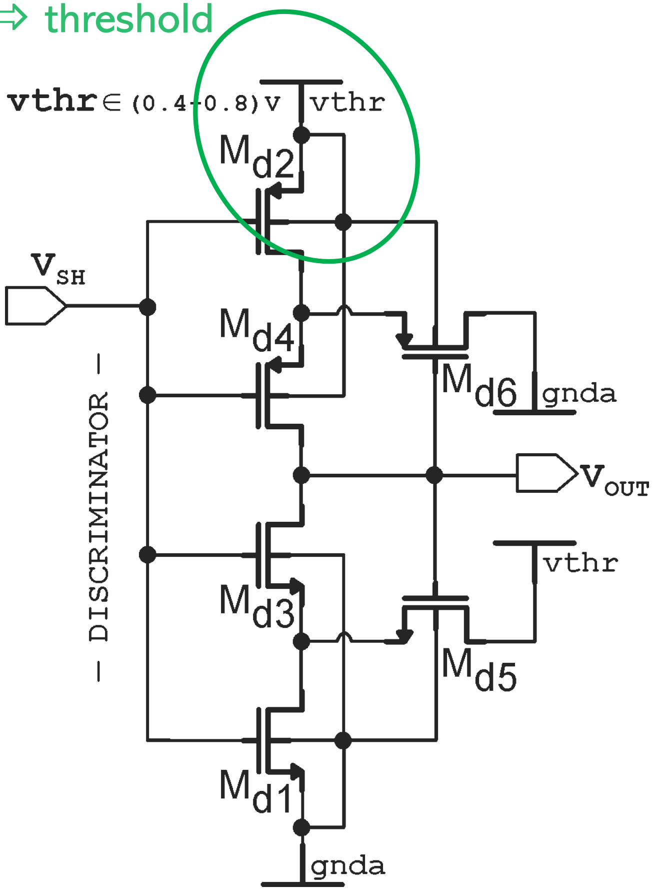
Low Power Supply Design (1)

- <100 nW power,
- compact, using inverter amplifiers with power supply and temperature variation compensation bias current.





power supply
⇨ threshold



- target: TPSCo65nm,

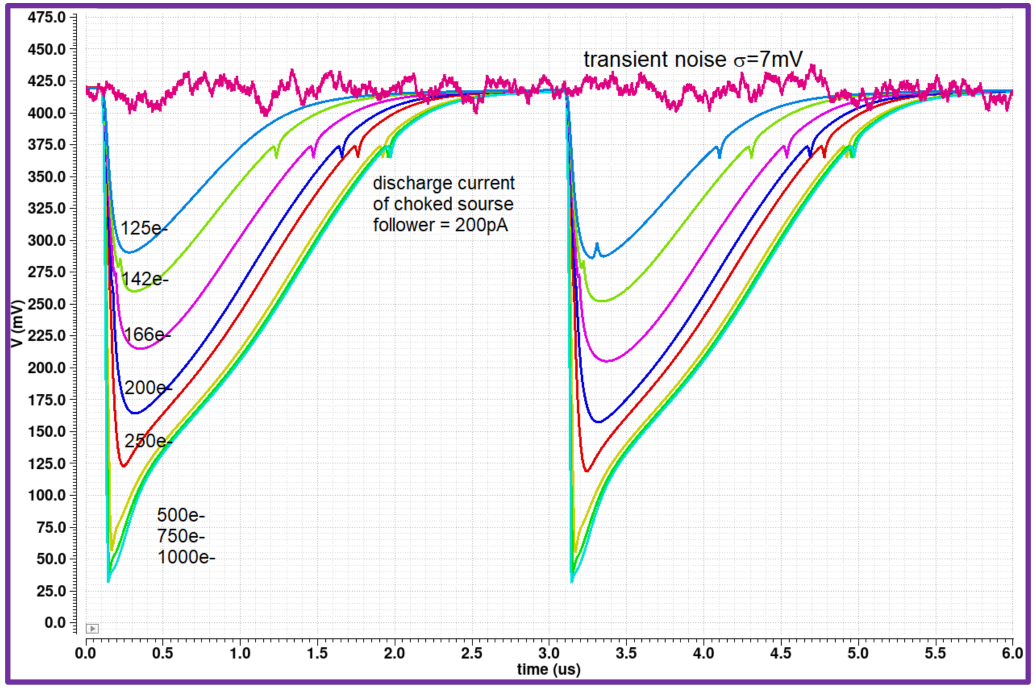
charge
multiplier CSA

I→V stage /
shaping filter

discriminator with zero
continuous power

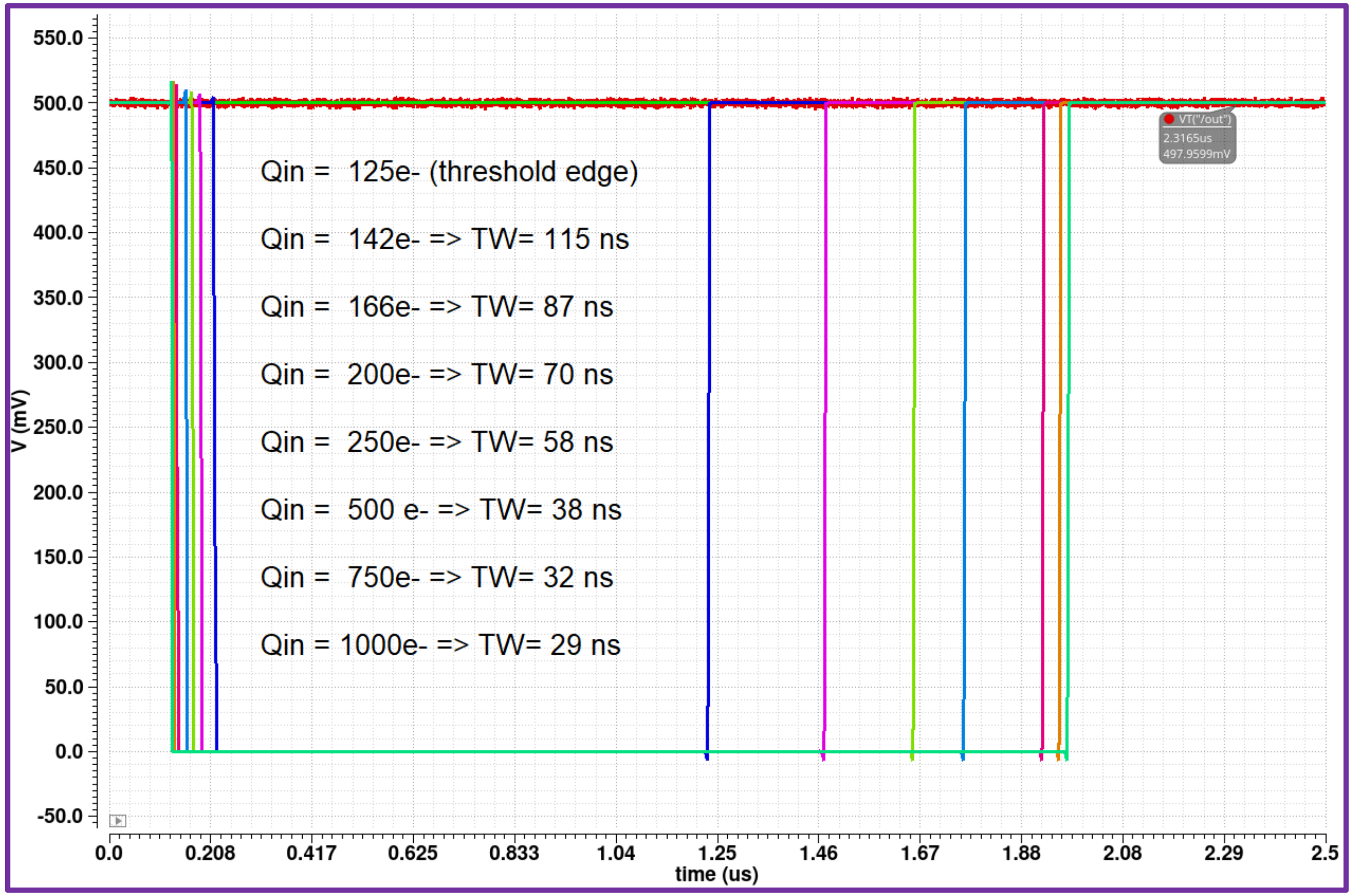
Low Power Supply Design (2)

CSA + shaping filter



waveforms from transient simulations for input charge signals ∈(125 e- , 1000 e-)
~1 mV/e- sensitivity

Discriminator



responses of Schmitt trigger gate discriminator for input charge signal ∈(125 e^- , 1000 e^-) @ TimeWalk < 115 ns

Summary

- SCFET-based CSA alternative to popular CSA solutions:
    - stable operation without h-f filtering capacitor
    - pole-zero cancellation ➲ intrinsic charge multiplication
    - small number of transistors needed
- event-driven readout architecture, enabling low-noise, selective, dead-timeless X-ray pixel readout:
    - ENC < 20e⁻ in continuous operation and ΔE/E ~1.3–1.8% for tender X-rays
    - validated silicon-proven neighbor-aware sampling using in hybrid detector prototype.
- SCFET CSA suitable for sub-100 nW :
    - local supply- and temperature-compensated biasing,
    - compact footprint compatible with ~25 μm-pitch MAPS tracking pixels.

Acknowledgements

- This work has been authored by employees of Brookhaven Science Associates, LLC under Contract No. DE-SC0012704 with the U.S. Department of Energy; Concepts, design and fabrication of ASICs have been covered by:
    - BES B&R: 456165021
    - NASA Grant NNX16AC42G
    - LDRD-A 21-020, LDRD-A 24-054, B&R Code: YN0100000
    - DOE Office of Science, DE-SC0012704, KA2501032/FWP# PO024, DOE Office of BER B&R: 456165021
    - TM 24-01 ATRO/IO – FY24TMAUG, TOF Boost 1, TOFCLIMR

IP

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