Akademia Górniczo-Hutnicza
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AGH University of Krakow

High performance TDC and ADC blocks at ultra-low power

Marek Idzik
AGH University of Krakow

I'd like to thank the participants of the DRD7.3a
project for their contributions to this presentation!

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XIII Front-End Electronics FEE 2026, 18-22 May 2026,Paris, France

Outline

- Introduction to ADC/TDC in DRD7
- ADC
- TDC
- Examples of readout ASICs with ultra-low power ADC/TDC

Introduction DRD7 → D7.3a

Number	Title	Description	Start date	End date	Institutions
D7.3a	High performance TDC and ADC blocks at ultra-low power	Develop ultra-low power high performance TDC and ADC blocks for use in future particle physics experiments.	Sep.24	Jun.27	AT-GUT; BE-KUL; ES-ICCUB; FR-IRFU; FR-CPPM; FR-IP2I; FR-OMEGA; KR-DGIST; PL-AGH; US-SLAC

- 7.3a works primarily as a forum – groups develop their ADC/TDC blocks (and related circuits), exchange experiences and results during meetings organized ~3 times per year
- Designs are done mostly in CMOS 130/65/28 nm

ADC

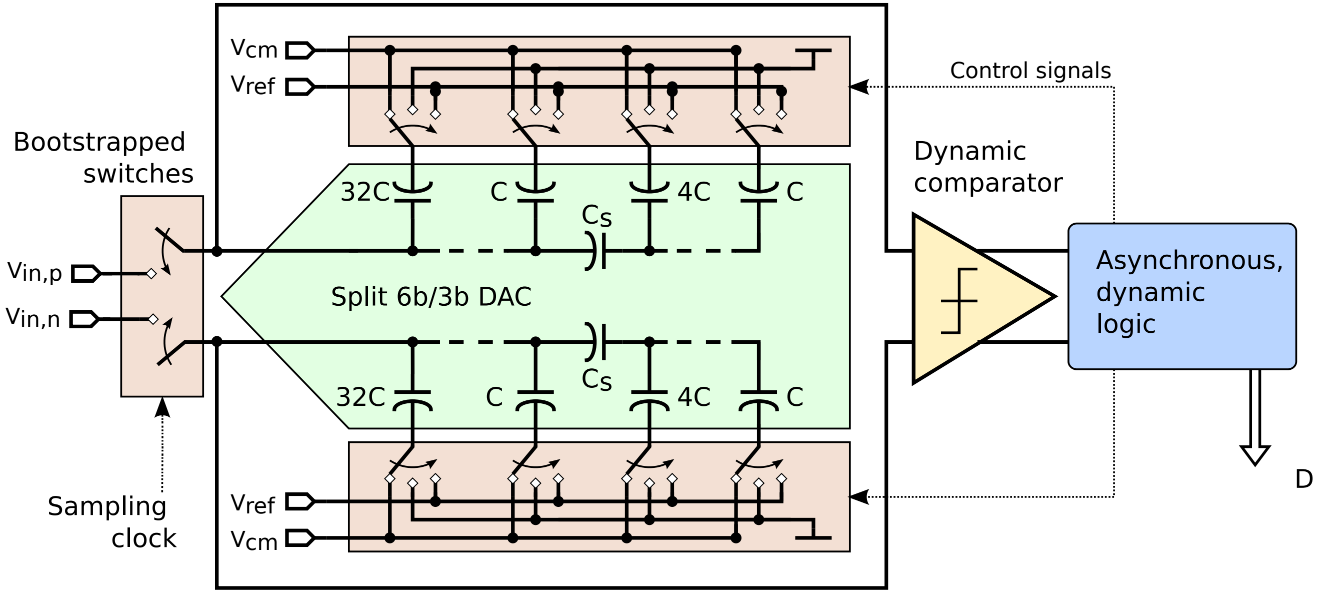
- **ADCs in DRD7.3a and their applications**

- ADC – State of the Art

CMOS 130 nm 10-bit SAR ADC

- ➢ Differential split capacitive DAC with MCS switching scheme – ***ultra low power***
- ➢ Dynamic comparator – ***no static power consumption***
- ➢ Asynchronous logic – no clock tree – ***power saving, asynchronous sampling***
- ➢ Bootstrapped sampling switch for good linearity

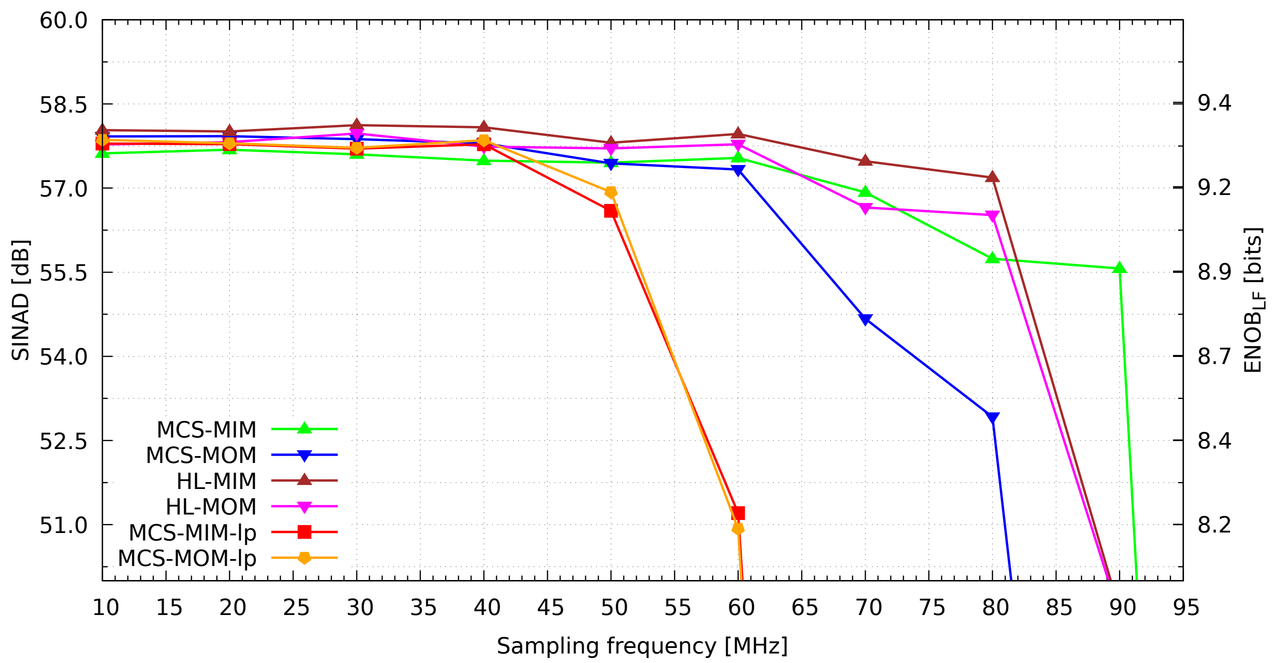
- Main parameters
  - Sampling rate up to 50 MSps
  - DNL, INL < 0.5 LSB
  - ENOB ~9.5 bits
  - Power 0.85mW@50 MSps
  - FOM 24 fJ/conv.-step
- Applications
  - HGCROC, TOFHIR, FLAME, HKROC, FLAXE, CALROC
- Recent updates
  - Internal threshold (not yet submitted)



M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moron, K. Swientek, An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs, Journal of Instrumentation, JINST 18 (2023) P11013

CMOS 65 nm 10-bit SAR ADC

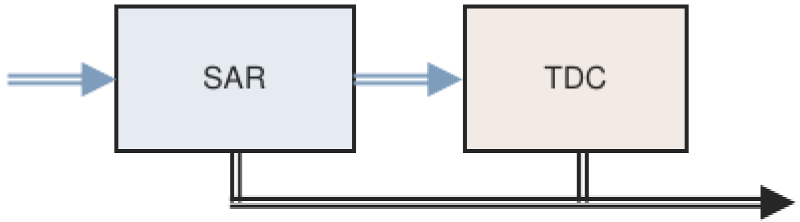
- Architecture as in 130nm
  - Versions with MIM/MOM DACs
  - MCS and HL switching schemes
  - 6-1-3 and 7-1-2 splits
- Main parameters
  - Sampling rate up to 80 MSps
  - DNL ~0.5, INL <1 LSB
  - ENOB 9.1-9.3
  - Power ~1mW@80 MSps
  - FOM_{LF} 16-24 fJ/conv.-step
- Applications
  - Monitoring ADC in lpGBT
  - Future PACIFIC++ for LHCb SciFi
- Recent updates (to be submitted VII 2026)
  - Increasing ENOB to ~9.5 bits
  - Conversion only when triggered

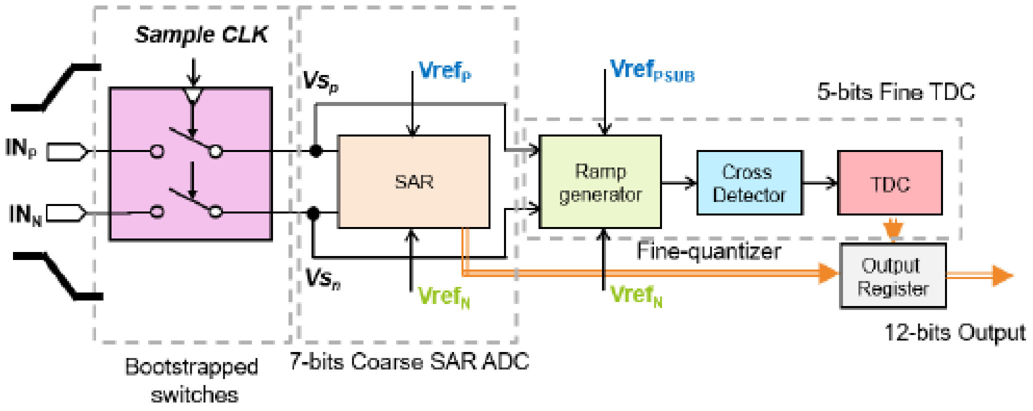


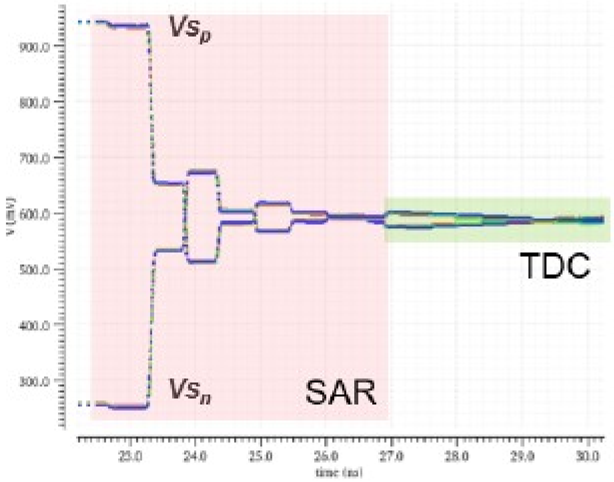
M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, Ultra-low power 10-bit 50–90 MSps SAR ADCs in 65 nm CMOS for multi-channel ASICs, 2024 JINST 19 P01029.

CEA IRFU 12-bit SAR-TDC ADC in CMOS 65 nm

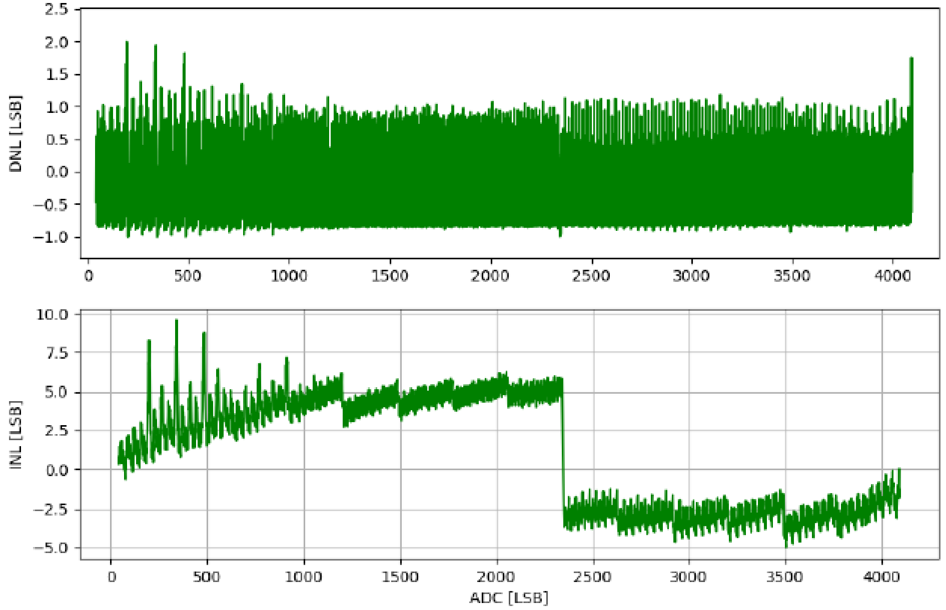
TDC-assisted SAR – SAR residual error converted by TDC – architecture gaining popularity



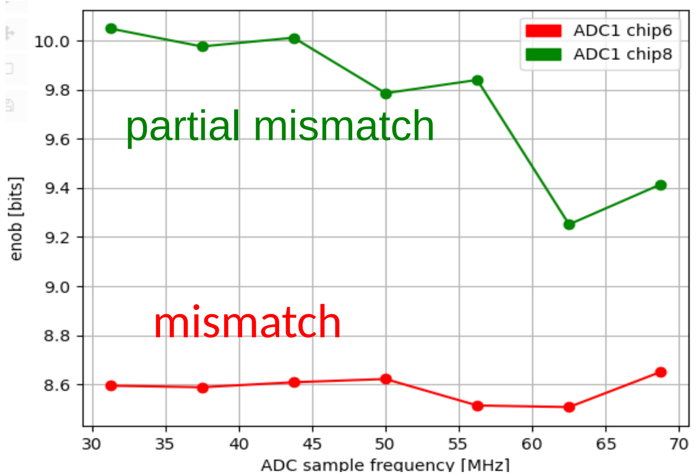




ADC Linearity



ADC ENOB

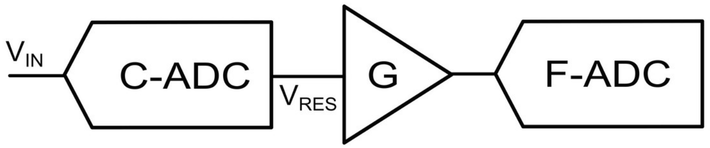


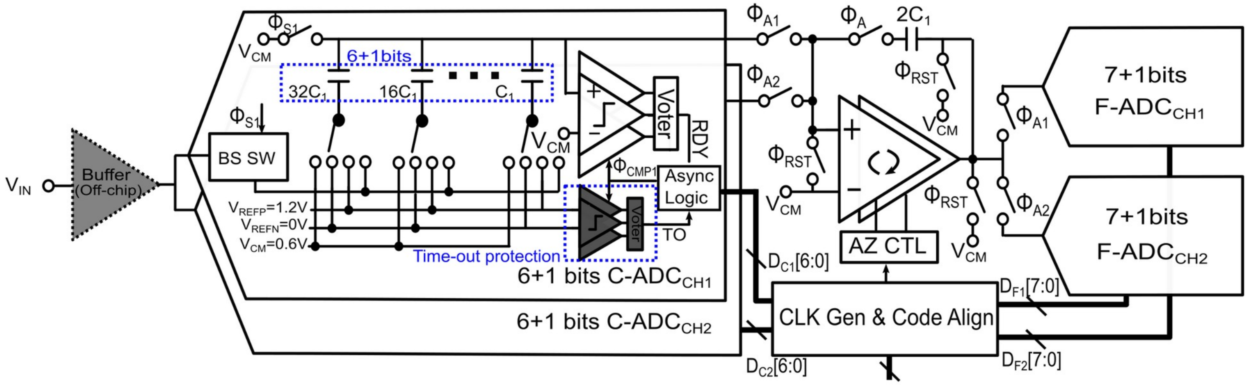
Performance summary (first iteration)	
Technology	CMOS 65 nm
Resolution	12 bits
Input range	1.9 Vpp.diff
Fs	50 MS/s (up to 70)
Power	0.95 mW
ENOB	**9.8 bits**
Area	0.037 mm²

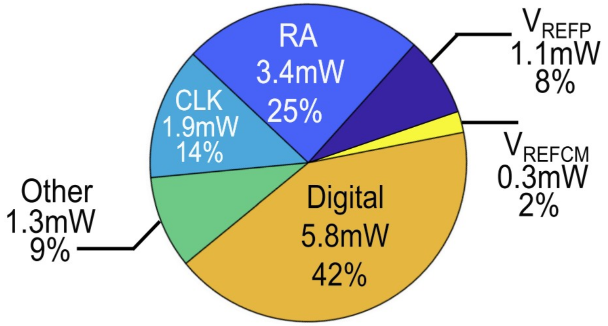
Sources of mismatch understood, an improved ADC version being prepared for submission…

KU Leuven 12-bit rad-hard pipeline-SAR ADCs in CMOS 65 nm and FD-SOI 22nm

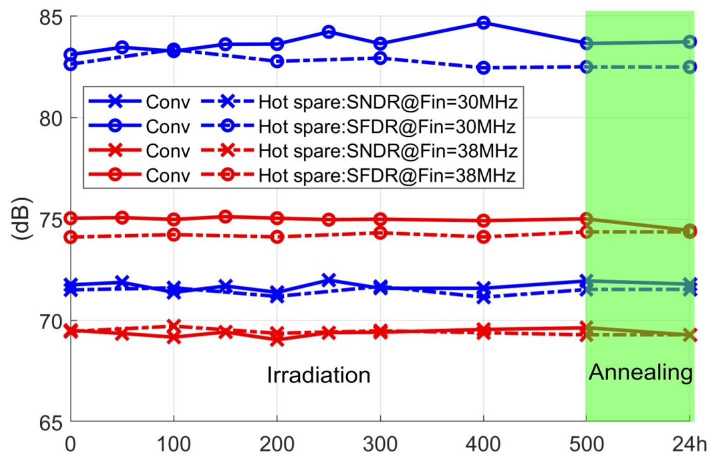
65nm – 80MS/s pipeline-SAR







Power breakdown



Measured SNDR and SFDR when the ADC works in conversion and hot spare modes versus radiation dose

22nm – 5MS/s SAR

New prototype in 22nm FD-SOI for Space Missions was produced recently. Key numbers:

- Power 0.55mW
- SNDR/ENOB = 67.55/10.9
- FOM_{LF} = 56.4 fJ/conv-step

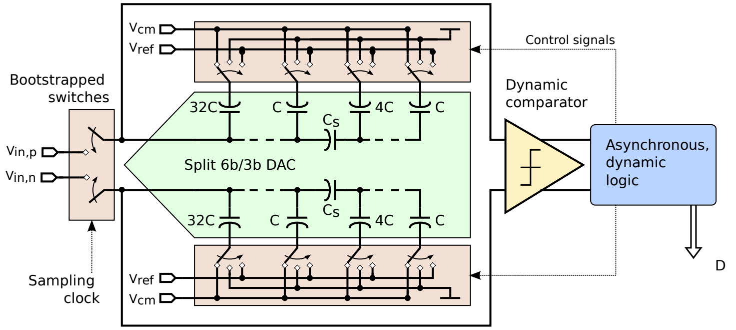
To be presented at:

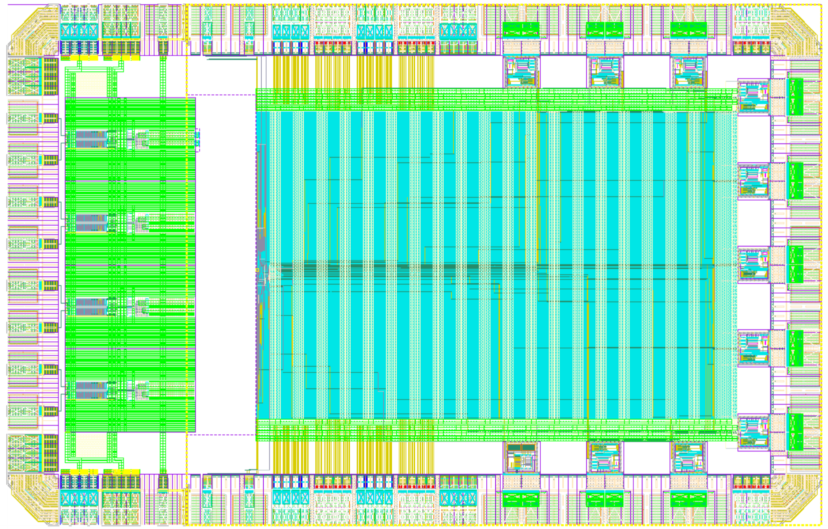
ISCAS 2026 https://2026.ieee-iscas.org/

and NSREC 2026

https://www.nsrec.com/

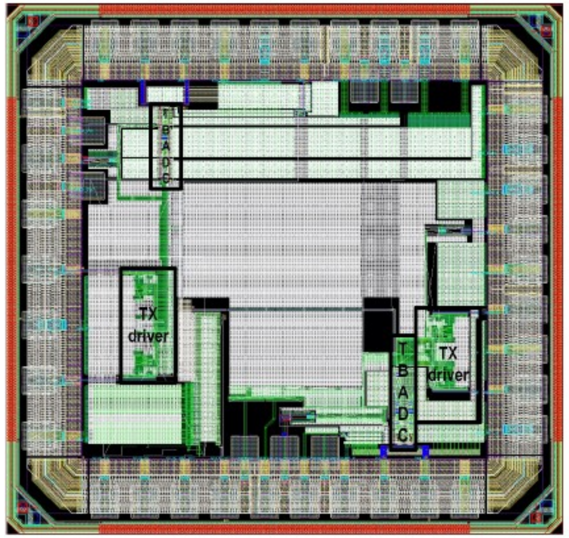
ADCs in CMOS 28 nm

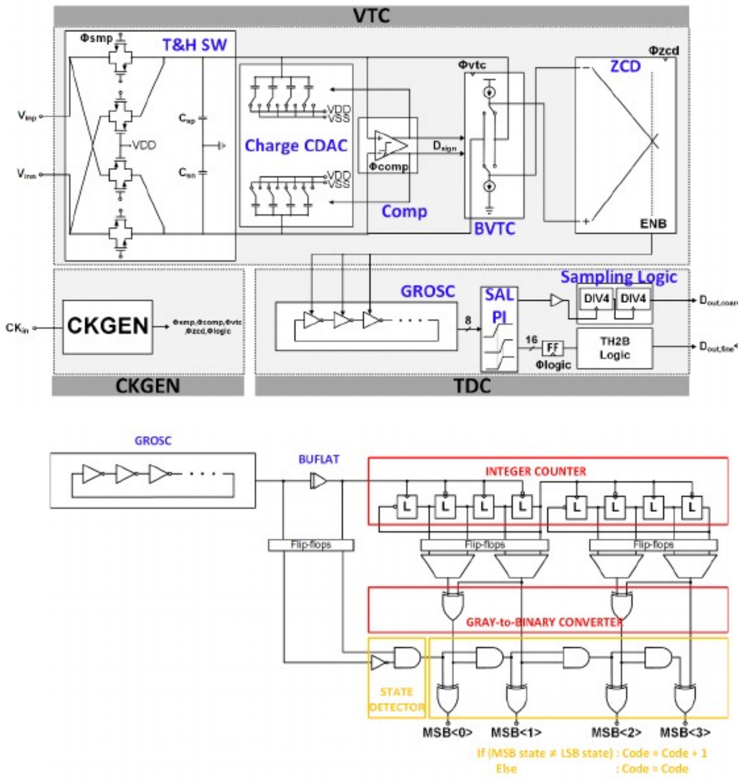




❑TB-ADC

- Sampling speed : 1.75-GS/s
- Power consumption : 3.3mW
- ENOB : 6.13-bit (@ Nyquist input frequency)





4-channel ~200MS/s (<1mW) 10-bit SAR ADC fabricated. Test setup just completed, test will start soon…

DGIST group designed various ~GS/S 6-8 bit ADCs, transmitters and receivers, plans to design higher resolution, slower ADCs

Other ADC designs in DRD7.3a

- 8-bit SAR ADC in CMOS 130 nm (AGH) for EICROC chips. Simplified version of 10-bit SAR ADC integrated directly in EIROC – works well.
- 12-bit SAR ADCs in CMOS 130nm and 65nm (ADC). First prototypes waiting for tests already few years – due to lack of man-power not yet tested…
- 12-bit SAR 100MS/s ADC in CMOS 65 nm (ICCUB). First prototype fabricated – first measurements not conclusive - under investigation…

ADC

- ADCs in DRD7.3a and their applications

- **ADC – State of the Art**

Resolution 10-14 bits, sampling 50-500 MS/s

ADC – Figure Of Merit (FOM)

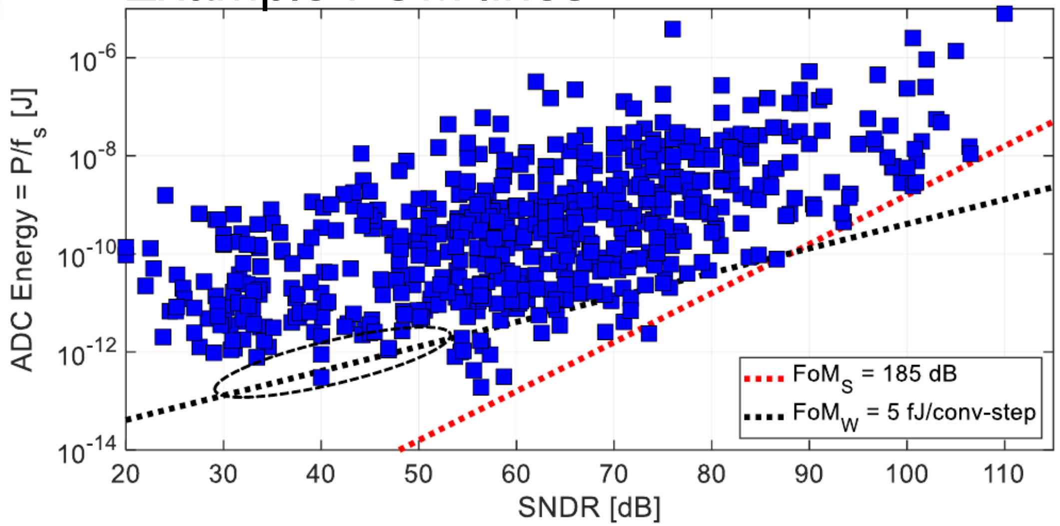
Walden FOM

$$FOM_W = \frac{Power}{f_{sample} * 2^{ENOB}}$$

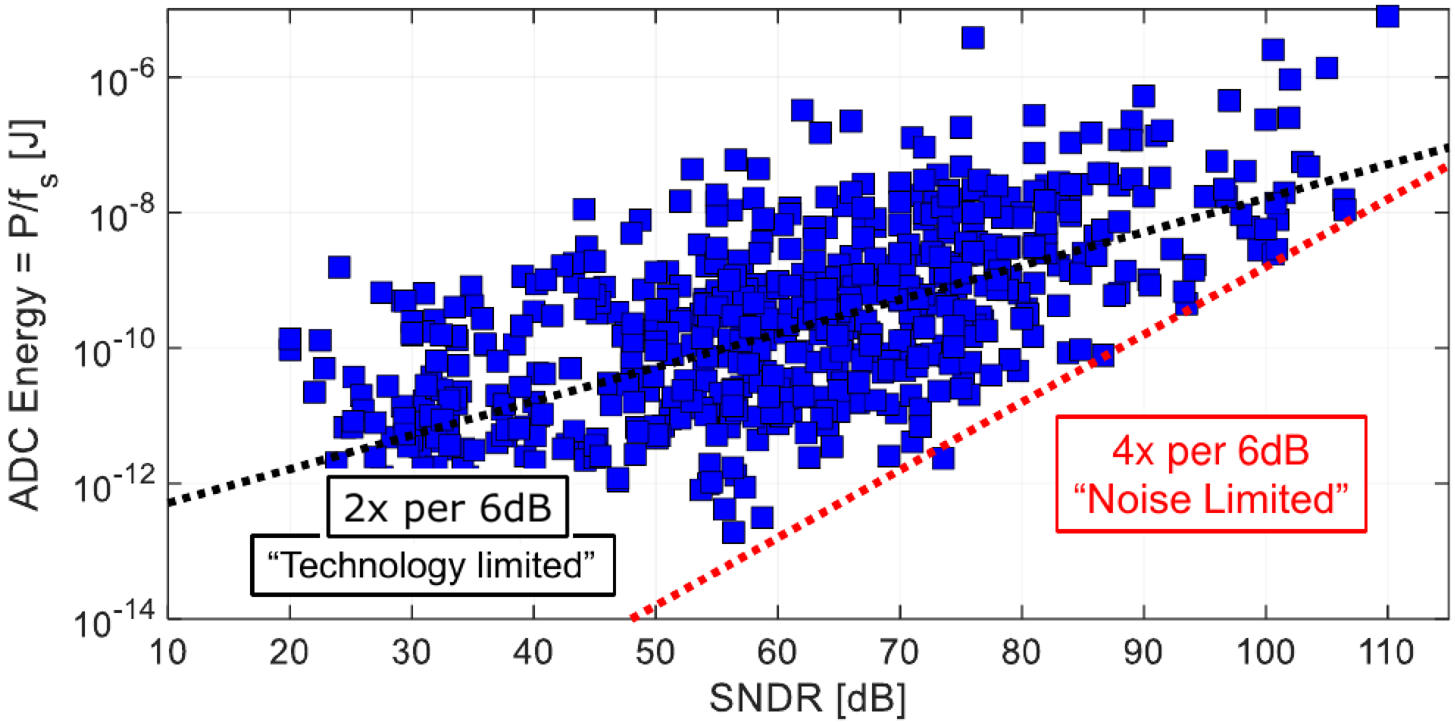
Schreier FOM

$$FOM_S = SNDR + 10 * \log\left(\frac{f_{sample}/2}{Power}\right)$$

Example FOM lines



Energy per conversion



B. Murmann, https://github.com/bmurmann/ADC-survey

ADC 65nm(130nm) – State of the Art

	JINST 2023 [1]	JINST 2024 [2]	ISSCC 2017 [3]	VLSI 2014 [4]	TCAS-I 2020 [5]	JSCC 2023 [6]
Architecture	SAR	SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR
Technology [nm]	130	65	65	65	65	65
Resolution [bit]	10	10	12	12	12	12
Area [mm^2]	0.048	0.014	0.08	0.48	0.198	0.049
Supply [V]	1.2	1.2	0.9	0.9	1.2	0.85
Sample rate [MS/s]	50	80	330	210	100	50
Power [mW]	0.85	1.04	6.23	5.3	1.9	0.46
SNDR [dB]	58.6	56.6	63.5	60.1	65.7	65
ENOB [bit]	9.4	9.1	10.3	9.7	10.6	10.5
FOM_W [fJ/conv.step]	24.4	23.5	15.4	30.5	12.1	6.3
FOM_S[dB]	163.3	162.5	167.7	163.1	169.9	172.4

CEA IRFU 12-bit SAR-TDC ADC in CMOS 65nm for the best working channel would have FOM_W ~ 21 fJ/conv.step

Only the best designs are selected, very good designs in 65nm have FOM_W 50-100 fC/conv.step

Recent and ongoing ADC designs in the HEP community are approaching state-of-the-art performance. A 12-bit 40MS/s ADC consuming <1mW is a very realistic goal in 65nm.

ADC 65nm(130nm) – State of the Art

[1] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moron, K. Swientek, An Ultra-Low Power 10-bit, 50 MSps SAR ADC for Multi-Channel Readout ASICs, Journal of Instrumentation, JINST 18 (2023) P11013

[2] M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, Ultra-low power 10-bit 50–90 MSps SAR ADCs in 65 nm CMOS for multi-channel ASICs, 2024 JINST 19 P01029.

[3] H. Huang, S. Sarkar, B. Elies, and Y. Chiu, “28.4 A 12b 330MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2017

[4] C.-Y. Lin and T.-C. Lee, “A 12-bit 210-MS/s 5.3-mW pipelined-SAR ADC with a passive residue transfer technique,” in Proc. Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2014

[5] S. Liu, H. Han, Y. Shen, and Z. Zhu, “A 12-bit 100-MS/s pipelined- SAR ADC with PVT-insensitive and gain-folding dynamic amplifier,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 8

[6] H. Yoon, C. Lee, T. Kim, Y. Kwon, and Y. Chae, “A 65-dB- SNDR pipelined SAR ADC using PVT-robust capacitively degenerated dynamic amplifier,” IEEE J. Solid-State Circuits, vol. 58, no. 4, Apr. 2023

ADC 28nm – State of the Art

	JSSC 2023 [1]	JSSC 2020 [2]	JSSC 2022 [3]	OJSSCS 2025 [4]	ISSCC 2022 [5]	JSSC 2016 [6]	TCAS 2026 [7]
Architecture	Pipe-SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR	SAR-TDC	SAR
Technology [nm]	28	28	28	28	28	28	28
Resolution [bit]	11	14	14	14	13	12	12
Area [mm^2]	0.05	0.018	0.013	0.048	0.004	0.047	0.028
Supply [V]	1	1.1	1.1	1	0.9	0.9	0.9
Sample rate [MS/s]	100	100	130	150	200	100	200
Power [mW]	1.33	0.7	0.82	1.72	1.3	0.35	1.1
SNDR [dB]	61.9	71.7	72.5	67.9	66.7	64.4	59.8
ENOB	10.0	11.6	11.8	11.0	10.8	10.4	9.6
FOM_W [fJ/conv.step]	13.1	2.2	1.8	5.7	3.7	2.6	6.9
FOM_S[dB]	167.7	180.2	181.5	174.3	175.6	175.9	169.4

Post-layout simulations of 10-bit SAR ADC (ENOB~9.4) designed at AGH, consuming ~0.8mW at ~200 MHz, give FOM_W < 6 fJ/conv.step

Only the best designs are selected, very good designs in 28nm have FOM_W 15-50 fC/conv.step

ADCs in CMOS 28nm show 2-4 times better energy efficiency than those in 65nm. Do we need anything better?

Pipeline-SAR, SAR and SAR-TDC architectures provide the best performance (in 65nm too).

ADC 28nm – State of the Art

[1] Y. Park, J. Song, Y. Choi, C. Lim, S. Ahn, and C. Kim, “An 11-b 100-MS/s fully dynamic pipelined ADC using a high-linearity dynamic amplifier,” IEEE J. Solid-State Circuits, vol. 55, no. 9, Sep. 2020.

[2] J.-C. Wang, T.-C. Hung, and T.-H. Kuo, “A calibration-free 14-b 0.7-mW 100-MS/s pipelined-SAR ADC using a weighted-averaging correlated level shifting technique,” IEEE J. Solid-State Circuits, vol. 55, no. 12, Dec. 2020

[3] J.-C. Wang and T.-H. Kuo, “A 72-dB SNDR 130-MS/s 0.8-mW pipelined-SAR ADC using a distributed averaging correlated level shifting ring amplifier,” IEEE J. Solid-State Circuits, vol. 57, no. 12, Dec. 2022.

[4] S. Song, T. Kang, S. Lee, and M. P. Flynn, “A 150-MS/s Fully Dynamic SAR-Assisted Pipeline ADC Using a Floating Ring Amplifier and Gain-Enhancing Miller Negative-C”, IEEE Open Journal of the Solid-State Circuits Society vol. 5, Dec. 2024

[5] M. Zhan, L. Jie, X. Tang, and N. Sun, “A 0.004 mm2 200MS/S pipelined SAR ADC with kT/C noise cancellation and robust ring-amp,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, vol. 65, San Francisco, CA, USA, Feb. 2022

[6] C. Liu, M. Huang, Y. Tu, A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC, IEEE Journal of Solid-State Circuits, Vol. 51, no. 12, Dec. 2016

[7] A. Li, Y. Shen, A. Huang, S. Liu, R. Ding, Z. Zhu, A 12-bit 200-MS/s SAR ADC With Capacitor-Reuse-Based Redundant Weighting Technique, IEEE Transactions on Circuits and Systems–II: Express Briefs, Vol. 73, no. 4, April 2026

ADC <28nm – State of the Art

	VLSI 2022 [1]	ISSCC 2024 [2]	JSSC 2022 [3]	JSSC 2026 [4]	JSSC 2023 [5]	JSSC 2025 [6]
Architecture	SAR	Pipe-SAR	Pipe-SAR	Pipe-SAR	SAR-TDC	Pipe-SAR
Technology [nm]	8	8	16	22	22	22
Resolution [bit]	12	12	11.5	14	12	14
Area [mm^2]	0.0036	0.017	0.008	0.037	0.048	0.019
Supply [V]	0.8	0.9	0.9	0.9	0.8	0.9
Sample rate [MS/s]	250	400	500	50	260	200
Power [mW]	0.56	2.1	2.8	0.36	0.97	2
SNDR [dB]	62	62.8	62.9	73.9	60.5	70.7
ENOB	10.0	10.1	10.2	12.0	9.8	11.5
FOM_W [fJ/conv.step]	2.2	4.7	4.9	1.8	4.3	3.6
FOM_S[dB]	175.5	172.6	172.4	182.3	171.8	177.7

The energy efficiency of ADCs in the smallest processes is close to 28nm – there is no big jump like between 65nm and 28nm, only the sampling rate increases.
There is no clear incentive to go below 28nm.

ADC <28nm – State of the Art

[1] J. Lee et al., “A 0.56 mW 63.6dB SNDR 250MS/s SAR ADC in 8 nm FinFET,” in Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits), Honolulu, HI, USA, Jun. 2022

[2] Y. Lim et al., “9.2 a 2.08 mW 64.4dB SNDR 400MS/s 12b pipelined-SAR ADC using mismatch and PVT variation tolerant dynamically biased ring amplifier in 8nm,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, CA, USA, Feb. 2024

[3] J. Lagos et al., “A 10.1-ENOB, 6.2-fJ/conv.-step, 500-MS/s, ringamp-based pipelined-SAR ADC with background calibration and dynamic reference regulation in 16-nm CMOS,” IEEE J. Solid-State Circuits, vol. 57, no. 4, Apr. 2022

[4] Z. Chen, S. Ye, J. Gao, Jie Li, L. Shen, An Energy-Efficient Pipelined-SAR ADC With Cascode Capacitively Degenerated Dynamic Amplifier and MSB Pre-Conversion Technique, accepted in IEEE J. Solid-State Circuits, 2026

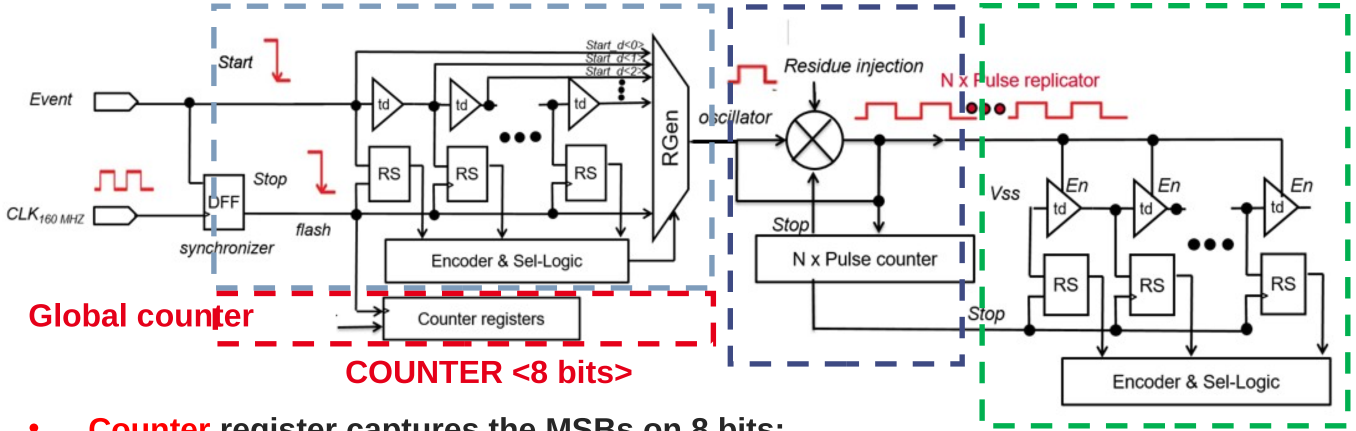
[5] H. Zhao and F. F. Dai, “A 12-bit 260-MS/s pipelined-SAR ADC with ring-TDC-based fine quantizer for automatic cross-domain scale alignment,” IEEE J. Solid-State Circuits, vol. 58, no. 10, Oct. 2023

[6] S. Ye, J. Gao, J. Li, Z. Chen, X. Xu, J. Cui, Y. Luan, L. Ye ,X. Zhang, R. Huang, L. Shen, A 2-mW 70.7-dB SNDR 200-MS/s Pipelined-SAR ADC Using Continuous-Time SAR-Assisted Detect-and-Skip and Open-Then-Close Correlated Level Shifting, IEEE J. Solid-State Circuits, vol. 60, no. 7, July 2025

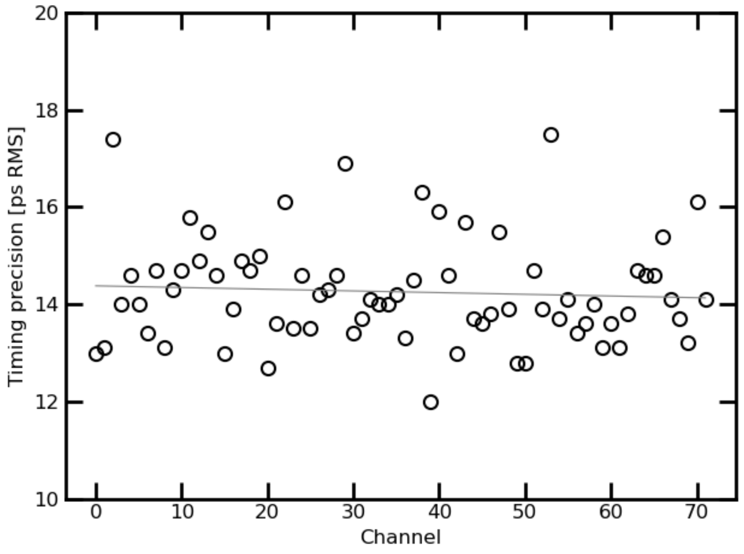
TDC

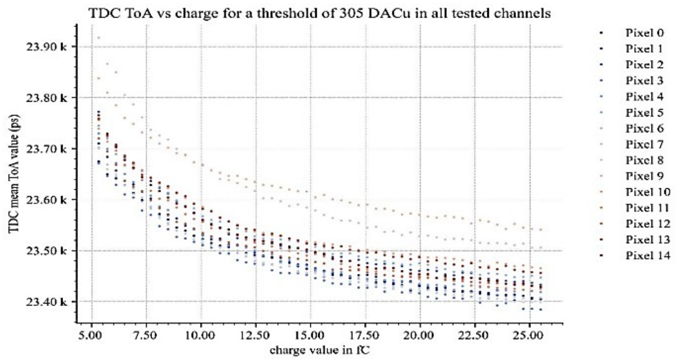
- **TDCs in DRD7.3a and their applications**
- TDC – State of the Art

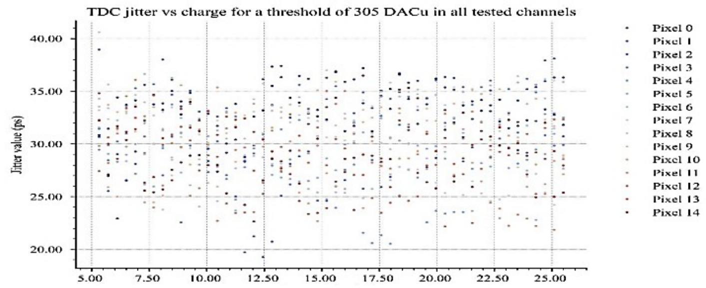
CEA IRFU 10-bit TDC ADC in CMOS 130 nm
3-step TDC based on Time Residual Amplifier



- Counter register captures the MSBs on 8 bits;
- CTDC, based on a DL provides 6 intermediate bits (5 of which are significant)
- FTDC, using the time residue amplification method, encodes the LSBs on 3 bits







Performance summary	
Technology [nm]	130
Resolution [ps]	24.4
Range [bit]	10
Nlinear [bit]	8.74
DNL [LSB]	1
INL[LSB]	1.4
Area [mm2]	0.051
Supply [V]	1.2
Conversion rate [MS/s]	40
Power [mW]	2.2
FOM [fJ/conv.step]	128.9

Applications:

HGCROC (CMS – ToA.ToT),

HKROC (PMT),

CALROC (SiPM),

EICROC (AC-LGAD)

SLAC – 6.25ps 11-bit TDC in CMOS 28 nm
THRIGLAV (THRee-d InteGrated LgAd driVer)

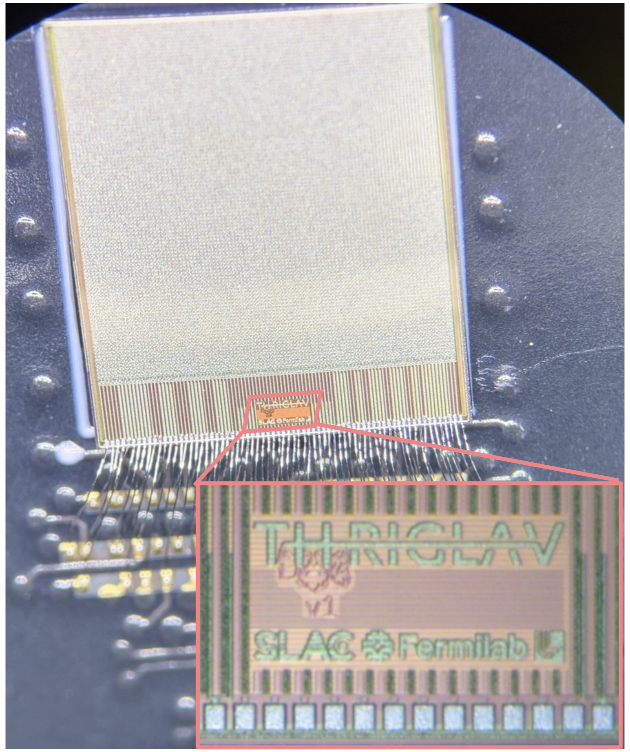
SLAC NATIONAL ACCELERATOR LABORATORY

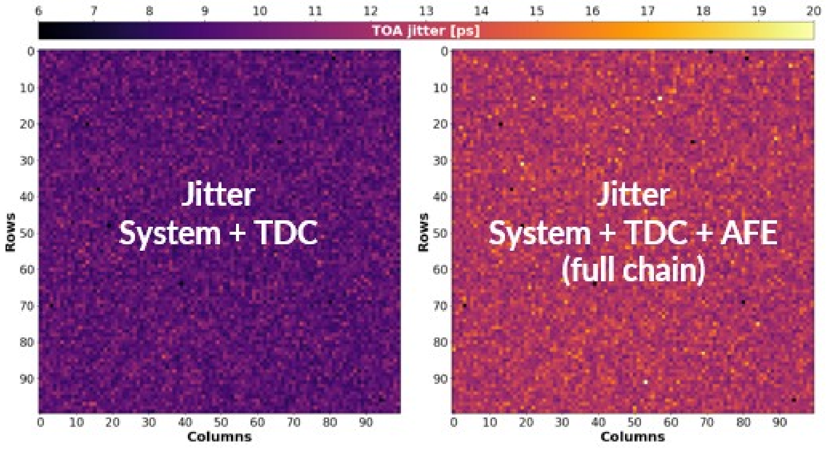
DOE Accelerate Innovations in Emerging Technologies: ***3D Integrated Sensing Solutions*** *(joint effort by SLAC, Fermilab and LLNL teams)*

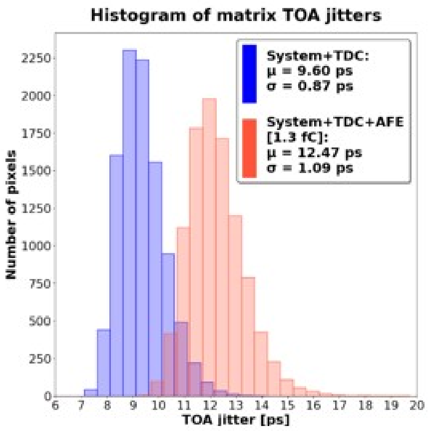
THRIGLAV (**THR**ee-d **I**nte**G**rated **L**g**A**d dri**V**er)
submitted Sept. 2025. Received Dec. 2025.

- (5x6mm^2) with 100x100 50µm pitch pixel array
  - Pixel:
    - Analog FE
    - TDC: TOA 11-bit, 6.25ps | TOT 8-bit, 50ps
    - 9-bit pixel config. register
    - Sparsified readout logic
  - Hierarchical timing-signal distribution H-tree
- Full digital backbend (global config., pixel config., sparsified readout and event builder)
- 5 GHz clock RX
- 2x 10 Gbps serializers + TX (20 Gbps data rate)

THRIGLAV v1 SLAC Fermilab







agh.edu.pl

Ongoing TDC designs in DRD7.3a

- 50ps resolution TDC in CMOS 28nm (CPPM) for hybrid pixels in future upgrades should be submitted in 2026. Prototype of pixel array already produced and verified
- 20-100ps resolution TDC in TPSCo 65 nm (IP2I Lyon) for MANTA chip in initial design stage
- 20ps resolution TDC in CMOS 65nm (SLAC) for MAPs. Design in progress...
- 3.5ps resolution rad-hard (100Mrad) TDC in CMOS 65nm (KU Leuven). Design in progress...
- ~10ps resolution TAC+ADC TDC in CMOS 130nm (AGH). 1st prototype functional, high INL – to be corrected
- 390ps resolution 40MS/s TDC in CMOS 65nm (AGH) for PACIFIC++ in LHCb SciFi. Submission in July 2026

TDC

- TDCs in DRD7.3a and their applications
- **TDC – State of the Art**

  Resolution 1-50 ps, conversion rate 3-250 MS/s

  (significantly fewer articles than for ADC)

TDC – Figure Of Merit (FOM)

Walden-like FOM is the most popular Figure-of-Merit for TDCs

$$FOM = \frac{Power}{f_{conversion} * 2^{ENOB}}$$

usually a rule-of-thumb approximation is used for ENOB, replacing it with a statically measured, effective number of linear bits N_{linear}

$$ENOB \simeq N_{linear} \simeq Range[bit] - \log_2(INL+1)$$

therefore

$$FOM = \frac{Power}{f_{conversion} * 2^{N_{linear}}}$$

This is a very rough estimation of energy efficiency...

TDC 65nm – State of the Art

	TNS 2023 [6]	JSSC 2014 [1]	ISSCC 2016 [2]	JSSC 2013 [3]	JSSC 2012 [4]	ISSCC 2022 [5]
Architecture	Three-step	Pipeline	SS-ADC	Two-step	SAR	Rec. RO
Technology [nm]	130	65	65	65	65	65
Resolution [ps]	24.4	1.12	6	3.75	9.77	24.5
Range [bit]	10	9	6.1	7	10	12
N_{linear} [bit]	8.74	7.57	5.76	5.28	8.42	9.17
DNL [LSB]	1	0.6	-	0.9	1.4	4.2
INL[LSB]	1.4	1.7	0.27	2.3	2	6.12
Area [mm^2]	0.051	0.14	0.17	0.02	0.11	0.002
Supply [V]	1.2	1.2	1.2	1.2	1.2	1.2
Conversion rate [MS/s]	40	250	40	200	80	4.8
Power [mW]	2.2	15.4	0.36	3.6	9.6	1.03
FOM [fJ/conv.step]	128.9	324.8	166.6	464.1	351.6	373.0

[6] is for 72 channels, all other for single channel TDCs

Power and FOM are given at 100% TDC occupancy – actual power may be significantly lower

TDC 65nm – State of the Art

[1] K. Kim, W. Yu, and S. Cho, ‘‘A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register IEEE J. Solid-State Circuits, vol. 49, no. 4, Apr. 2014

[2] A. Sai, S. Kondo, T. T. Ta, H. Okuni, M. Furuta, and T. Itakura, ‘‘A 65 nm CMOS ADPLL with 360μW 1.6ps-INL SS-ADC-based period- detectionfree TDC,’’ in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Jan. 2016

[3] K. S. Kim, Y. H. Kim, W. S. Yu, and S. H. Cho, “A 7 bit, 3.75 ps resolution two-step time-to-digital converter in 65 nm CMOS using pulse-train time amplifier,” IEEE J. Solid-State Circuits, vol. 48, no. 4, Apr. 2013

[4] H. Chung, H. Ishikuro, and T. Kuroda, “A 10-bit 80-ms/s decision- select successive approximation TDC in 65-nm CMOS,” IEEE J. Solid- State Circuits, vol. 47, no. 5, May 2012

[5] F. Arvani and T. C. Carusone, “A reconfigurable 5-channel ring- oscillator-based TDC for direct time-of-flight 3D imaging,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 69, no. 5, May 2022.

[6] F. Bouyjou, E. Delagnes, F. Couderc ,D. Thienpont ,J.D. Gonzalez-Martinez, F. Dulucq ,F. Guilloux, I. Mandjavidze, "A Three-Step Low-Power Multichannel TDC Based on Time Residual Amplifier", IEEE Transactions on Nuclear Science, vol. 70, no. 12, Dec. 2023

TDC <=28nm – State of the Art

	IEEE Access 2025 [1]		IEEE TIM 2023 [2]			VLSI 2022 [3]	ISSCC 2015 [4]	THRIGLAV TDC
Architecture	Single RO		Vernier			Vernier	Stochastic	Vernier RO
Technology [nm]	28		28			28	14	28
Resolution [ps]	4.4	15.4	4.7	11.5	43	8.5	1.17	6.25
Range [bit]	10.8	9.16	12.03	12.03	12.03	11	10	11
N_{linear} [bit]	9.29	8.38	10.72	11.02	11.10	9.28	8.28	9.42
DNL [LSB]	0.43	0.46	1.13	0.62	0.58	0.3	0.8	1
INL[LSB]	1.8	0.72	1.48	1.02	0.91	2.3	2.3	2
Area [mm^2]	0.08		0.0096			0.006	0.036	0.001
Supply [V]	0.9	0.55	1			1	0.6	0.9
Conversion rate [MS/s]	125	100	3.51	3.65	4.94	15	100	40
Power [mW]	12.3	1.7	0.188	0.182	0.067	0.2	0.78	0.5
FOM [fJ/conv.step]	157.2	51.1	31.8	24.0	6.2	21.5	25.1	18.3

THRIGLAV is for 10000 channels, all other are single channel TDCs

Power and FOM are given at 100% TDC occupancy – actual power may be significantly lower.

Power efficiency of TDCs in 28nm is much higher than in 65nm.

TDC <=28nm – State of the Art

[1] O. Järvinen et al., “A 100–750 MS/s 11-bit time-to-digital converter with cyclic-coupled ring oscillator,” IEEE Access, vol. 9, 2021

[2] V.-N. Nguyen and J.-W. Lee, “A 4.7-ps resolution recirculating cyclic Vernier TDC using DWA-based mismatch correction and a register-based time amplifier,” IEEE Trans. Instrum. Meas., vol. 72, 2023

[3] V.-N. Nguyen, X. T. Pham, and J.-W. Lee, “An 8.5 ps resolution, cyclic Vernier TDC using a stage-gated ring oscillator and DWA-based dynamic element matching in 28 nm CMOS,” IEEE Trans. Instrum. Meas., vol. 71, 2022, Art. no. 2002012.

[4] S. Kim, W. Kim, M. Song, J. Kim, T. Kim, and H. Park, “A 0.6V 1.17 ps PVT-tolerant and synthesizable time-to-digital converter using stochastic phase interpolation with 16× spatial redundancy in 14 nm FinFET technology,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2015

Examples of readout ASICs with ultra-low power ADCs/TDCs in CMOS 130nm

Design coordination+FE

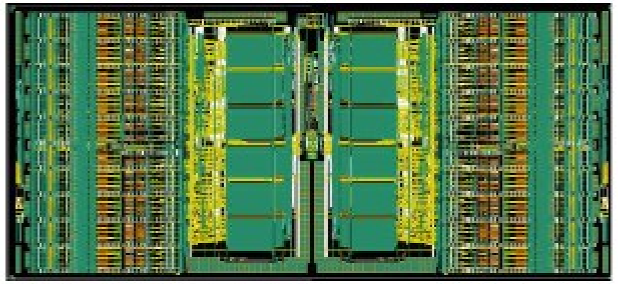
Fast ADC (10/8 bit)

TDC (ToA/ToT)

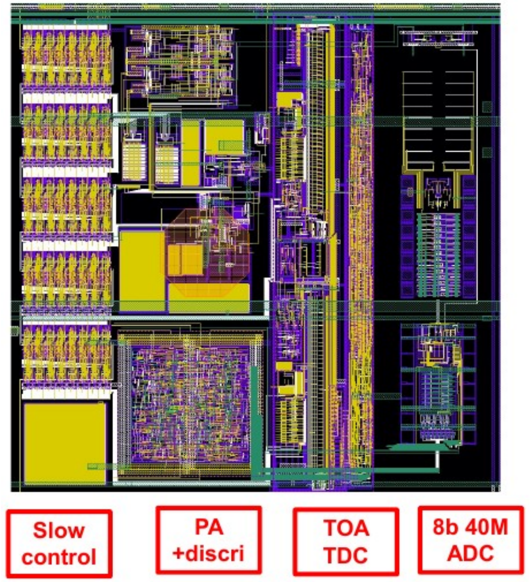
Power per channel is of the order of 10 mW, still too much, but the main bottlenecks are not ADC/TDC...

Collaboration is a natural choice in complex ASIC design, especially given human resource constraints.

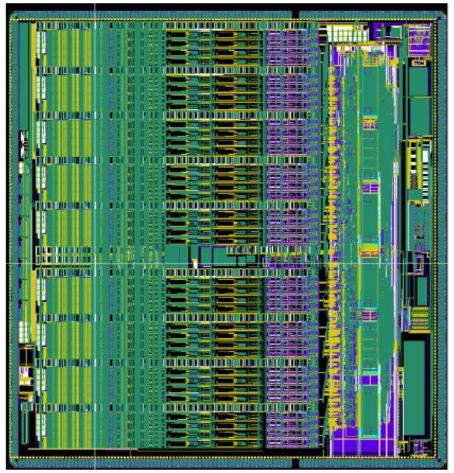
HGCROCs



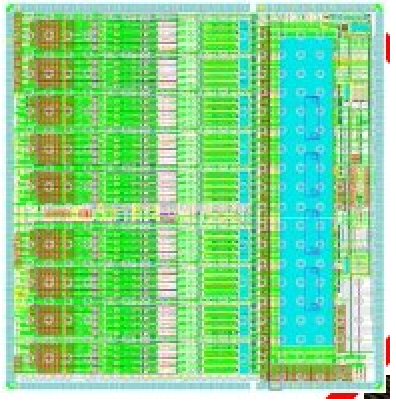
EICROCs



CALROCs



HKROC



Summary

- Recent ADC/TDC designs follow the State of the Art striving for the highest performance (FOM). Hopefully in close future we will have more such IP blocks (not only in DRD7.3a)
- For state-of-the-art ADCs, 28nm CMOS appears to be the last big step towards the ultimate FOM
- State of the Art TDCs in 28nm are much more energy efficient than those in 65nm
- First multichannel readout ASICs with ultra-low power ADCs/TDCs have already been designed, and more will surely follow
- Considering the potential of modern CMOS technologies (mainly 28 nm), the most important need (apart from funds) is not better technology, but human resources capable of utilizing this potential.