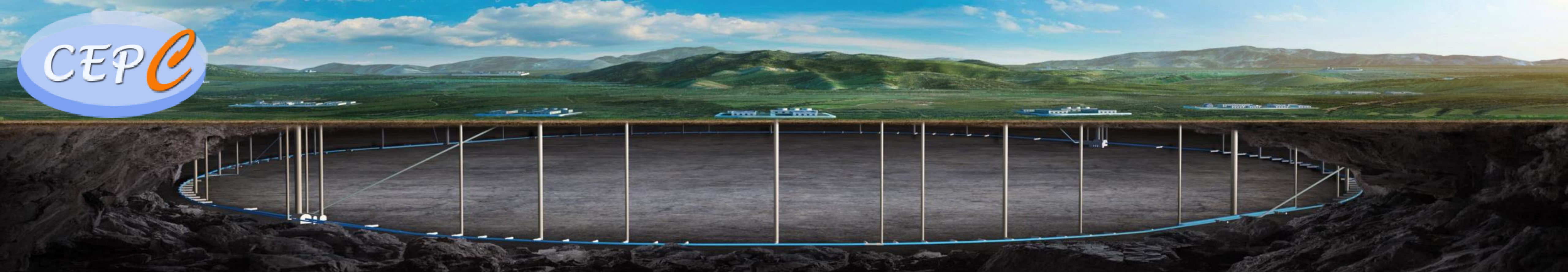

Frontend chip development of the electronic system for the CEPC reference detector

Wei Wei
On behalf of the CEPC Electronics team

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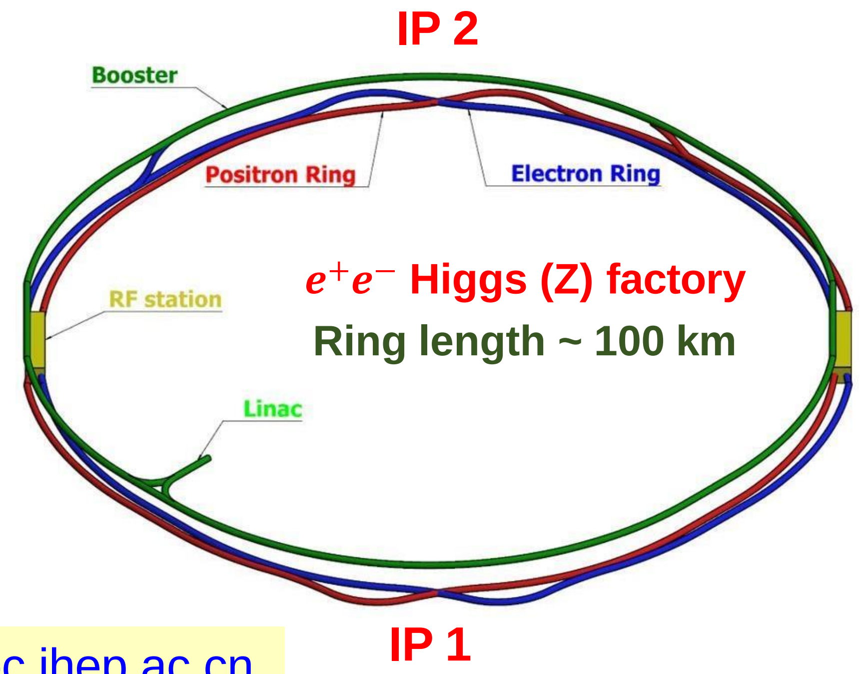
May. 19th, 2026, FEE-2026

Content

The Circular Electron Positron Collider

- The CEPC was proposed in 2012 right after the Higgs discovery. It aims to start operation in 2030s, as an e^+e^- Higgs / Z factory.
- To produce Higgs / W / Z / top for high precision Higgs, EW measurements, studies of flavor physics & QCD, and probes of physics BSM.
- It is possible to upgrade to a *pp* collider (SppC) of s ~ 100 TeV in the future.



http://cepc.ihep.ac.cn

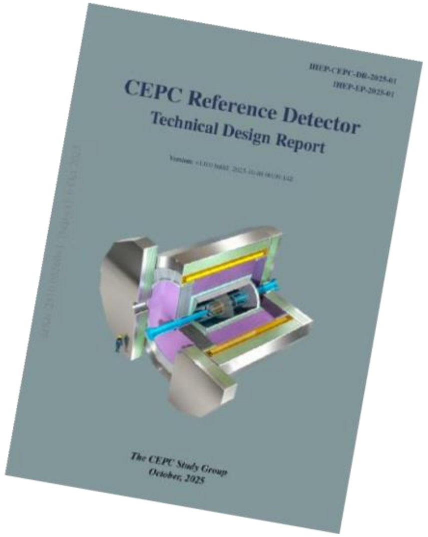
TDR of A Reference Detector

- In October 2025 the CEPC team released TDR of **a reference detector**

- This is to demonstrate the readiness and feasibility of the detector technologies. A detector that meets the requirements could be constructed and commissioned within a decade, and the scoped physics program could be fulfilled.

Baseline Scenario in TDR

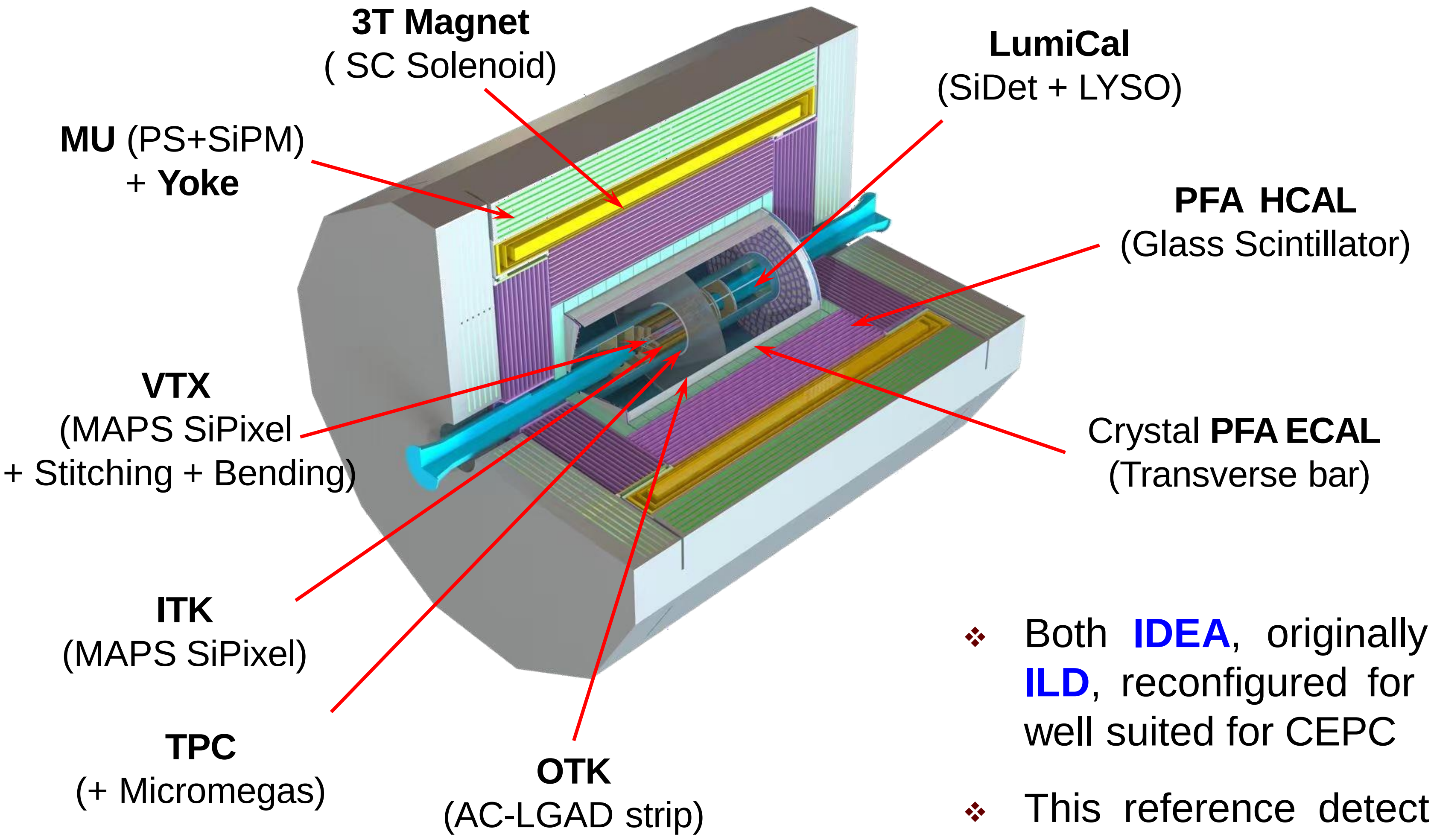
Operation mode	**ZH**	**Z**	**W^+W^-**
s [GeV]	240	91	~160
SR Power (MW)	**30**	**12.1**	**30**
L / IP [$\times 10^{34}$ cm^{-2}s^{-1}]	5	26	16
Run Time [years]	15	4	1
$\int L\,dt$ [ab^{-1}], 1-IP	10	13	1.2
Event Yields	2.0×10^{6}	5.6×10^{11}	1.0×10^{7}


IHEP-CEPC-DR-2025-01
IHEP-EP-2025-01
CEPC Reference Detector
Technical Design Report
The CEPC Study Group
October, 2025

https://doi.org/10.48550/arXiv.2510.05260
1503 authors, 385 institutes, 47 countries

- After the baseline program being approved the international collaborations can propose and decide on the designs of the two final detectors. External contributions could bring back the initial physics program, maybe even the upgrade scenarios.

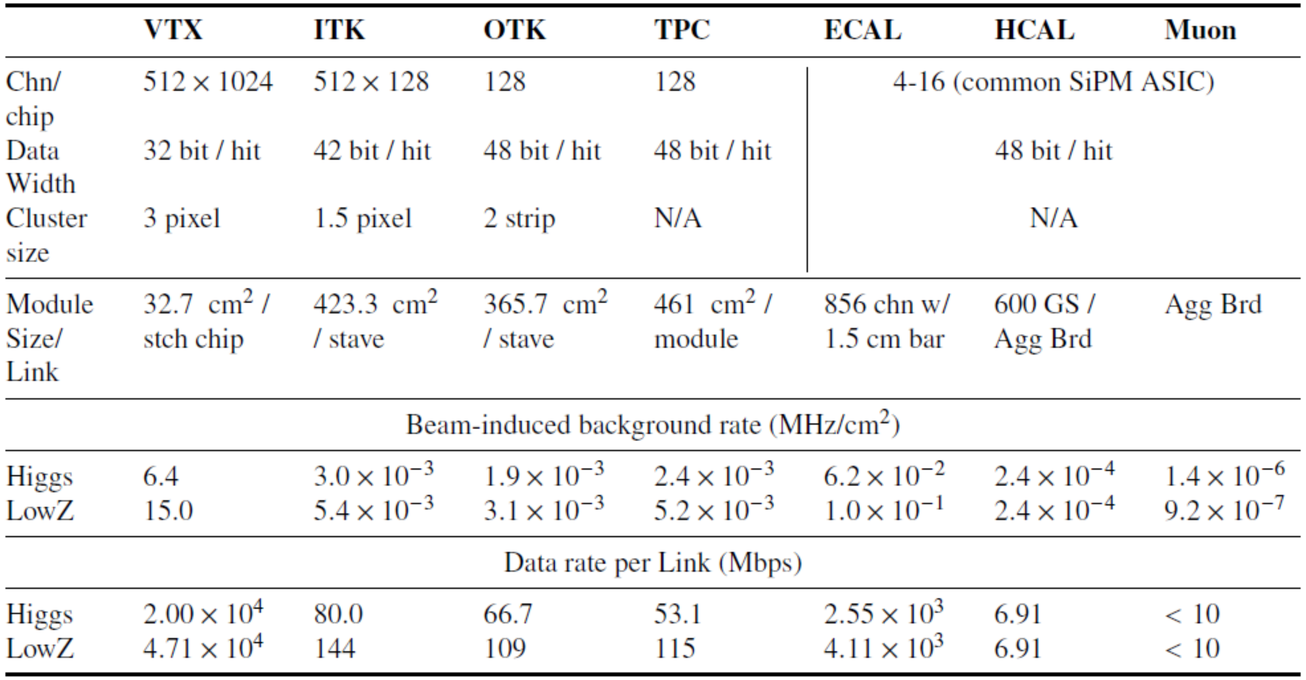
Design of A Reference Detector



- Both **IDEA**, originally proposed for FCC-ee, and **ILD**, reconfigured for the circular e^+e^- collider, are well suited for CEPC
- This reference detector, designed for CEPC, can be readily adapted for use at other circular e^+e^- colliders, such as **FCC-ee**

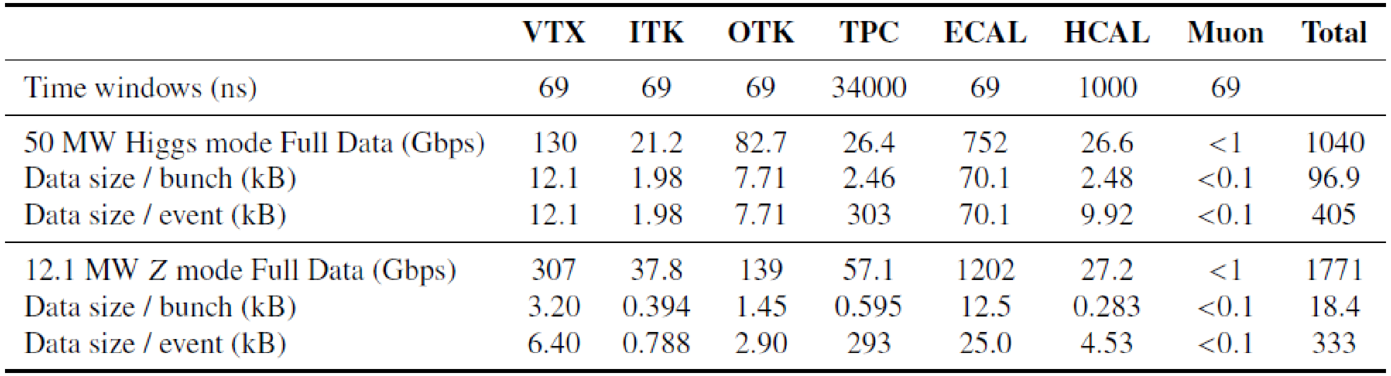
Critical Input from Sub-Det & MDI

Background rate and data rate for the electronic system



	VTX	ITK	OTK	TPC	ECAL	HCAL	Muon
Chn/ chip	512 × 1024	512 × 128	128	128	4-16 (common SiPM ASIC)		
Data Width	32 bit / hit	42 bit / hit	48 bit / hit	48 bit / hit	48 bit / hit		
Cluster size	3 pixel	1.5 pixel	2 strip	N/A	N/A		
Module Size/ Link	32.7 cm^2 / stch chip	423.3 cm^2 / stave	365.7 cm^2 / stave	461 cm^2 / module	856 chn w/ 1.5 cm bar	600 GS / Agg Brd	Agg Brd
Beam-induced background rate ($\mathrm{MHz/cm}^2$)							
Higgs	6.4	3.0×10^{-3}	1.9×10^{-3}	2.4×10^{-3}	6.2×10^{-2}	2.4×10^{-4}	1.4×10^{-6}
LowZ	15.0	5.4×10^{-3}	3.1×10^{-3}	5.2×10^{-3}	1.0×10^{-1}	2.4×10^{-4}	9.2×10^{-7}
Data rate per Link (Mbps)							
Higgs	2.00×10^4	80.0	66.7	53.1	2.55×10^3	6.91	< 10
LowZ	4.71×10^4	144	109	115	4.11×10^3	6.91	< 10

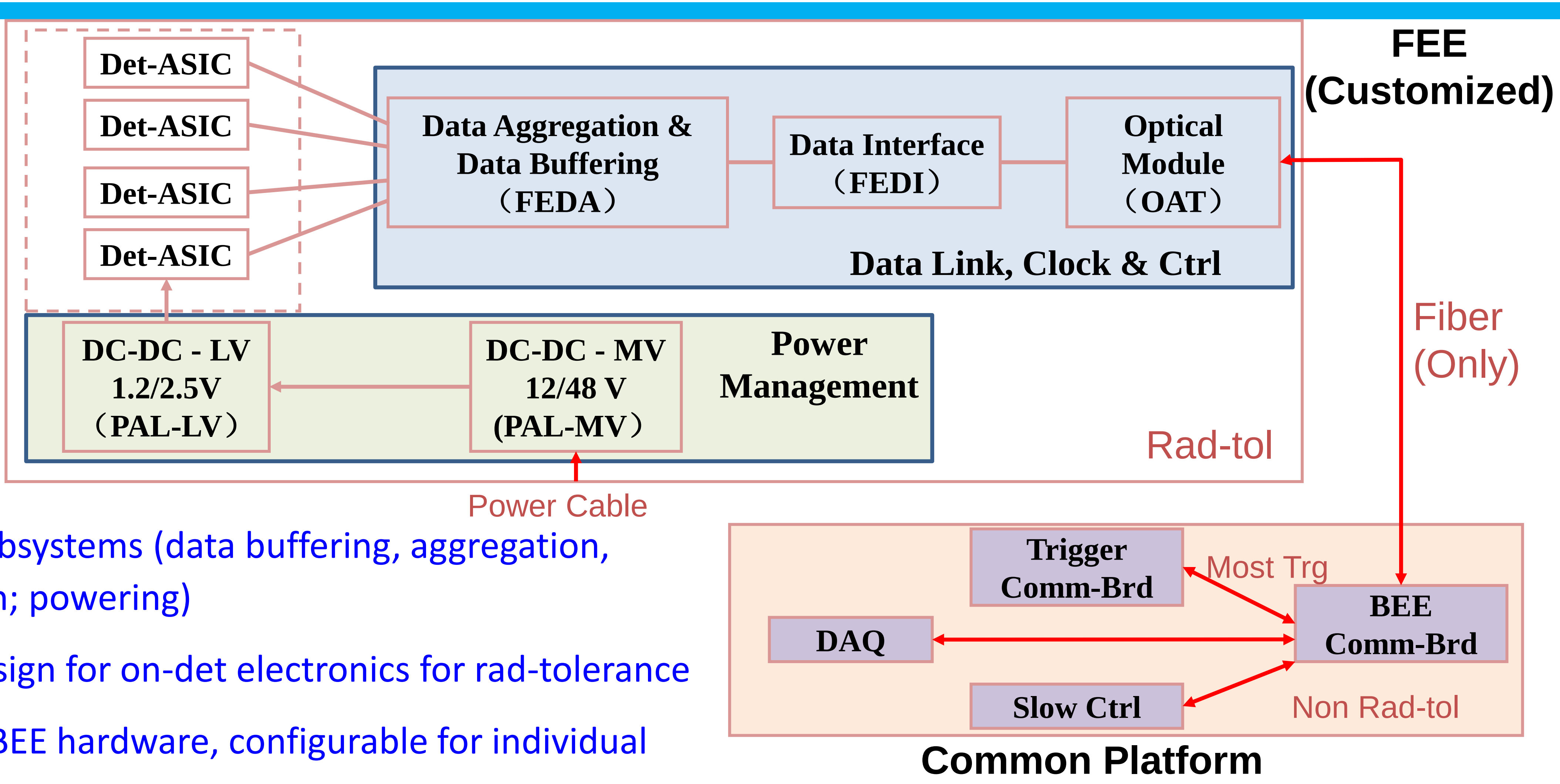
Time window and data rate for TDAQ system



	VTX	ITK	OTK	TPC	ECAL	HCAL	Muon	Total
Time windows (ns)	69	69	69	34000	69	1000	69	
50 MW Higgs mode Full Data (Gbps)	130	21.2	82.7	26.4	752	26.6	<1	1040
Data size / bunch (kB)	12.1	1.98	7.71	2.46	70.1	2.48	<0.1	96.9
Data size / event (kB)	12.1	1.98	7.71	303	70.1	9.92	<0.1	405
12.1 MW Z mode Full Data (Gbps)	307	37.8	139	57.1	1202	27.2	<1	1771
Data size / bunch (kB)	3.20	0.394	1.45	0.595	12.5	0.283	<0.1	18.4
Data size / event (kB)	6.40	0.788	2.90	293	25.0	4.53	<0.1	333

- Safety factor of 2 used for background rate estimation from MDI study
- Only Endcap data rate demonstrated for the highest requirements for the electronics
- Data rate includes: background rate * detector area * (possible) cluster size * data width
- MDI study is still in progressing, with more detailed distribution, radiation, and shielding

Overall framework of the CEPC Elec system



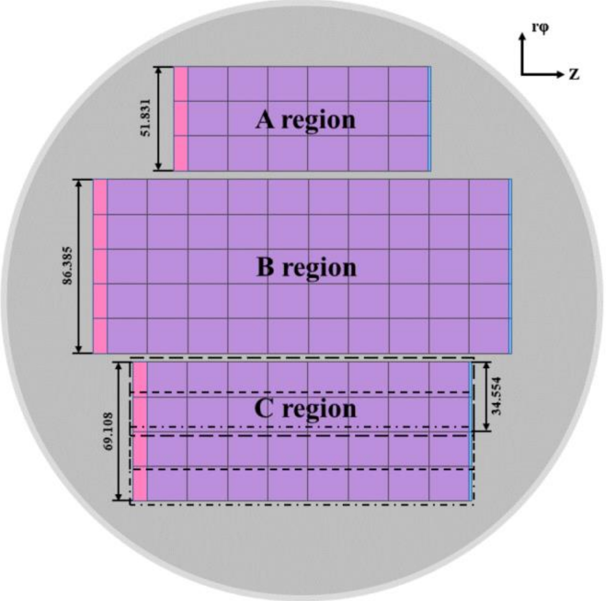
- Common subsystems (data buffering, aggregation, transmission; powering)
- Full ASIC design for on-det electronics for rad-tolerance
- A common BEE hardware, configurable for individual subsystems.
- TDAQ interface is (probably) only on BEE

Key Electronic Components

- FEE ASICs for sub-detectors
- Common FEE
  - Common Data Link
  - Common Powering

Vertex Detector Baseline layout

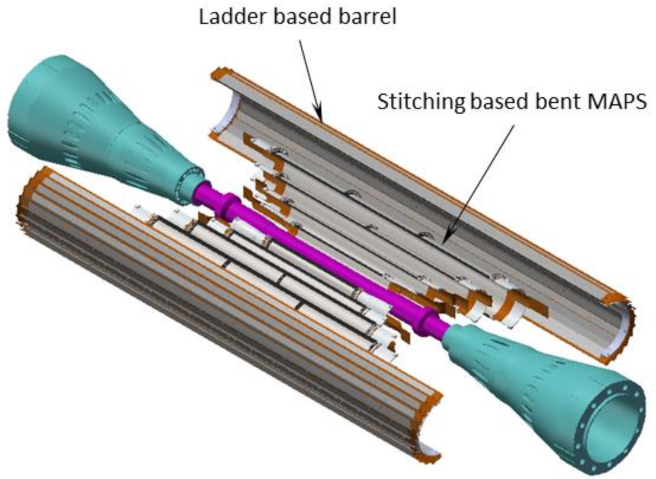
- Baseline :4 single layer of bent MAPS + 1 double layer ladders
  - Alternative option: 3 double layer ladders
- Inner layer: Use single bent MAPS for Inner layer (~0.15m^2)
  - Low material budget 0.06%X0 per layer
  - Different rotation angle in each layer to reduce dead area
- Outer layer: Double layer Ladder (~0.28% X0 per layer)

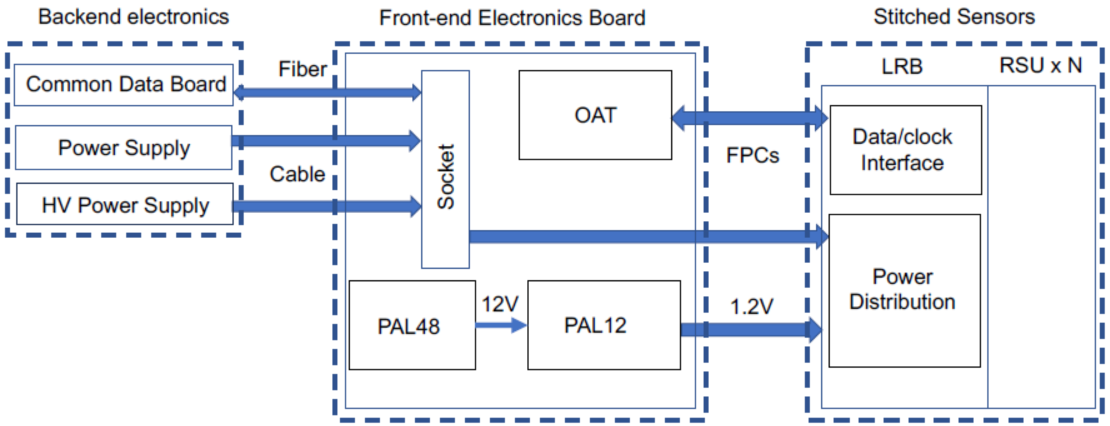


Long barrel layout (no endcap disk)

to cover cos θ<=0.991

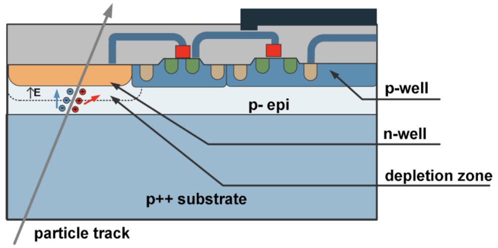
CVTX/ PVTX X	radius mm	length mm
CVTX 1	11.1	161.4
CVTX 2	16.6	242.2
CVTX 3	22.1	323.0
CVTX 4	27.6	403.8
PVTX 5	39.5	682.0
PVTX 6	47.9	682.0

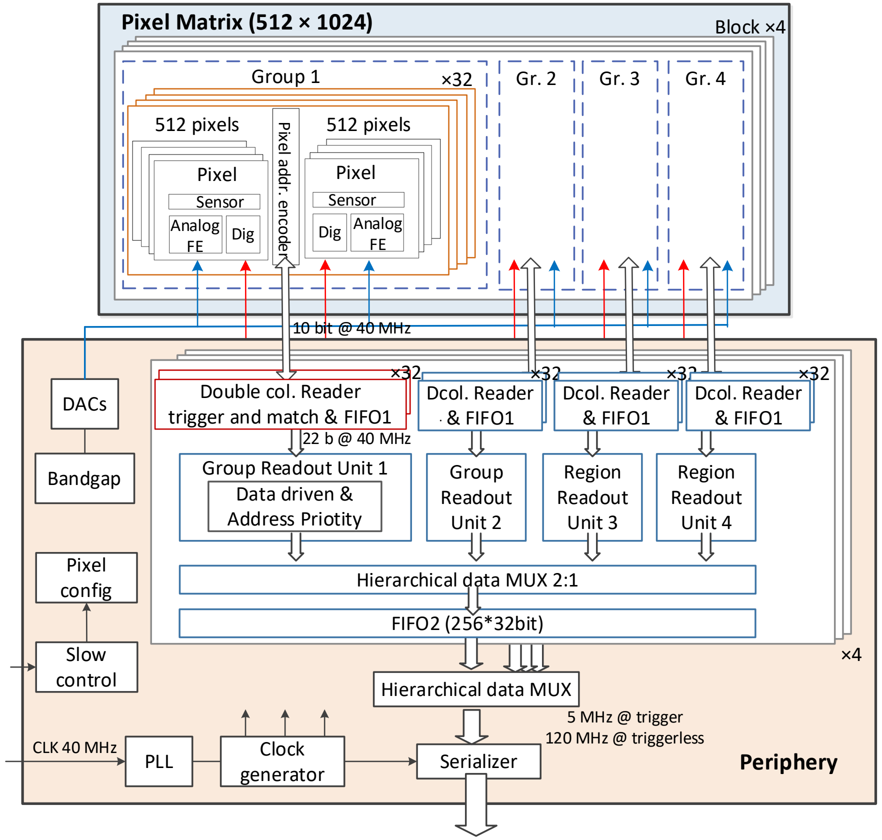




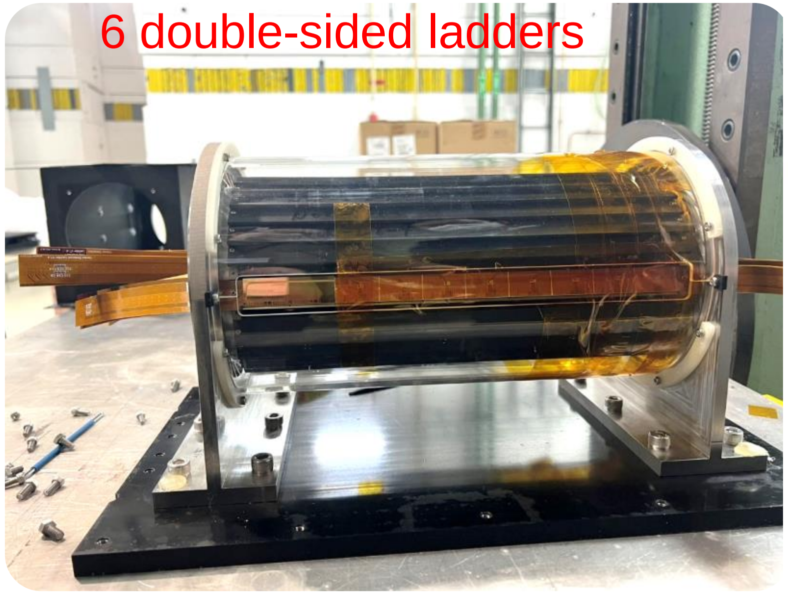
R&D effort: vertex detector prototype

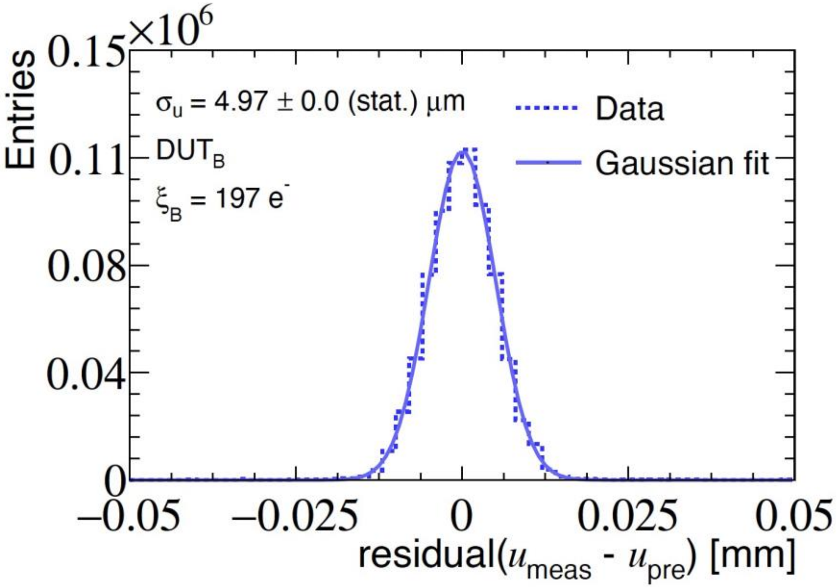
Monolithic Pixels





Ladder readout system





TaichuPix-based prototype detector tested at DESY in April 2023

Spatial resolution ~ **4.9 µm**

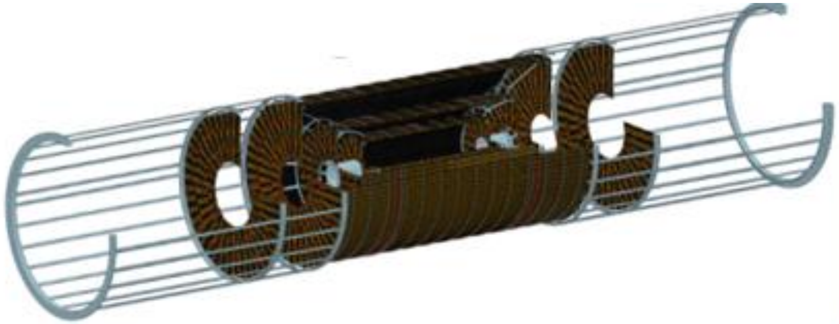
See Wei WEI's presentation in TWEPP2023: https://indico.cern.ch/event/1255624/contributions/5443785/

Choice of technology for next R & D

- Next step foundry: SK hynix system fab in Wuxi China (90nm technology with stitching feasibility)

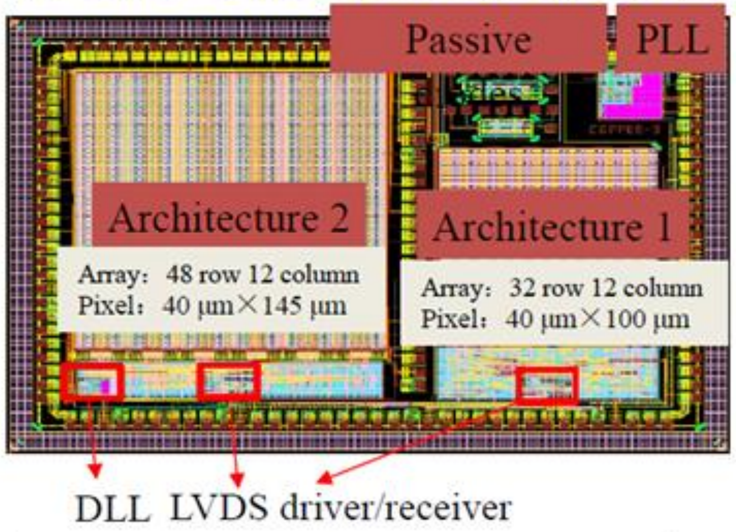
	Requirements	**TPSCo 65 nm**	**HLMC 55 nm**	**HC90L**
Feature size	55 – 90 nm	65 nm	55 nm	90 nm
Epitaxial layer thickness	10 - 25 μm	10 μm	3-5 μm	4 – 8.5 μm (default) Can be changed to 20μm
Resistivity of epi-layer	> 1 kΩ•cm	~130 Ω•cm	Low resistivity ~10 Ω•cm	30-50 Ω•cm (default) Can upgraded to 5kΩcm
Availability of deep N-well	Yes	Yes	Yes	Yes
Availability of deep P-well	Yes	Yes	Yes	Optional
Numbers of metal layers	> 6	Max. 7	Max. 5	Max. 5
Availability of stitching	Yes	Yes	Yes	Yes
Cost “ratio”(NRE)		1	0.85	0.3

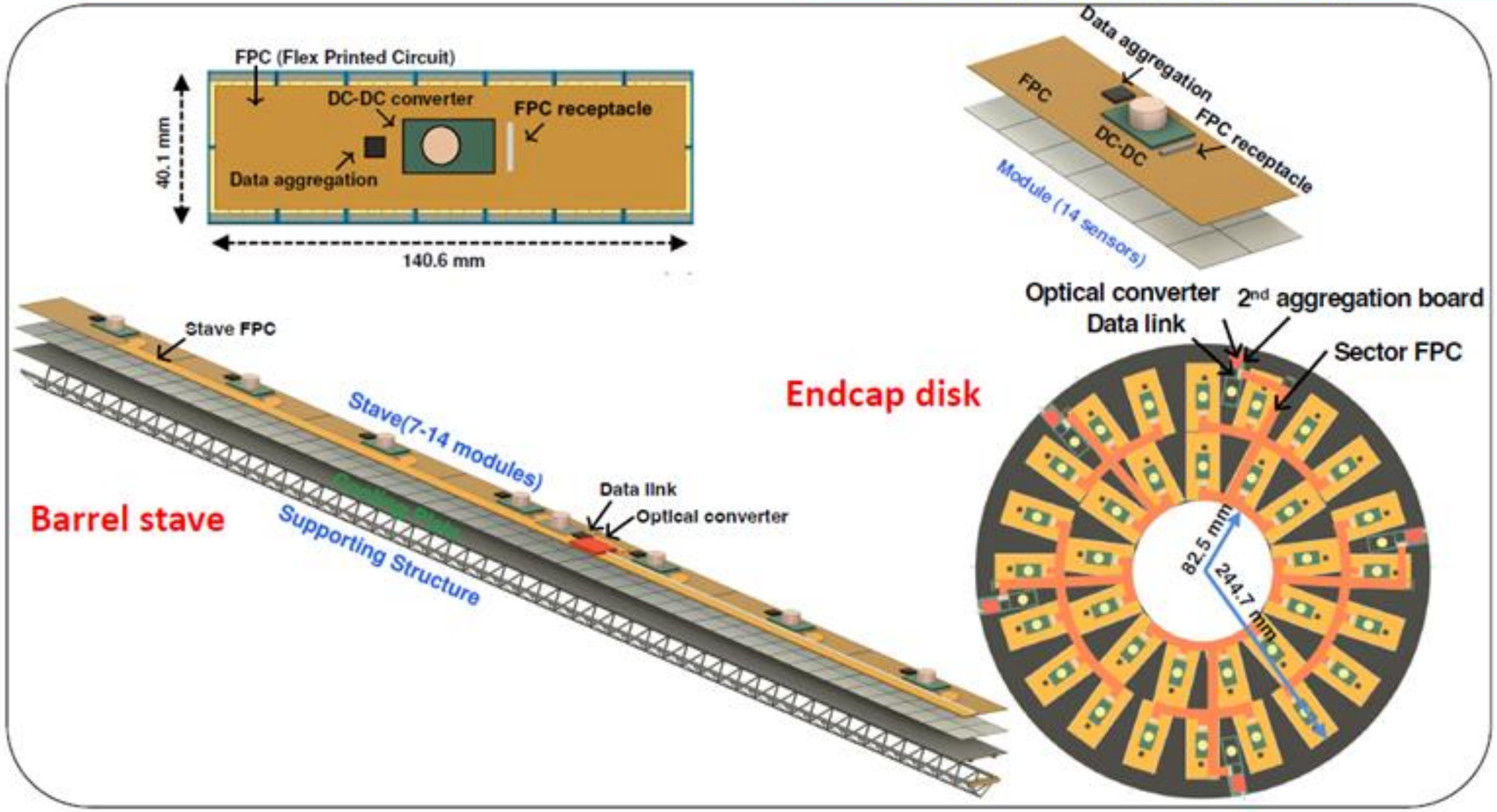
Inner Tracker with HV-CMOS Pixels



- ☐ Three barrel and four endcap layers (~20 m^2).
- ☐ HV-CMOS sensor COFFEE2 has verified the sensor process and in-pixel analog front-end.
- ☐ The latest COFFEE3 sensor, submitted for tape-out in Jan and received in May 2025, is currently undergoing testing.

HV-CMOS sensor prototype (COFFEE3)

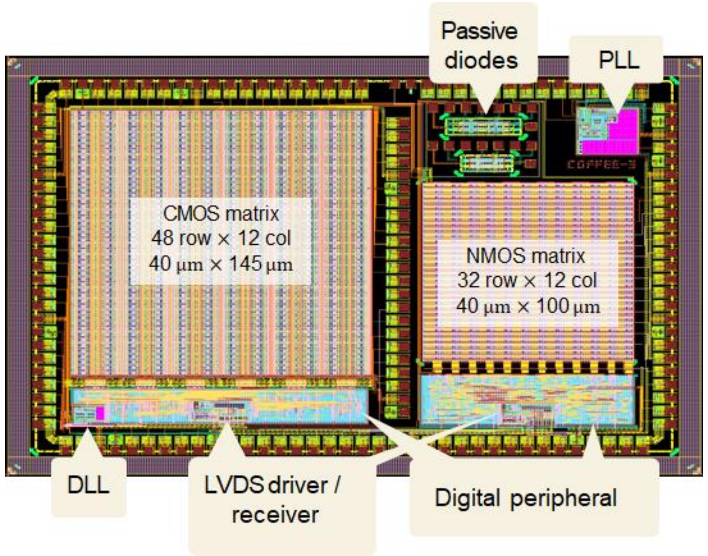


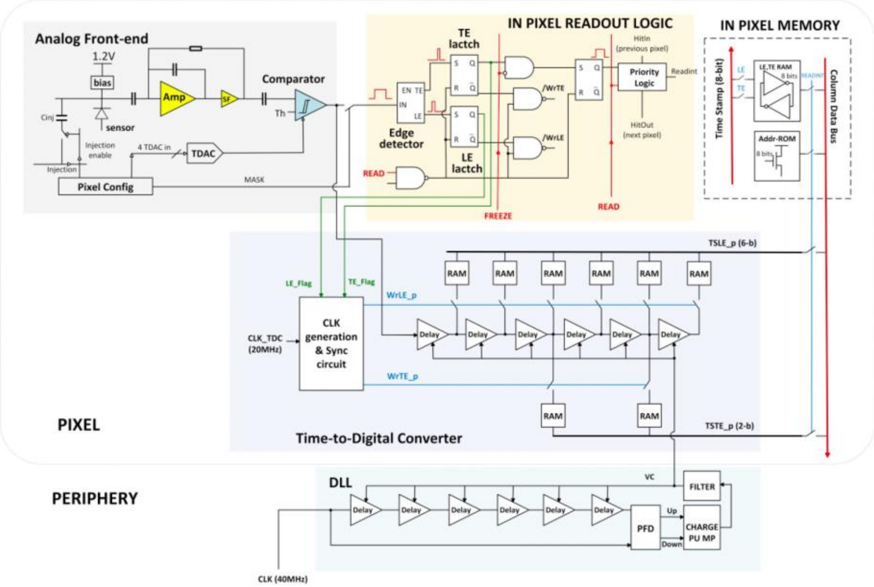


HV-CMOS sensor specification for ITK	
Sensor size	2 cm × 2 cm
Sensor thickness	150 µm
Array size	512 × 128
Pixel size	34 µm × 150 µm
Spatial resolution	8 µm × 40 µm
Timing resolution	3-5 ns
Power	200 mW/cm^2
Process node	55 nm

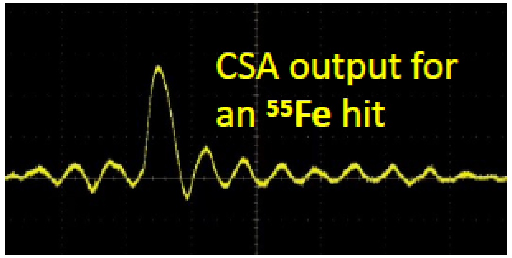
See Yang Zhou’s talk on Friday

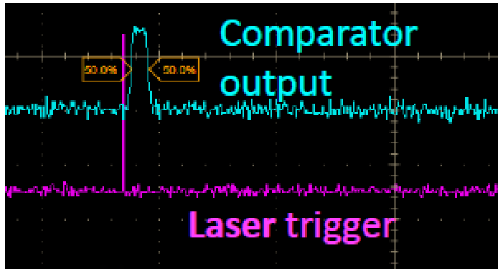
R&D Progress on HV-CMOS Pixel Sensor COFFEE



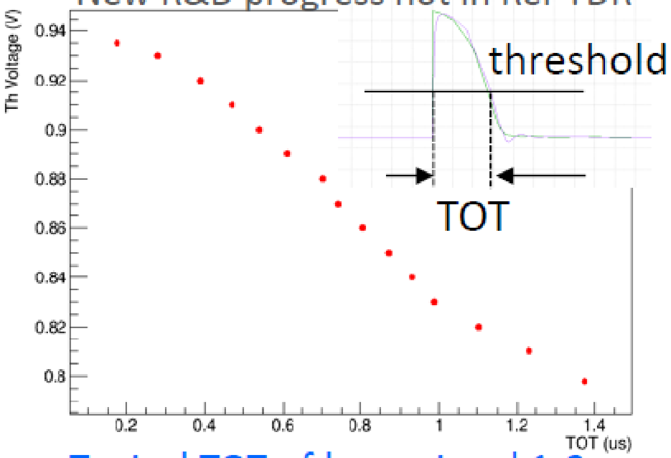


- COFFEE3 chip designed on 55nm HVCMOS
  - ‘CMOS matrix’: digital TDC in pixel
  - ‘NMOS matrix’: limited design flexibility yet no crosstalk using 3- well
  - IP validations: PLL, DLL, LVDS driver/ receivers …

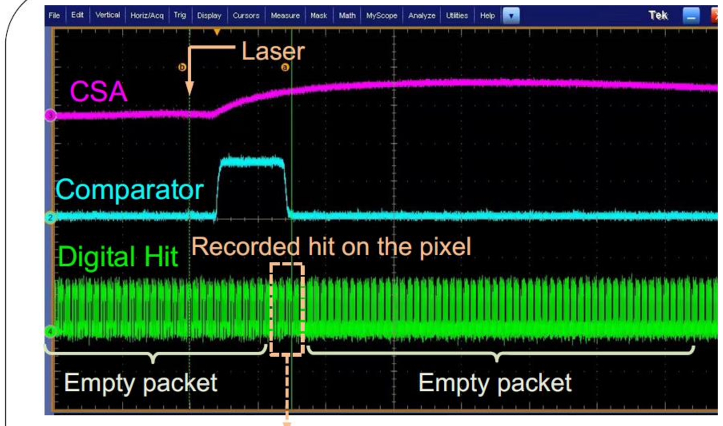




New R&D progress not in Ref-TDR



Typical TOT of laser signal 1-2 μs, consistent with simulation



4 bit	4 bit	8 bit	8 bit	6 bit	2 bit	7 bit	3 bit
header	CHIP_TS	LE_coarse	TE_coarse	LE_fine	TE_fine	Addr_Row	Add_Col
0 1 1 0	0 1 0 1	0 0 0 1 0 1 1 0	0 1 1 0 1 0 1 1	1 1 0 0 0 0	0 0	0 0 0 0 0 0 1	0 0 0

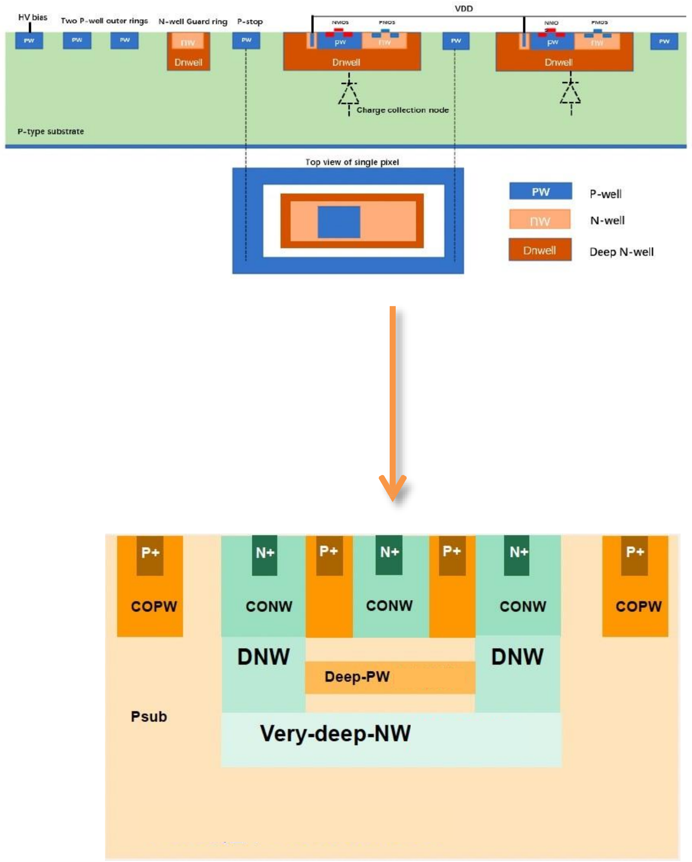
A valid transmission packet corresponding to a hit

Correct row & column address

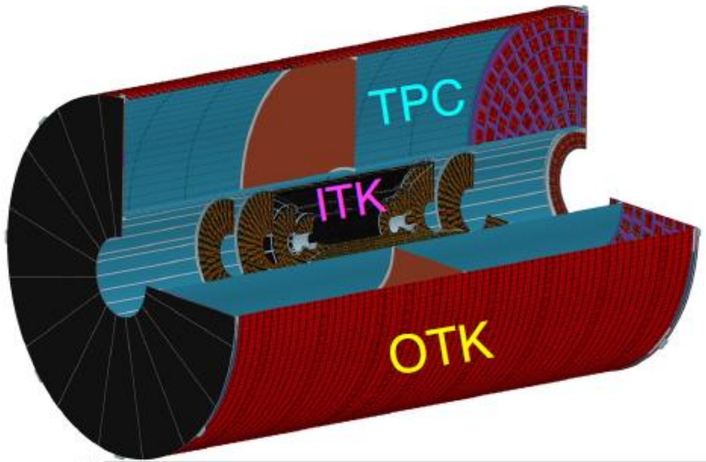
New R&D progress not in Ref-TDR

COFFEE status: CHiR chip submitted

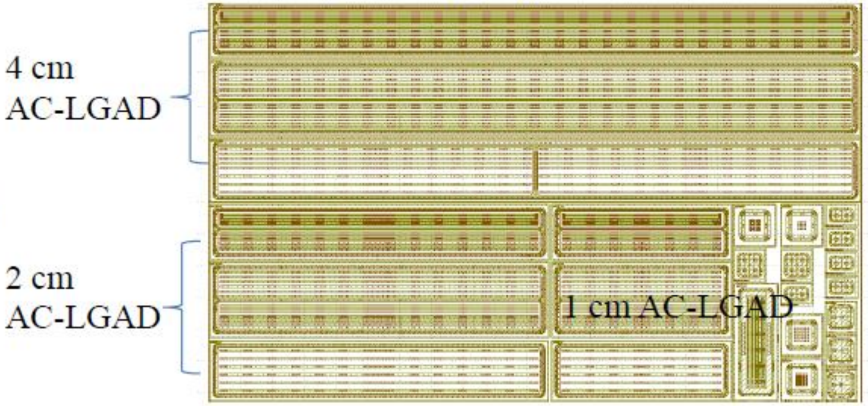
- Limitation of previous foundry:
  - No access of high-resistivity wafers
  - Triple-well process → cross-talk between sensor (deep-n) and PMOS circuit
- Agreement with a new foundry to carry on R&D
- First MPW submitted in early January 2026
- CHiR (COFFEE-HiRes) design goal
  - Priority: to validate the process with high-res wafers
    - 1k/2k/4k Ohm cm wafers available from two manufactures
  - Radiation effects of simple components (eg. MOS) with or w/o radiation hardening
  - Implementation of "Five-well process": to validate basic IP not affected by process modification



Outer Tracker Based on AC-LGAD Sensor



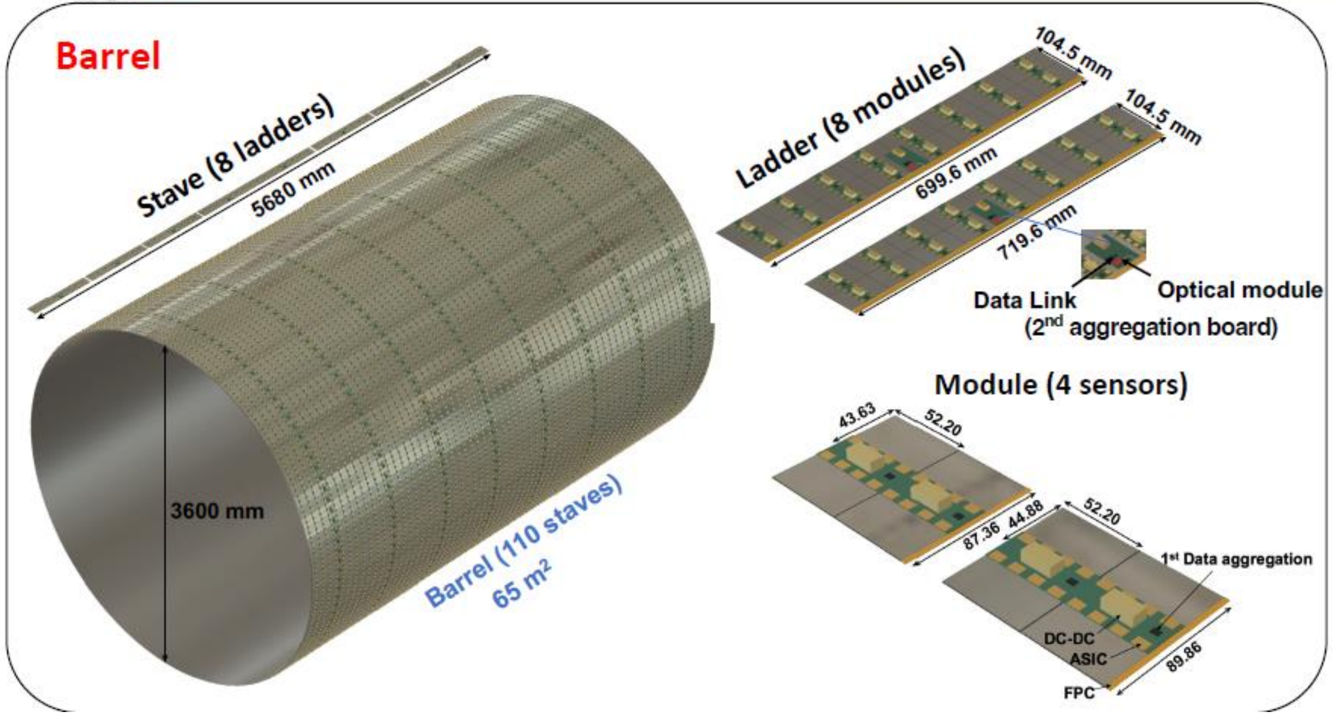
AC-LGAD prototype (latest submitted)



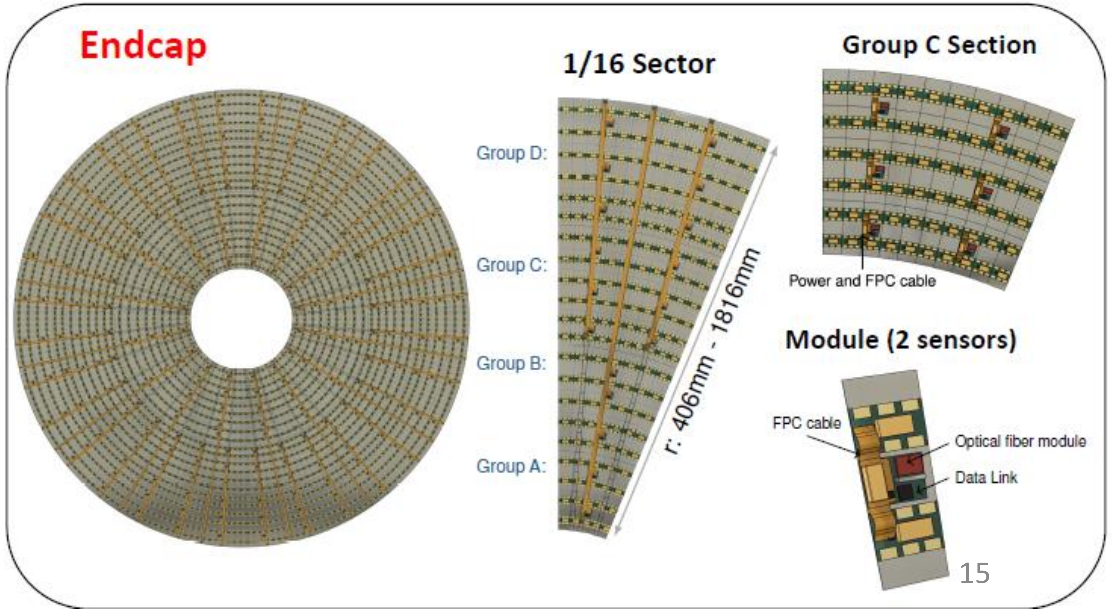
- ❑ One barrel layer and one endcap layer (~85 m^2).
- ❑ The latest LGAD sensor was submitted for tape-out in March and waiting for the return.

LGAD sensor specification for OTK	
Sensor size	(3-4.5) cm × (3-5) cm
Strip pitch	~100 μm
Spatial resolution	10 μm
Timing resolution	50 ps
Power	300 mW/cm^2

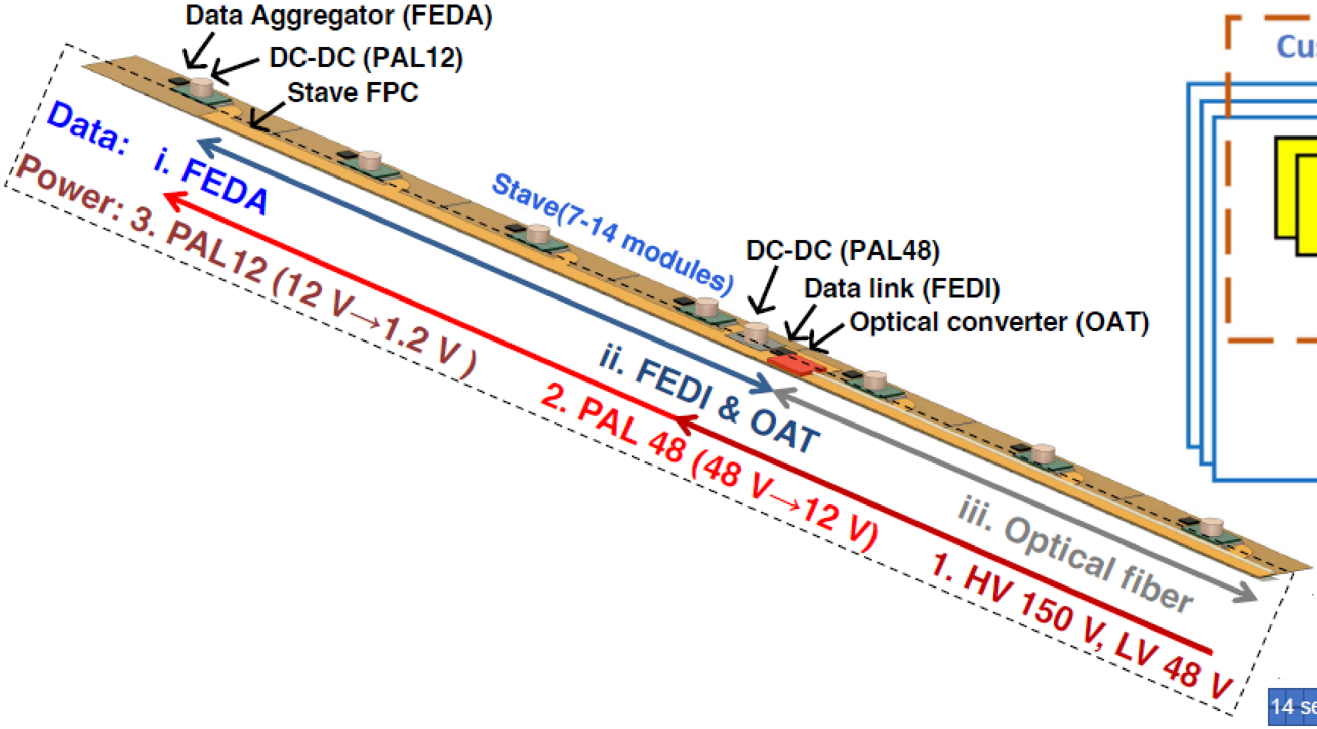
Barrel

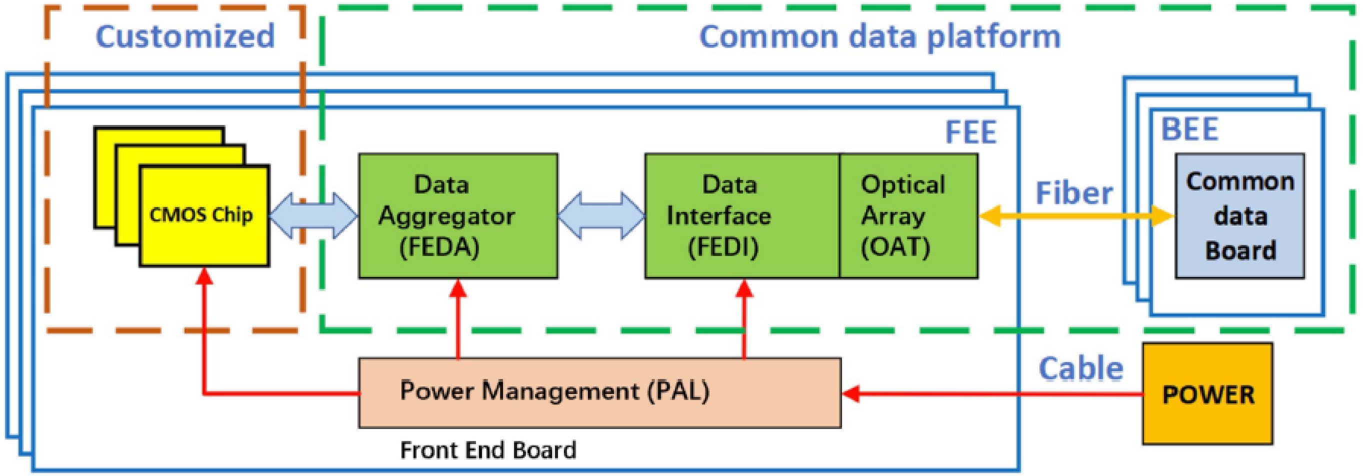


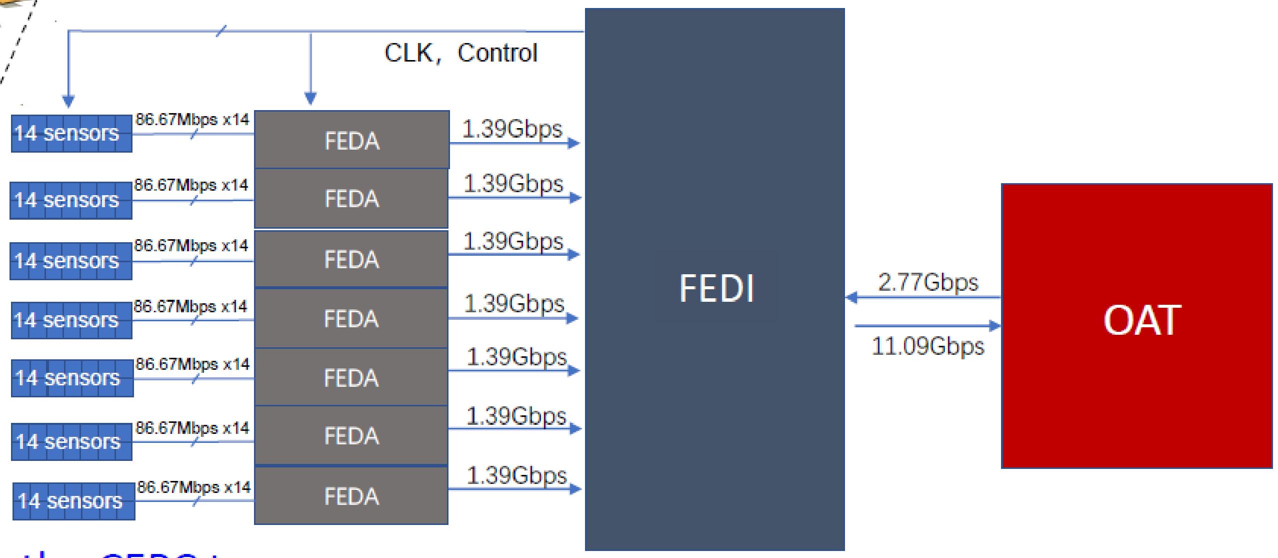
Endcap



Readout Electronics framework for TRK







- In the readout design, each sensor can tolerate up to 86.67 Mbps, corresponding to a maximum hit rate of 4.1×10^{5} Hz/cm^{2} – about 42 times higher than the estimated peak background hit rates (9.9×10^{3} Hz/cm^{2}) under the most challenging high-luminosity Z-pole operation mode.

The FEDA, FEDI, OAT, and PAL chips are under development by the CEPC team.

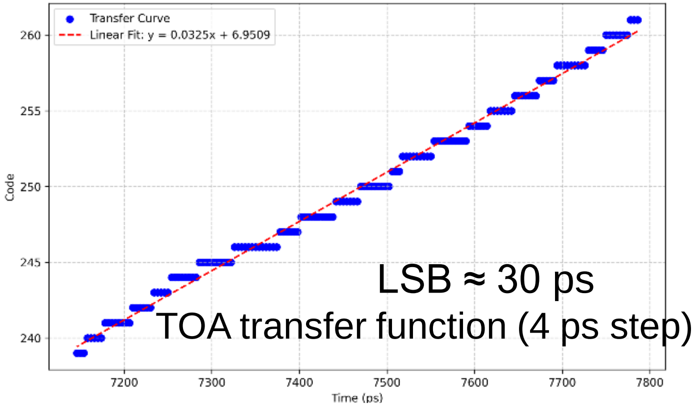
See Xiongbo YAN’s talk on Thursday

Progress on AC-LGAD readout chip LATRIC

Two versions in 2025 Aug and Oct.

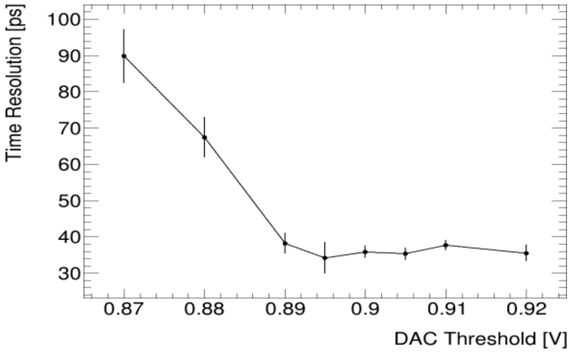
- It integrates Preamplifer, Discriminator, TDC, and Serializer.
- LATRIC-V0, with LSB of 29.8 ps, has been verified.

Tested with LGAD by wire bonding

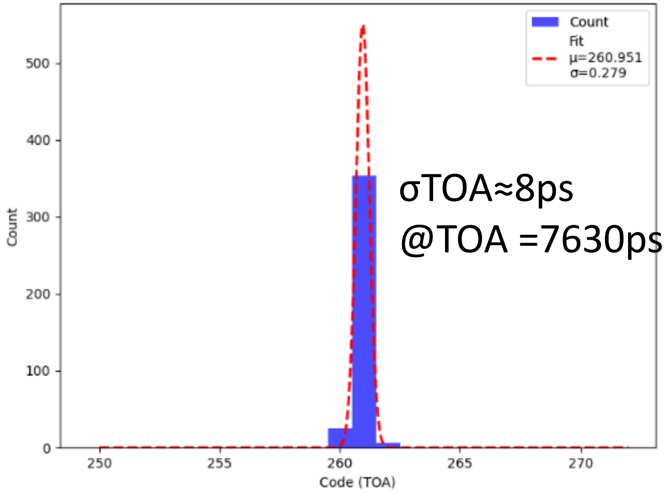


LSB ≈ 30 ps

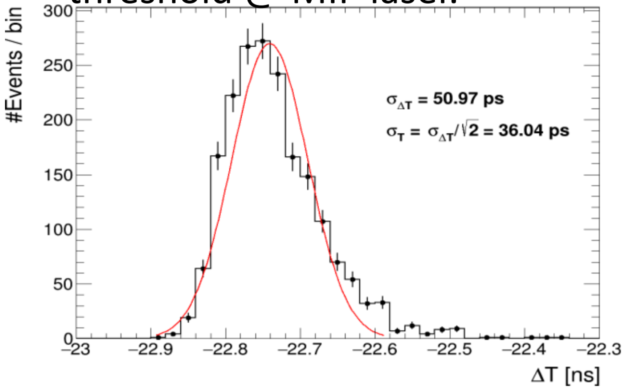
TOA transfer function (4 ps step)



The resolution deceases with threshold @ MIP laser.



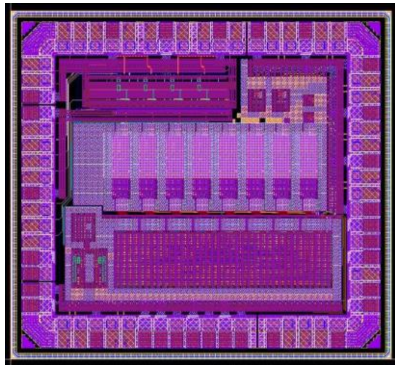
σTOA≈8ps
@TOA =7630ps



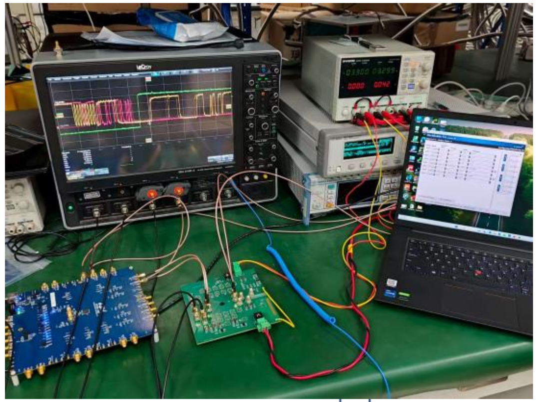
$\sigma_{\Delta T}$ = 50.97 ps

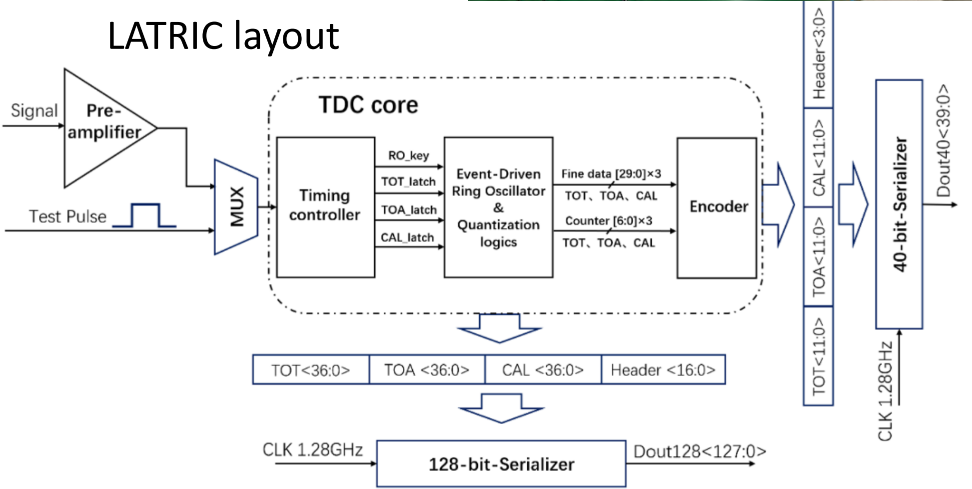
$\sigma_T = \sigma_{\Delta T}/\sqrt{2}$ = 36.04 ps

LATRIC + LGAD TOA coincidence
@ Laser intensity = MIP



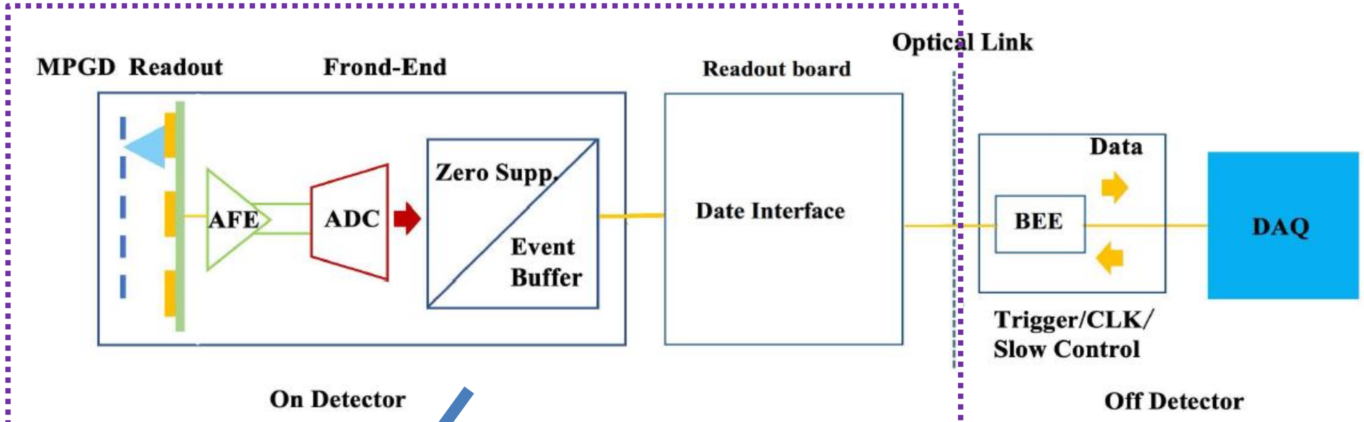
LATRIC layout

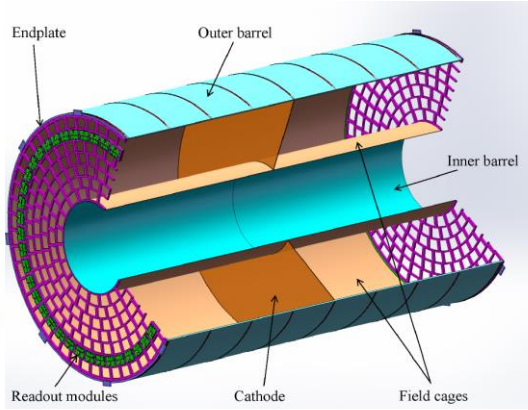


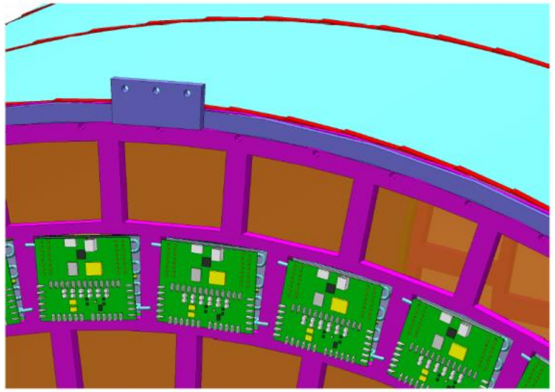


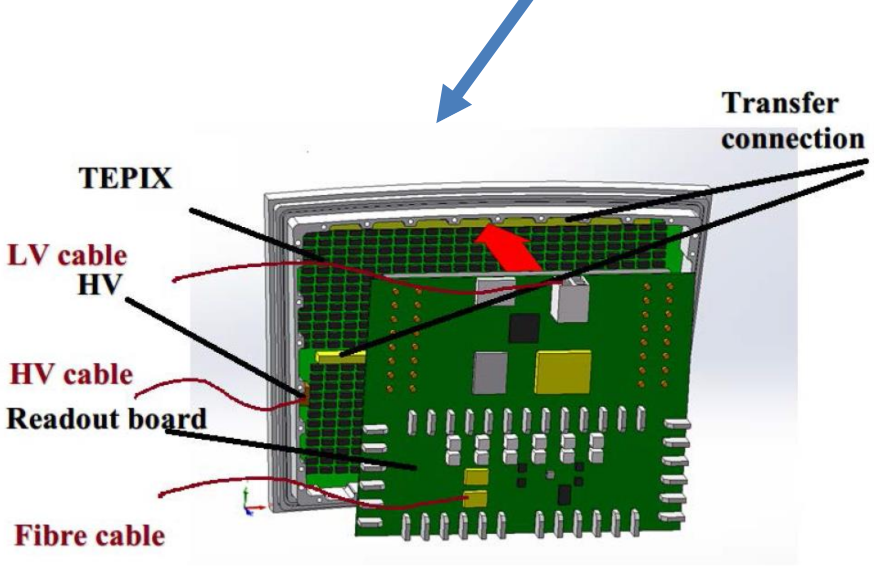
TPC readout electronics

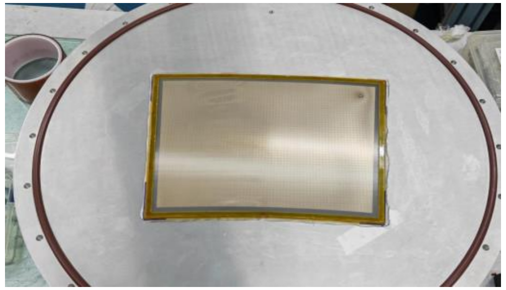
Electronics











On detector: readout modules

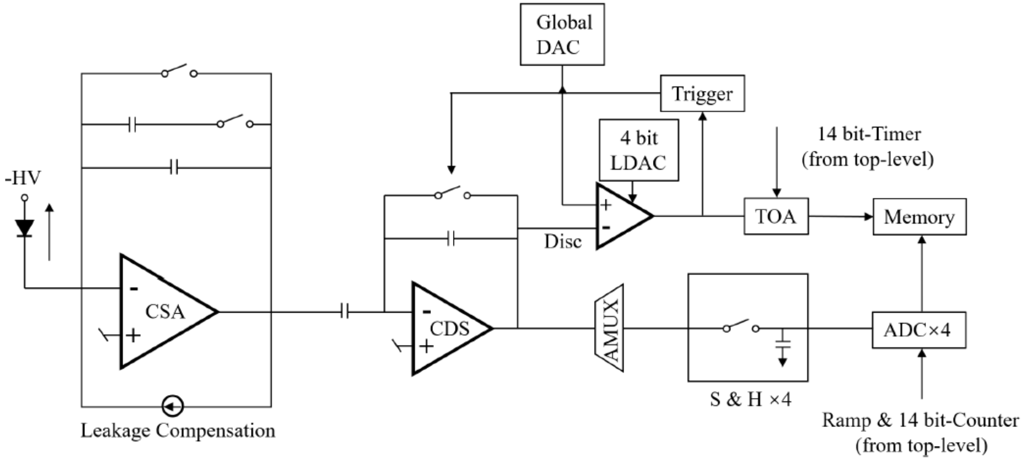
- Double-mesh Micromegas with high granularity readout (500μm × 500μm pad size) for electron multiplication and IBF suppression
- FEE board: a readout ASIC chip array. Interposer connection between pads and ASIC chis
- Readout board: data interface and data concentrator

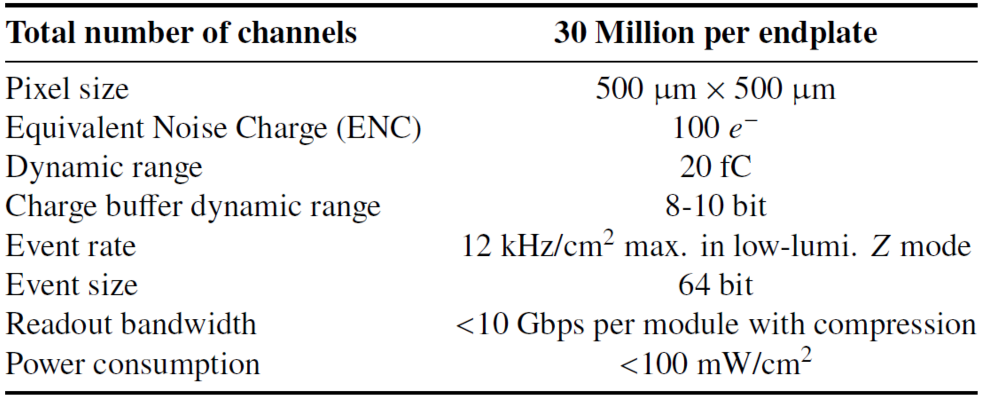
Off detector:

- High-speed optical links
- Off-detector BEE
- Data Acquisition (DAQ) system

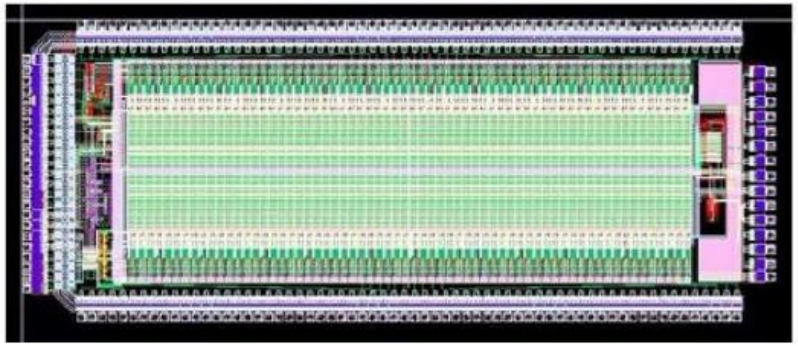
Detailed design of readout ASIC

- Readout ASIC
  - Low-power readout ASIC: TEPIX
    - Charge-sensitive preamplifier
    - Correlated double sampling shaper
    - 4-channel sample/hold circuits and 8-10 bit ADC
    - 14 bit-timer (from top-level)
  - Enabling precise charge (8-10 bit) and time-of-arrival (14-bit, 5 ns resolution) measurements





Total number of channels	30 Million per endplate
Pixel size	500 μm × 500 μm
Equivalent Noise Charge (ENC)	100 e^-
Dynamic range	20 fC
Charge buffer dynamic range	8-10 bit
Event rate	12 kHz/cm^2 max. in low-lumi. Z mode
Event size	64 bit
Readout bandwidth	<10 Gbps per module with compression
Power consumption	<100 mW/cm^2

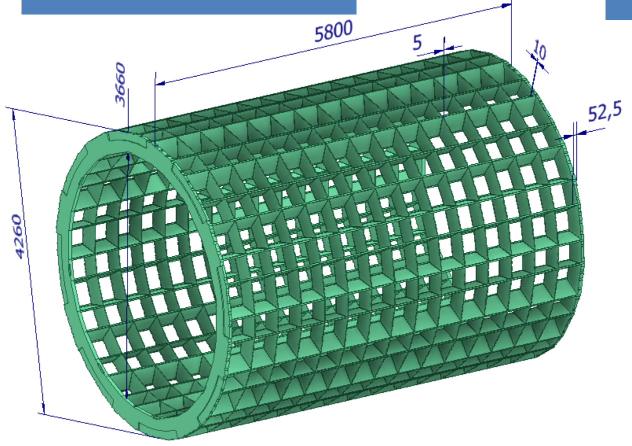


- TEPIX prototype
  - 128 channels using 180 nm process
  - Chip size: 2.2 mm × 5.6 mm

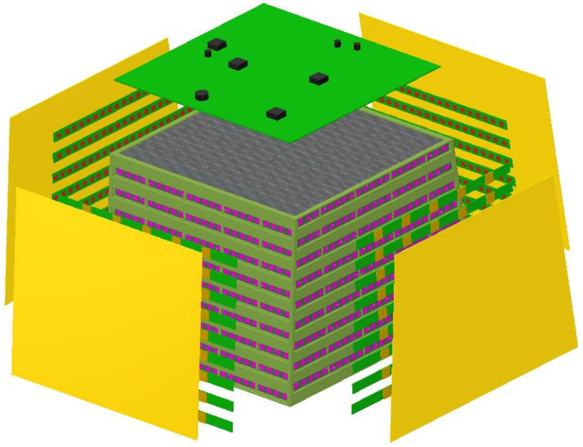
- The pixel-array based chip will be designed, when the optimized pad-size of the TPC eventually determined

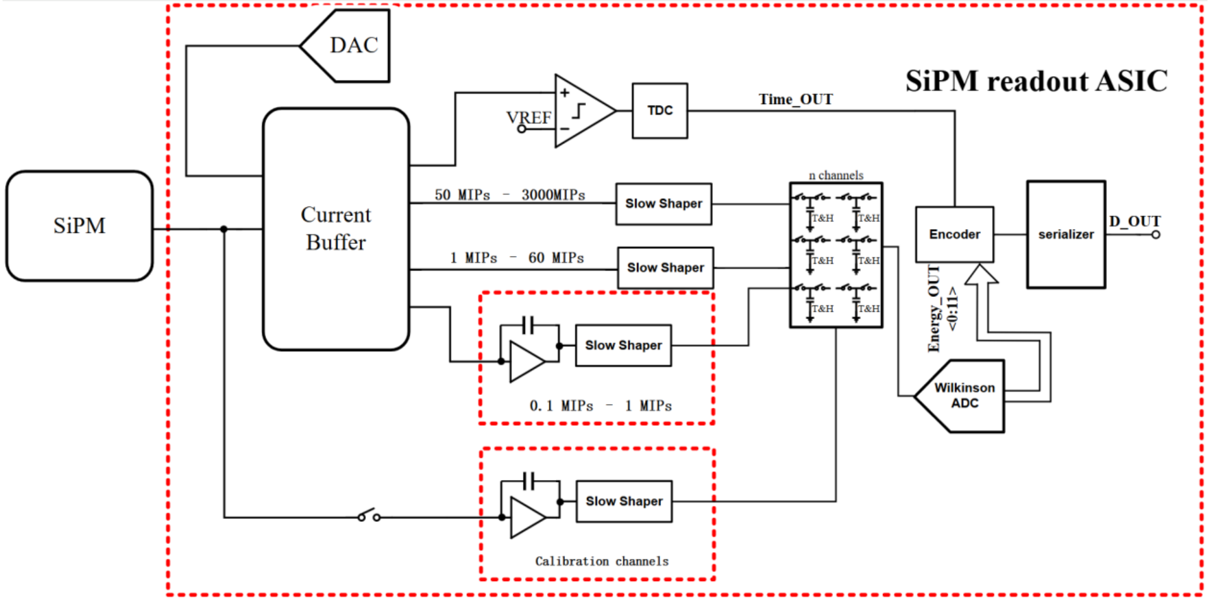
ECAL readout electronics

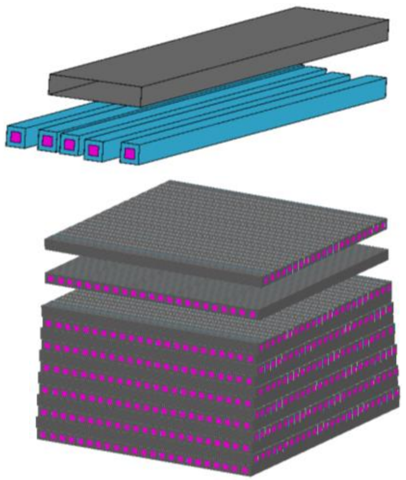
Main Structure



Module Integration







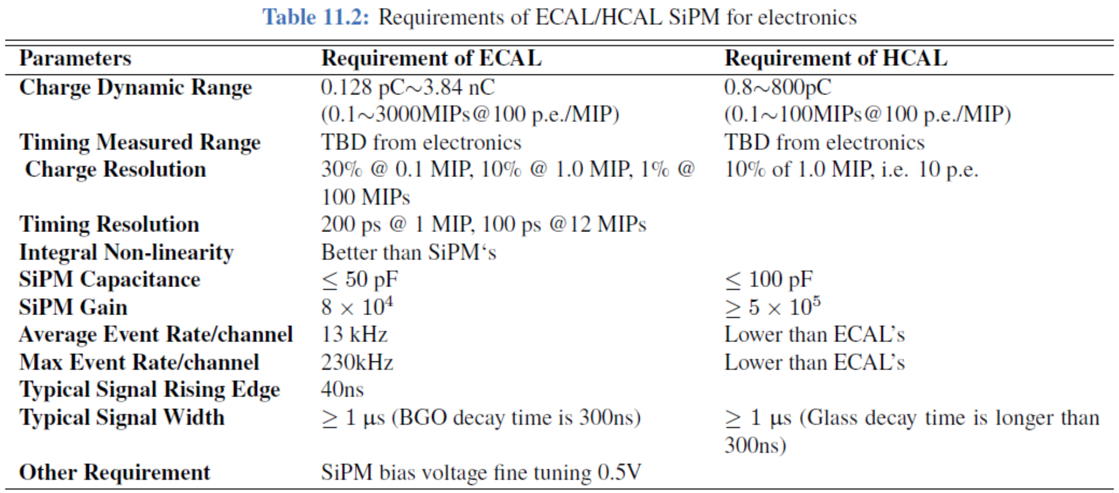


Table 11.2: Requirements of ECAL/HCAL SiPM for electronics

Parameters	Requirement of ECAL	Requirement of HCAL
Charge Dynamic Range	0.128 pC∼3.84 nC (0.1∼3000MIPs@100 p.e./MIP)	0.8∼800pC (0.1∼100MIPs@100 p.e./MIP)
Timing Measured Range	TBD from electronics	TBD from electronics
Charge Resolution	30% @ 0.1 MIP, 10% @ 1.0 MIP, 1% @ 100 MIPs	10% of 1.0 MIP, i.e. 10 p.e.
Timing Resolution	200 ps @ 1 MIP, 100 ps @12 MIPs	
Integral Non-linearity	Better than SiPM's	
SiPM Capacitance	≤ 50 pF	≤ 100 pF
SiPM Gain	8×10^4	$\geq 5 \times 10^5$
Average Event Rate/channel	13 kHz	Lower than ECAL's
Max Event Rate/channel	230kHz	Lower than ECAL's
Typical Signal Rising Edge	40ns	
Typical Signal Width	≥ 1 μs (BGO decay time is 300ns)	≥ 1 μs (Glass decay time is longer than 300ns)
Other Requirement	SiPM bias voltage fine tuning 0.5V	

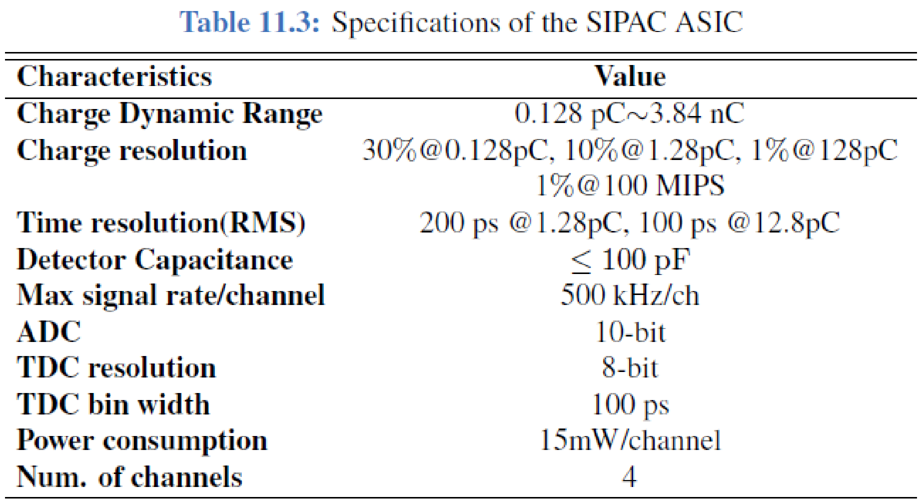
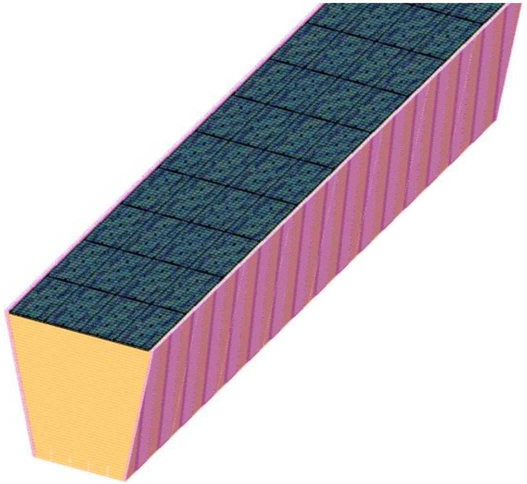
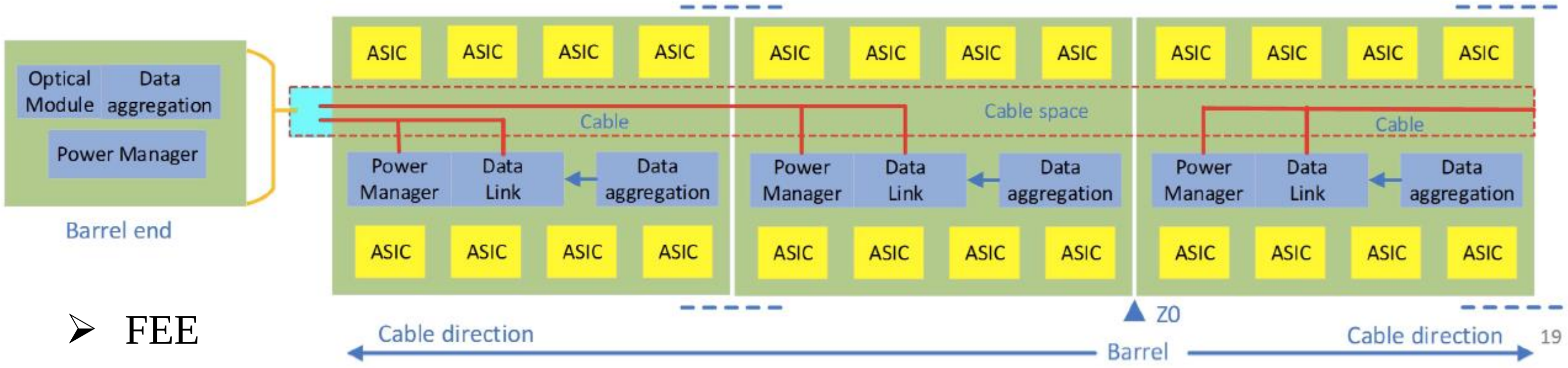


Table 11.3: Specifications of the SIPAC ASIC

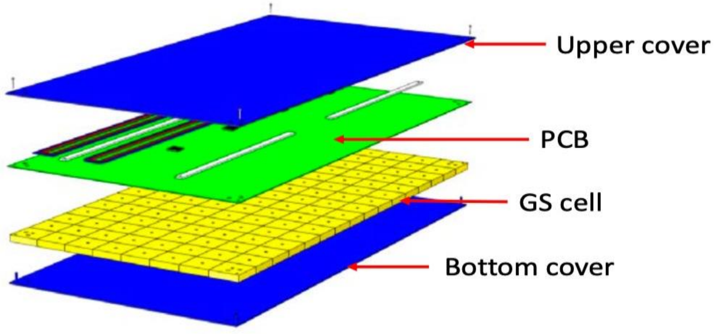
Characteristics	Value
Charge Dynamic Range	0.128 pC∼3.84 nC
Charge resolution	30%@0.128pC, 10%@1.28pC, 1%@128pC 1%@100 MIPS
Time resolution(RMS)	200 ps @1.28pC, 100 ps @12.8pC
Detector Capacitance	≤ 100 pF
Max signal rate/channel	500 kHz/ch
ADC	10-bit
TDC resolution	8-bit
TDC bin width	100 ps
Power consumption	15mW/channel
Num. of channels	4

HCAL readout electronics

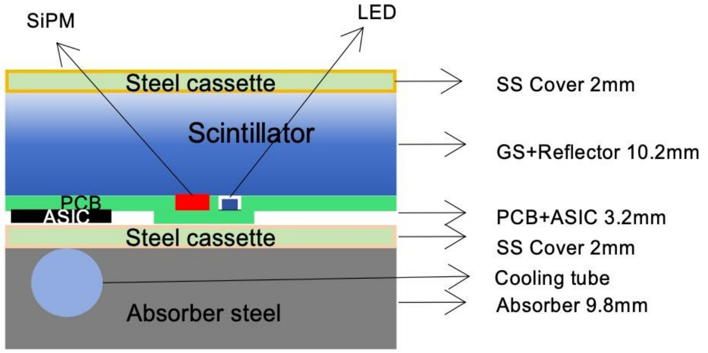




- FEE



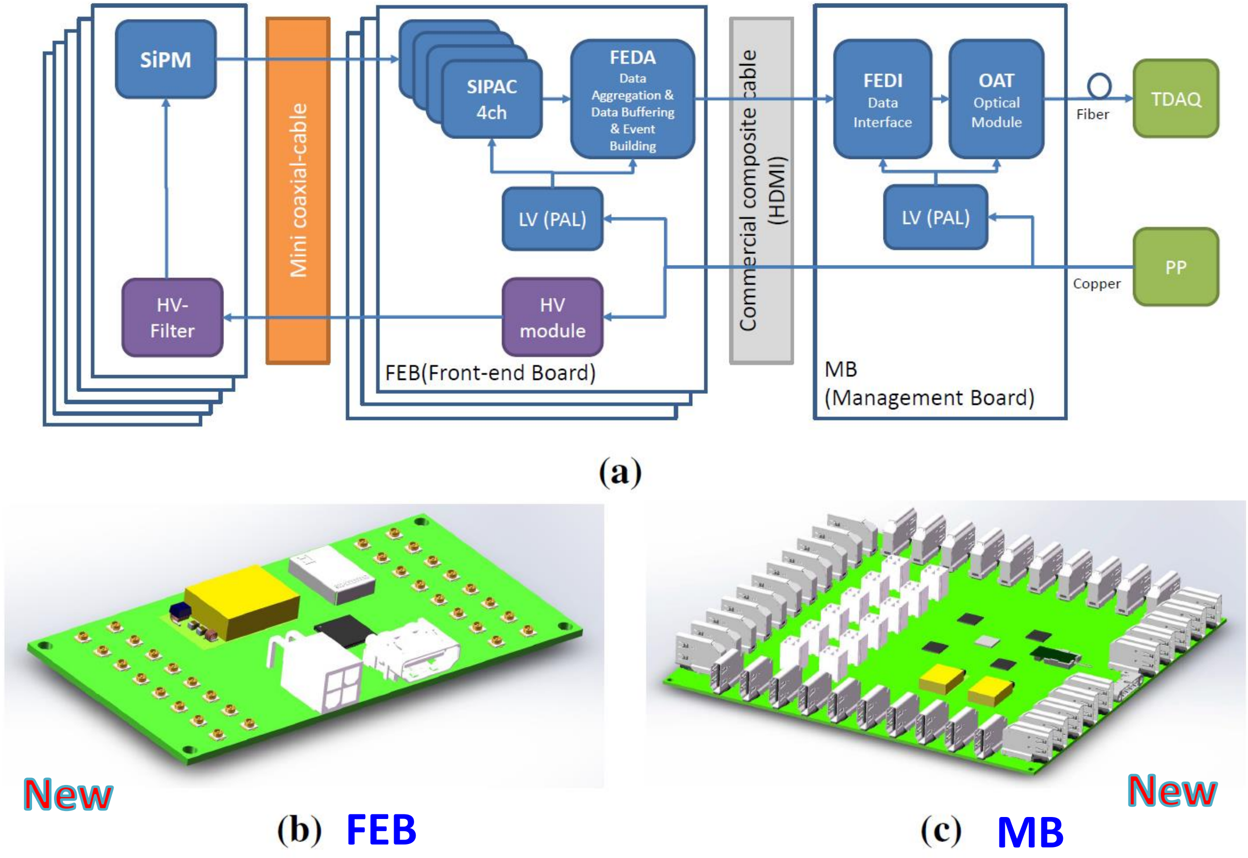
- **Front-End Electronics (FEE) readout boards in HCAL cell Box**
  - Thickness: 3.2mm = PCB 1.2mm + ASIC Chip 2mm
  - SiPMs, ASICs and Data Aggregation
  - PCB dimensions: flexible in different positions
- **SiPM-readout ASIC: under development**
  - Self-developed for CEPC calorimeter system
  - Functionality: energy and time measurements
  - Power consumption: target at 15mW/ch
- **Aggregation board at the end of barrel, cable connection**



See Mingkuan YUAN’s Poster ID 108

Muon readout electronics

- According to the R&D results and required performance: $N_{pe} > 200, \sigma_T < 0.5ns$
- Use the same chip designed for calorimeter, but customize the FEB based on ASIC according to the constraints in detector modules.
- Three stages for readout
  - SiPM tile: SiPM on PCB
  - FEB: Front-End Electronics Board, each having 32 chs, mini HV generator integrated.
  - MB: Management Board, central node for multiple functions.



(a)

New

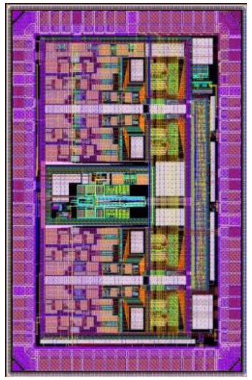
(b) FEB

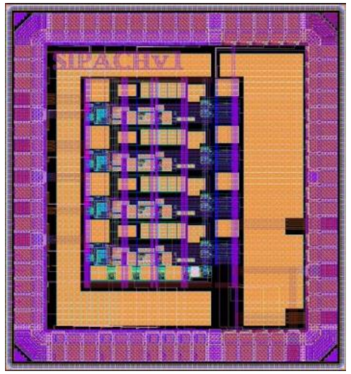
New

(c) MB

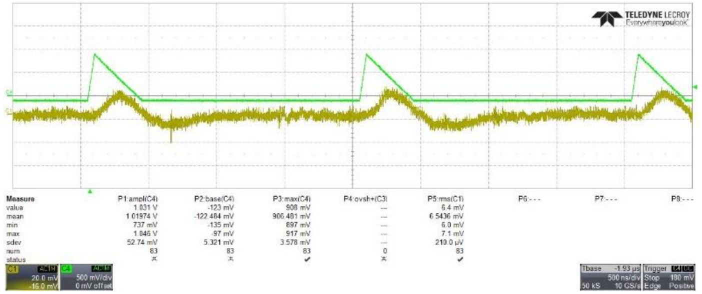
Fig. 9.3

Progress on SiPM readout ASIC SIPAC

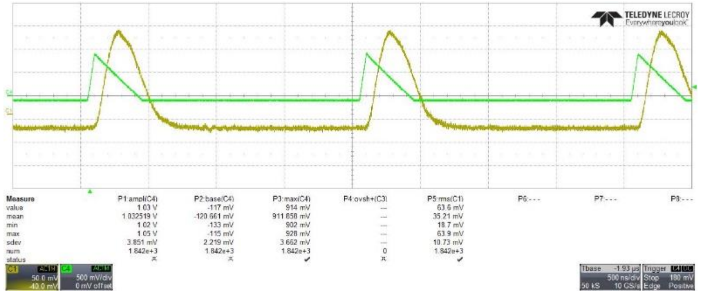

SIPAC-E



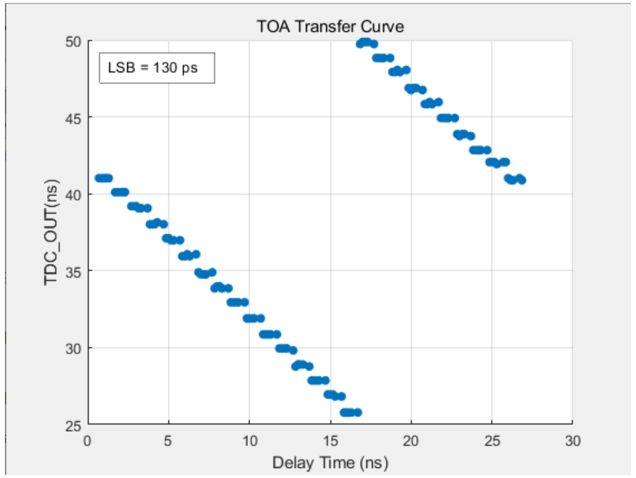
SIPAC-H



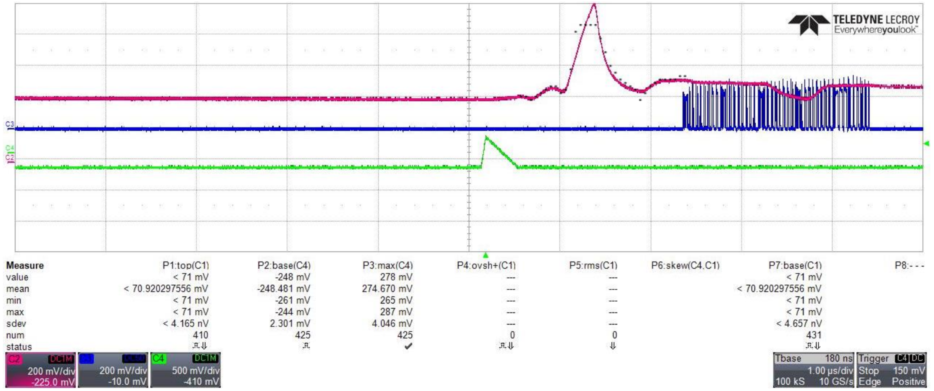
High gain output (yellow, 20mV small)



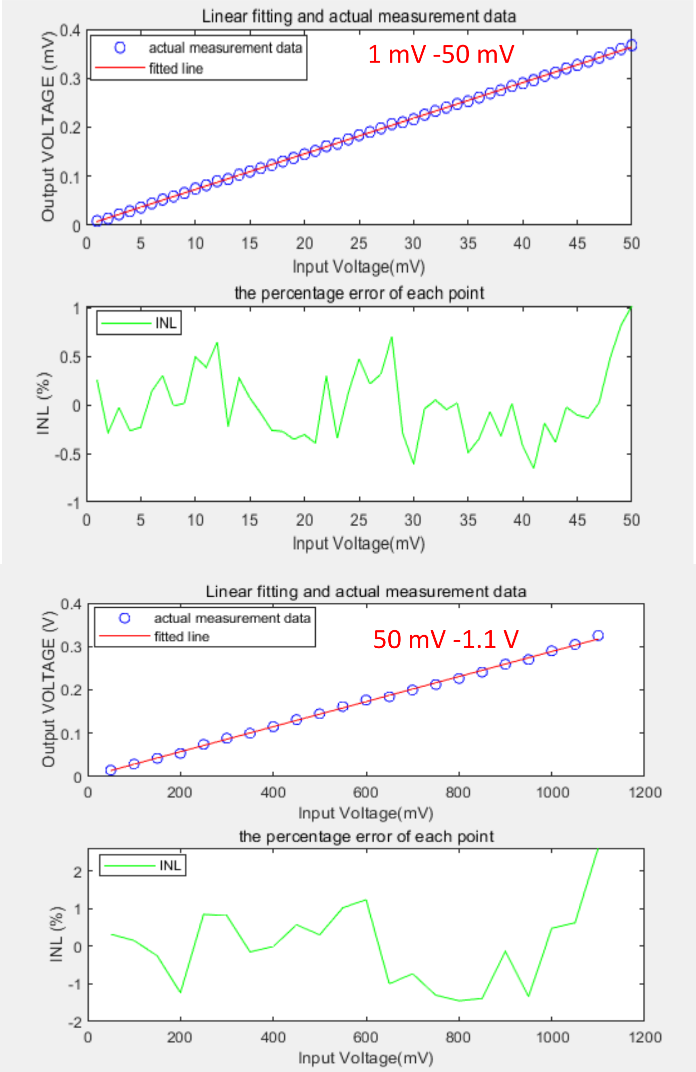
Low gain output (yellow, 200mV large)



TDC tested transfer curve



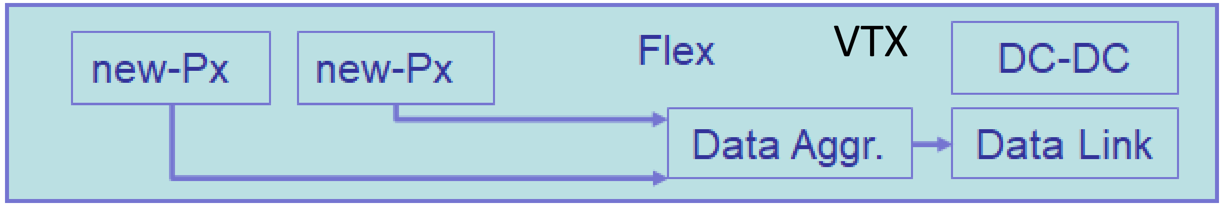
ADC digitization functionality test



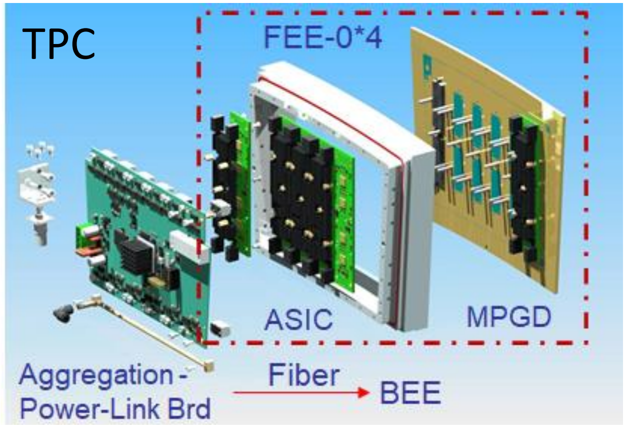
Dynamic range
of the high/low gain range

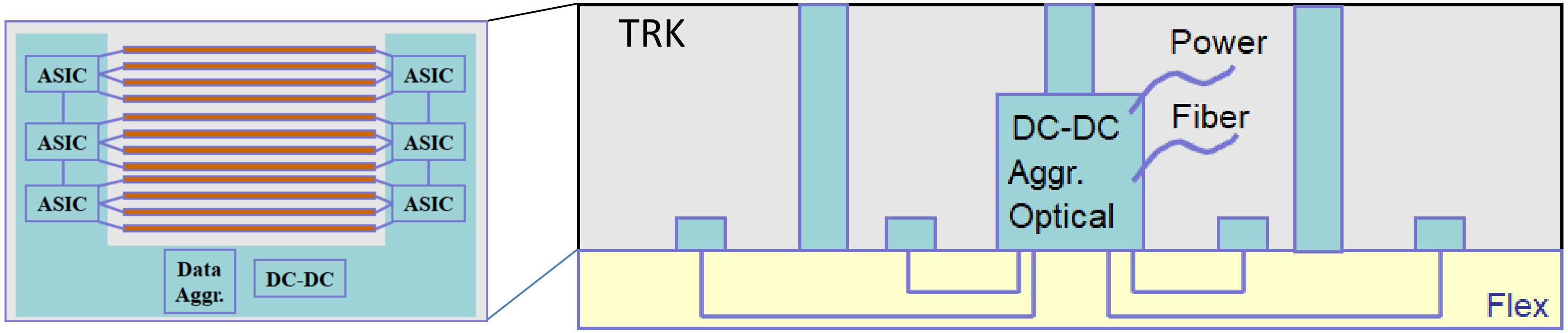
- Preliminary test results achieved, further test ongoing

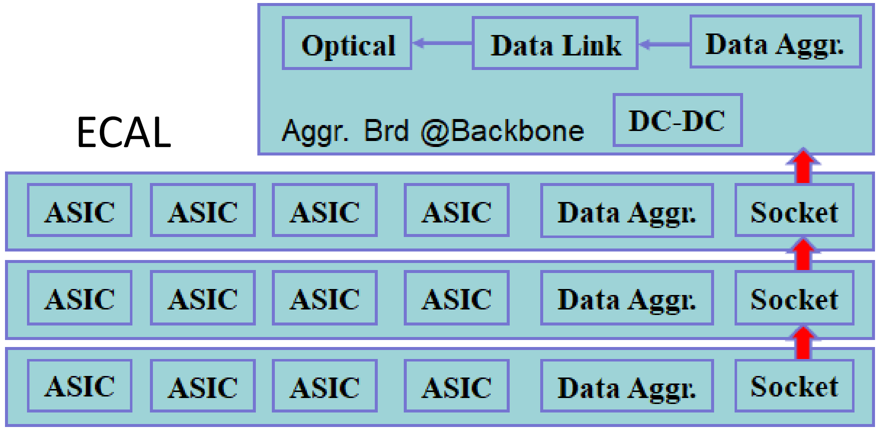
An overview of the Sub-Det readout Elec.

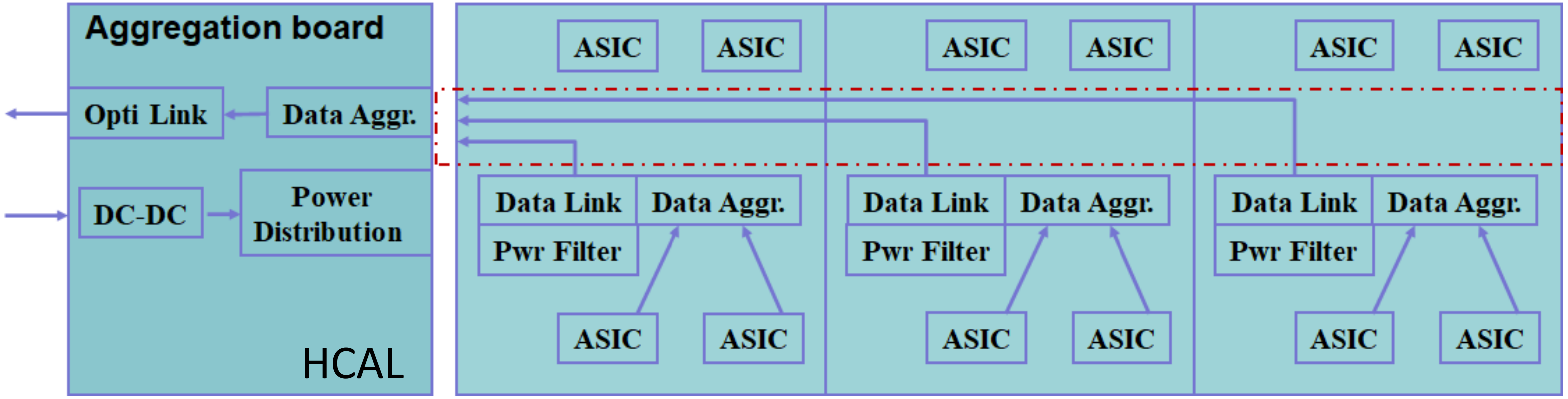


- All sub-det readout electronics were proposed based on this unified framework, maximizing the possibility of common design usage.

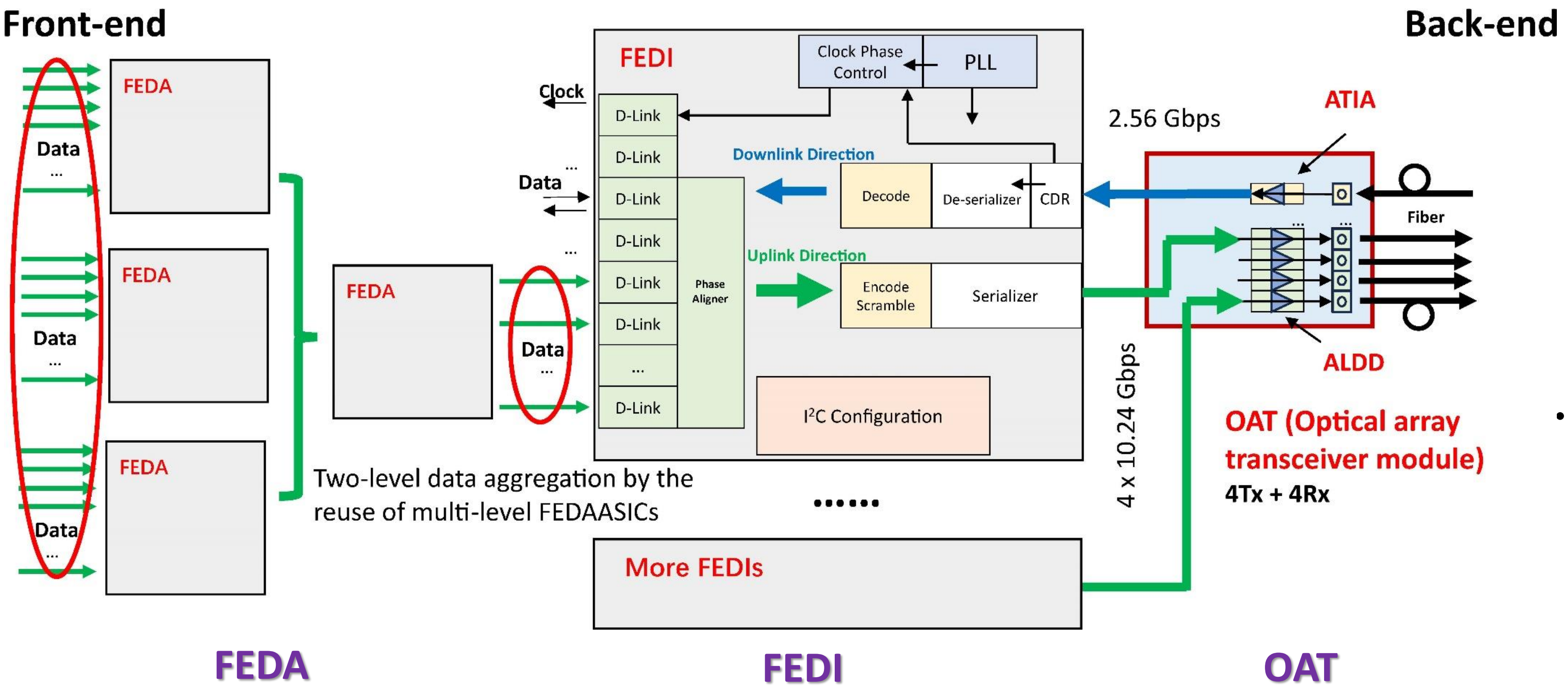








Detailed design on Data Transmission Structure



Two-level data aggregation by the reuse of multi-level FEDAASICs

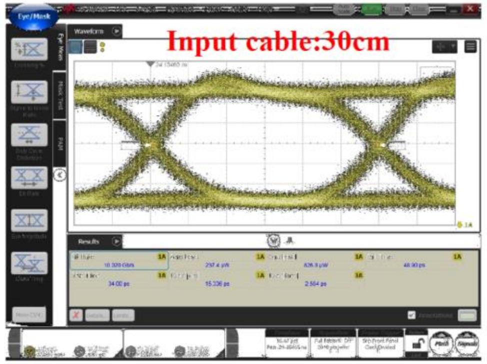
- **Design Team**
  - **IHEP:3 + 3**
  - **CCNU:2+8**
  - **NPU:2+2**
  - **USTC:1+2**
  - **WTU:2+2**
  - **IPAS:1+1**
  - **HPU:1+2**

- Pre-Aggregation ASIC (FEDA): Intend to fit with different front-end detector (different data rates/channels)
- GBTx-like Data Link ASIC (FEDI): Bidirectional serdes ASIC including ser/des, PLL, CDR, code/decode …
- Array Laser Driver ASIC (ALDD) + TIA ASIC (ATIA) + Customized Optical module (OAT)

R&D efforts and results on Data Link

- Self-developed GBT-like prototypes verified:
  - 5.12 GHz PLL + 10.24 Gbps Serializer verified√
  - 2.56 Gbps CDR + 2.56 Gbps Deserializer verified√
  - Phase aligner under test

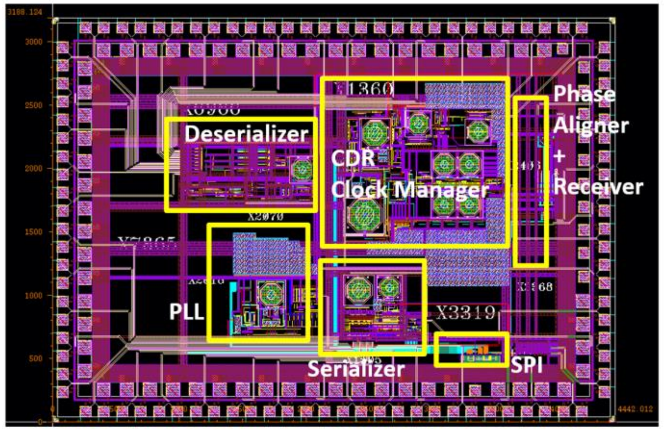
- 10 Gbps Laser Driver Verified √
- Customized optical module prototype Done √
- The rad-tol fiber will be investigated together with the accelerator clocking system



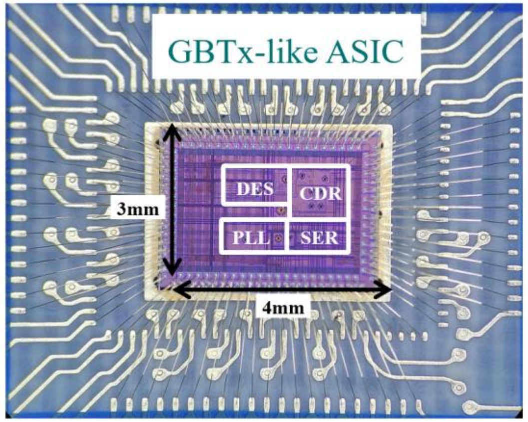
10 Gbps optical eye

Bit Rate	10Gbps	RMSJ	2.6ps
Rise Time	34.0ps	PPJ	15.3ps
Fall Time	48.9ps	Amp	589.4µW

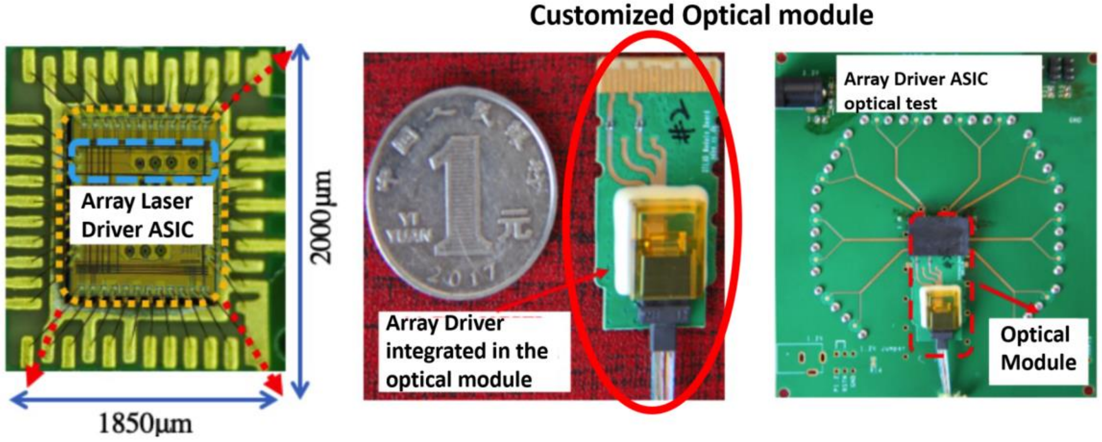
10 Gbps optical eye diagram



GBT-like ASIC prototype layout

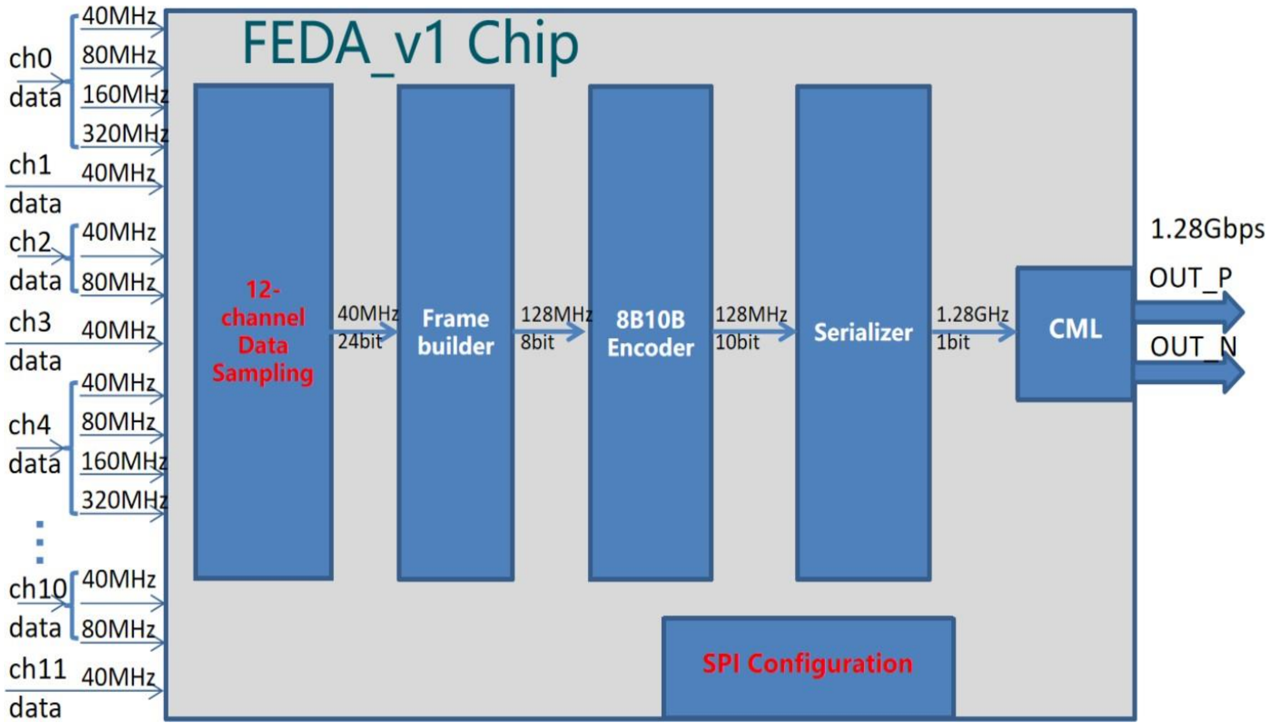


GBT-like ASIC wire-bonding picture

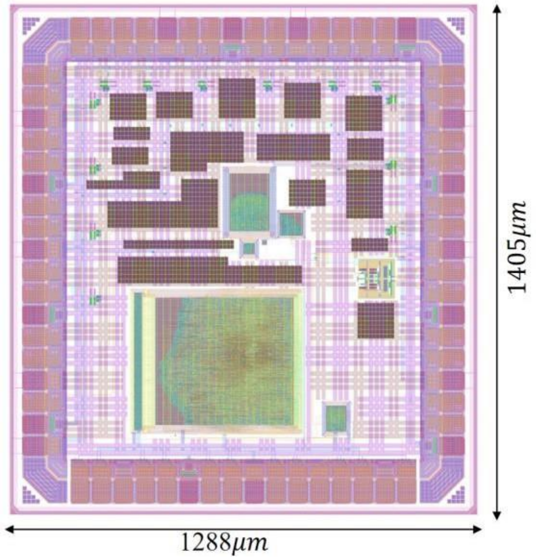


4 x 10 Gbps/ch VCSEL Array Driver with customized optical module

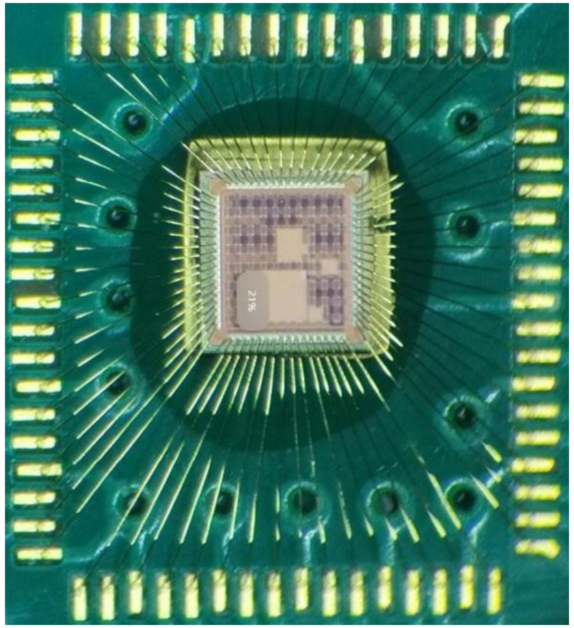
FEDA for data aggregation



FEDA block diagram



FEDA die layout

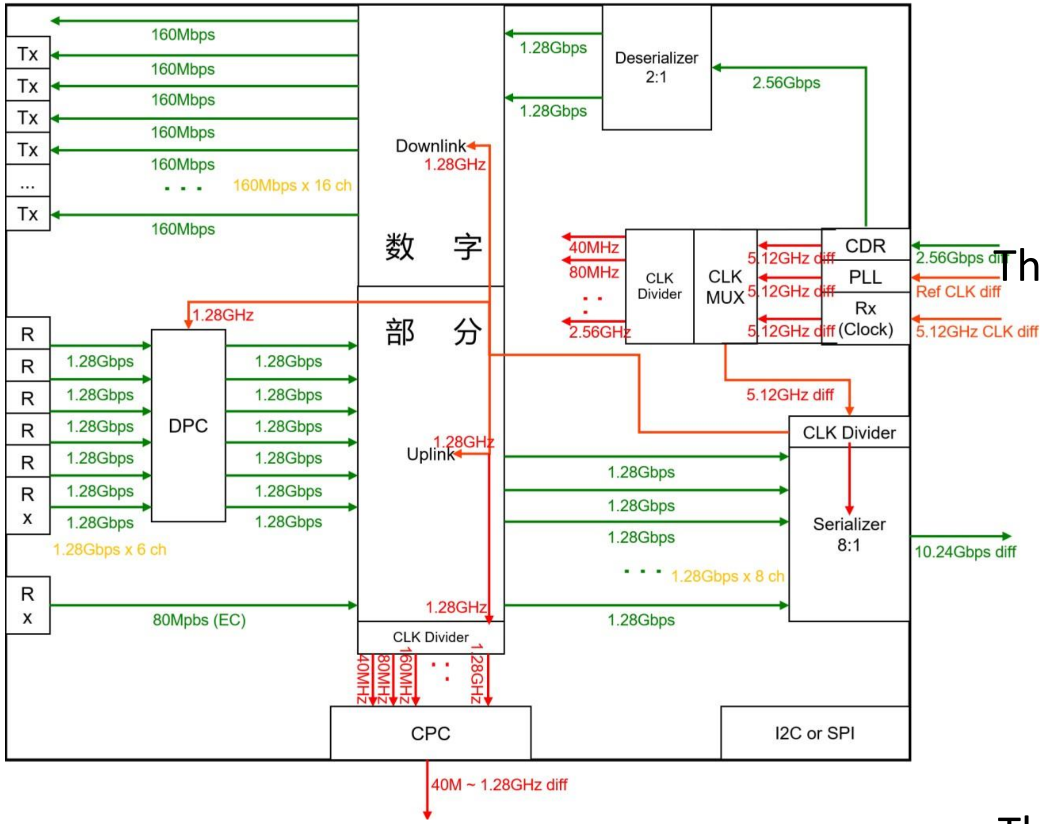


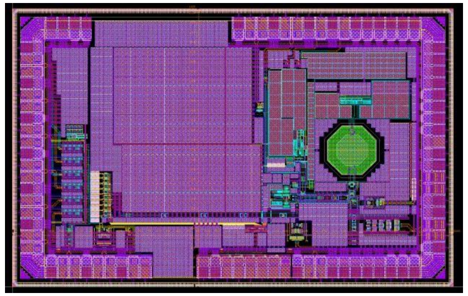
FEDA wire-bonded on PCB

- Post-layout simulation has verified the functionality,
- The chip was taped out in Oct. 2025,
- Testing is on-going.

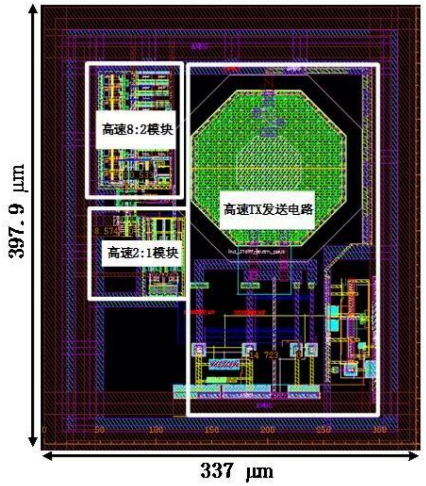
FEDI for data interface

- The chip is in final integration & full chip verification phase
- To be tapeout in July 2026

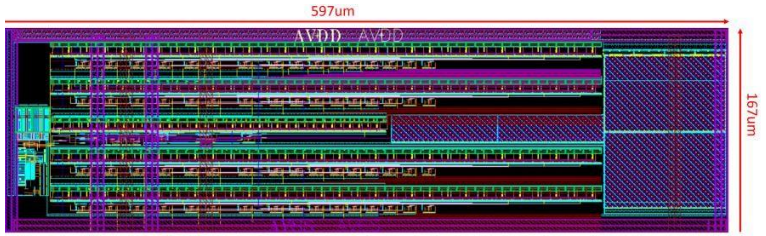




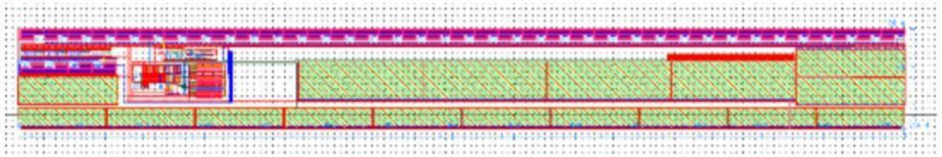
The high-speed clock module（95%）



The serializer、de-serializer module（90%）



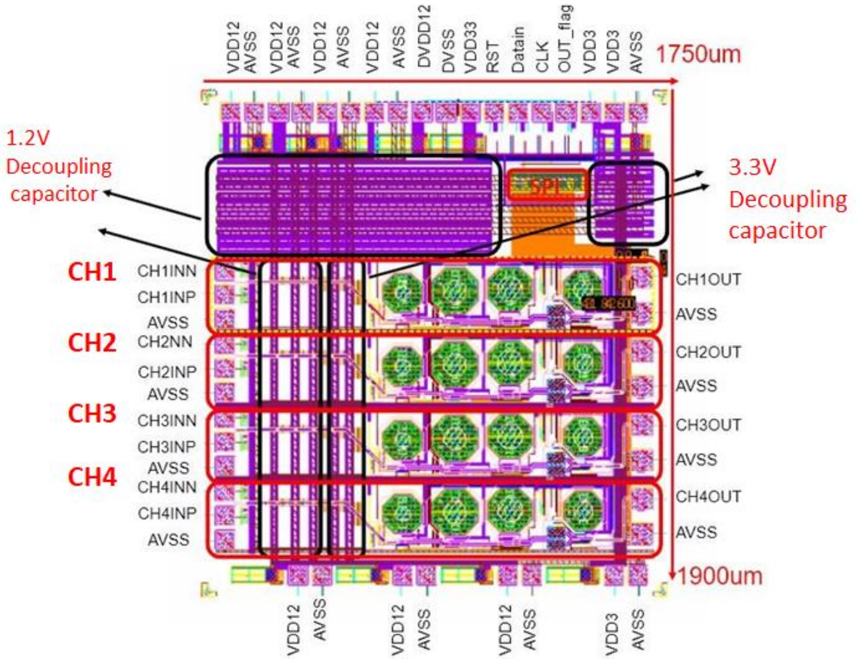
The data phase control module（90%）



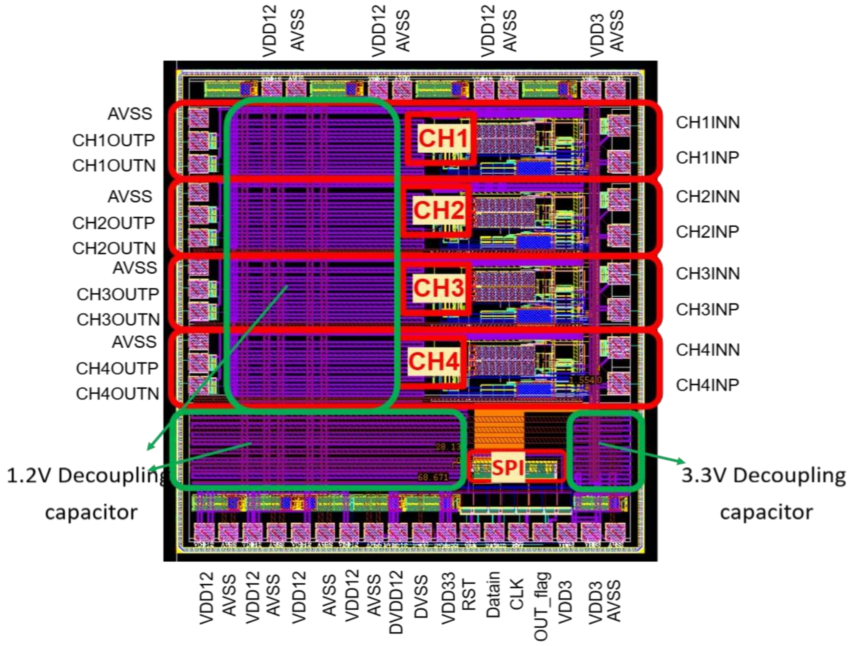
Layout Area：716x80u

The clock phase control module（90%）

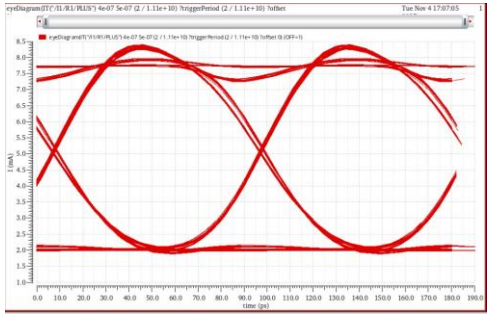
ALDD & ATIA for OAT, the opto- module



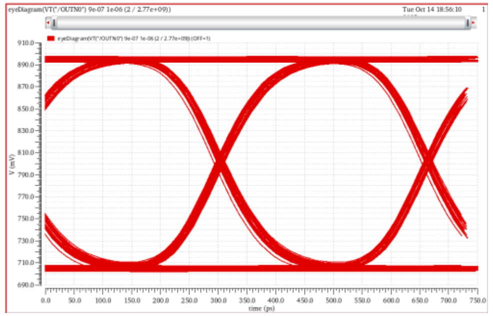
ALDD 4 x 11.09 Gbps/ch



ATIA 4 x 2.77 Gbps/ch



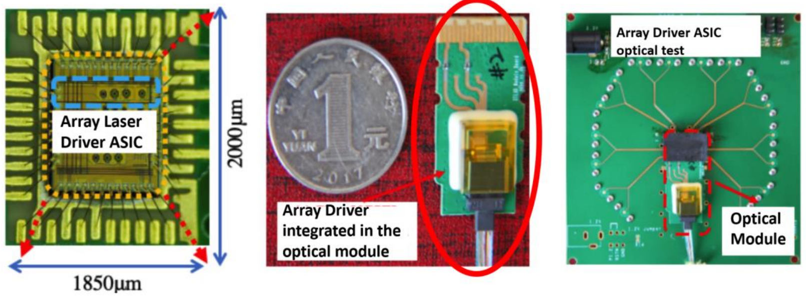
ALDD simulated eye diagram, post-layout, single channel



ATIA simulated eye diagram, post-layout, single channel

- ALDD & ATIA taped out in Oct. 2025.
- Test is on-going.

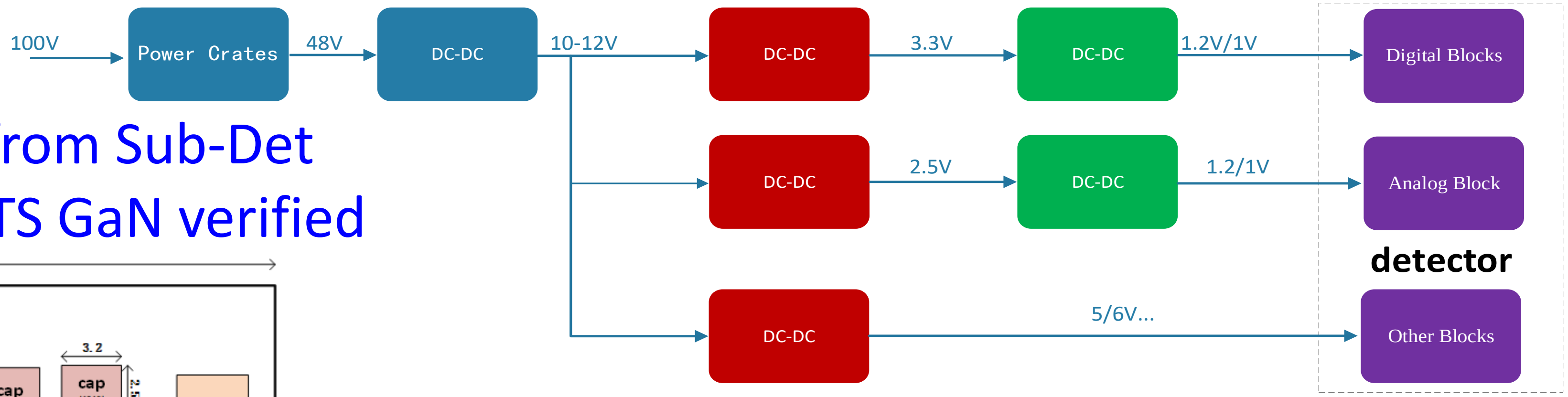
Customized Optical module



4 x 10 Gbps/ch VCSEL Array Driver with customized optical module

R&D efforts preliminary design on powering

- Structure of the power distribution system



100V
Power Crates
48V
DC-DC
10-12V
DC-DC
3.3V
DC-DC
1.2V/1V
Digital Blocks
DC-DC
2.5V
DC-DC
1.2/1V
Analog Block
detector
DC-DC
5/6V…
Other Blocks

- Design spec summarized from Sub-Det
- Preliminary rad-tol. of COTS GaN verified

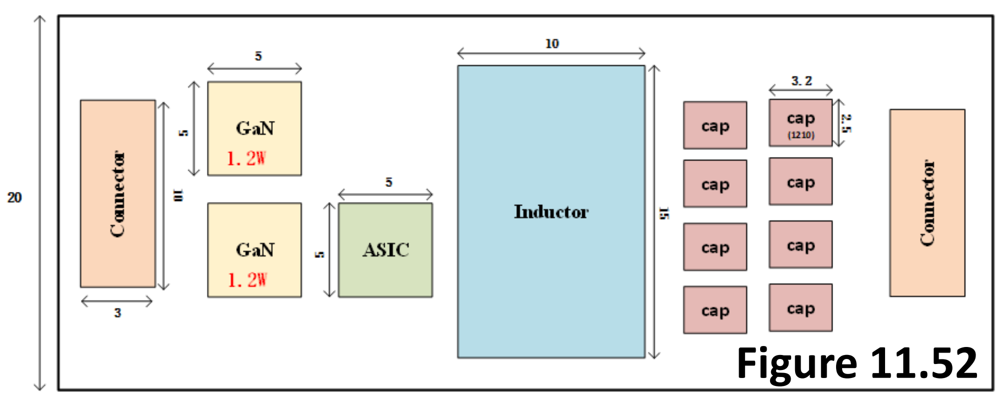
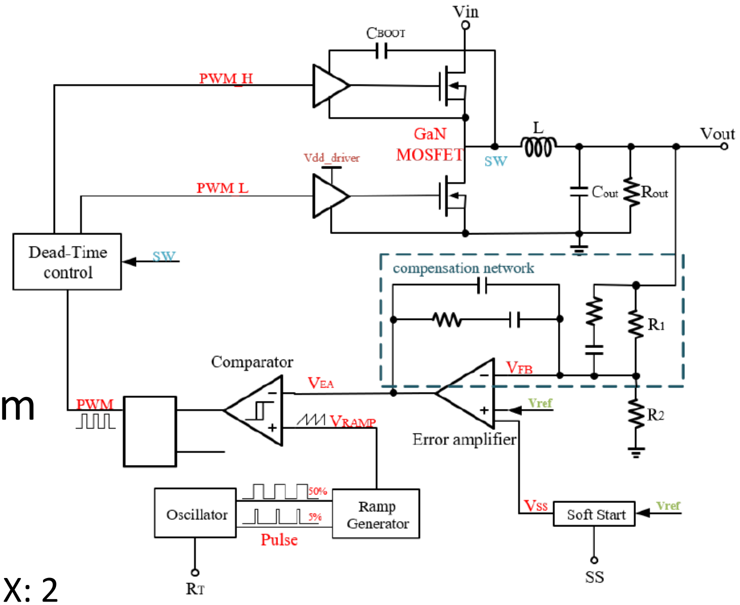


Figure 11.52

	Nominal	Range
Input V	48V	36V-48V
Output V	1.2V	1.2V、3.3V
Output Current	10A	
Output ripple	10mVpp	
Efficiency	85%	80%-85%-80%（light-nom -heavy）
Dimension	50mmX20mmX6.7mm	Including cooling & shielding
TID	5 Mrad（Si）	
Magnet	3T	

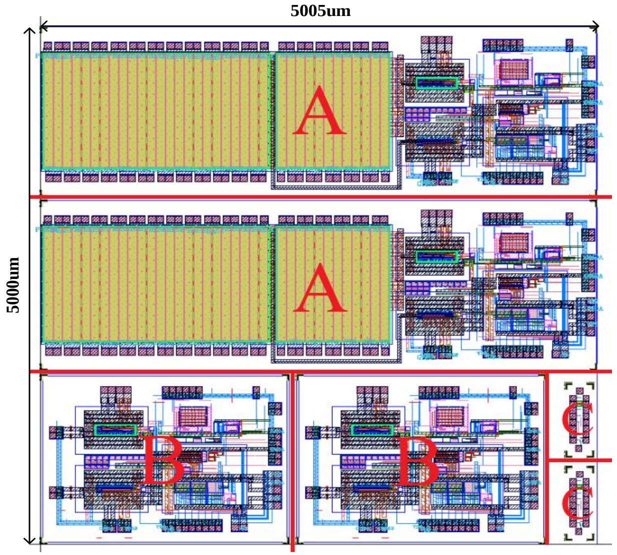
- Proposed design of BUCK DC-DC convertor

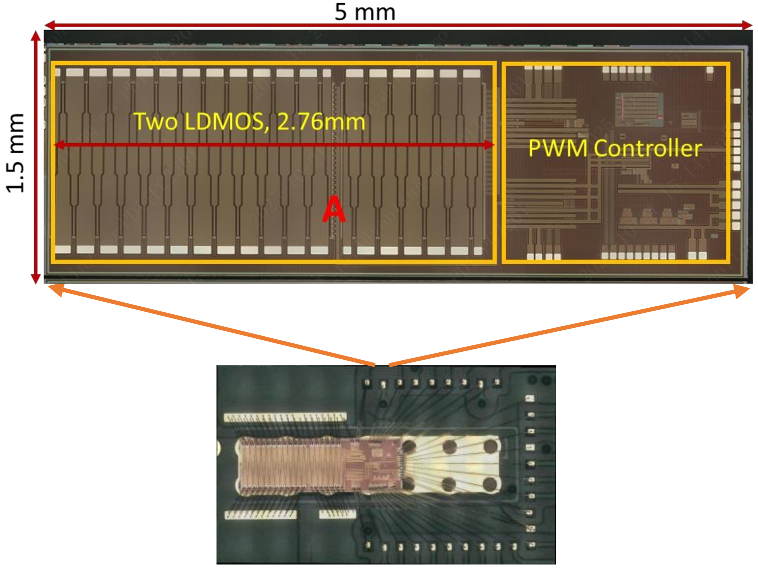
PAL Series



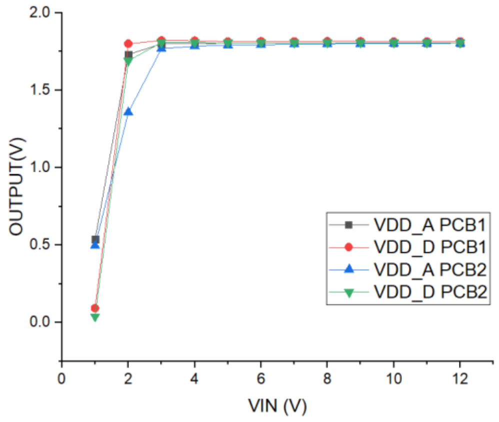
- Design team
  - IHEP: 3
  - NPU: 1+2
  - USTC: 1+1
  - TECHORILUX: 2

PAL – DC-DC controller design

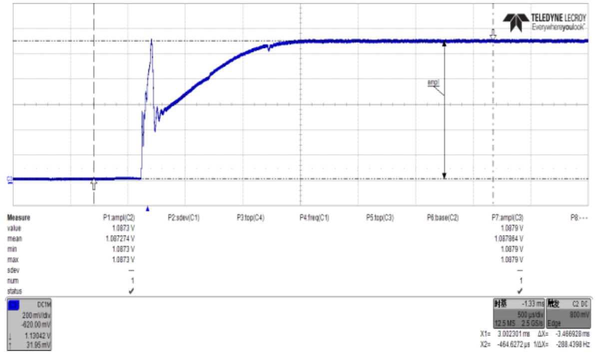




1st Tapeout in 2025



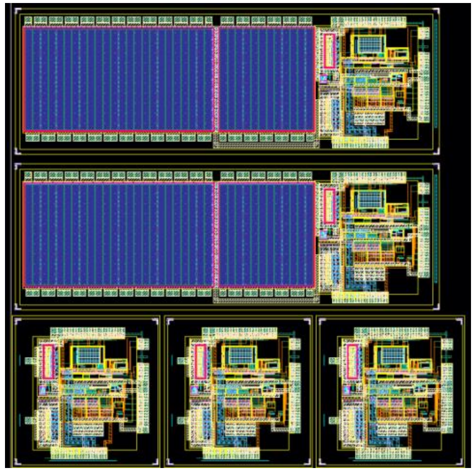
Supply analogue/digital power for controller (1.8V)



Measure	P1:ampl(C2)	P2:sdev(C1)	P3:top(C4)	P4:freq(C1)	P5:top(C3)	P6:base(C2)	P7:ampl(C3)	P8:---
value	1.0873 V						1.0879 V	
mean	1.087274 V						1.087864 V	
min	1.0873 V						1.0879 V	
max	1.0873 V						1.0879 V	
sdev	---						---	
num	1						1	
status	✓						✓	

X1= 3.002301 ms ΔX= -3.466928 ms
X2= -464.6272 µs 1/ΔX= -288.4398 Hz

Transient Output



Revision tapeout in 2026

- Test with external Si/GaN power transistors continued
- Test done with the 1st tapeout, bugs detected and understood
- A revision tapeout submitted in Jan. 2026 to correct the issues

Research team

- A wide collaboration was built involving most of the affiliations in the HEP field in China (~50 people involved in different areas).
- We are working to expand the collaboration, including attracting international colleagues. We are also trying to join in the DRD7.

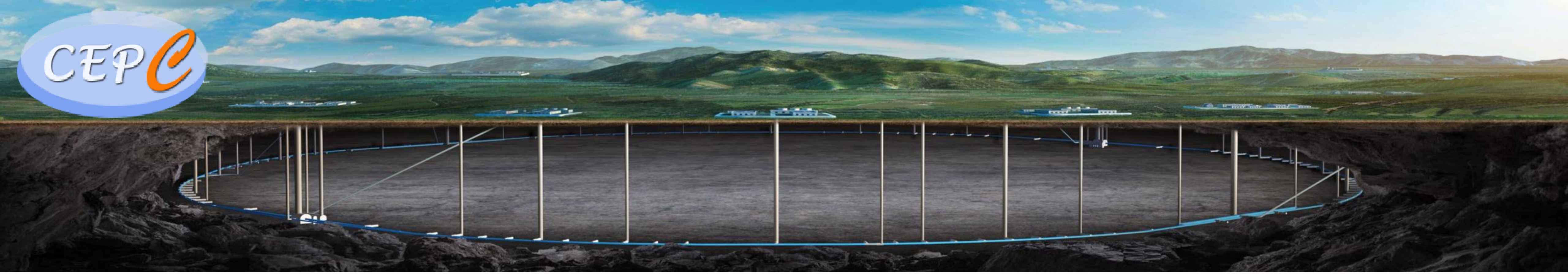
- Overall electronics and BEE: IHEP(5)
- Sub-detector readout electronics: IHEP(11), Tsinghua(5), CCNU(3), NPU(7), SDU(4), NJU(3)
- Data link: CCNU(3), IHEP(3), USTC(2), NPU(4)
- Powering: NPU(3), IHEP(2), USTC(2)

ASIC development & teams

Name	Application	Functional	Foundry & technology	Similar chips	Leading person	Development team	Staff	Students
New VTX chip	VTX	VTX-Stitching	Towerjazz 180nm / 65nm / HL90	MOSAIX	Yunpeng Lu (IHEP)	NPU, CCNU, SDU, NJU	10	8
TEPIX	TPC	Pixel TPC	TSMC 180nm (SMIC 55nm)	Timepix3/4	Zhi Deng (THU)	IHEP	1	4
COFFEE	ITK	HVCMOS	SMIC 55nm HV / new foundry	MightyPix	Yiming Li (IHEP)	ZJU, NPU, DMU，SDU, NJU	8	12
LATRIC	OTK	LGAD-TOF	SMIC 55nm	ALTIROC	Xiongbo Yan (IHEP)	CCNU, WTU, HPU	9	10
SIPAC	SiPM ASIC	ECAL, HCAL, Muon	SMIC 55nm	HGCROC、SPIROC	Huaishen Li (IHEP)	CCNU, NPU	5	6
FEDI	Common Elec	Data Link	SMIC 55nm	lpGBT	Di Guo (CCNU)	IHEP, NPU, USTC, WTU, HPU	9	16
OAT	Common Elec	Optical	SMIC 55nm	VTRx+	Di Guo (CCNU)	IPAS, IHEP	3	3
FEDA	Common Elec	Data Aggregation	SMIC 55nm	lpGBT	Di Guo (CCNU)	IHEP, NPU	2	4
PAL	Common Elec	DC-DC	SMIC 180nm HV	bPolx	Jia Wang (NPU)	IHEP, USTC, TECHORILUX	7	3

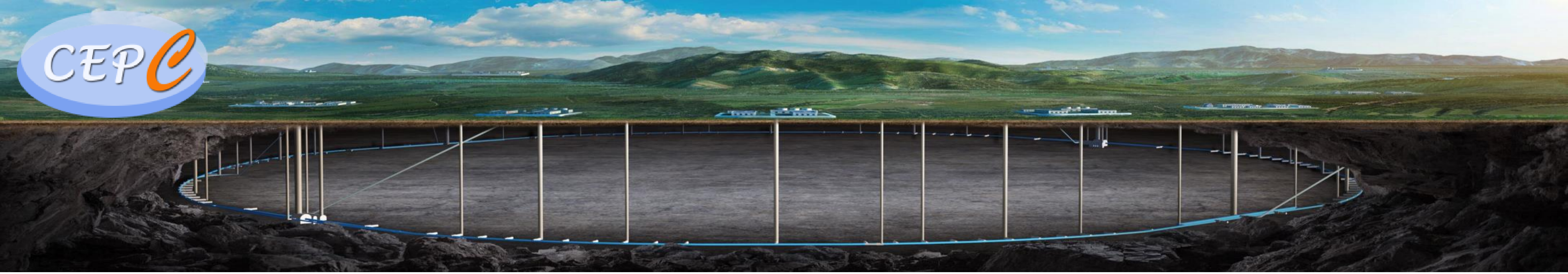
Summary

- CEPC Reference TDR released and key R&D will continue to be prepared for the next 5-year plan
- Full Data Transmission (Frontend Triggerless) + Backend Trigger was chosen to be baseline for the 1st operational phase
  - Background rate under ctrl for Higgs & Low LumiZ
  - Backup scheme on Partial full data transmission + Partial fast trigger (VTX only if necessary)
- All ASIC design with dedicated people power, 1st / 2nd ver. of most ASIC taped out, still aiming at:
  - 3-year to prototype the ASIC
  - 5-year to be finalization
- Other key R&D to be kept on pace
  - Serial powering for future silicon detector
  - Wireless comm as an alternative scheme, while parallel people power allocated other than the main R&D



Thank you for your attention!

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences



BACKUP

中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Consideration on global framework of Elec-TDAQ

- Two main stream frameworks for the electronics-TDAQ can be simply categorized as full data transmission (FEE-Triggerless readout) & readout with conventional trigger
- Comparison on main aspects

	Full data transmission	Conventional Trigger	Superiority
Where to acquire trigger info	On BEE	On FEE	Full data transmission
Trigger latency tolerance	Medium-to-long	Short	
Compatibility on Trigger Strategy	Hardware / software	Hardware only	
FEE-ASIC complexity on Trigger	Simple	Complex on algorithm	
Upgrade possibility on new trigger	High	Limited	
FEE data throughput	Large	Small	Conventional Trigger
Maturity	Mature but relatively new	Very mature	
Resources needed for calculation	High	Low	
Representative experiments	CMS, LHCb, …	ATLAS, BELLE2, BESIII, …	

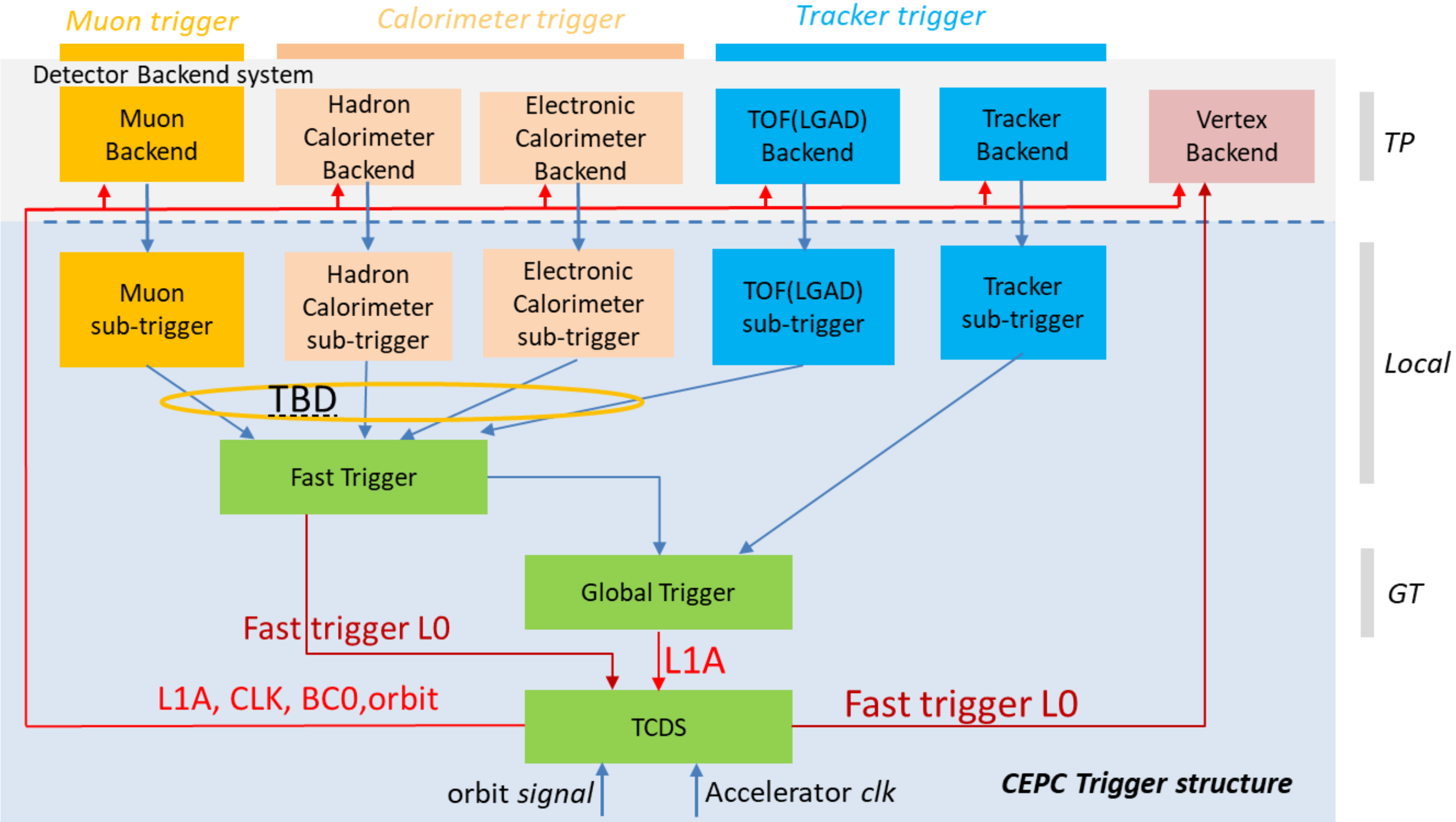
Our choice on global framework

- We choose **Full Data Transmission (Frontend Triggerless) + Backend Trigger** as our baseline global framework, while keep conventional trigger (to be explained) readout as the backup :

1. Maintain the maximum possibility for new physics and future upgrades.
   - Readout all the information w/o pre-assumed trigger conditions.
2. Speed-up the FEE-ASIC iteration & finalization process
   - W/o the need to consider the undefined trigger algorithm, esp. regarding the potential tight schedule.
3. Enable a common platform design for all Sub-Detectors
   - Common BEE Brd, common Trg Brd, common data interface…
   - Scalable based on the detector volume
4. Sufficient headroom for FEE data transmission based on the current MDI background rate
   - 11Gbps per link on FEE (max by ×4 links)

Backup scheme of the framework

- The proposed framework was based on the estimated background rate of all sub-det.
- Background rate indicated the data link capability can manage the Phase I operation of Higgs & Low LumiZ in the first ten years
  - Shielding optimization ongoing to suppress the background
  - High LumiZ situation is still not fully understood, but in the 2nd ten years
    - Replaceable detectors e.g. VTX, ITK.. can be upgraded with new chips with intel-compression and advanced trigger in case
    - Unreplaceable detectors e.g. ECAL, HCAL can be upgraded with more fiber channels



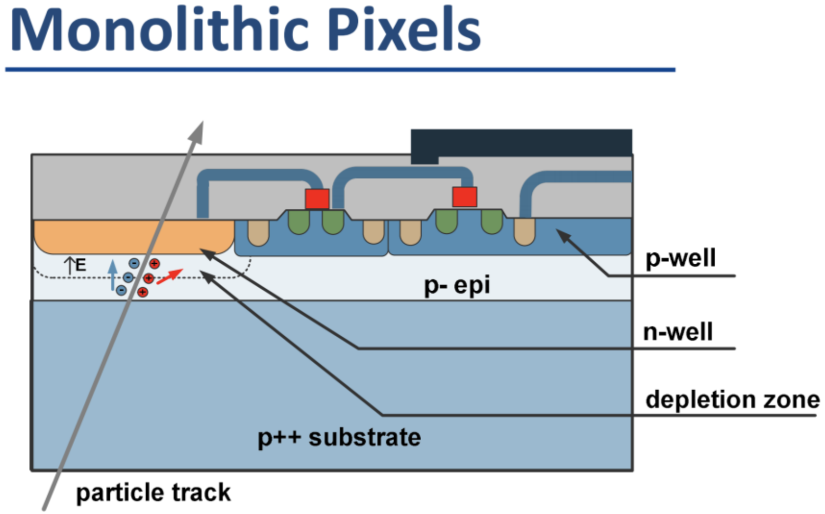
CEPC Trigger structure

The conventional trigger scheme can serve as a backup plan, with sufficient on-detector data buffering and reasonable trigger latency, the overall data transmission rate can be controlled.

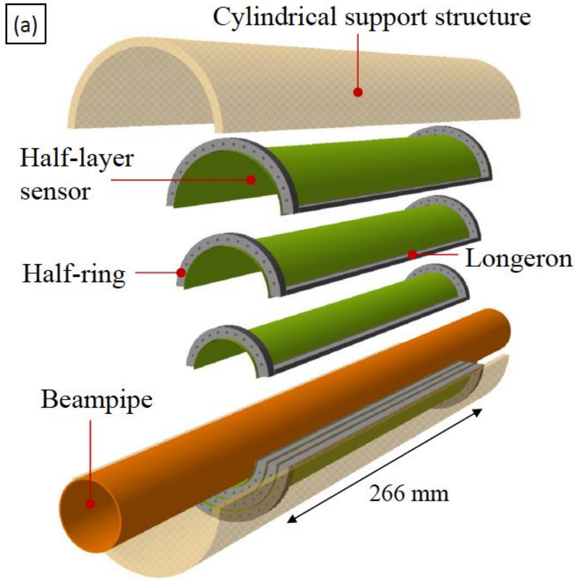
Vertex Detector

- Vertex detector Technology selection
  - Baseline: based on curved CMOS MAPS (Inspired by ALICE ITS3 design[1])
    - Advantage: 2~3 times smaller material budget compared to alternative (ladder)
  - Alternative: Ladder design based on CMOS MAPS

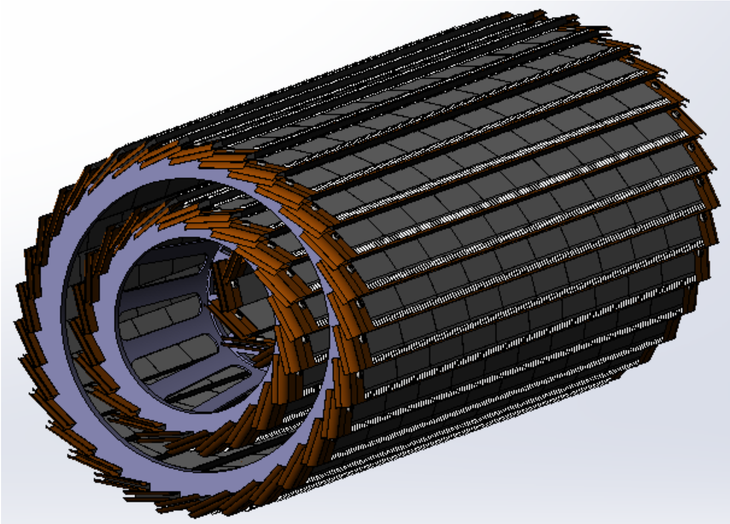
Monolithic active Pixel CMOS (MAPS)



Baseline: curved MAPS



Alternative: ladder based MAPS



[1] ALICE ITS3 TDR: https://cds.cern.ch/record/2890181

ITK Barrel Design with HV-CMOS Pixels

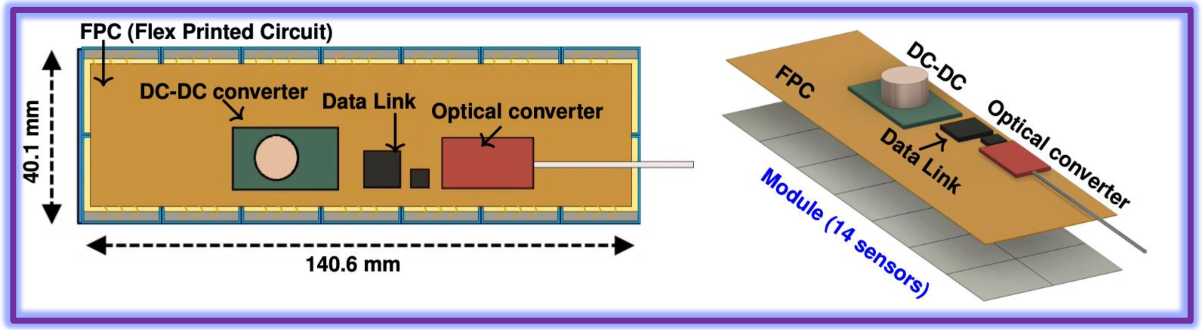
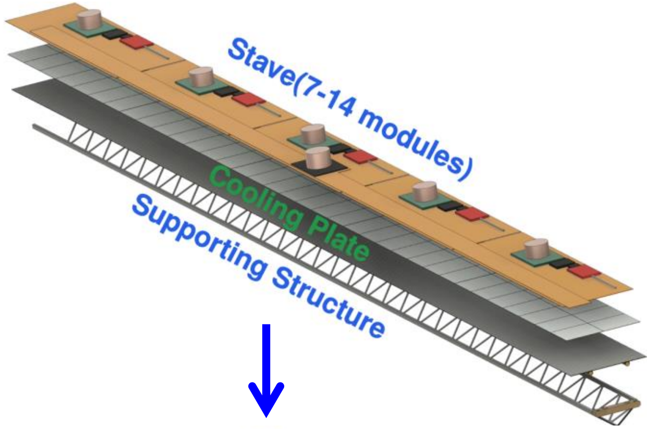
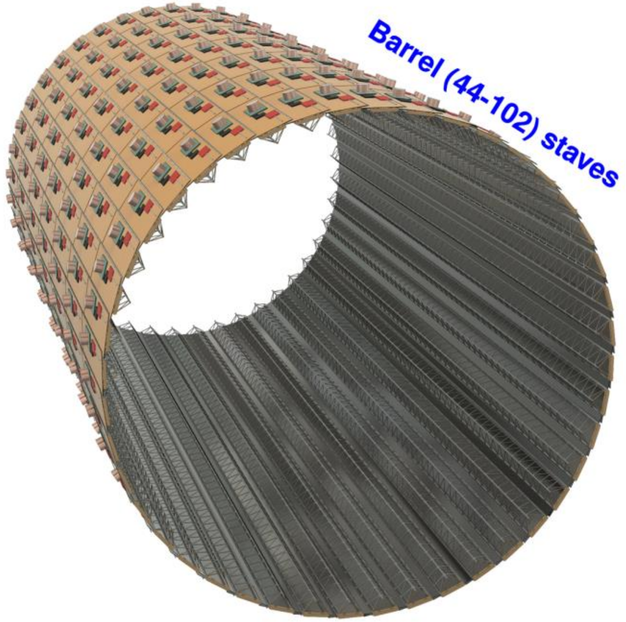


Figure 5.37

5.3.2.1 ITK barrel design





- HV-CMOS pixel sensor:
  - Sensor size: 20 mm × 20 mm
  - Pixel size: 34 μm × 150 μm (spatial resolution: 8 μm × 40 μm)
- Module:
  - 14 sensors (2 rows × 7 columns)
  - Module dimensions: 140.6 mm × 40.1 mm
- Stave length: 986.6 mm (ITKB1), 1,409.6 mm (ITKB2), and 1973.2 mm (ITKB3)
- Barrel radii: 235 mm (ITKB1), 345 mm (ITKB2), and 555.6 mm (ITKB3)

The designed 3 ITK barrel layers has a total surface area of 13.3 m², including 33,264 sensor chips, with a power consumption of ~26.6 kW.

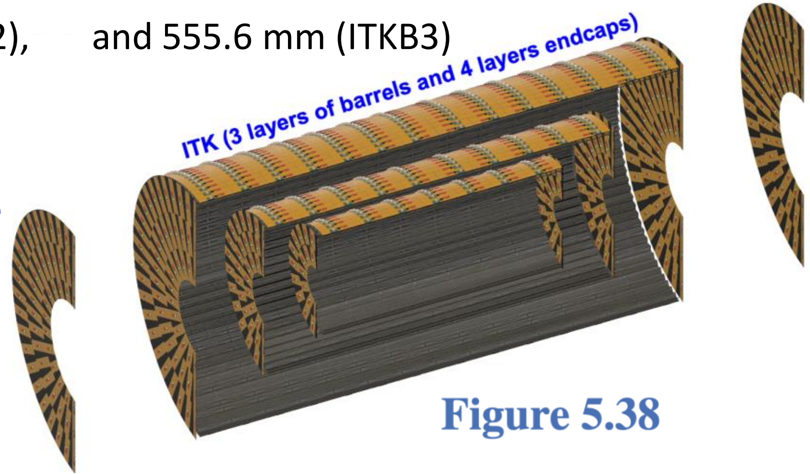
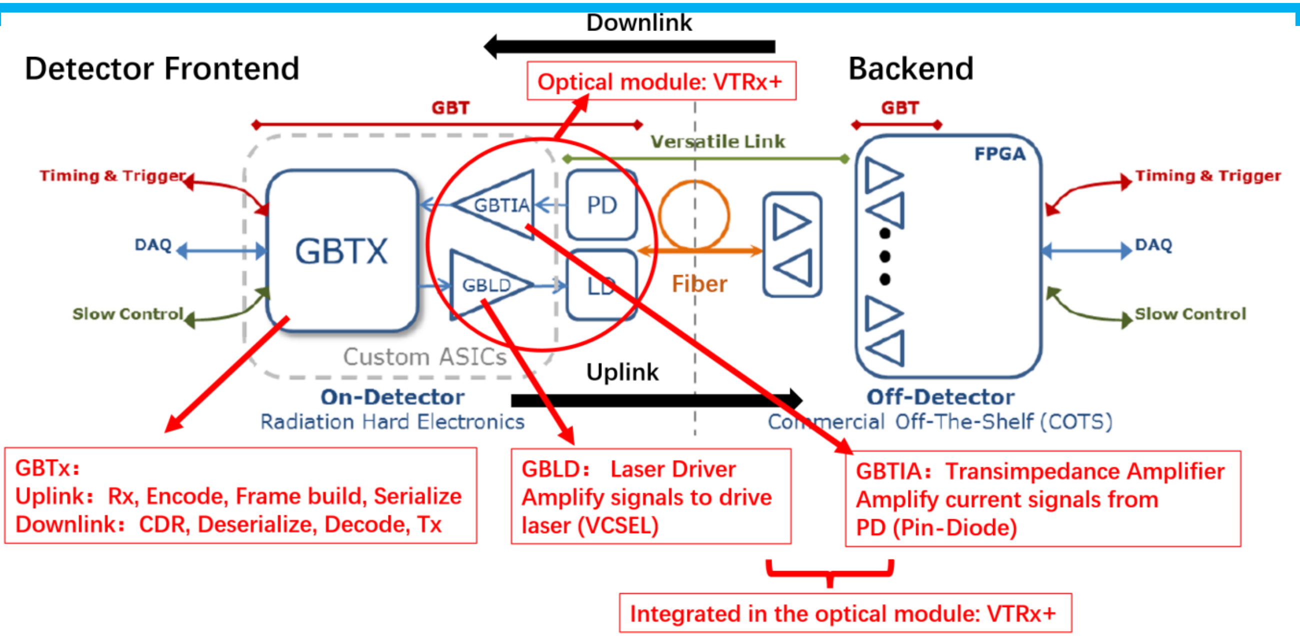


Figure 5.38

Technical Survey on Data Transmission System

- **GBT Project:**
  - The lpGBT & VTRx chip series, developed by CERN, are widely used by LHC experiments, as a common project
  - Core components:
    - GBTx: Bidirectional Serdes ASIC
    - GBLD: Laser driver
    - GBTIA: Transimpedance amplifier
    - Customized Optical Module
  - However the base clock frequency of CEPC 43.3MHz is not compatible with lpGBT system
- **Our choice:**
  - Build a GBT-like universal bidirectional data transmission system
  - Take the lpGBT as a reference, the protocol can be a minimum & necessary set for the readout, clocking & control



Optical module: VTRx+

GBTx：
Uplink：Rx, Encode, Frame build, Serialize
Downlink：CDR, Deserialize, Decode, Tx

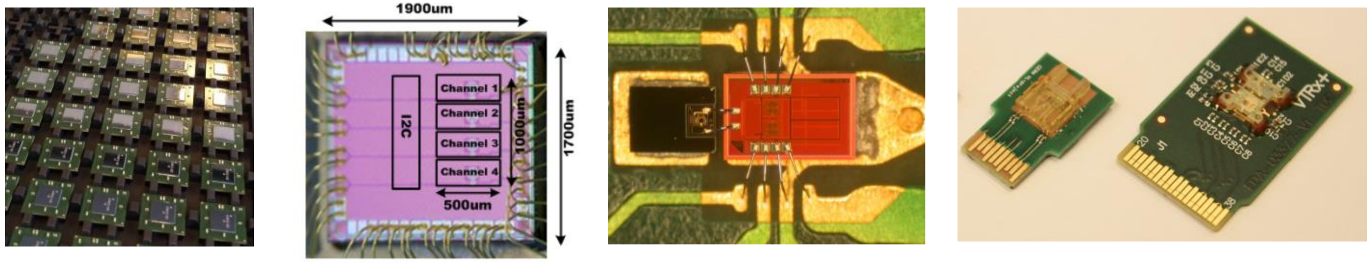
GBLD：Laser Driver
Amplify signals to drive laser (VCSEL)

GBTIA：Transimpedance Amplifier
Amplify current signals from PD (Pin-Diode)

Integrated in the optical module: VTRx+

GBT Architecture Developed by CERN

Ref. P. Moreira, The GBT Project, 2007



lpGBTx
Uplink: 10.24Gbps
Downlink: 2.56 Gbps

GBLD (LDQ10)
10.24 Gbps x 4ch

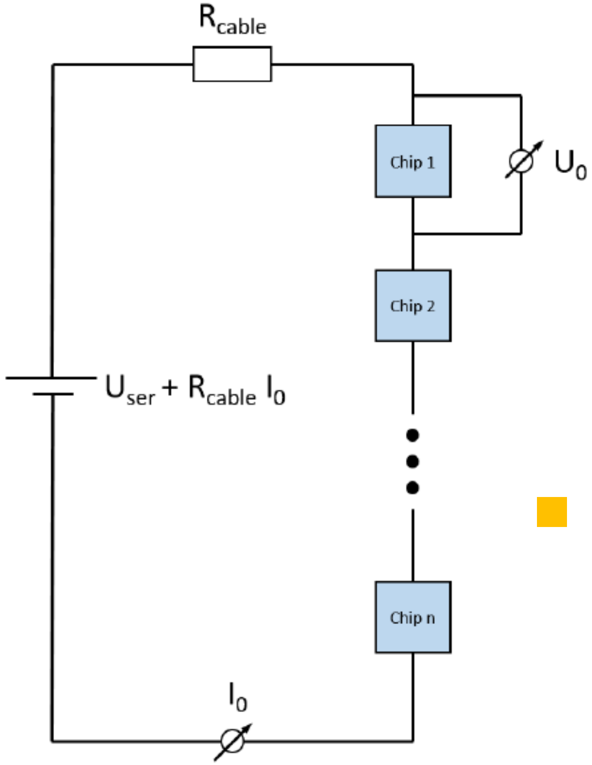
GBTIA
2.56 Gbps

VTRx+
4Tx + 1Rx
Array Optical Module

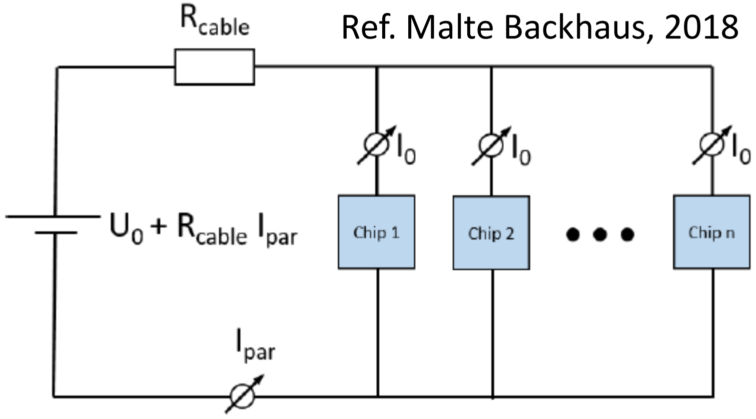
GBT Series ASICs and optical module

Ref. P. Moreira, GBT Chipset Status and Production Plans, 2013

Technology survey and our choice on Powering



Serial Powering



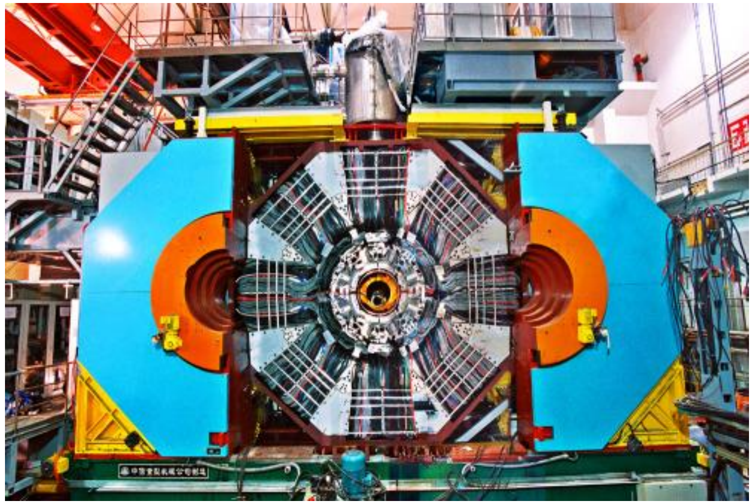
Ref. Malte Backhaus, 2018

Parallel Powering

	Serial Power	Parallel Power
Material	Much less	
Cabling	Much less	
Installation	Much easier	
Maturity	New	Very mature
System Reliability	Potential issue	Very robust

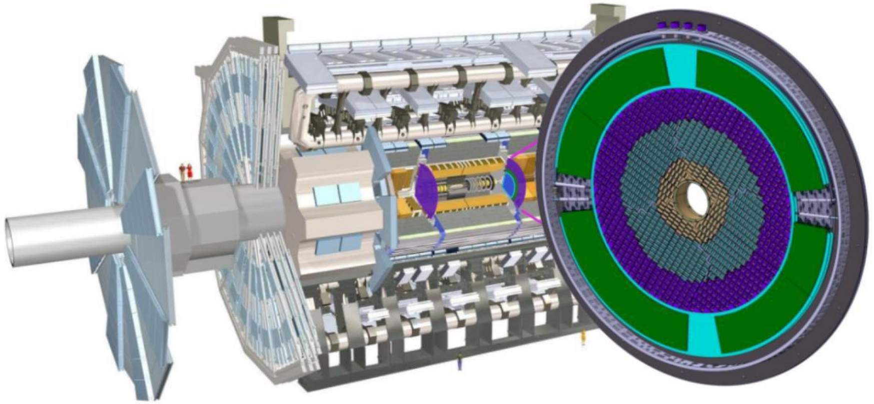
- On powering distribution
  - Serial Powering is superior in many aspects (material, cabling and installation…) than Parallel Powering, especially on VTX & TRK
  - It is also a hot area with a lot of focused R&D
  - However, due to the common substrate at negative voltage for the stitching sensor in VTX, serial powering is not feasible
- Our choice
  - As a general platform, we chose (conventional) Parallel Powering as the baseline scheme, while to keep pace on R&D of Serial Powering as the backup scheme

Previous experience on electronic systems



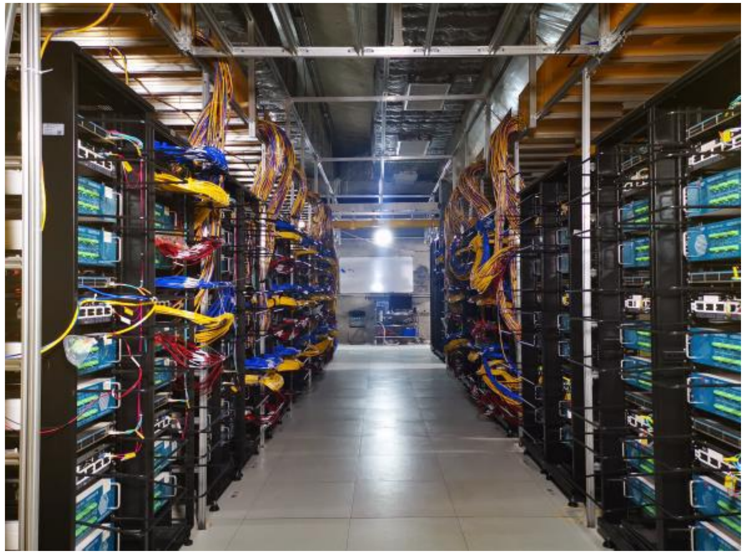
BESIII

JUNO experiment

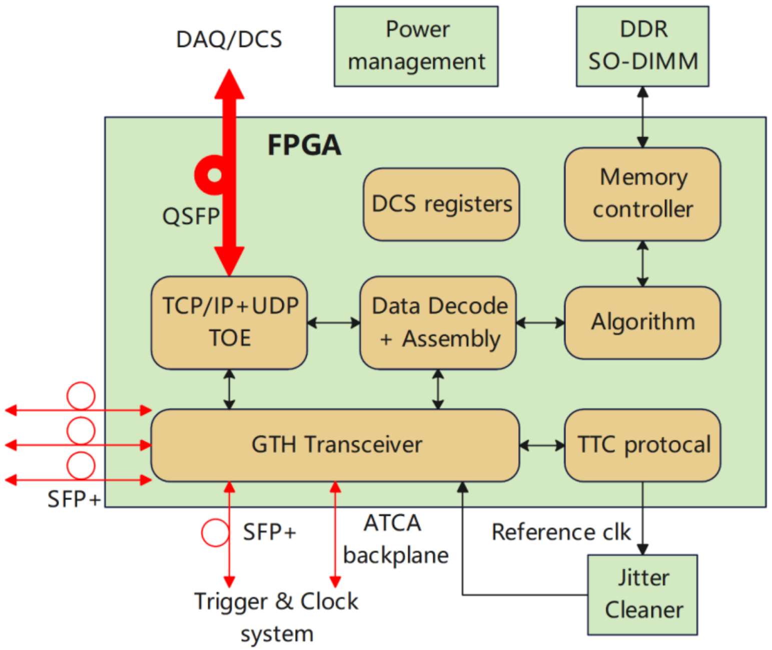


ATLAS HGTD
(Ref. J. Zhang http://b.mtw.so/6ide9O)

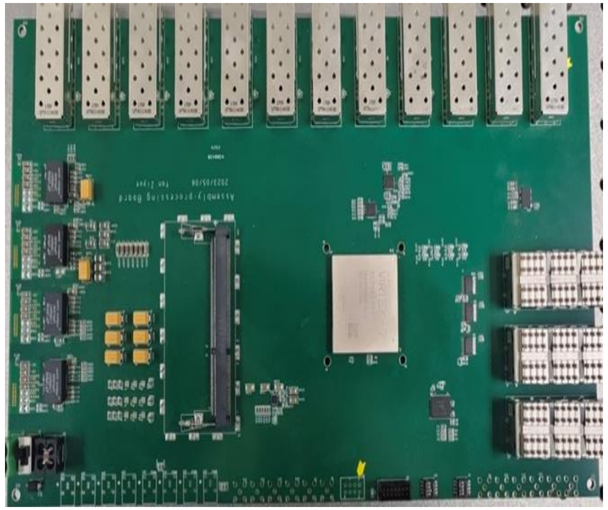
- Our team has developed the electronics systems for most of the major particle physics experiments in China, including BESIII, Dayabay, JUNO, LHAASO…
- Also in international collaborations as ATLAS HGTD…
- We have extensive experience in electronics system design from the FEE to BEE



Detailed design on common BEE



The back-end Card structure



Data aggregation and processing board Prototype for Vertex detector

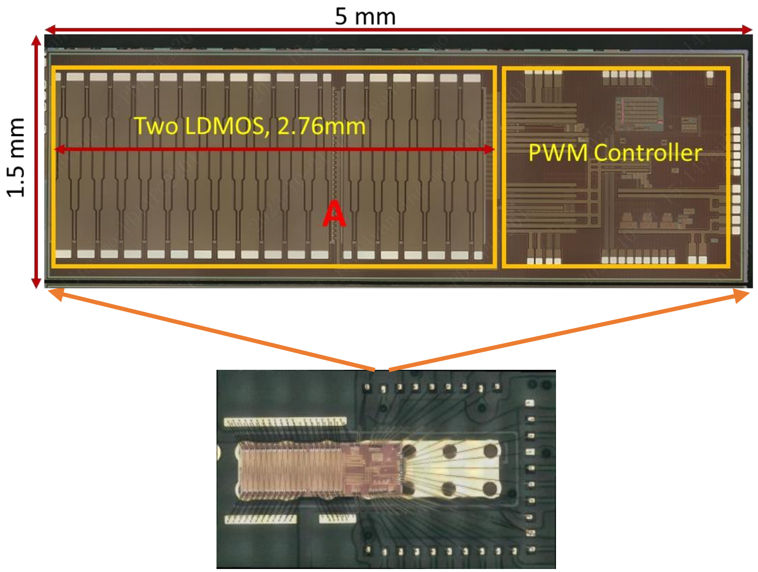
	KC705 (XC7K325T-2FFG900C)	KCU105 (XCKU040-2FFVA1156E)	VC709 (XC7VX690T-2FFG1761C)	VCU108 (XCVU095-2FFVA2104E)	XCKU115
Logic Cells(k)	326	530	693	1,176	1451
DSP Slices	840	1920	3,600	768	5520
Memory (Kbits)	16,020	21,100	52,920	60,800	75,900
Transceivers	16(12.5Gb/s)	20(16.3Gb/s)	80(13.1Gb/s)	32(16.3Gb/s) and 32(30.5Gb/s)	64(16.3Gb/s)
I/O Pins	500	520	1,000	832	832
Cost	2748 (650)	3882(1500)	8094	7770	

- Routing data between the optical link of front-end and the highspeed network of DAQ system.
- Connect to TTC and obtain synchronized clock, global control, and fanout high performance clock for front-end.
- Real-time data processing, such as trigger algorithm and data assembly.
- On-board large data storage for buffering.
- Preference for Xilinx Kintex UltraScale series due to its cost-effectiveness and availability.

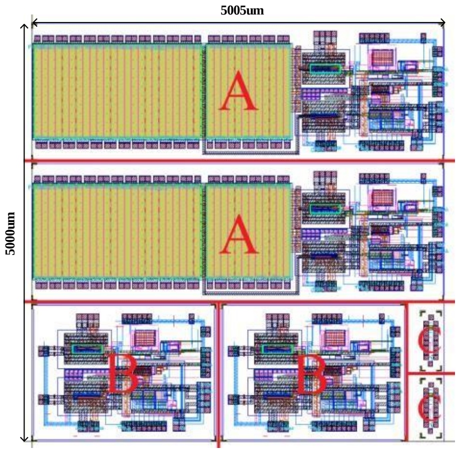
- A cost-driven device selection: FPGA XC7VX690T
- Interface： SFP+ 10Gbps X12 + QSFP 40Gbps X3
- Implement real time FPGA based machine learning for clustering, hit point searching, and tracking algorithms

DC-DC controller

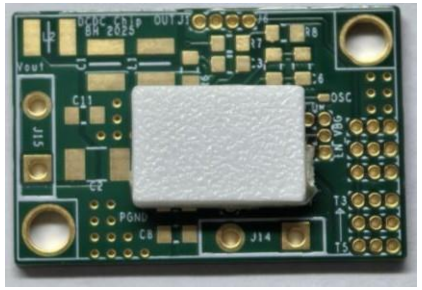
The tape-out in January 2025



Die wire-bonded on a PCB



The layout



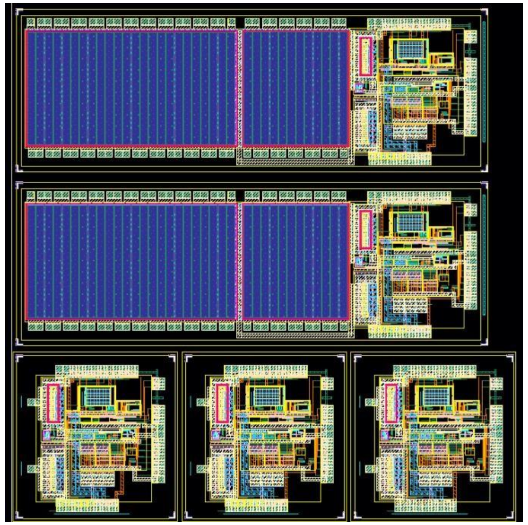
Test PCB

The built-in power transistor does not work stably, problem identified. Tests continued with an external Si power transistor. The PCBs for tests with GaN power transistors are received from the wire-bonding house. Tests are starting.

The tape-out in Junuary 2026

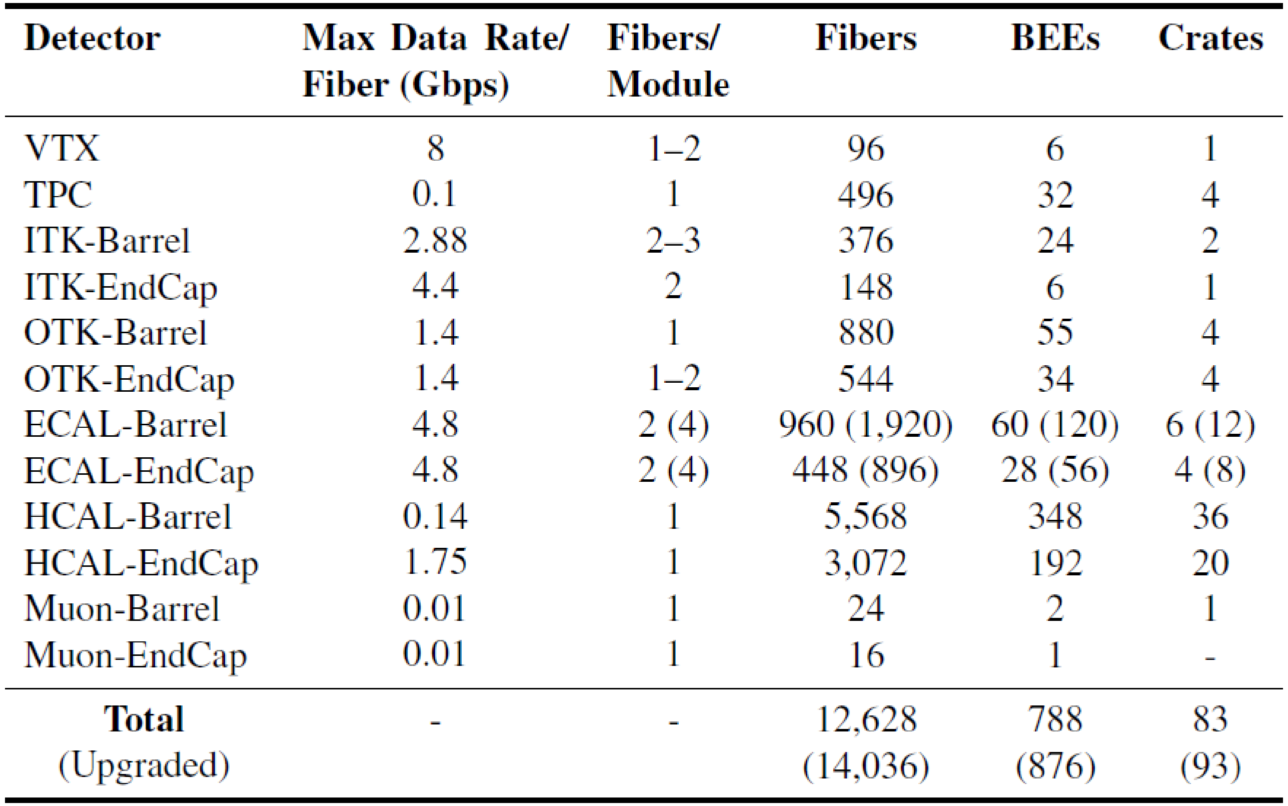
changes：

1. Correct the problem in the built-in power transistor to avoid current leak.
2. ESD protection only to GND
3. Removed the enabling circuit to the band-gap.
4. Improved powering up sequence, and added pre-power-drop circuit.
5. Die size reduces from 2.17*1.48 mm^2 to 1.38*1.42 mm^2
6. Test points for irradiation.



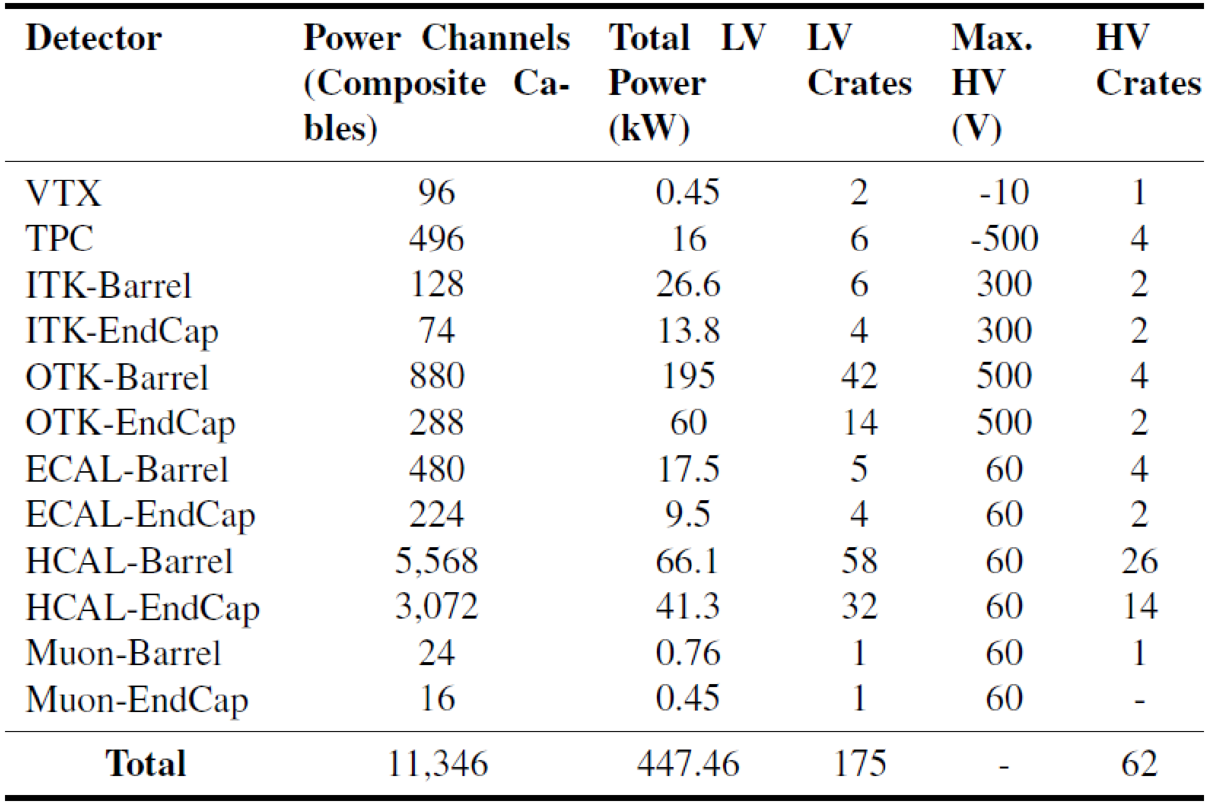
Electronics interface to the counting room

Data Link, Fibers & BEE



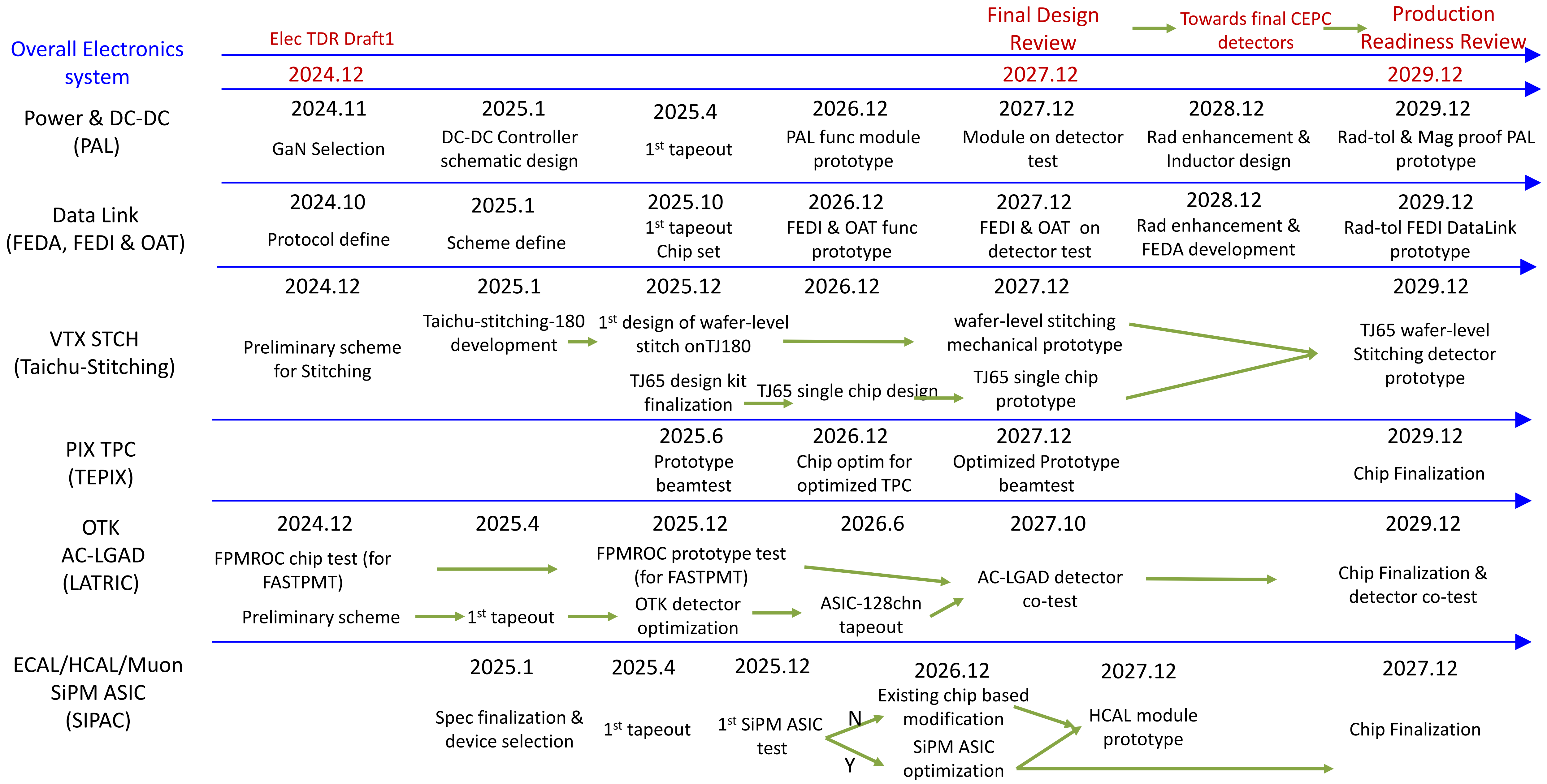
Detector	Max Data Rate/ Fiber (Gbps)	Fibers/ Module	Fibers	BEEs	Crates
VTX	8	1–2	96	6	1
TPC	0.1	1	496	32	4
ITK-Barrel	2.88	2–3	376	24	2
ITK-EndCap	4.4	2	148	6	1
OTK-Barrel	1.4	1	880	55	4
OTK-EndCap	1.4	1–2	544	34	4
ECAL-Barrel	4.8	2 (4)	960 (1,920)	60 (120)	6 (12)
ECAL-EndCap	4.8	2 (4)	448 (896)	28 (56)	4 (8)
HCAL-Barrel	0.14	1	5,568	348	36
HCAL-EndCap	1.75	1	3,072	192	20
Muon-Barrel	0.01	1	24	2	1
Muon-EndCap	0.01	1	16	1	-
Total (Upgraded)	-	-	12,628 (14,036)	788 (876)	83 (93)

On-detector LV, HV & cables



Detector	Power Channels (Composite Cables)	Total LV Power (kW)	LV Crates	Max. HV (V)	HV Crates
VTX	96	0.45	2	-10	1
TPC	496	16	6	-500	4
ITK-Barrel	128	26.6	6	300	2
ITK-EndCap	74	13.8	4	300	2
OTK-Barrel	880	195	42	500	4
OTK-EndCap	288	60	14	500	2
ECAL-Barrel	480	17.5	5	60	4
ECAL-EndCap	224	9.5	4	60	2
HCAL-Barrel	5,568	66.1	58	60	26
HCAL-EndCap	3,072	41.3	32	60	14
Muon-Barrel	24	0.76	1	60	1
Muon-EndCap	16	0.45	1	60	-
Total	11,346	447.46	175	-	62

- Fiber/cable numbers updated(reduced) according to the latest detector design
- The on-detector connection described in each sub-D chapter, while the inter-detector connection newly described in the mechanical chapter
- The patch panel related interface newly described also in the mechanical chapter



Overall Electronics system

- 2024.12 Elec TDR Draft1
- 2027.12 Final Design Review → Towards final CEPC detectors →
- 2029.12 Production Readiness Review

Power & DC-DC (PAL)

- 2024.11 GaN Selection
- 2025.1 DC-DC Controller schematic design
- 2025.4 1st tapeout
- 2026.12 PAL func module prototype
- 2027.12 Module on detector test
- 2028.12 Rad enhancement & Inductor design
- 2029.12 Rad-tol & Mag proof PAL prototype

Data Link (FEDA, FEDI & OAT)

- 2024.10 Protocol define
- 2025.1 Scheme define
- 2025.10 1st tapeout Chip set
- 2026.12 FEDI & OAT func prototype
- 2027.12 FEDI & OAT on detector test
- 2028.12 Rad enhancement & FEDA development
- 2029.12 Rad-tol FEDI DataLink prototype

VTX STCH (Taichu-Stitching)

- 2024.12 Preliminary scheme for Stitching
- 2025.1 Taichu-stitching-180 development →
- 2025.12 1st design of wafer-level stitch onTJ180 → 2027.12 wafer-level stitching mechanical prototype
- TJ65 design kit finalization → TJ65 single chip design → TJ65 single chip prototype
- 2026.12
- 2029.12 TJ65 wafer-level Stitching detector prototype

PIX TPC (TEPIX)

- 2025.6 Prototype beamtest
- 2026.12 Chip optim for optimized TPC
- 2027.12 Optimized Prototype beamtest
- 2029.12 Chip Finalization

OTK AC-LGAD (LATRIC)

- 2024.12 FPMROC chip test (for FASTPMT) → 2025.12 FPMROC prototype test (for FASTPMT) → 2027.10 AC-LGAD detector co-test
- Preliminary scheme → 2025.4 1st tapeout → OTK detector optimization → 2026.6 ASIC-128chn tapeout → AC-LGAD detector co-test
- 2029.12 Chip Finalization & detector co-test

ECAL/HCAL/Muon SiPM ASIC (SIPAC)

- 2025.1 Spec finalization & device selection
- 2025.4 1st tapeout
- 2025.12 1st SiPM ASIC test
- N → 2026.12 Existing chip based modification → 2027.12 HCAL module prototype
- Y → SiPM ASIC optimization → HCAL module prototype; → 2027.12 Chip Finalization

People-power for Electronics system

	Overall	BEE	VTX	TPC	ITK+OTK (LATRIC)	CAL (SiPM)	Muon	Data Link	Power	Wireless
Staff	5	1	10	1	9	5	1	9	7	4
Postdoc + Student	0	3	8	4	10	6	0	16	3	5
Total Sum	5	4	18	5	19	11	1	25	10	9

- The headcounts are not to the FTE
- Some staffs are shared by multiple projects, while postdocs / students are dedicated to the projects

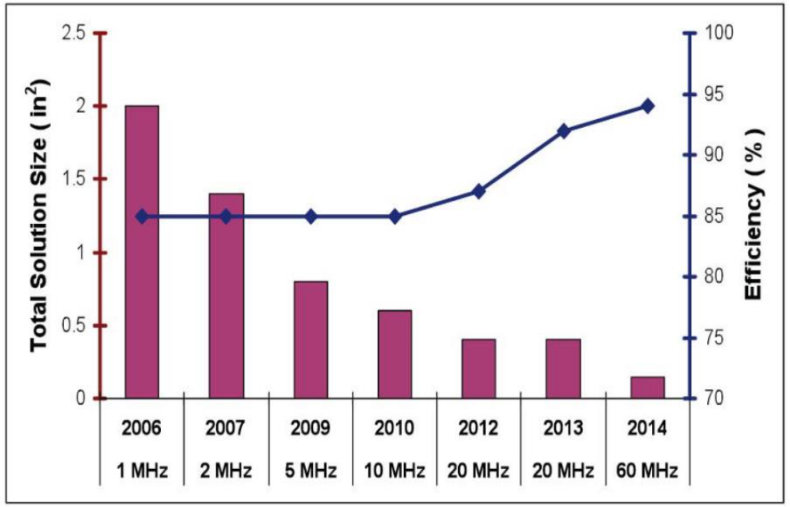
Affiliations for Electronics system

	Overall	BEE	VTX	TPC	ITK+OTK (LATRIC)	CAL (SiPM)	Muon	Data Link	Power	Wireless
IHEP	×	×	×		×	×	×	×	×	×
CCNU			×		×	×		×		
THU				×						
NPU			×					×	×	
NJU			×		×			×		
USTC								×	×	
WTU					×			×		
IPAS								×		
HPU					×			×		
T-ORILUX									×	
SDU			×							
NCU			×							
IME										×
USST							×			

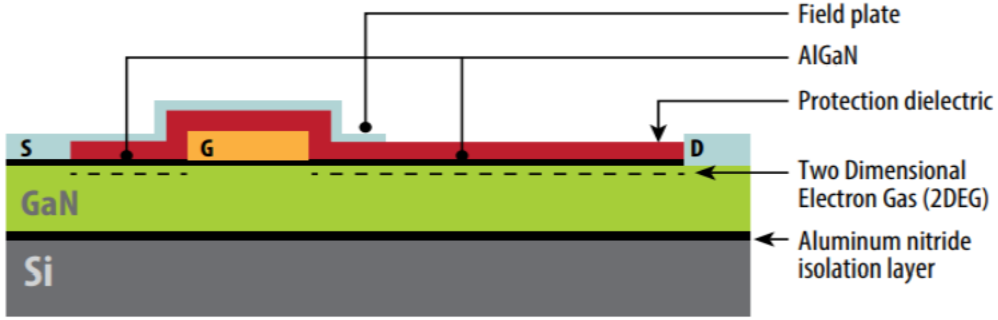
Naming of new ASICs

- Data Link：
  - FEDA: Front-End Data Aggregator ASIC
  - FEDI: Front-End Data Interface ASIC
  - OAT： Optical Array Transceiver Module
    - ALDD: Array Laser Diode Driver ASIC
    - ATIA: Array Transimpedance Amplifier ASIC
- Power：
  - PAL: Power At Load
- OTK ASIC:
  - LATRIC： LGAD Timing and Readout Integrated Chip
- SiPM ASIC：
  - SIPAC： SiPM ASIC for Calorimeter

Technology survey and our choice on Powering

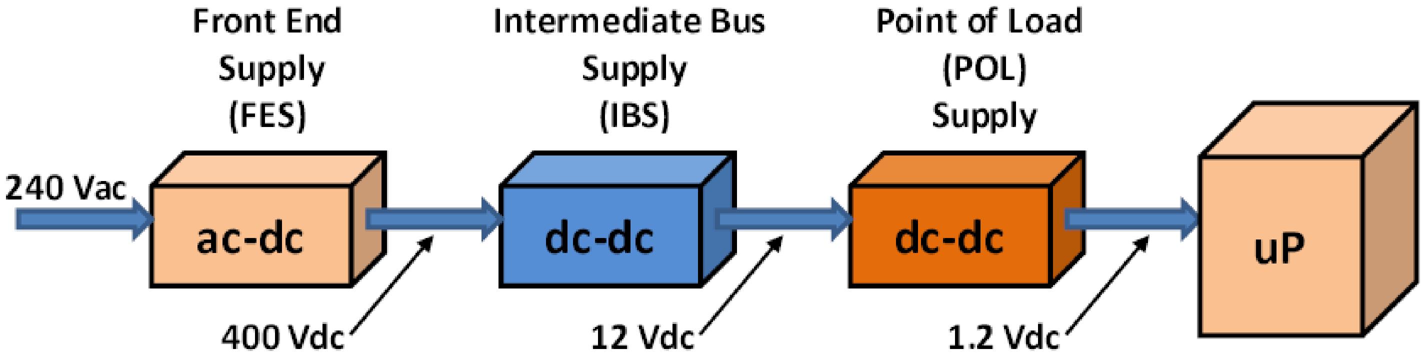


Higher switching Freq, smaller size,
higher efficiency, lower on-resistance



Increased radiation hardness (no SiO2, responsible for most TID effects in Si MOSFETs, in contact with the channel)

Ref. Satish K Dhawan, 2010
Ref. S. Michelis, Prospects on the Power and readout efficiency

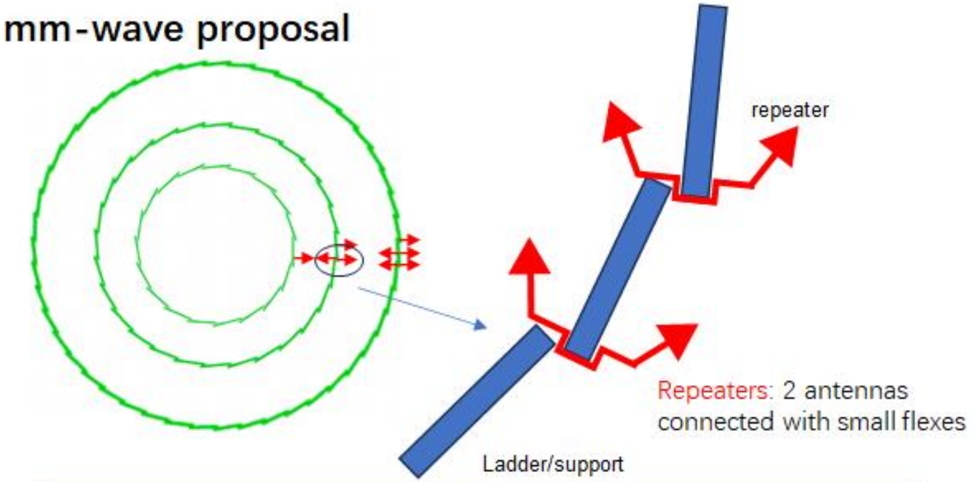


A 400V to 1.2V chain, lower power loss on cable

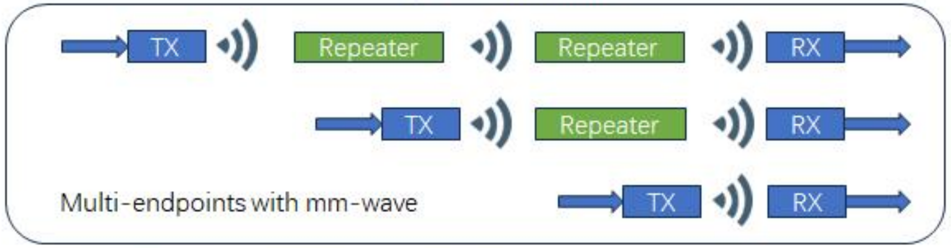
- Investigation was also conducted to compare the key component schemes of the power module, esp on LDO & DC-DC convertor.
- The GaN transistor has been a game changer in recent years, enabling DC-DC converters to achieve ultra-high efficiency, high radiation tolerance, and noise performance comparable to LDO.
- We choose a GaN-based DC-DC as the baseline power module scheme. This also enables high voltage power distribution, for low cable material and low power loss.

R&D efforts and results on WLess Comm

mm-wave proposal



Repeaters: 2 antennas connected with small flexes

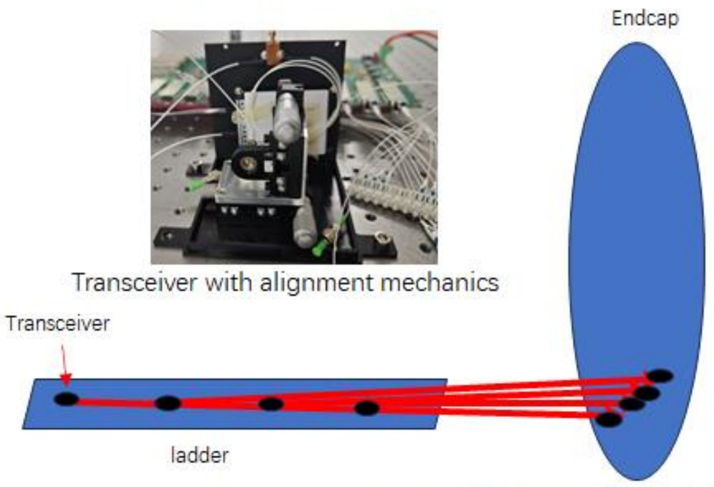


Multi-endpoints with mm-wave

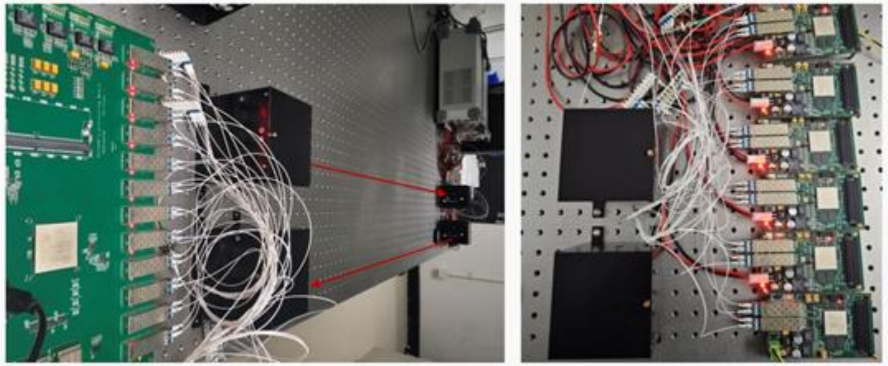
Test with evaluation boards – SK202
- Based on the commercial 60GHz RF chip ST60A2 transceiver from ST Microelectronics company.
- The transmission speed can exceed 900Mbps when the distance is less than 6 cm.

- Design a small PCB module with ST60A2. LNA and custom antenna.
- Higher bandwidth and longer distance
- Evaluate the interference with detector
- Under design, cheap and easy
- → custom transceiver + antenna +AIP

Optical wireless proposal



Transceiver with alignment mechanics



DWDM transceivers +AWG + lens
- Up to 6-meter free space optical transmission distance
- 10Gbps X 12 channels bandwidth
- PRBS 31bits error rate < BER-15 @ 10Gbps under 1.6m distance

A summary of FEE power

	Vertex	**Pix(ITKB)**	**Strip (ITKE)**	**OTKB**	**OTKE**	**TPC**	**ECAL-B**	**ECAL-E**	**HCAL-B**	**HCAL-E**	**Muon**
Channels per chip	512*1024 Pixelized	512*128	1024	128		128	8~16 @common SiPM ASIC				
Technology	65nm CIS	55nm HVCMOS	55nm HVCMOS	55nm CMOS		65 CMOS	55nm CMOS (or 180 CMOS?)				
Power Supply Voltage (for DC-DC) (V)	1.2	1.2	1.2	1.2		1.2	1.2 (or 1.8?)				
Power@chip	40mW/cm^2 200mW/chip	200mW/cm^2 800mW/chip	200mW/cm^2 800mW/chip	20mW/chn 2.56W/chip		280µW/chn 35mW/chip 100mW/cm^2	15mW/chn 240mW/chip				
Max chips@module	29	14	14	22	22	1115	64	120	8	92	167
Power@module (W)	5.8	11.2	11.2	27.6	27.6	32.2	30	30	9	11	4.7