FE-Electronic, 2026/05/18-22

OBELIX-1, a dedicated MAPS for the Belle II experiment

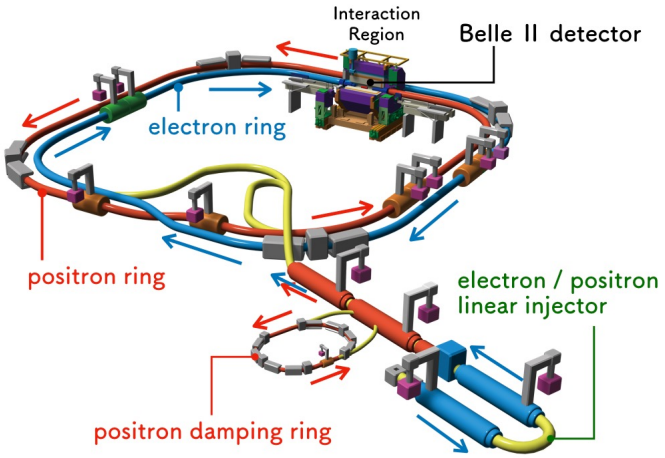
Thanh Hung PHAM on behalf of The Belle II VTX collaboration

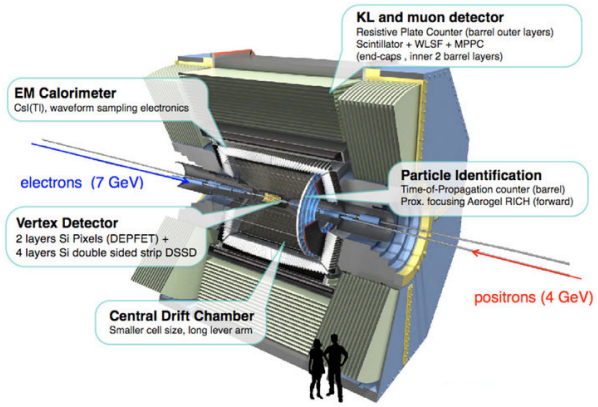
- SuperKEKB Accelerator and Belle II Experiment
- VTX Upgrade
- TJ-Monopix Measurements
- OBELIX Design
- Summary & Status

OBELIX Design Team

- CPPM, Marseille
- INFN & University of Pisa
- INFN & University of Bergamo
- IFIC (CSIC-UV), Valencia
- IPHC, Strasbourg
- KEK, Tsukuba
- MBI, Vienna
- University of Bonn
- University of Dortmund

SuperKEKB Accelerator & Belle II Detector





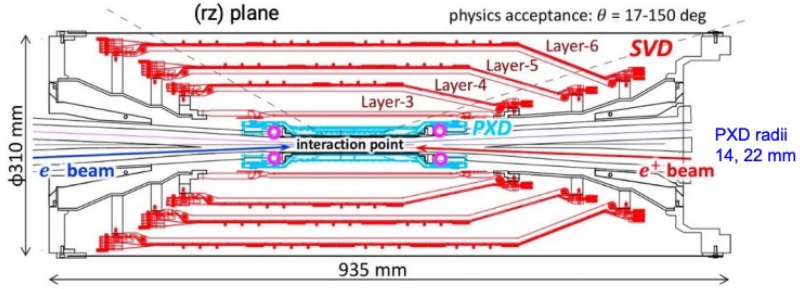
- **SuperKEKB accelerator:**
  - Tsukuba – Japan
  - e+e- collider, 3km circumference
  - Asymetric energies: 7 GeV (e^-) x 4 GeV (e^+)
  - Nominal operation at Y(4S) on $\sqrt{s}$=10.58GeV for B meson factory but also charm and tau
  - High Luminosity (world record) by using nano beam and large crossing-angle:
    - Peak: 5.2×10^{34} $cm^{-2}s^{-1}$ (Ultimate goal: 6×10^{35} $cm^{-2}s^{-1}$)
    - Integrated today: 804 fb^{-1} (Final target: 50 ab^{-1})

- **Belle 2 Detector:**
  - Vertex detector (VXD): PXD (2 layers) & SVD (4 layers)
  - Tracking detector : Central Drif Chamber (CDC)
  - Particle identification : TOP & ARICH
  - EM Calorimeter (ECL)
  - KL and muon detector

BELLE II Vertex detector and upgrade

- **PXD :**
  - Layer 1 & 2
  - DEPFET pixels
  - radius: 1.4cm & 2.2 cm
  - Material budget = 0.25% Xo/layer
  - Integration time = 20 µs
  - Spatial resolution ~15µm

- **SVD:**
  - Layer 3, 4, 5, 6
  - Double-Sided Silicon Detector + APV chips
  - Radius: 3.9cm to 13.5cm
  - Material budget = 0.76% Xo/layer
  - Spatial resolution : 7 to 12 µm (p-side) & 15 to 25 µm (n-side)
  - Time resolution ~3ns



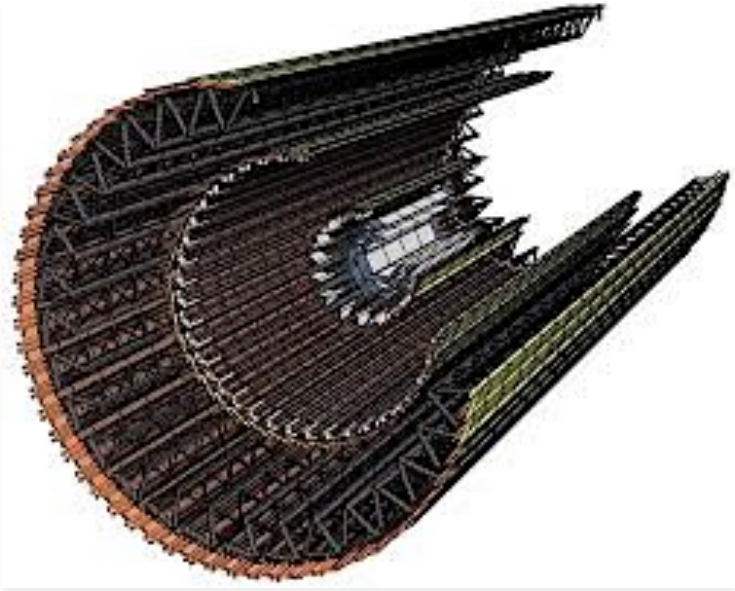
layer	PXD1	PXD2	SVD3	SVD4	SVD5	SVD6
radius (mm)	14	22	39	80	104	135
trigger rate (kHz)	30		30 with 6 APV25 samples 70 with 3 APV25 samples			
occupancy (%)	3		2.6	0.8	0.6	0.4
hit rate (MHz/cm^2)	52.2	33.9	2.8	0.9	0.4	0.2
TID (MRad)	> 20		10	10	10	10
NIEL $\times 10^{12}$ (cm^{-2})	100		10	10	10	10

TABLE IV: Limits of the current VXD system, encompassing both technical and physics-driven performances.

- **Higher luminosity ➔ Increase in:**
  - Beam background (hit rate)
  - Trigger latency for high efficiency
  - Irradiation level (TID & NIEL)

➔ **VTX upgrade**

VTX Upgrade



#ladders = 160
#sensors ~2500

- **Requirements:**
  - Spatial resolution: <10-15 µm
  - Total Material budget: 3.5% X_0
  - Average hit rate: lower than 120MHz
  - Time precision: <100ns
  - Trigger rate: 30KHz
  - Trigger latency: 5-10µs
  - Rad. Hard (inner)
    - TID < 100 kGy/year
    - 10 years fluence <$5x10^{13}_{neq}/cm^2$/year

+ Time stamping < 5ns
+ Information for L1 triggers

- **Concept:**
  - Same sensor for all layers based on DMAPS technologie
  - Low space-time granularity ➔ occupancy << 1%
  - 2 inner layers (iVTX) :
    - All silicon concept ladder
    - Material budget < 0.3% X_0
    - TPG (Thermal Pyrolitic Graphite)
  - 3 outer layers (oVTX):
    - Sensor+flex+cooling-plate+support
    - Material budget < 0.8% X_0
    - Water cooling

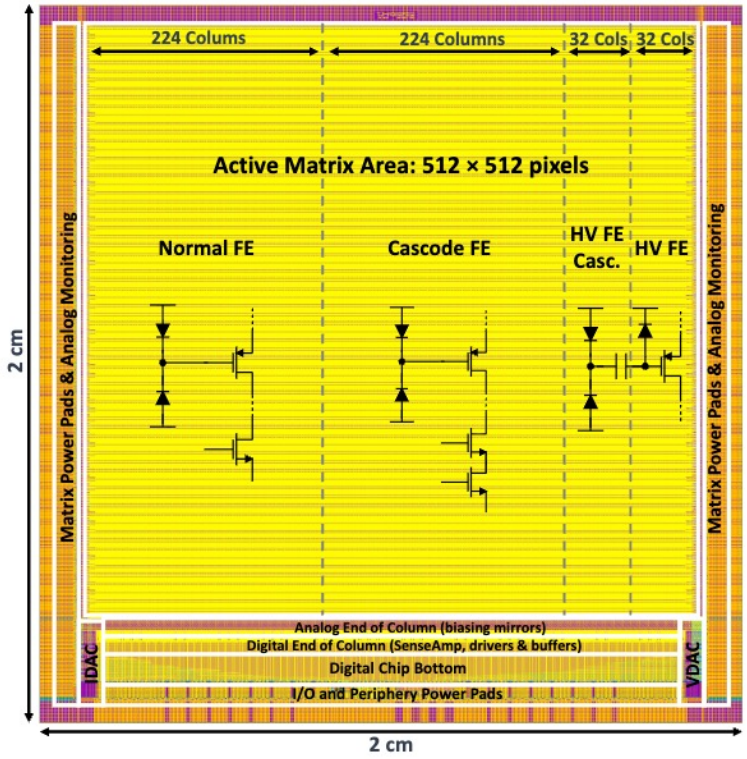
From TJ-Monopix to OBELIX

	Belle-II depleted MAPS	TJ-Monopix2
Sensitive area	~30x17 mm^2	17x17 mm^2
Sensitive thickness	~30 µm	25-100 µm
Pitch	30 to 40 µm	33 µm
Signal digits	1 to few bits	7 bits ToT
Integration time	50 to 100 ns	25 ns
Hit rate (average)	120 MHz/cm^2	> 100 MHz/cm^2
Triggered read-out	30 kHz, lat. 10 µs	
Power	~200 mW/cm^2	200 mW/cm^2
TID fluence	~1 MGy ~5.10^{14} n_{eq}/cm^2	1 MGy 3.10^{15} n_{eq}/cm^2
Oper. Temp.	room+	-20 °C

The TJ-Monopix2 fulfilled almost all Belle II requirements
➔ Forerunner for OBELIX-1 (**O**ptimized **BEL**LE II P**ix**el Sensor)

- **The OBELIX-1 concept will emphasize on:**
  - **Digital-on-Top integration flow**
  - **Increasing matrix dimensions**
  - **Adding on-chip LDOs**
  - **New digital logic**

TJ-Monopix2 – Key points



Source: K.Moustakas (2021), Bonn University
DOI: https://doi.org/10.48565/5q6f-cf97

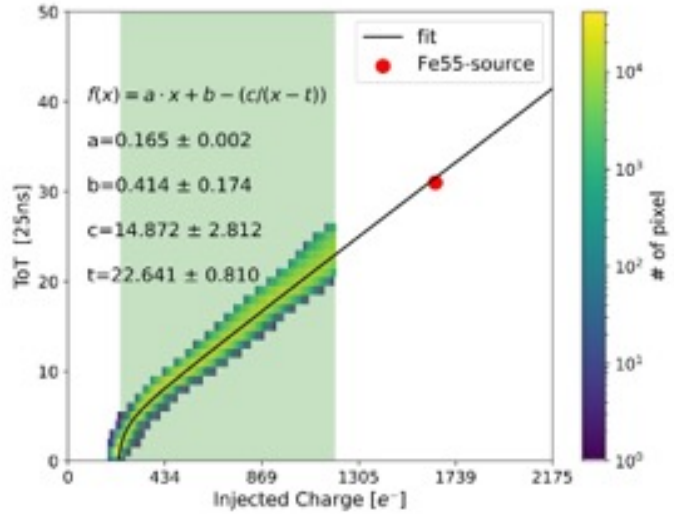
- Key points:
  - **Technology** : 180nm with modified process for full depletion
  - **Architecture** : Column-drain with data-driven readout
  - **Pixel matrix** : 512x512 pixels (33.04x33.04 μm^2)
  - **Front-end** : 4 ALPIDE like pixel flavors based on Front-End circuit (Normal/Cascode) & Input coupling (DC/AC)
  - **Threshold Tuning** : 3-bit DAC per pixel for fine threshold tuning
  - **Timing** : 7-bit timestamping with 25 ns clock period (ToA and ToT)

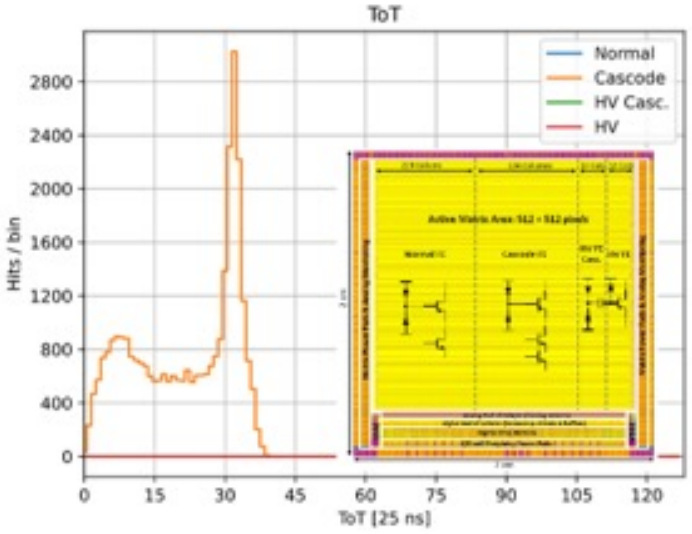
TJ-Monopix2 – Test results (lab mesurement)

- Threshold/noise (un-irradiated chips)
  - Stable operation down to THR~ 250 e- (MIP signal in 30 µm Si MPV ~2000 e-)
  - THR dispersion ~8 e- after THR tuning
  - Noise ~6 e-

- ToT calibration with ^{55}Fe source
  - DC = 9 e- /DAC
  - AC = 18 e- /DAC

➔ Match with designed DAC resolution & injection capacitor

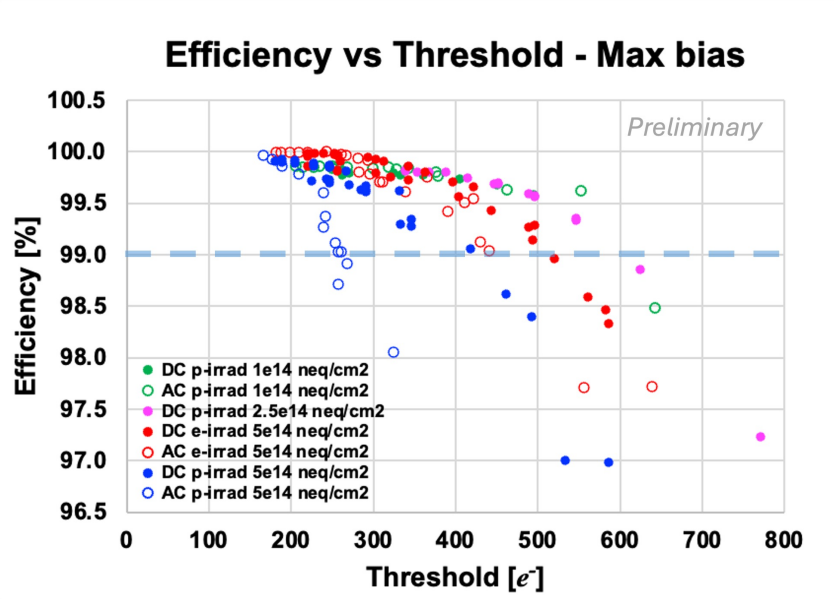


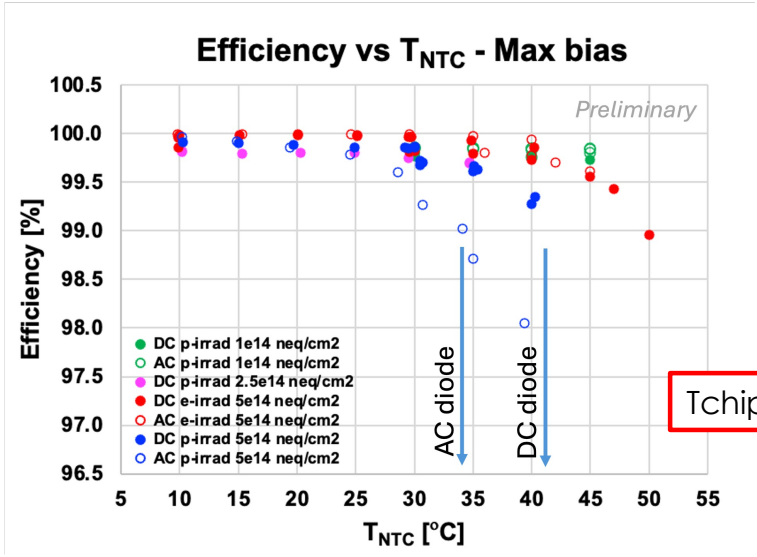


TJMP2 sensor is divided in 4 regions with different pixel FE

TJ-Monopix2 – Test results (beam test)

- Different beam test campaigns from 2022 to 2025 allow the choice of the front-end and operational temperature for OBELIX:
  - 3 p-irradiated: NIEL 1-2.5-5x10^{14} neq/cm^2
  - 1 e-irradiated: NIEL 5x10^{14} neq/cm^2

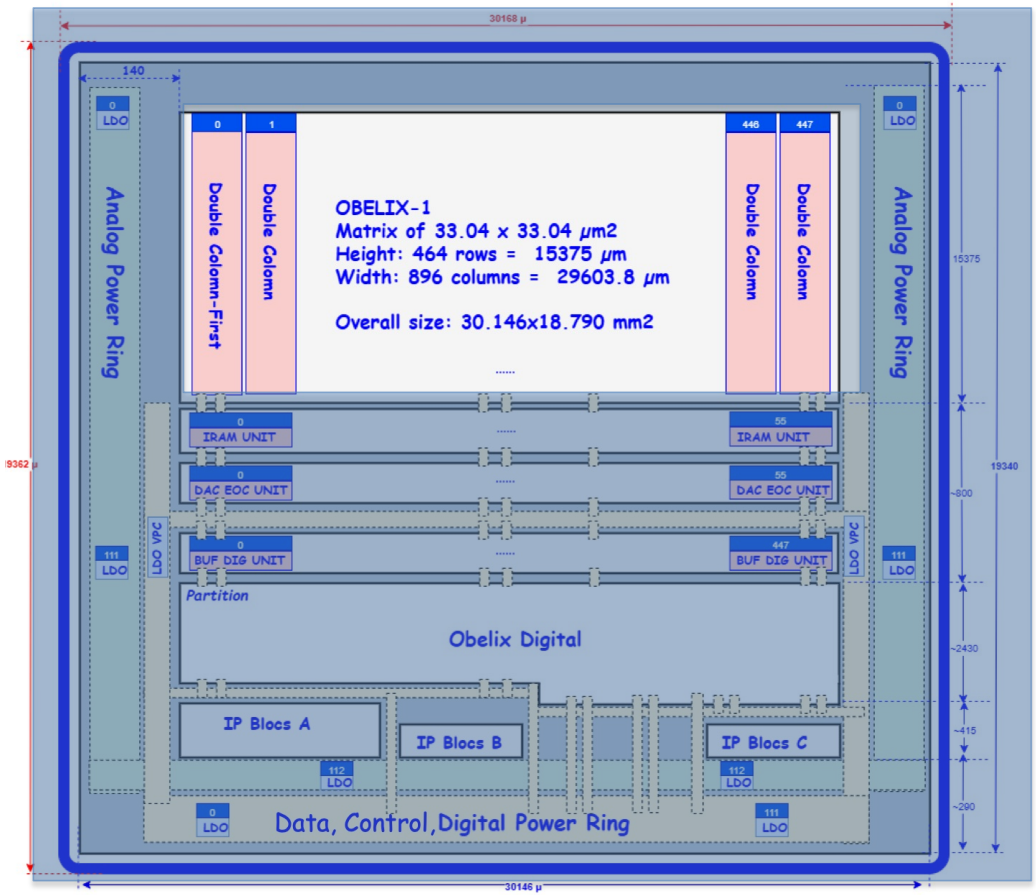




Tchip ~ TNTC + 7°C

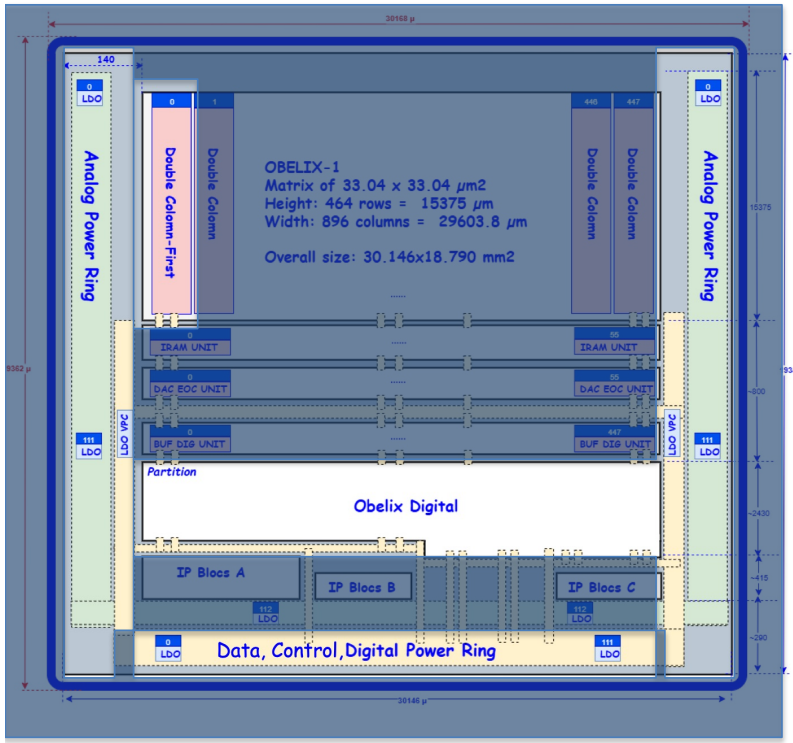
- **Operational temperature: <40°C**
- **Fake hit rate at 500 e- THR & 40 °C ~ 10^{-2} Hz/pixel (10^{-3} MHz/cm^2)**
- **Effi_dc < 99 % at THR > 400 vs Effi_ac < 99 % at THR > 250**
- **At 40°C: Effi_dc > 99 % vs Effi_ac <99 %**

OBELIX design



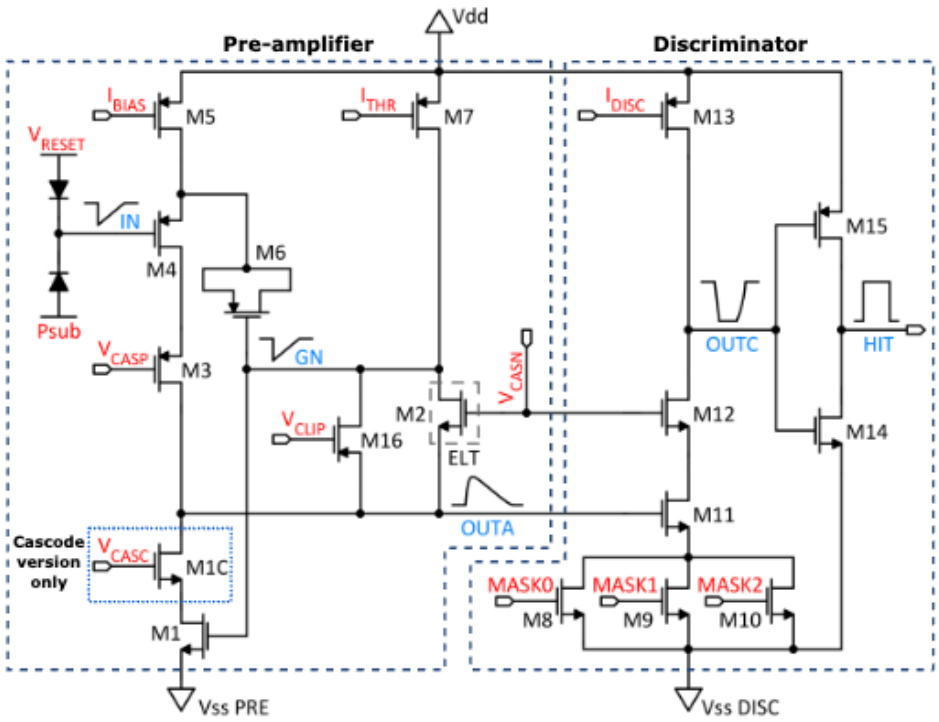
- **Pixel matrix: same pixel & readout architecture as TJ-Monopix2 but:**
  - Reduction of timing clock time stamping frequency to 21.2 MHz
  - New BCID (timing clock) drivers for mitigating cross-coupling effects
  - Increased threshold tuning (IDAC) to compensate on-chip gradient temperature
  - Increase matrix size to 464x896
  - Increase injection range by replacing pulsing voltage buffer

OBELIX design



- **Powering: new powering scheme based on on-chip regulation**
  - LDO regulators for all power inputs
  - LDO bypass possible from external
  - Single analog domain
- **Monitoring:**
  - 32 power and 32 temperature sensors
  - 4 pixels with various signal outputs
- **Digital periphery:**
  - 2 level data buffering & triggers management
  - Trigger output for L1 (outer layer only)
  - High precision time stamping at low hit rate (outer layer)

Front End



TJ-Monopix2 Cascode FE & DC coupling

Source: K.Moustakas, PHD Thesis, Bonn University,2021

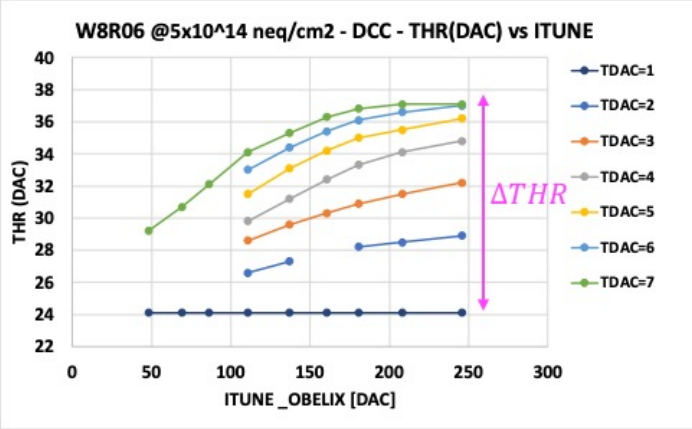
- Interdependent parameters controlling the FE gain and hence threshold but could be summarized as follows:
  - IBIAS : Amplifier's gain and bandwidth
  - ITHR : Return to base-line time constant
  - VCASN : V_{OUT} base-line ➔ Discriminator threshold
  - I_{DISC} : Discriminator bandwidth + threshold
    ➔ I_{DISC} is used to fine tune the discriminator threshold ($I_{DISC} = I_{M11}$)

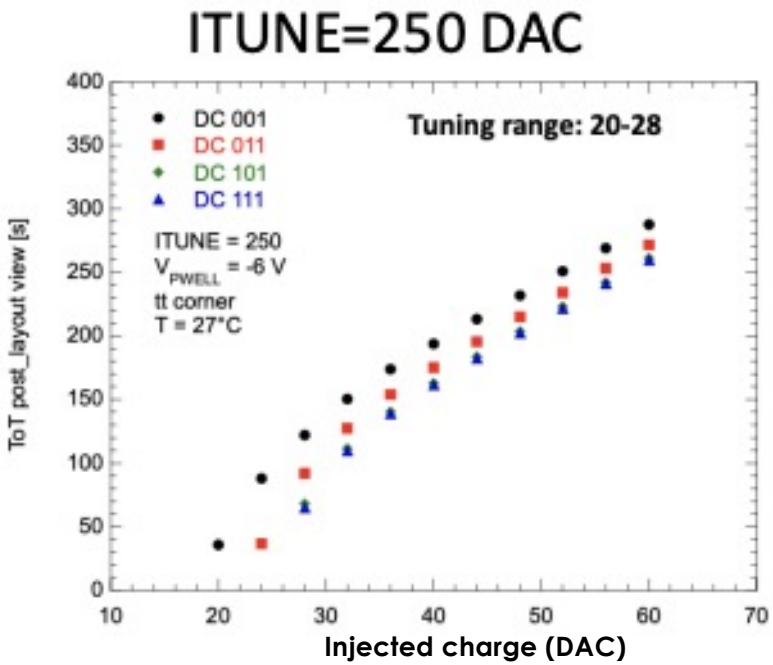
➡
- ✓ Cross-correlation of measurements and simulations to validate the simulation testbench
- ✓ Determine the tuning range for compensating temperature variation

Front End (Suite)

- Measurement vs Post-layout simulation:

  - **Injection capacitor** : High agreement (~220 aF @ DC/~343 aF @ AC)
  - **Gain** : Meas/Sim < 1.25 (x2 of signal duration)
  - **Threshold Ratio** : Meas/Sim = 1.45 (with FS option)
  - **ToT vs Qinj** : Not conclusive (chip-to-chip variation)
  - **THR@Temperature** : 8 DAC/10 °C (35 °C,-,40 °C)
    - **4xITUNE in OBELIX** : overwritng with external source in measurment
    - **non-irradiated** : 6.5-9.5 DAC (meas) vs 8 DAC (sim)
    - **irradiated chip** : 13 DAC (DC) & 8 DAC (AC)

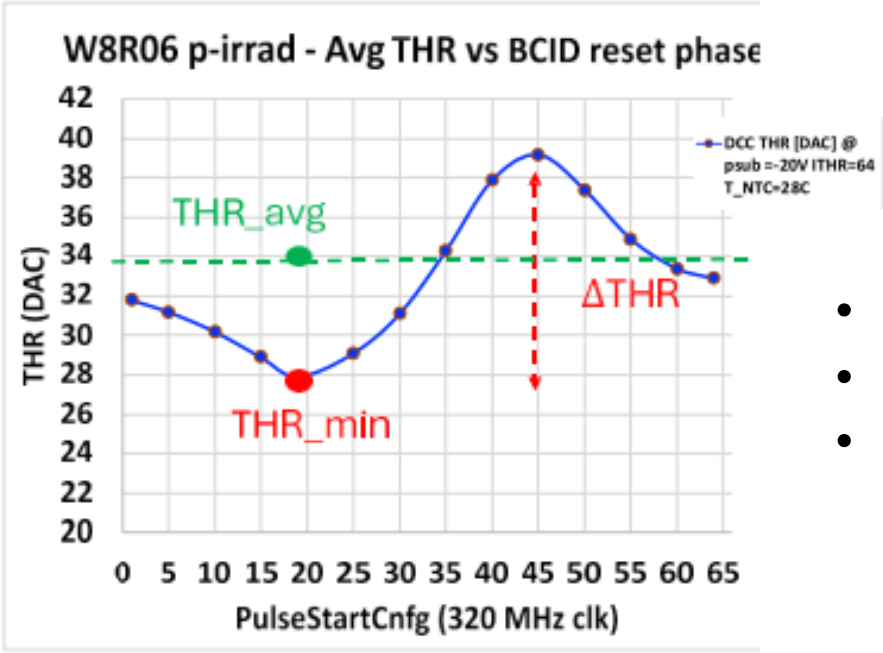




Simulation (DC, PWELL@-6V)

BCID coupling effect & mitigation

- Threhold oscillation correlating to BCID phase observed in measurement

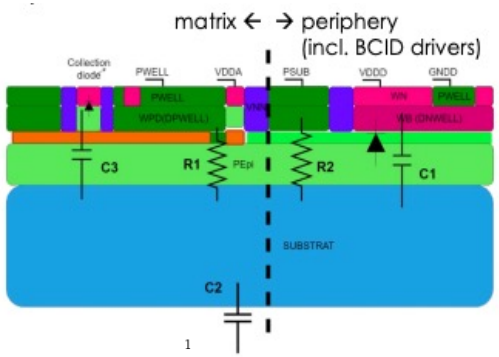


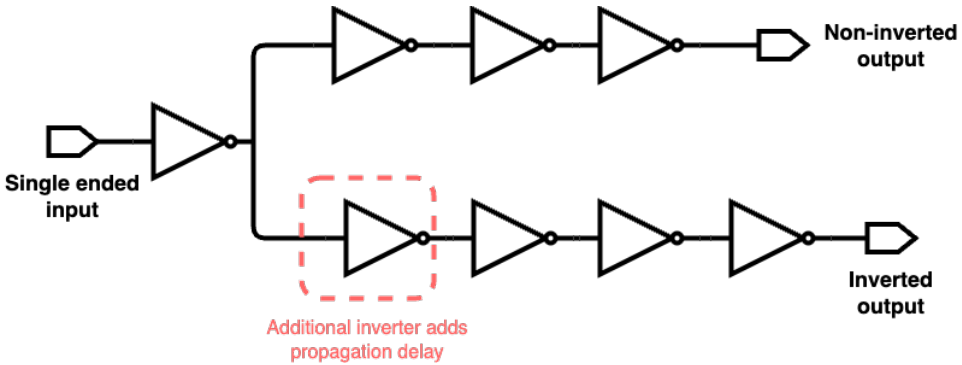
- Δ THR ~120 e-
- Not reproducible in simulation ➔ Global effect
- Up to 180 e- with OBELIX due to larger pixel matrix

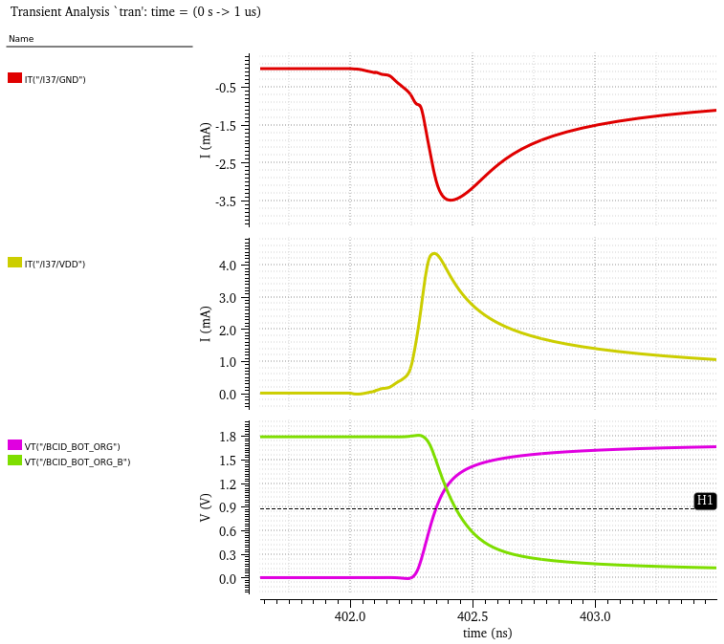
http://arxiv.org/abs/2402.12153

BCID coupling effect & mitigation

- Possibly caused by noise induce by BCID drivers power supply to pixel input through substrat:
  - All BCID column-drivers commuting together ➔ generating large current spikes on digital power supply
  - Not ideal driver having perfectly balenced and symetric complemntary outputs



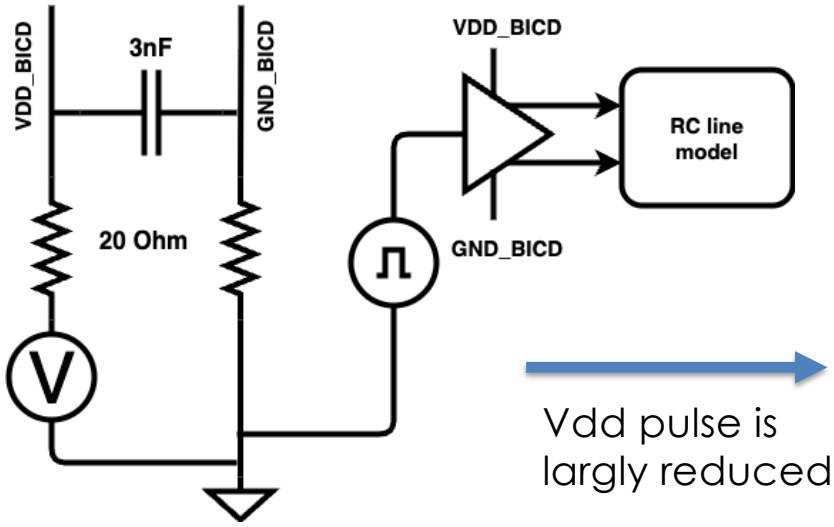




TJ-Monopix BCID buffer driver & simulation

BCID coupling effect & mitigation

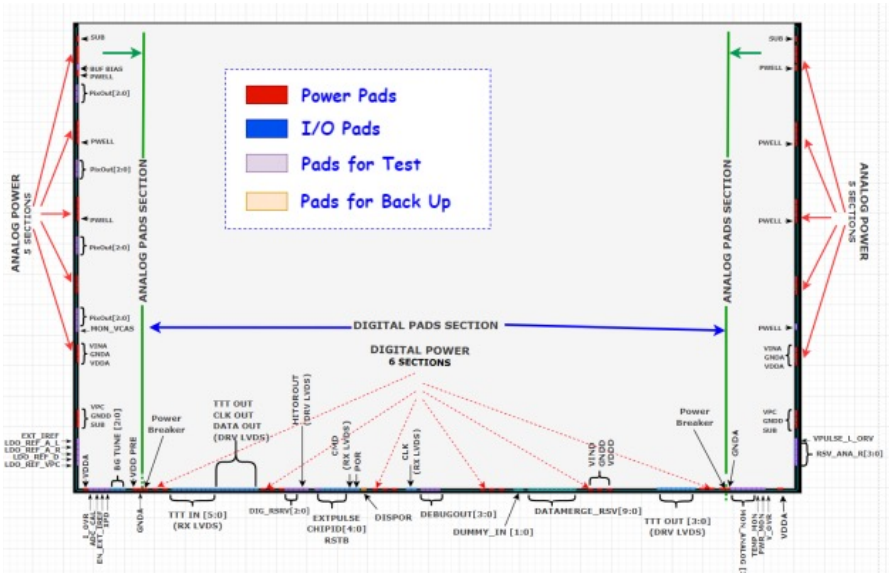
- Mitigation: Limitation of output swing & slew rate using complementary source follower output stages
  - Reduced current drawn from VDDD
  - Reduced peak current
  - Reduced voltage swing from 1.8 V to 0.75 V
- Simulation Test Bench (for comparison only, not for absolute values)
- Data integrity validated with full testbench including: Buffer, Pixel double column + readout circuit



Power distribution & on chip regulation

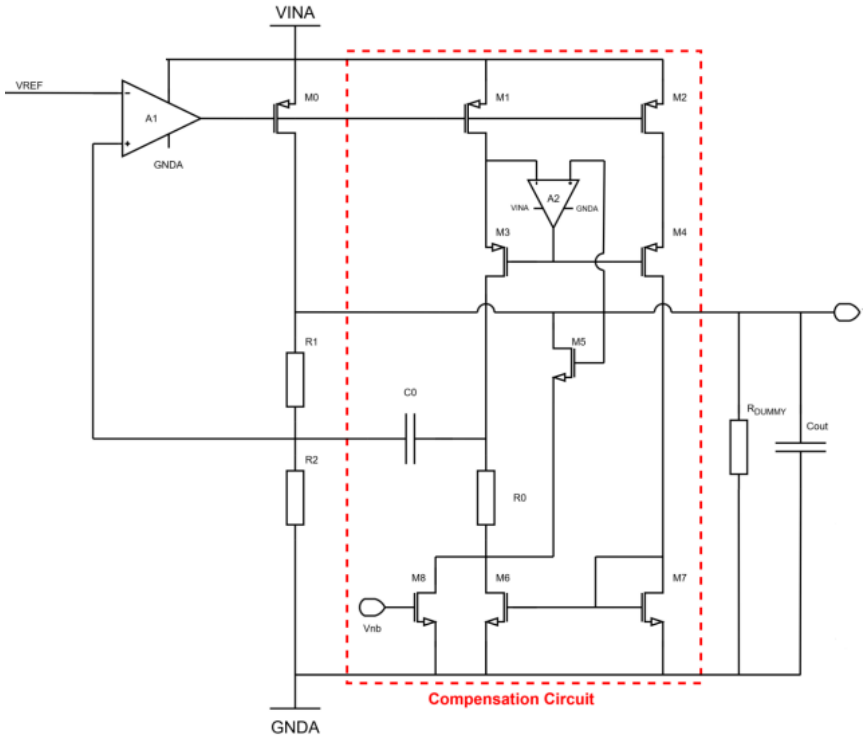
- OBELIX power consumption :

Contributor	Analog (mW)	Digital (mW) @ 120 MHz/cm²
Matrix	432	7.5
Periphery	59	550
Pads	0	18
Pass Transistor @ 2V	50	64



- Power pad distribution:
  - Analog Power Pads ➔ Left and Right sides
    - 5 Sections of VINA, VDDA, and GNDA Pads
    - PWELL & PSUB pads for matrix and sensor substrate biasing
  - VPC Pads ➔ Left and Righ side
  - VDD PRE Pad → Bottom side
  - Digital Power Pads → Bottom side
    - 6 sections of VIND, VDDD, and GNDD Pads

Power distribution & on chip regulation



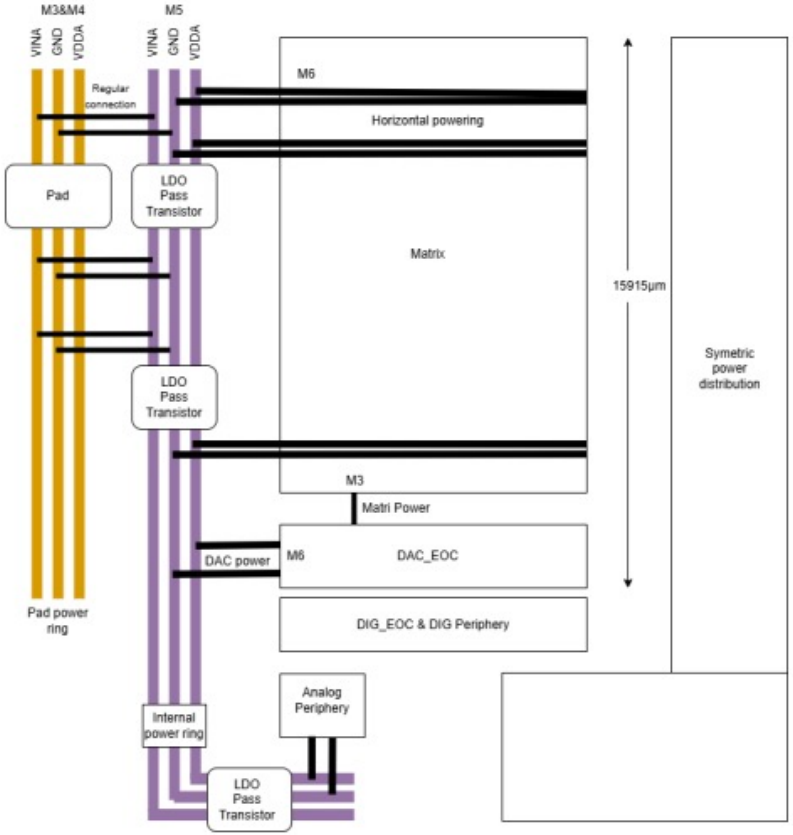
Regulator's architecture with compensation circuit

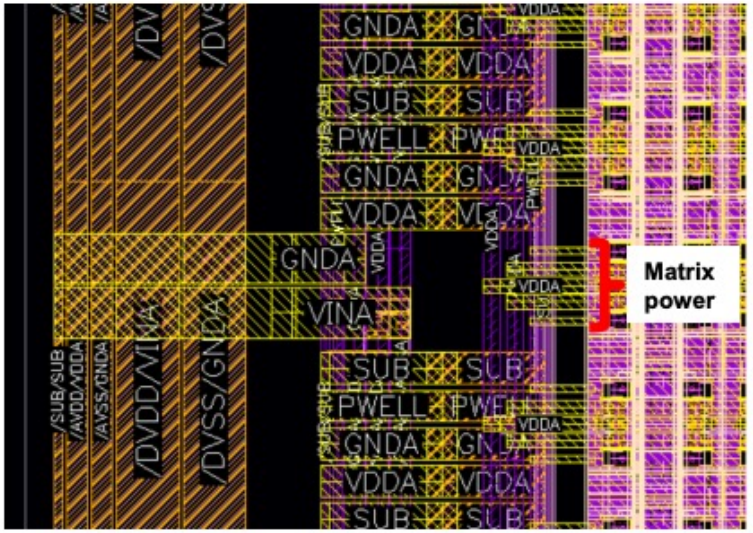
J. Kampkoetter and al, stabilization and protecti on of the Shunt-LDO regulator for the HL-LHC pixel detector upgrades

- On chip regulation:
  - LDO-Pre : Pre-regulation from VINA to power LDO tuning DAC
  - LDO-VPC: Bit-line Pre-charge voltage for Matrix SRAM readout circuit
  - 2 LDOA : Analog power domain with distributed pass transistors
  - LDOD : Digital power domain with distributed pass transistor

- LDO architecture:
  - Same architecture for all OBELIX's LDO
  - Compensation circuitry inherited from RD53 project concept and adapted for OBELIX
  - R0 & C0 form a double zero allowing circuit stabilization
  - The output voltage is defined by the feedback factor (R1, R2) and the reference voltage
  - Dummy resistor ensures minimum load current for stabilization

Power distribution & on chip regulation

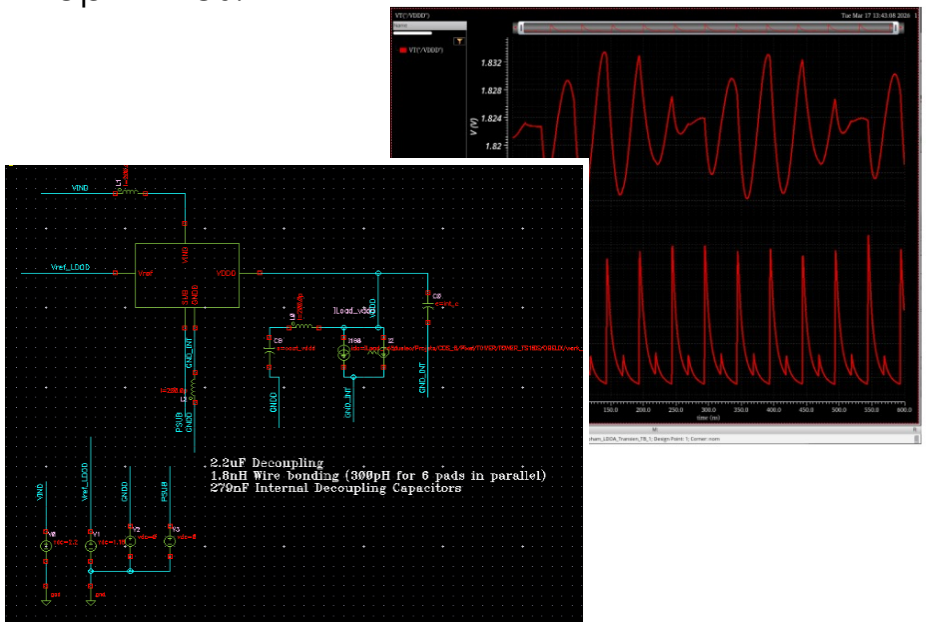




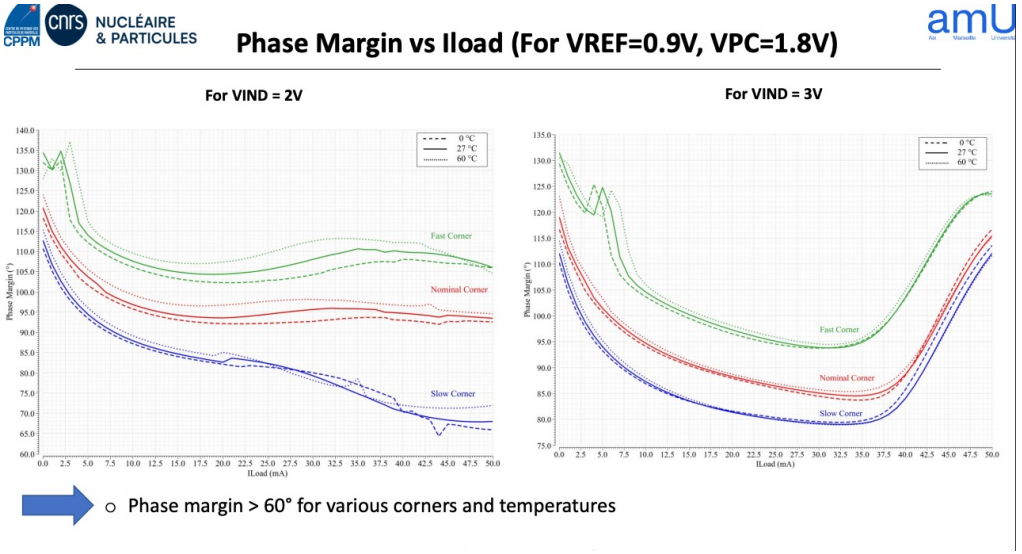
- Symmetrical power distribution on left and right sides to minimize voltage drop.
- Identical distribution system for digital power at the bottom of the circuit.

LDO performance simulations

- All LDOs meet specifications from simulation (Input/Output voltage, Load/Line regulation, Max load current, Load/Line transient)
- PM > 55° for chip-level extraction, corner & temperature variations.
- Start-up conditions validated with full pad frame using 100µs, 1ms and 100ms input voltage ramp-up times.

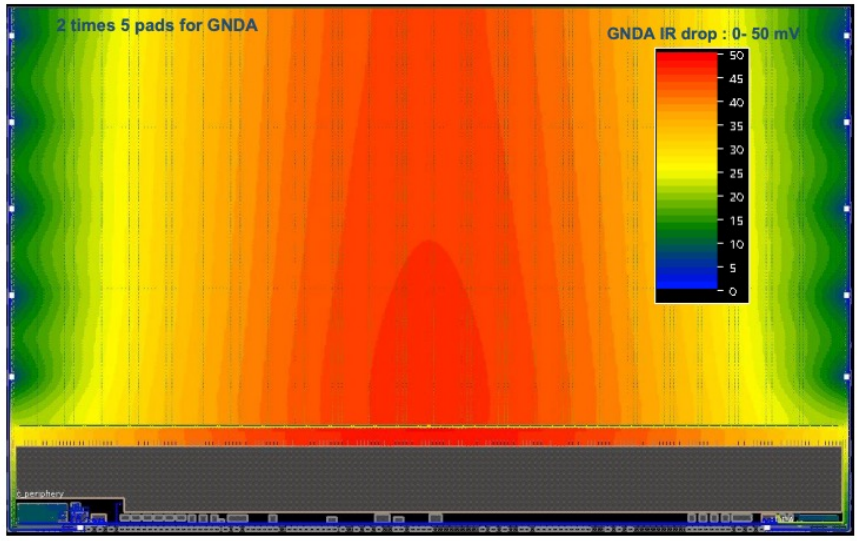


VDDD at regulator output vs digital current profile at 120MHz & 270nF on chip coupling capacitors

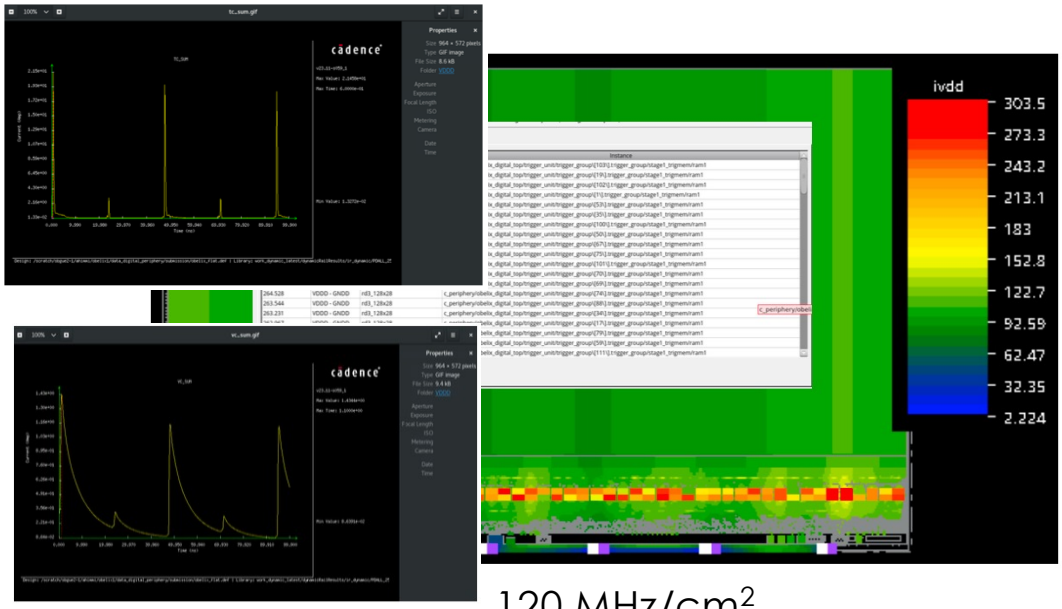


IR-Drop simulation

- **Static IR-Drop :**
  - Can not intergrate LDO into Voltus Flow ➔ Without regulation effect
  - VDDA & GNDA voltage drop are less than 15 mV in lateral direction (uncompensated) & 60mV/50mV (VDDA/GNDA) in horizontal direction (current bias compensation)
  - VPC voltage drop < 165mV



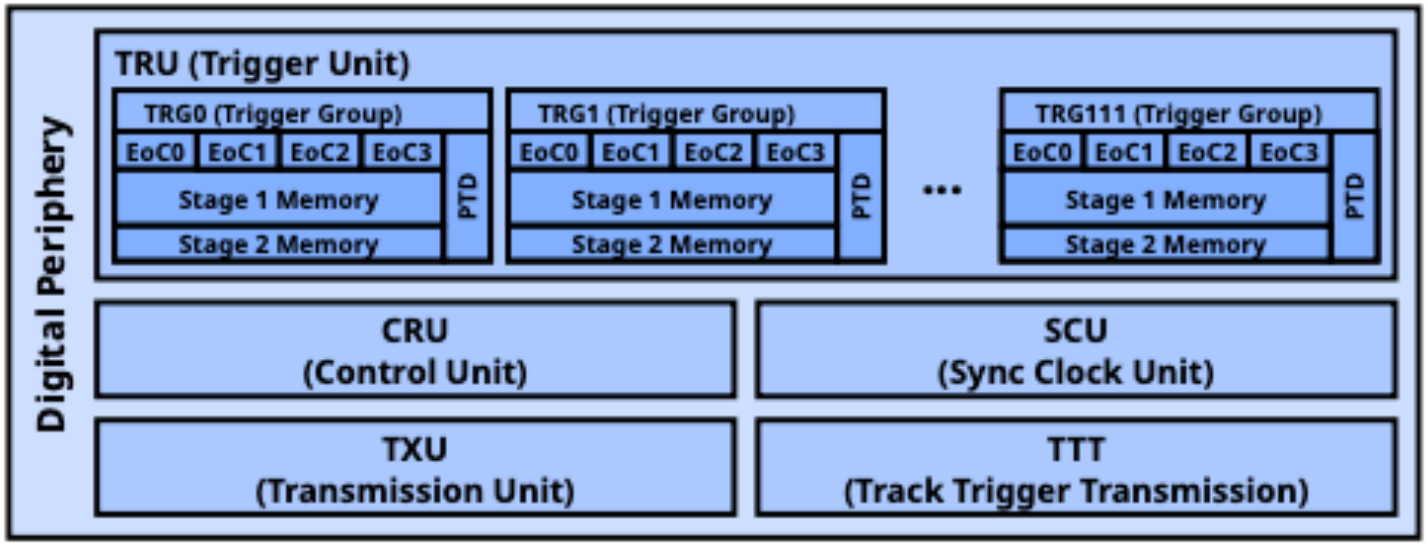
- **Dynamic IR-Drop :**
  - Digital power domain: Voltus flow & VCD files simulation inputs
  - Without LDO & Powered from Pads
  - Low IR-Drop across the circuit
  - At 120MHz/cm2 hit rate: large voltage drops at DRAM memory ➔ 10% local timing derating factor added from already 10% of global timing derating factor



120 MHz/cm^2

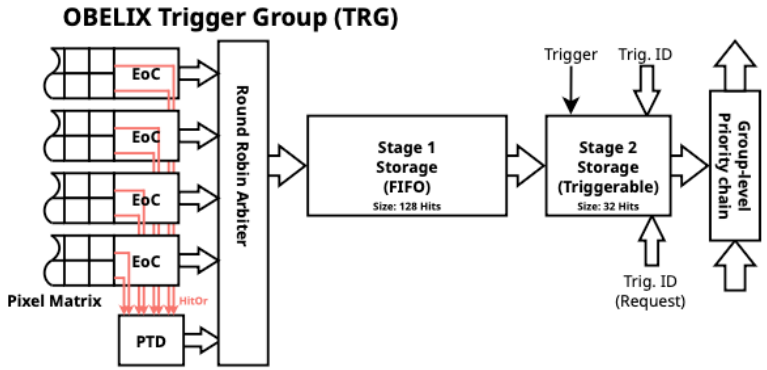
Digital periphery

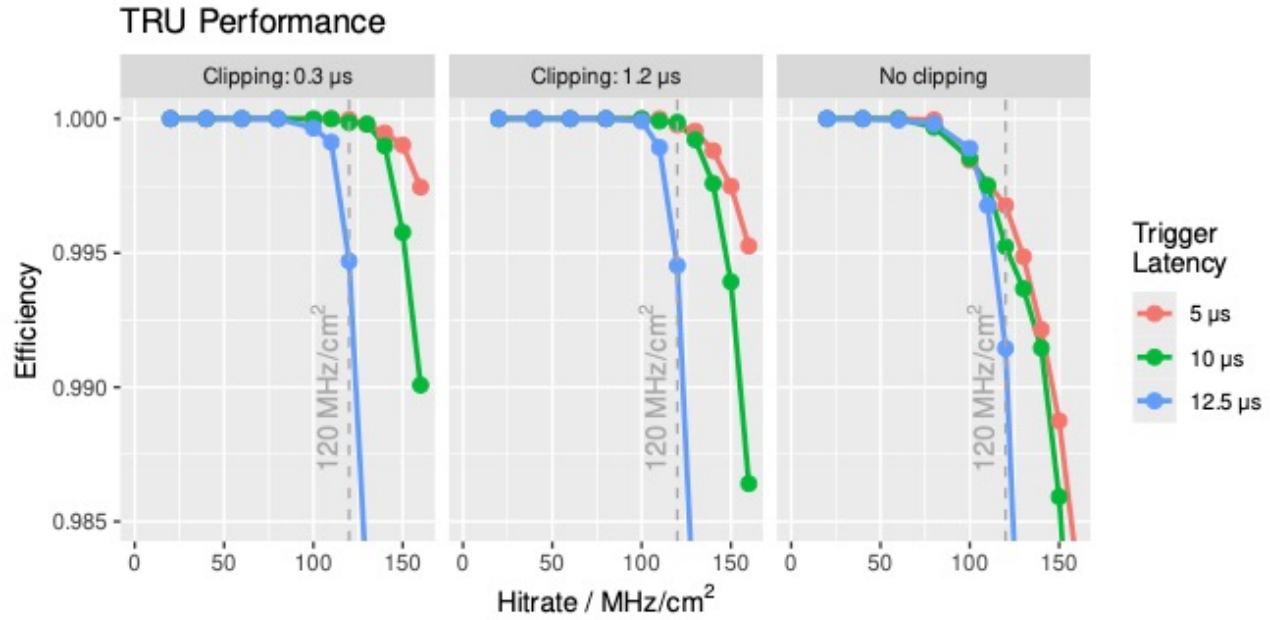
- Entirely new digital periphery in OBELIX that features:
  - Optimized logic to buffer data and meet Belle II specifications regarding for hit rate, trigger rate and trigger latency
  - A Peripheral Time to Digital Converter (PTD) providing a time binning of 2.95 ns from a 160 MHz input clock
  - A low-latency, low-granularity trigger that feeds the L1 trigger system, known as Track Trigger Trasmission (TTT)



Trigger Unit

- The Trigger Unit (TRU):
  - Provide matrix readout sequence (EoC logic)
  - 2 Stage data buffering
  - Trigger management

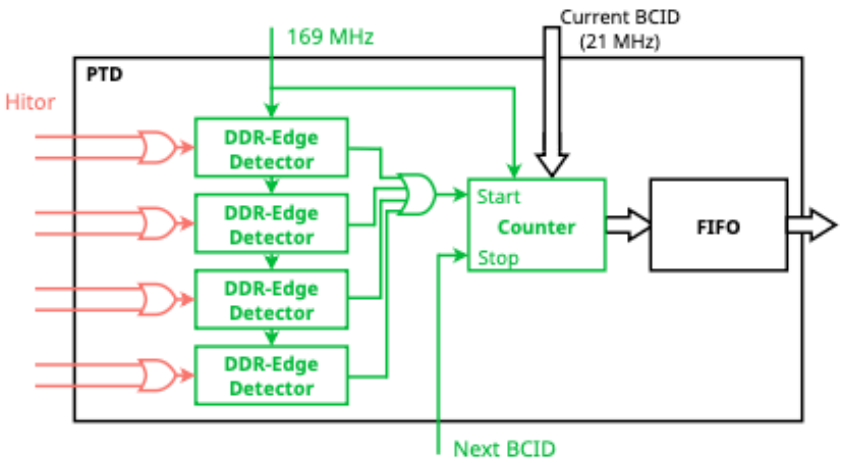


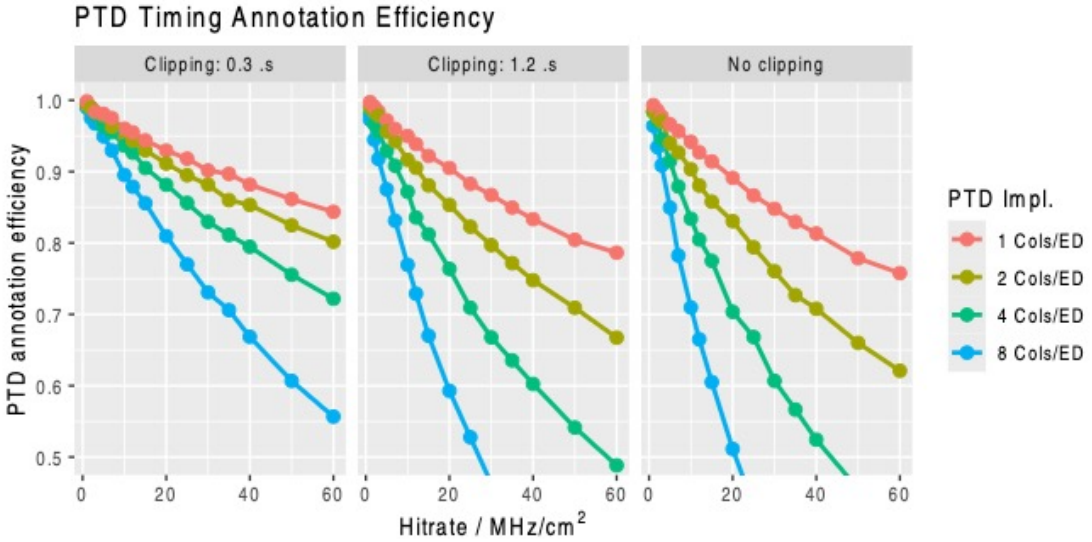


Source: M. Babelux (2025). TU. Wien
DOI: *10.34726/hss.2025.107368*

Peripheral Time to Digital

- Peripheral Time to Digital converter:
  - Sample Hit-Or from 8 column with double edge input clock to atteint 3.95 ns time binning
  - 2 Cols/ED is choiced for OBELIX ➔ high performance at low hit rate and consump less than 1 Cols/ED option

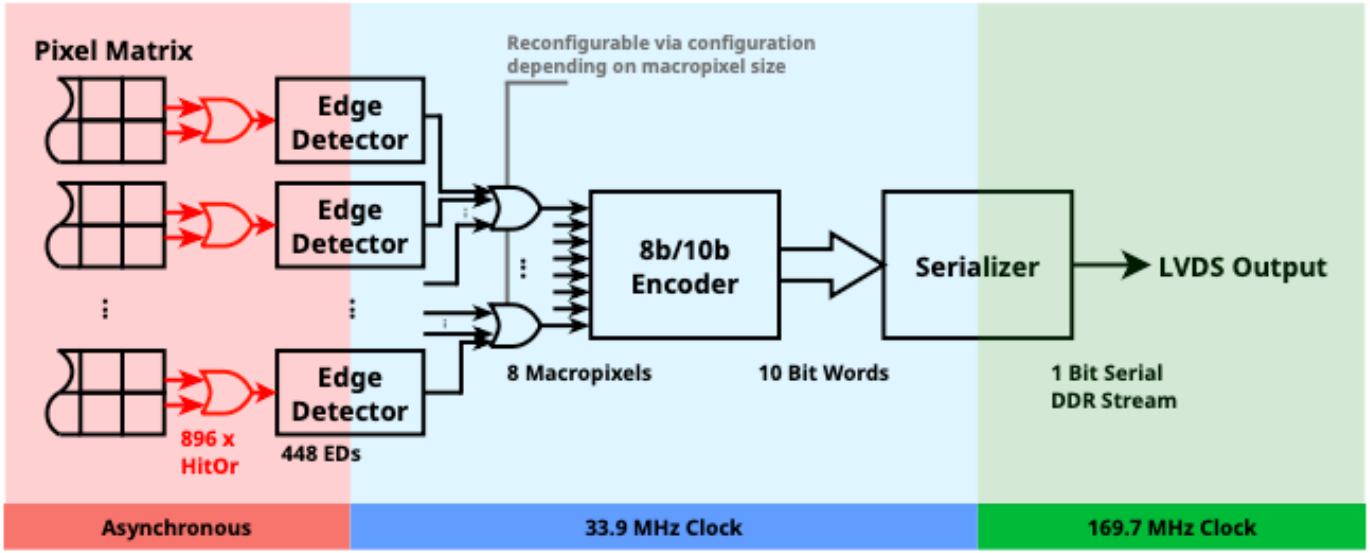




Source: M. Babelux (2025). TU. Wien
DOI: 10.34726/hss.2025.107368

Track Trigger Transmission

- Track Trigger :
  - **Low granularity**: using HitOr signals from multiple columns ➔ macro-pixel
  - **Low latency** : 3 cycles of 35 MHz clock + HitOr propagation time (< 42ns)
  - Additional trigger information contributes to L1 increase trigger system efficiency



Source: M. Babelux (2025). TU. Wien
DOI: 10.34726/hss.2025.107368

Verifications

- **Functional:**
  - CocoTB:
    - Written by RTL designer (therefore, not considered as independent)
    - Helpful for module-level testing
  - UVM
    - Abstract testbench of the top-level design of the digital periphery
    - Coverage-Driven Verification
    - Scalability & Reuse
    - Developed by verification designer
  - FPGA
    - implementation of RTL code on an Intel Cyclone 10GX 220 FPGA to emulate 128 DCs
    - Fast and powerful testing of digital periphery features.
- **Connectivity:**
  - Mixed-mode simulation:
    - Default configuration test
    - Verifies the core connection between the digital periphery and analog blocks.

Summary & Status :

- Confirmed TJ-Monopix2 performances (Lab & Beam tests), validating the technology for the Belle II environment

- OBELIX-1 development by integrating key improvements:
  - Optimized LDO-based power distribution
  - New BCID drivers to mitigate cross-coupling
  - Enhanced threshold tuning range

- The chip has been submitted to foundry. Chip return expected in Q4 2026

- Due to time constraints, several critical aspects of the design were not fully presented:
  - Monitoring & Testability: power & temperature sensors and monitoring pixels
  - Injection Buffer for increasing pulsing range

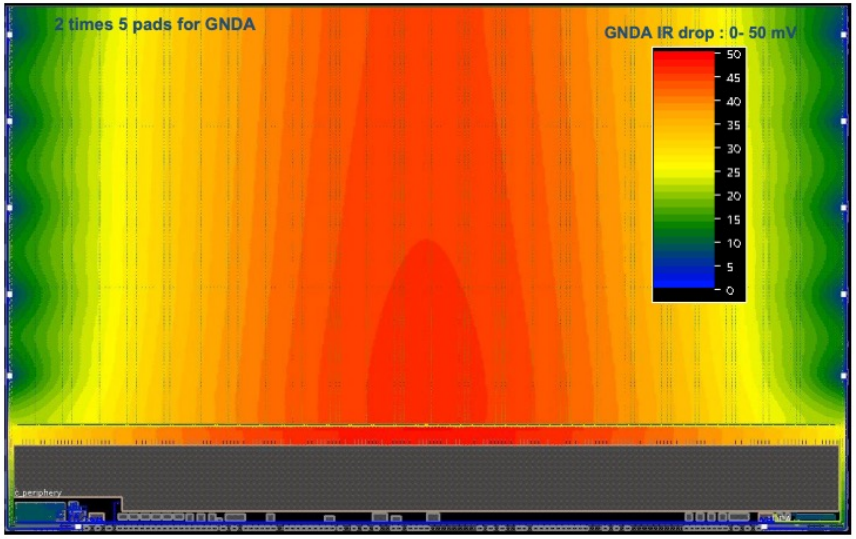
Acknowledgements

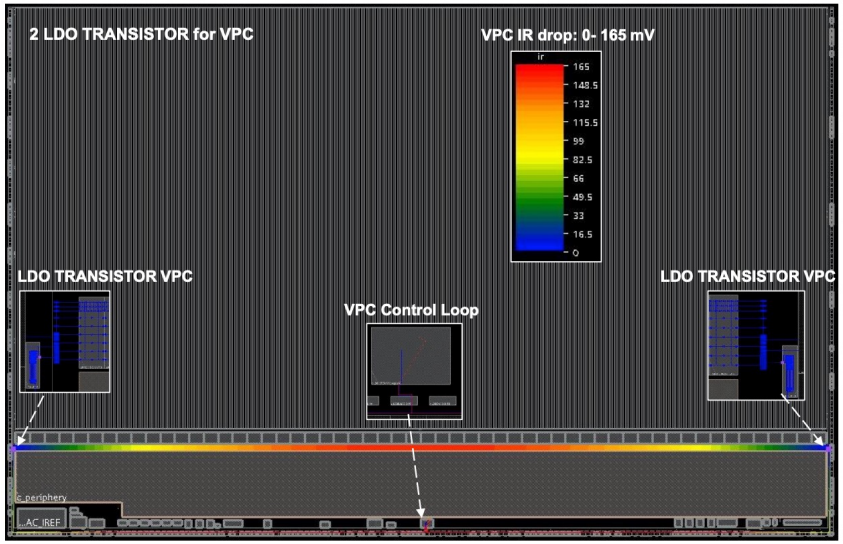
Sepcial thanks you to:

- The Design & Testing Teams for their valuable contributions thoughout the project
- The DESY service for their outstanding support and the beam test facility

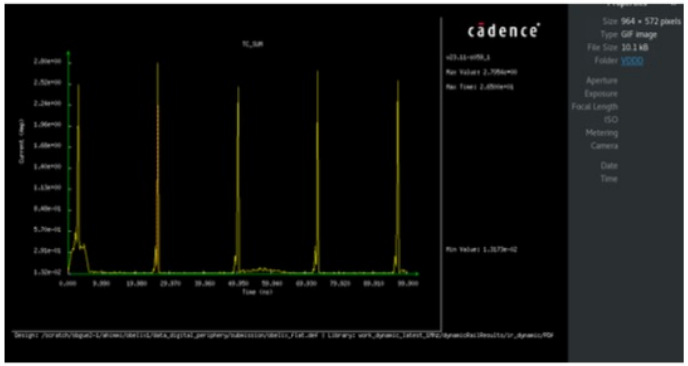
Backup

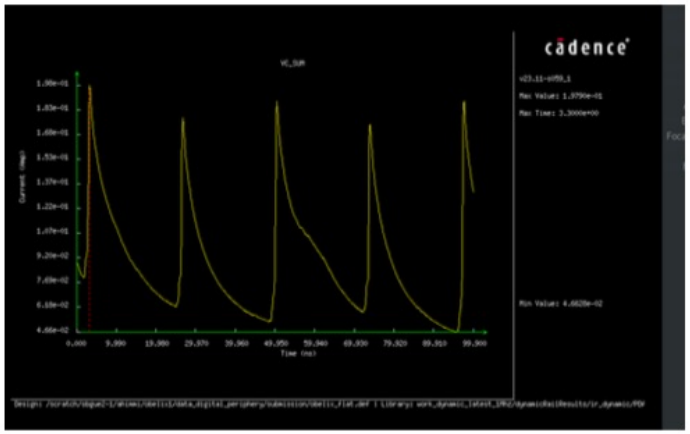
IR-Drop simulation

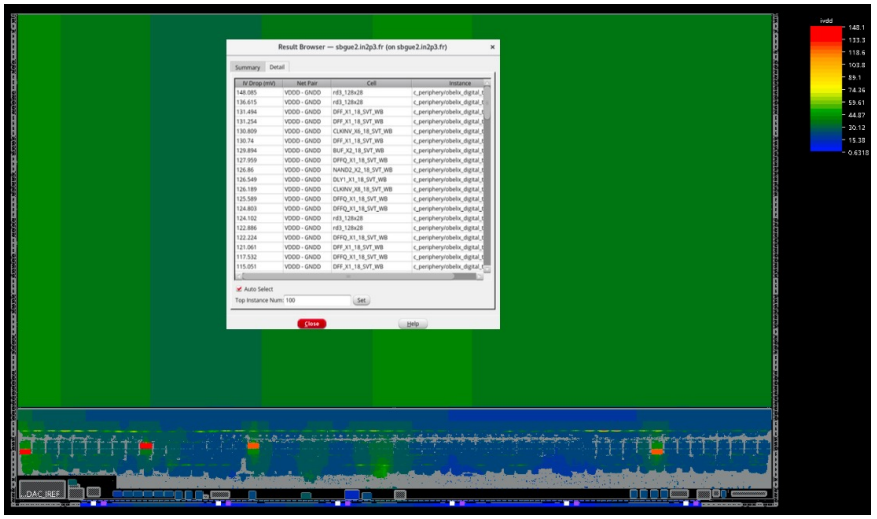




IR-Drop simulation

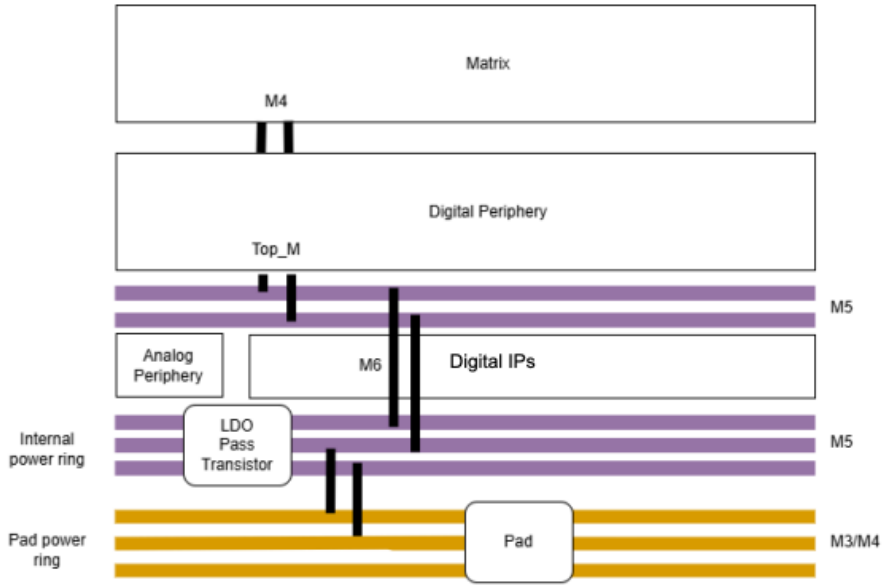


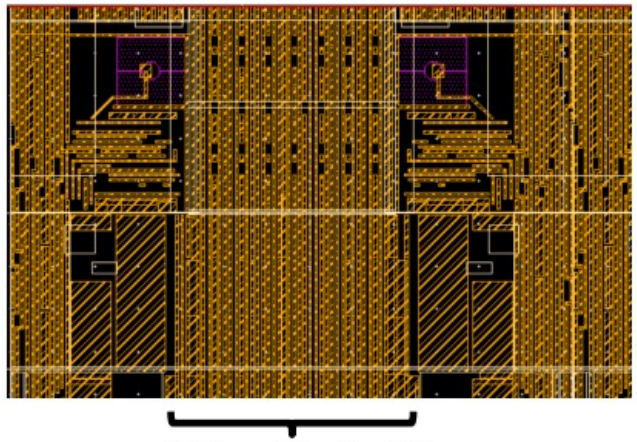




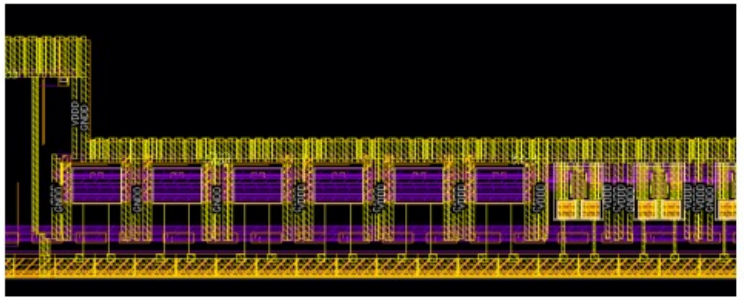
1 MHz/cm^2

Power distribution & on chip regulation





Digital power & Signal from Digital Periphery to Matrix (M4)



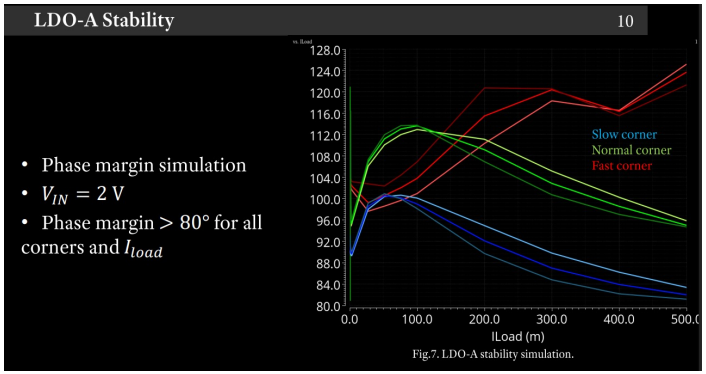
- Digital power distribution:
  - 112 Pass-transistors spreads over digital section
  - LDO control is implemented
  - Six pad groups (VIN, VDD and GND) for unregulated power and external coupling
  - Pixel matrix's digital power is supplied from the bottom and share the Digital Periphery's power domain

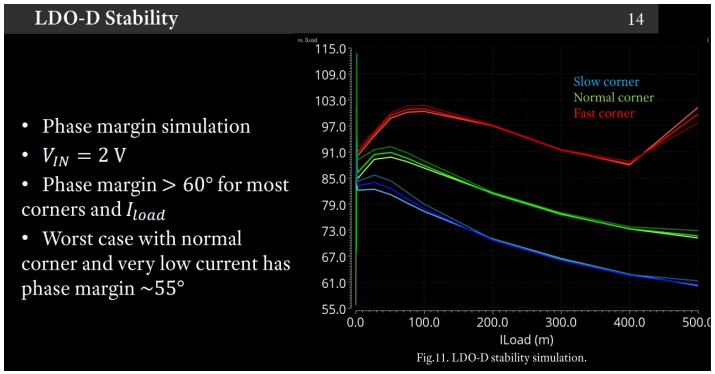
LDO performance simulations

LDO	Pre-Regulator	VPC	VDDA	VDDD
Input voltage	2 V – 3 V	Idem	Idem	Idem
Output voltage	1.62 V – 1.98 V	1.4 V – 1.8 V	1.62 V – 1.98 V	1.62 V – 1.98 V
Load current	0 – 50 mA	0 – 50 mA	0 – 500 mA	0 – 500 mA
Load regulation	20 mV@50 mA	Idem	20 mV@500 mA	20 mV@500 mA
Line regulation	20 mV@1 V	Idem	Idem	Idem
Load & Line transient	<180 mV	Idem	Idem	Idem
Coupling capacitance	2.2 µF	Idem	Idem	Idem
Temperature range	0 – 60°C	Idem	Idem	Idem

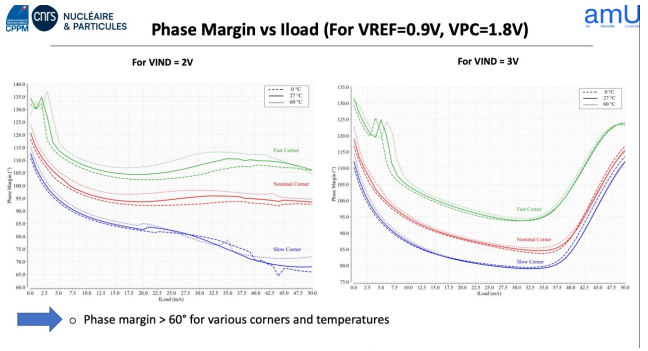
- All LDOs meet specifications.
- PM > 55° for chip-level extraction, corner & temperature variations.
- Start-up conditions validated with full pad frame using 100µs, 1ms and 100ms input voltage ramp-up times.

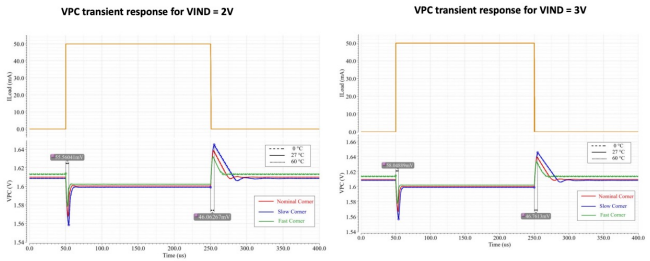
LDO performance simulations





Source: X.Yu, KEK, Obelix design review





Source: R.boudagga, CPPM, Obelix design review

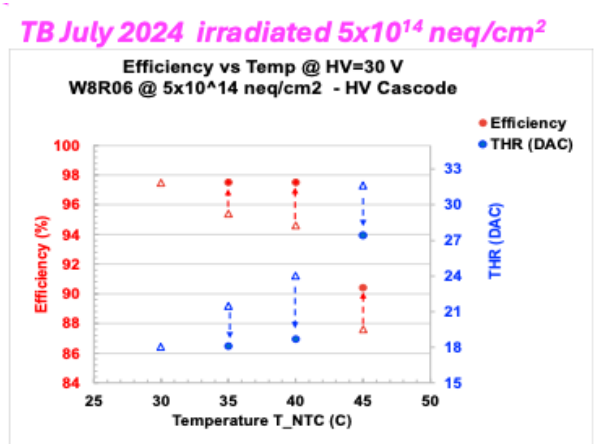
TJ-Monpix2 – Test results (beam test)

- Several beam test campaigns (DESY, 5 GeV electrons)
  - July 2022 : un-irradiated sensors & high threshold ~500 e-
  - July 2023: low threshold 250 – 300 e- & NIEL irrad chip $5x10^{14}$ neq/cm^2 with 24MeV protons tested at room temperature
  - July 2024: 2 new irradiated chips NIEL $5x10^{14}$ neq/cm^2 & TID 100 Mrad & high temperature (T_{NTC}=30-45°C)
  - March 2025: several NIEL fluences & more Temperature explored

ampli	coupling	Efficiency (%)
Normal	DC	99.99
Cascode	DC	99.79
Normal	AC (HV)	99.13
Cascode	AC (HV)	98.11

NIEL irrad chip $5x10^{14}$ neq/cm^2 at room temperature

Higher THR & lower efficientcy when increasing temperature

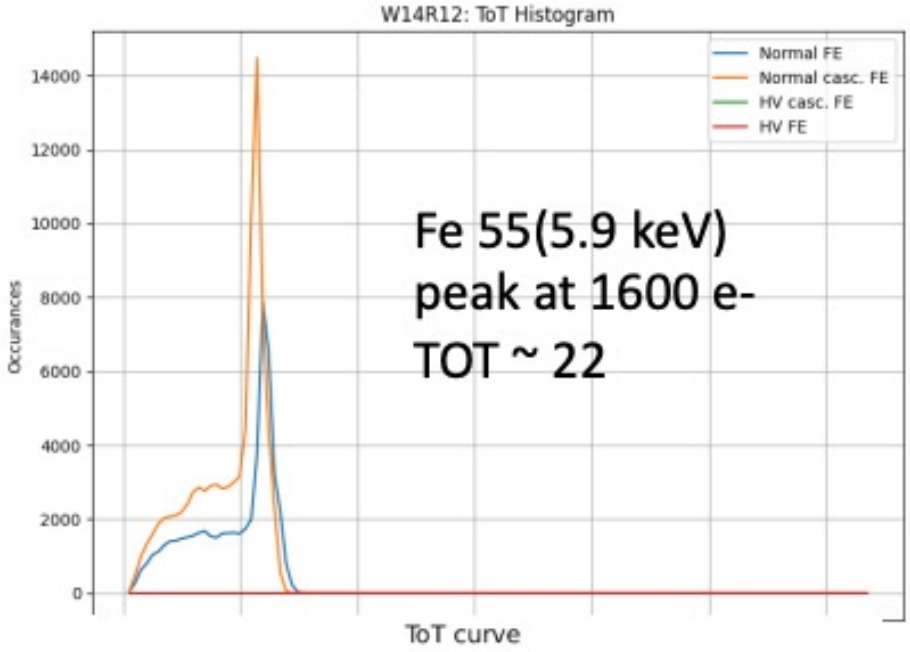


VTX Upgrade

Layer	1	2	3	4	5
Radius (mm)	14.1	22.1	82.5/89	108/114.5	135.5/140
No of Ladder	6	10	36	48	60
No of Sensor/Ladder	4	4	16	20	24
Mat. Budget(% Xo)	0.3	0.3	0.6	0.6	0.6
Expected hit rate(MHz/cm^2)	34	16	0.76	0.41	0.27

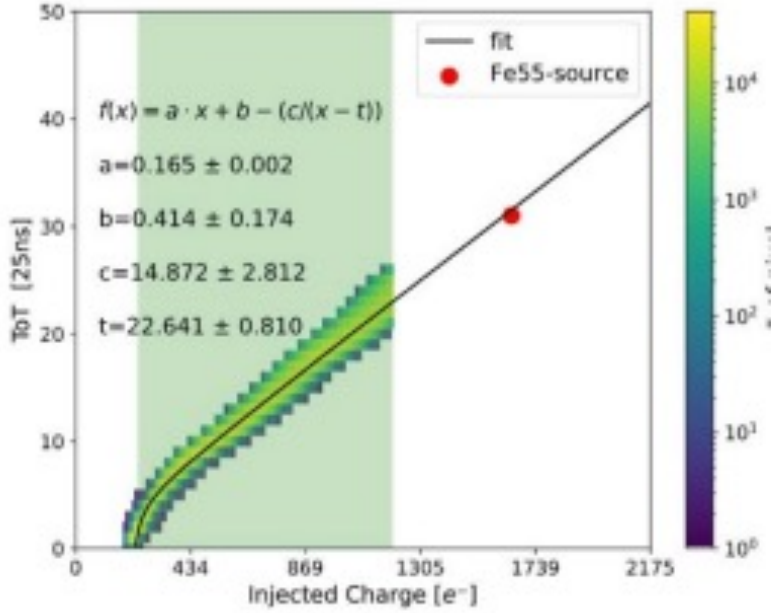
TJ-Monpix2 – Test results (lab mesurement)

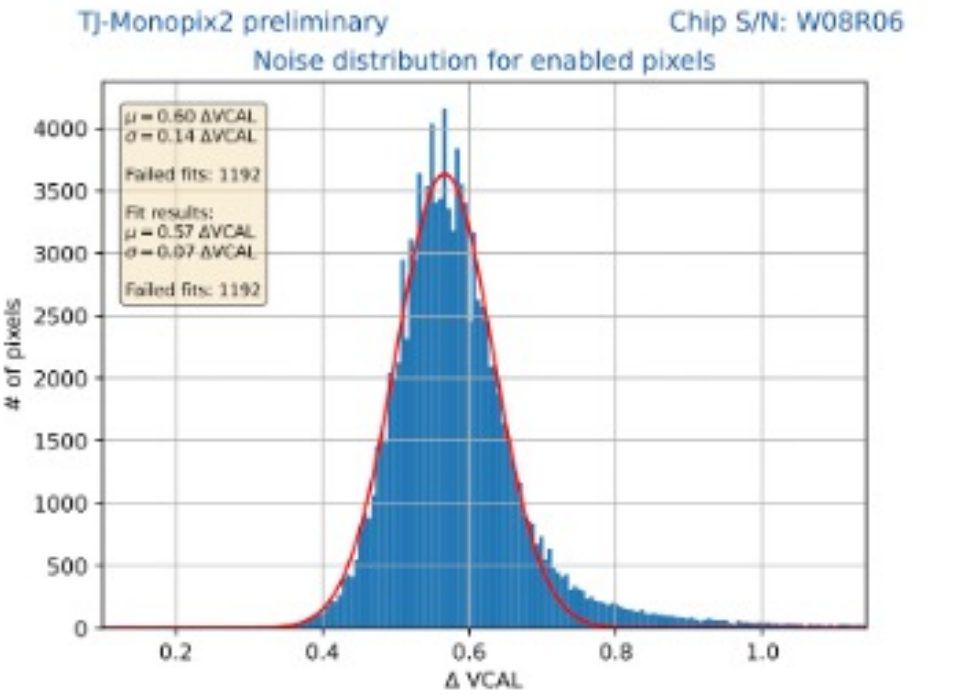
- Threshold/noise (un-irradiated chips)
  - Stable operation down to THR~ 250 e- (MIP signal in 30 µm Si MPV ~2000 e-)
  - THR dispersion ~8 e- after THR tuning
  - Noise ~6 e-



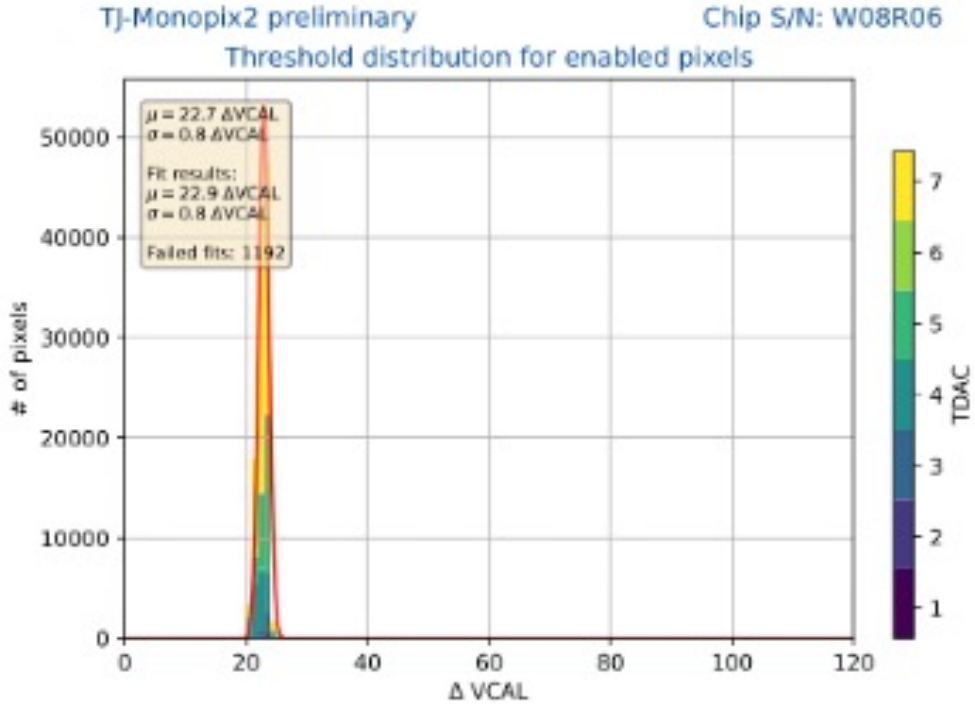
- ToT calibration with ^{55}Fe source
  - DC = 9 e- /DAC
  - AC = 18 e- /DAC

➔ Match with designed DAC resolution & injection capacitor

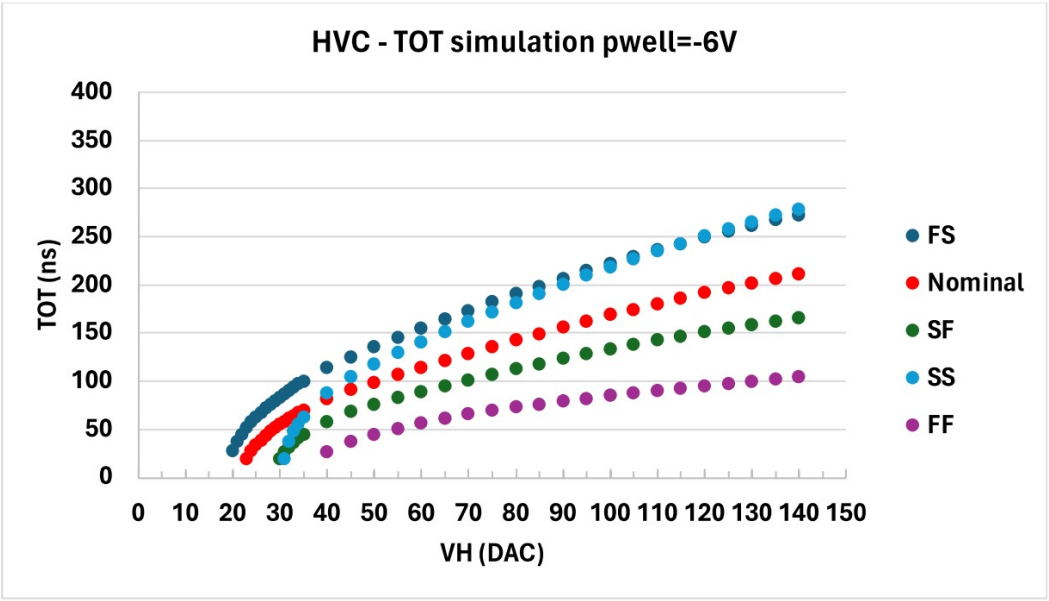


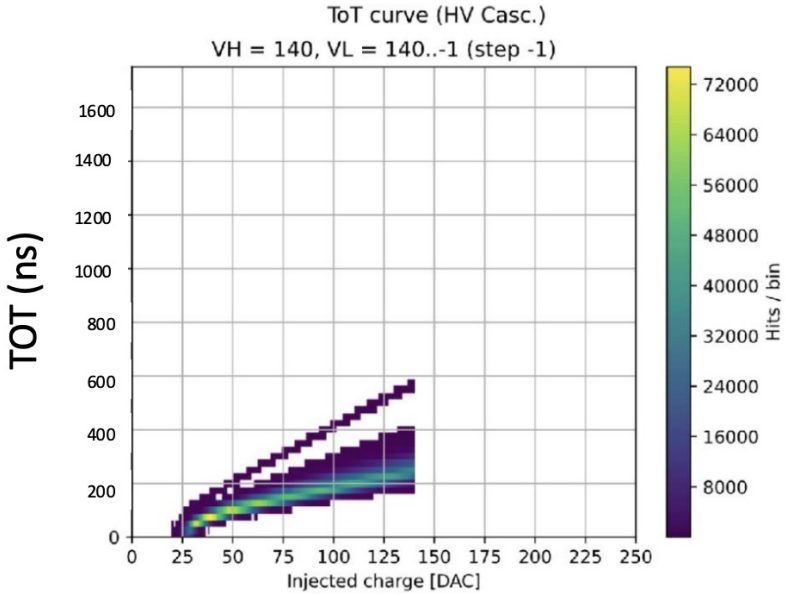


(c) Noise distribution



(b) Threshold distribution


HVC - TOT simulation pwell=-6V
TOT (ns)
VH (DAC)
FS
Nominal
SF
SS
FF


ToT curve (HV Casc.)
VH = 140, VL = 140..-1 (step -1)
TOT (ns)
Injected charge [DAC]
Hits / bin

20