ALCOR: A MIXED-SIGNAL ASIC FOR THE DRICH DETECTOR OF THE EPIC EXPERIMENT AT THE EIC

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Outline

- ePIC-dRICH detector at EIC
- ALCOR architecture overview
- Main results from ALCOR-32
- ALCOR-64: design upgrades and BGA packaging
- Summary

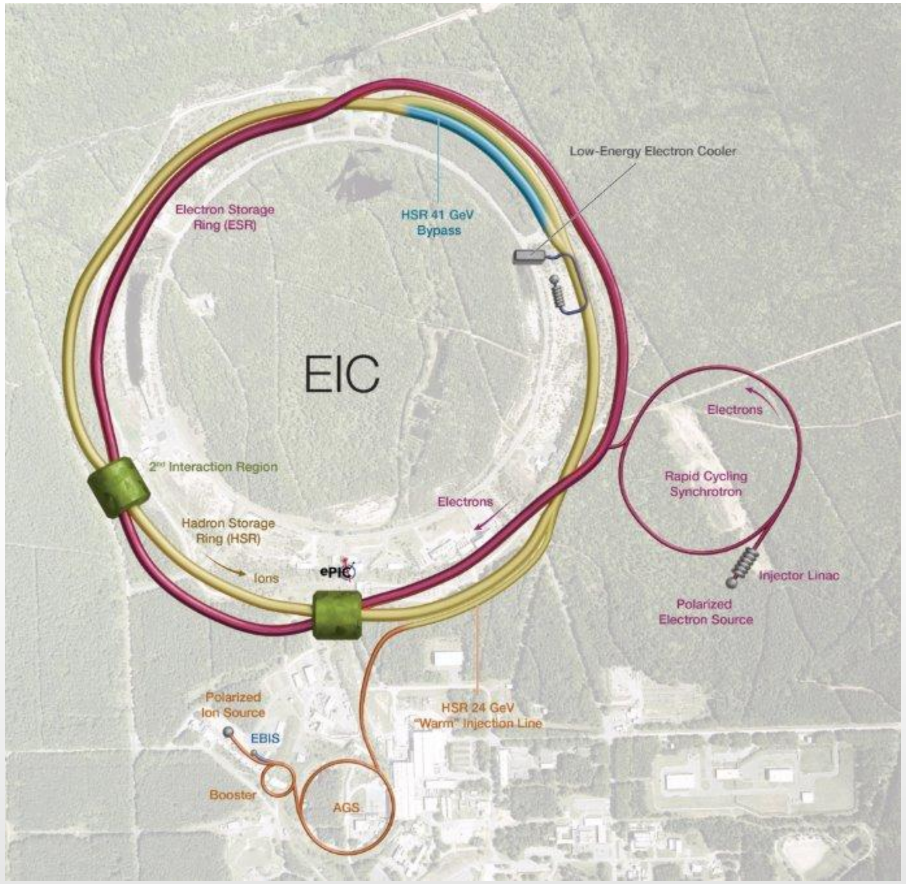
The ePIC experiment at the EIC

Electron-Ion Collider (EIC) at BNL: major US project in nuclear physics, one of the most important future facilities in the field

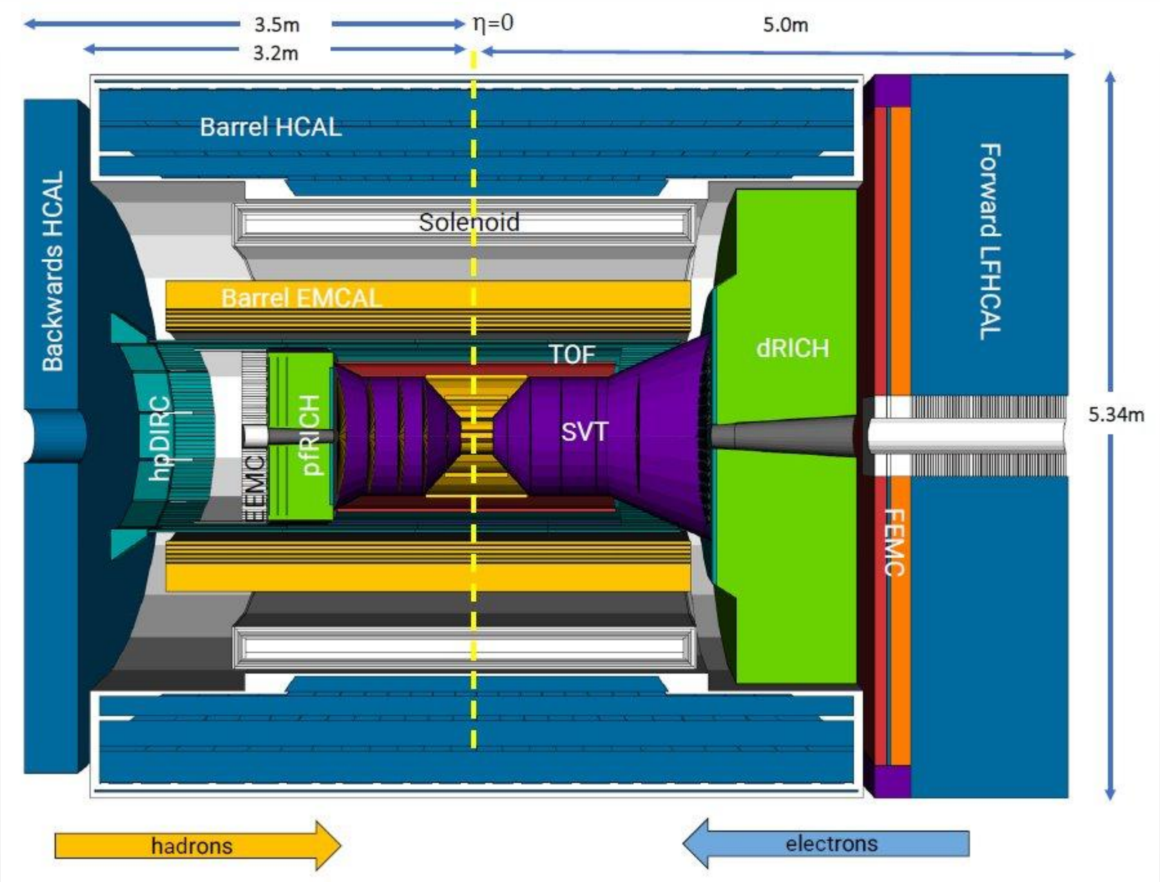
- Collision of **e$^-$** and **ions** (from proton to uranium)
- Center-of-mass energy from **20** to **140 GeV**
- Highly **polarised beams**: ~70%
- High luminosity: **10^{33} cm^{-2}s^{-1}**
- One approved experiment: **ePIC**
- Start of operations in the early 2030s

Physics goals:

- Precise measurements in non-perturbative QCD
- Origin of mass & spin of the nucleons
- 3D imaging of the nuclear structure



The ePIC experiment at the EIC



Tracking

- 1.7 T magnet
- Si MAPS Tracker
- MPGDs (μRWELL / MicroMegas)

PID

- high performance DIRC
- proximity focusing RICH
- **dual-radiator RICH**
- TOF (AC-LGAD)

Calorimetry

- barrel: imaging EMCal
- backward: $PbWO_4$ EMCal
- forward: finely segmented
- outer barrel + backward HCal

The dual-radiator RICH (dRICH) for forward PID

Compact and cost-effective solution for broad momentum coverage (3-50 GeV/c) at forward rapidity (1.5-3.5)

- **Radiators**: aerogel (n ~ 1.026) and C_2F_6 (n ~ 1.00086)
- **Mirrors**: large outward-reflecting, **6 sectors**
- **Photosensors**: **3x3 mm^2 SiPMs, 0.5 m^2 per sector**, in **1 T magnetic field** and radioactive environment (10^{10}-10^{11} n_{eq}/cm^2 total exposure 10 y operation)

- **SiPM** based readout

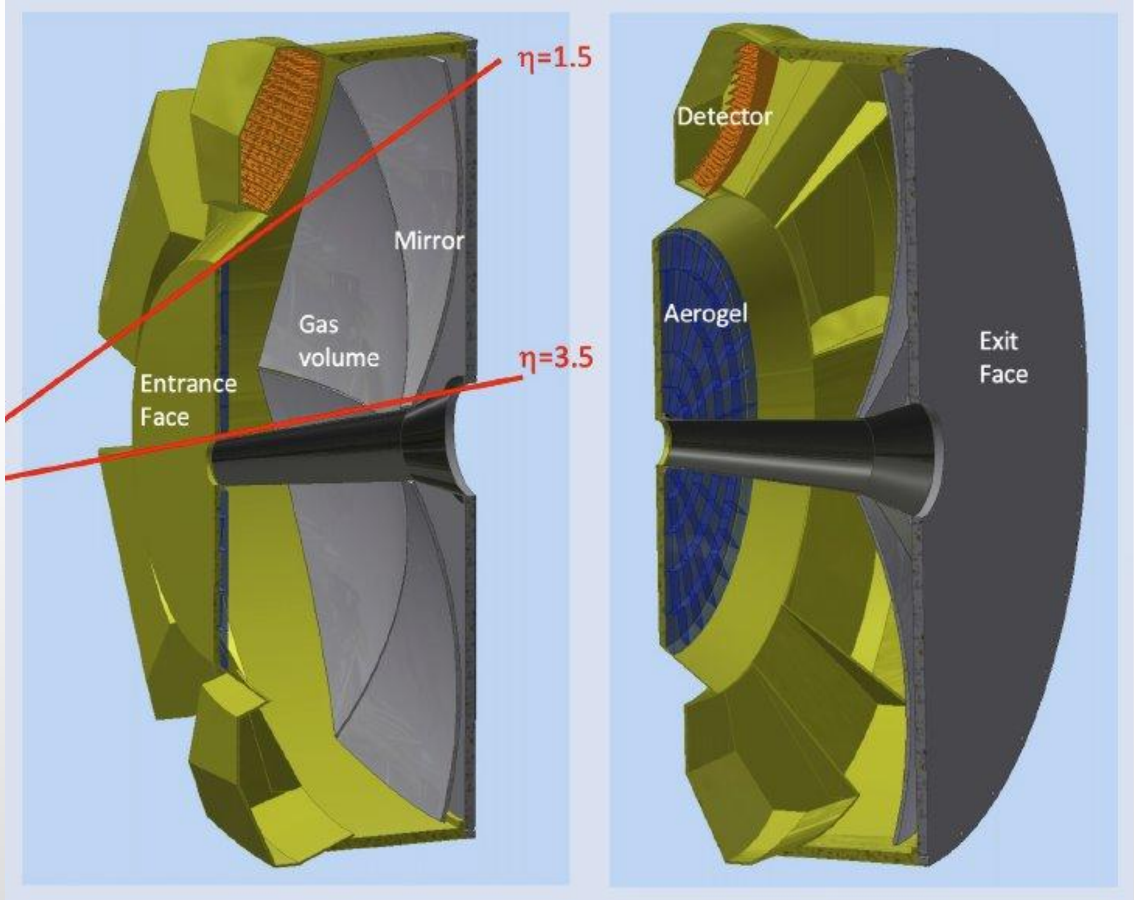
✓ **Single Photon** sensitivity ~ 30 phs per Cherenkov event

✓ Good **timing performance** < 100 ps

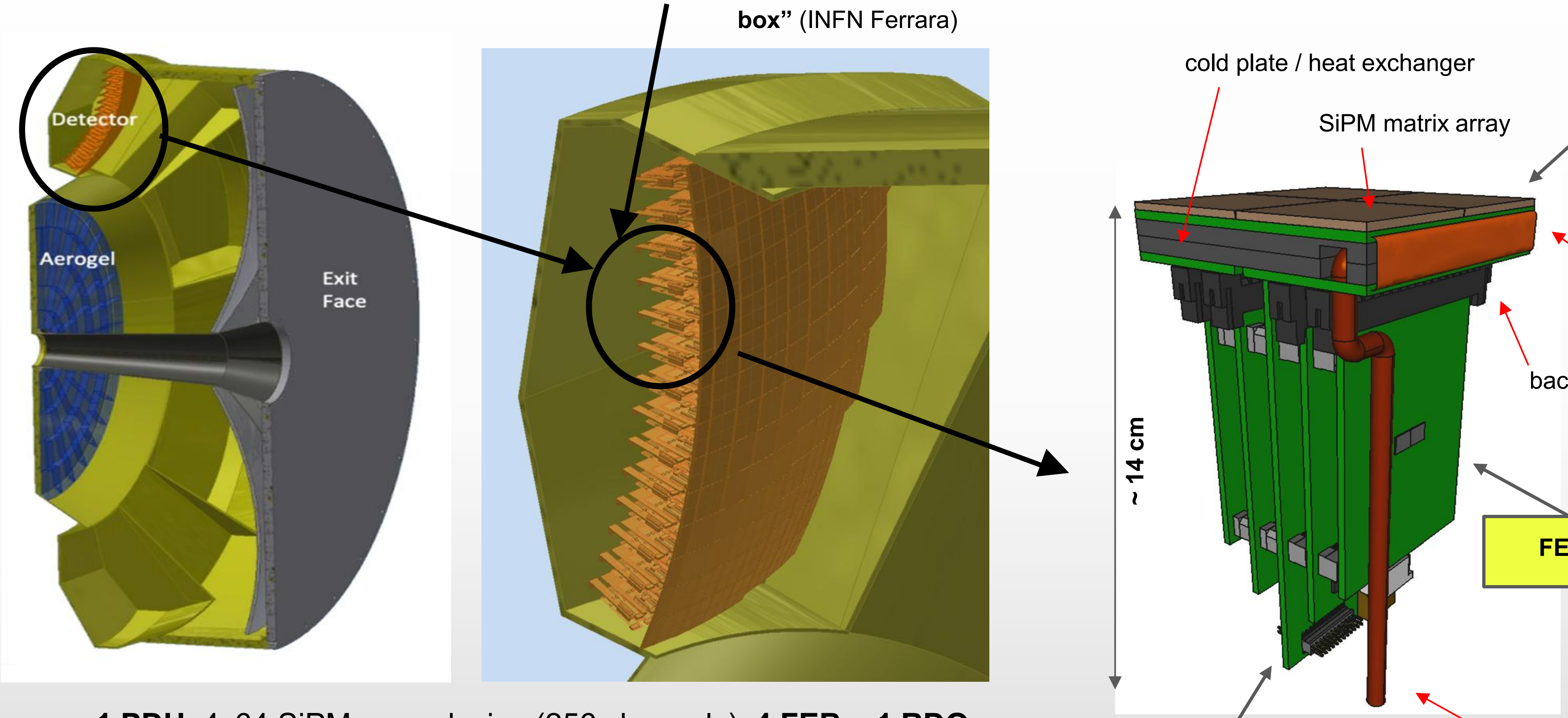
✓ **Cheap** and **insensitive to magnetic fields**

✗ **High DCR** and **high radiation sensitivity** requires:

  - cooling → **T = -30/-40°C**
  - annealing → **in-situ temperature cycles**
  - timing → **fast electronics**



dRICH electronics overview



PDUs inside dRICH sector **“detector box”** (INFN Ferrara)

cold plate / heat exchanger

SiPM matrix array

SiPM sensors

(INFN Bologna)

flex PCB

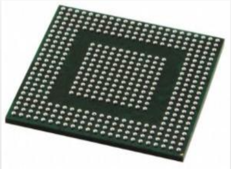
back-side connectors

FEB

RDO

(INFN Bologna)

connections to services
HV, LV, DAQ, …



ALCOR ASIC
(64-channel, BGA)

- **1 PDU**: 4x64 SiPM array device (256 channels), **4 FEBs, 1 RDO**
- **1 ALCOR** (64 channels) per **FEB:** 8x8 SiPM matrix readout
- 6 sectors: 208 PDUs/sector → 1248 PDUs for full dRICH readout
- **4992 FEBs → 4992 ALCOR-64**
- **319488** readout **channels**

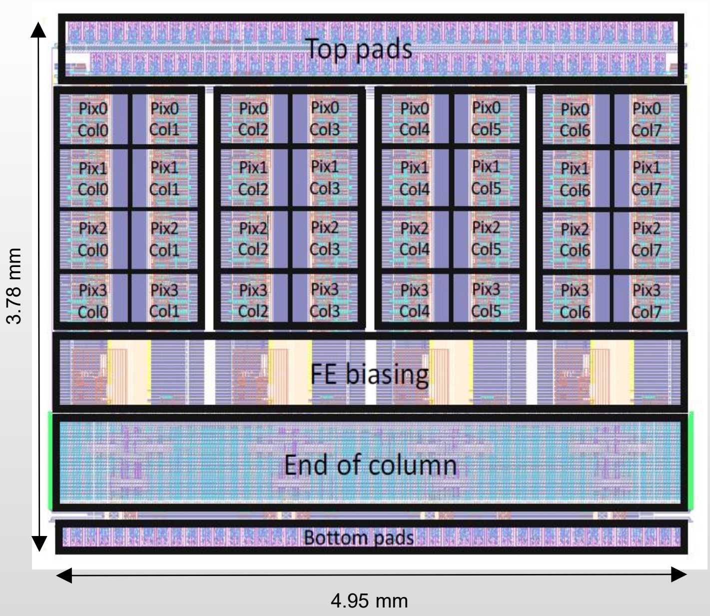
ALCOR: A Low power Chip for Optical sensor Readout

Main requirements for the ePIC dRICH detector

- ➢ Provide **single-photon time tagging** of signals coming from SiPM sensors
- ➢ Cope with **SiPM DCR: 300 kHz/channel** (at max SiPM radiation damage)

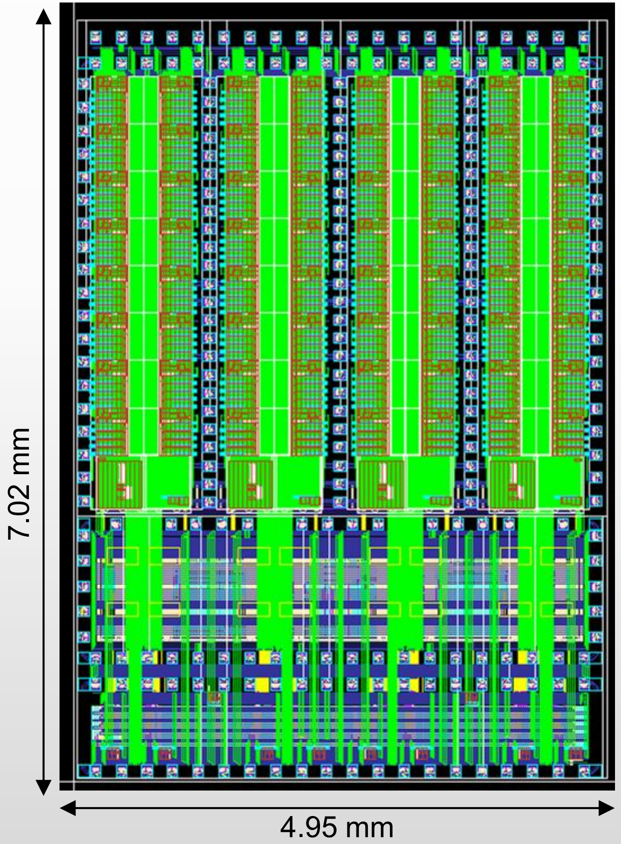
- **32** or **64-pixel matrix** mixed-signal ASIC with on-chip signal amplification, conditioning and digitization
- **ToA** + **ToT** or **Slew-Rate** measurements for **time walk compensation**
- **Triggerless readout**, fully digital output
- Power consumption **~12 mW/channel**
- **110 nm** CMOS technology

ALCOR-32



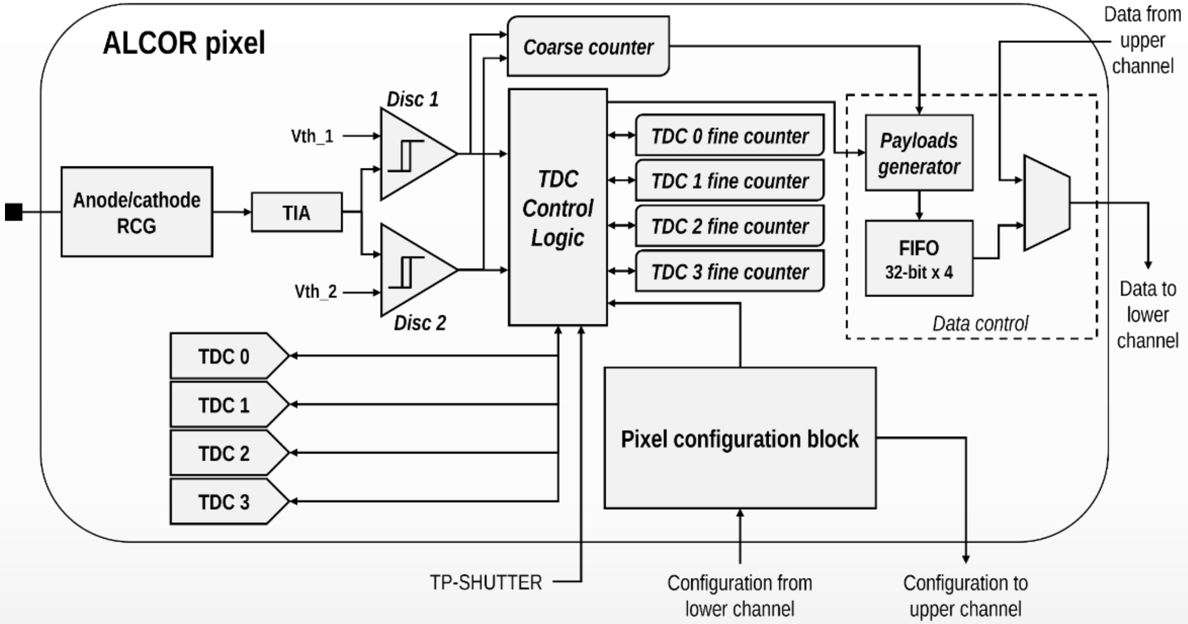
- ALCORv1: Developed for the DarkSide Experiment for SiPM readout at cryogenic temperature
- **32-channel**, **wire-bond**
- **320 MHz clock** frequency
- 4 LVDS 320 MHz DDR Tx links
- Extensively used within the ePIC-dRICH Collaboration **since 2021** and validated with multiple **successful beam tests** (ALCORv2)

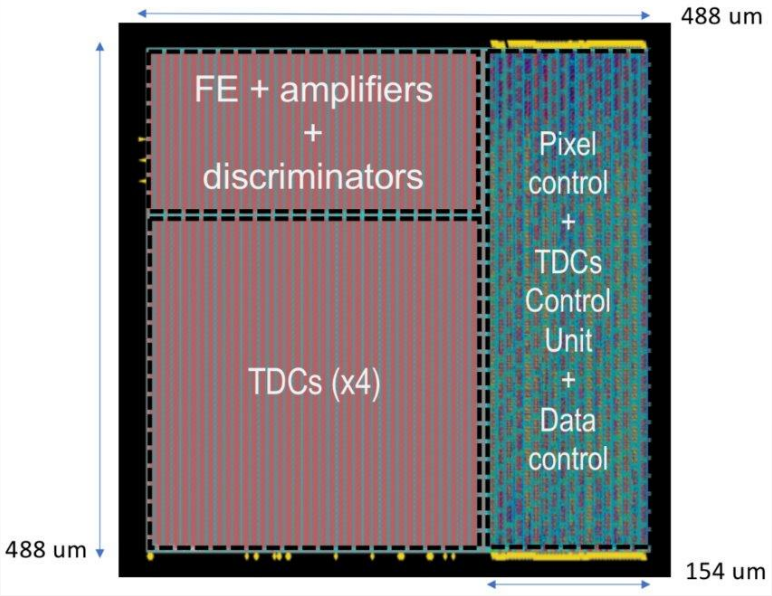
ALCOR-64



- New version (ALCORv3) with specific EIC-driven features
- **64-channel, FC-BGA** package
- Increased amplifier bandwidth to improve time resolution
- Hardware **shutter** to inhibit events digitization (asynchronous with ns time window) and **suppress out-of-time SiPM DCR hits**
- **394 MHz clock** frequency
- 8 LVDS 394 MHz DDR Tx links

ALCOR pixel architecture





pixel size: 440 x 440 μm²

- **Dual-polarity RCG input stage** current conveyor (**Z_{in}= 10-20 Ω**) + **TIA** with 4 gain settings
- **2 leading edge discriminators** with independent (and per pixel) threshold settings (6-bit DAC) → **V_{th} = 0.5 p.e.**
- **4 TDCs** based on **analogue interpolation** with **20-40 ps** time-bin (at 394 MHz clock frequency)
- Pixel control logic handles TDC operation, pixel configuration, operating mode and data transmission
- Test pulse injection into the analog FE or TDC + **Shutter** to inhibit events digitization and suppress out-of-time SiPM DCR hits

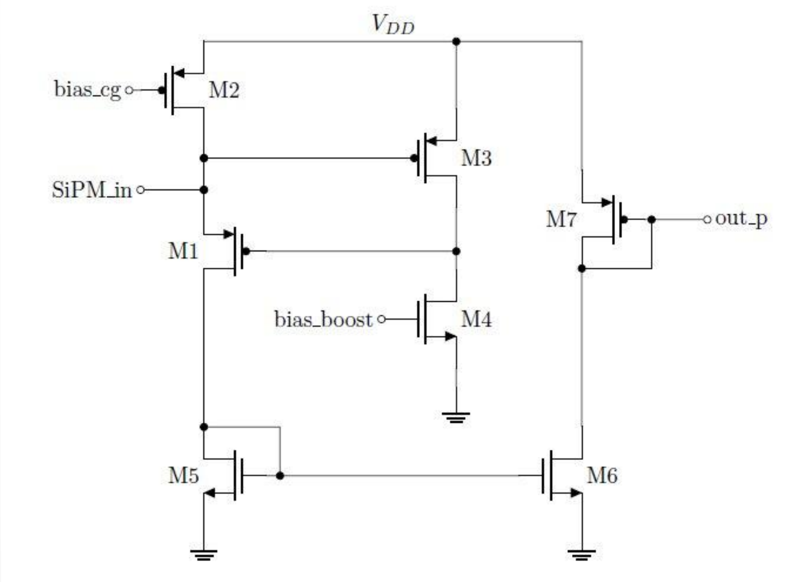
ALCOR Front-End

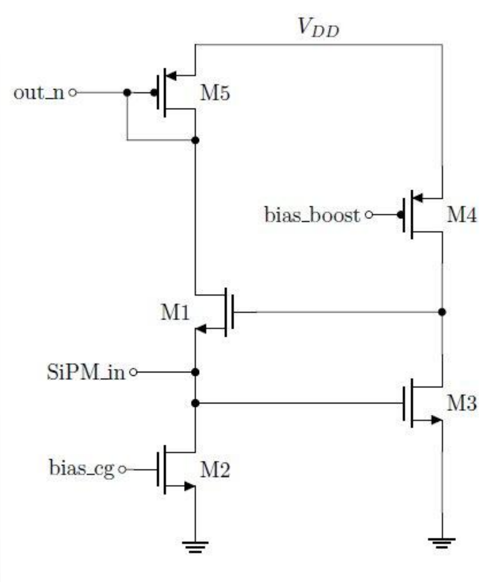
Input stage

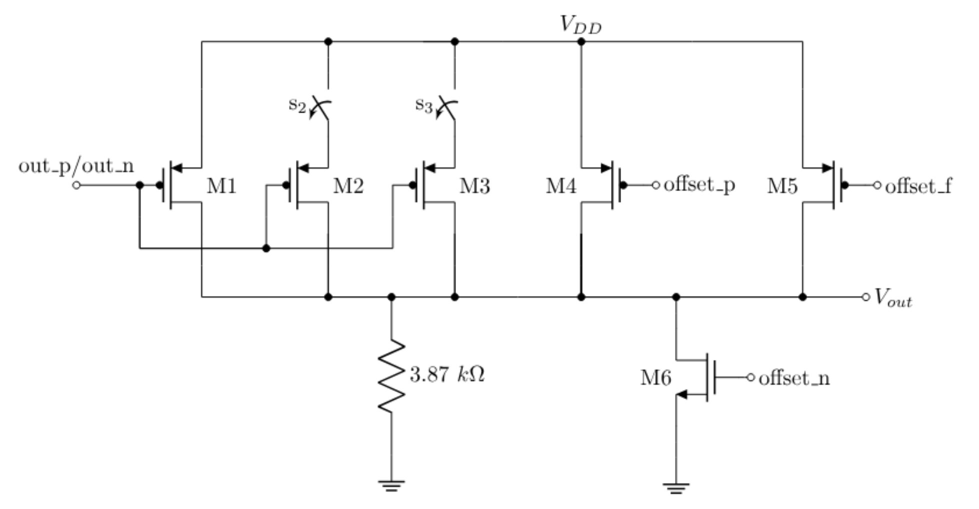
- Dual-polarity RCG current conveyor
- Programmable bias currents: CG (30-100 µA) and BOOST (1-4 mA)
- Z_{in} ~ 10-20 Ω

Output stage

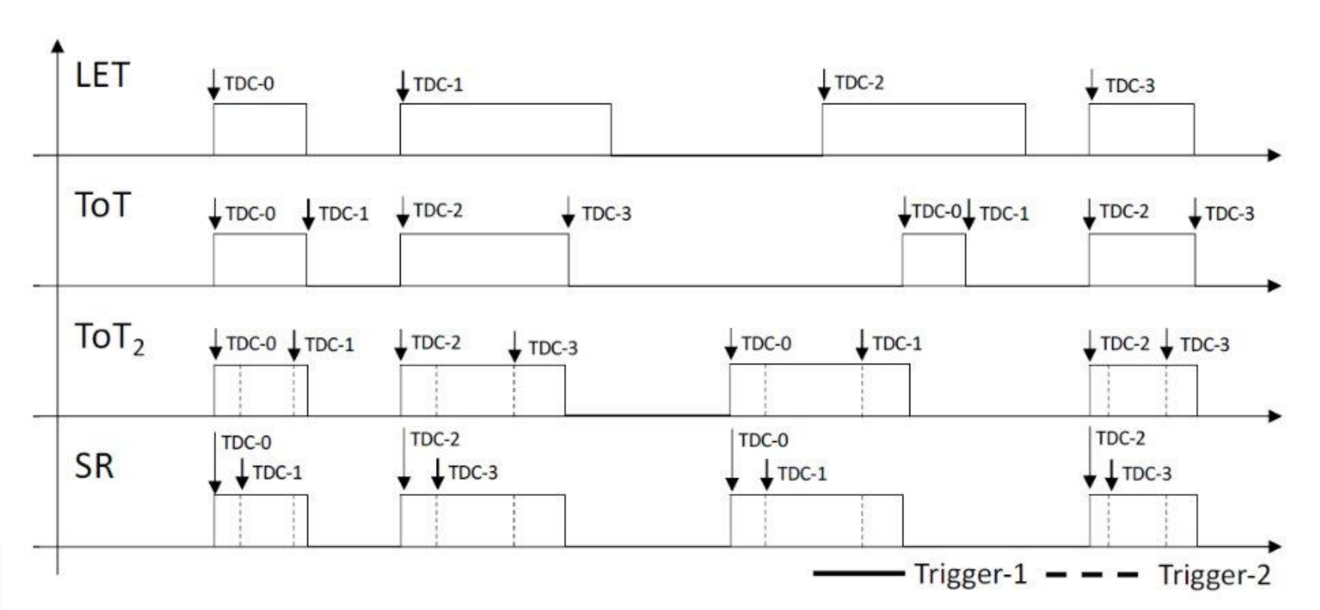
- TIA gain: 3.87 kΩ
- 4 gain settings: 1/3, 4/3, 7/3 and 10/3
- DC coupled: baseline compensation based on gain and CG bias current settings + fine offset adjustment (3-bit)







ALCOR pixel operating modes



4 operating modes:

- **LET**: leading edge measurement
- **ToT**: Time-over-Threshold measurement using the first discriminator for both edges
- **ToT2**: Time-over-Threshold measurement using both discriminators
- **SR**: slew-rate measurement

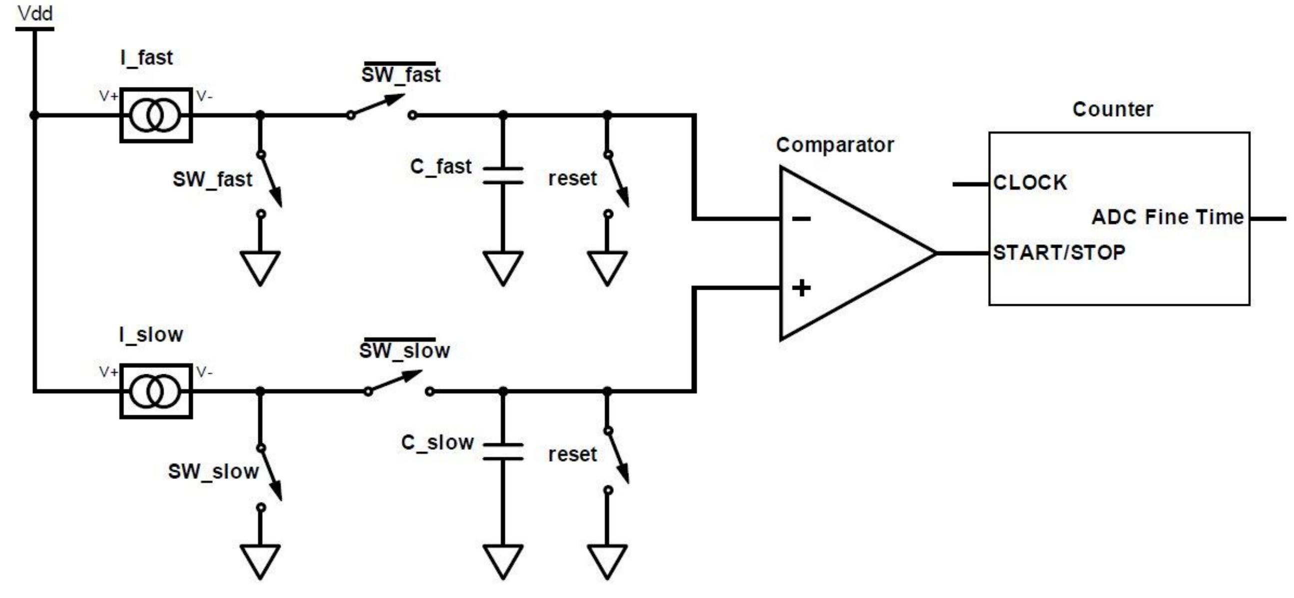
Each mode can be set to:

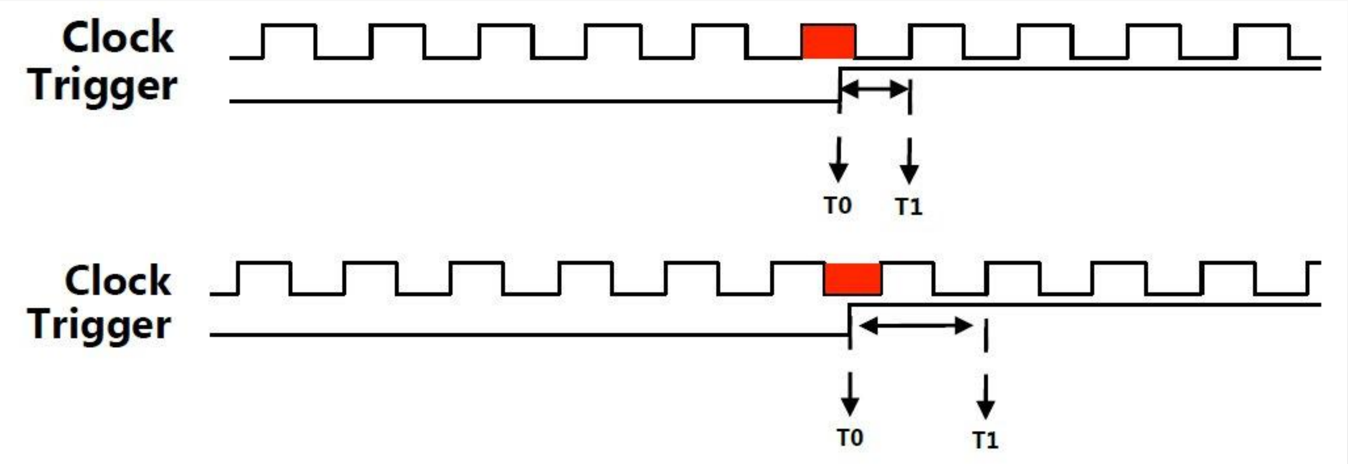
- **FE**: normal operation mode
- **FE_TP**: send test-pulse to analogue front-end
- **TDC_TP**: send test-pulse to pixel control logic to test and calibrate TDCs (bypass front-end)

Each pixel can also be disabled

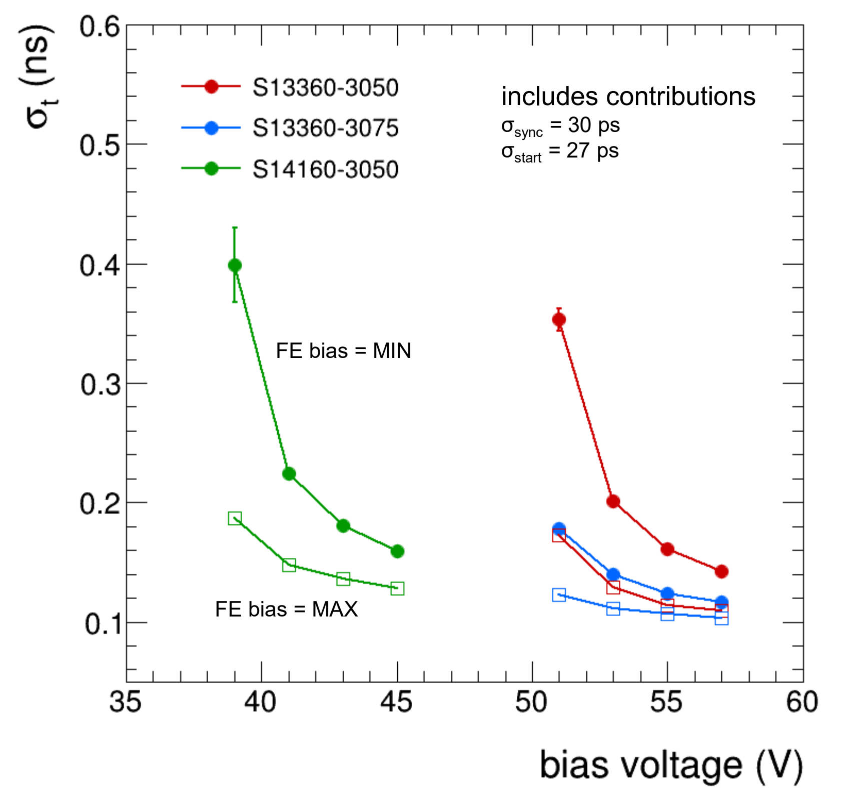
Time to Digital Conversion

- Coarse time: 15-bit clock counter
- Time conversion performed by **TDC** based on **analogue interpolation** (9-bit fine time):
  - ***fast ramp***: constant current to charge C_{fast} → measure phase between event trigger and clock
  - ***slow ramp***: smaller constant current to charge C_{slow} → counts clock cycles until C_{slow} and C_{fast} are equal
- I.F. 64 or 128 → **LSB = 20-40 ps** @394 MHz
- Measured time interval: 0.5 - 1.5 clk period
- TDC conversion time: [170, 500] ns
- 4 TDCs per pixel for **event derandomization**

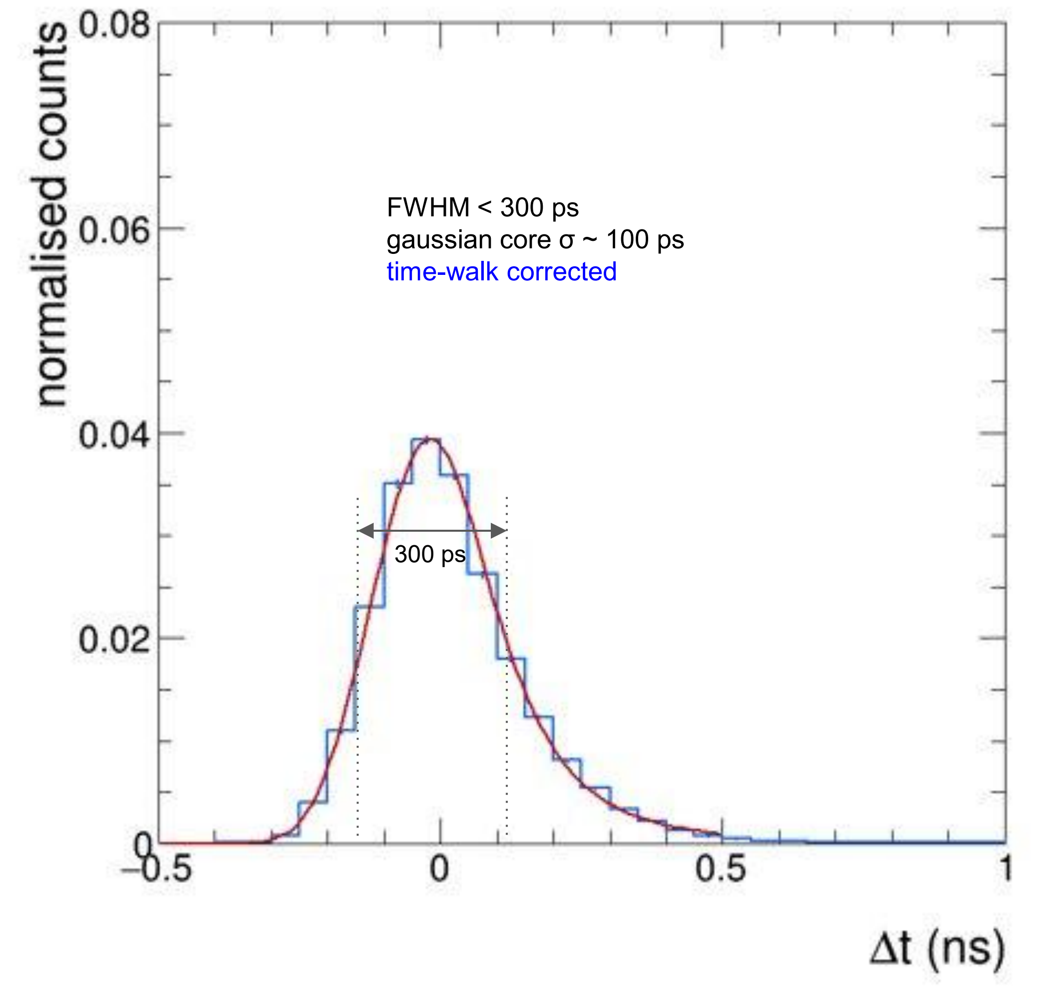




ALCOR-32 Laser timing measurements



- ➔ Better time resolution with **75 μm SPADs**
- ➔ Comfortably below **σ_t = 150 ps** also at low Vbias

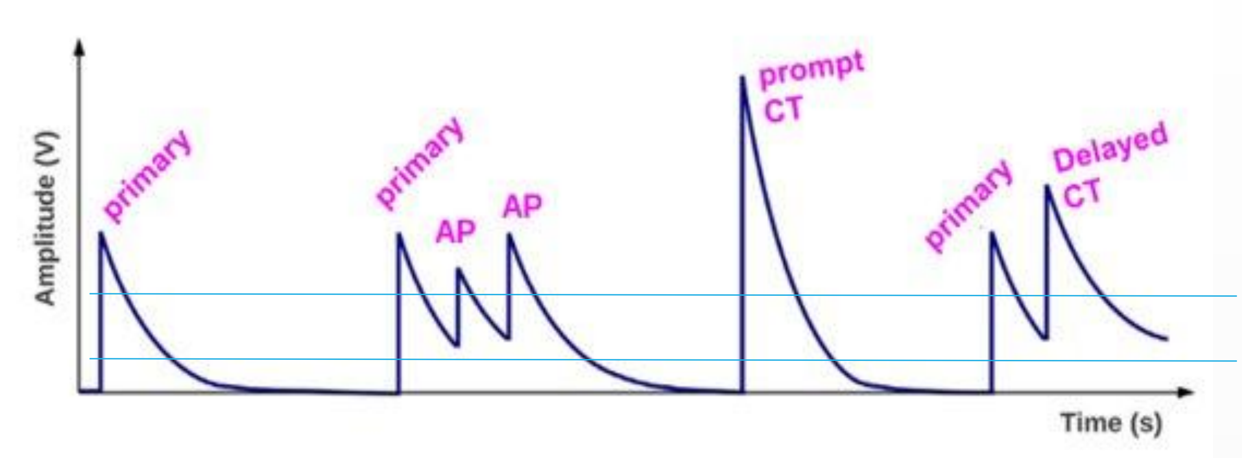


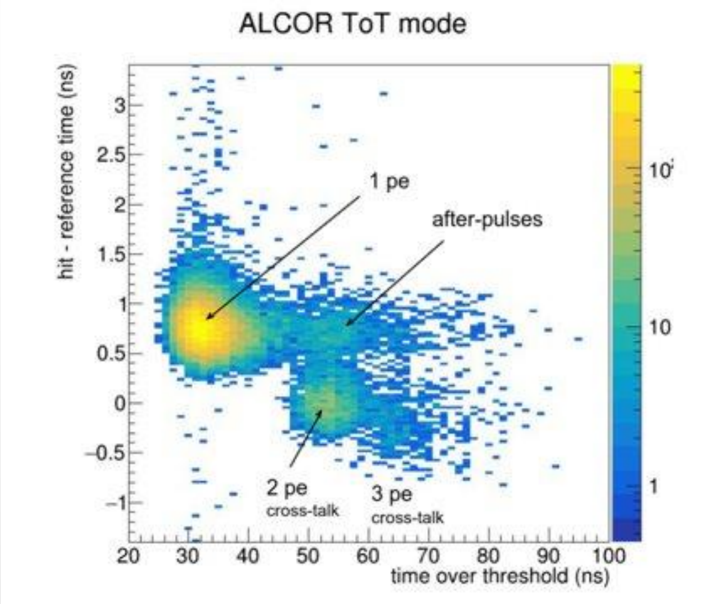
includes contribution for laser-ALCOR synchronization (σ_{sync} = 30 ps) and reference time resolution (σ_{start} = 27 ps)

Time walk correction

Time walk correction needed to improve overall time resolution

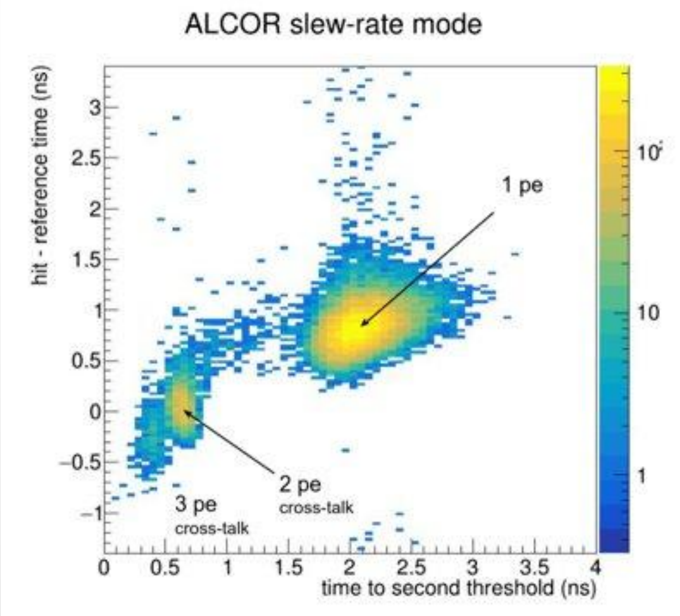
→ studies with laser setup using ***ToT*** and ***Slew Rate*** measurements



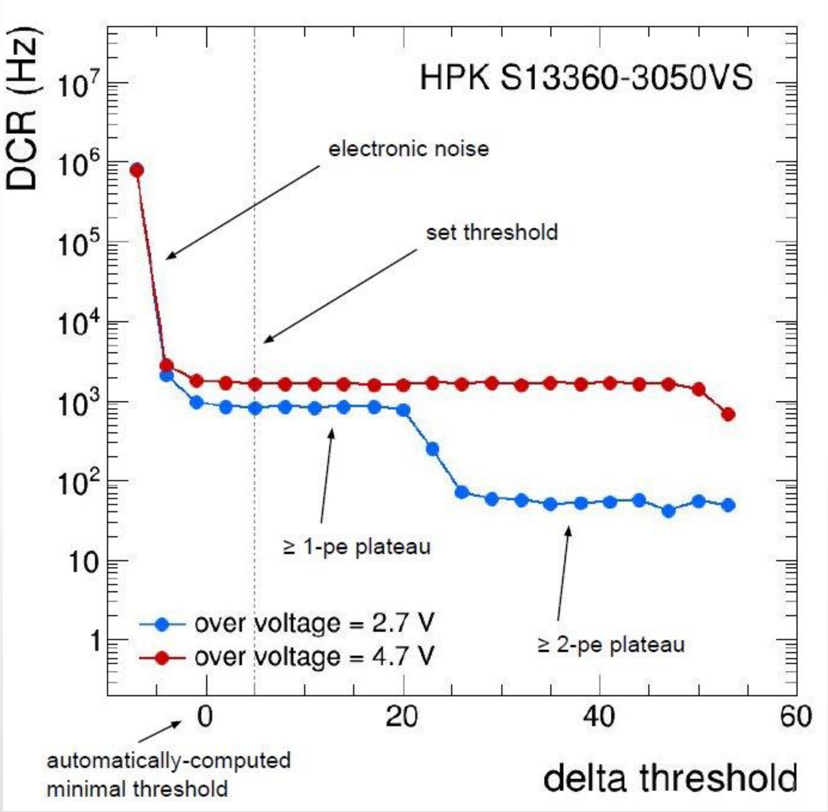

ALCOR ToT mode

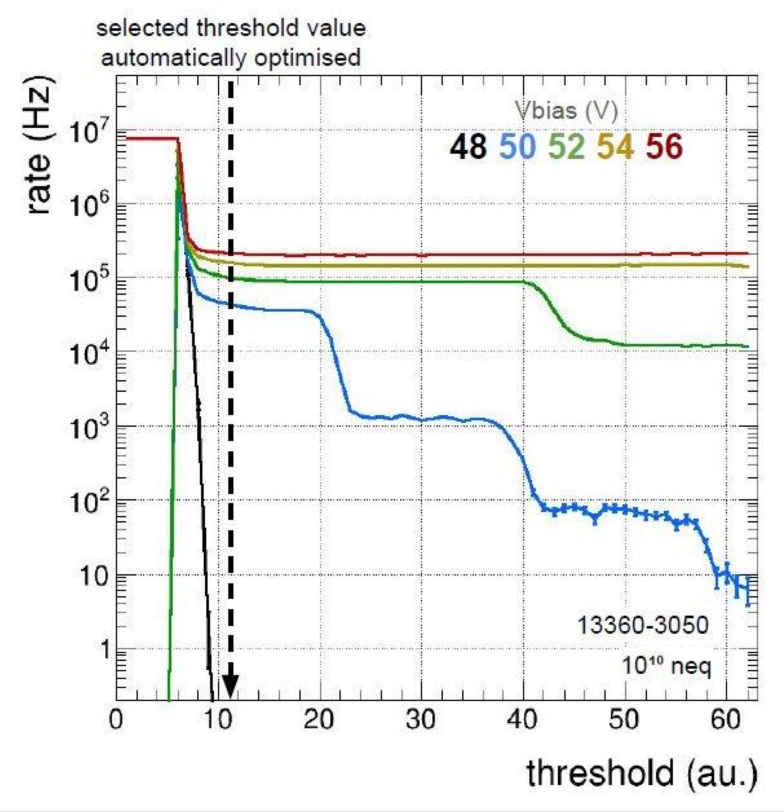
✗ ***ToT mode*** cannot distinguish between afterpulses (slow-rise time, large ToT) and cross-talk (fast rise-time, large ToT)

✓ ***SR mode*** provides better separation


ALCOR slew-rate mode

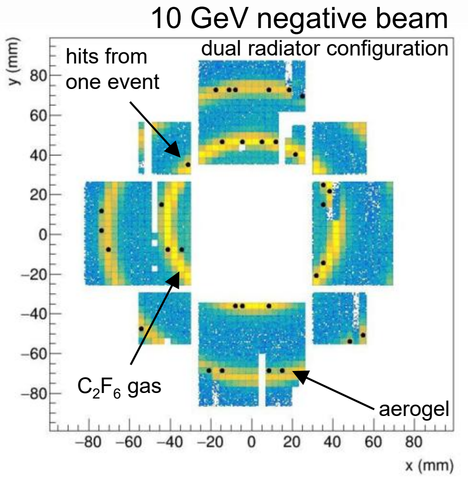
ALCOR-32 threshold scan

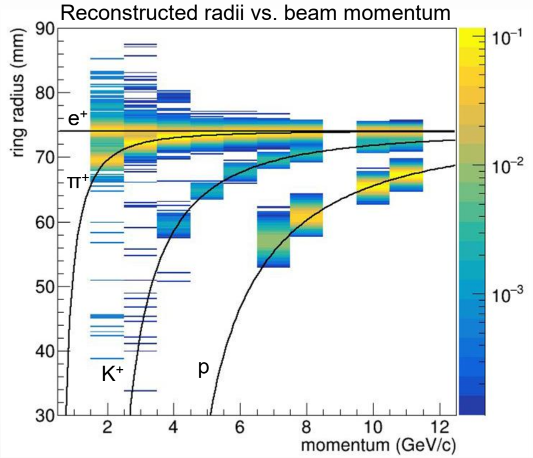




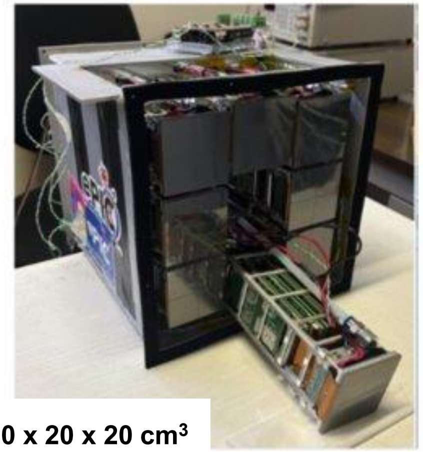
ALCOR-32 beam tests at CERN-PS

- Successful beam tests with prototype **dRICH** and **PDUs** (CERN-PS, October 2023, May 2024)
- HPK S13360-3050 and S13360-3075 (3x3 mm², T lower than -30°C)
- 32 FE-DUAL (64 ALCOR-32, **2048 channels**)
- DAQ: Xilinx Kintex 7 KC705

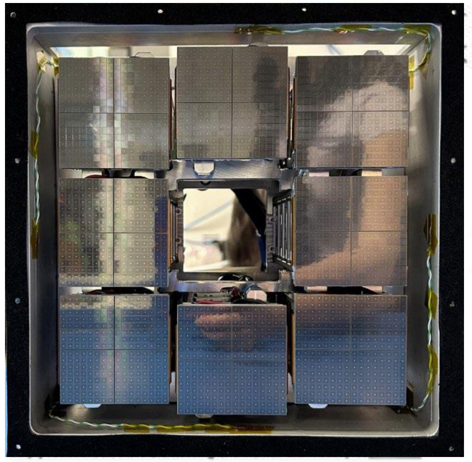




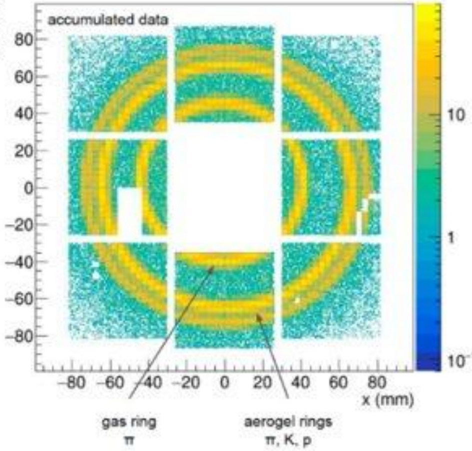
Realistic detector plane based on dRICH PDUs **Validated**

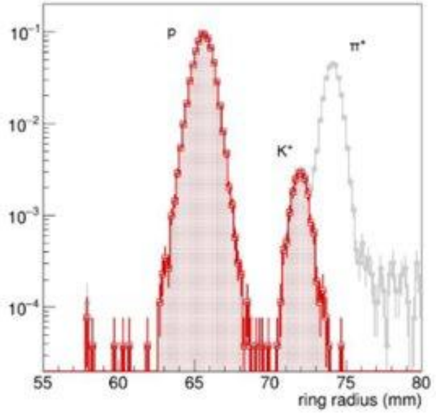


20 x 20 x 20 cm³



dRICH prototype got the expected performance and radiator interplay





Radiation tolerance

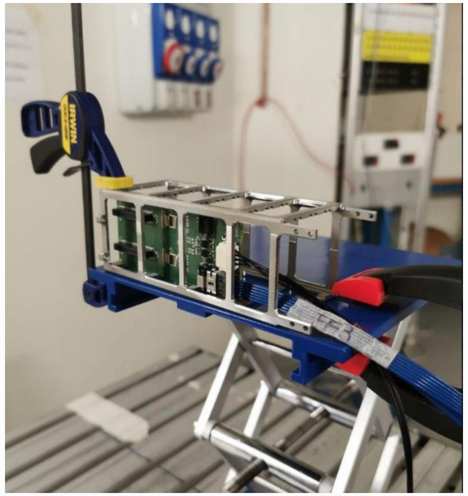
The dRICH-PDUs are in a moderately hostile radiation environment

- **Φ (p+n > 20 MeV) = 700 Hz/cm^2**
- **TID ≅ 2.3 krad (for 1000 fb^{-1})**

} safety factor of 5 included

➢ Irradiation tests campaign: **SEU/SEL** and **TID tests** at Centro of Proton-Therapy in Trento with **ALCOR-32** in **Jul 2024** and **Dec 2024**
  - Beam: 100 MeV proton
  - Intensity: 10 - 100 nA
  - Runs: typically 600 s
  - Fluence collected per run: 10^{11} - 10^{12} p/cm^2

- **Total fluence: 4.64 · 10^{12} p/cm^2** (Jul 2024) and **3.2 · 10^{12} p/cm^2** (Dec 2024)
- **Total TID: 436 krad**
- **Technology is sufficiently radiation tolerant** to be used in the ePIC dRICH environment
- **SEU rate is within the expected manageable levels**: in ALCOR-64 TMR SEU protection added also for periphery registers, Hamming code SEU protection for FSMs

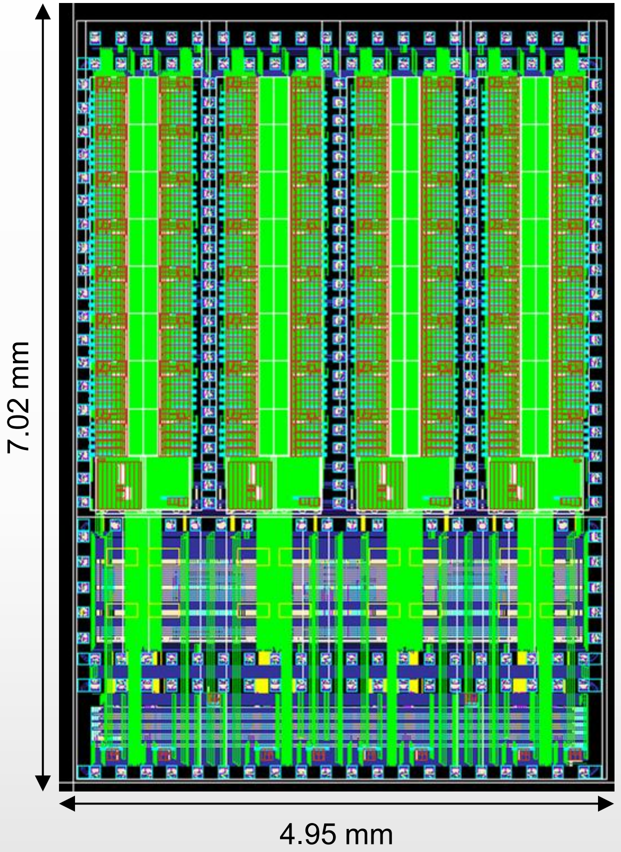


Detailed results presented at the 29th Jan 2025 dRICH Meeting: https://indico.bnl.gov/event/26313/

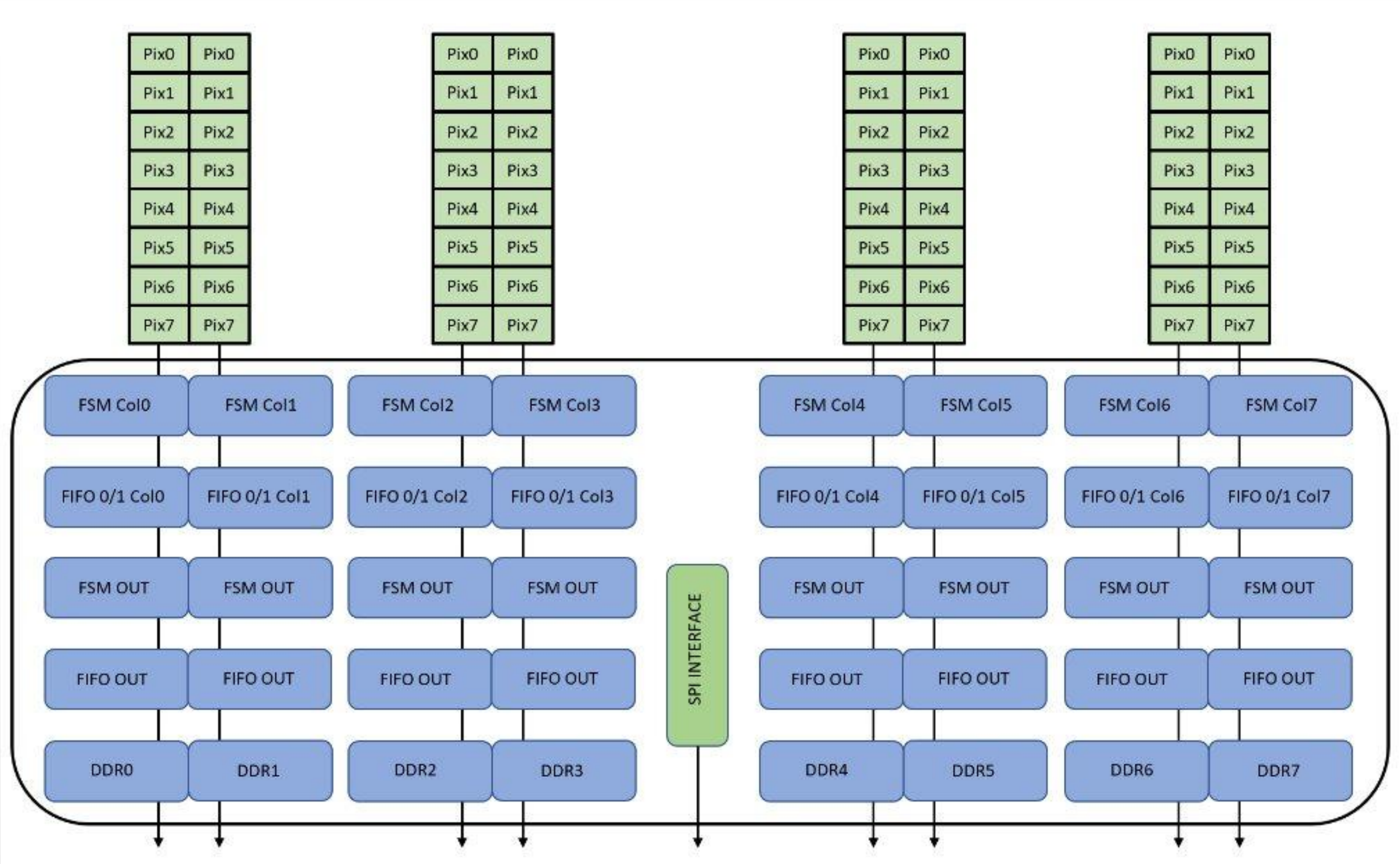
ALCOR-64 (V3)

- **64-pixel** matrix (8x8) mixed-signal ASIC
- Single-photon time tagging + **Time-over-Threshold** or **Slew-Rate** measurements for **time walk correction**
- On-chip **signal amplification**, **conditioning** and **digitization**, 32-bit event word
- **Shutter** to inhibit events digitization (asynchronous with ns time window) and **suppress out-of-time SiPM DCR hits**
- Trigger-less readout with fully digital output: **8 LVDS 394 MHz** DDR Tx links with 8b10b encoding
  - 2.4 Mhits per pixel in LE mode
  - 1.2 Mhits per pixel in TOT/SR mode
- "New orbit" command through reset signal:
  - Data encapsulated in frames every coarse counter rollover
  - New orbit forces a rollover condition (ALCOR rollover = 2^{15} clk cycles ≈ 83 μs, EIC orbit period ≈ 12.8 μs)

- Flip-chip **BGA package (no RDL was available)**
- **Improved SEU protection (TMR with autocorrection or Hamming encoding)**
- Power consumption **~12 mW/channel**
- **0.11 μm CMOS technology**



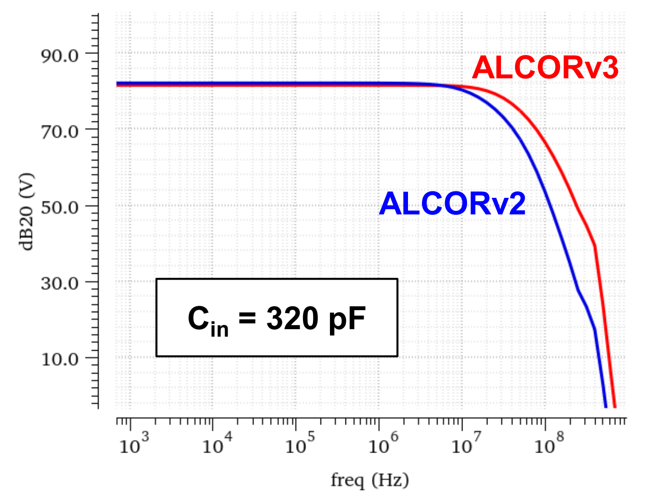
Block diagram

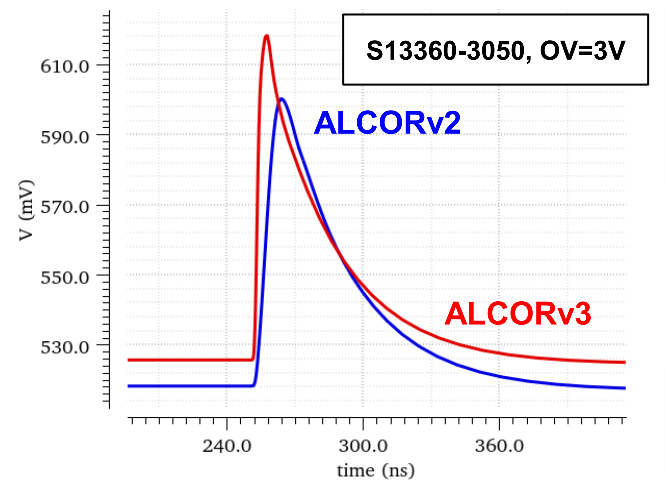


ALCOR-64 frontend

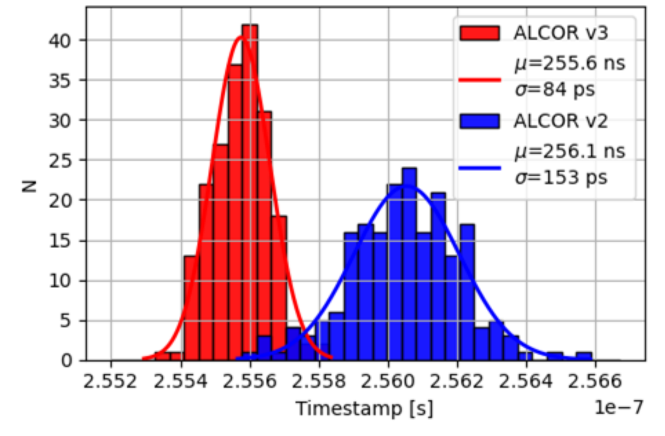
Small revisions on ALCOR FE design

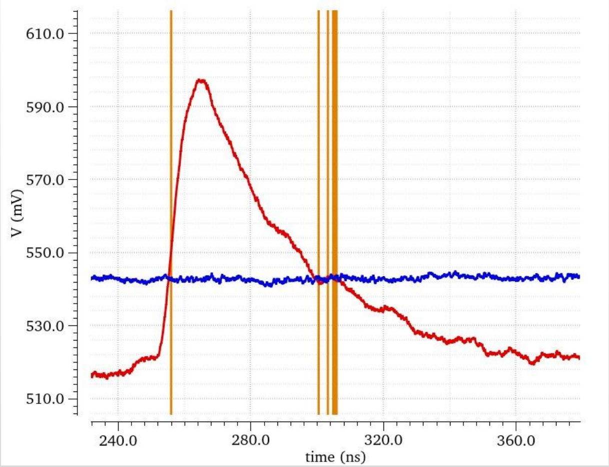
- **Increased amplifier bandwidth** to improve time resolution
  - transient noise simulations
  - Vth = 0.5 p.e.
  - **jitter: 153 ps → 84 ps**
- **Discriminator** with programmable **hysteresis** to avoid re-triggering on slow tail with low thresholds





S13360-3050, OV=3V





ALCORv2 transient noise sim

Digital shutter

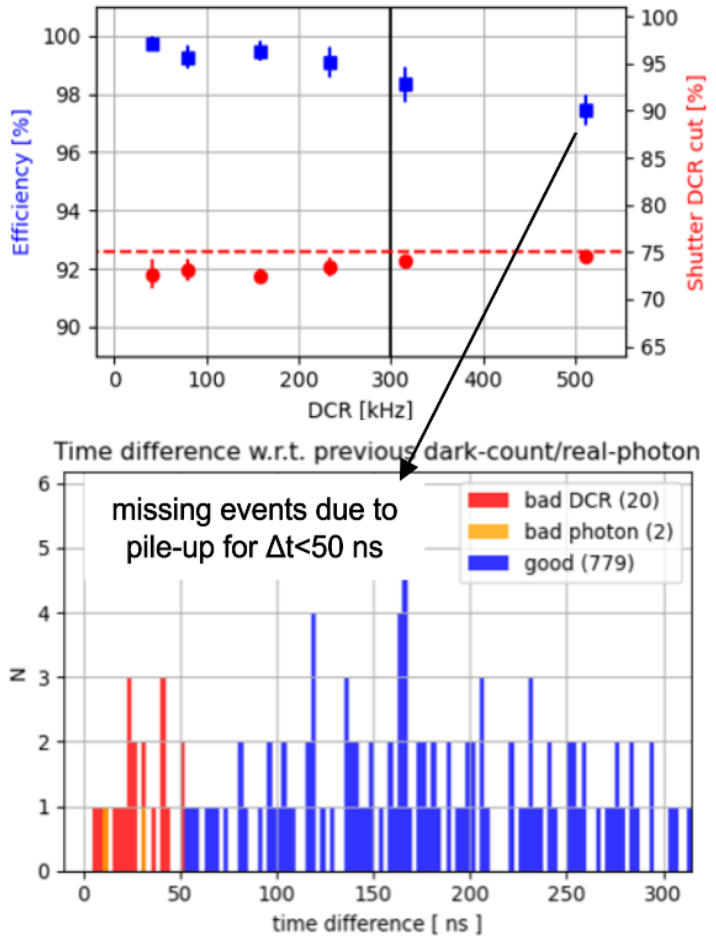
- Expected DCR below 300 kHz (with online annealing cycles on SiPM)
- Digital Shutter “inhibit” pixel digital logic to suppress out-of-gate DCR hits and reduce data throughput (~10.2 ns bunch crossing, ~300 ps bunch length)

$$\text{Reduction Factor} = \frac{\text{EIC bunch crossing period}}{\text{shutter time window}} = \frac{10.2\ \text{ns}}{t_{shutter}}$$

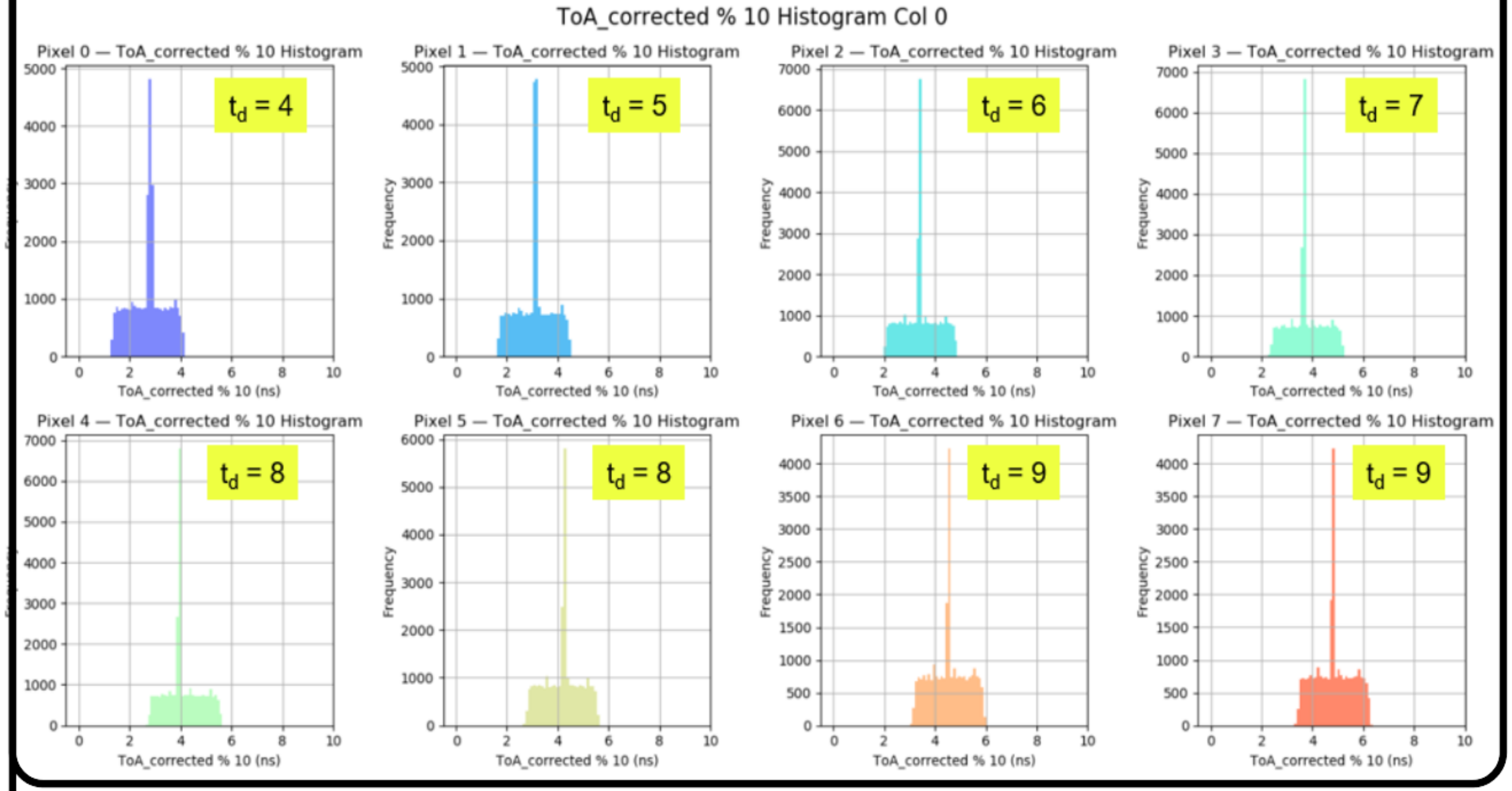
- The external Test-Pulse is used as enable for the analogue trigger
- The minimum width of this timing window can be of the order 2-3 ns
- Each pixel implements a programmable delay chain to set the proper shutter timing window
- 4 configuration bits allow you to choose 16 steps from 0 to 15 delays
- Each delay step is approximately 350 ps (TYP corner)
- Additionally, the End of Column circuits allow you to choose a programmable delay, on the shutter signal, to adjust the skew between columns (16 steps from 0 to 15, each step approximately 100 ps)
- Shutter needed only when DCR becomes higher due to SiPMs taking radiation damage over time. Use first period of ePIC data taking to optimize shutter calibration
- Two complementary off-chip data throughput reduction approaches are being considered to perform online data filtering at sub-detector level against pure dark-count events:
    - INFN Roma: Online AI-based distributed data reduction (more details in C. Rossi talk at RICH2025)
    - INFN Genova: SciFi Interaction Tagger (more details in S. Vallarino talk at the 2025 EICUG EC Workshop)

Digital shutter simulations

Single-channel mixed-signal sim (including FE time-walk and pile-up effects)

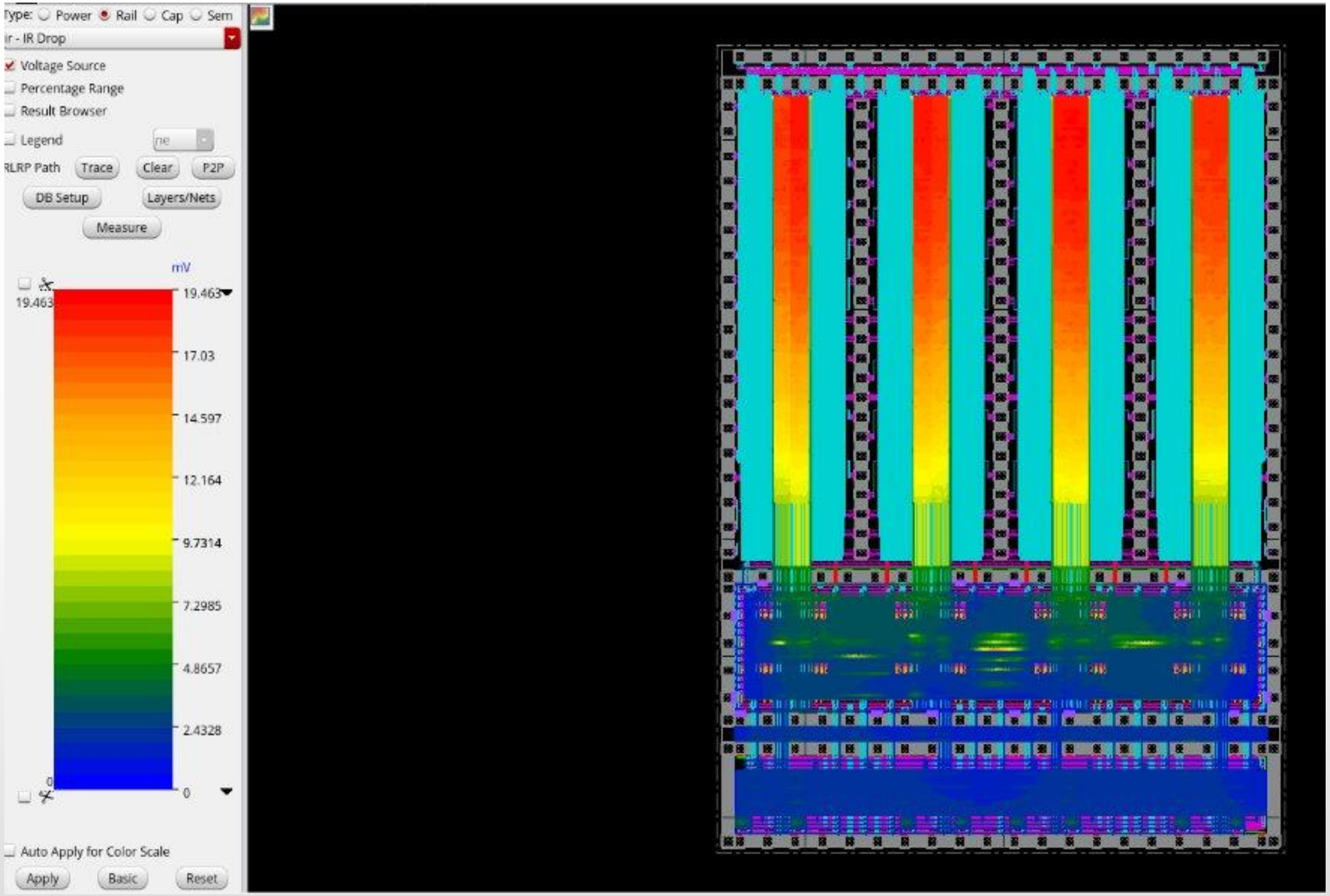


Full-chip digital sim (ideal case) to verify shutter distribution for the whole ALCOR chip: use in-pixel programmable delay chain (4 bits, LSB ڷ 350 ps) to center shutter window for each pixel/column



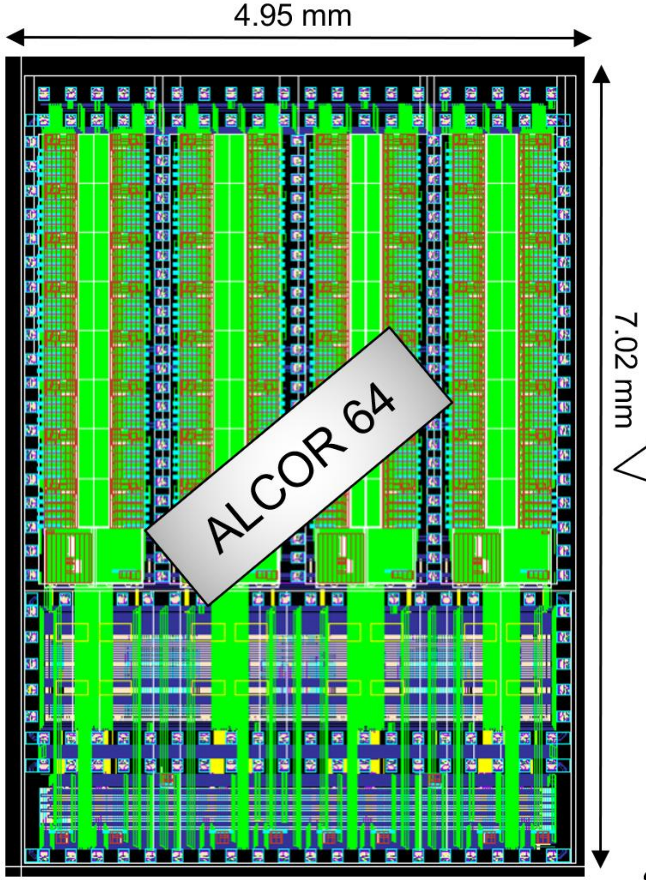
➔ **FE** (jitter, time-walk, pile-up) and **physics** (real photon signals distribution) contributions **not included in this simulation**

Power analysis IR drop (digital)



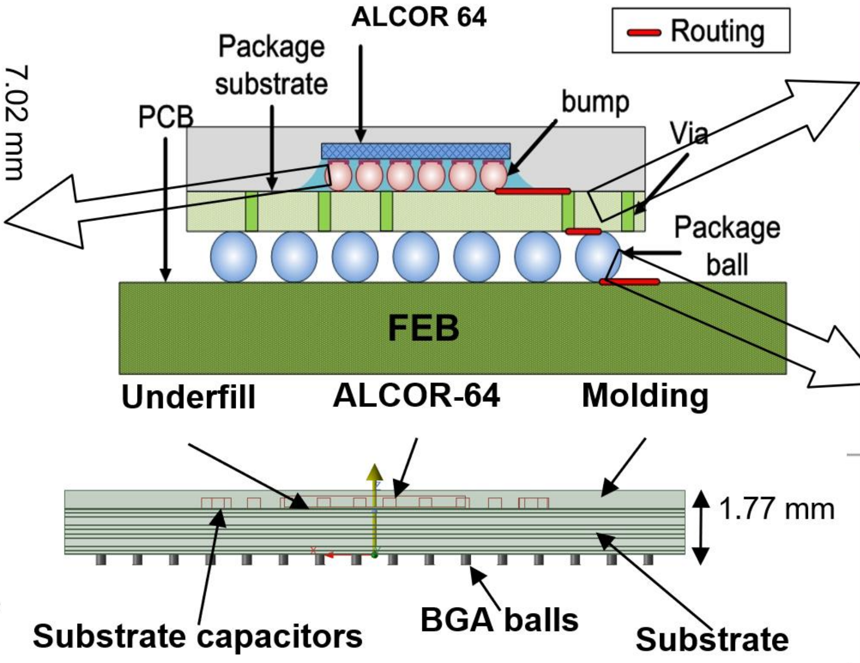
Analysis done with VCD file form post pnr simulation at 400 MHz clock (expected total power 1.2 W: digital + analogue + bias)

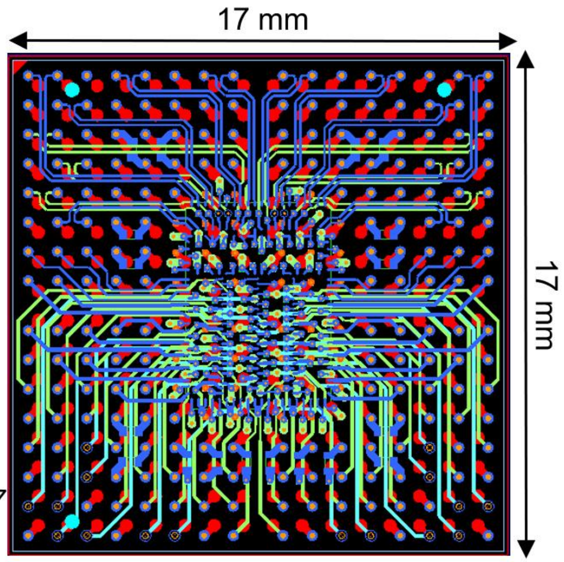
ALCOR-64 BGA package

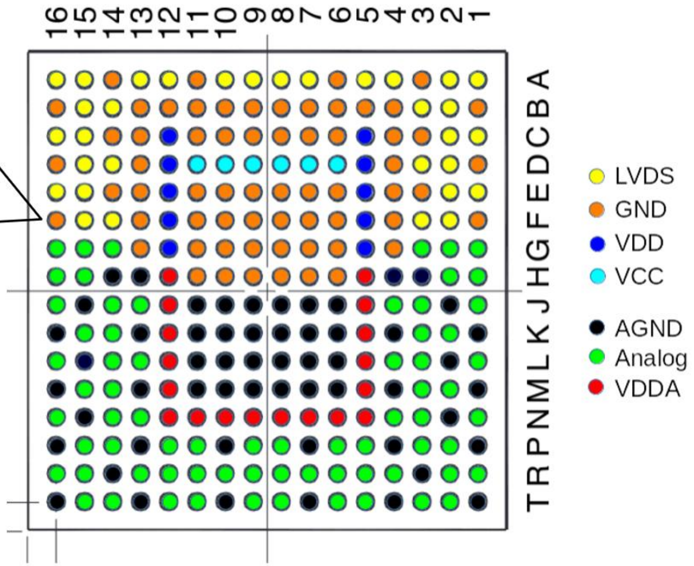


FC-BGA: flip-chip ball grid array

- BGA 256 Ball 17x17mm
- Pitch: 1 mm
- BT-Epoxy
- 10 Layers (2+N+2)





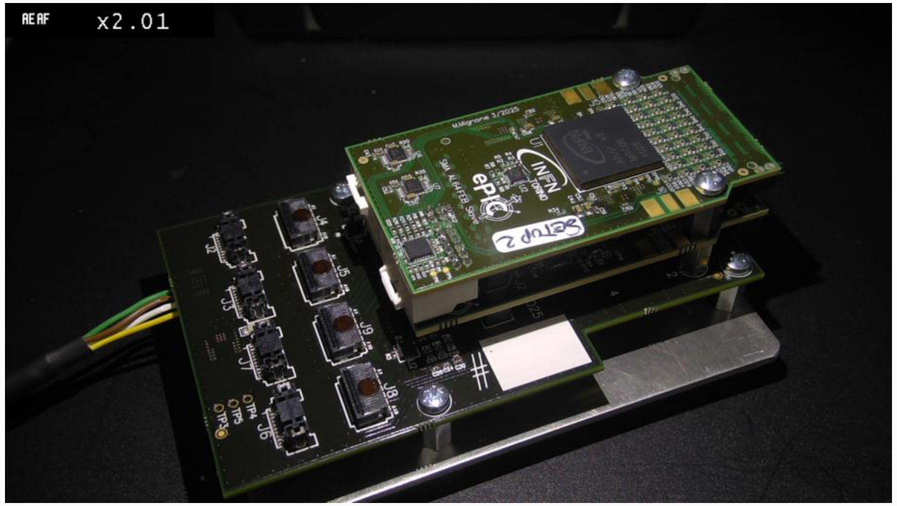


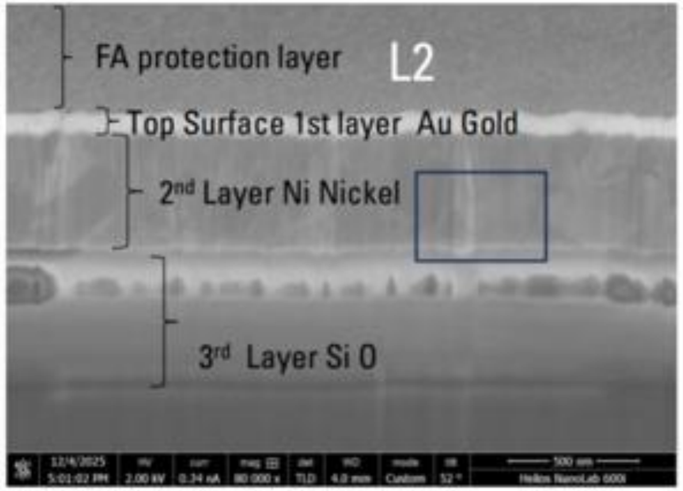
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	🟡	🟡	🟠	🟡	🟡	🟠	🟡	🟡	🟡	🟡	🟠	🟡	🟡	🟠	🟡	🟡
B	🟠	🟡	🟡	🟠	🟠	🟠	🟠	🟠	🟠	🟠	🟠	🟠	🟠	🟡	🟡	🟠
C	🟡	🟡	🟠	🟠	🔵	🟠	🟠	🟠	🟠	🟠	🟠	🔵	🟠	🟠	🟡	🟡
D	🟠	🟡	🟡	🟠	🔵	🩵	🩵	🩵	🩵	🩵	🩵	🔵	🟠	🟡	🟡	🟠
E	🟡	🟡	🟠	🟠	🔵	🟠	🟠	🟠	🟠	🟠	🟠	🔵	🟠	🟠	🟡	🟡
F	🟠	🟡	🟡	🟠	🔵	🟠	🟠	🟠	🟠	🟠	🟠	🔵	🟠	🟡	🟡	🟠
G	🟢	🟢	🟢	🟠	🔵	🟠	🟠	🟠	🟠	🟠	🟠	🔵	🟠	🟢	🟢	🟢
H	🟢	🟢	⚫	⚫	🔴	🟠	🟠	🟠	🟠	🟠	🟠	🔴	⚫	⚫	🟢	🟢
J	🟢	⚫	🟢	🟢	🔴	⚫	⚫	⚫	⚫	⚫	⚫	🔴	🟢	🟢	⚫	🟢
K	⚫	🟢	🟢	⚫	🔴	⚫	⚫	⚫	⚫	⚫	⚫	🔴	⚫	🟢	🟢	⚫
L	🟢	⚫	🟢	🟢	🔴	⚫	⚫	⚫	⚫	⚫	⚫	🔴	🟢	🟢	⚫	🟢
M	⚫	🟢	🟢	⚫	🔴	⚫	⚫	⚫	⚫	⚫	⚫	🔴	⚫	🟢	🟢	⚫
N	🟢	⚫	🟢	🟢	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🔴	🟢	🟢	⚫	🟢
P	⚫	🟢	🟢	⚫	🟢	🟢	⚫	🟢	🟢	⚫	🟢	🟢	⚫	🟢	🟢	⚫
R	🟢	🟢	⚫	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	🟢	⚫	🟢	🟢
T	⚫	🟢	🟢	⚫	🟢	🟢	⚫	🟢	🟢	⚫	🟢	🟢	⚫	🟢	🟢	⚫

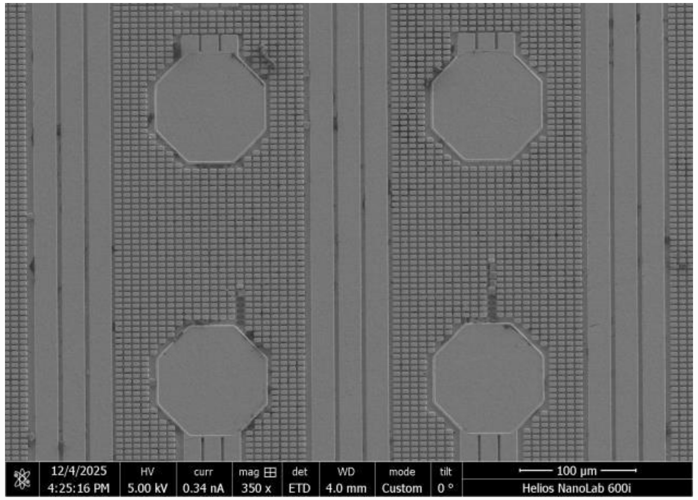
🟡 LVDS
🟠 GND
🔵 VDD
🩵 VCC

⚫ AGND
🟢 Analog
🔴 VDDA

ALCOR-64 status







Nov 2025: 1st Run flip-chip die attach failed due to solder overflow causing short circuits between bump pads

- **FIB dissection + SEM-EDX analysis** (Dec 2025) on one die showed that **UBM layers extend beyond the bump pads**, covering additional areas of the chip surface above the passivation layer
- This metallization **creates a wetting surface** that facilitates solder migration from the substrate-side bumps to the die, leading to **short circuits between adjacent pads**
- UBM process managed by packaging vendor (via different subcontractor)
- Testing on four chips confirmed the presence of short circuits
- Exploring alternatives for **UBM and bumping process**:
  - IMEC informed us that **new Flip-Chip TLR** has been introduced by the foundry this year
  - UBM and bumping process can be done on single dies via IMEC subcontractor

Summary

- ALCOR is a **64-channel mixed-signal ASIC** adopted for the readout of the **SiPM sensors** for the **ePIC dRICH** detector
- **ALCOR-32** has been extensively used within the dRICH Collaboration in the last 5 years: several laboratory and beam tests demonstrated the ALCOR-based readout capability to measure single photons with good time resolution and rate capability
- **ALCOR-64** includes all features and specifications required for the ePIC dRICH:
  - 64 channels, BGA package, shutter, 394.08 MHz clock frequency
  - **Packaging issues** introduce an important delay in our schedule
  - Discussions ongoing to find alternative UBM process and preparation for new MPW run
- Exploring alternatives for UBM and bumping process to be still on schedule for the installation planned in 2032

Backup

SEU/SEL results (July 2024)

ECCR/BCR/PCR registers checked against SEU (every second)

- ECCR σ = (9.4 ± 1.8) · 10^{-14} cm^2/bit periphery register → no TMR in ALCOR v2.1
- BCR σ = (7.6 ± 1.1) · 10^{-14} cm^2/bit periphery register → no TMR in ALCOR v2.1
- **PCR σ = (3.3 ± 0.5) · 10^{-15} cm^2/bit** pixel register → TMR (accumulating bit flips due to auto-correction bug in triplicated registers)

SEU rate in ePIC:

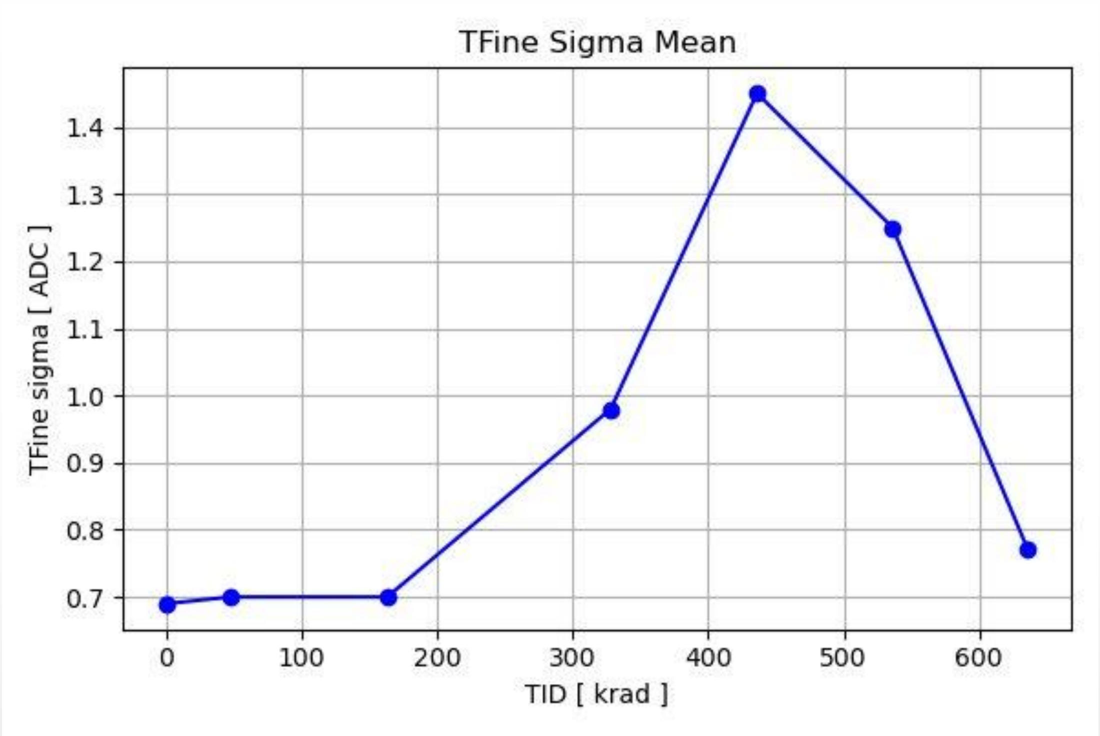
- dRICH Flux = 140 (h > 20 MeV) / (cm^2 s)
- ALCOR bits: (2048 + 192) = 2240 → ALCOR-64 bits will be 4480
- Total ALCOR: 4992
- Total bits: 4992 · 4480 = 2.2 · 10^7 bits

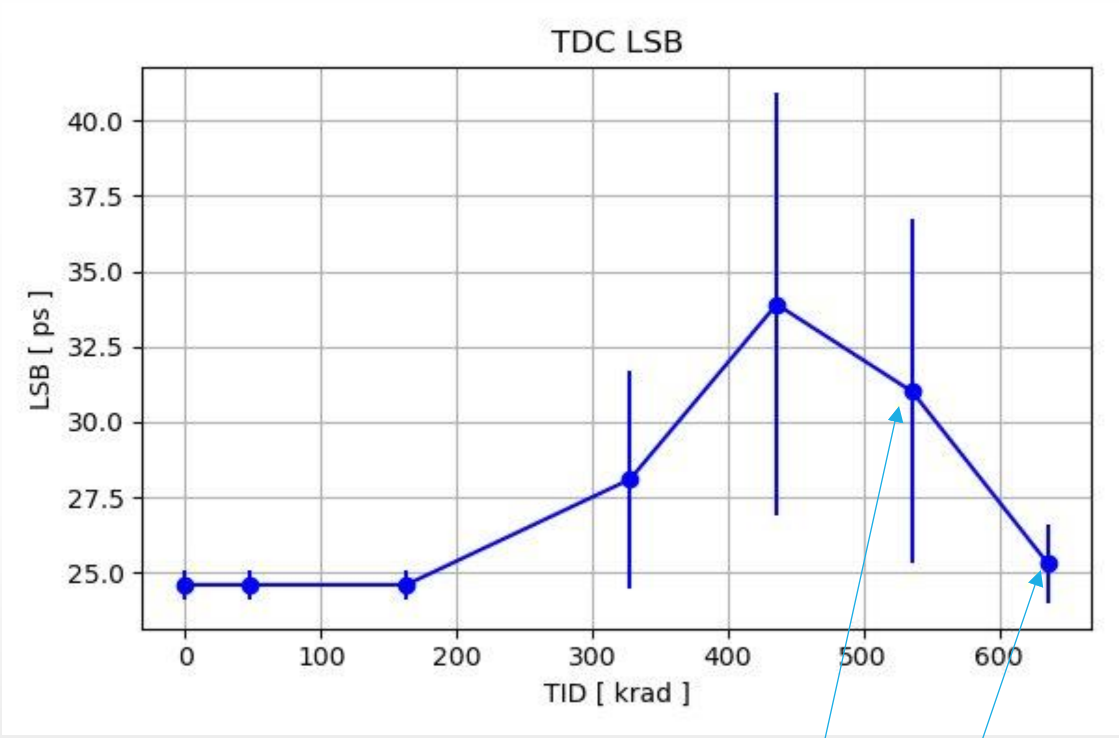
➢ σ = 3.3 · 10^{-15} cm^2/bit → **MTBF** = 9.8 · 10^4 seconds → every **27 hours**

➢ No latchup events (from power supply currents monitoring)

SEU rate is within the expected manageable levels

TID results - TDC error & LSB





***last two points = 436 krad after 10 hours and 5 months**

- Technology is sufficiently radiation tolerant to be used in the ePIC dRICH environment
- Similar results w.r.t. irradiation tests performed on another ASIC with same technology [1]
- Also other FEB components will be tested and validated