Photon-to-Digital Converter Readout in 65 nm CMOS with sub-10 ps Timing Precision

May 18th , 2026, Paris, France

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3IT Institut interdisciplinaire d'innovation technologique UdS

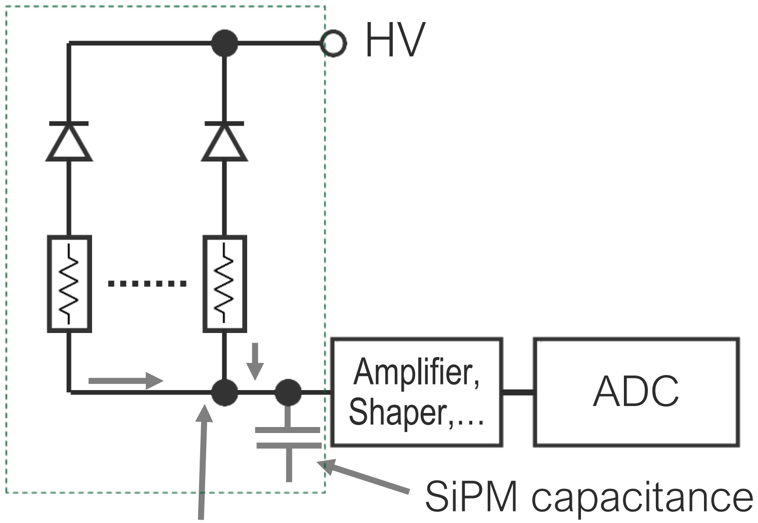
Canada NRC·CNRC

OAK RIDGE National Laboratory

UdS Université de Sherbrooke

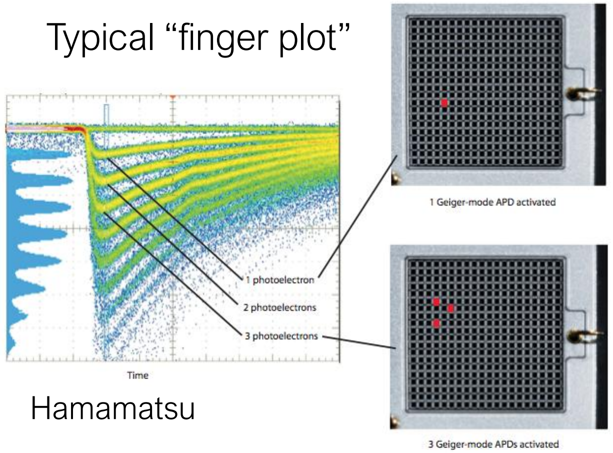
Photon-to-Digital Converters

Analog SiPM:



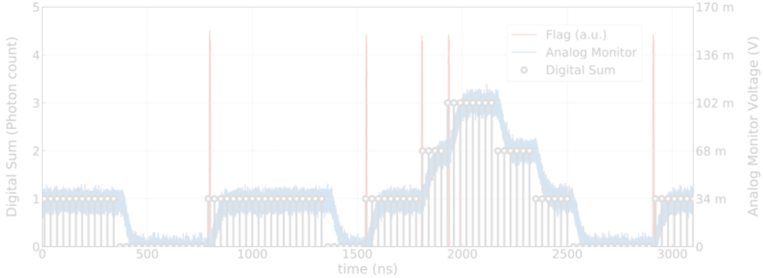
SiPM capacitance → electronic noise

Analog current sum

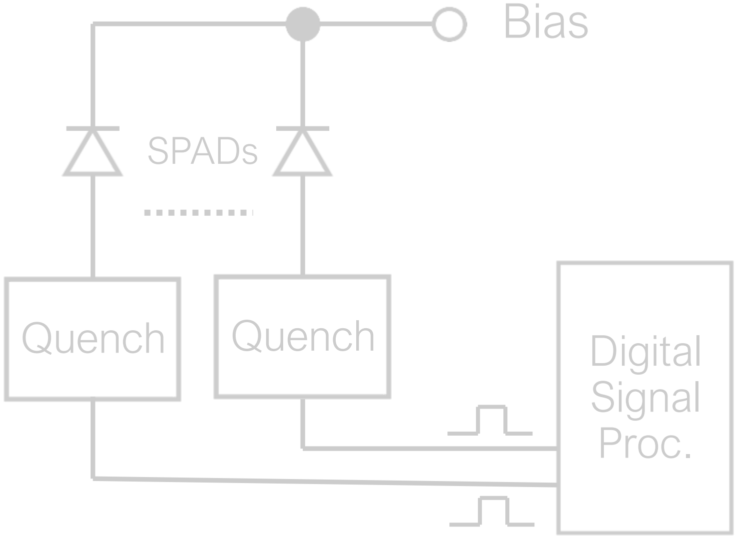

Typical "finger plot"

Hamamatsu

PDC (Digital SiPM):



Rossignol T et al. "A 3D photon-to-digital converter readout for low-power and large-area applications" (2024) Journal of Instrumentation (19) P09017 10.1088/1748-0221/19/09/P09017



Benefits:

- ○ Direct digital readout:
  - Precise photon counting resolution on the whole dynamic range
  - Can lower static power consumption significantly
- ○ Disabling noisy SPADs: Dark Count Rate (DCR) reduction
- ○ Programmable hold-off delay: mitigation of after-pulsing
- ○ Embedded signal processing: number of photons, dark count filters, time-to-digital conversion, etc.

Photon-to-Digital Converters

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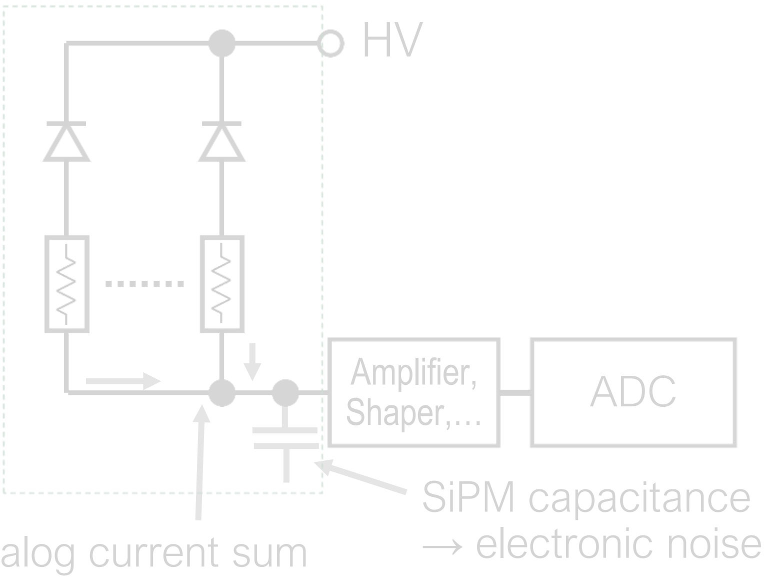


HV

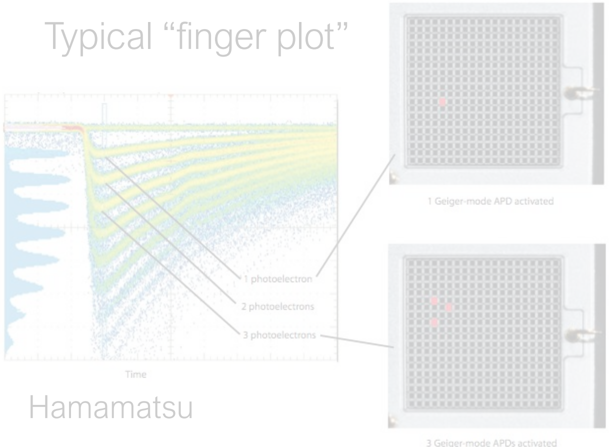
Amplifier, Shaper,…

ADC

SiPM capacitance → electronic noise

Analog current sum

Typical “finger plot”



Hamamatsu

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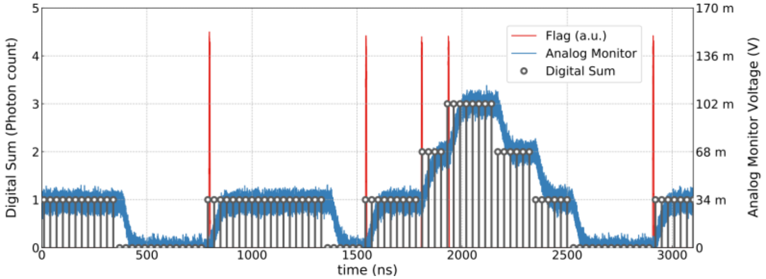

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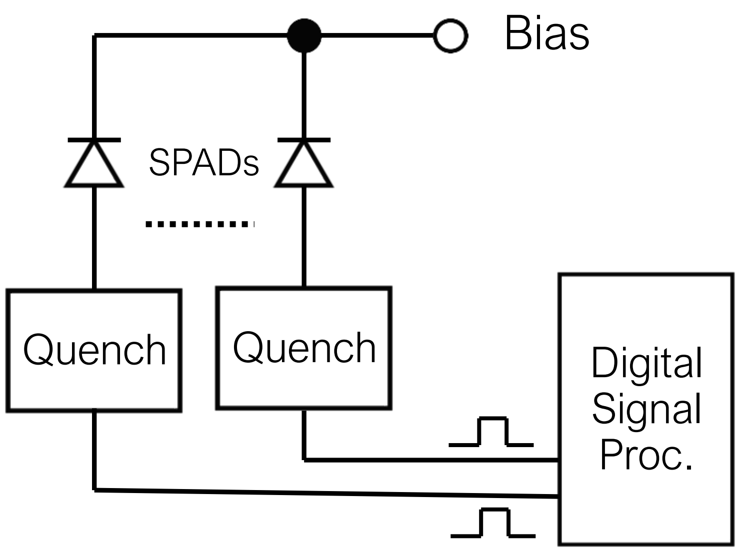

Bias

SPADs

Quench

Quench

Digital Signal Proc.

Benefits:

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Photon-to-Digital Converters - 3D versus 2D

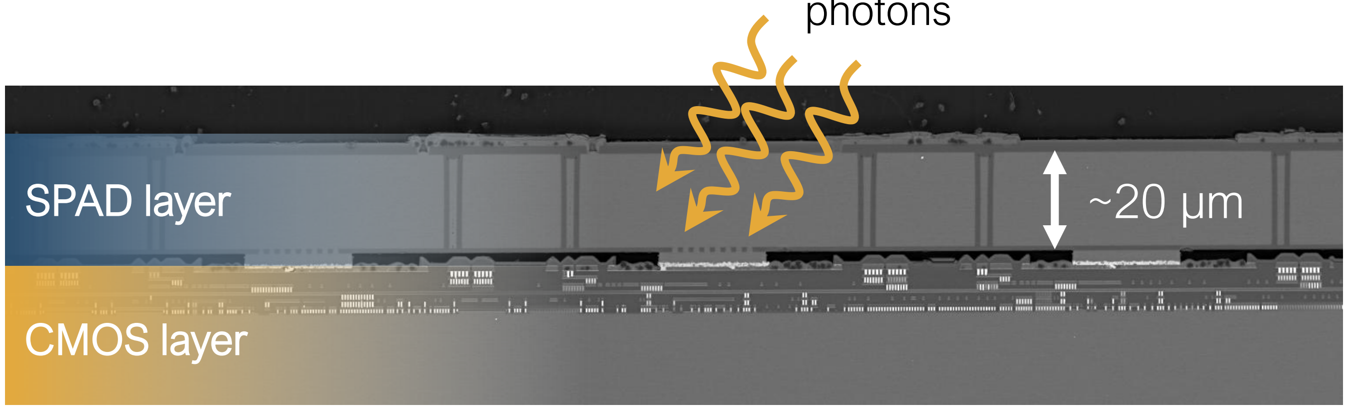
2D

🟦 = SPAD layer

🟨 = CMOS electronics layer

The solution:

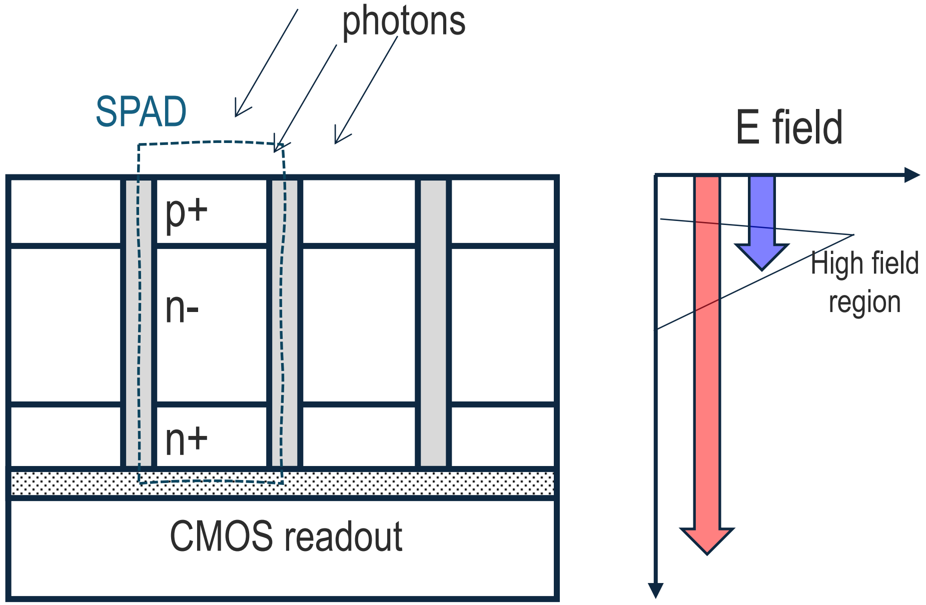
3D vertical integration



- ○ Enables high photosensitive fill factor
  with
- ○ Advanced digital processing
- ○ Choice of SPAD optimal technology
  with
- ○ Choice of CMOS optimal technology for application specific functions

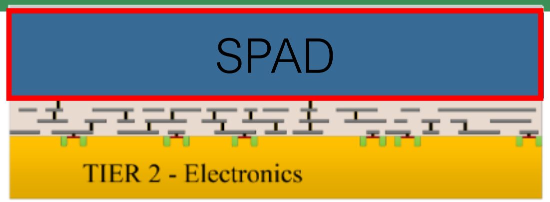
Pratte JF et al. "3D Photon-to-Digital Converter for Radiation Instrumentation: Motivation and Future Works" (2021) Sensors;21(2):598. 10.3390/s21020598

SPAD Array – Architecture Overview



- Thinned SPAD array (~20 µm)
  - Backside connection (cathode)
  - No through-silicon-vias (TSV)
  - Full thickness trench isolation [1]
- High Fill-Factor because no TSV

Actual implementation



- Frontside illuminated p^+n SPAD:
  - junction near the photon incidence face
- For λ ~ 400 nm (violet):
  - 3/4 of photons absorbed within 100 nm from entrance face (in Si)
    - Before/in the high field region
  - Less photoelectron drift
  - Laterally uniform electric field

} High timing resolution

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1. Ito, Kyosuke, et al. "A Back Illuminated 10µm SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm." 2020 IEEE International Electron Devices Meeting (IEDM). IEEE, 2020.

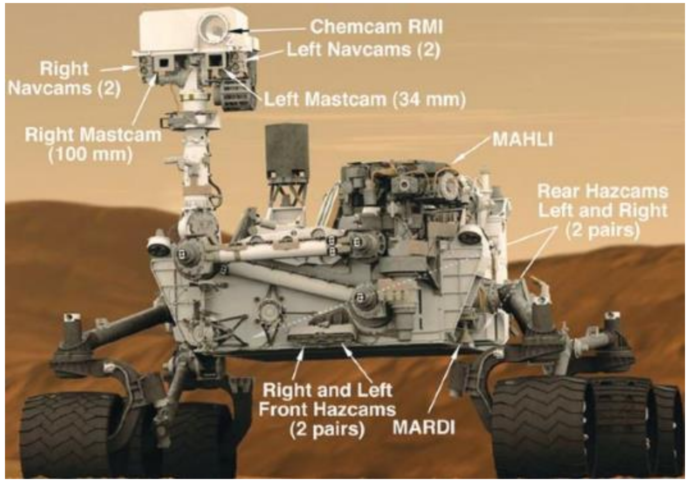
Fabricated by Teledyne DALSA

High-end CCD process line
--> excellent for SPAD R&D

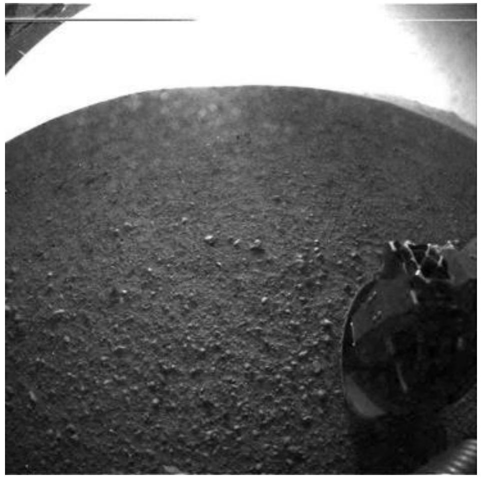
- 150 mm process line
- low contaminant / gold free clean rooms

World top 5 MEMS Foundry
--> excellent for wafer level integration

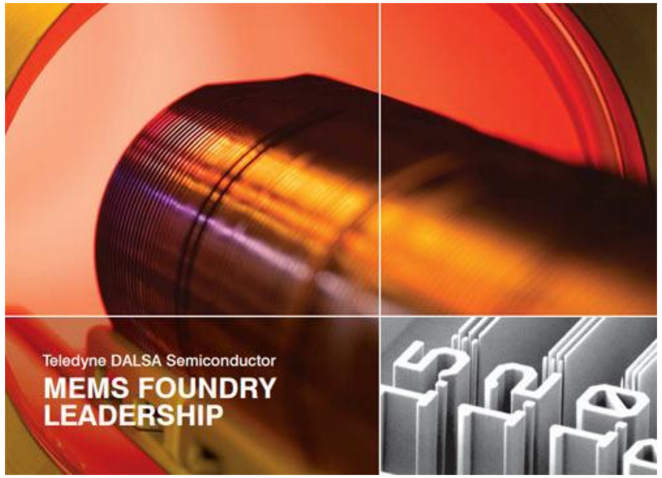
- 150 mm and 200 mm process line
- Wafer thinning, deep etching, bonding, ...



The Eyes of the Mars Curiosity Rover. Tech Briefs (2012)



Life on Mars: Rover landing gives boost to Canadian tech sector. The Globe and Mail (2012)



Courtesy of Teledyne DALSA

MEMS Foundry Rankings (2017 sales in US$M)	
STMicroelectronics	174
Teledyne DALSA	60
Silex Microsystems	50
TSMC	47
X-Fab	42

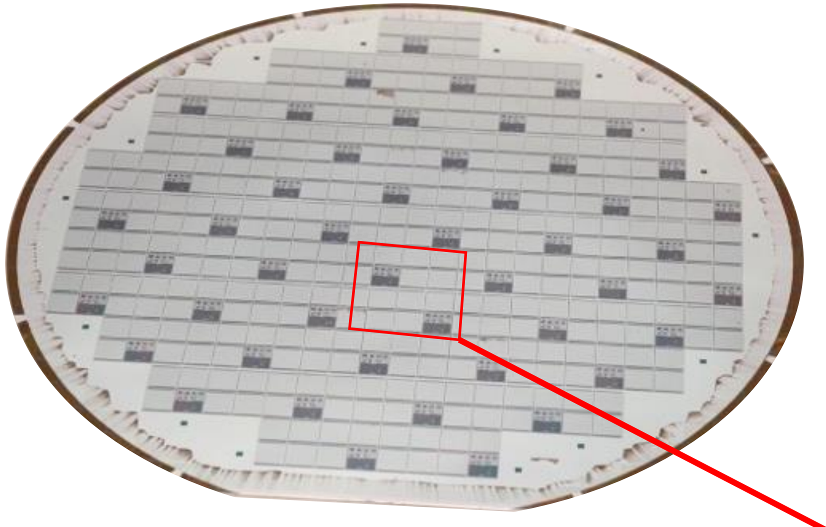
Status of the MEMS Industry 2018 Market and technology Report
Yole Development (2018)

TELEDYNE DALSA
Everywhereyoulook™

Teledyne DALSA Semiconductor (est. 1980)

~ 500 employees located at Bromont near Montreal, Canada

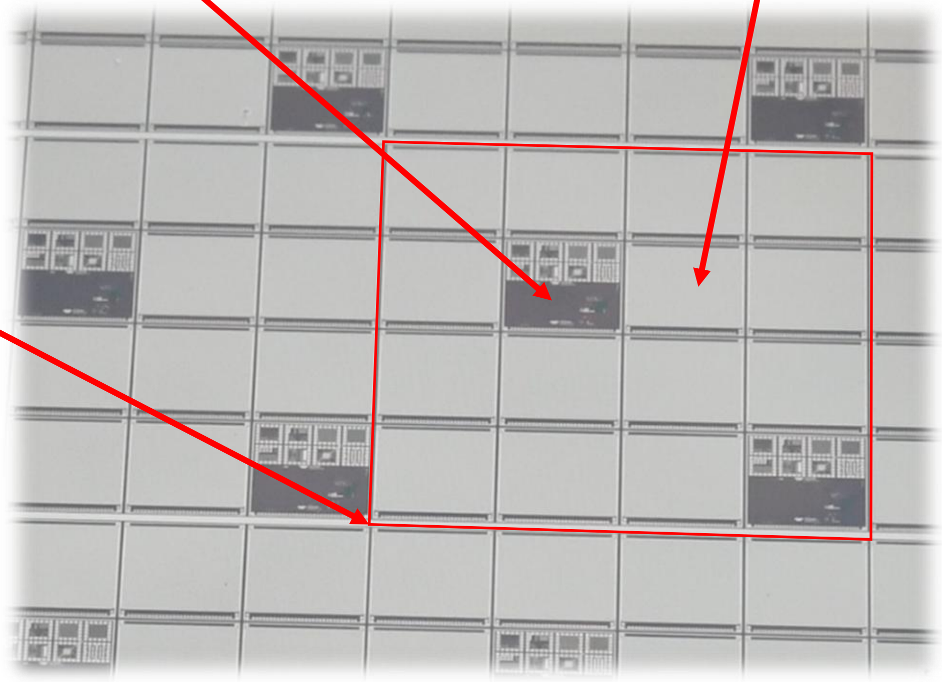
SPAD wafer bonding to CMOS wafer – Assembling the PDC

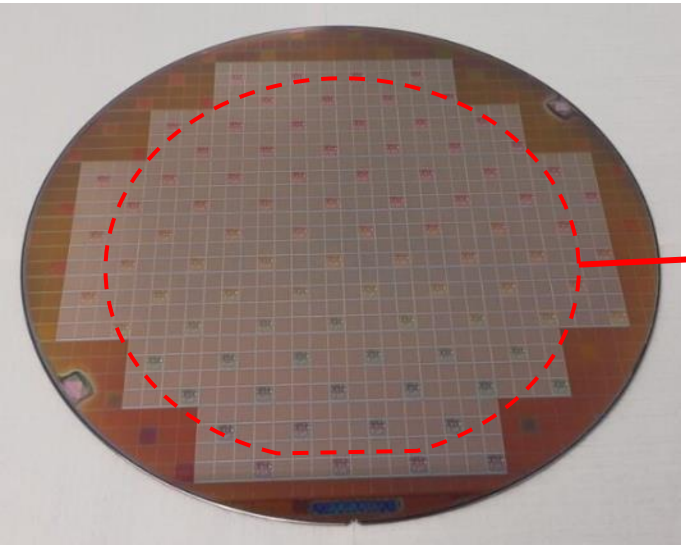


Process
monitoring
structures

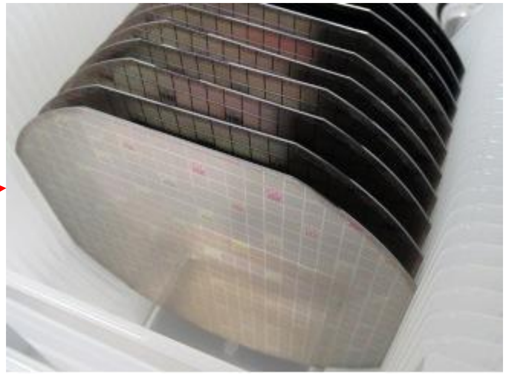
and

bonding
alignment





200 mm TSMC 180 nm CMOS wafer



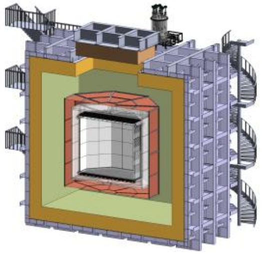
Resized to 150 mm

PDC flavors

Developing a multi-purpose ASIC in 180 nm and 65 nm technology

180 nm – Low-Power PDC

- Particle physics

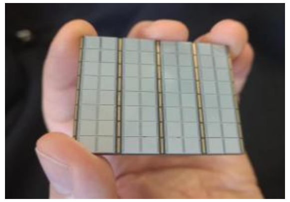


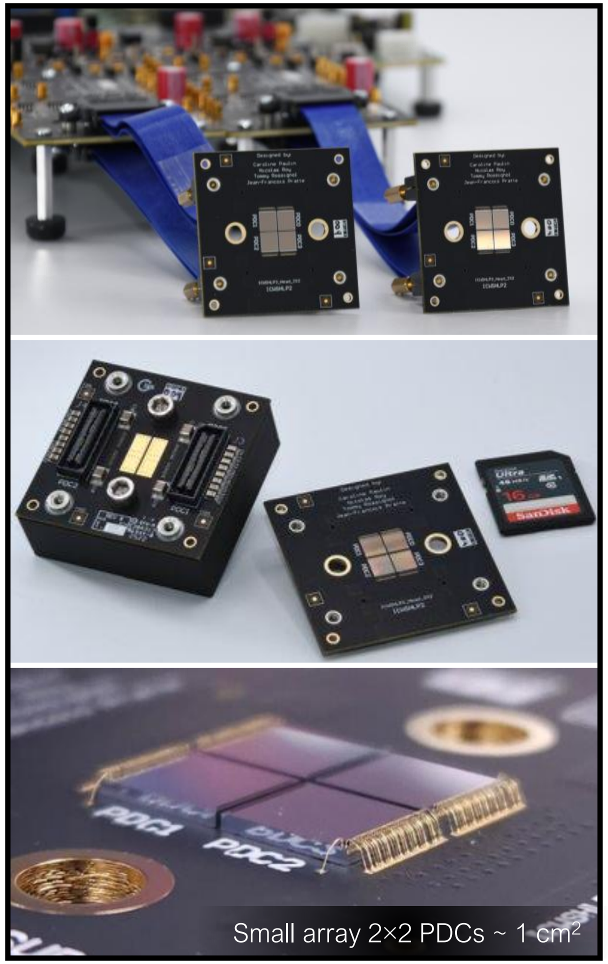
e.g. ARGO

- Neutron Imaging

e.g. ORNL

- 8x8 tile in development

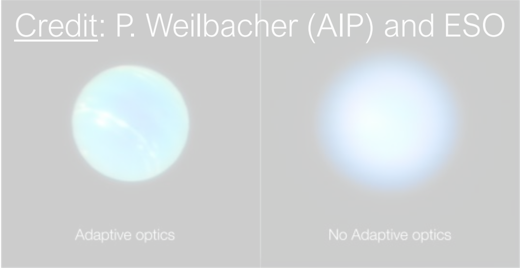




Small array 2×2 PDCs ~ 1 cm²

65 nm – Timing-Optimized PDC

- Adaptive Optics for Astrophysics:

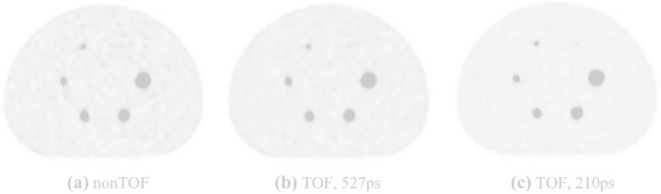


Credit: P. Weilbacher (AIP) and ESO

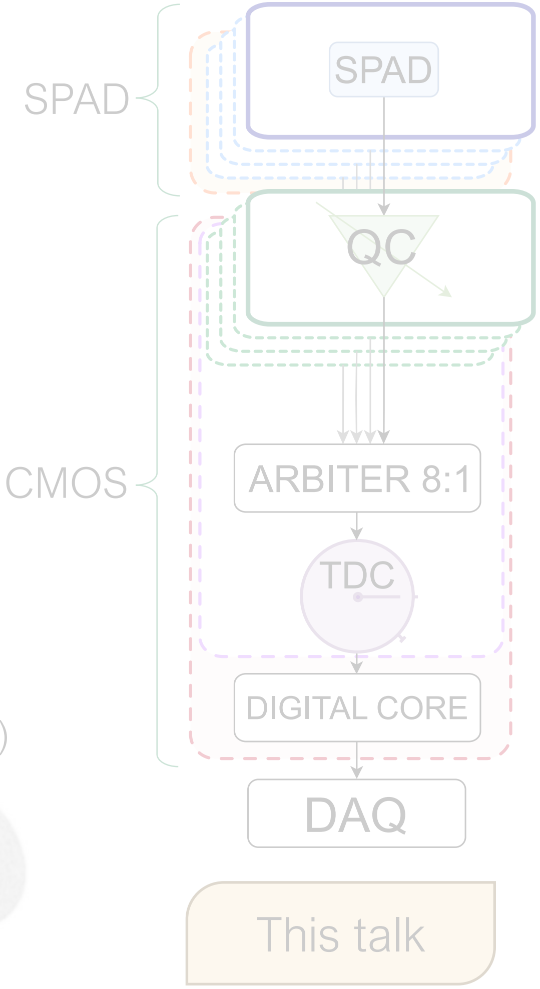
- Quantum telecommunications

e.g. Quantum Encryption and Science Satellite

- Medical imaging (TOF-PET, TOF-CT)



e.g. ToF PET



SPAD

CMOS

SPAD

QC

ARBITER 8:1

TDC

DIGITAL CORE

DAQ

This talk

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180 nm – Low-Power PDC

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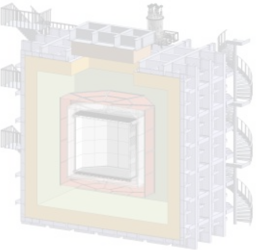

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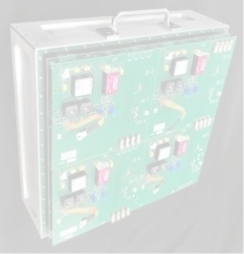

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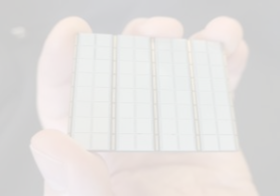

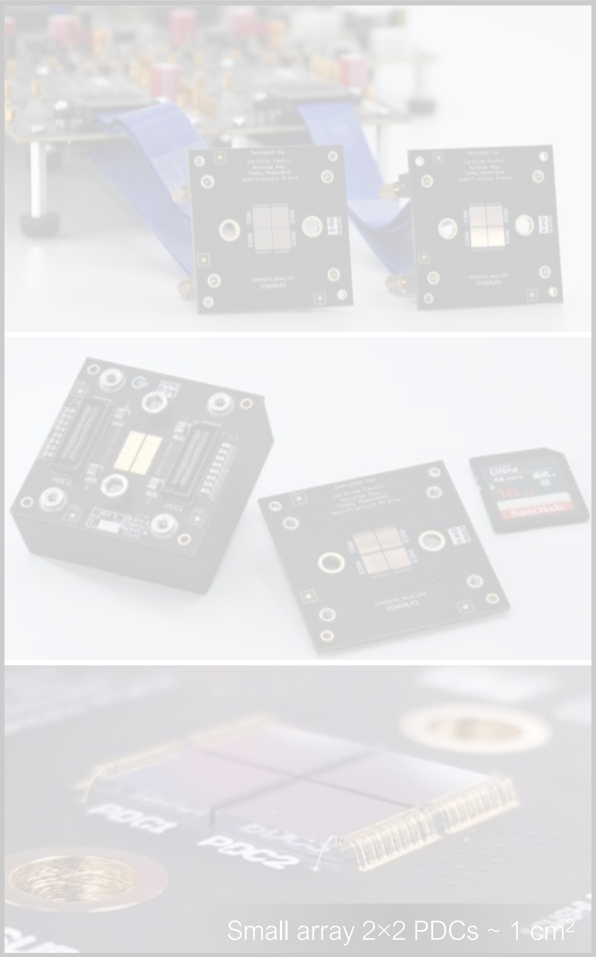

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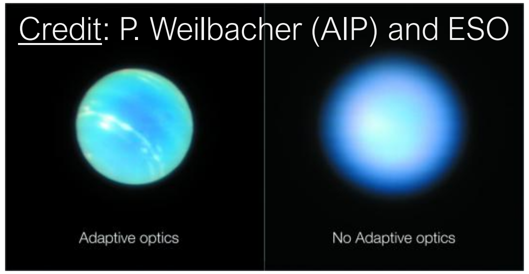

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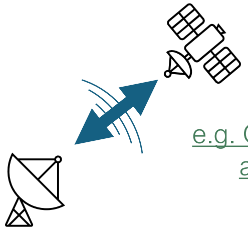

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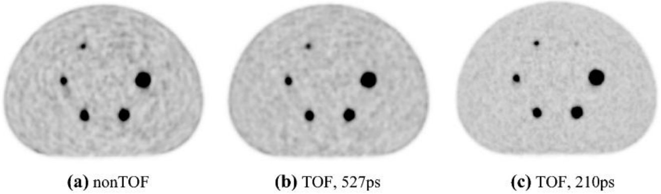
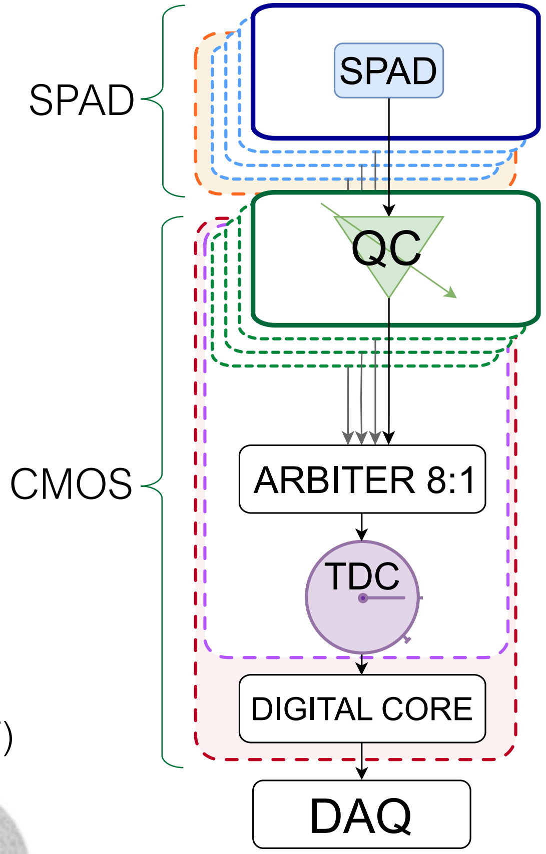


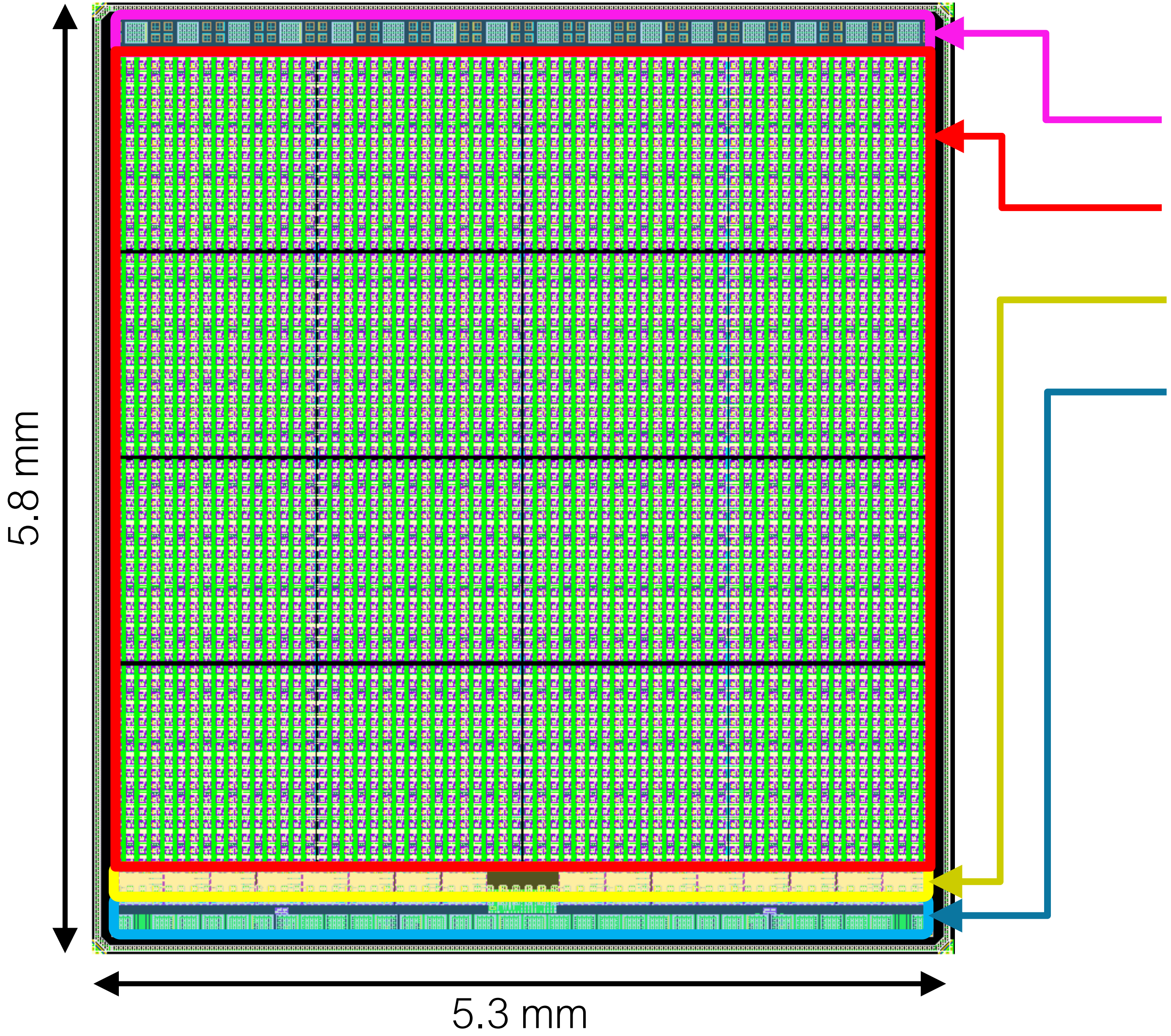
(a) nonTOF (b) TOF, 527ps (c) TOF, 210ps

e.g. ToF PET



This talk

PDC Crystal-based architecture

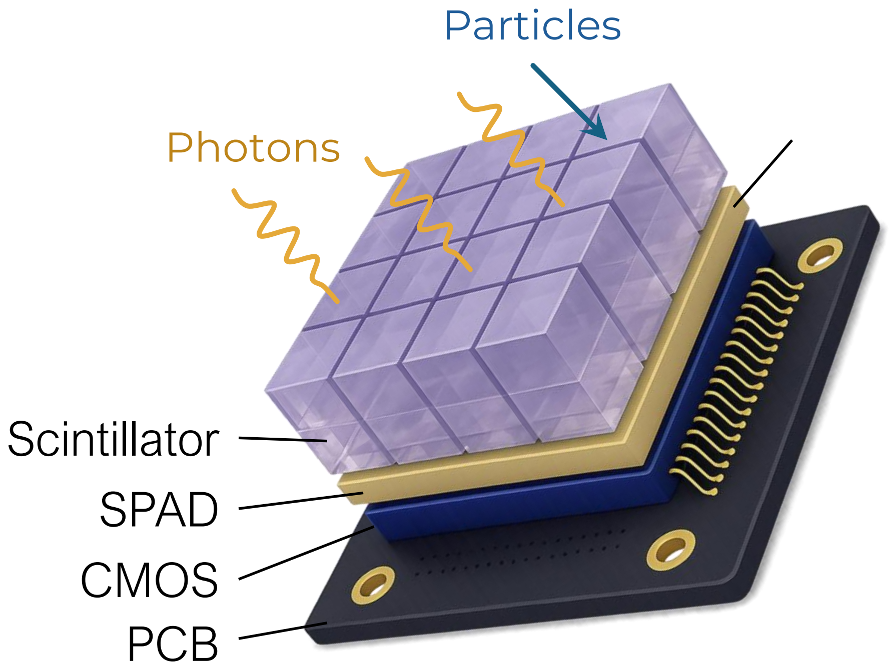


Validation structures

5×5 mm^2 active area (4096 SPADs)

Post-processing area (16 SRAM blocks)

32 × IO pads (2.5 Gb/s serializer)



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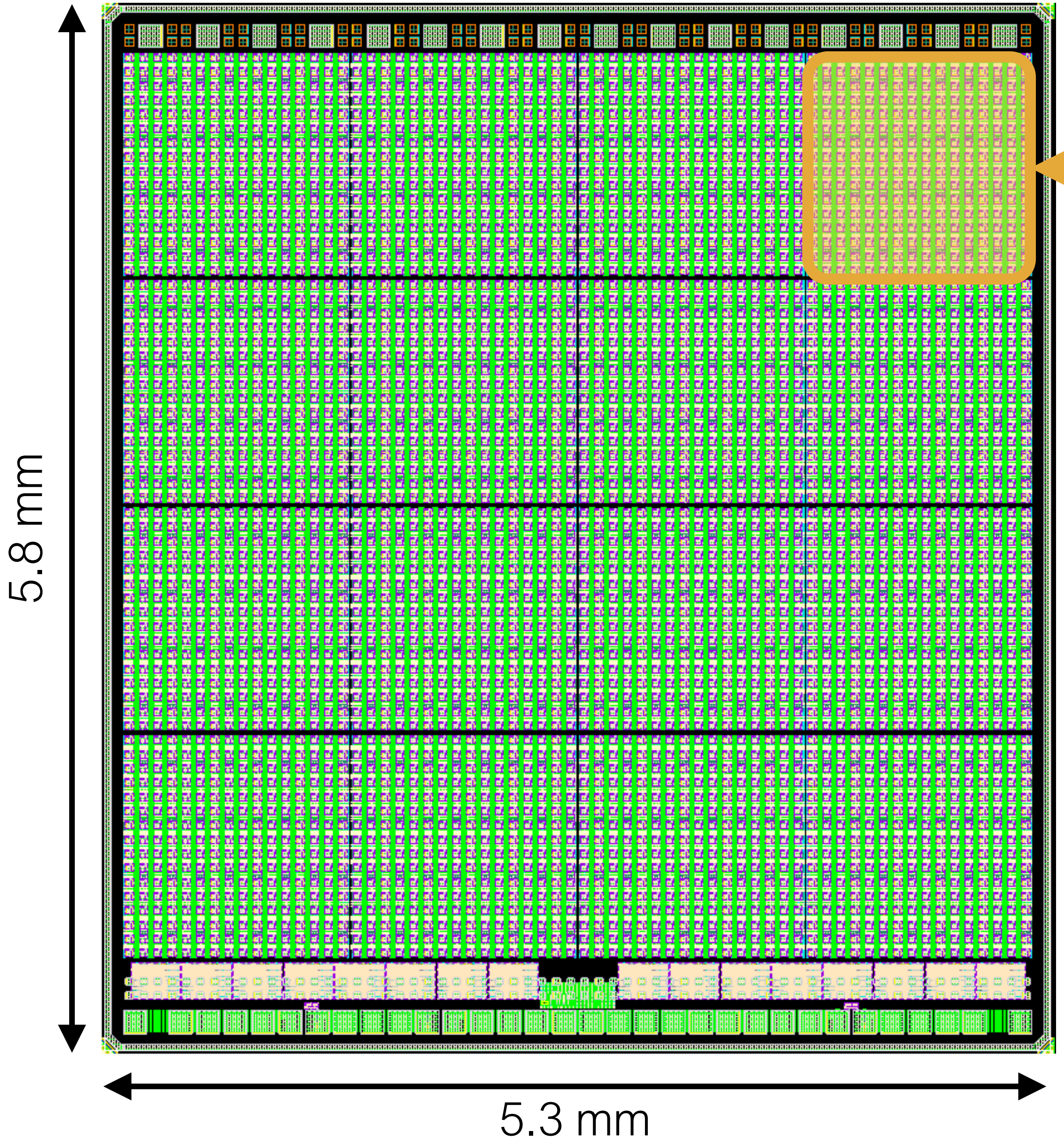
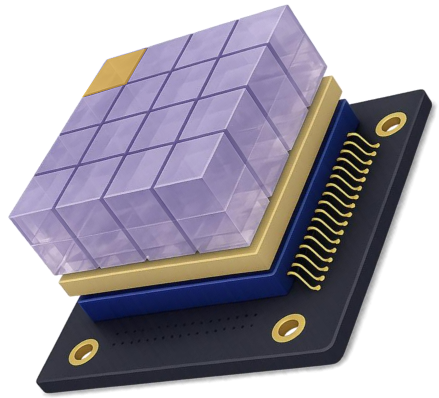
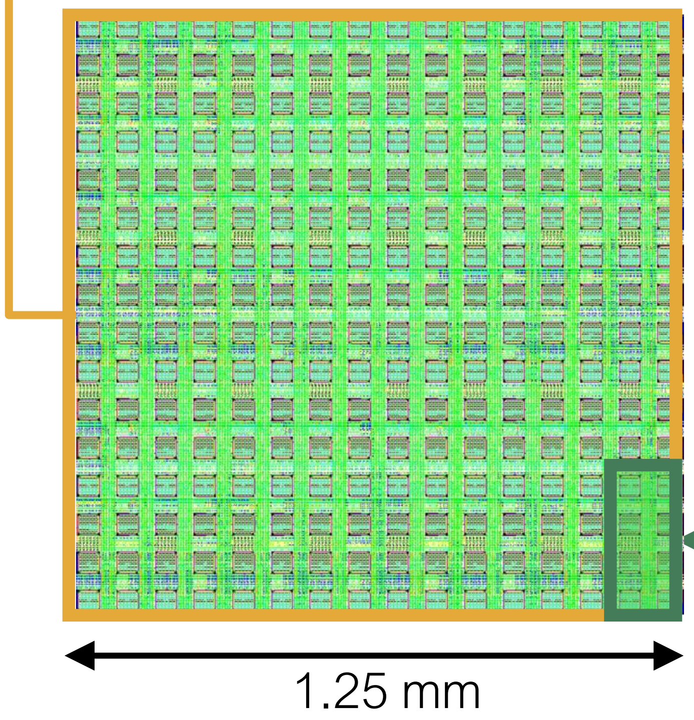
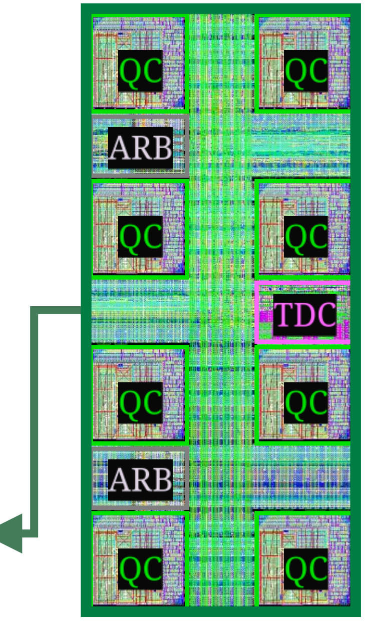




Crystal-based sector:

- 256 SPADs
- 32 QC groups
- 32 TDCs
- Event detection
- Time & energy binning

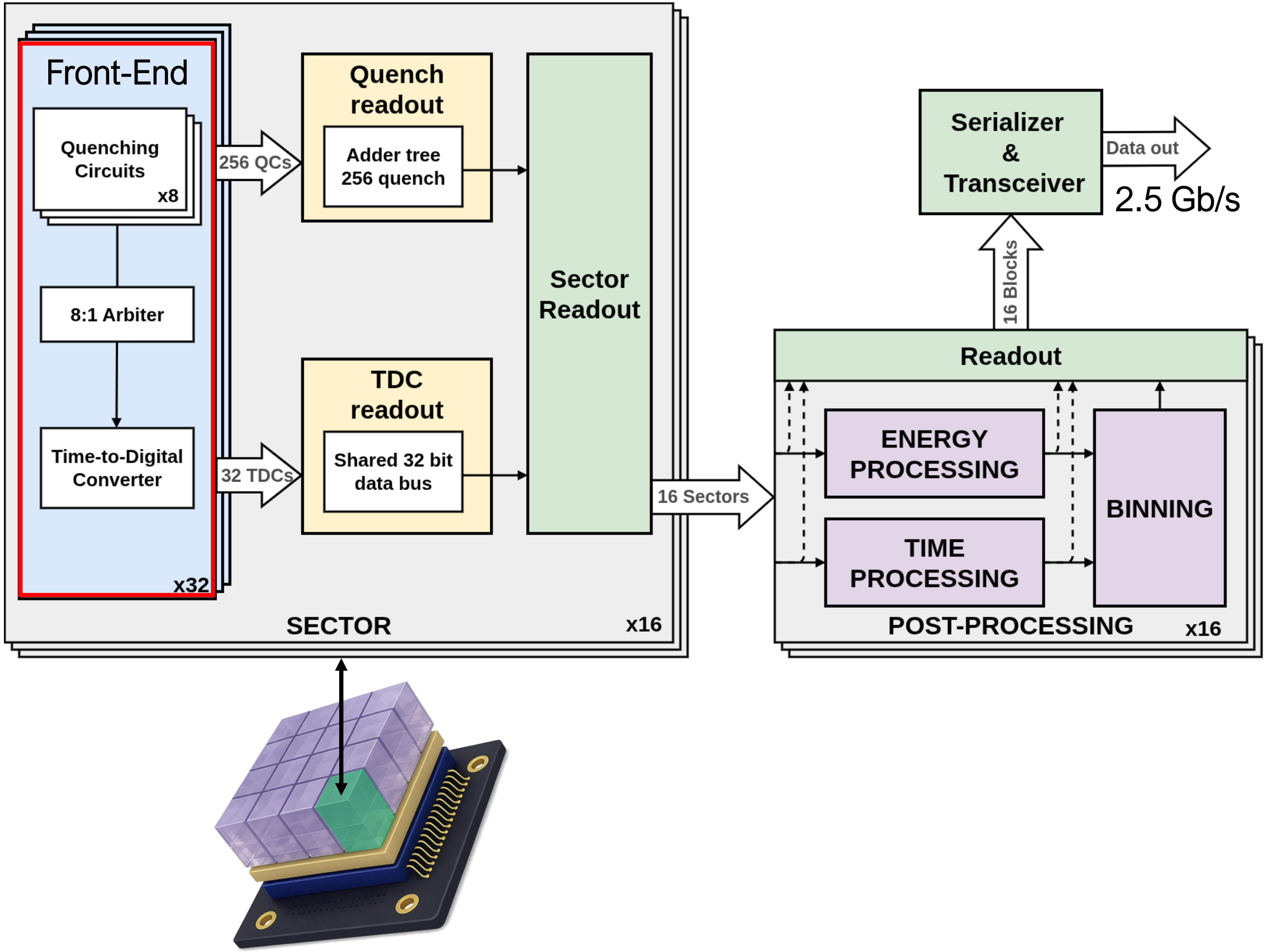




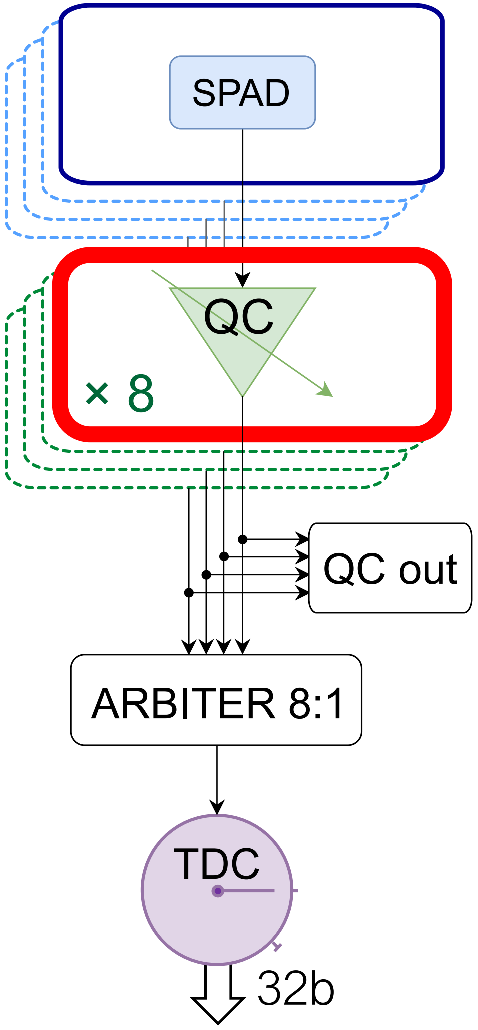
1 QC group
(8 SPADs,
1 TDC)

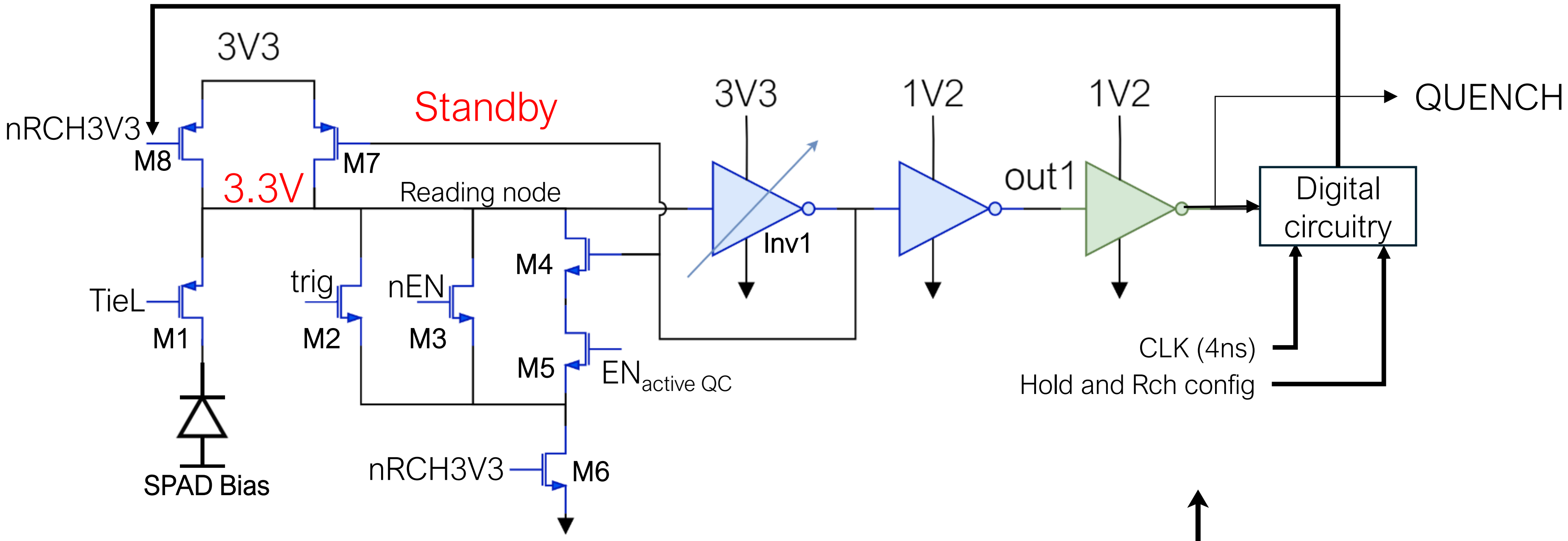
Architecture

- Front-End
  - 1 QC per SPAD
  - 1 TDC:8 SPAD
    - Skew correction
    - 12 bits of time code
    - 12 bits of global time reference (clk)
    - 8 bits of address
- Sector readout
  - Energy branch
    - Adder tree for 256 SPADs
    - Programmable event detection
  - Timing branch
    - Shared data bus readout for 32 TDCs
- Post-processing
  - Time-code sorting
  - Energy and timing histogram
  - Best linear unbiased estimator (BLUE)



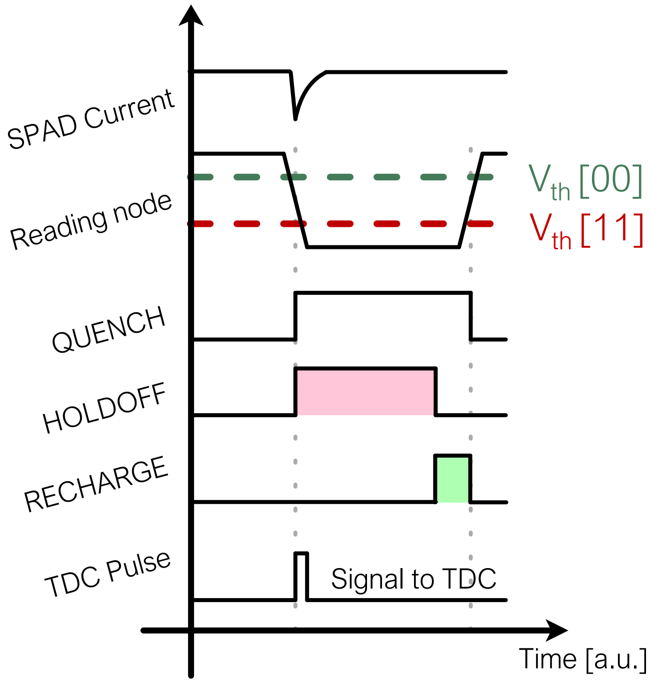
Quenching Circuit





The QC features:

- **Configurable threshold inverter-**based discriminator topology (Inv1)
- **Configurable** holdoff and recharge timing
- **Active quench** (AQ) NMOS
- QC **enabling** and **triggering** circuit
- Maximum of 6.6V SPAD excess voltage



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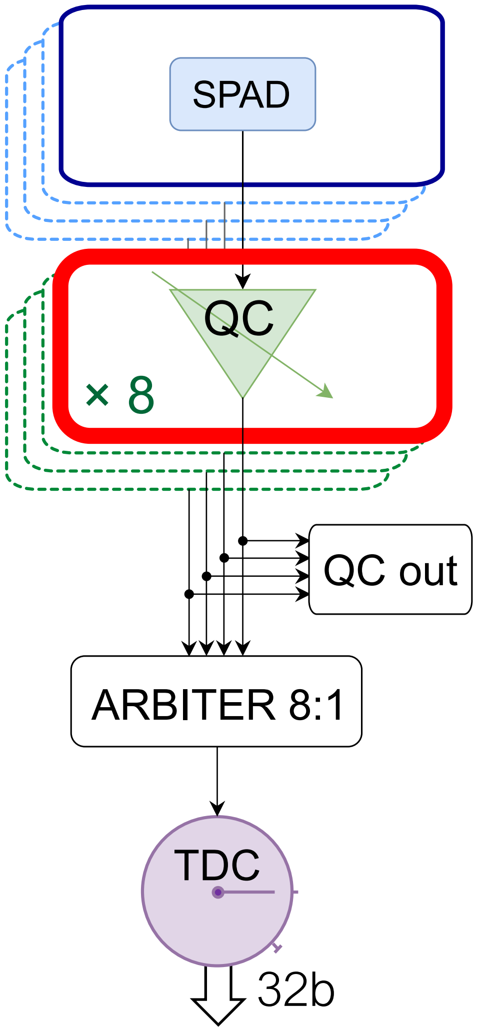

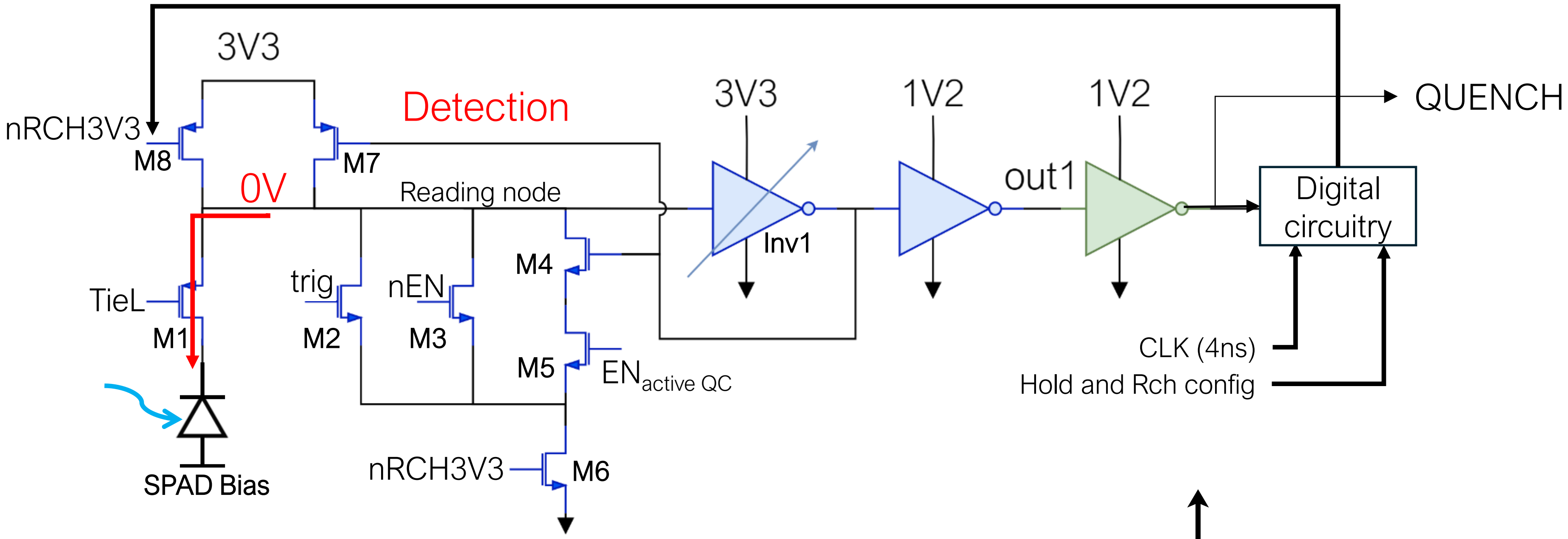

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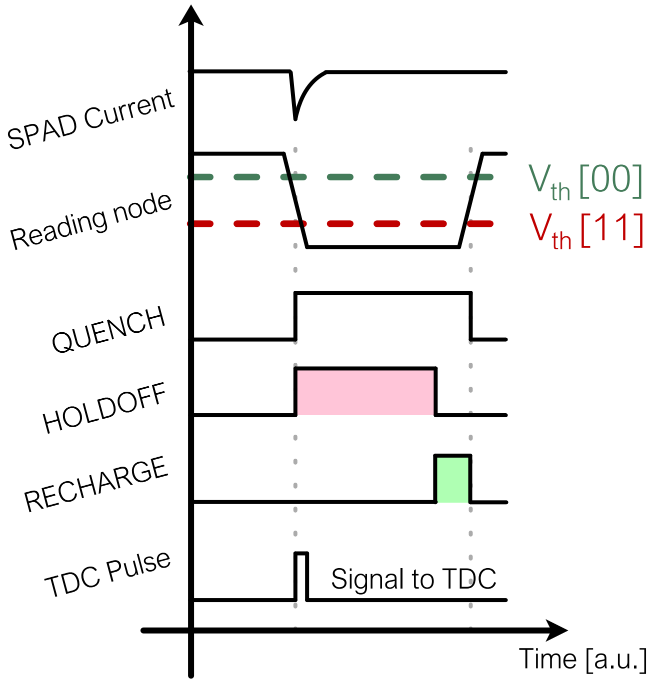
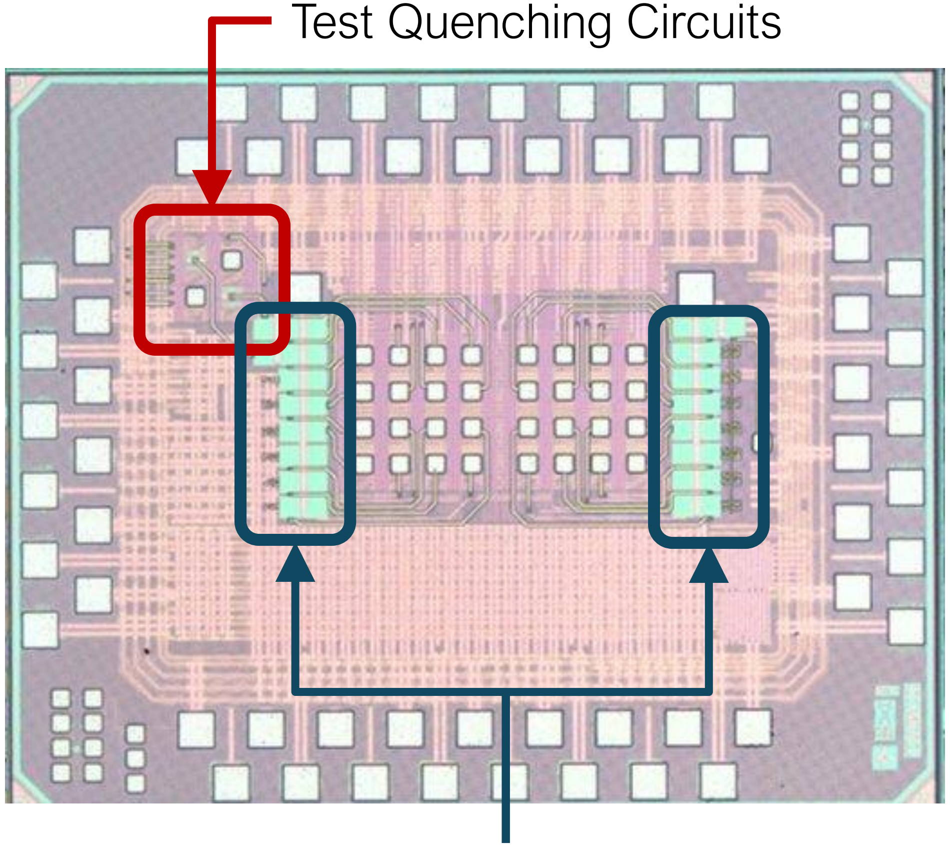
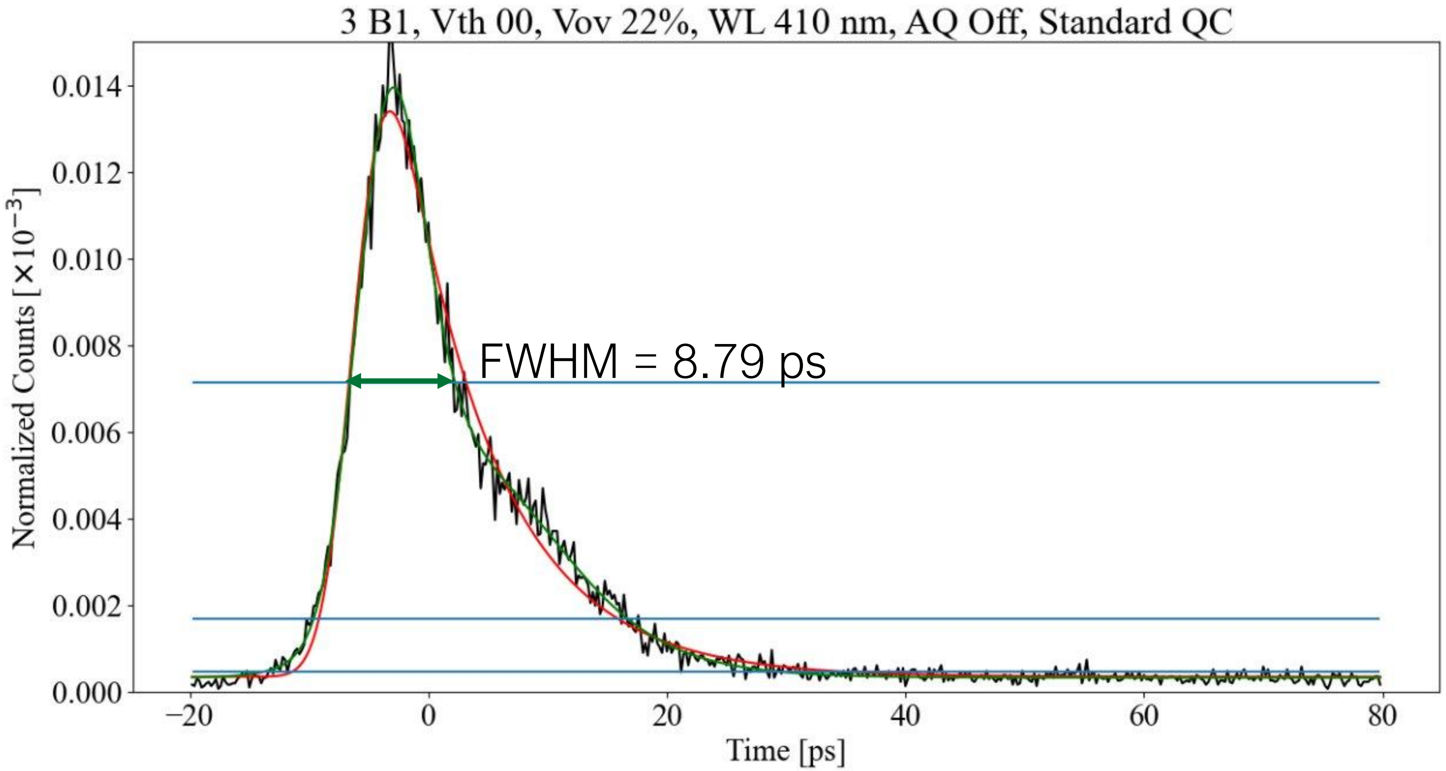


Quenching Circuit

Test ASIC - 2024

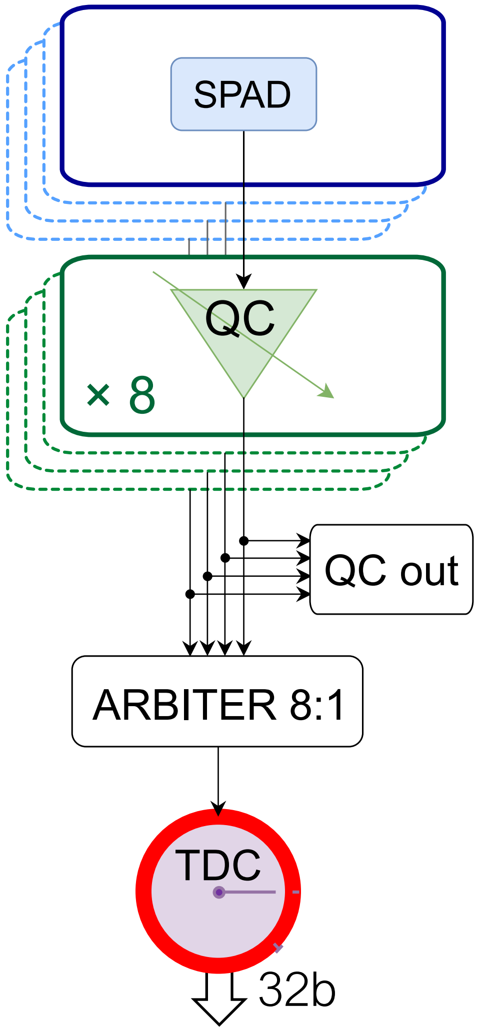

Test Quenching Circuits

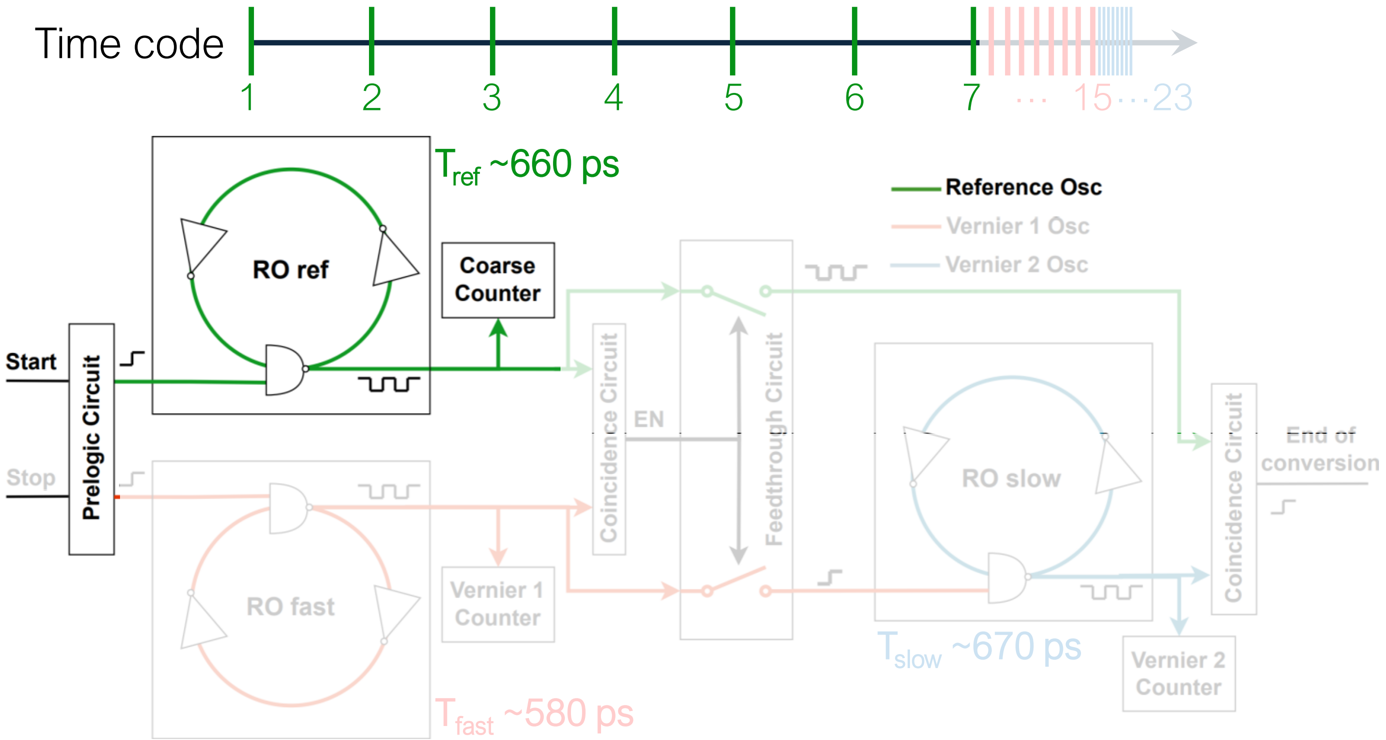
2D CMOS SPADs
for testing purposes


3 B1, Vth 00, Vov 22%, WL 410 nm, AQ Off, Standard QC

FWHM = 8.79 ps

Time-to-Digital Converter (TDC)





- Dual Vernier Architecture to reduce the number of cycles
  - Reduced dead time
  - Improved timing precision
- Calibration mode
  - Digitally controlled ring oscillators (DCRO) with switched capacitors
  - Frequency counter for each ring
  - DCRO frequency registers calculated outside of the ASIC

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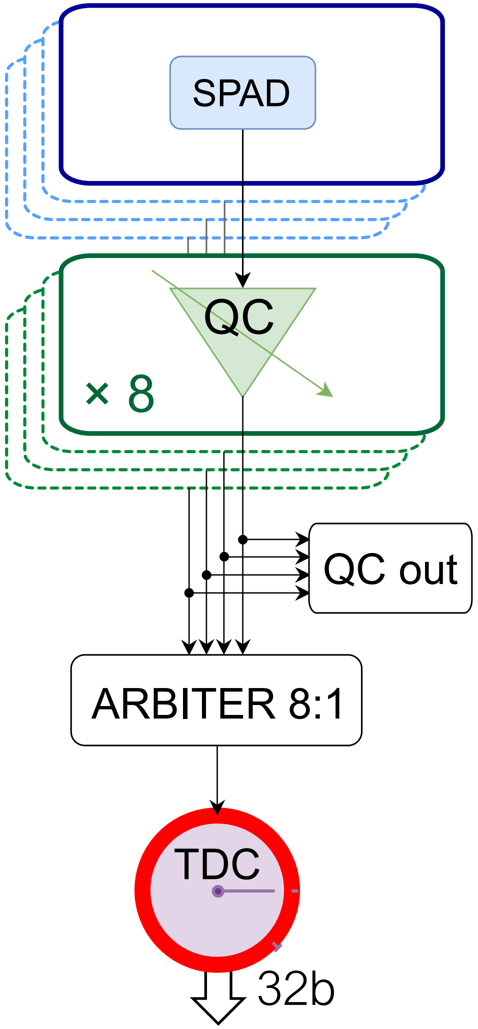

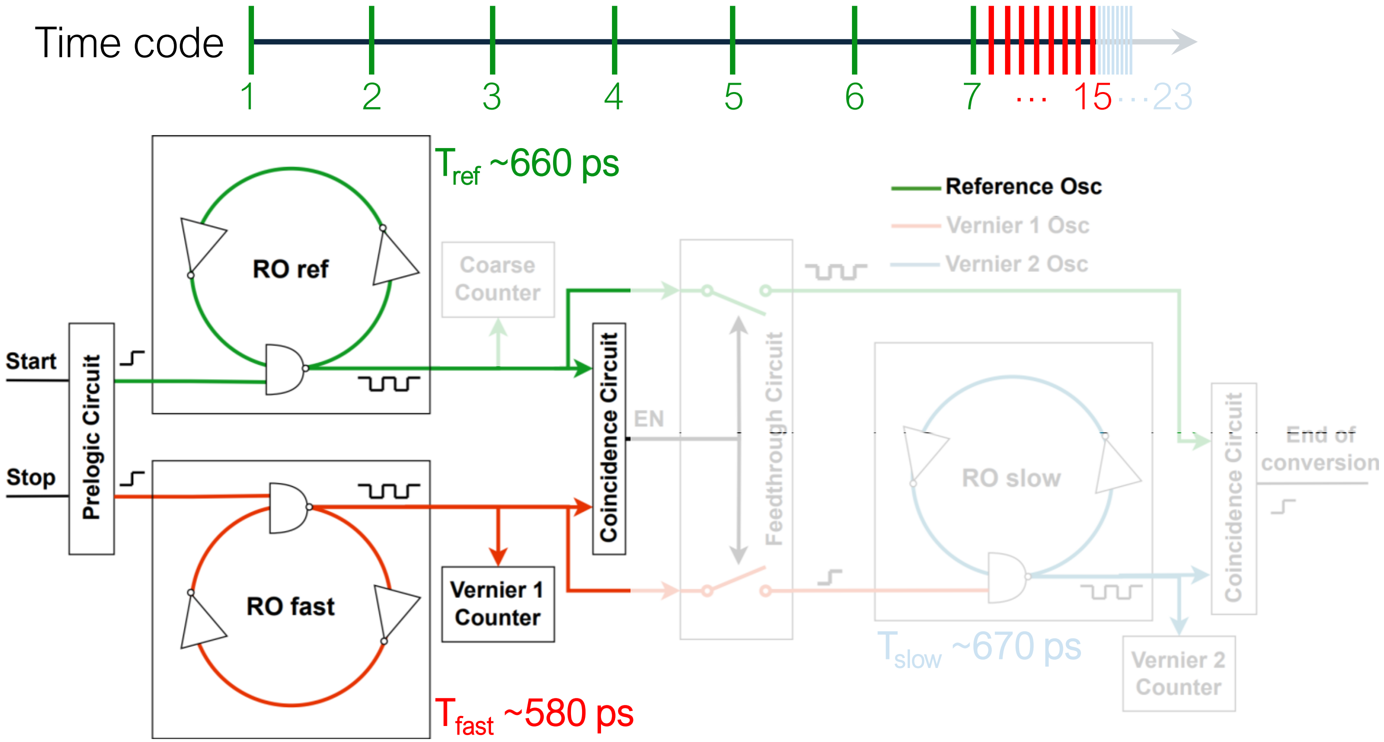

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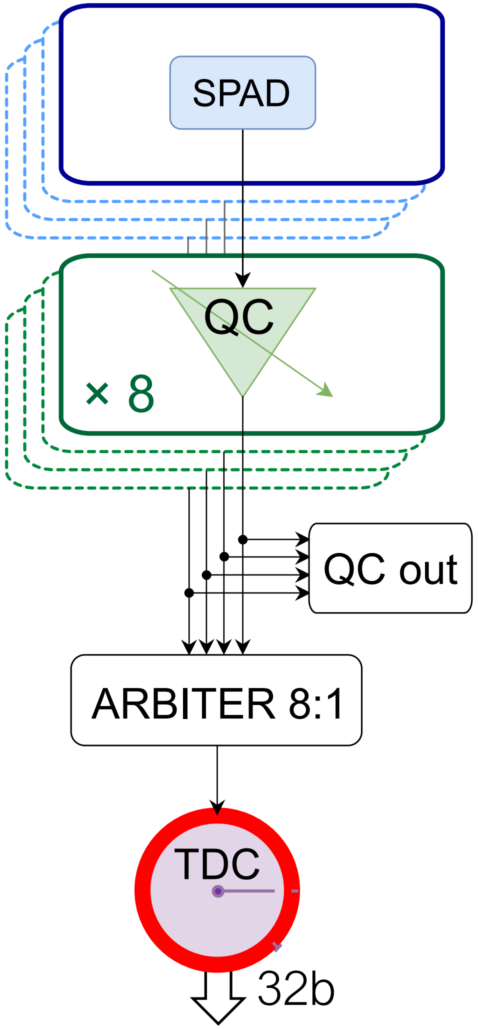

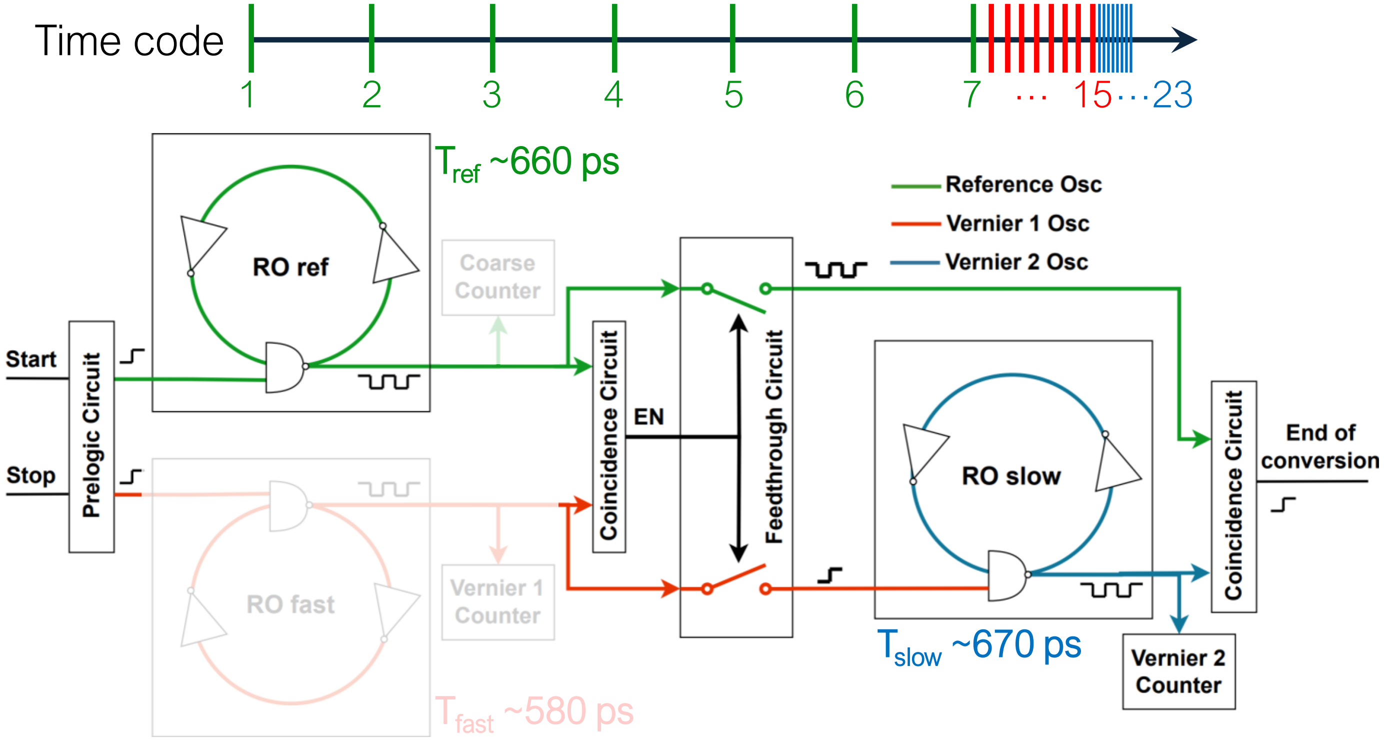

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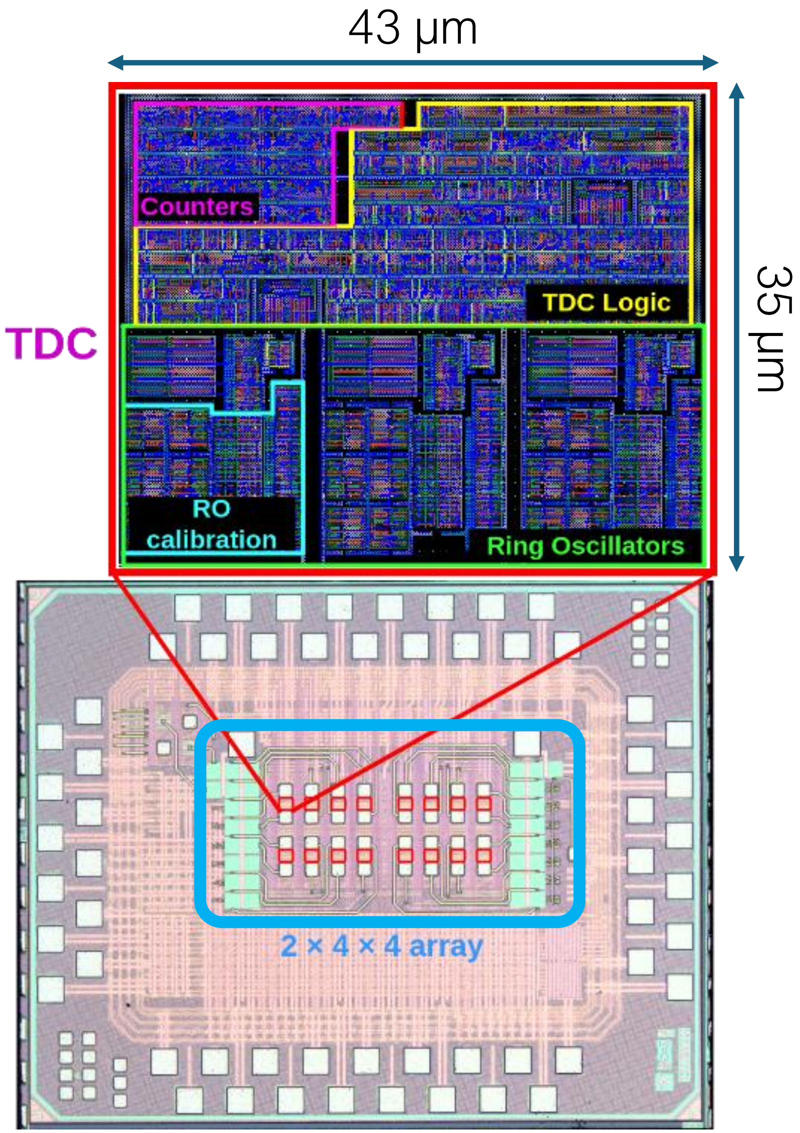
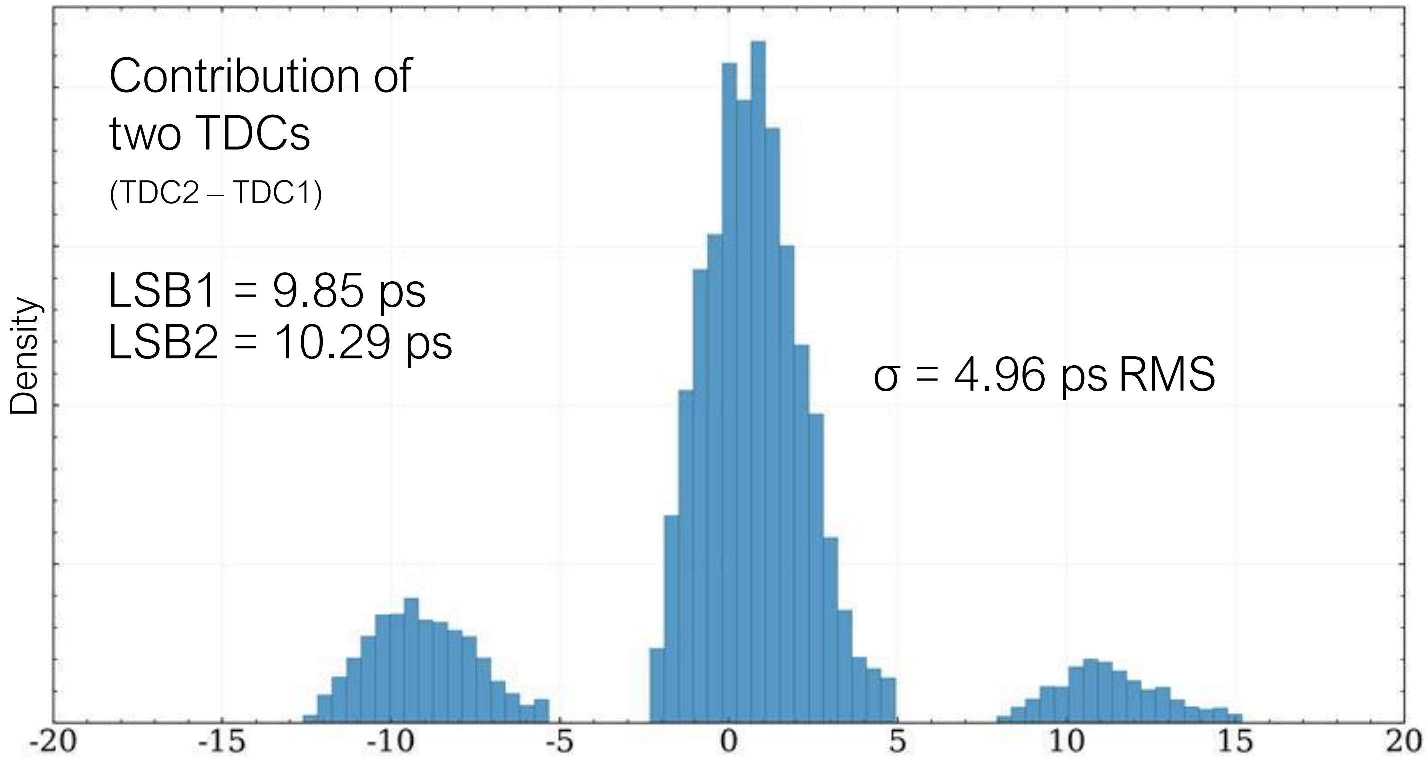
  - Digitally controlled ring oscillators (DCRO) with switched capacitors
  - Frequency counter for each ring
  - DCRO frequency registers calculated outside of the ASIC

Time-to-Digital Converter (TDC)

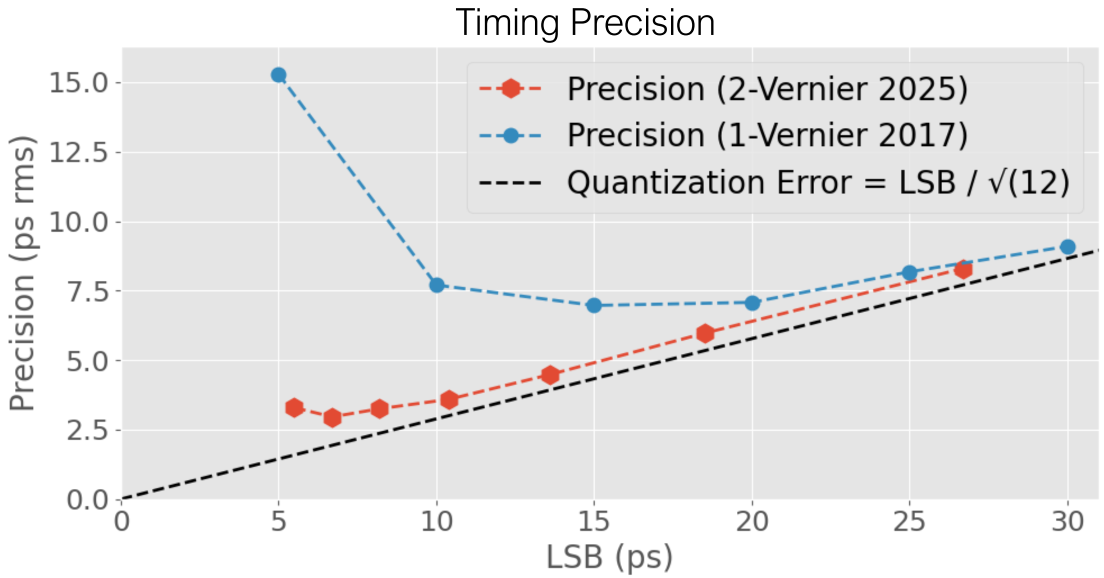
Test ASIC - 2024

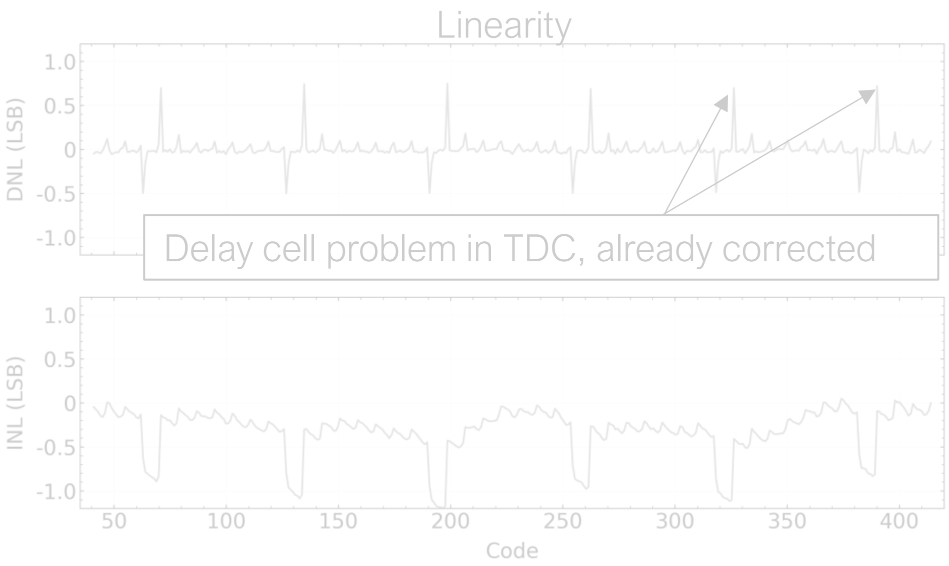




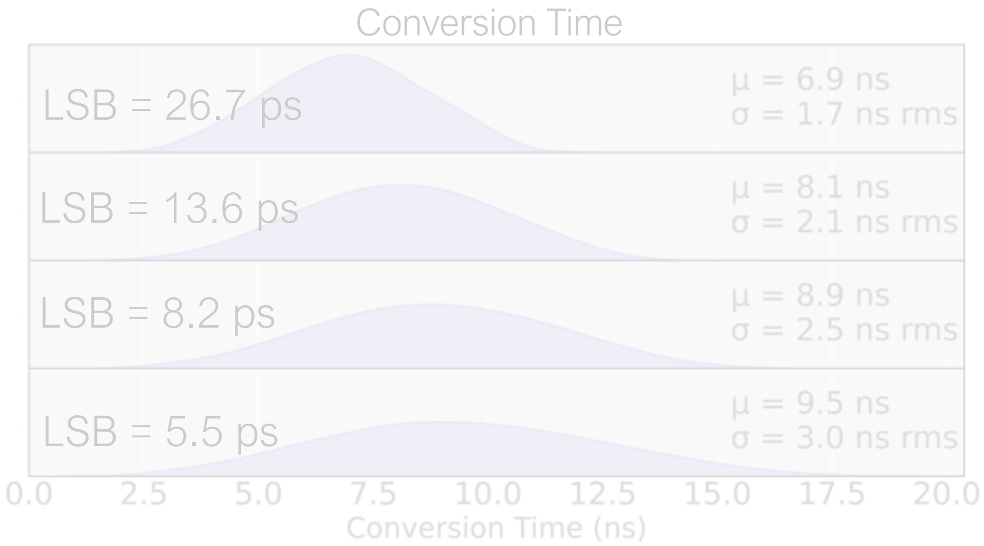
- Time code subtraction of two TDCs
- Distribution σ = 4.96 ps_{rms}
- Each TDC σ = 3.51 ps_{rms}

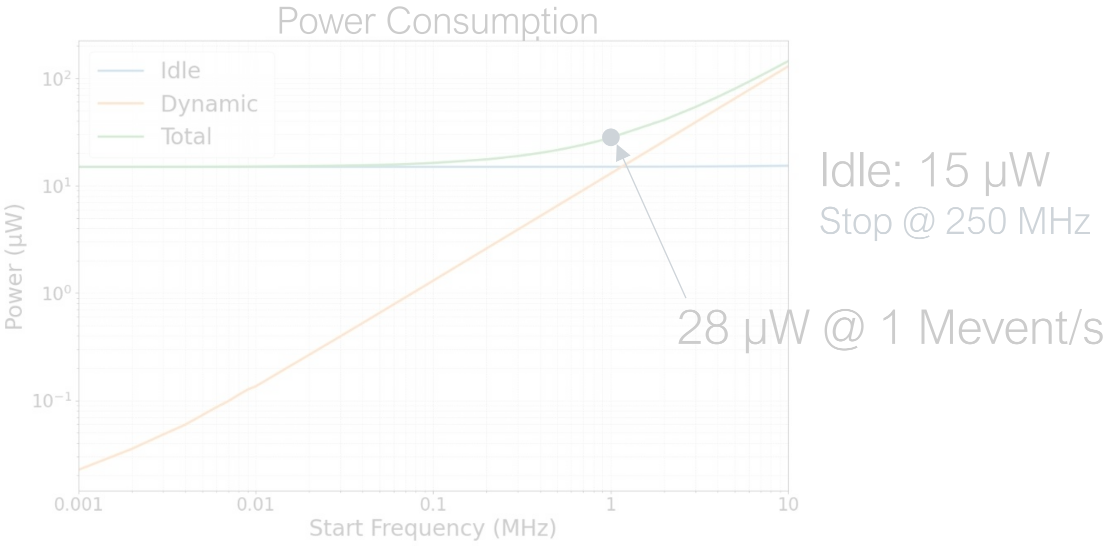
Time-to-Digital Converter (TDC)


Timing Precision


Linearity

Delay cell problem in TDC, already corrected


Conversion Time


Power Consumption

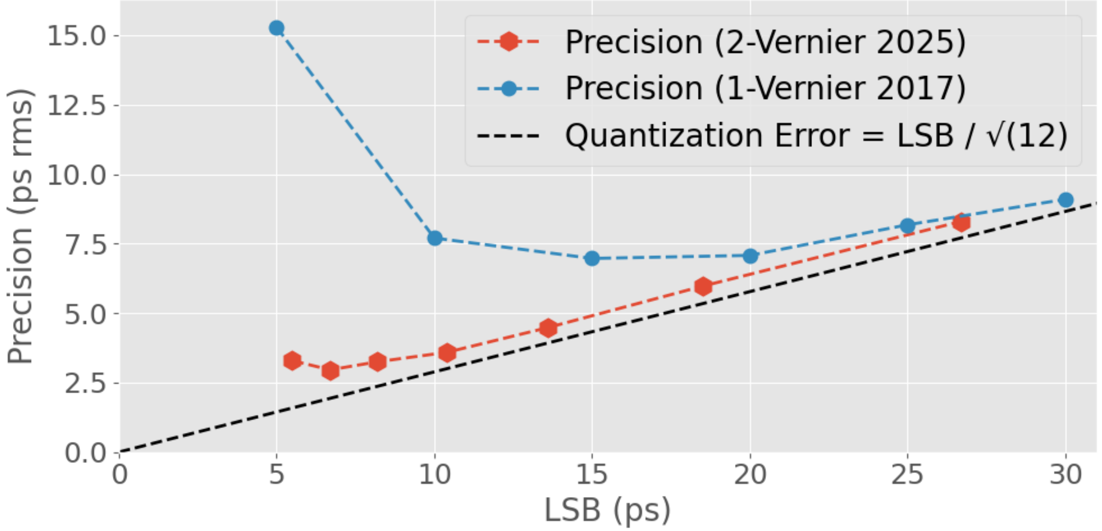
Idle: 15 µW

Stop @ 250 MHz

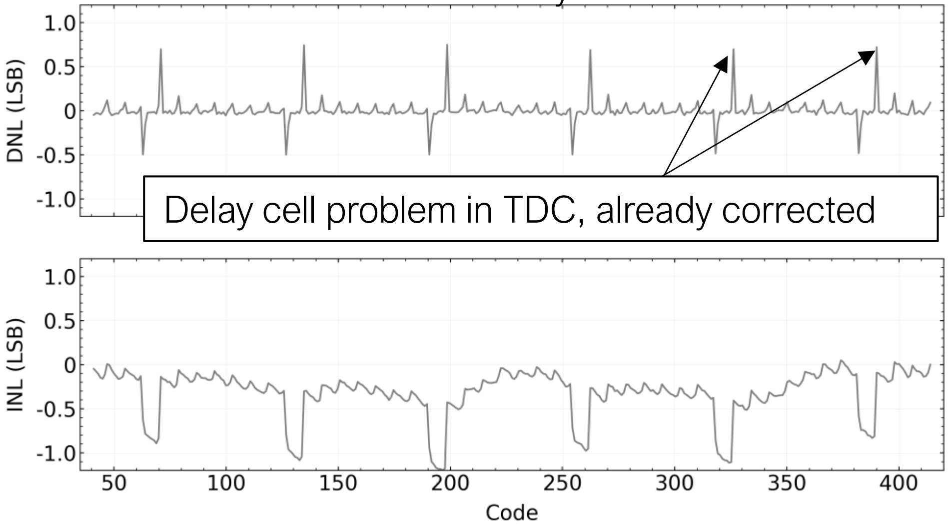
28 µW @ 1 Mevent/s

Time-to-Digital Converter (TDC)

Timing Precision

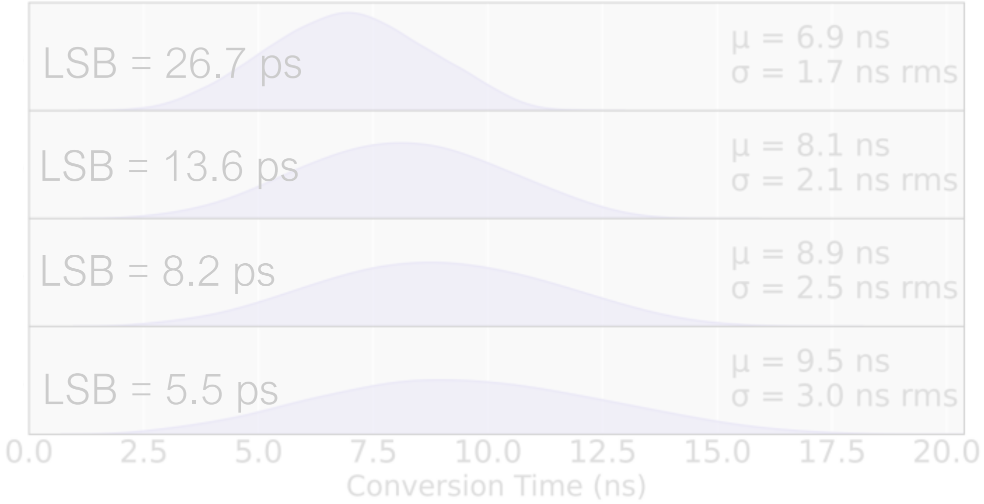


Linearity

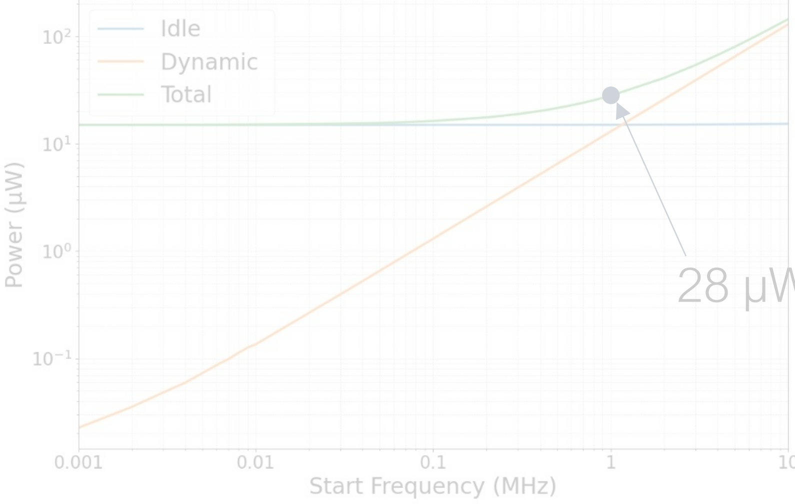


Delay cell problem in TDC, already corrected

Conversion Time



Power Consumption



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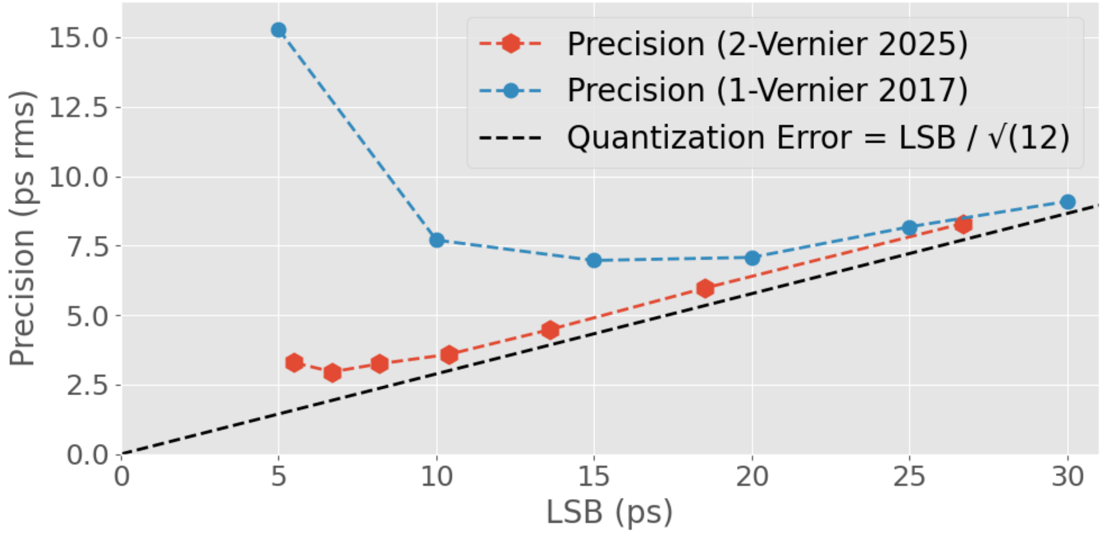
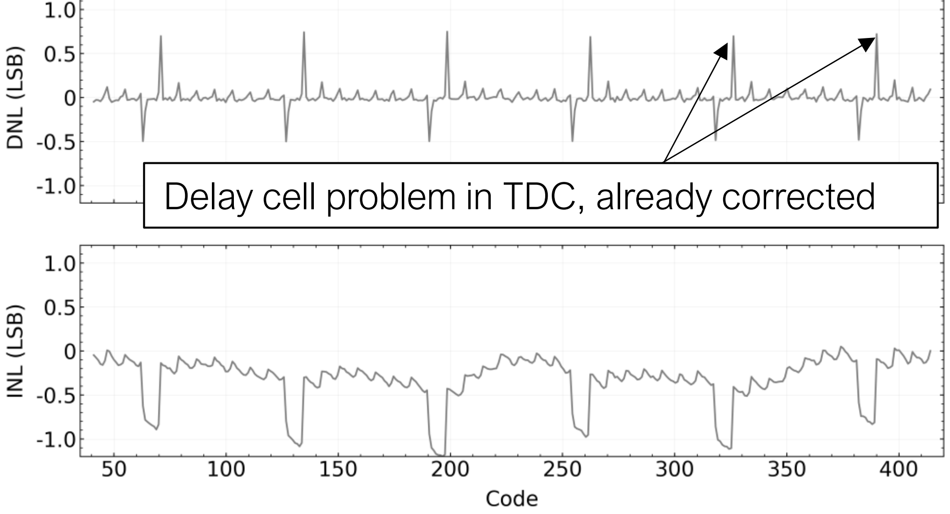

Timing Precision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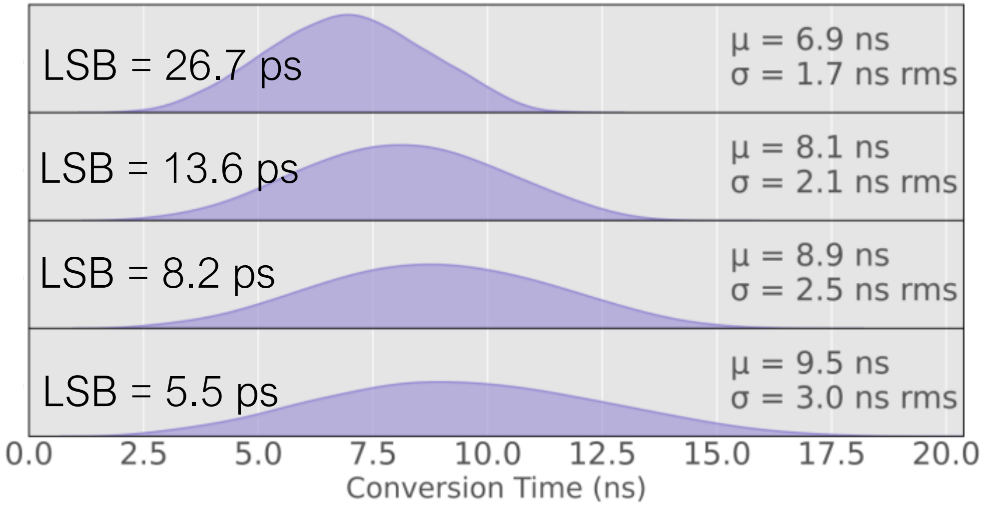
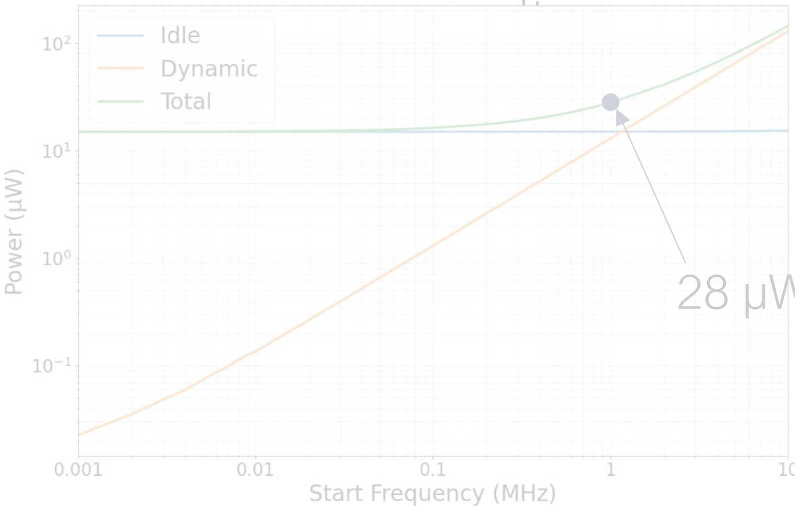

Conversion Time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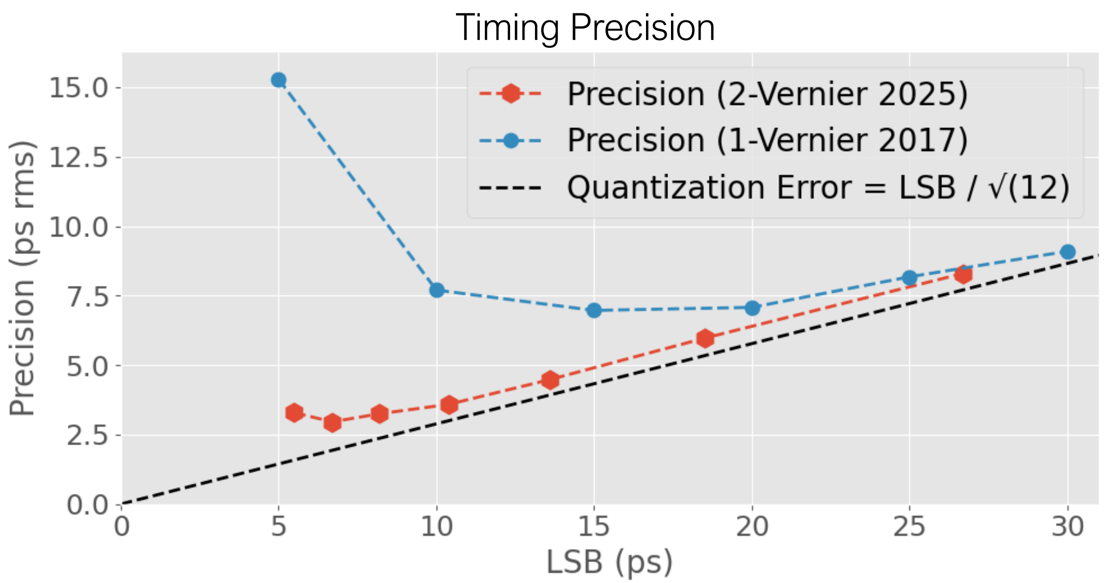
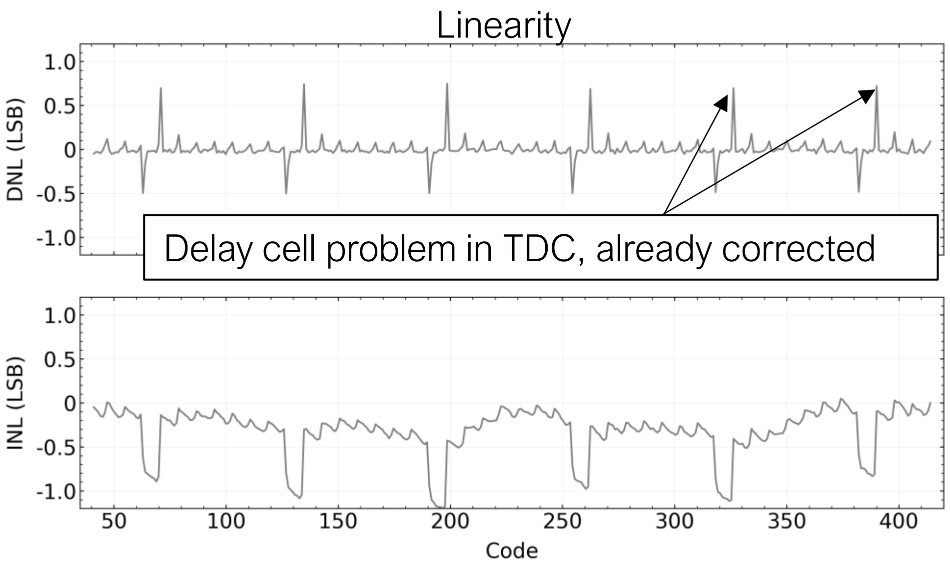
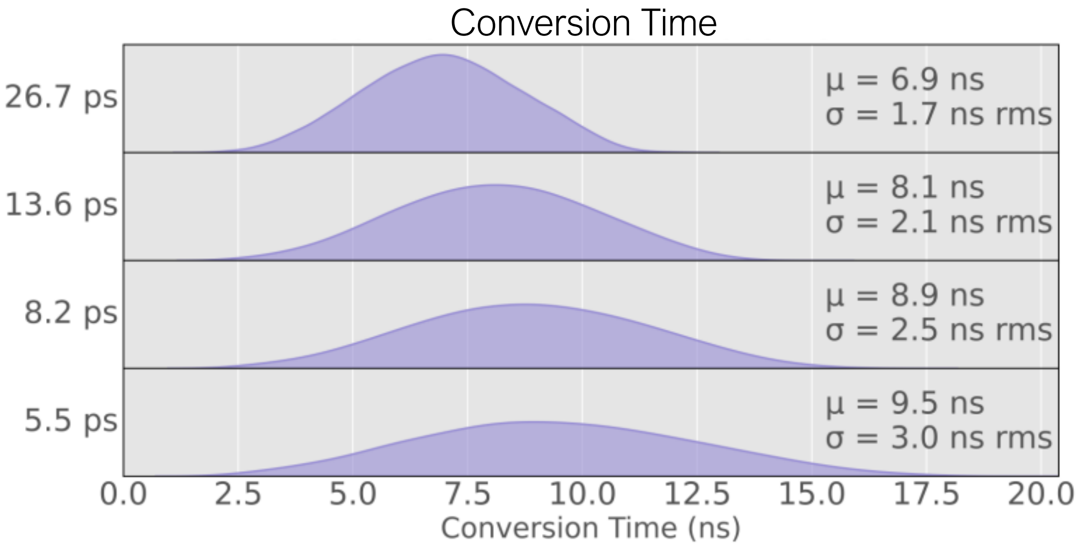
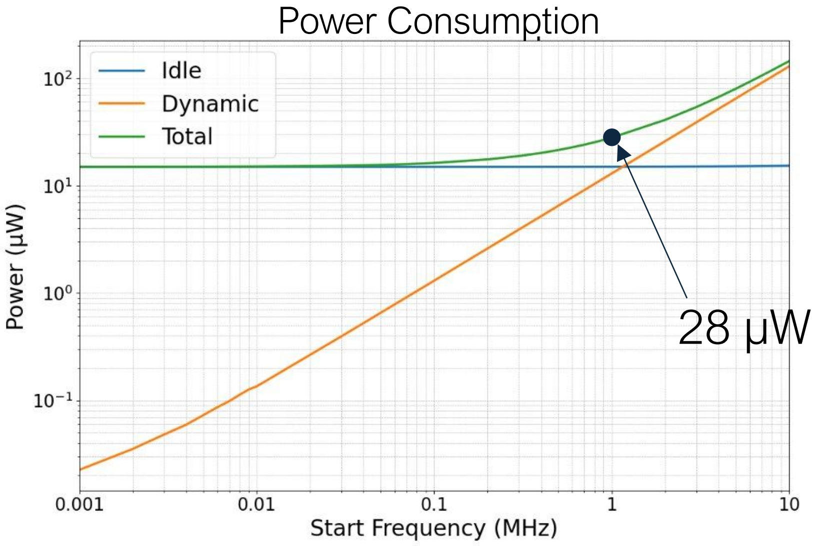
Time-to-Digital Converter (TDC)


Timing Precision


Linearity

Delay cell problem in TDC, already corrected


Conversion Time


Power Consumption

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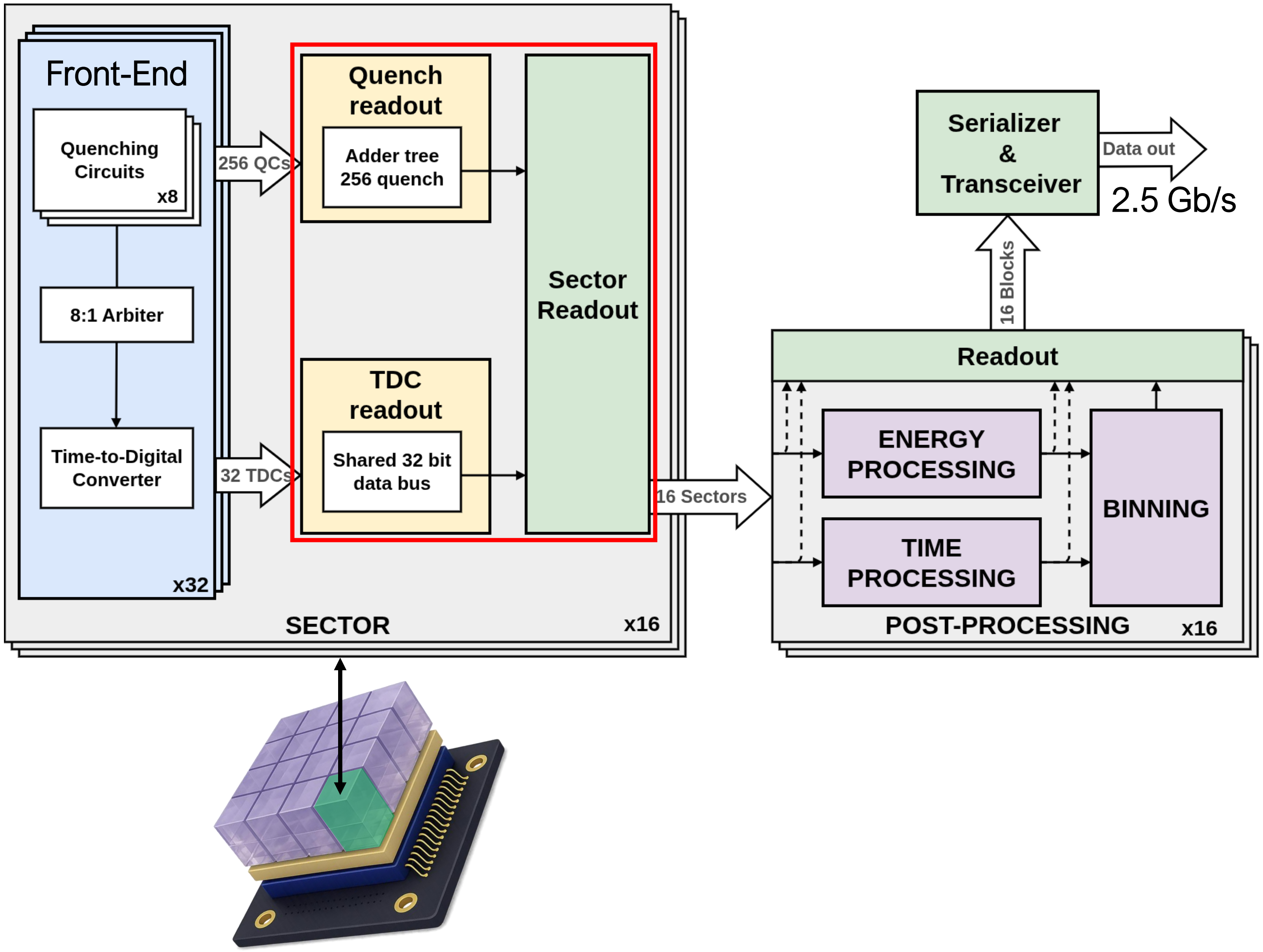
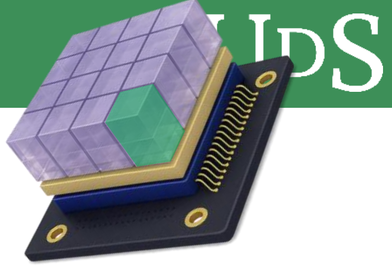
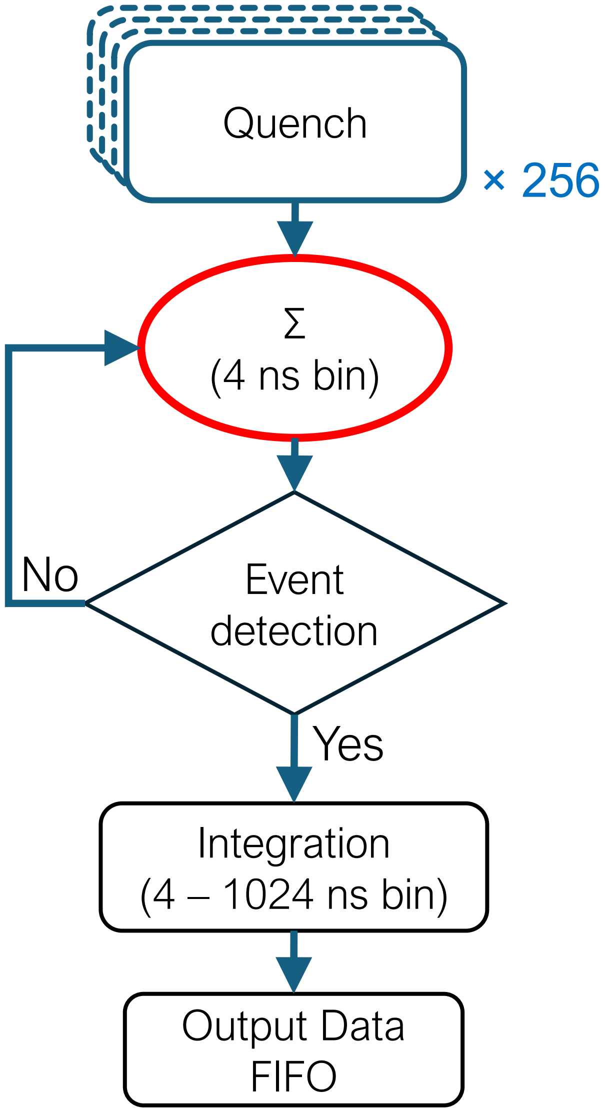
Architecture

- Front-End
  - 1 QC per SPAD
  - 1 TDC:8 SPAD
    - Skew correction
    - 12 bits of time code
    - 12 bits of global time reference (clk)
    - 8 bits of address
- Sector readout
  - Energy branch
    - Adder tree for 256 SPADs
    - Programmable event detection
  - Timing branch
    - Shared data bus readout for 32 TDCs
- Post-processing
  - Time-code sorting
  - Energy and timing histogram
  - Best linear unbiased estimator (BLUE)



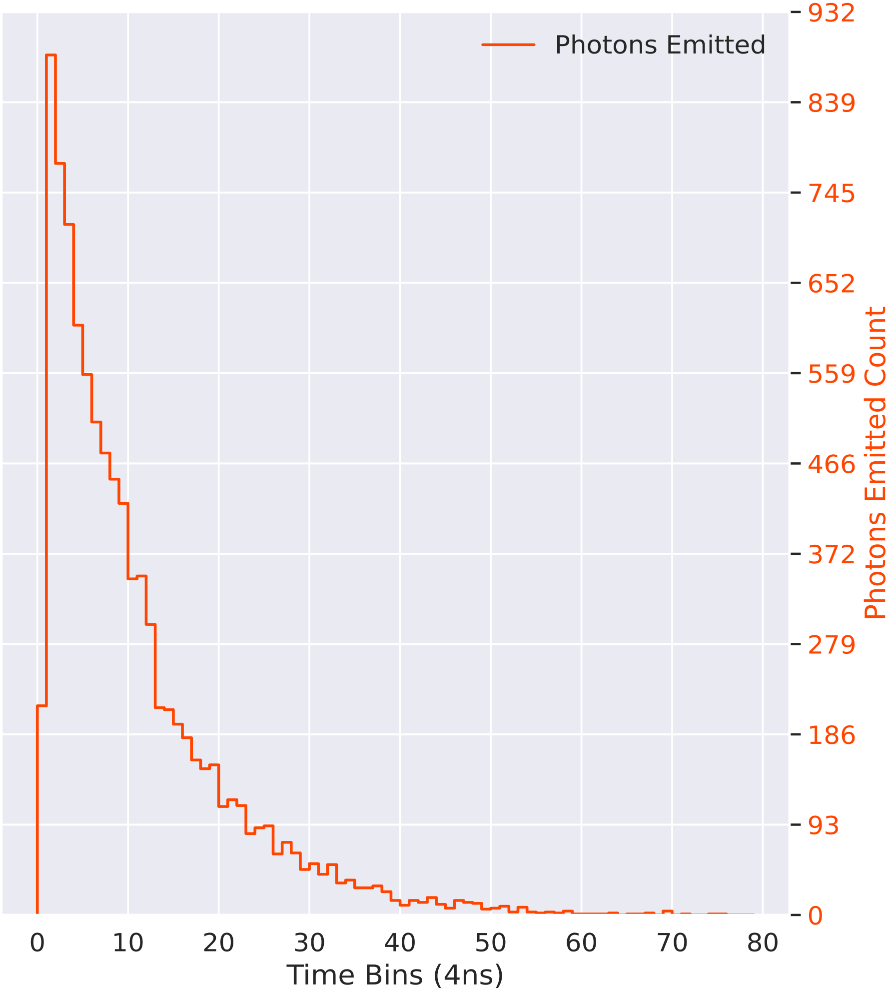
Energy Branch with Digital Sum




Quench
× 256
Σ
(4 ns bin)
No
Event detection
Yes
Integration
(4 – 1024 ns bin)
Output Data FIFO

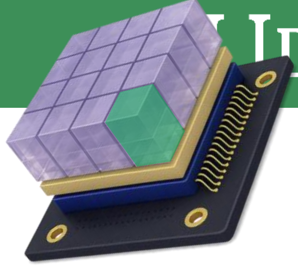
Digital Sum Features:

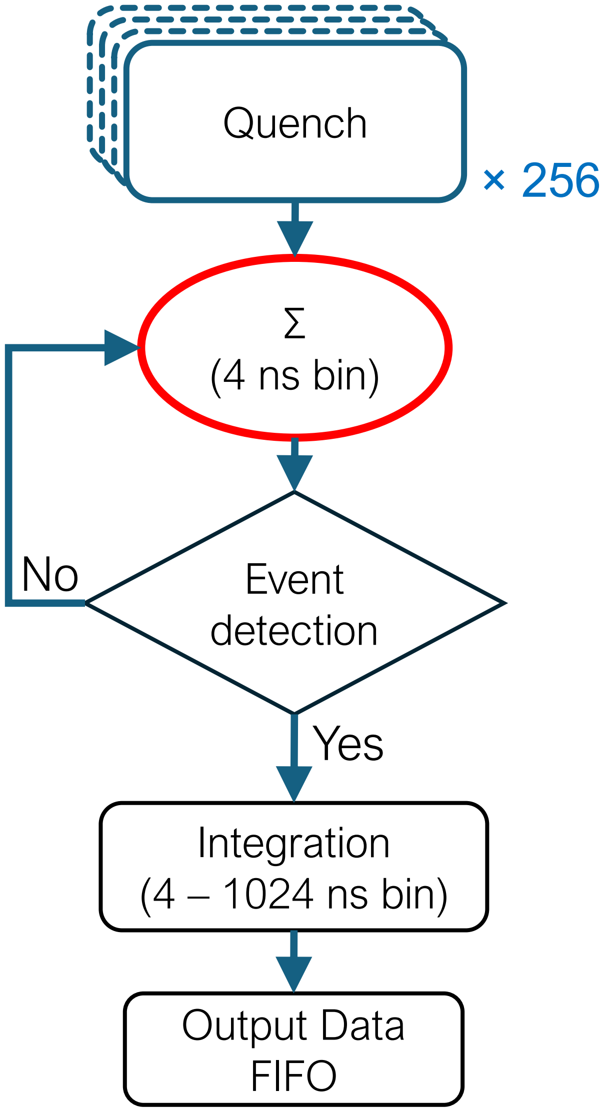
- Digital sum with a **4 ns sampling rate**
- Sum the number of quenching circuits:
  - Fired within a 4 ns window
- Event detection referenced to system clock global count;
  - Programmable threshold and hysteresis
- Sum integration
  - Configurable integration period
  - Configurable number of bins
- Output:
  - Energy bins integrated over N × 4 ns



GEANT4 + DSAS + Digital Simulation results

Energy Branch with Digital Sum





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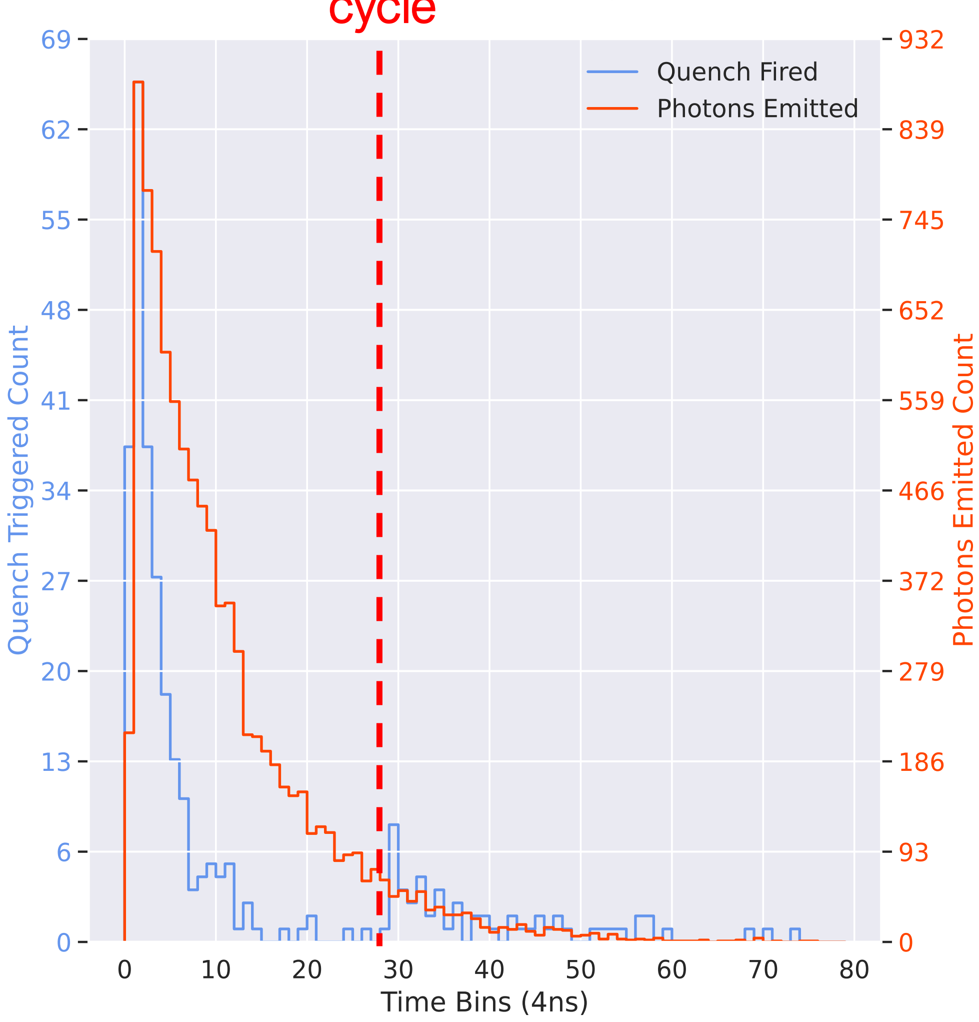
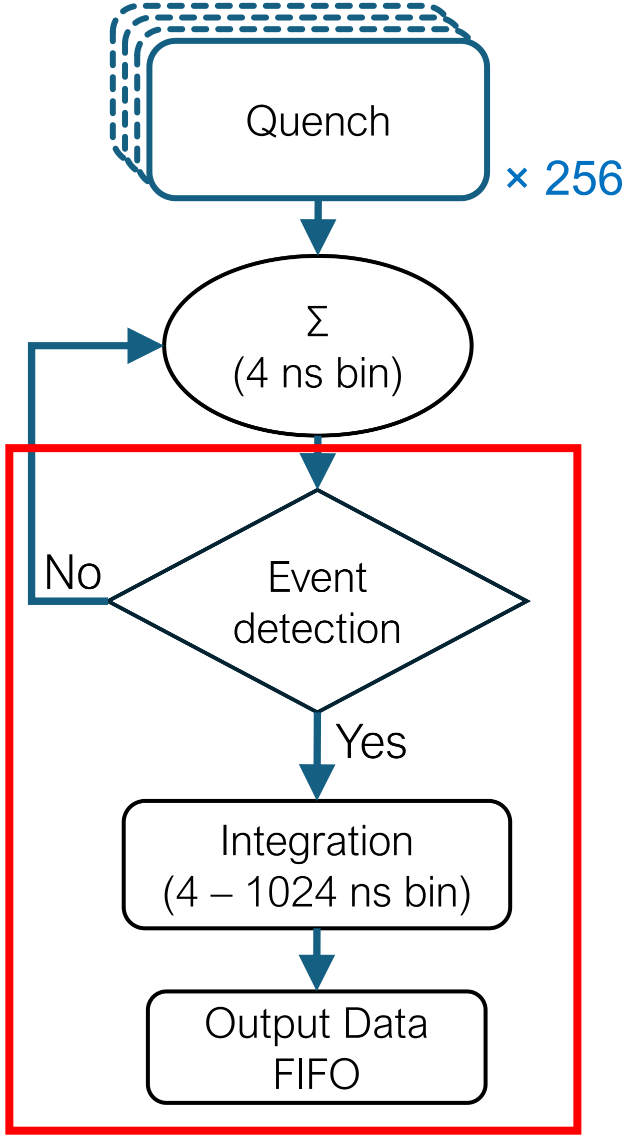


GEANT4 + DSAS + Digital Simulation results

Energy Branch with Digital Sum



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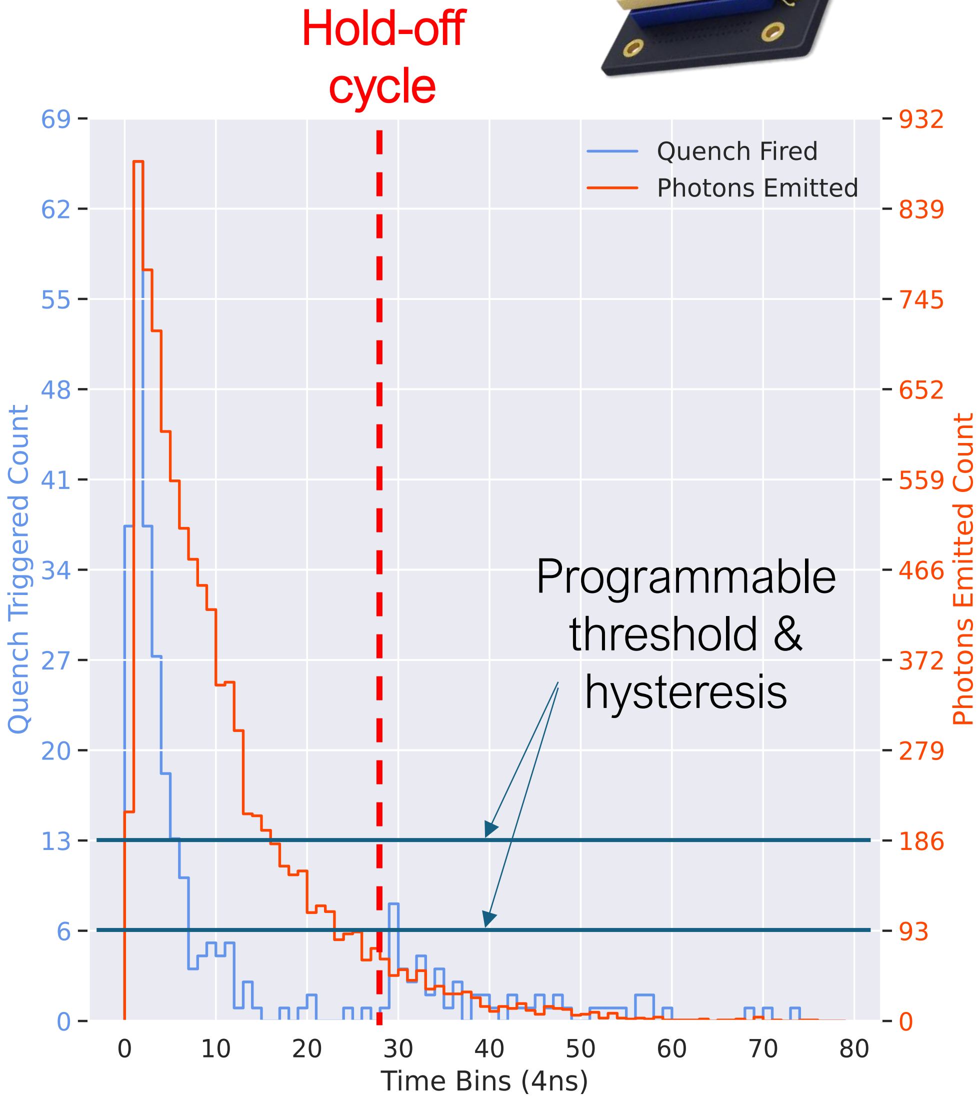

GEANT4 + DSAS + Digital Simulation results

Architecture

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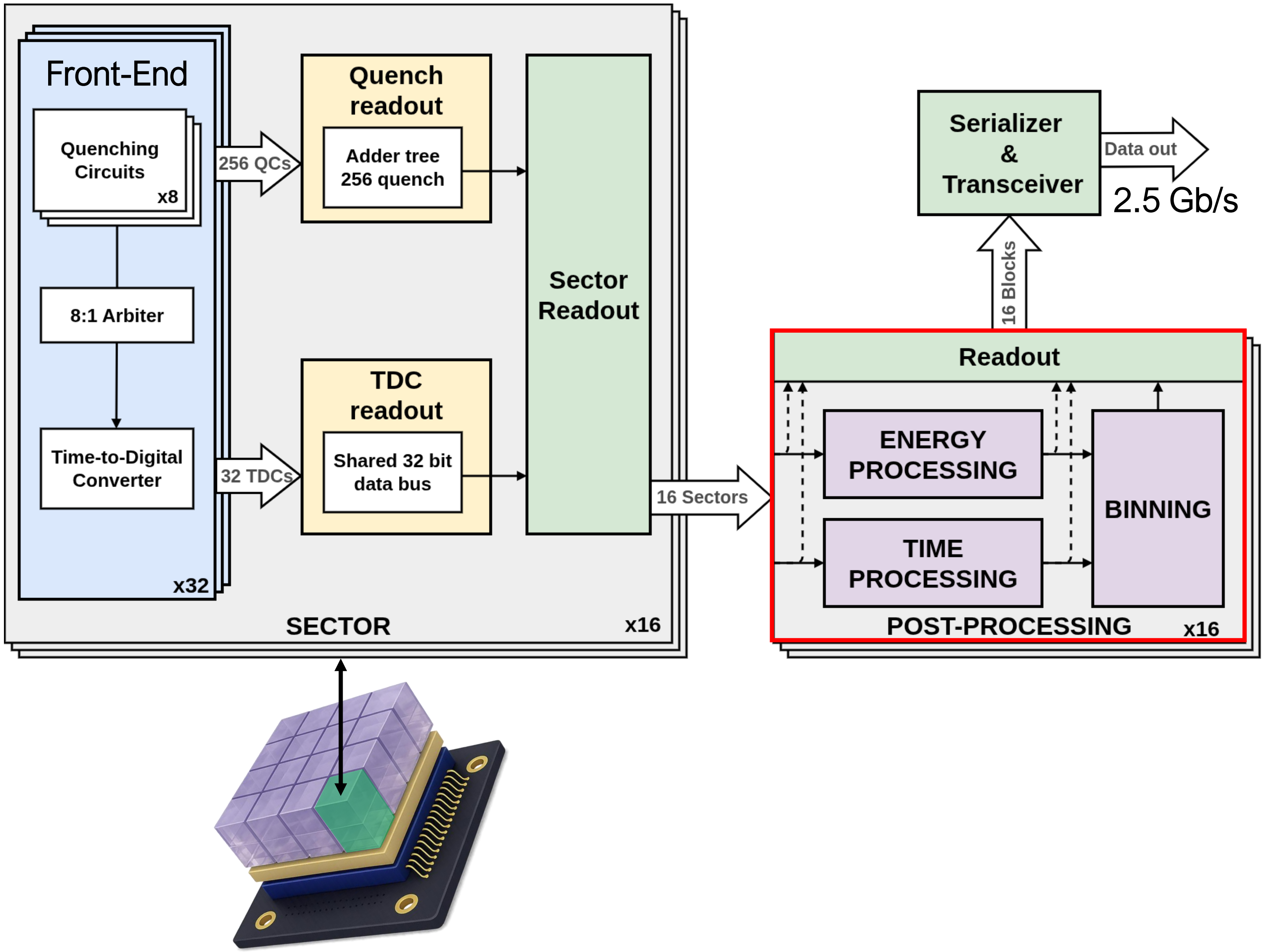


Front-End

Quenching Circuits

x8

8:1 Arbiter

Time-to-Digital Converter

x32

256 QCs

32 TDCs

Quench readout

Adder tree 256 quench

TDC readout

Shared 32 bit data bus

Sector Readout

SECTOR

x16

16 Sectors

Readout

ENERGY PROCESSING

TIME PROCESSING

BINNING

POST-PROCESSING

x16

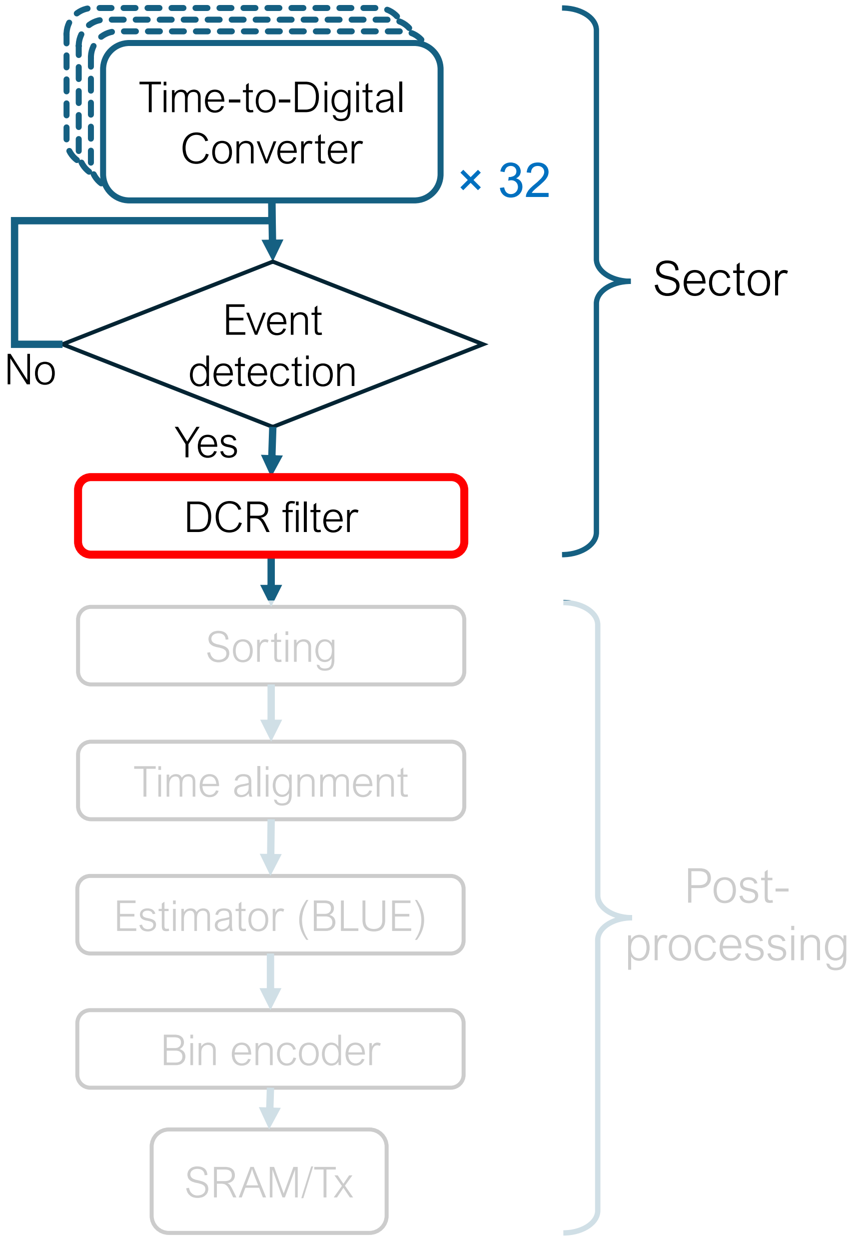
16 Blocks

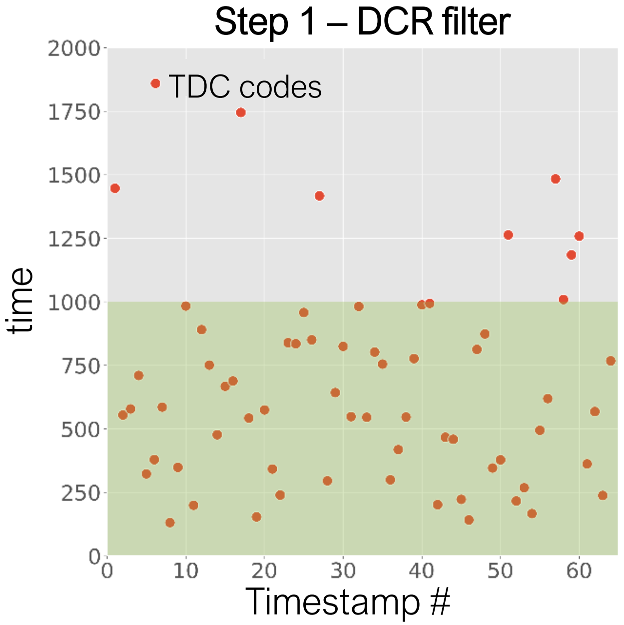
Serializer & Transceiver

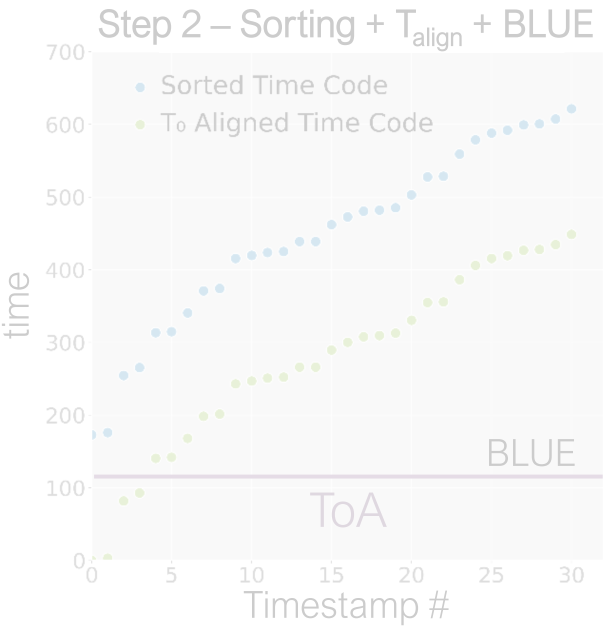
Data out

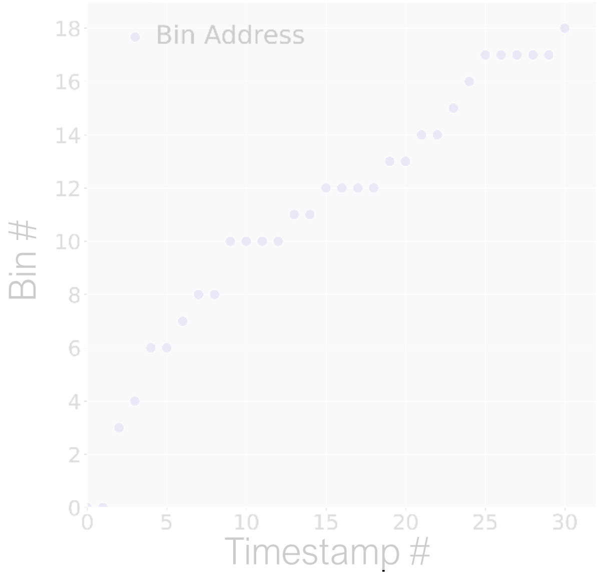
2.5 Gb/s

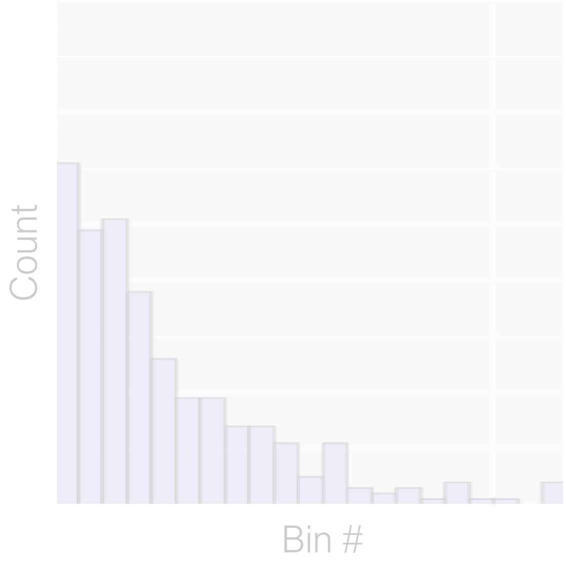
Timestamp management (event driven mode)



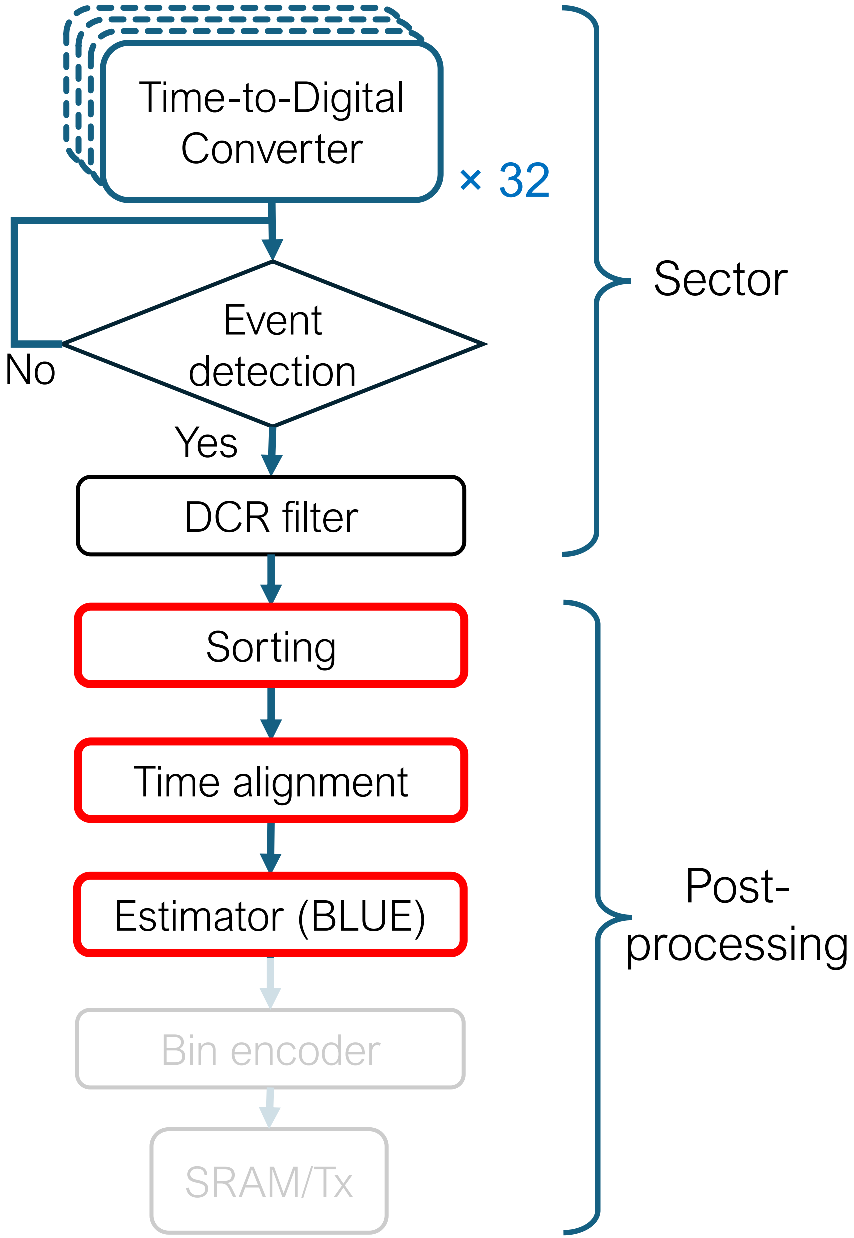

Step 1 – DCR filter


Step 2 – Sorting + T_{align} + BLUE


Step 3 – Bin encoder


Step 4 – Histogram

Timestamp management (event driven mode)



Time-to-Digital Converter

× 32

Event detection

No

Yes

DCR filter

Sorting

Time alignment

Estimator (BLUE)

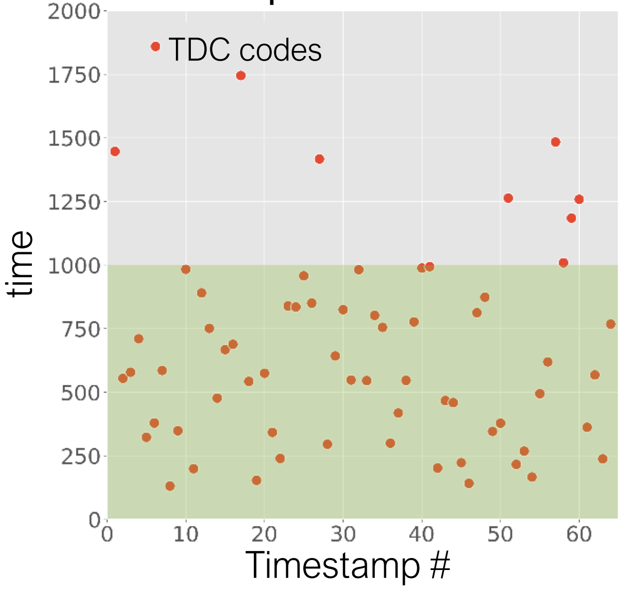
Bin encoder

SRAM/Tx

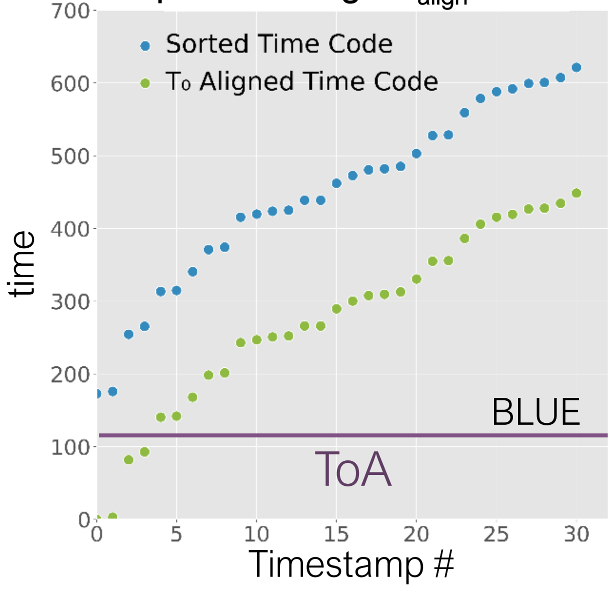
Sector

Post-processing

Step 1 – DCR filter



Step 2 – Sorting + T_{align} + BLUE



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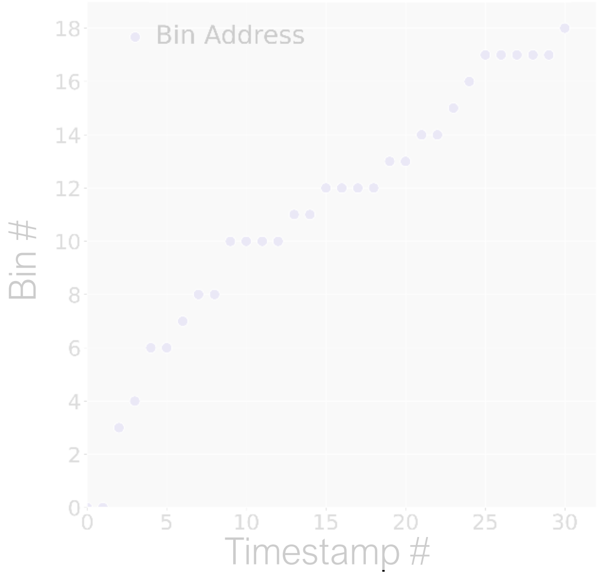

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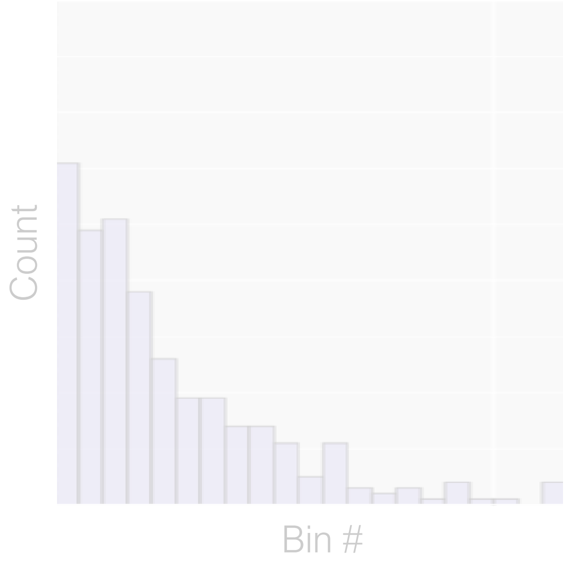
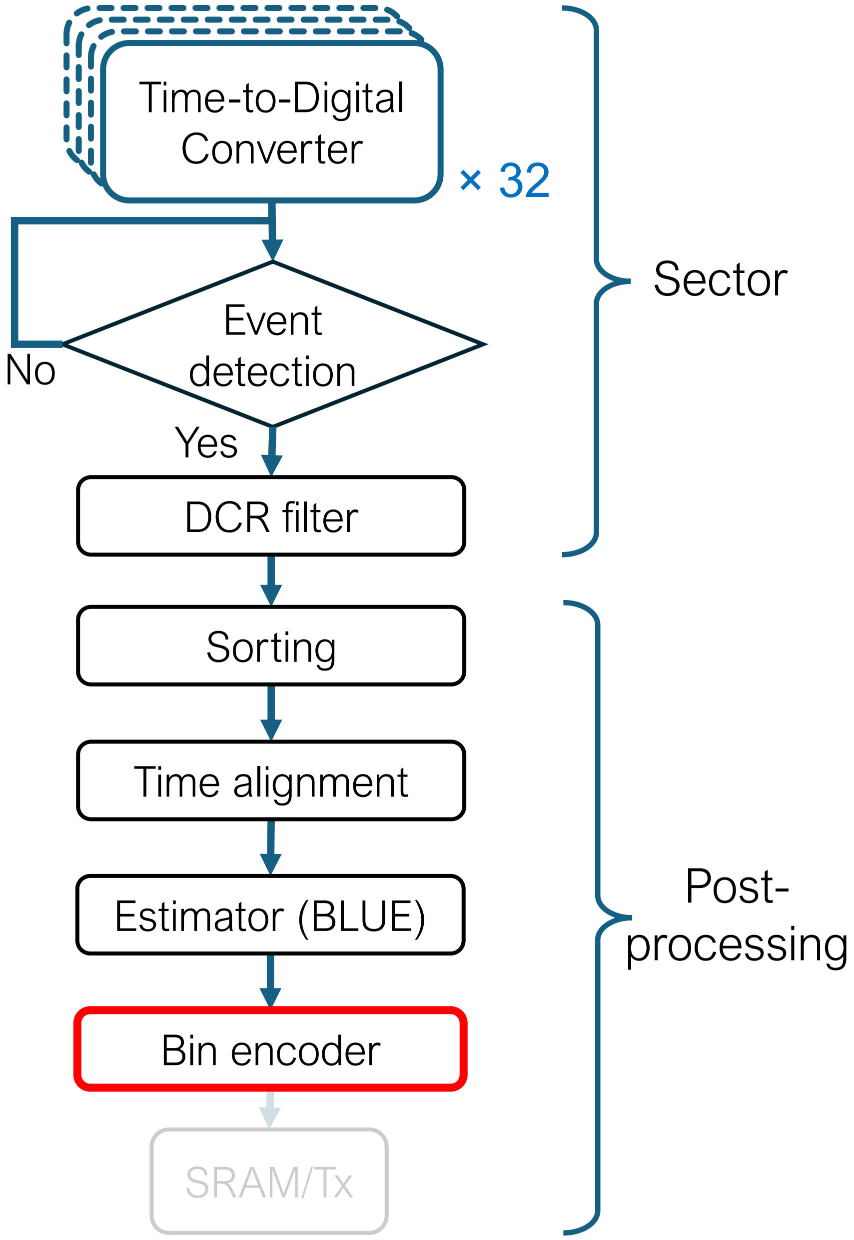


Timestamp management (event driven mode)



Time-to-Digital Converter

× 32

Event detection

No

Yes

DCR filter

Sector

Sorting

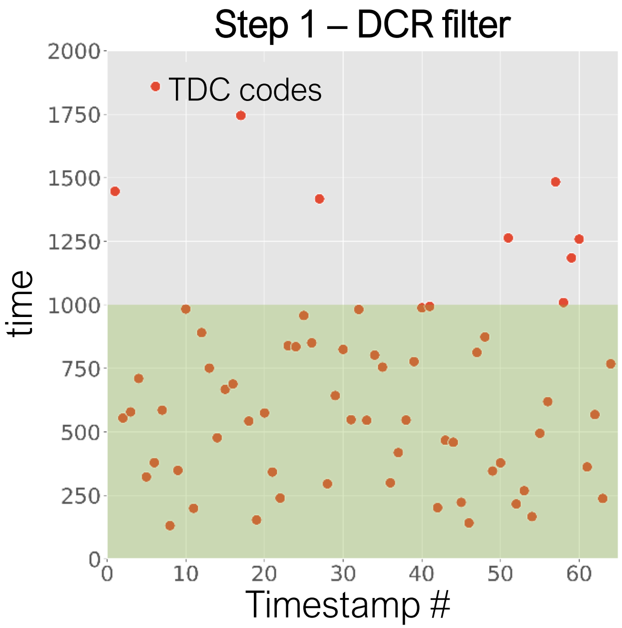
Time alignment

Estimator (BLUE)

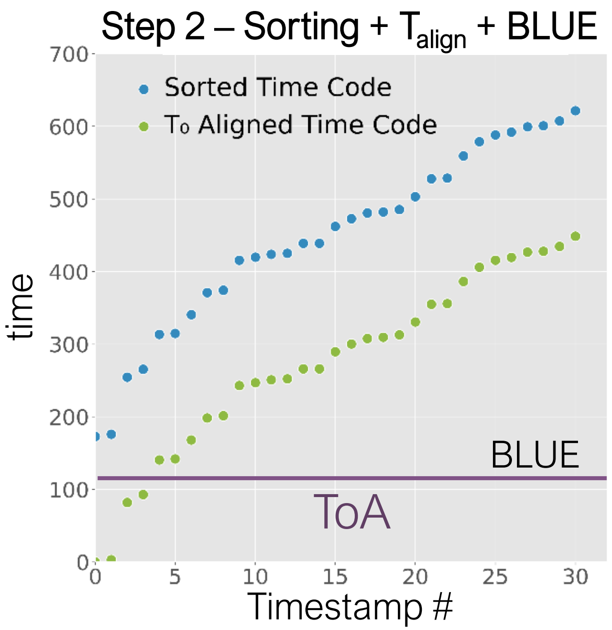
Bin encoder

SRAM/Tx

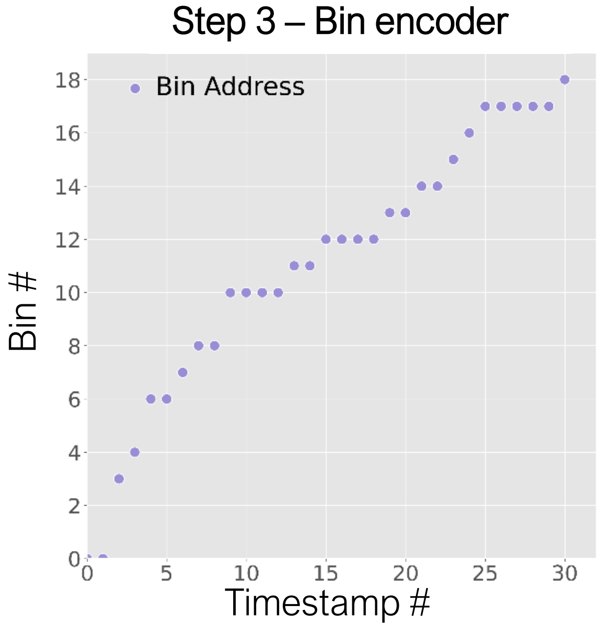
Post-processing



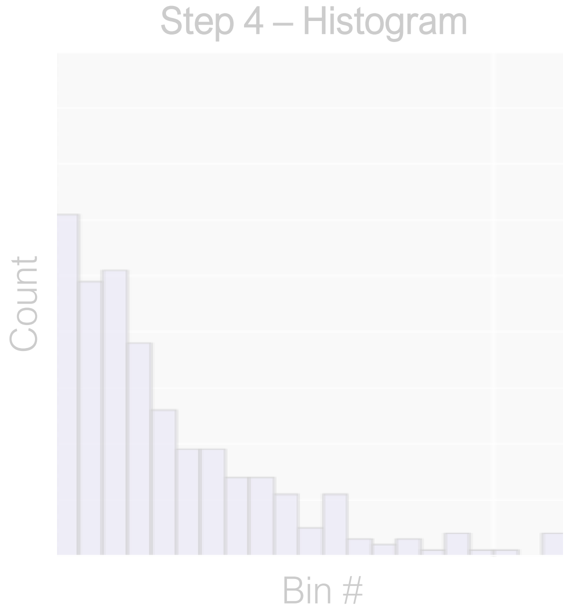
Step 1 – DCR filter



Step 2 – Sorting + T_{align} + BLUE

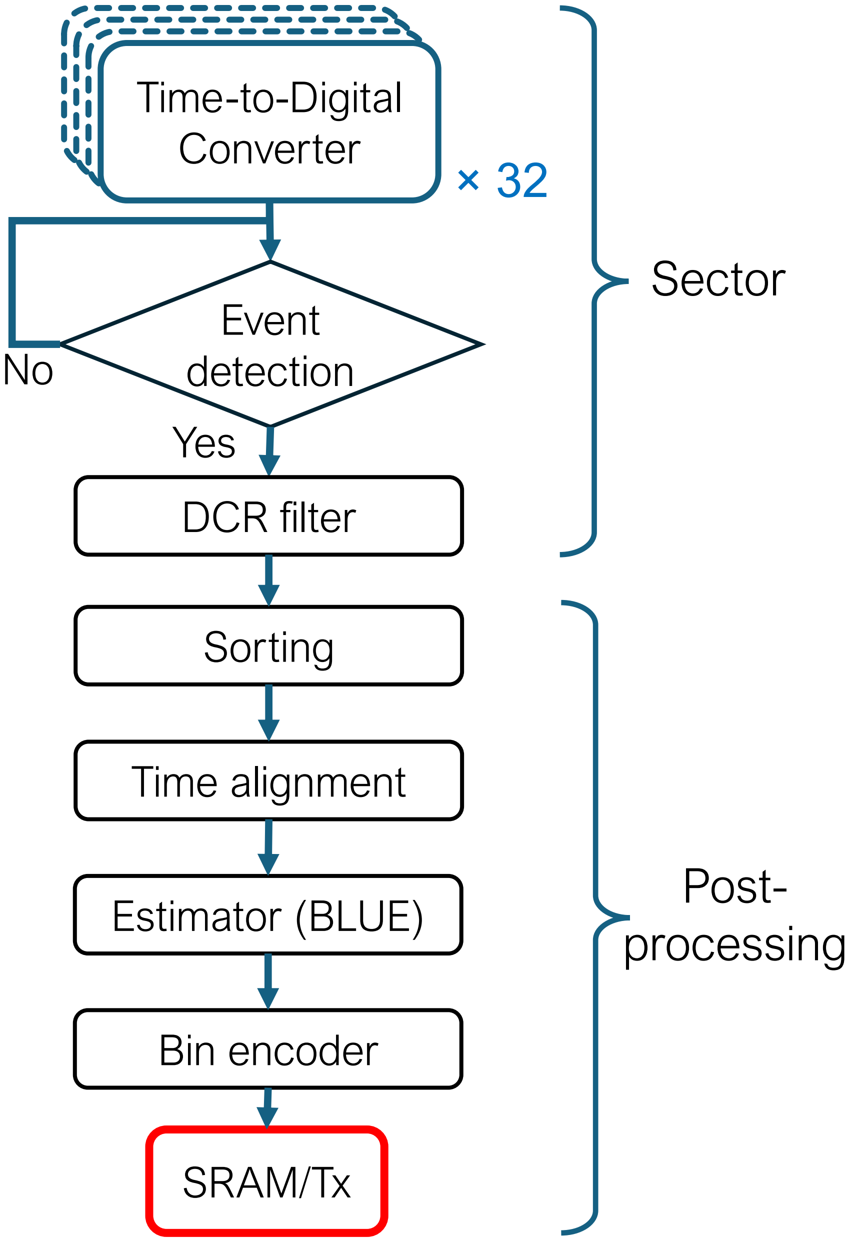


Step 3 – Bin encoder



Step 4 – Histogram

Timestamp management (event driven mode)



Time-to-Digital Converter × 32

Event detection

No

Yes

DCR filter

Sector

Sorting

Time alignment

Estimator (BLUE)

Bin encoder

SRAM/Tx

Post-processing

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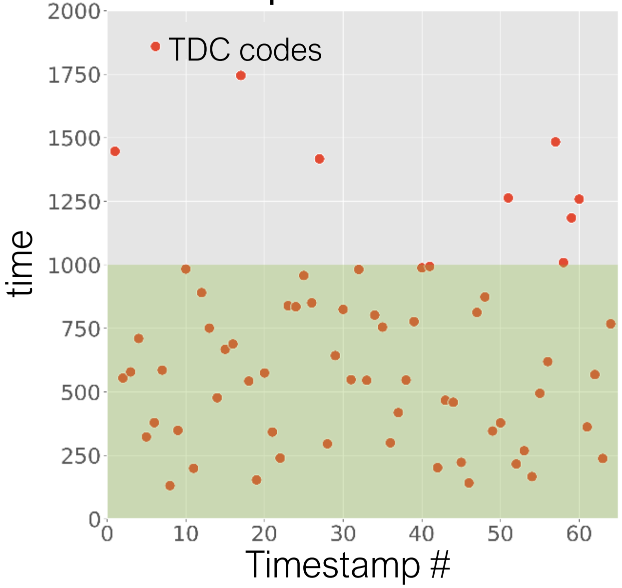

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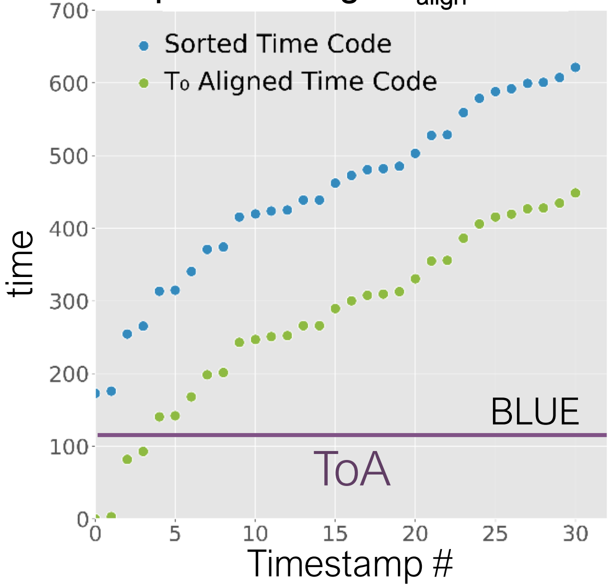

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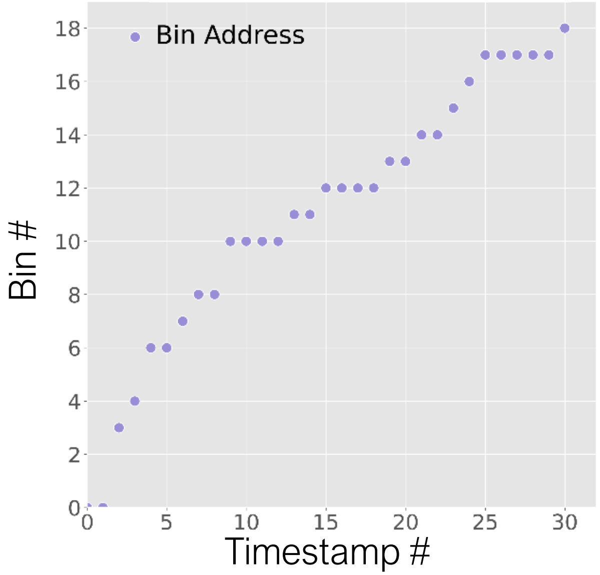

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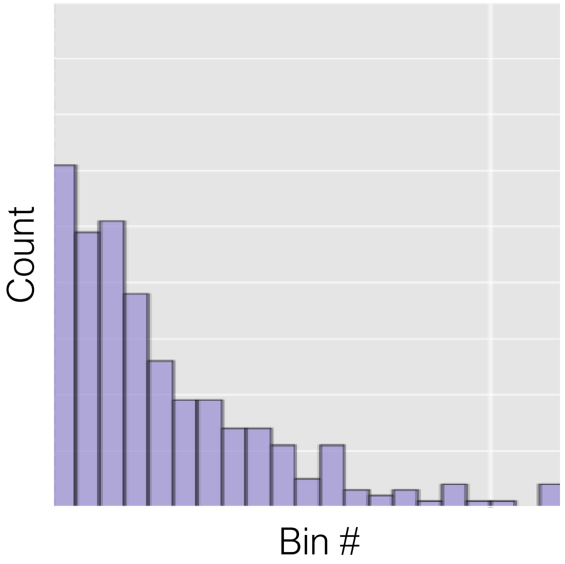
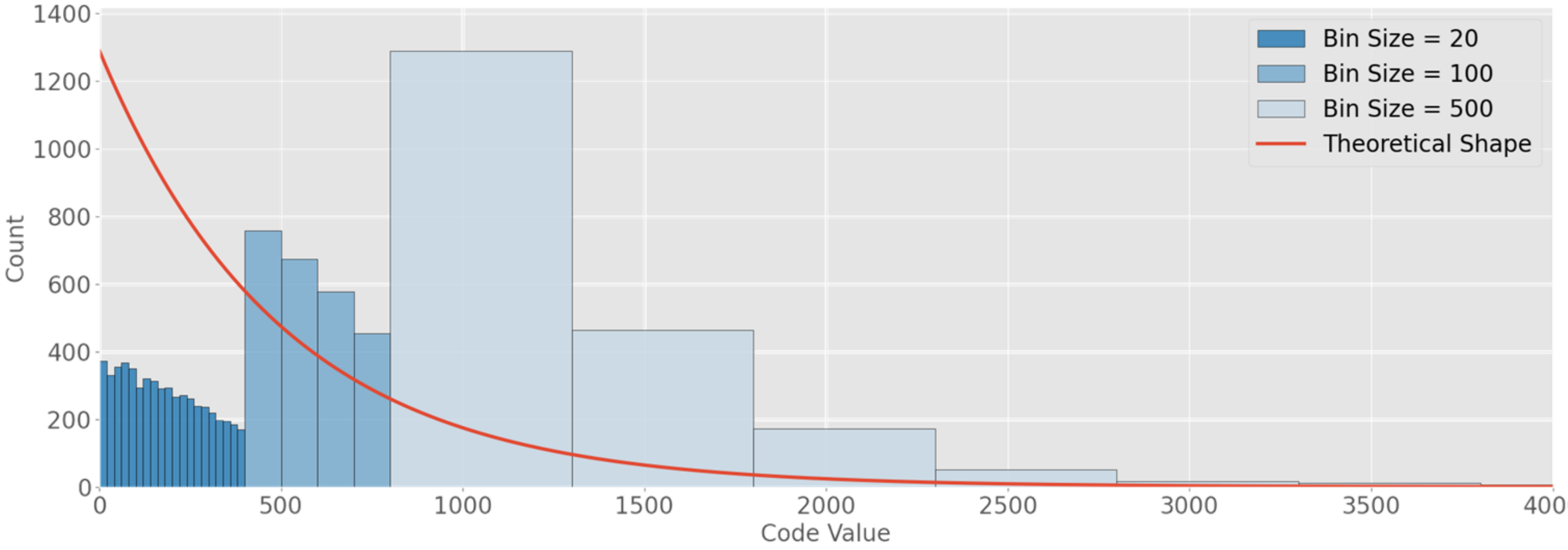
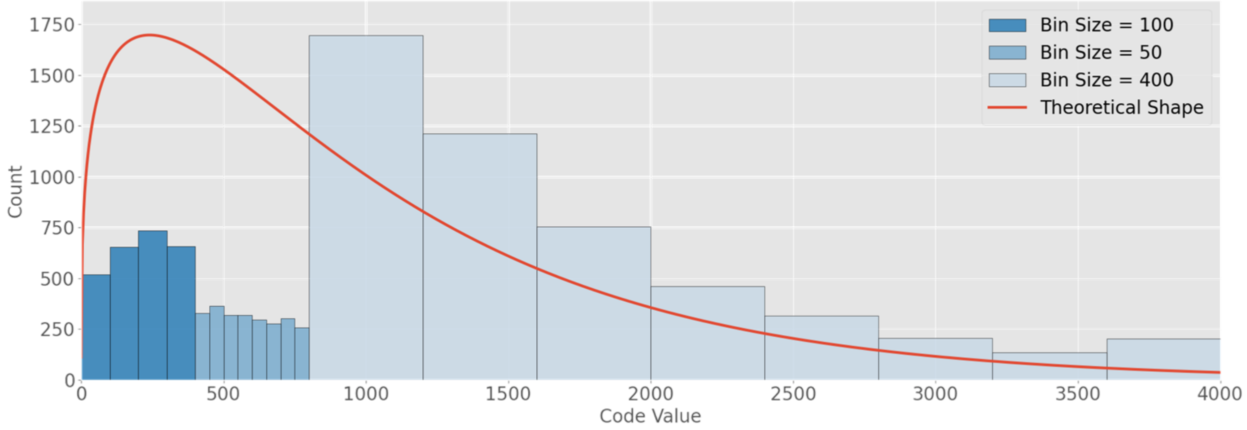


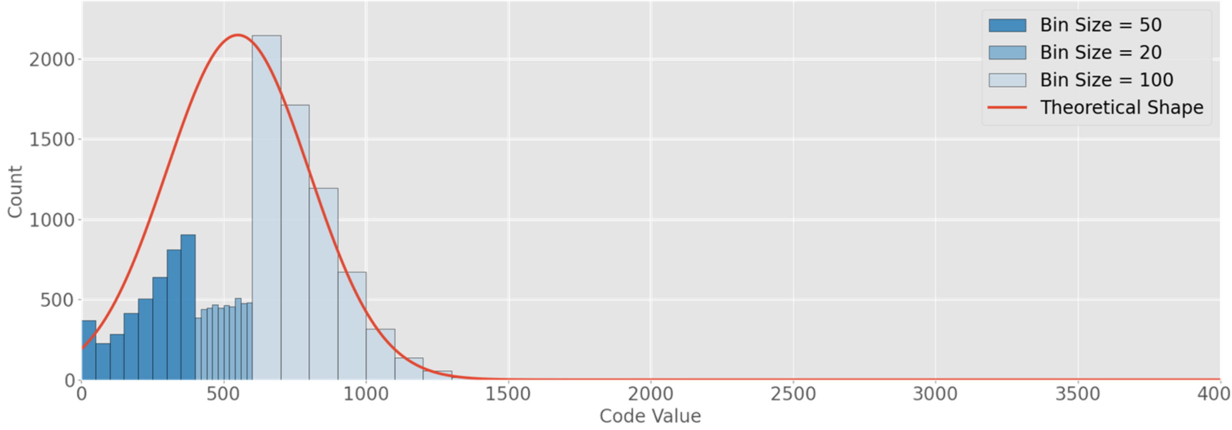
Timestamp binning

Timestamp binning features:

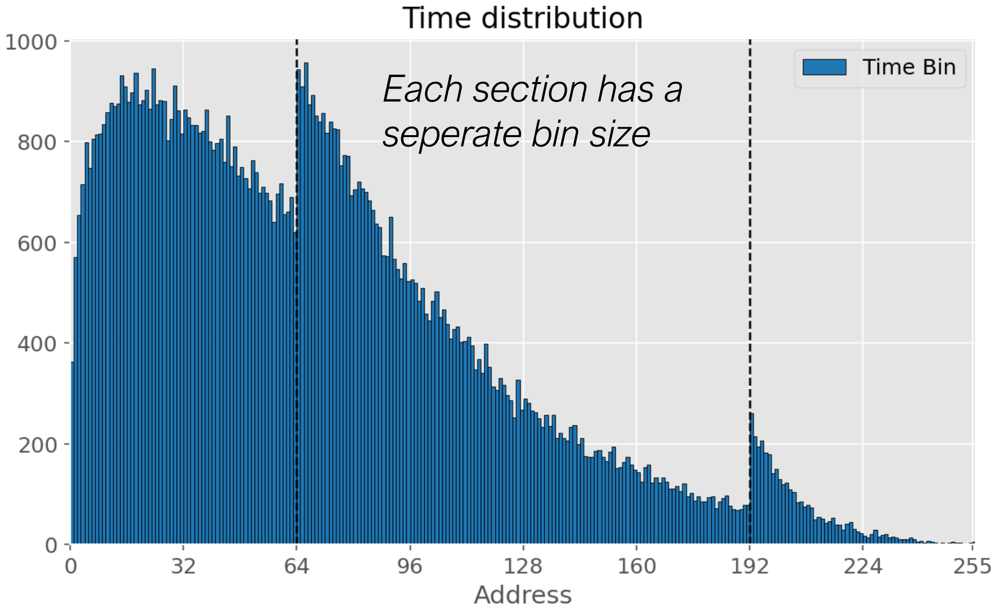
- ○ Binning to enable data compression
- ○ Bin sizes are configurable
- ○ Bins are grouped by size
- ○ Up to 4 bin sizes
- ○ 256 bins per sector maximum

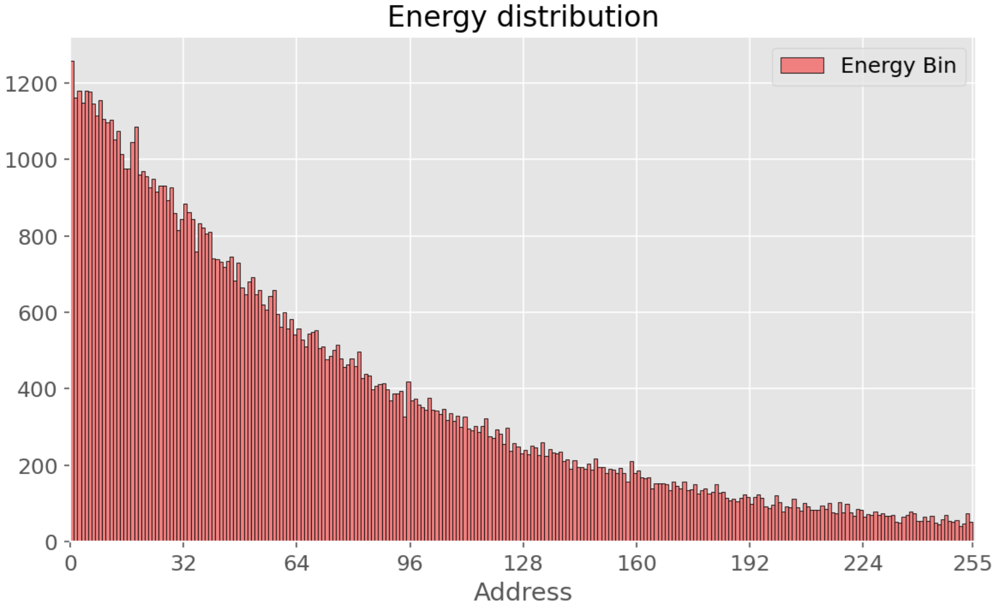




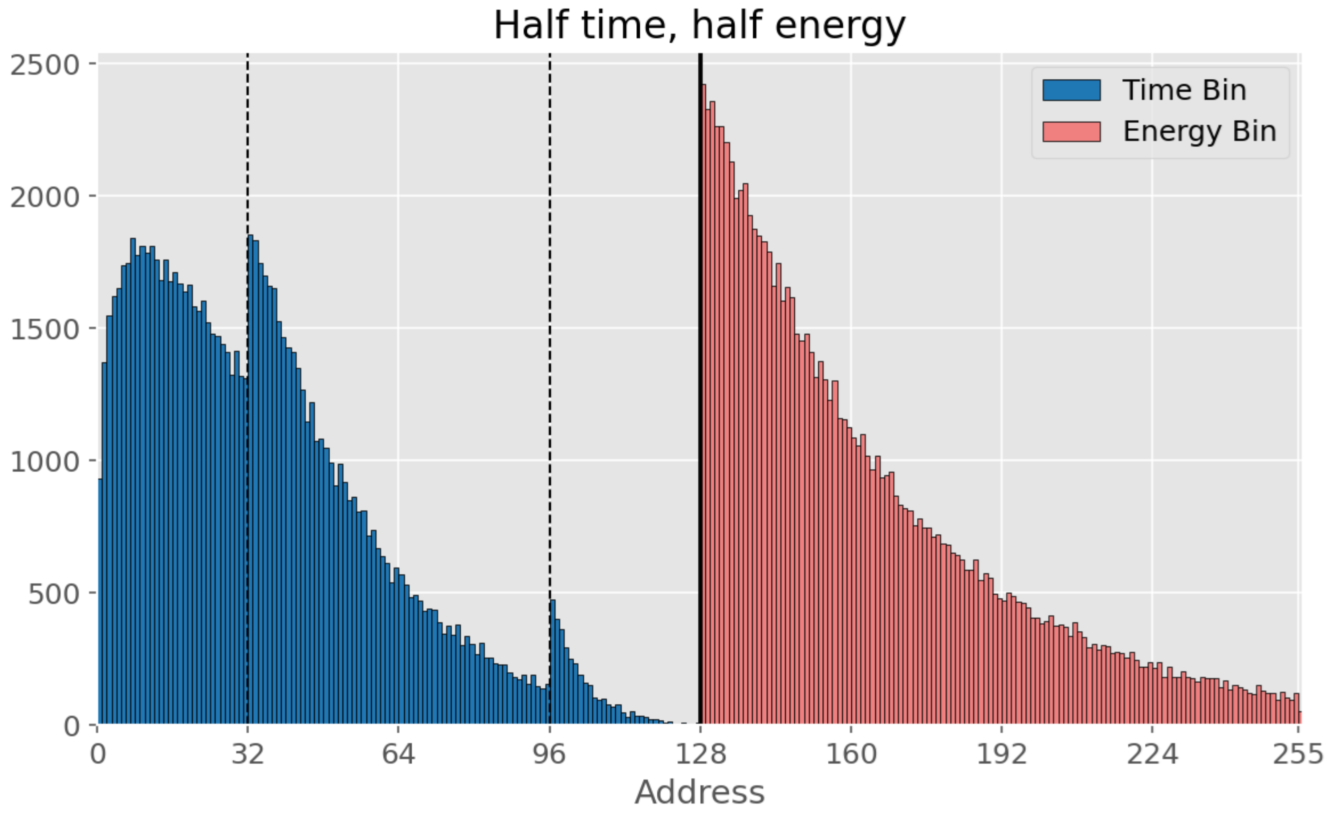


Energy & Timestamp 1D binning





- ○ Energy & timestamp binning at the same time
- ○ 256 bins per sector maximum (to be split between energy & time)

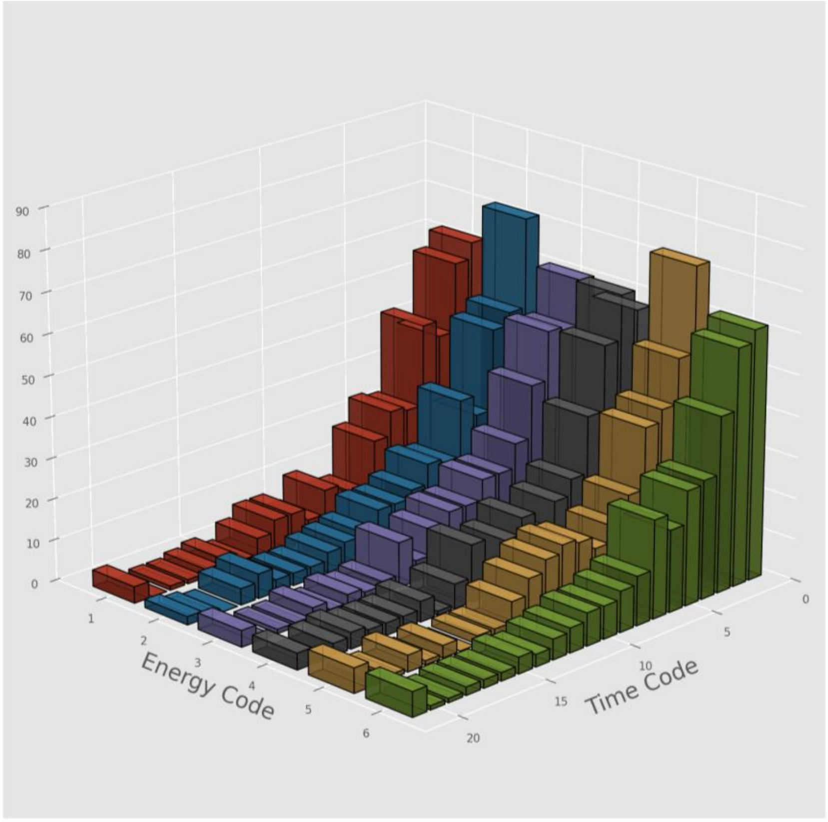


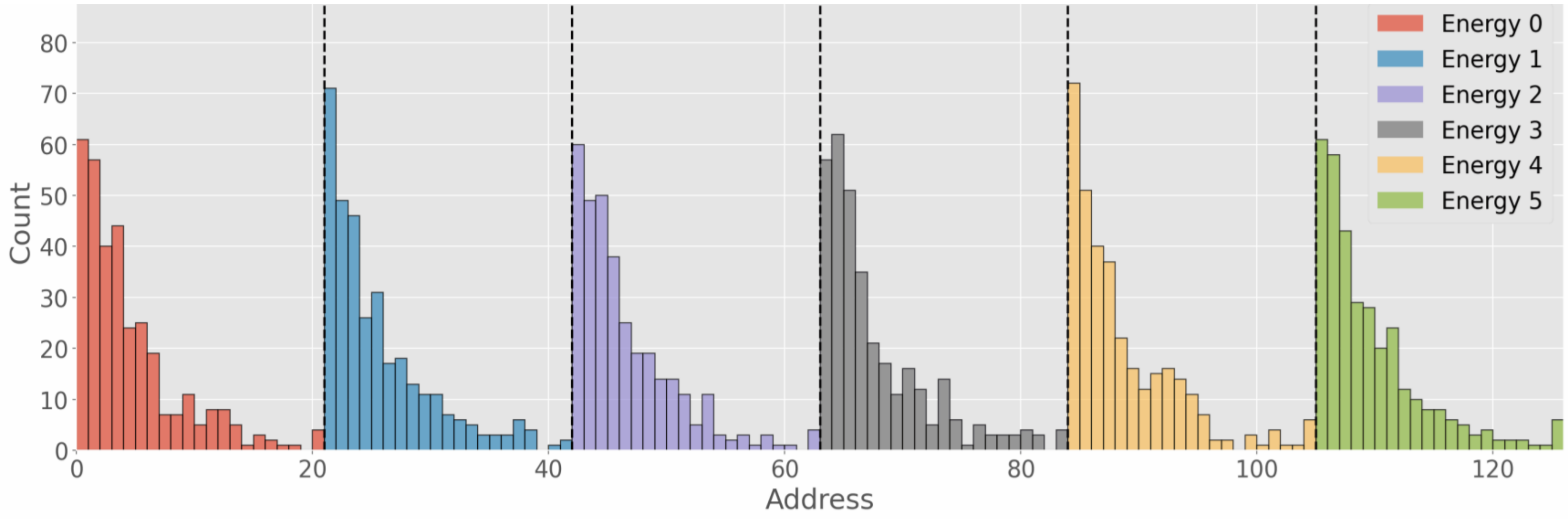
*Plots are for representative purposes only.

Post-Processing – 2D Event binning

Rebuilding the event within the PDC will feature:

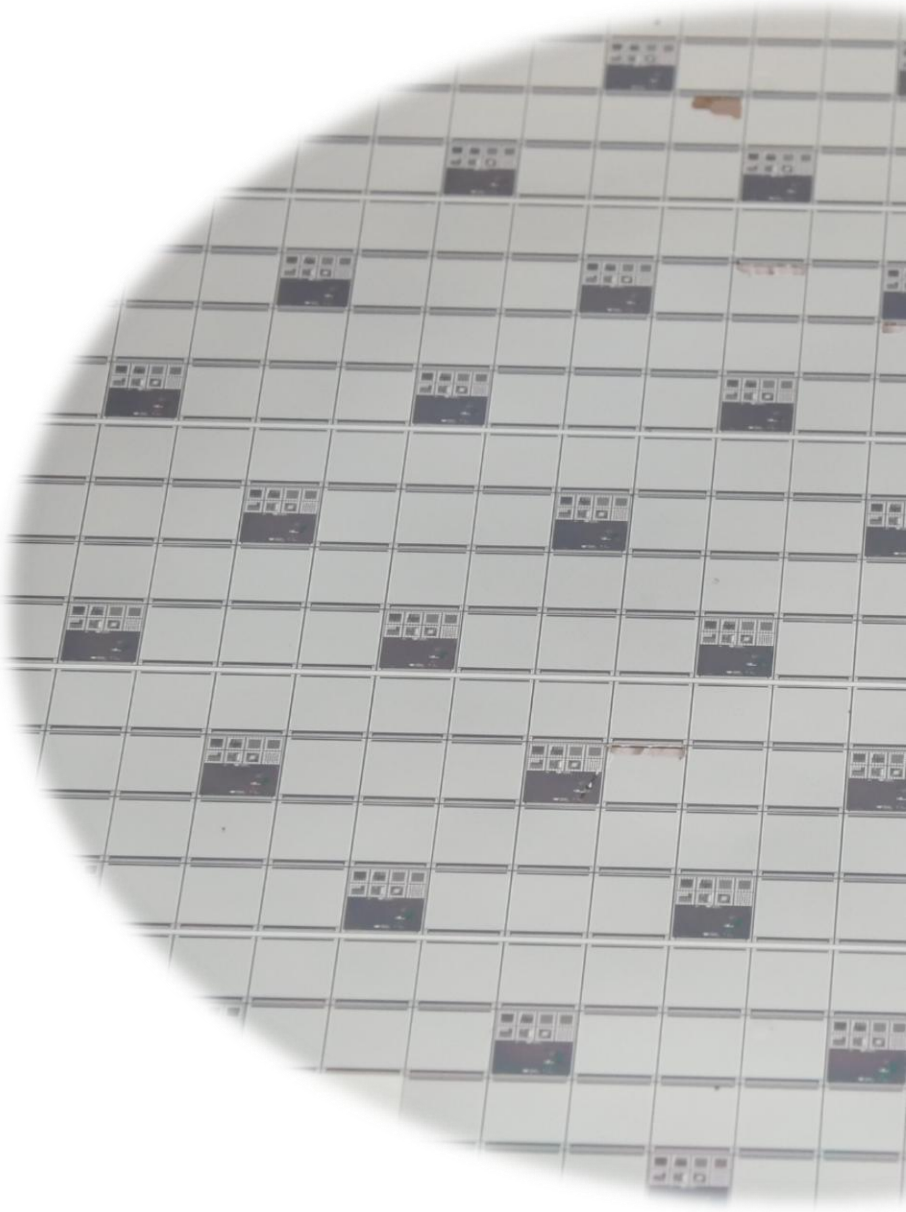
- 1 to 6 configurable energy bins (results of digital sum processing)
- Timestamp binning within each energy bin
- Data stored in SRAM blocks





Conclusion

- Quenching circuit @ 8.8 ps FWHM
- TDC @ 3.5 ps RMS
- Event detection capabilities
- Timing and Energy binning embedded
- Other functionalities for different applications
  - High speed single photon camera mode (~48 kfps)
  - Timestamp streaming mode
  - Energy streaming mode
- Next step: 3D assembly



Sherbrooke: A team's work

Université de Sherbrooke

- **Jean-François Pratte**
- **Serge Charlebois**
- Artur Turala
- Catherine Pepin
- Frédéric Vachon
- Gabriel Lessard
- Guillaume Théberge-Dupuis
- Jérémy Chenard
- Jérôme Deshaies
- Keven Deslandes
- **Nicolas Roy***
- Olivier Lepage
- Raffaele Aaron Giampaolo
- Robin Scarpellini
- Samuel Lavoie-Drainville
- Sean Prentice
- Simon Carrier
- Tommy Rossignol

Collaborators

- Fabrice Retiere (TRIUMF)
- Jean-Pierre Véran (NRC)
- Lorenzo Fabris (ORNL)
- Stéphane Martel (TDS)
- Samuel Parent (TDS)
- Simon Viel (Carleton)
- Thomas Jennewein (UW)
- nEXO Collaboration
- nEXO Canada

3IT Institut interdisciplinaire d'innovation technologique

Oak Ridge National Laboratory

Fraunhofer IZM

Innovation.ca Canada Foundation for Innovation | Fondation canadienne pour l'innovation

Teledyne Imaging Everywhereyoulook™

TRIUMF

Arthur B. McDonald Canadian Astroparticle Physics Research Institute

NSERC CRSNG

Fonds de recherche sur la nature et les technologies Québec

RESMIQ Regroupement Stratégique en Microsystèmes du Québec

CMC Microsystems

Berkeley Lab Lawrence Berkeley National Laboratory

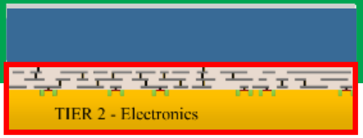
Canada First Research Excellence Fund | Apogée Canada Fonds d'excellence en recherche

Institut Quantique

Université de Sherbrooke

BACKUP

Low Power Photon-to-Digital Converter Architecture



Digital Sum

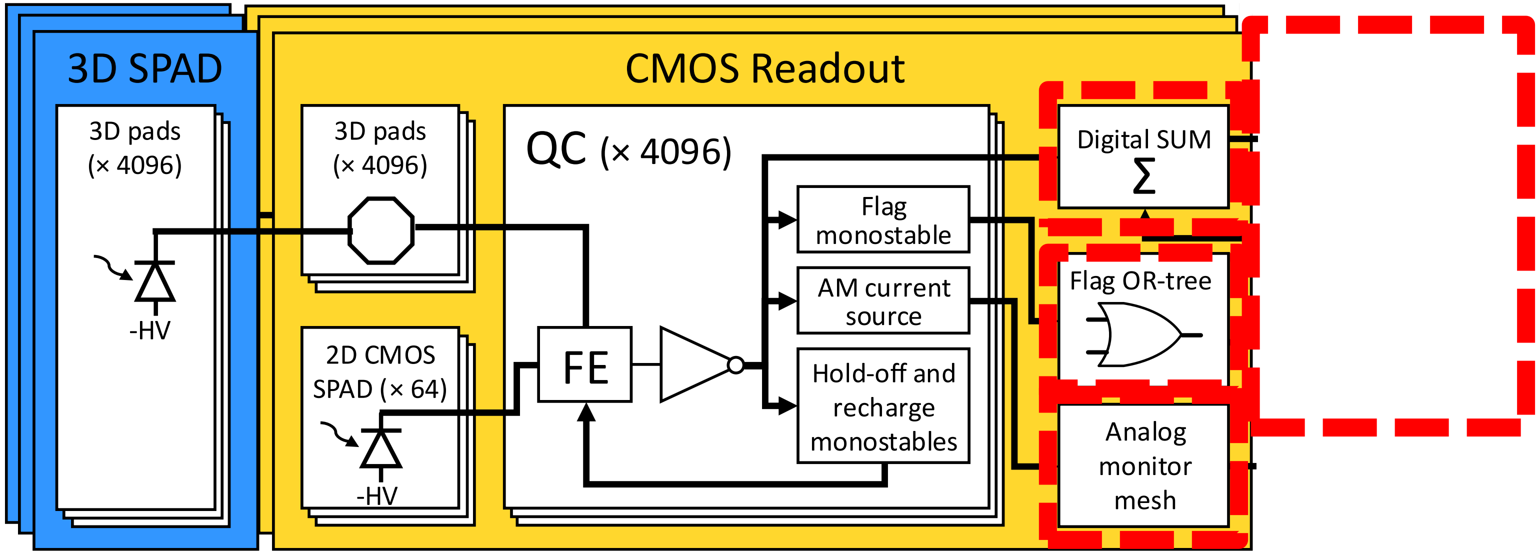
- Digital count of triggered SPADs inside a bin (dynamic range of 4096 photons).
- Adjustable bin width from 10 ns up to µs.
- Internal FIFO of 128 bins.

Flag output

- Pulsed output (adjustable from few ns to tens of ns).
- From an OR-tree.
- Timing jitter better than 100 ps RMS (i.e. external TDC).

Analog Monitor

- Current proportional to triggered SPADs.



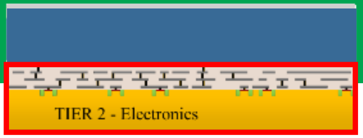
×64 PDCs/Controller

Controller (1 for 64 PDCs)

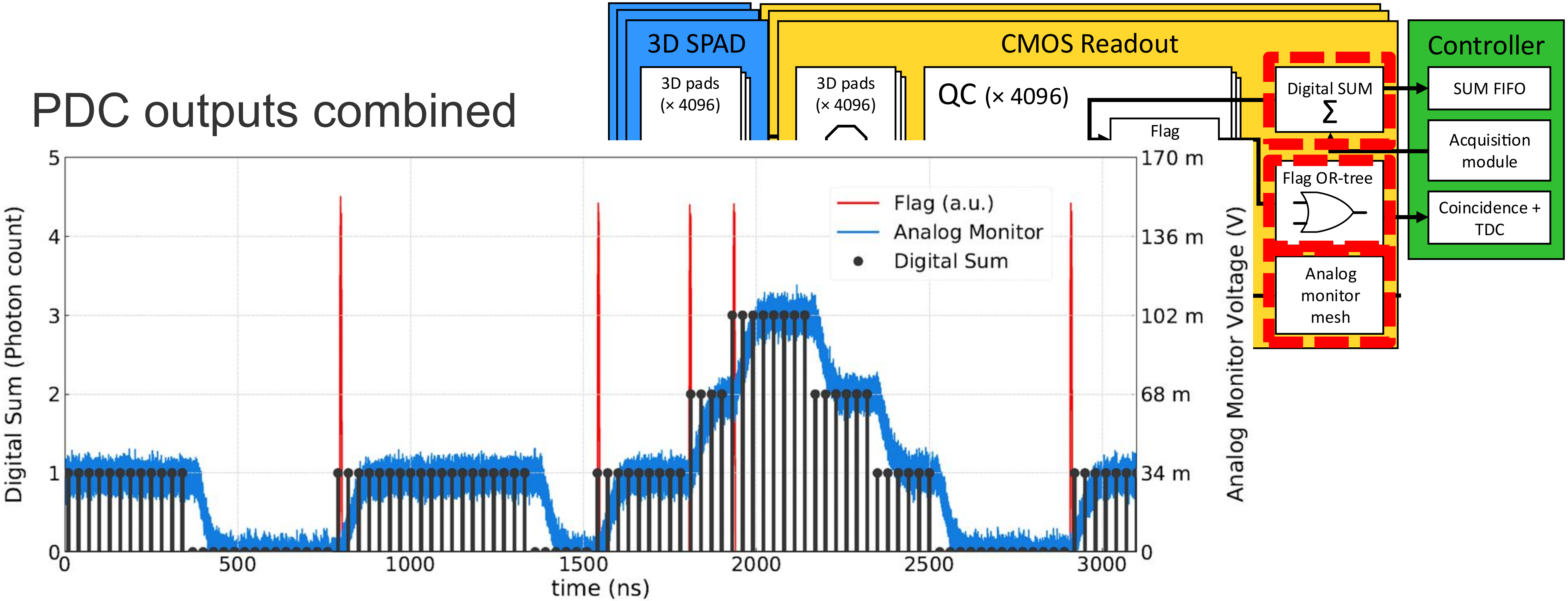
- Start PDC acquisition, based on the number of flag received to discriminate dark count.
- Bank of TDCs for timing measurements on flags.
- Receives data from PDCs and includes post-processing.
- Communicate with an external computer.

T. Rossignol *et al*., A 3D photon-to-digital converter readout for low-power and large-area applications, 2024 *JINST* **19** P09017

Low Power Photon-to-Digital Converter Architecture

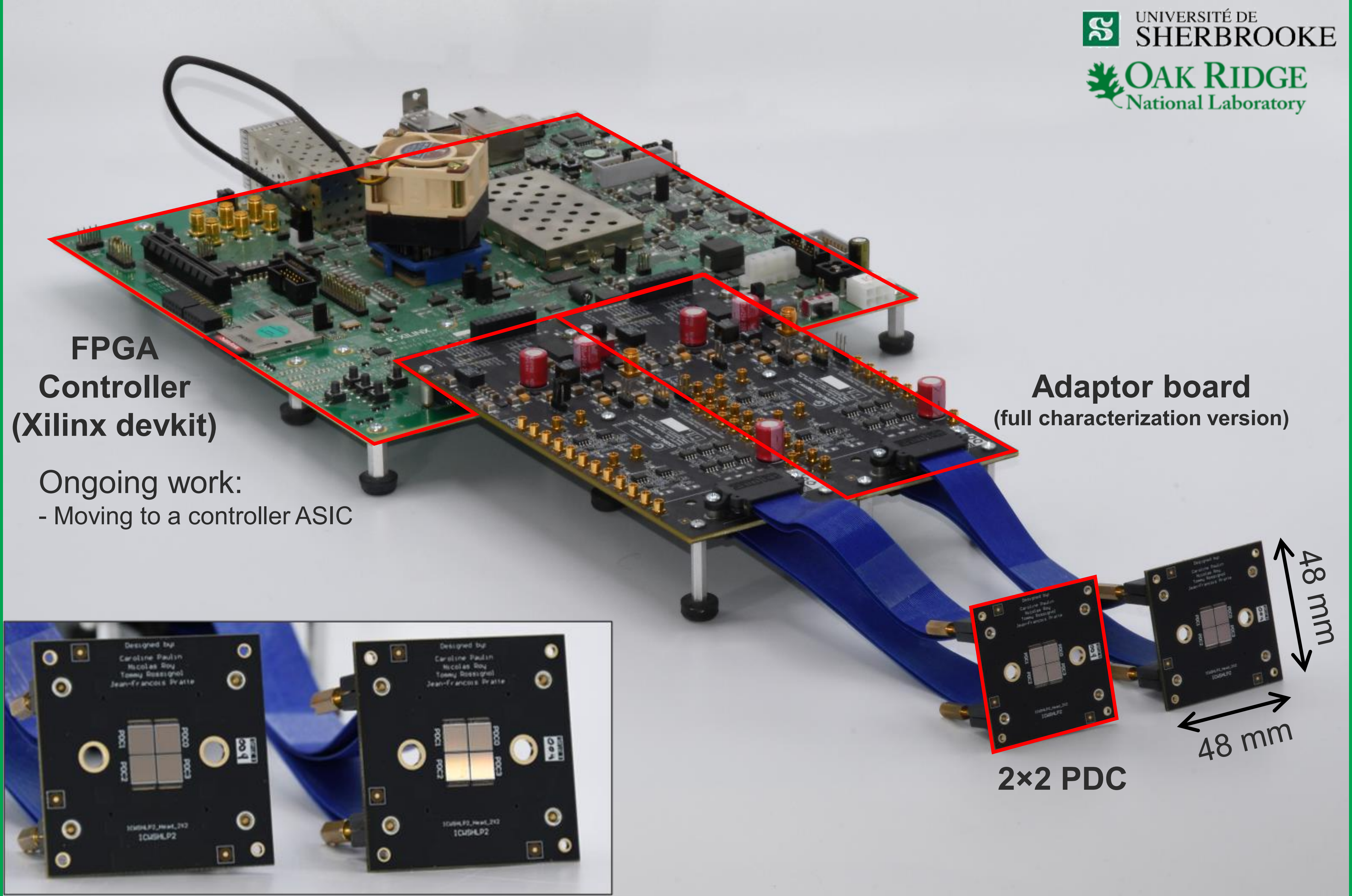


PDC outputs combined



T. Rossignol *et al.*, A 3D photon-to-digital converter readout for low-power and large-area applications, 2024 *JINST* **19** P09017

From the PDC to a test platform

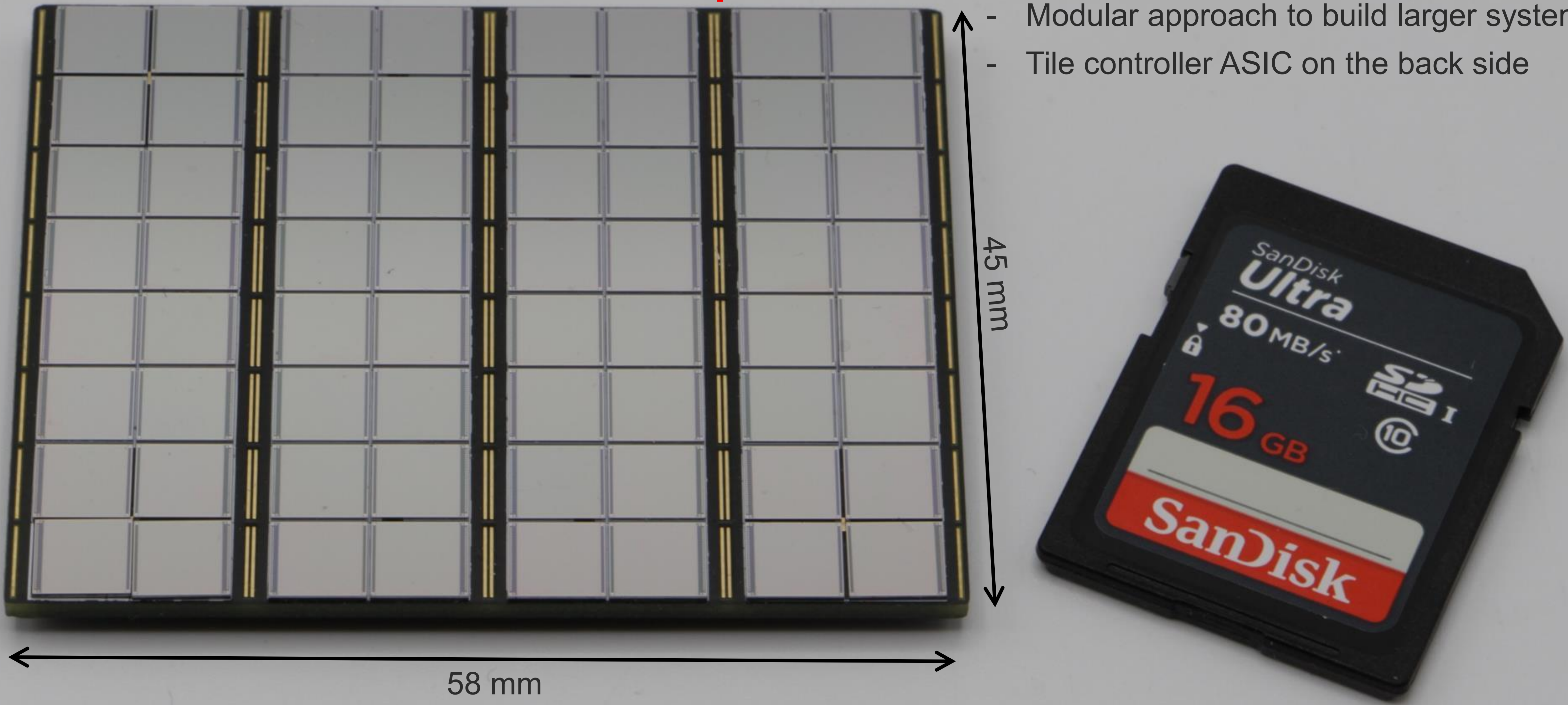


Ongoing work:

- Moving to a controller ASIC

Final goal: Modular 8×8 PDC Tile

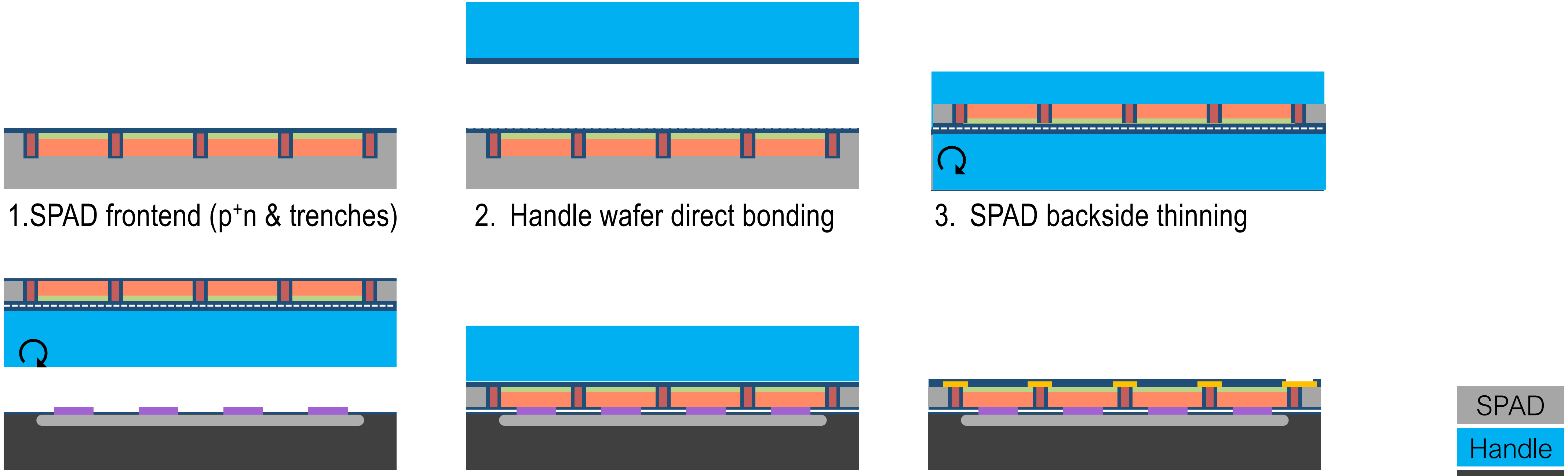
This is a Mockup!



- 8×8 PDC per tile
- Modular approach to build larger system
- Tile controller ASIC on the back side

3D SPAD Process Overview

- Combining high-end optoelectronic process (CCD) with MEMS-type 3D integration technologies
- 3 substrates, 2 wafer bonding steps, 16 masks and > 350 fabrication steps
- All at Teledyne DALSA facility (Bromont, Québec)



1.SPAD frontend (p^+n & trenches)

2. Handle wafer direct bonding

3. SPAD backside thinning

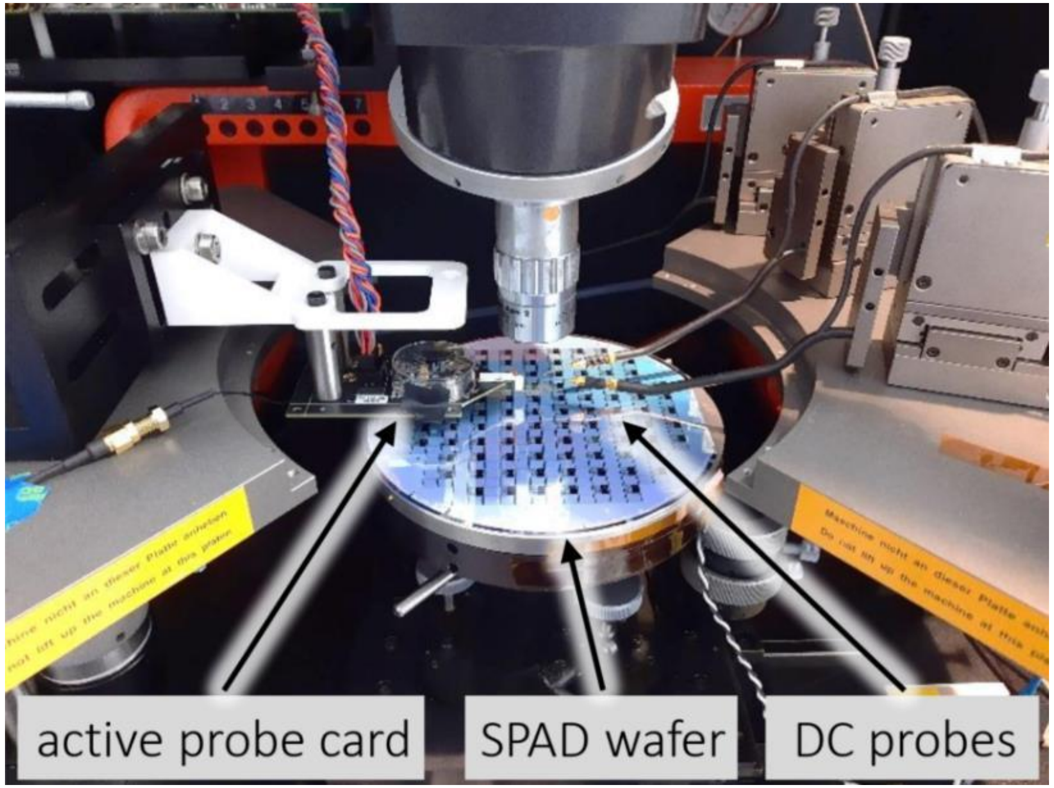
4. Al-Ge wafer-to-wafer 3D bonding

5. Handle wafer removal

6. SPAD backend (metal contacts)

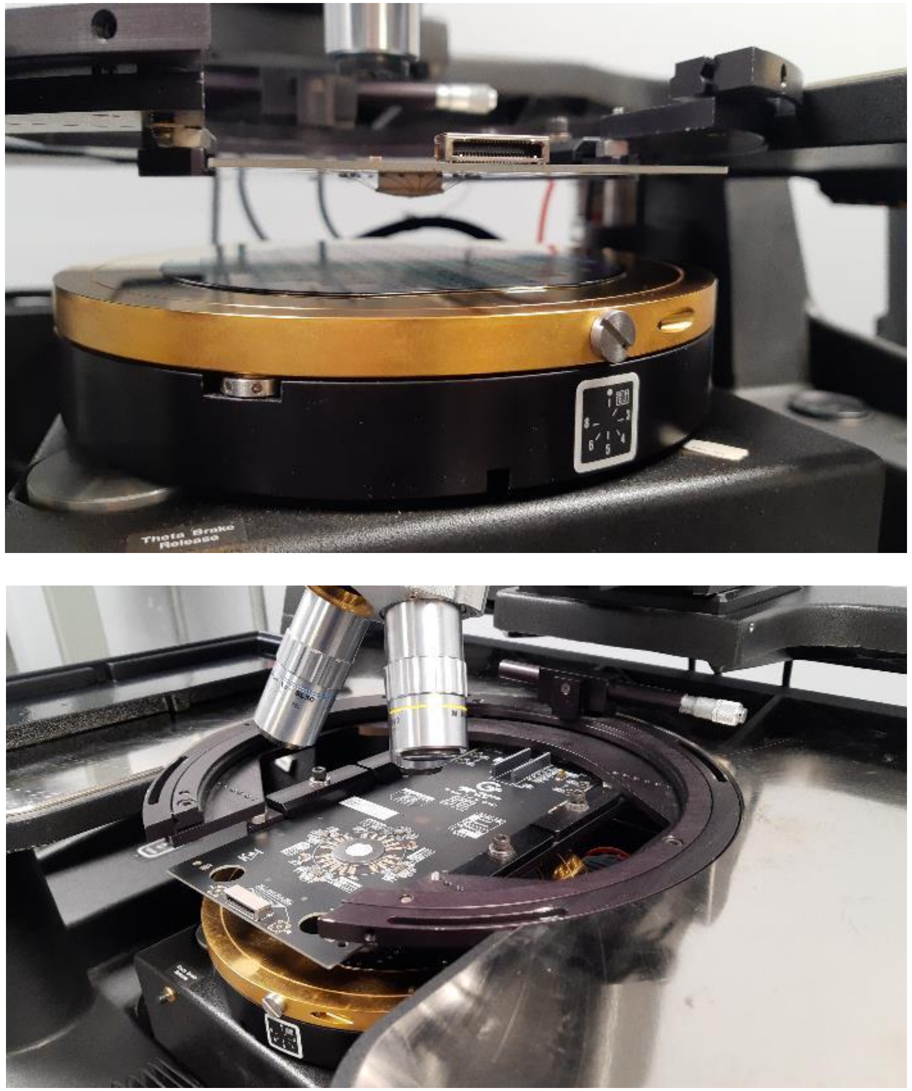
Wafer Level Probing

SPAD probing in Geiger-mode

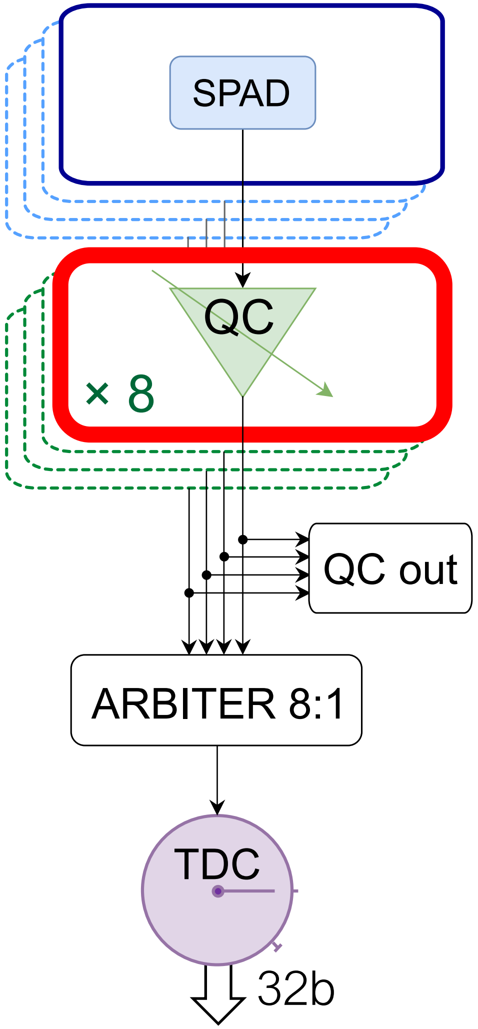


Parent, Samuel, et al. "Wafer-Level Characterization and Monitoring Platform for Single-Photon Avalanche Diodes." *IEEE Journal of the Electron Devices Society* (2024).

PDC (CMOS+SPAD) probing

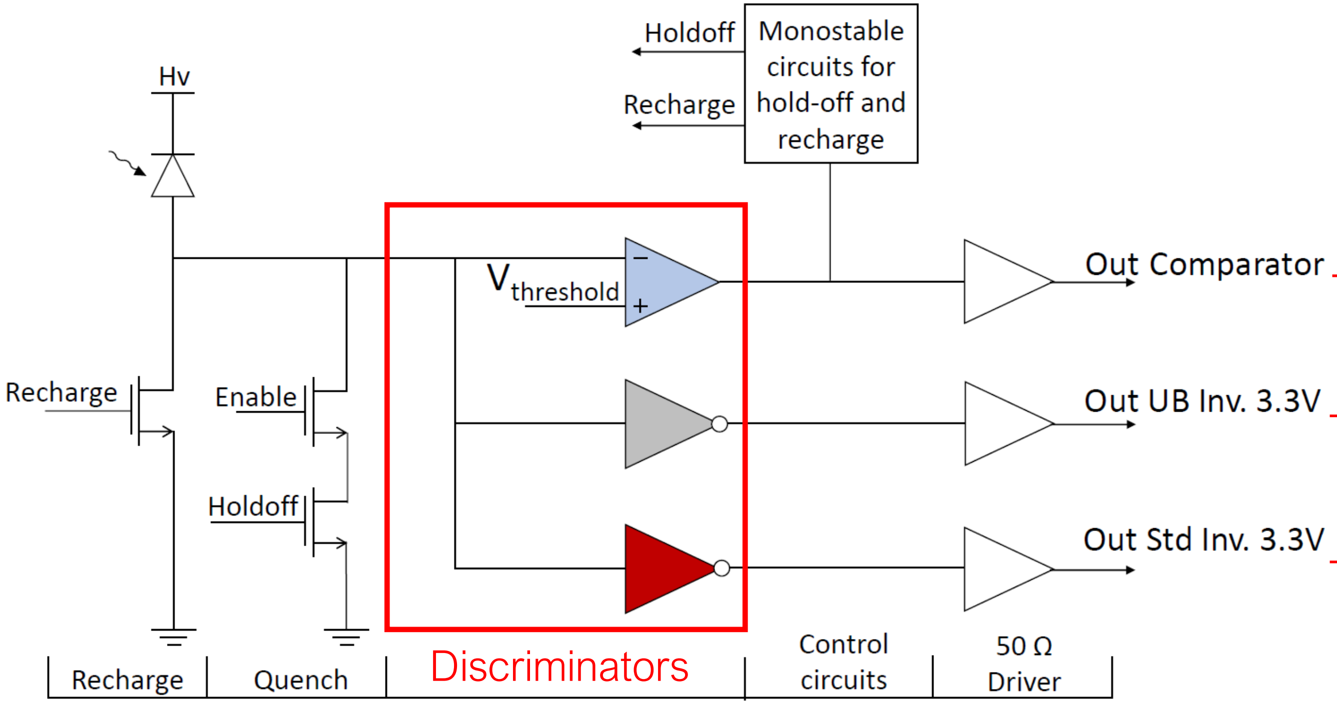


Quenching Circuit (previous work)



Previous work on QC discriminators comparison [1]

1. Comparator
2. Unbalanced inverter (UB) - $\mathrm{NMOS}/\mathrm{PMOS} \sim 19$
3. Standard inverter (Std) - $\mathrm{NMOS}/\mathrm{PMOS} \sim 3$



SPTR ~ 7.4 ps FWHM

SPTR ~ 9.2 ps FWHM

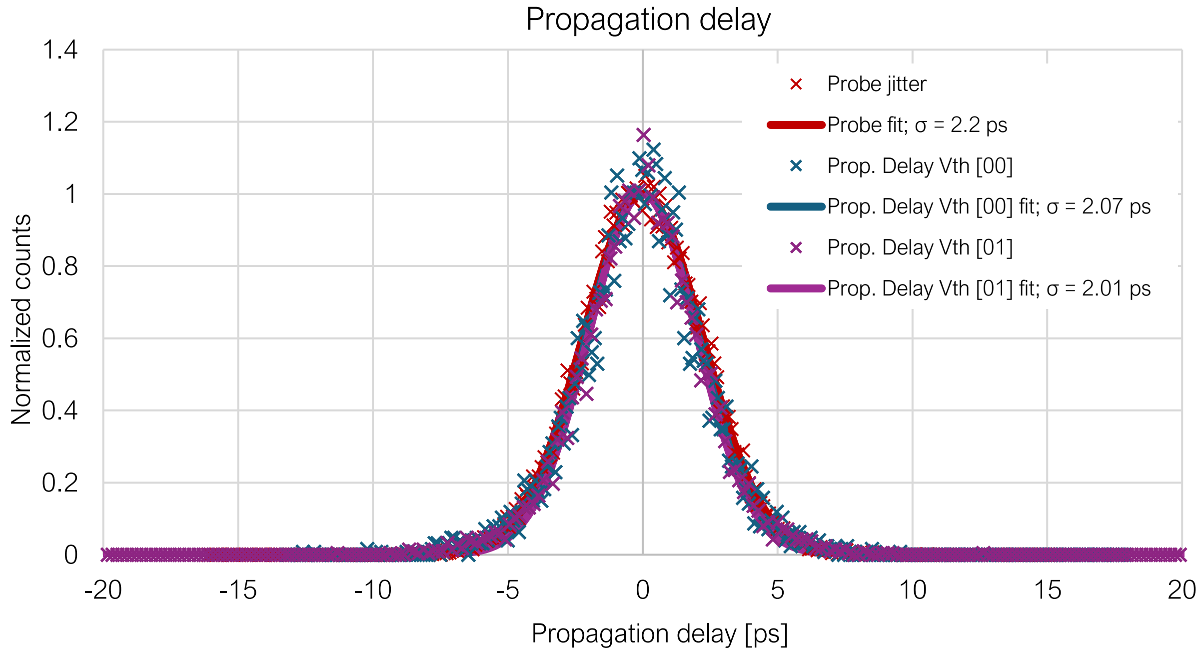
SPTR ~ 10.1 ps FWHM

[1] Nolet, Frederic et al. (2023). Quenching Circuit Discriminator Architecture Impact on a Sub-10 ps FWHM Single-Photon Timing Resolution SPAD. Instruments. 7. 10.3390/instruments7020016.

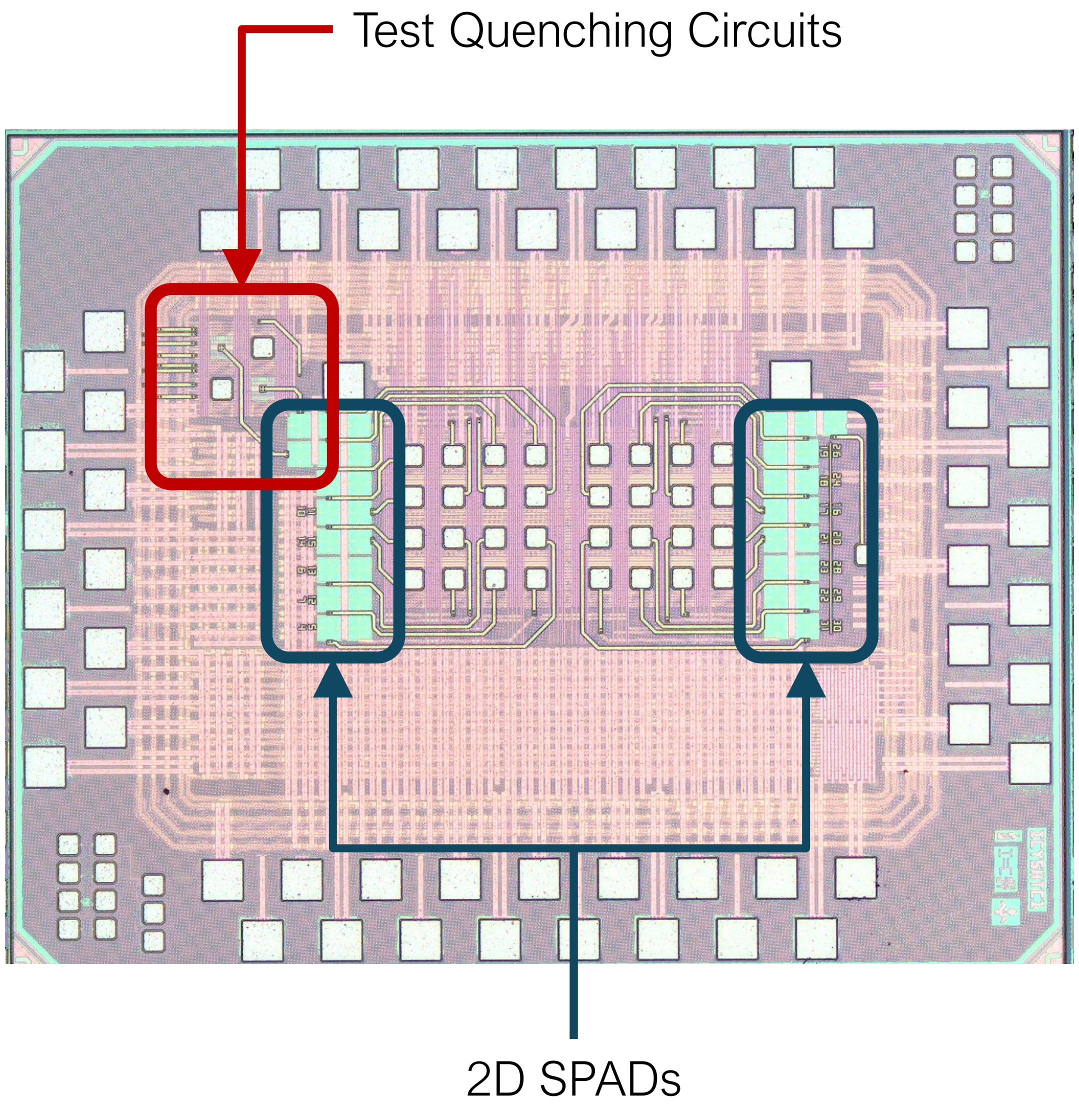
PDC – Prototype results

The results are based on measurements on the 65 nm CMOS prototype:

- 2 QCs per board, each:
  - Connected to a 2D SPAD on board as input
  - Connected to a PAD at the output
- 3 boards
- ~2 ps RMS electronic pulse jitter shown last year



NSS 2024 - Giampaolo



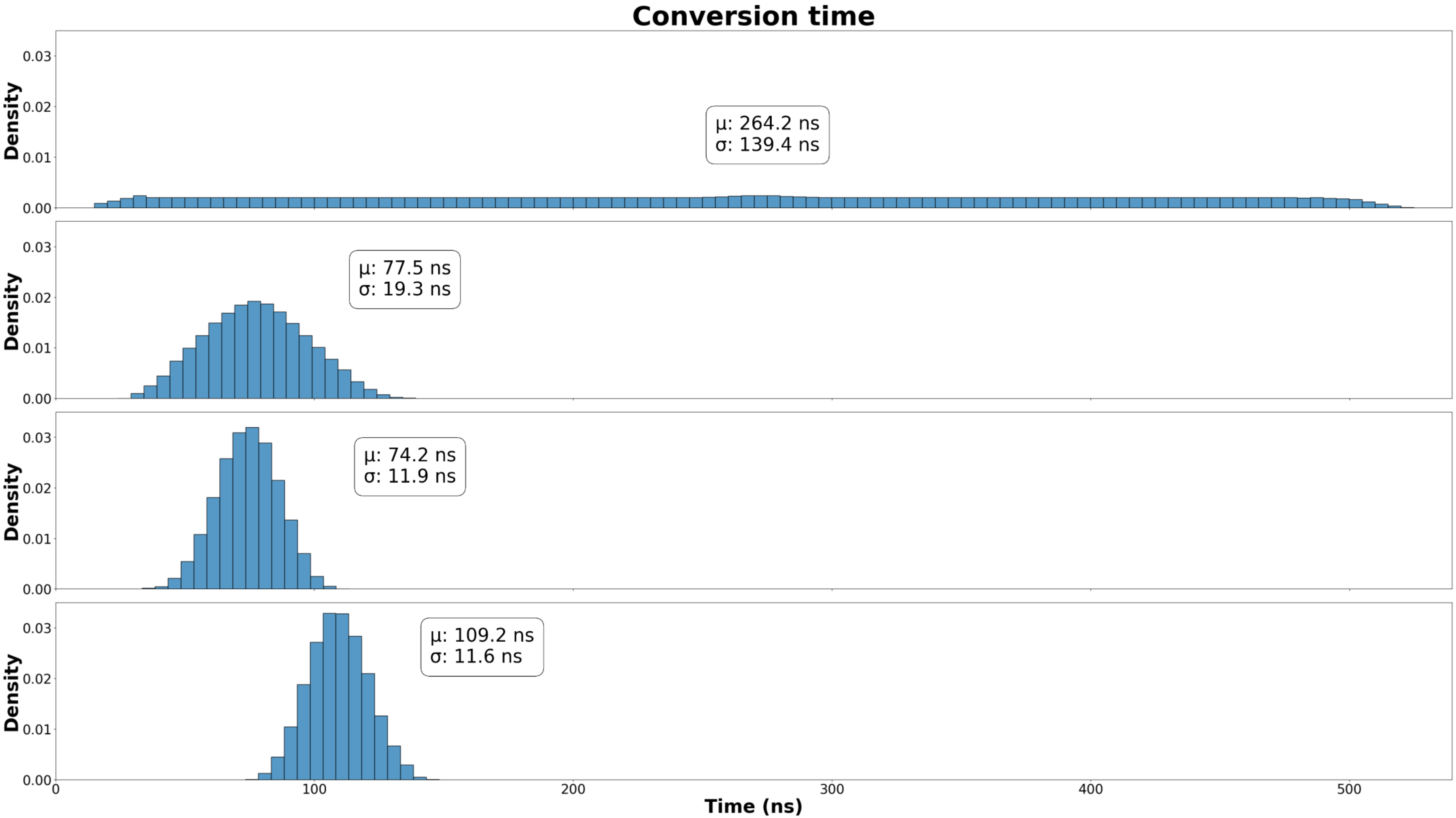
Conversion time at LSB = 50 ps and dynamic range = 20 ns (TSMC 180 nm)

SV

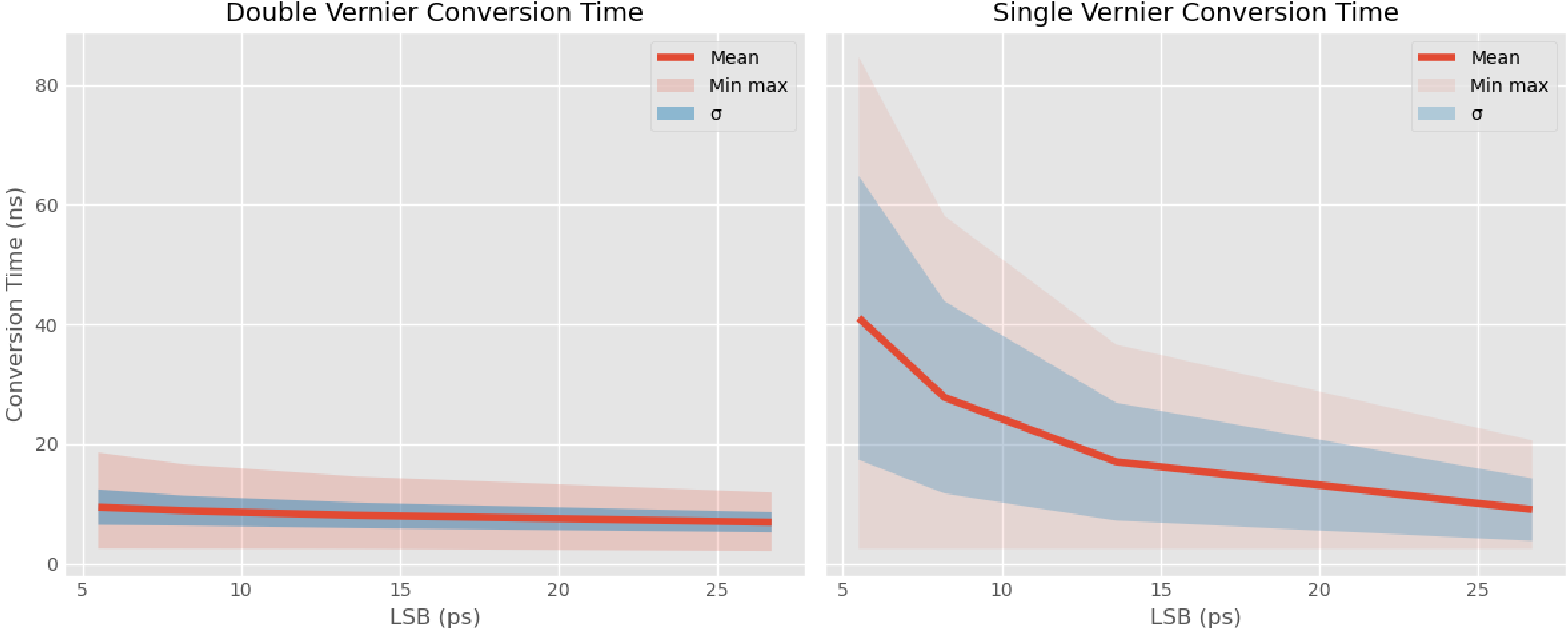
DV

TV

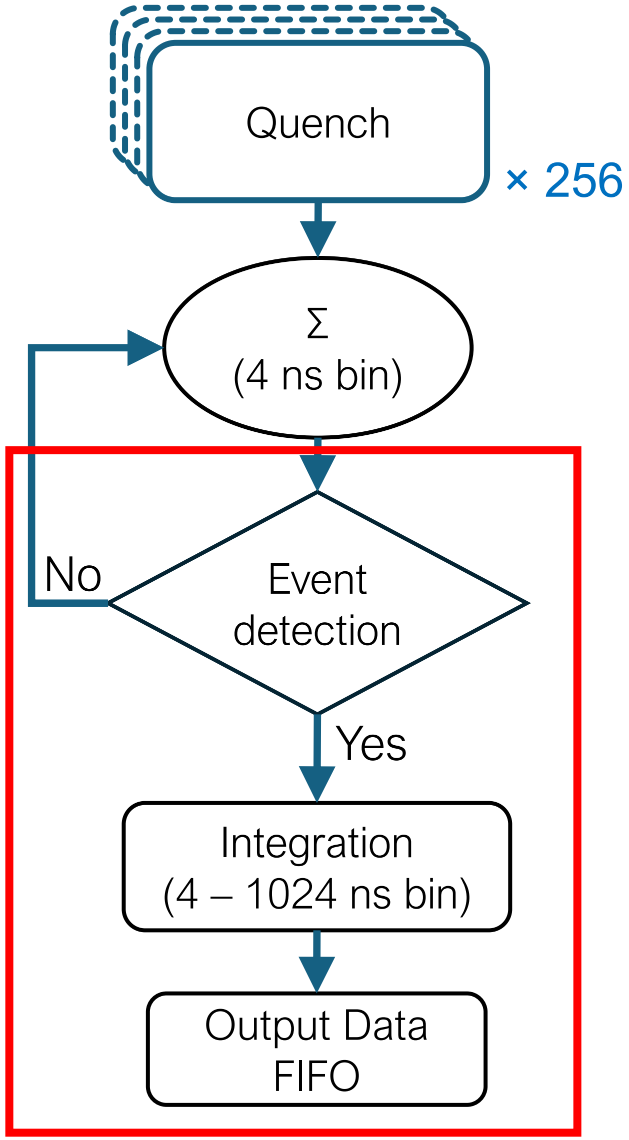
QV



Conversion Time

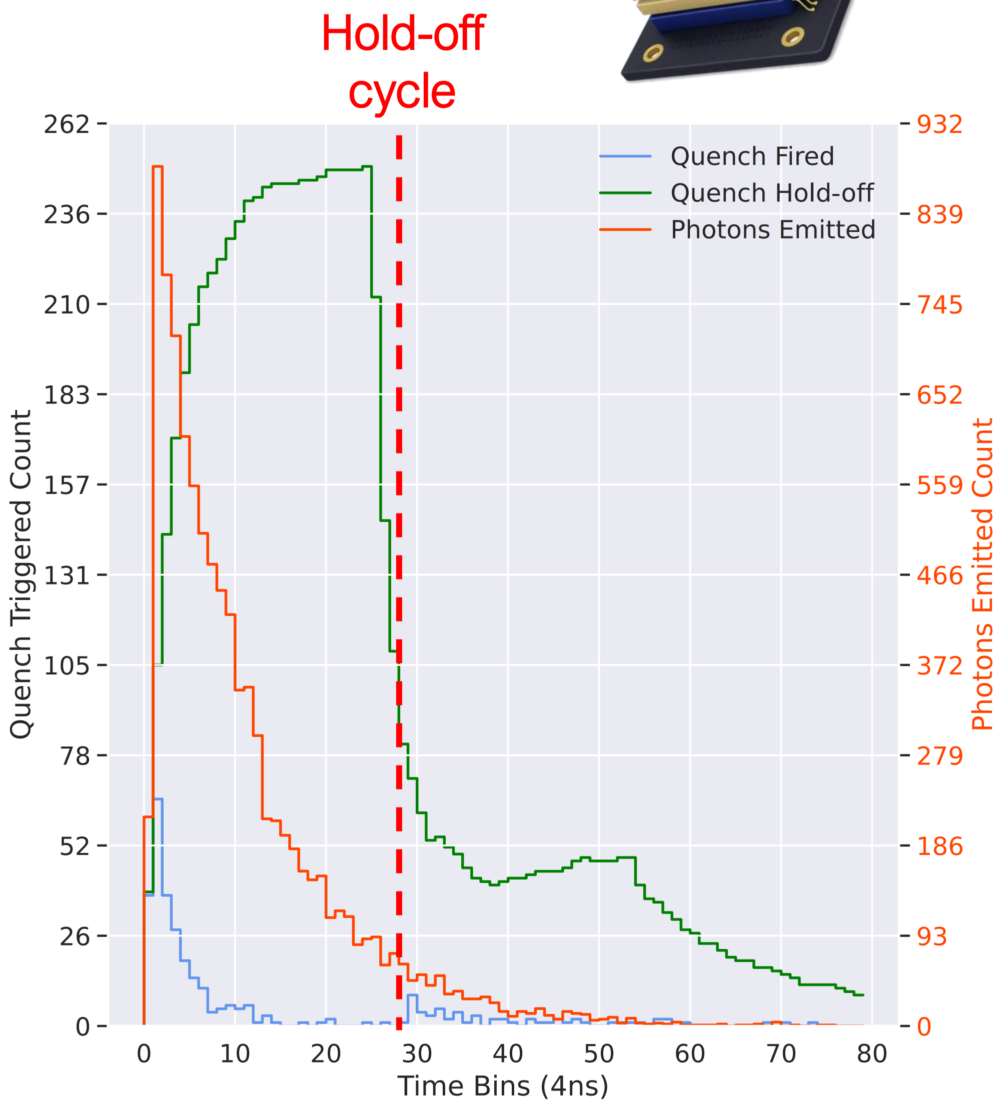


Sector – Energy Branch with Digital Sum



Digital Sum Features:

- Digital sum with a **4 ns sampling rate**
- Sum the number of quenching circuits:
  - **Fired** within a 4 ns window
  - **In hold-off** within a 4 ns window
- Event detection referenced to system clock **global count**;
  - Programmable threshold and **hysteresis**
- Sum integration
  - Configurable integration period
  - Configurable number of bins
- Output:
  - **Energy bins** integrated over N × 4 ns



GEANT4 + DSAS + Digital Simulation results