A sub-5 ps jitter time-to-digital converter ASIC with back-gate delay tuning in 22 nm CMOS

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FERMILAB-SLIDES-26-0065-ETD

Agenda

- Introduction and Motivation
  - Microelectronics at Fermilab
  - Applications for Picosecond Timing
- Time-to-Digital Converter ASIC Design and Measurement Results
- Further Developments

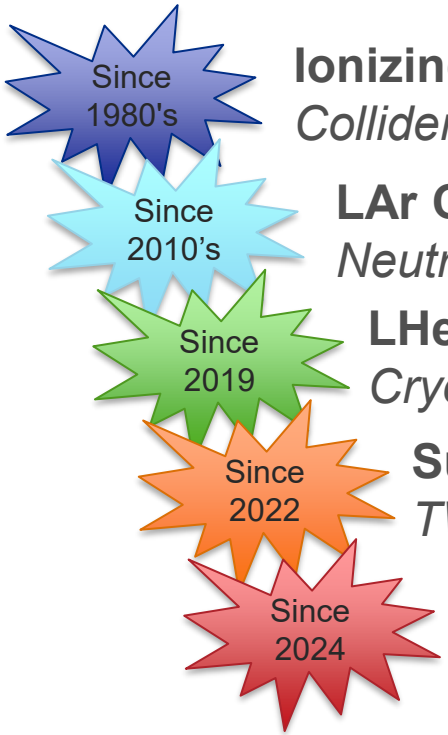
Fermilab at a Glance

- America's particle physics and accelerator laboratory
- Operates the largest US particle accelerator complex
- ~1,900 staff and ~$600M/year budget
- 6,800 acres of federal land
- Facilities used by 4,000 scientists from >50 countries

As we move into the next 50 years, our vision remains to solve the mysteries of matter, energy, space, and time for the benefit of all.

Integrated Circuit Design Over ~ 5 Decades at Fermilab

A diverse portfolio of microelectronics expertise surrounding low-noise, low-power readout of novel detectors operating in extreme environments.



Ionizing Radiation (> 1 Grad, 1,000x higher than outer space)
Collider Experiments (FCC, HL-LHC)

LAr Cryogenic Electronics (77K-100K)
Neutrino Experim… …periments (Skipper-CCDs)

See Ben Parpillon's Talk
Weds @ 11:00 am

LHe Cryogenic…
Cryo Detectors (SNSPDs, TES, etc.), Quantum Information Science

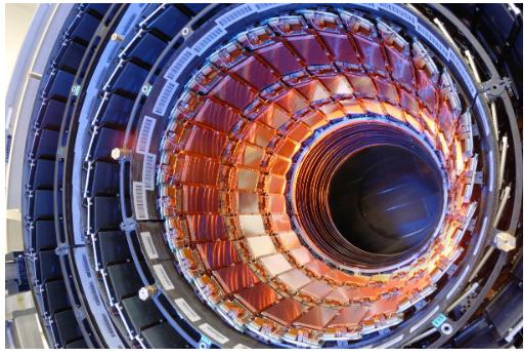
Superconducting Electronics (~100mK)
TWPAs, JPAs (ADMX), QIS for HEP

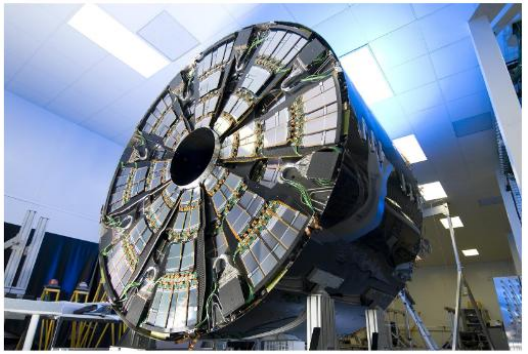
Silicon Photonics
Micro-Ring Modulators, readout for quantum sensing/computing

Applications for Picosecond Timing

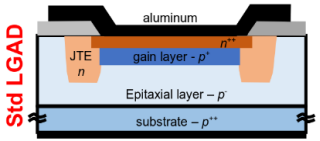
LGAD Tracking Detectors

- Future colliders need tracking detectors with 5-25 ps timing and 5-30 μm spatial resolution [11]:
  - → FCC-hh
  - → Electron-Ion Collider (EIC)
  - → Muon Collider…
- LGADs are a leading sensor candidate with 20-30ps timing resolution, but how to read them out?





HEP Application	Pitch Range	Time Resolution	Power	Noise - ASIC	Frame Rate	Gain
e+ e- collider	~ 1 mm	< 10 ps	~1 W/cm²	n.a.	Circular ~50MHz Linear 120Hz-300MHz	~10
Proton or muon collider	< 25 μm	< 10 ps	~1 W/cm²	n.a.	40 MHz	~10
BES Application	**Pitch Range**	**Time Resolution**	**Full Well**	**Noise - ASIC**	**Frame Rate**	**Gain**
Soft x-ray imaging	100 μm	n.a.	> 100 keV	< 1 keV	< 1 MHz	> 5
Mossbaeur Spectroscopy	100 μm	< 5 ns	> 1 MeV	< 4 keV	< 1 MHz	> 5
X-ray Spectroscopy	> 100 μm	n.a.	< 20 keV	< 100 eV	< MHz	20
Momentum Microscope	100 μm	< 100 ps	> 30 keV	< 1 keV	1 MHz	20
FES						
LCLS Pulse Train	100 μm	< 350 ps	> 3 MeV	< 2 keV	>3 GHz burst	3-5
NIF	< 100 μm	< 20 ps	> 10 MeV	< 3 keV	>50 GHz burst	~10



Single LGAD pixel

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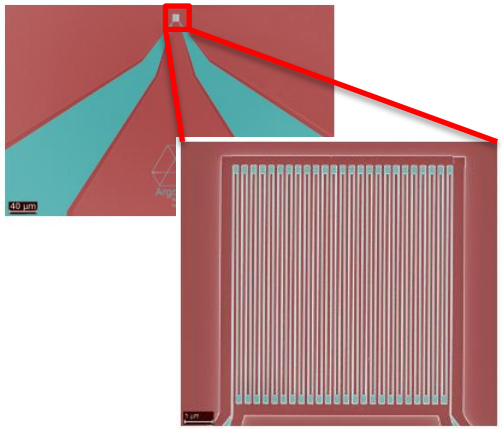
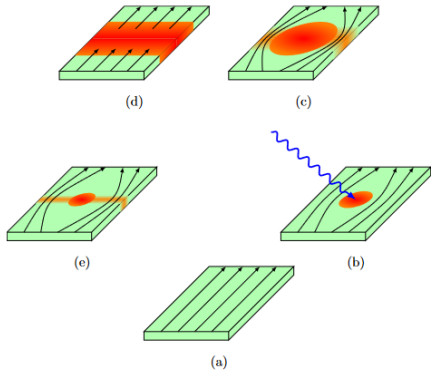
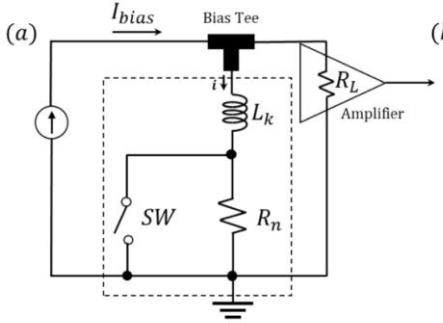
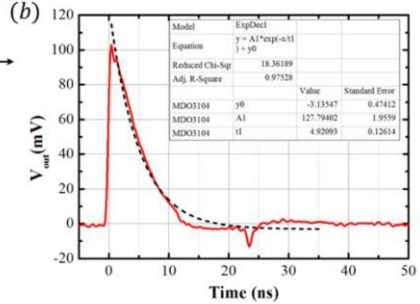
Superconducting Nanowire Single-Particle Detectors (SNSPDs)









- Ideal inductors when superconducting
- Resistive when heated by a photon/particle

- Risetime ~Lk/(Rn+RL) ~100's ps
- FallTime ~Lk/RL ~10's ns

Motivation:

- SNSPDs are fast, and fast-timing ASICs are needed to preserve that resolution.
- **Cryogenic readout** designs are key to reduce heat load.

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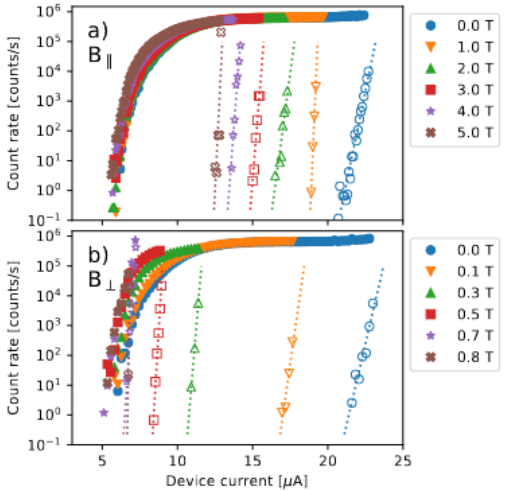
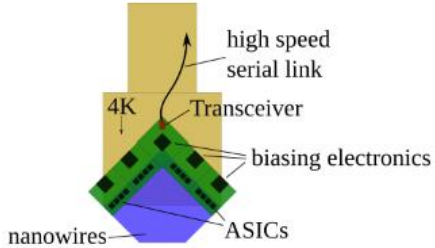
SNSPDs at the EIC

- Electron-Ion Collider: Novel accelerator under development at BNL to probe proton mass, other challenges.
- SNSPD operation at cryo + high magnetic fields can help increase acceptance by instrumenting difficult regions of the machine.
- Radiation hardness under investigation.

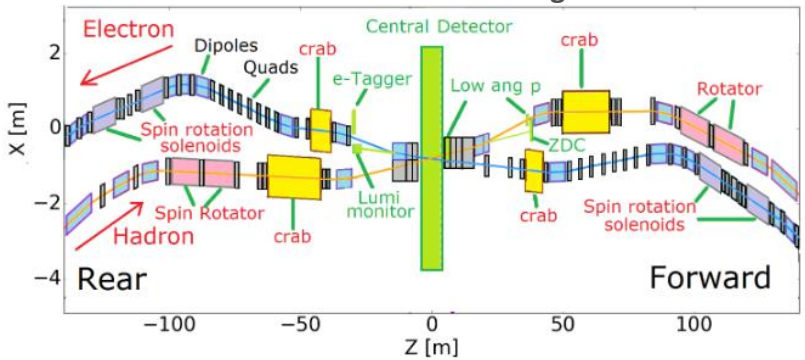


SNSPD operation at high B-field; zero dark counts.



Integration concept with SNSPDs, ASICs, and high-speed readout links.

Electron-Ion Collider Diagram



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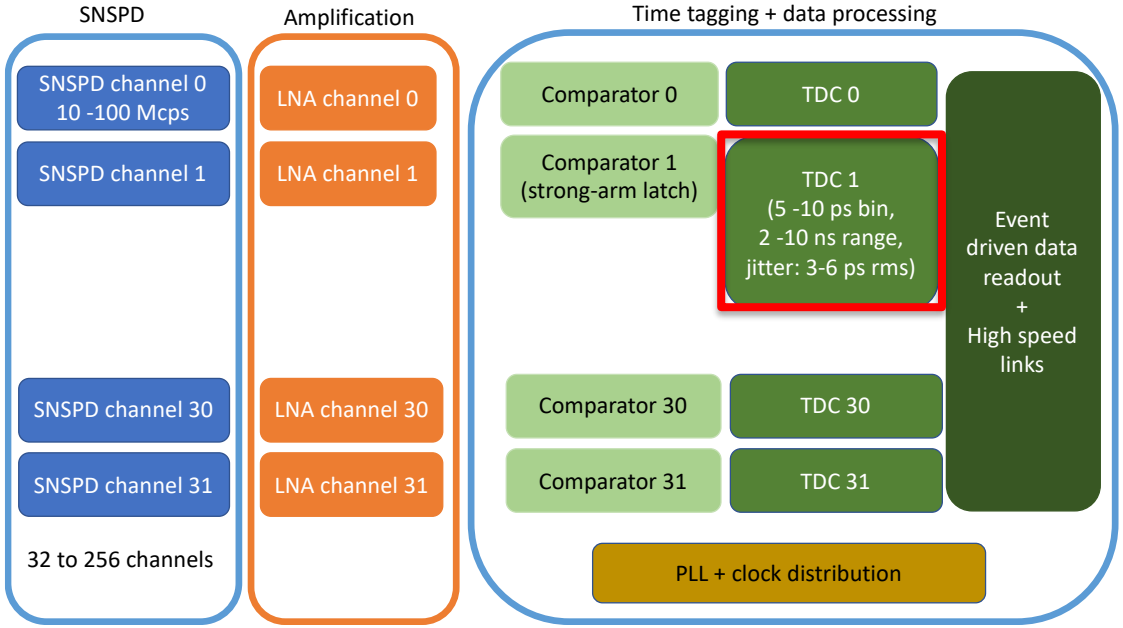
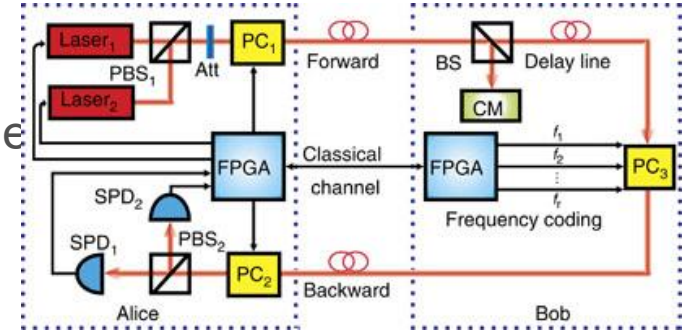
SNSPDs in Quantum Communication

The Challenge: High-bandwidth time-correlated single photon counting in a cryogenic environment.



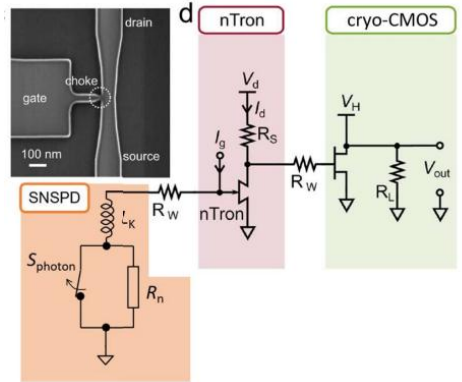
DOE NASA RFI 86 FR6315 [4]

1 – 10 Gcps



A Quantum Secure Direct Communications System (Hu [10])

Integration with superconducting electronics:



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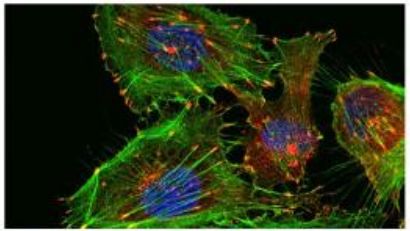
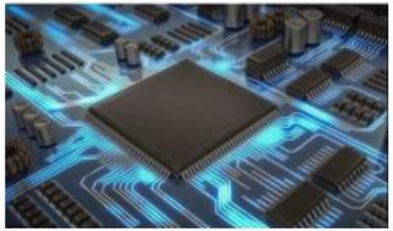
Diverse Other Applications

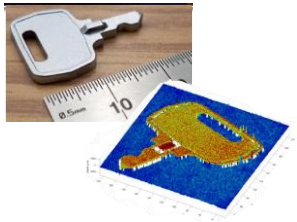
Lidars and Automotive



Bio Imaging and Life Science

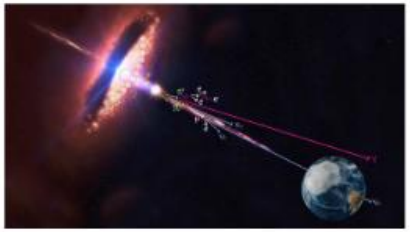


Fast timing applications



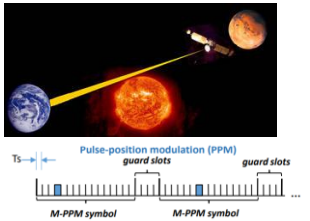
Rangefinding / 3D Modeling

Advanced manufacturing



Astro-particle physics

Quantum science and cryptography



Optical Space Communication

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Picosecond Timing ASIC Development

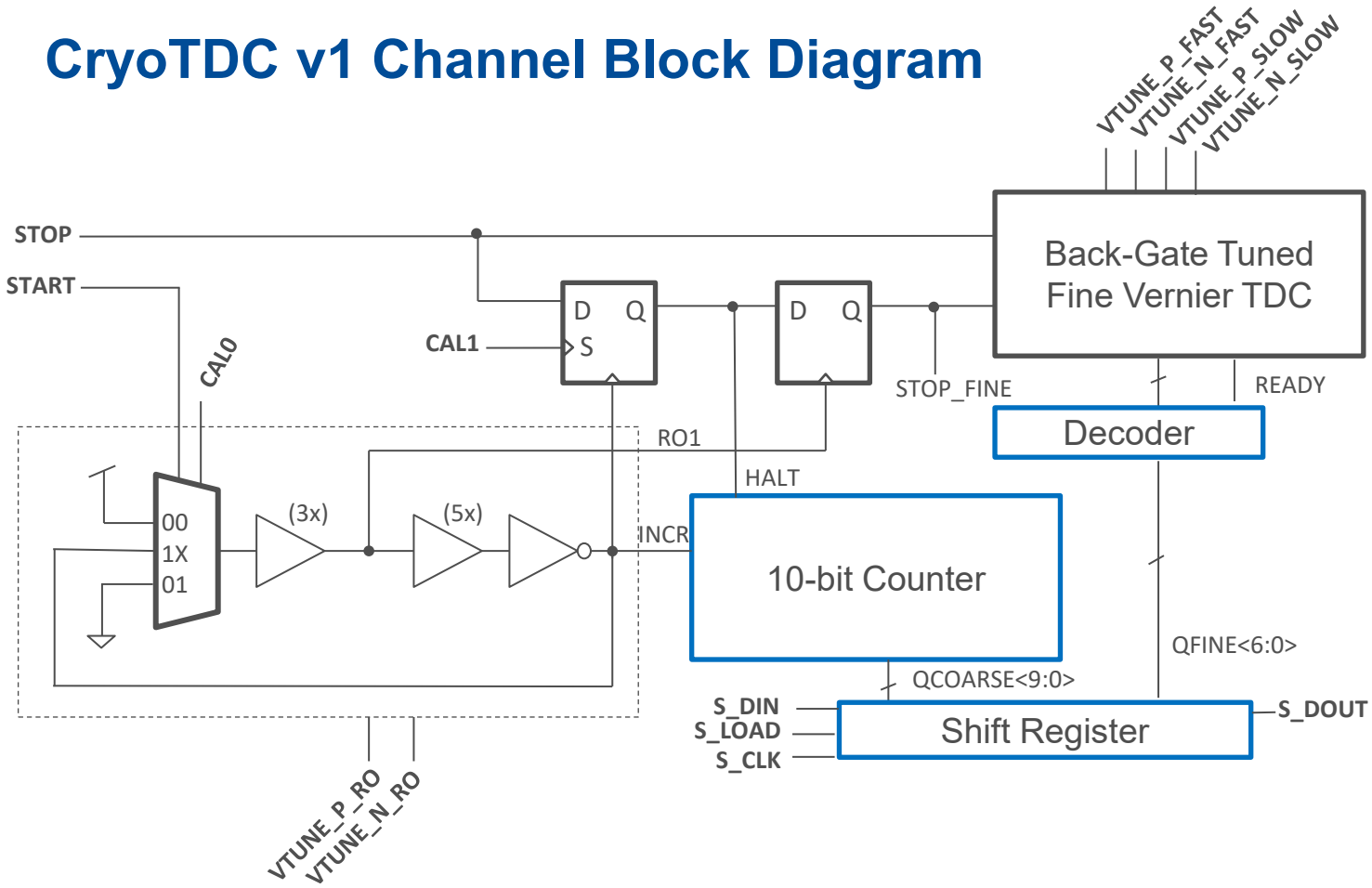
Picosecond Timing ASIC Development

- Design Objectives:
  - → 5-10 ps resolution
  - → 3-6 ps jitter
  - → 2-10 ns dynamic range
  - → Operation at cryogenic (4K) and room temperature.
  - → ~ few 100 uW per channel
- ASIC Versions:

  Nov 2021 – CryoTDC v1: Single-channel TDC Demonstrator

  Oct 2023 – SUNROCK: 32-channel Prototype w/ Peripheral Circuits

CryoTDC v1 Channel Block Diagram

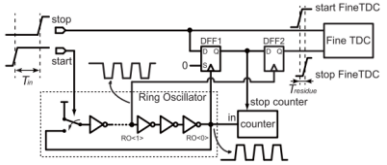


Total Pins: 22

- 6 analog inputs
- 7 digital inputs
- 3 digital outputs
- 6 power pins

Not Shown:

* RO1, HALT, INCR, and STOP_FINE are mux'd to **two** digital outputs with the select done by 4 shift register bits.
* RESET pin



Enomoto et al. [2]

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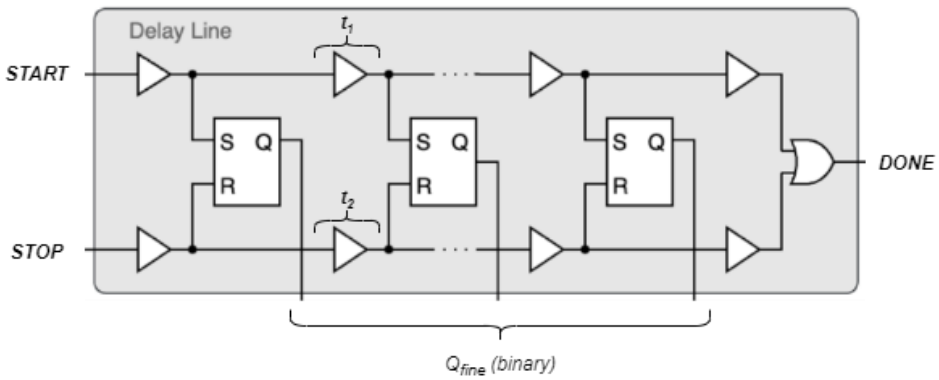
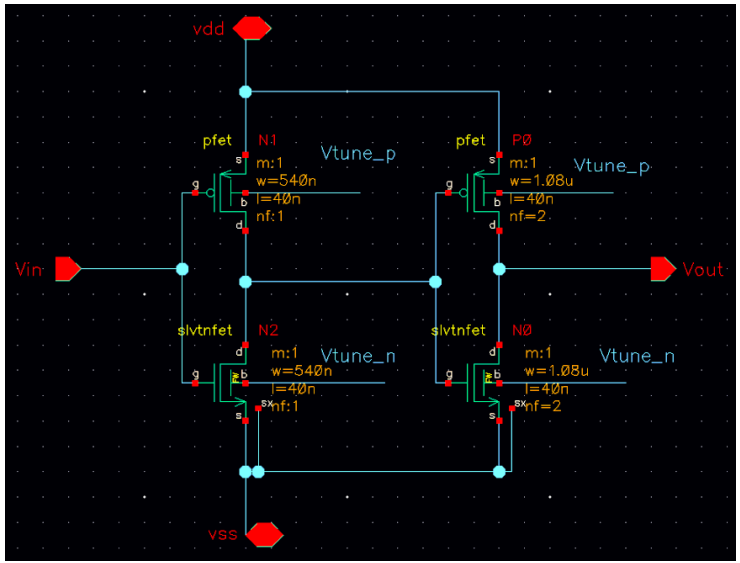
Fine Vernier TDC

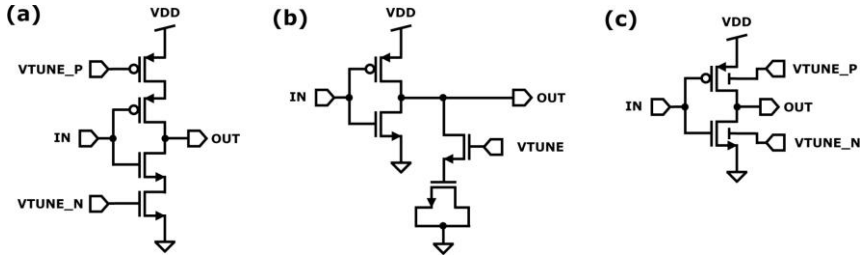


- t_1 and t_2 are tuned to be very close to each other.
- 1 LSB = $t_{R(fine)} = (t_2 - t_1)$
- STOP is always faster than START.
- If START arrives first at stage *n*, Q[n]=1
- Result is thermometer-coded: “How many LSBs does it take for STOP to catch up to START?”

Delay Tuning with Back-Gate Bias



Fine TDC Delay Stage



Comparison between back-gate tuning and conventional approaches.

- Fine TDC delay cells and RO delay cells are same architecture (different sizing)
- Speed is tuned by FDSOI back-gate biasing
  - Low complexity
  - Small footprint
  - No noise contribution from bias circuits
- 6 separate tuning voltages (all 0~2V w.r.t. VSS)
  - Fine TDC fast chain, slow chain, and coarse TDC ring oscillator (NMOS and PMOS separately).

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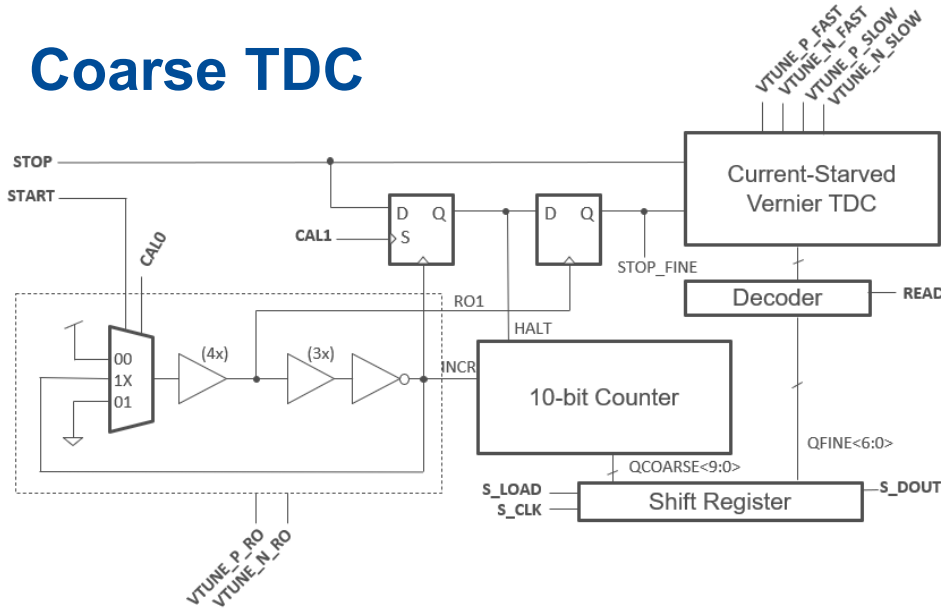
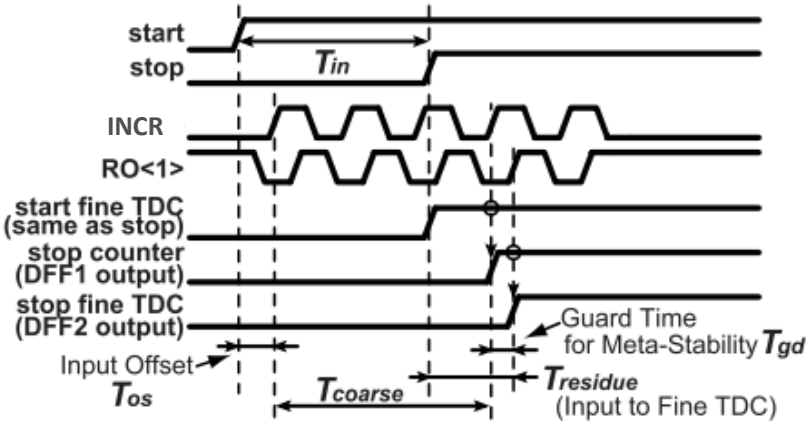
Coarse TDC



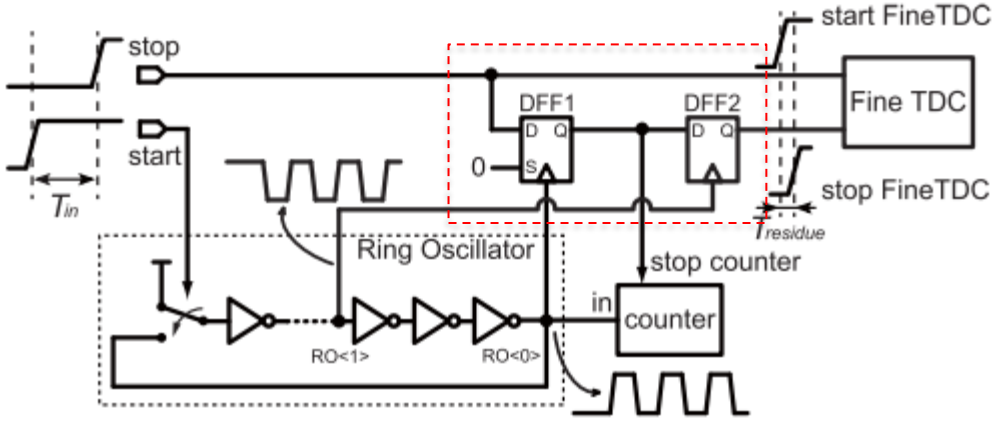


Enomoto et al. [2]

START starts the ring oscillator. The counter counts up until STOP, and the residue is encoded by the fine TDC:

$$T_{in} = T_{OS} + T_{coarse} + T_{gd} - T_{residue}$$
$$= \left(T_{OS} + T_{gd}\right) + N_{coarse}\left(t_{R(coarse)}\right) - N_{fine}\left(t_{R(fine)}\right)$$

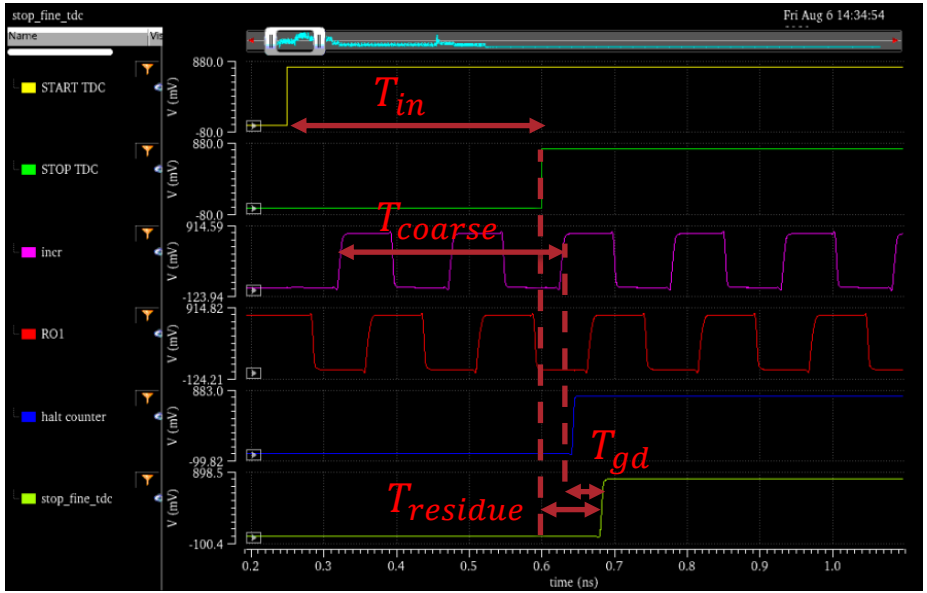
Coarse-to-Fine Coupling with DFFs



Enomoto, et al. [2]

- Traditional TDCs couple with a multiplexer → unwanted $T_{D\to Q}$, possibly different for different inputs. ☹
- In our design, DFF1 is triggered on the *first coarse TDC increment after STOP arrives.* (With constant offset $T_{clk\to Q}$)
- The remainder ($t_{incr} - t_{STOP}$) is digitized by the fine TDC.
- Why have DFF2? STOP and RO<0> are asynchronous, so we need to suppress any metastability in DFF1's output before the fine TDC.
- DFF2 is triggered slightly after DFF1 ($T_{incr} + T_{gd}$). We assume DFF1's output has settled within T_{gd}.

Simulation of an Example Measurement



From calibration, we have:

$$t_{R(fine)} = -2.6375 \text{ ps}$$
$$t_{R(coarse)} = 152.75 \text{ ps}$$
$$T_{OS} + T_{gd} = -173.62 \text{ ps}$$

For this measurement, $Q_{fine} = 33$ and $Q_{coarse} = 4$, so:

$$T_{in} = T_{OS} + T_{coarse} + T_{gd} - T_{residue}$$
$$\approx 350.343 \text{ ps}$$

(Actual T_{in} was 350 ps)

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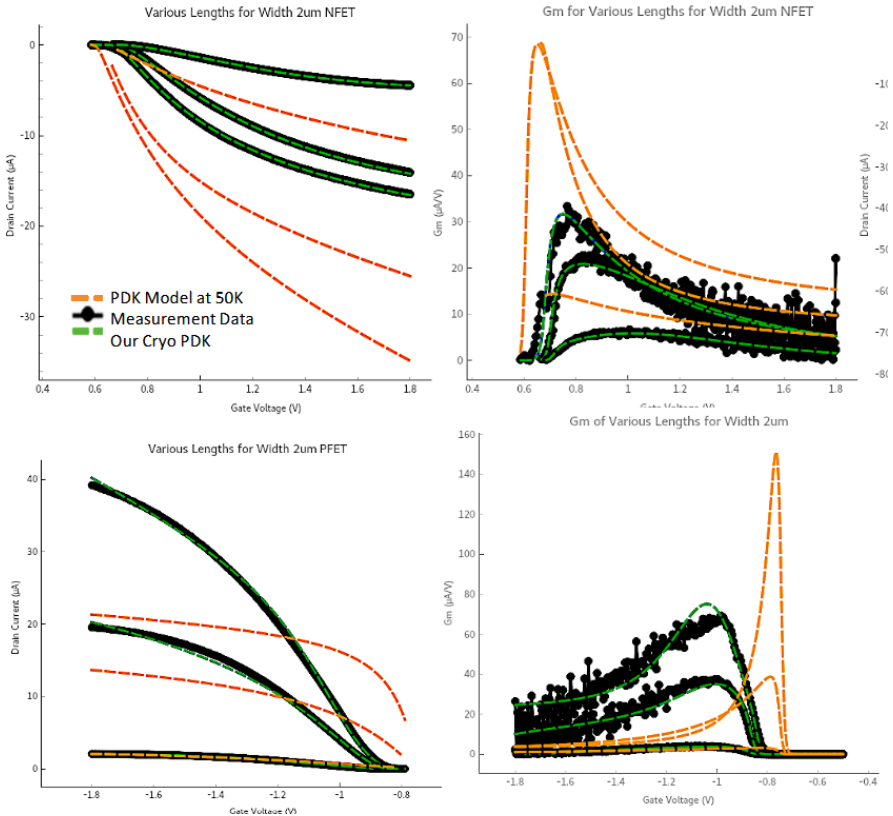
A Note on Cryomodels

- Fermilab is developing cryogenic models for GF 22FDX in collaboration with EPFL, Synopsys, and GlobalFoundries.
- At present, models cover SLVT and EGLVT FETs at 3.8K
- Unfortunately, these models were not available at design time for the cryoTDC – and do not match the flavors used in the cryoTDC core.
- For more information, see: https://doi.org/10.2172/2426440 (Olivia Seidel, IceQubes 2024)



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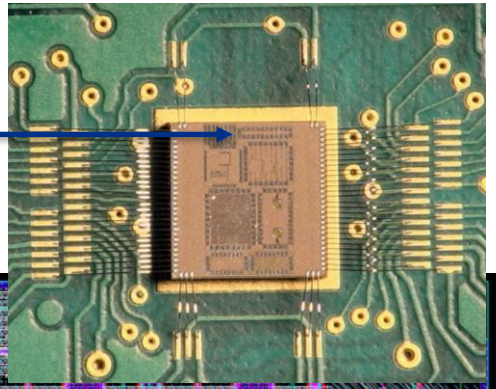
Test Chip



≈ 250 µm

≈ 1000 µm

≈ 20 µm

[Digital Readout and Control]

[Fine TDC]

≈ 150 µm

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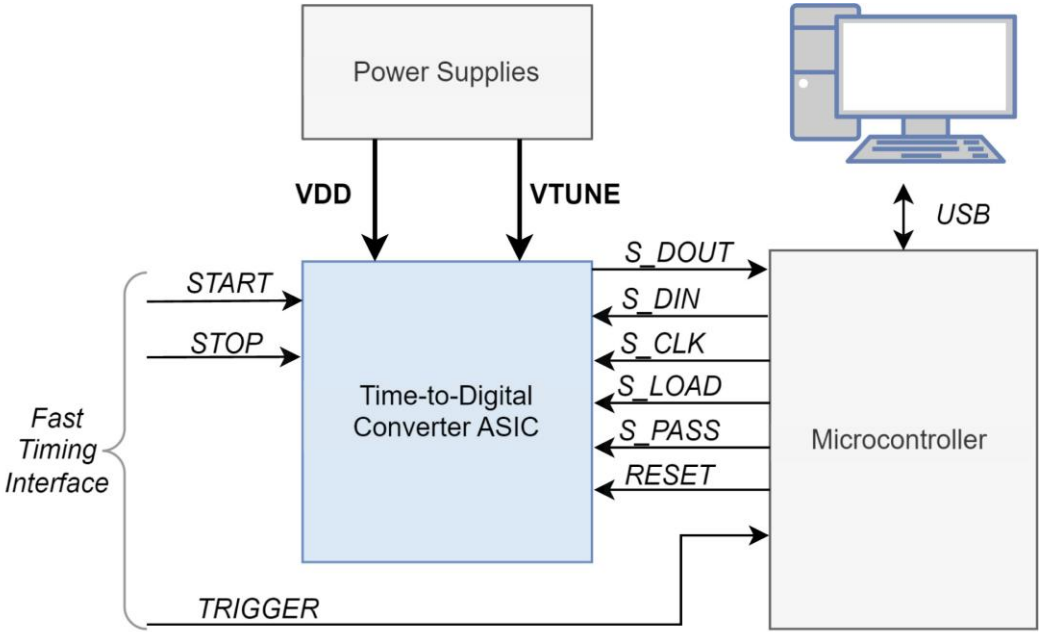
Testing the CryoTDC

Test Sequence:

- Pulse generator (745-OEM) sends START + STOP to ASIC and TRIGGER to microcontroller.
- ASIC computes $t_{STOP} - t_{START}$ and stores it to an on-chip register.
- After a short delay, the microcontroller reads the value in the on-chip register.

To calibrate resolution, fixed time offset pulses (0 ps, 100 ps, 10 ns) are supplied and coefficients are calculated off-chip.



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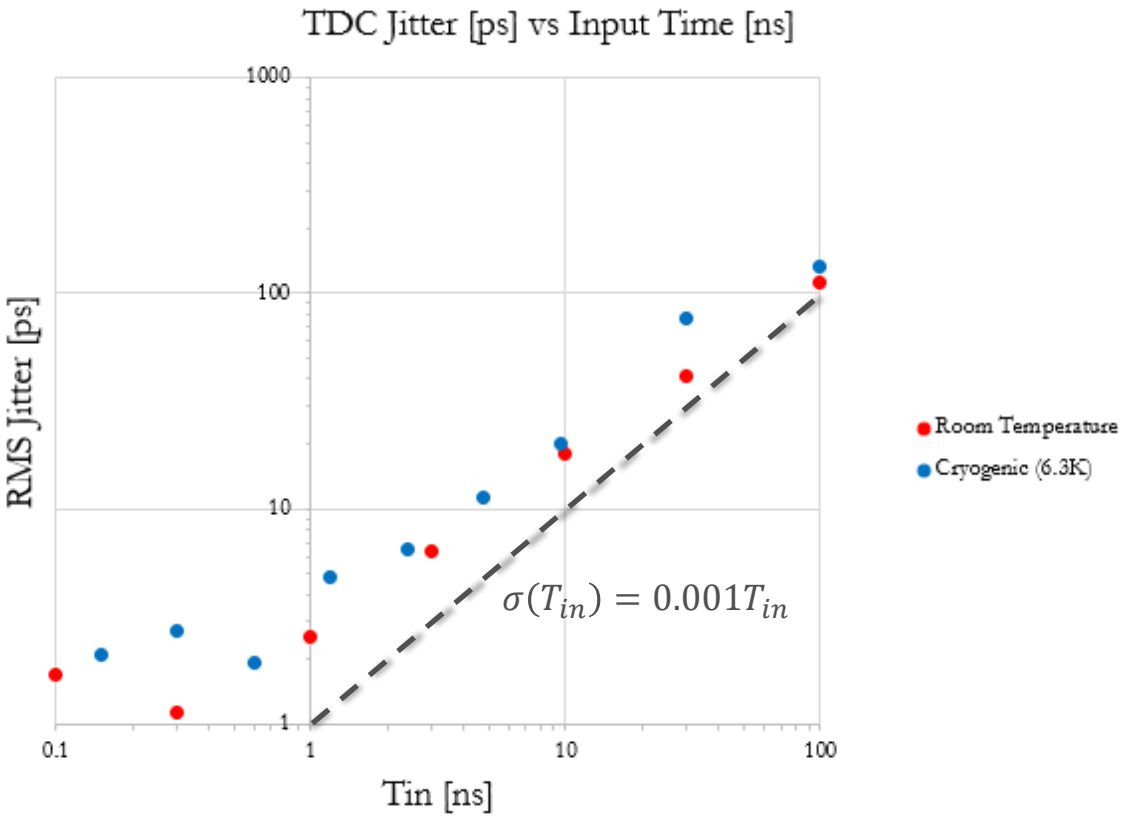
Result: Jitter vs T_{in}

- At low T_{in}, test instrument jitter dominates the measurement.
- At high T_{in}, jitter accumulation in the ring oscillator results in a linear correlation.
- Flicker noise dominates thermal noise, so cryogenic results resemble warm.



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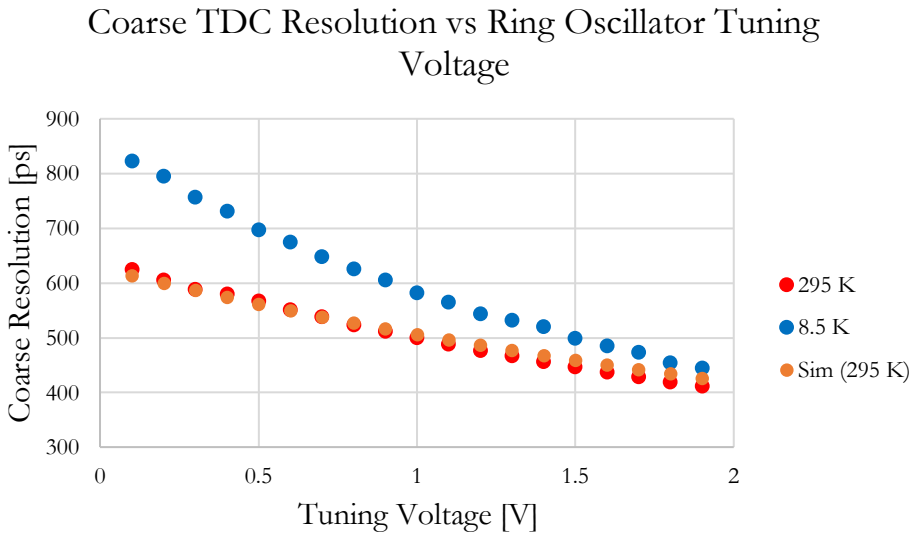
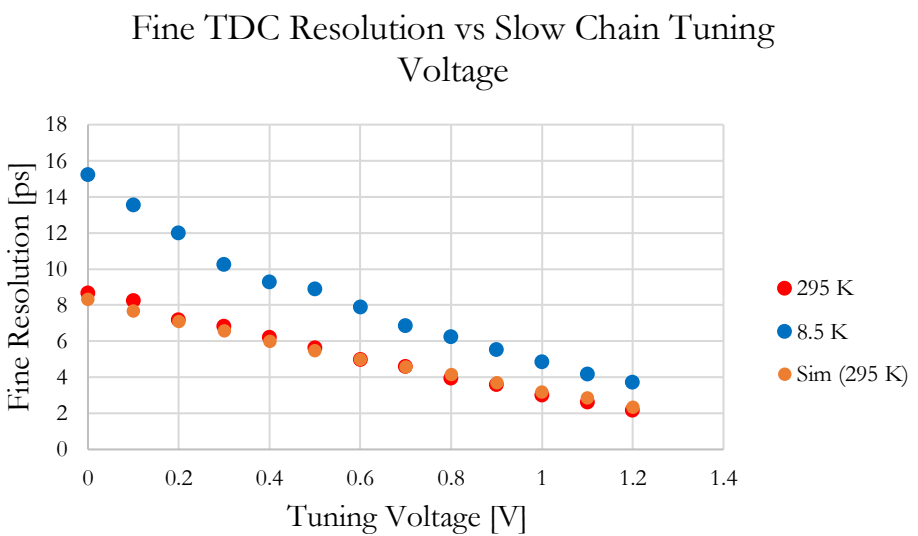
Back-Gate Tuning





- PMOS tuning voltage is inverse to NMOS to balance rise/fall times.
- Good agreement with simulation results at room temperature
- RoomT TDC Tuning slope: ≈**118 ps/V (coarse)** ≈**5.4 ps/V (fine)**
- Cryo TDC Tuning Slope: ≈**216 ps/V (coarse)** ≈**9.6 ps/V (fine)**

Power and Operation Speed

- Testbench maximum readout rate is **~1 Mcps**, limited by microcontroller I/O. The fine TDC is designed to operate at **~100 Mcps**.
- To estimate power at higher frequencies, we assume:

$$P\left(f_{samp}\right) = P_{RO} t_{RO} f_{samp} + E_{fine} f_{samp} + P_{Quiescent}$$

- P_{RO} and $P_{Quiescent}$ can be measured. We make a conservative assumption on t_{RO} and fit E_{fine} from low-speed data.

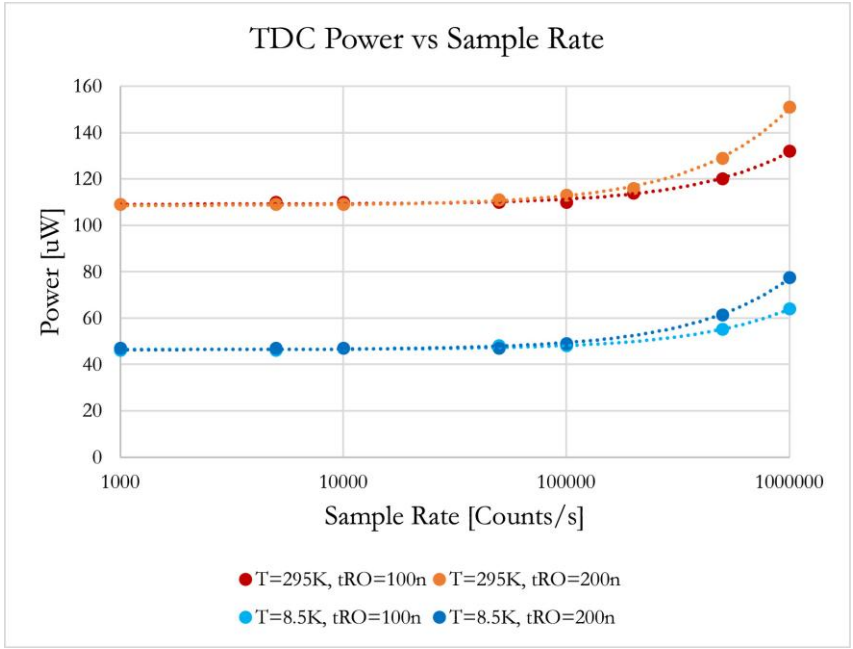
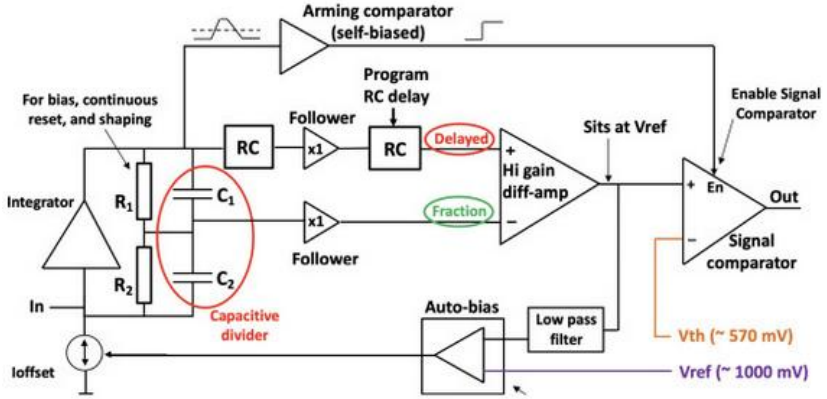
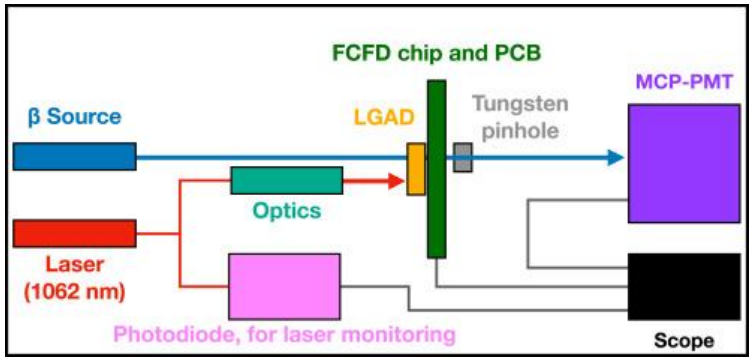


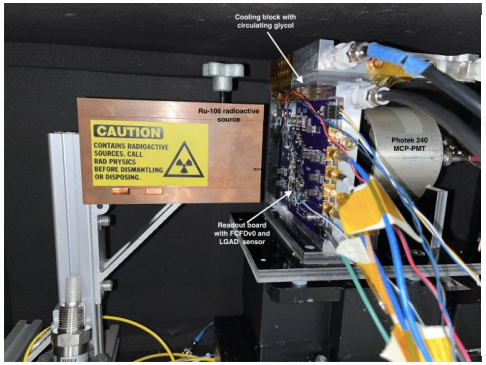
Figure of merit	295 K	8.5 K
Quiescent Power ($P_{Quiescent}$, µW)	109	46.6
Energy per fine ADC Conversion (E_{fine}, pJ)	3.30	3.03
Ring Oscillator Power (P_{RO}, µW)	193	142
Estimated Channel Power at 100 kcps (µW)	110	47
Estimated Channel Power at 100 Mcps (µW)	632	492

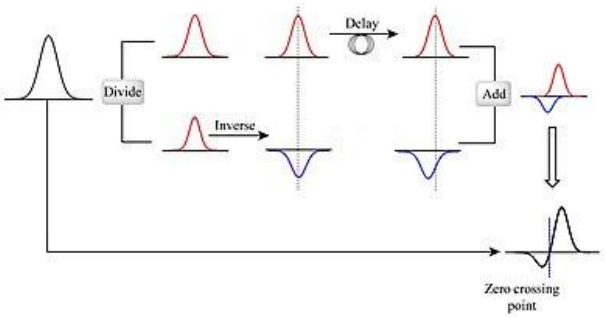
The Fermilab Constant-Fraction Discriminator (FCFD)

- FCFDv0 is a front-end readout chip for LGADs which uses CFD to locally compensate for input signal time walk.
- The FCFD includes pulse injection (5~26 fC) which mimics LGAD signals for easy characterization.









Images from [11]

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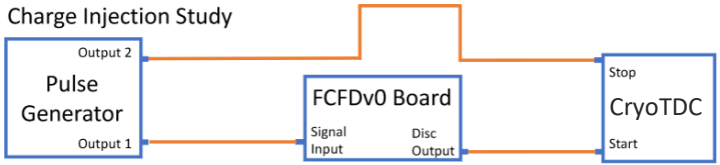
Readout Results with FCFD

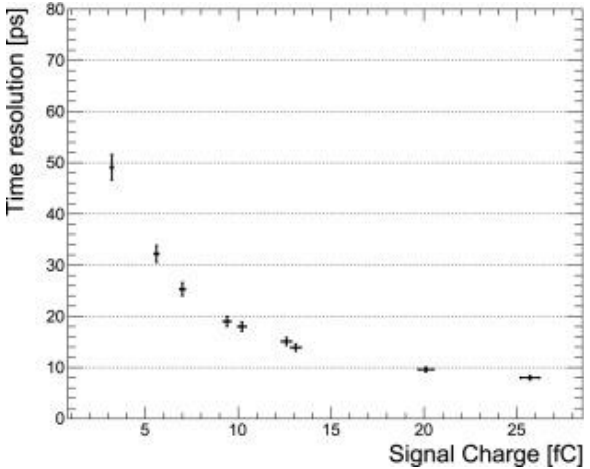
- CryoTDC v1 achieves sensor-limited readout fidelity with FCFDv0.
- Intrinsic readout RMS noise O(5ps).

Pulse Generator Study

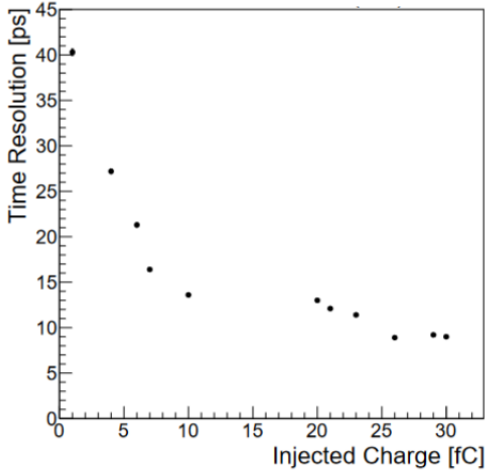
Charge Injection Study



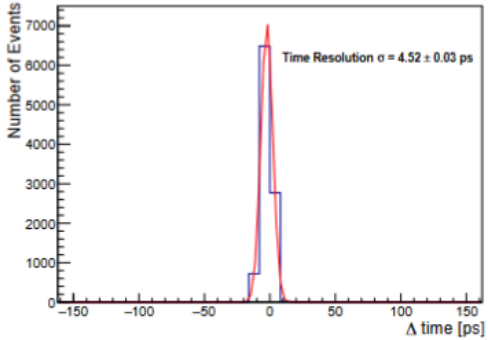
Time Resolution vs Injected Charge Measured with an Oscilloscope (reference) [11]



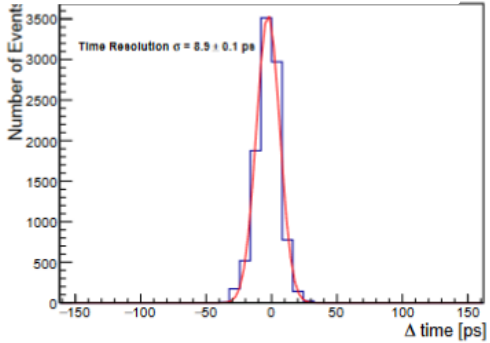
Time Resolution vs Injected Charge Digitized with CryoTDC v1



RMS Noise (Pulse Generator → CryoTDC v1)



RMS Noise (FCFD (26 fC) → CryoTDC v1)



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Summary of Figures of Merit

Reference	Dutton 2015 (ISSCC)	Roy 2017 (TRPMS)	Zhang 2019 (JSSC)	Nolet 2020 (IET)	Talala 2023 (JSSC)	Pass 2023 (ICEE)	This Work	
Technology (nm)	130	65	180	65	110	65	22 FDSOI	
# of Channels	1	4	144 x 6 x 2	1	256	Sim	1	
Cryogenic Results	None	None	None	None	None	None	8.5 K	
Resolution (ps)	71	6.9	48.8	5.5	25.4	20	295K	8.5K
							6.20	8.52
TDC Area (mm^2)	0.03	0.00125	0.025	0.00151	0.024	0.002704	0.003	
TDC Power (mW)	14.1	0.16	2.9	0.02	0.11	0.32	295K	8.5K
							0.63	0.49
Range (ns)	18.8	3	200	4	3.25	168	**	
Conversion Rate (MS/s)	14000	5	666	1	0.28	5	100	
Figure of Merit (Rate/Res.×Pow. ×Area)	466	3620	188	5470	4.2	289	295K	8.5K
							8530	7980

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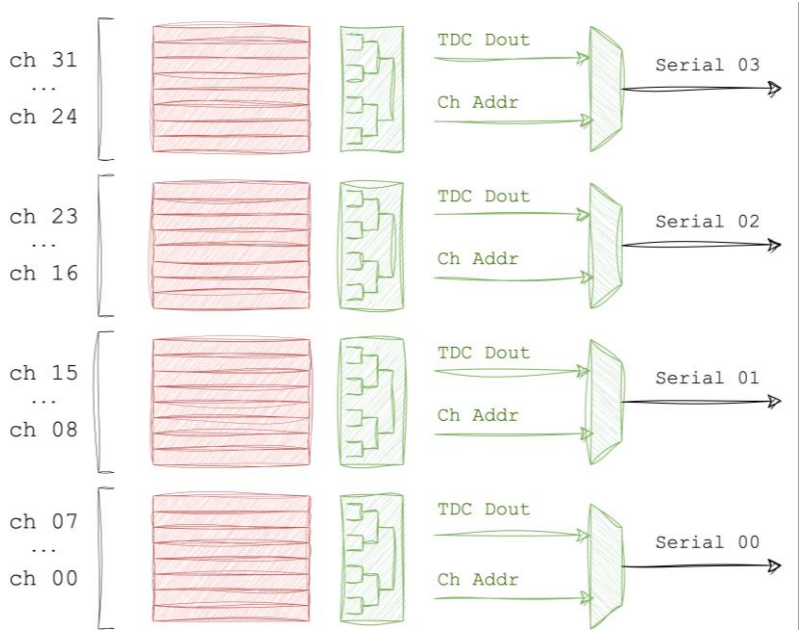
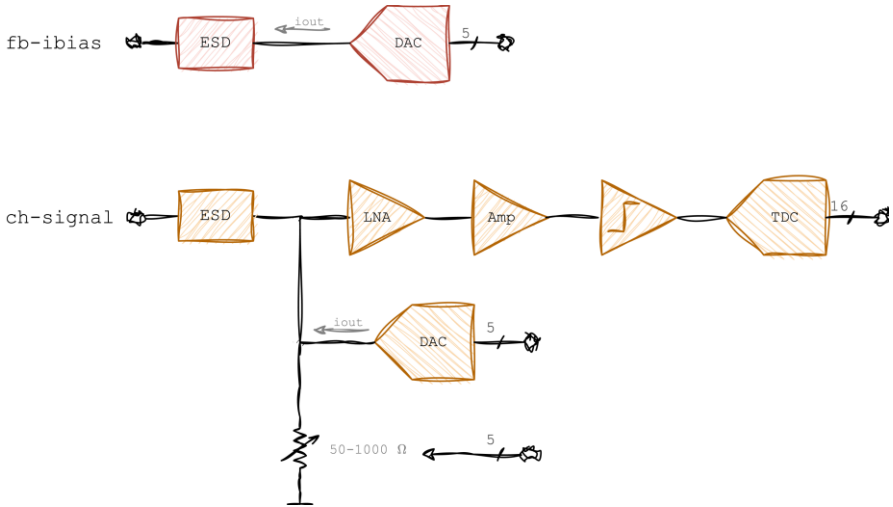
Further Developments

SUNROCK

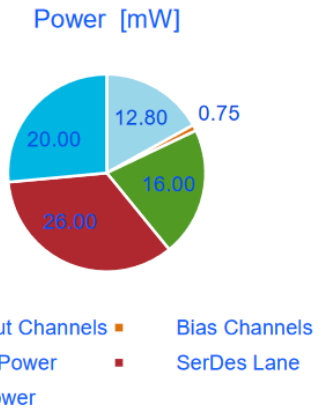
- 32x channels, a shared clock and readout architecture, and DC biasing for SNSPDs.

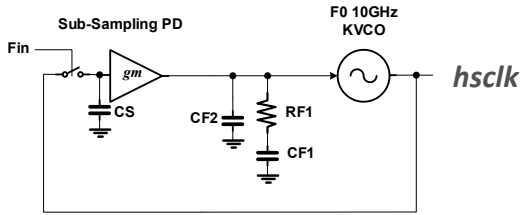


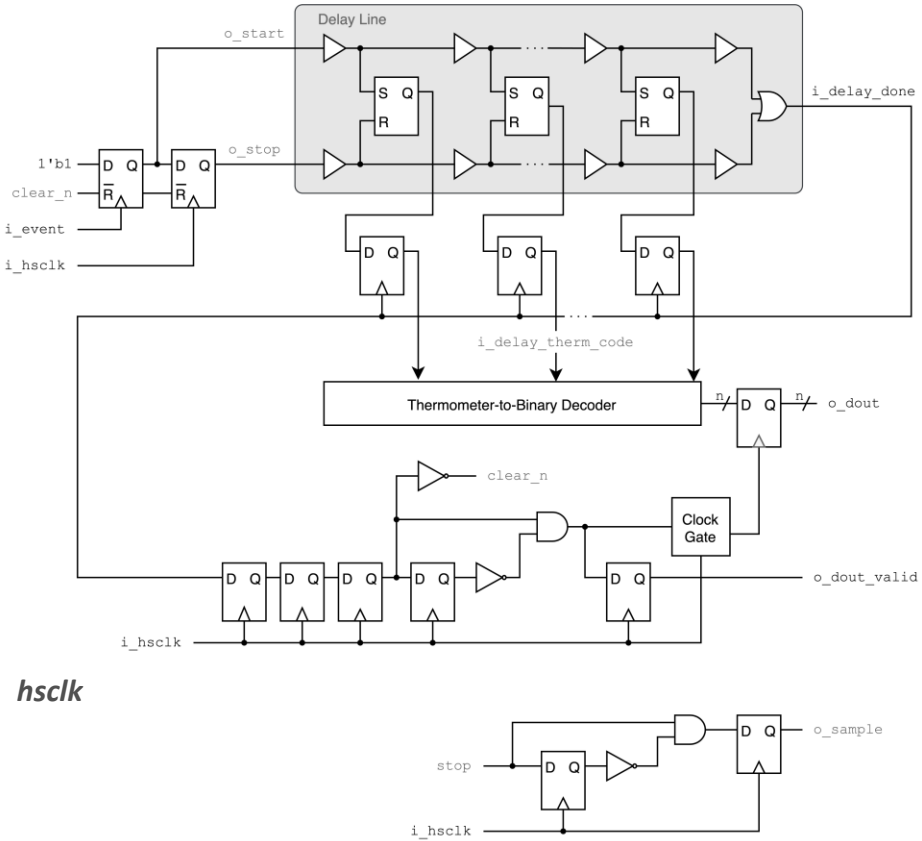


SUNROCK TDC Architecture

- Fine TDC design essentially identical to CryoTDC v1.
- Coarse counter is clocked by *hsclk*
- *hsclk* (10.0 GHz) is produced on-chip by a novel cryogenic sampling PLL with ~10fs rms jitter.







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SUNROCK Test Chip

- Successfully taped out.
- Testing has been significantly delayed due to engineering resources but is currently underway.

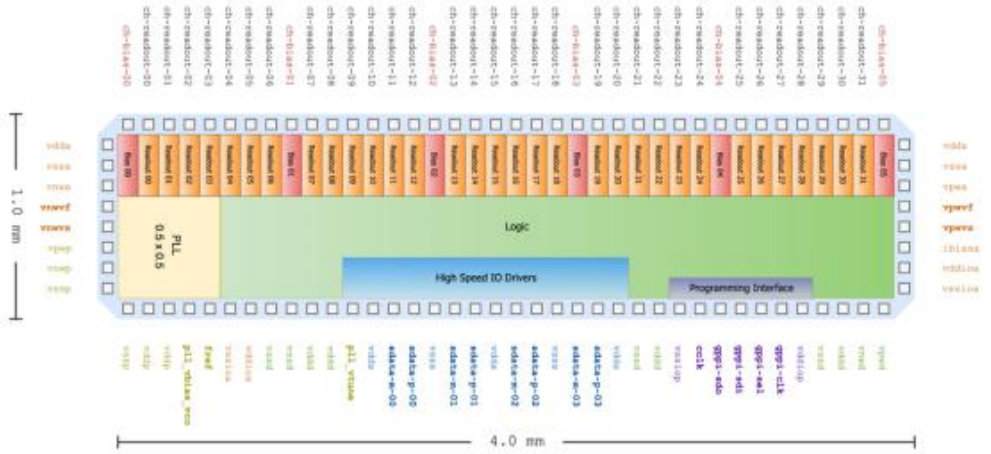

Figure 1. High-Level Floorplan of SUNROCK ASIC

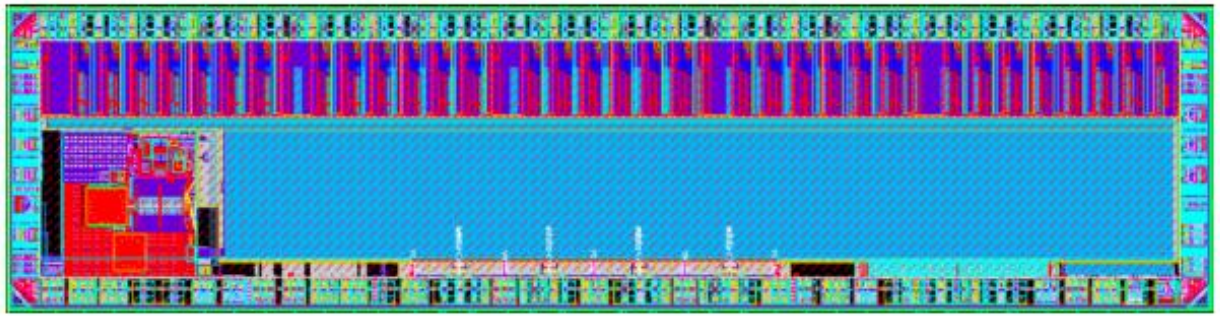

Figure 2. Detailed Layout Screenshot of SUNROCK ASIC

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Thank you for your attention!

Please direct any questions or feedback to:

aquinn [at] fnal [dot] gov

More Fermilab Talks this Week:

"Smart Pixels: In-Pixel AI for on-sensor data filtering"
Benjamin Parpillon – Weds @ 11:00 am

"Constant Fraction Discriminator Readout Chip for ePIC"
Artur Apresyan – Thurs @ 11:30 am

For more technical info, check out our NIM-A Paper:

A sub-5 ps jitter time-to-digital converter ASIC with back-gate delay tuning in 22 nm CMOS

Adam Quinn [a 1], Si Xie [a b 1], Artur Apreysan [a], Farah Fahim [a], Sergey Los [a], Cristián Peña [a], Carlos Eugenio Perez Lara [a 2], Tom Zimmerman [a], Davide Braga [a]

[a] Fermi National Accelerator Laboratory, PO Box 500, Batavia, 60510-5011, IL, USA
[b] California Institute of Technology, 1200 E California Blvd, Pasadena, 91125, CA, USA

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Backup

References

[1] Harbaugh, J. (2017, May 22). *Deep Space Optical Communications (DSOC)*. NASA. Retrieved October 3, 2021, from https://www.nasa.gov/mission_pages/tdm/dsoc/index.html.

[2] Jet Propulsion Laboratory, California Institute of Technology. (2018). *Superconducting Nanowire Single Photon Detectors For Deep Space Optical Communication*.

[3] Ho, R., Mai, K., & Horowitz, M. (2001). The future of wires. *Proc. IEEE, 89*, 490-504.

[4] Fermi National Accelerator Laboratory. (2021). *Joint DOE-NASA development of custom readout electronics for Superconducting Nanowire Single Photon Detector* (p. 1).

[5] SLAC National Accelerator Laboratory. *TDC development for future detectors: Initial technology evaluation*. U.S. Department of Energy Office of Science.

[6] P. Dudek, S. Szczepanski and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," in *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 240-247, Feb. 2000, doi: 10.1109/4.823449.

[7] R. Enomoto, T. Iizuka, T. Koga, T. Nakura and K. Asada, "A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18- μm CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 1, pp. 11-19, Jan. 2019, doi: 10.1109/TVLSI.2018.2867505.

[8] B. V. Bockel, P. Leroux and J. Prinzie, "Tradeoffs in Time-to-Digital Converter Architectures for Harsh Radiation Environments," in *IEEE Transactions on Instrumentation and Measurement*, vol. 70, pp. 1-10, 2021, Art no. 2005710, doi: 10.1109/TIM.2021.3100355.

[9] Global Foundries. *22FDX Design Kit and Technology Training Book.* TTM-000022 Revision 9.

[10] Hu, Jianyong & Yu, Bo & Jing, Ming-Yong & Xiao, Liantuan & Jia, Suotang & Qin, Guo-Qing & Long, Gui. (2016). Experimental quantum secure direct communication with single photons. Light: Science & Applications. 5. e16144. 10.1038/lsa.2016.144.

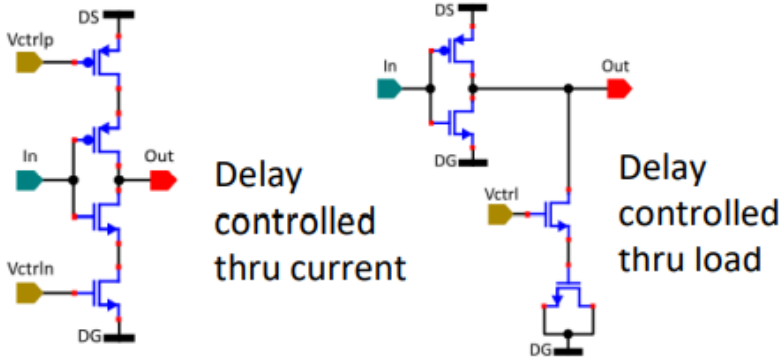
References, Cont'd

[11] Si Xie, Artur Apresyan, Ryan Heller, Christopher Madrid, Irene Dutta, Aram Hayrapetyan, Sergey Los, Cristián Peña, Tom Zimmerman, *Design and performance of the Fermilab Constant Fraction Discriminator ASIC,* Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, Volume 1056, 2023, 168655, ISSN 0168-9002, https://doi.org/10.1016/j.nima.2023.168655. (https://www.sciencedirect.com/science/article/pii/S0168900223006459)

Traditional Tuning Methods

$$\text{Delay} \propto \frac{I}{C}$$

- Current starved:
- Shunt capacitor:



SLAC [5]

Tuning is important!

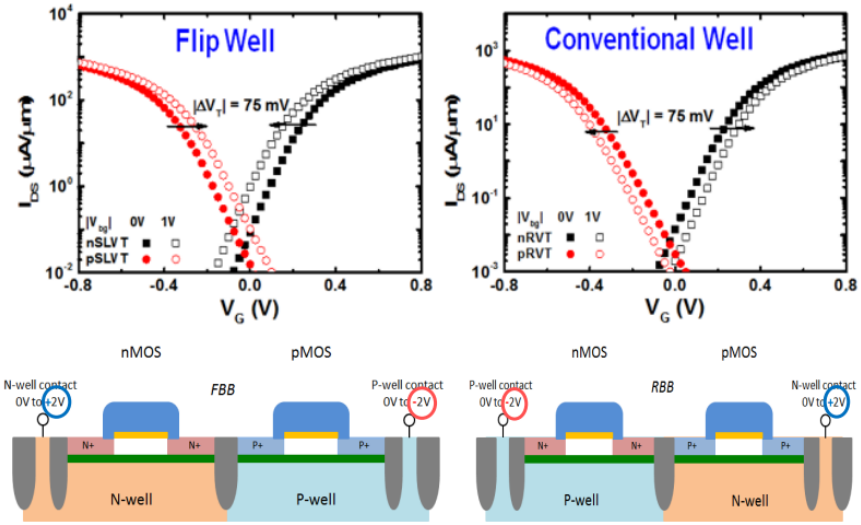
- Small PVT variation in t_1, t_2 → big variation in t_R

But comes with a lot of side-effects:

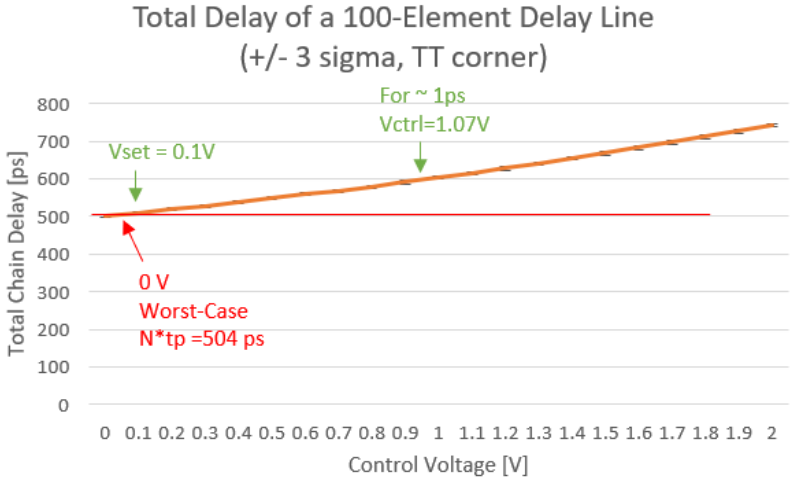
- Parasitic R, C even at maximum V_{ctrl}
- Die area doubled (or more)
- Tuning FET noise contribution

What if we could tune t_1, t_2 without adding **any** FETs?

22FDX Back-Gate Biasing



GF 22FDX Training Manual [9]



Back-gate biasing modulates V_{Th}, changing drive strength and thus delay.

DILVERT has six independent bias voltages:

$$V_{tune\_p\_fast}, V_{tune\_n\_fast}$$
$$V_{tune\_p\_slow}, V_{tune\_n\_slow}$$
$$V_{tune\_p\_RO}, V_{tune\_n\_RO}$$

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TDC Characteristic Equation Derivation

The relationship between T_{in} and the TDC digital codes may be derived as follows, starting from the definition:

$$T_{in} = T\left(stop\right) - T\left(start\right) \tag{1}$$

Letting $T\left(start\right) = 0$ and noting that the *stop* signal directly triggers $start_{fine}$ we have:

$$T_{in} = T\left(start_{fine}\right) \tag{2}$$

The characteristic equation of the fine TDC is:
$T_{lsb(fine)} Q_{fine} = T\left(stop_{fine}\right) - T\left(start_{fine}\right)$. Substituting (2) yields:

$$T_{in} = -T_{lsb(fine)} Q_{fine} + T\left(stop_{fine}\right) \tag{3}$$

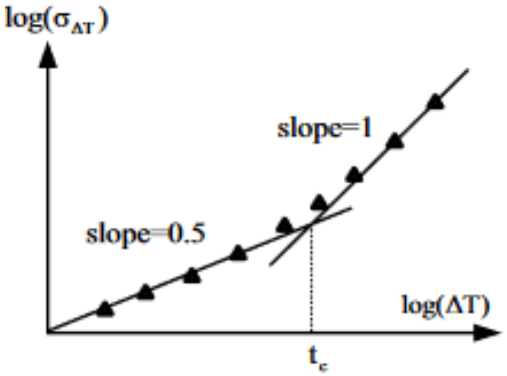
Finally, due to the fixed propagation delay from DFF1 through DFF2, we note that:
$T\left(stop_{fine}\right) = T_{lsb(coarse)} Q_{coarse} + T_{gd}$, so we have:

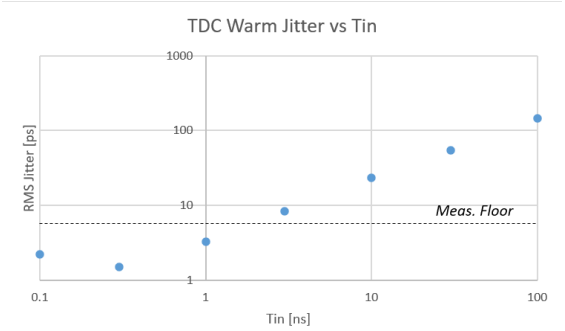
$$T_{in} = -T_{lsb(fine)} Q_{fine} + T_{lsb(coarse)} Q_{coarse} + T_{gd} \tag{4}$$

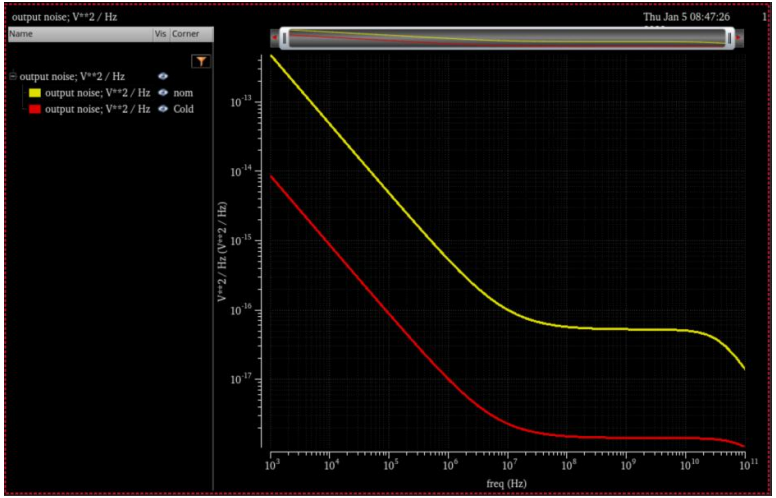
The three calibration parameters $T_{lsb(fine)}$, $T_{lsb(coarse)}$, and T_{gd} may be calculated by applying pulses of known length to the input of the TDC. After establishing these values, T_{in} may be calculated from Q_{coarse} and Q_{fine}.

Flicker Noise Contribution

- For a free-running RO, $\sigma_{\Delta T}$ is dominated by thermal noise at low ΔT, flicker at high ΔT.
- Our TDC shows $\sigma_{\Delta T} \propto \Delta T$ which is characteristic of flicker noise.
- Empirical models give $t_c \approx \frac{1}{36 f_c}$. For the inverters in DILVERT RO, $f_c \approx 10\ \mathrm{MHz}$, so $t_c \approx 2.7\ \mathrm{ns}$. (From measurement, $t_c \approx 0.5$ to $5\ \mathrm{ns}$, limited by Meas. Floor)







C. Liu and J. McNeill, "Jitter in oscillators with 1/f noise sources," in Proc. IEEE Int. Symp. Circuits and Systems (ISCAS), 2004, pp. 773–776.

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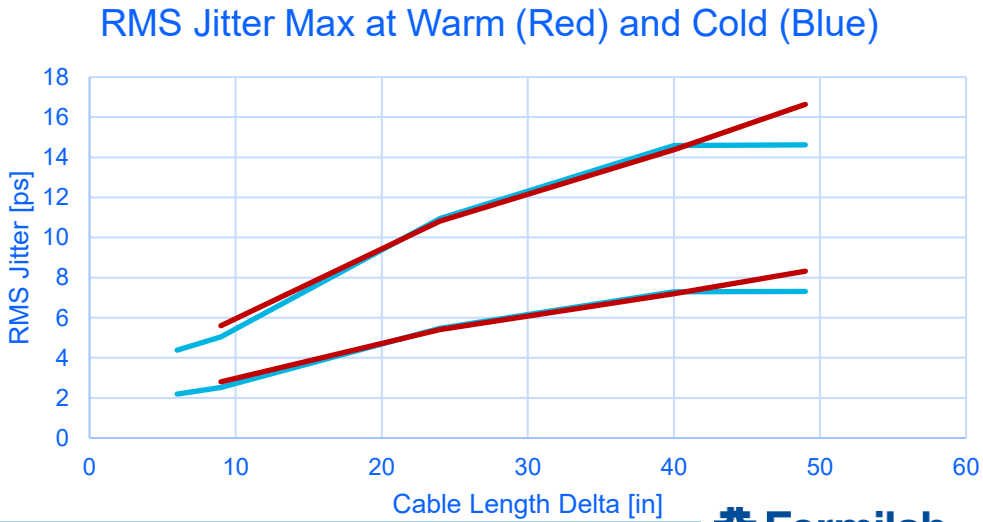
(Update 2/7/2023) Splitter Noise Measurements

Goal: Estimate the jitter performance possible from DILVERT fine TDC.

- Eliminate instrumentation noise by using a cable delta + splitter to generate START/STOP.
- Circumvent issues with calibration + course counts by examining fine counts.

Delta/Temp	Avg Qfine	RMS Noise [LSB]	For LSB=6ps	For LSB=12ps
6in 6K	21.73046	0.364787008	2.19	4.38
9in 6K	41.91884	0.419846533	2.52	5.04
24in 6K	72.61523	0.912814773	5.48	10.95
40in 6K	69.48798	1.215260398	7.29	14.58
49in 6K	65.08617	1.218580317	7.31	14.62
9in 296K	53.37575	0.466708555	2.8	5.6
24in 296K	44.07214	0.901775747	5.41	10.82
40in 296K	94.71844	1.197597789	7.19	14.37
49in 296K	74.44589	1.387048054	8.32	16.64



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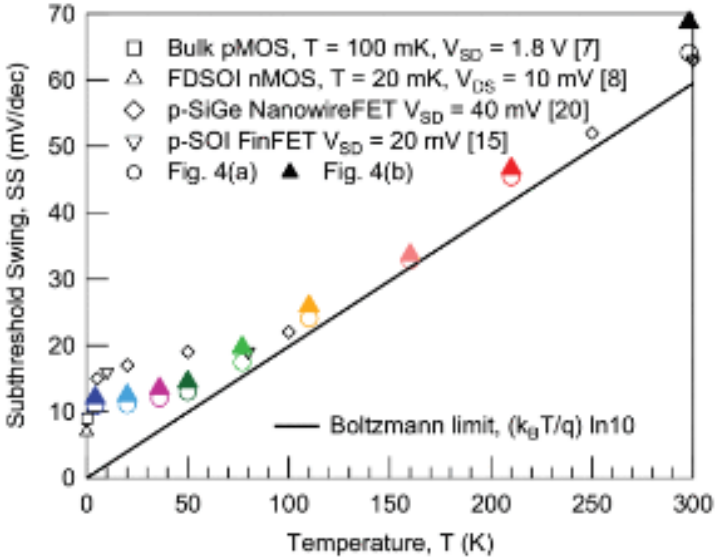
Our Model Approach

- Start with foundry PDK provided by GF --> **re-extract** the parameters we think will change at cryo
- Constrain the parameters to reasonable ranges based on physics expectations and literature when applicable
- **Isothermal** model at 3.8K
- Change the input pdk:
  - BSIM-IMG 102.8 doesn't include effects like subthreshold slope saturation [14][18] (but the latest BSIM-IMG 102.9.6 does)
  - We model that by setting **temp** to the value where our **subthreshold slope saturates**
  - **Set temp** = **tnom** to remove temp dependent params
- Extracted values back into the PDK



Subthreshold Swing Saturation as a function of Temperature for various devices [18]

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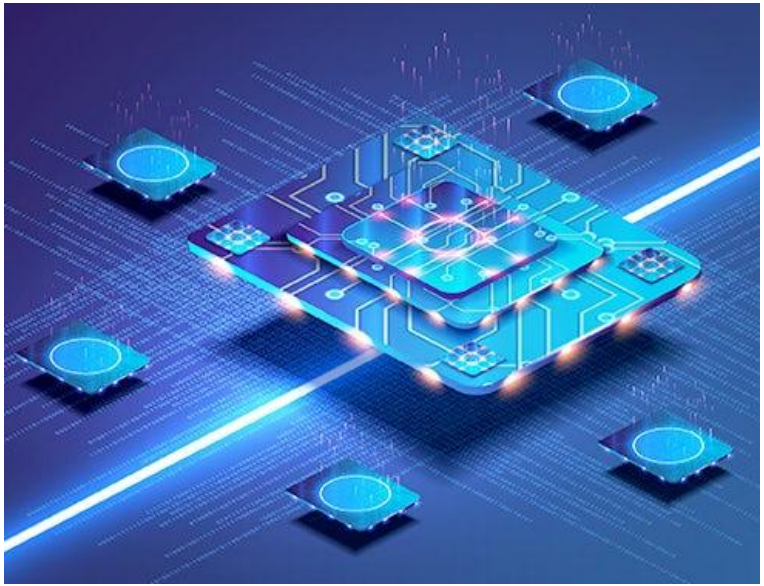
Design Goals for the next 20 years: Enable Smart Sensors

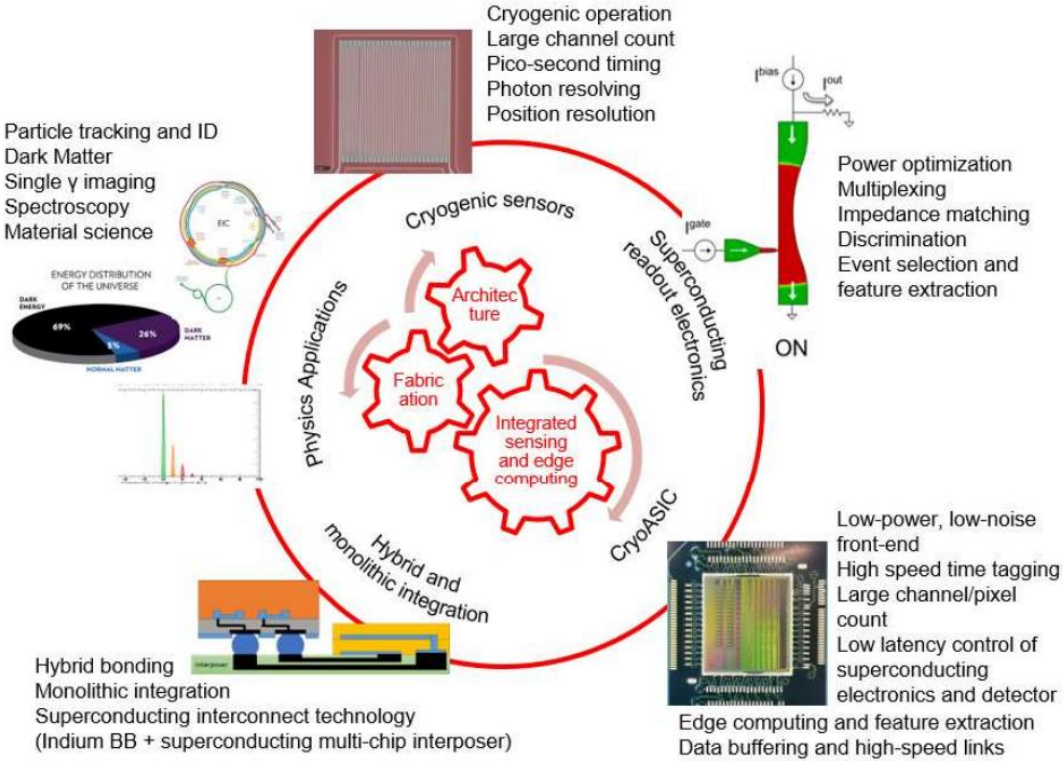
- Novel sensors; CMOS sensors
- Low power, low noise, ultra-sensitive analog for sensor signals
- Advanced digital architectures and verification methods
- AI-on-chip, Quantum cryoelectronics, 6G and beyond
- Integrated high speed communication between modules and off-detector



Extremely important to work with industry to leverage production-scale processing

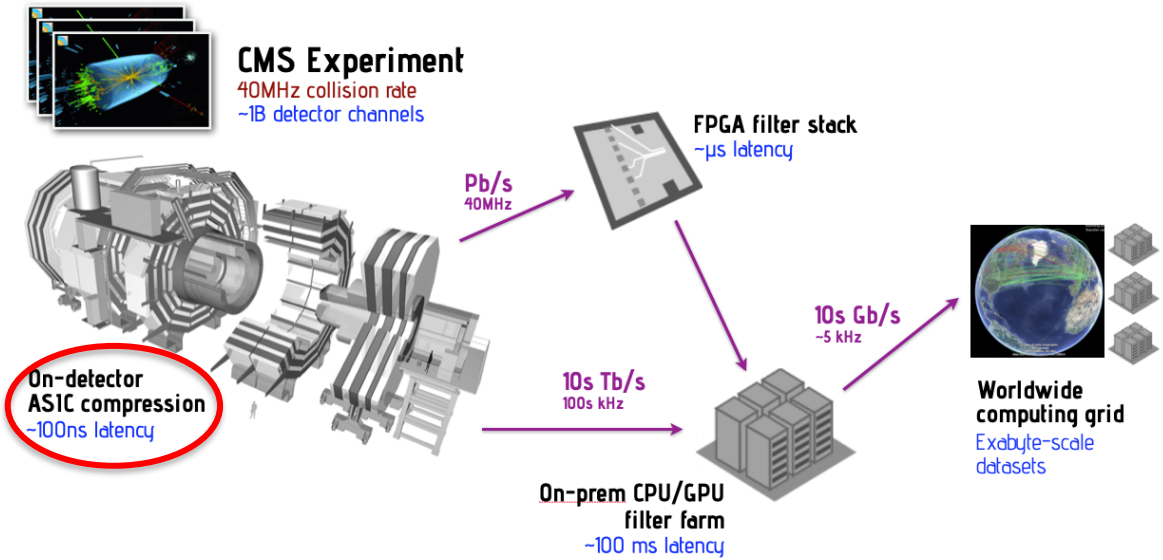
Microelectronics at Fermilab: Quantum/Cryo Analog

- Advances in HEP, DM detection, quantum imaging demand better detectors:
  - → Extreme **spatial/temporal resolution**
  - → Extreme **environments** (cryo, rad-hard)
  - → Extremely **low noise** (< 1 e-)
- Beyond CMOS technology demonstration:
  - → **Cryo silicon photonics**
  - → **Superconducting readout**
  - → **Quantum instrumentation**

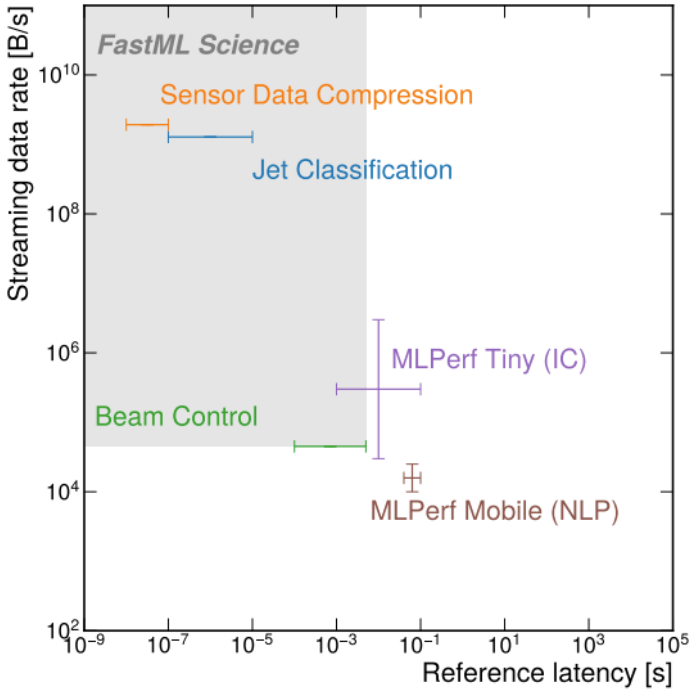


Microelectronics at Fermilab: Digital & ML

- Ever-higher luminosity and event rates in particle trackers create a “data deluge”
- Need data compression at the edge, or valuable physics data will be lost.

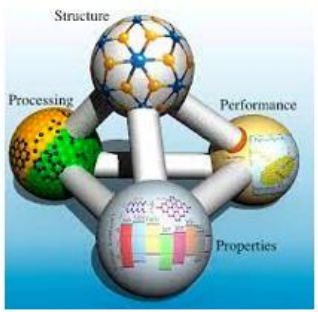


FoMs for Science vs Industry ML



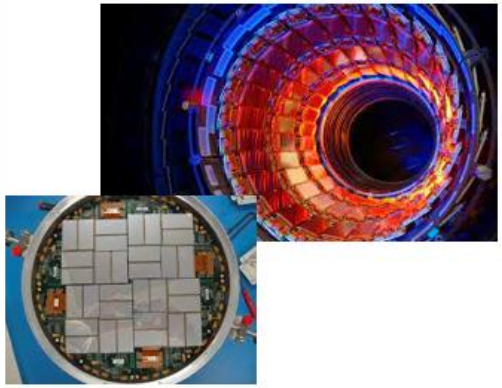
Technology Transfer at National Labs

ACADEMIC RESEARCH



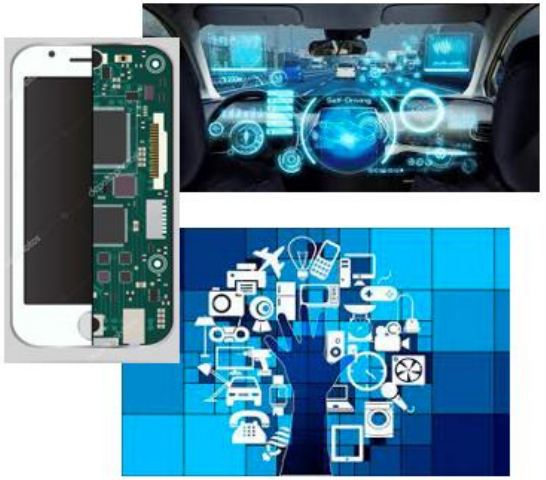
- Support interdisciplinary research
- Enables new scientific discovery and foundational engineering
- Novel solutions
- Mission: new knowledge and education of students

NATIONAL LABS: ADVANCED SCIENTIFIC INSTRUMENTATION



- Support scientific experiments operating in extreme environments
- Mid-size scaling for large experiments
- Mission: robust performance over several decades

INDUSTRY – PRODUCT DRIVEN



- Support consumer electronics
- Mature fabrication facilities
- Mission: incremental product driven design

Increase technology readiness level

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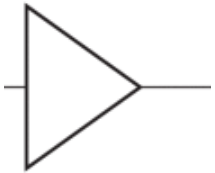
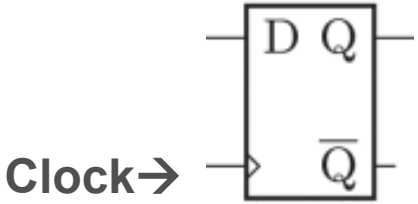
All You Need to Know

Gate



Delays a signal by a few (~20) ps

Flip-Flop



Data (**D**) is captured at the rising edge of **clock**.

Clock	D	Q_{next}
Rising edge	0	0
Rising edge	1	1
Non-rising	X	Q

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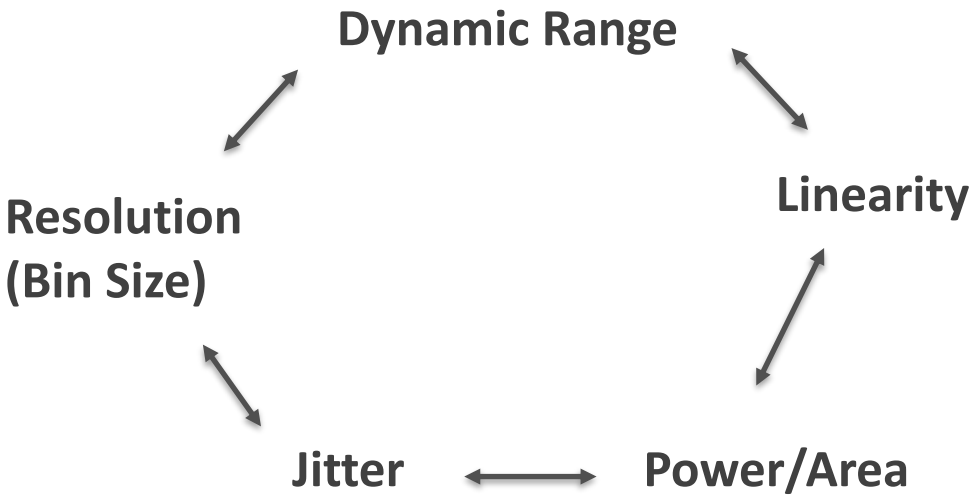
Time-to-Digital Converter Design Trade-offs



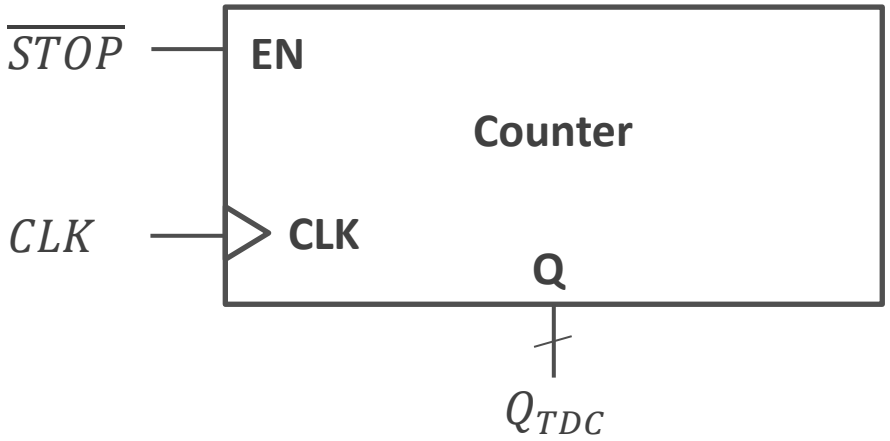
Time-to-Digital Converter = A Counter?

Dynamic Range: $Q_{MAX} \propto 2^N$ 😀

Resolution: T_{CLK} 😟

Other Issues:

- Clock generator?



FO4 scaling (TT, low V_{DD}, high temp)

L_{drawn}	0.18µm	0.13µm	0.10µm	0.07µm	0.05µm	0.035µm
FO4, pS	90	65	50	35	25	17.5
Frequency, GHz	0.7	1	1.25	1.8	2.5	3.6

Ho, et al. [3]

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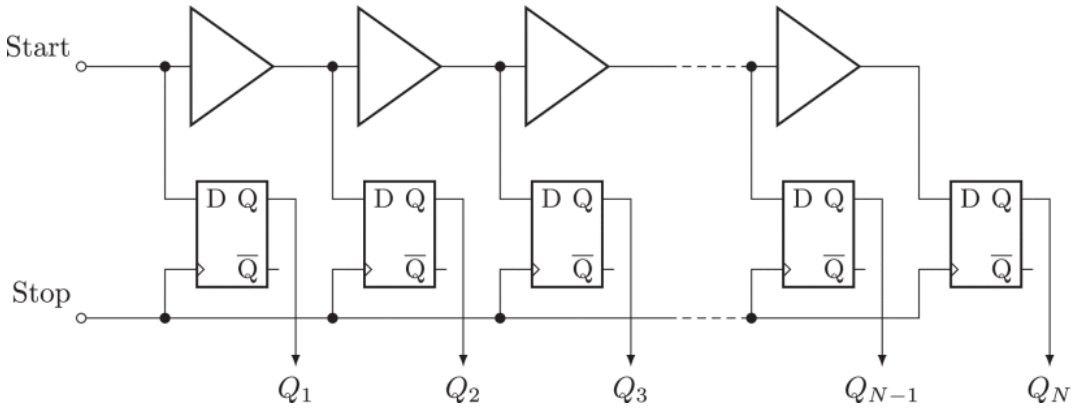
Gate-Level Resolution (Flash TDC)

Dynamic Range: $Q_{MAX} \propto N$ 😟

Resolution: τ_{gate} 😐

Other Issues:

- Linearity & Mismatch
- Thermometer decode
- Delay on the STOP line?



From Bockel [8]

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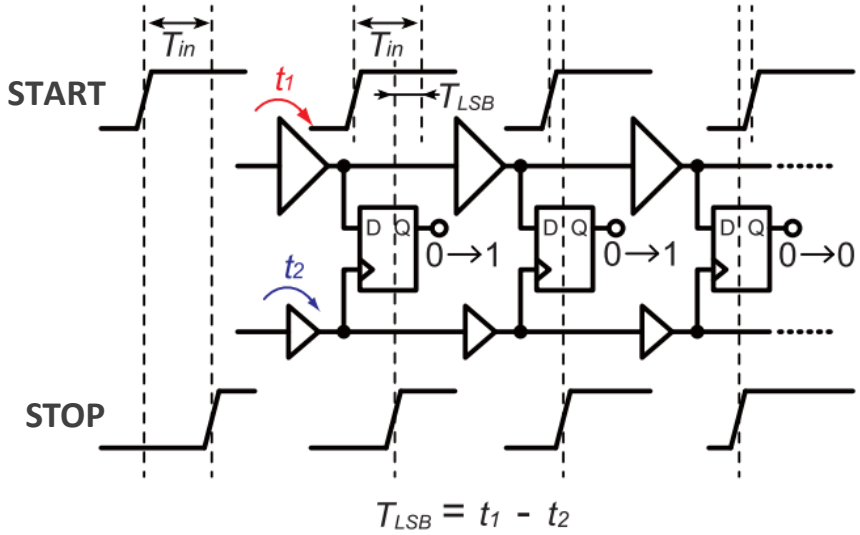
Sub-Gate Resolution (Vernier TDC)

Dynamic Range: $Q_{MAX} \propto N$ 😟

Resolution: $\ll \tau_{gate}$, limited by jitter 😀

Other Issues:

- Linearity & Mismatch
- Need tunable delay elements
- Thermometer decode
- Processing time may be > Dynamic Range



Enomoto [7]

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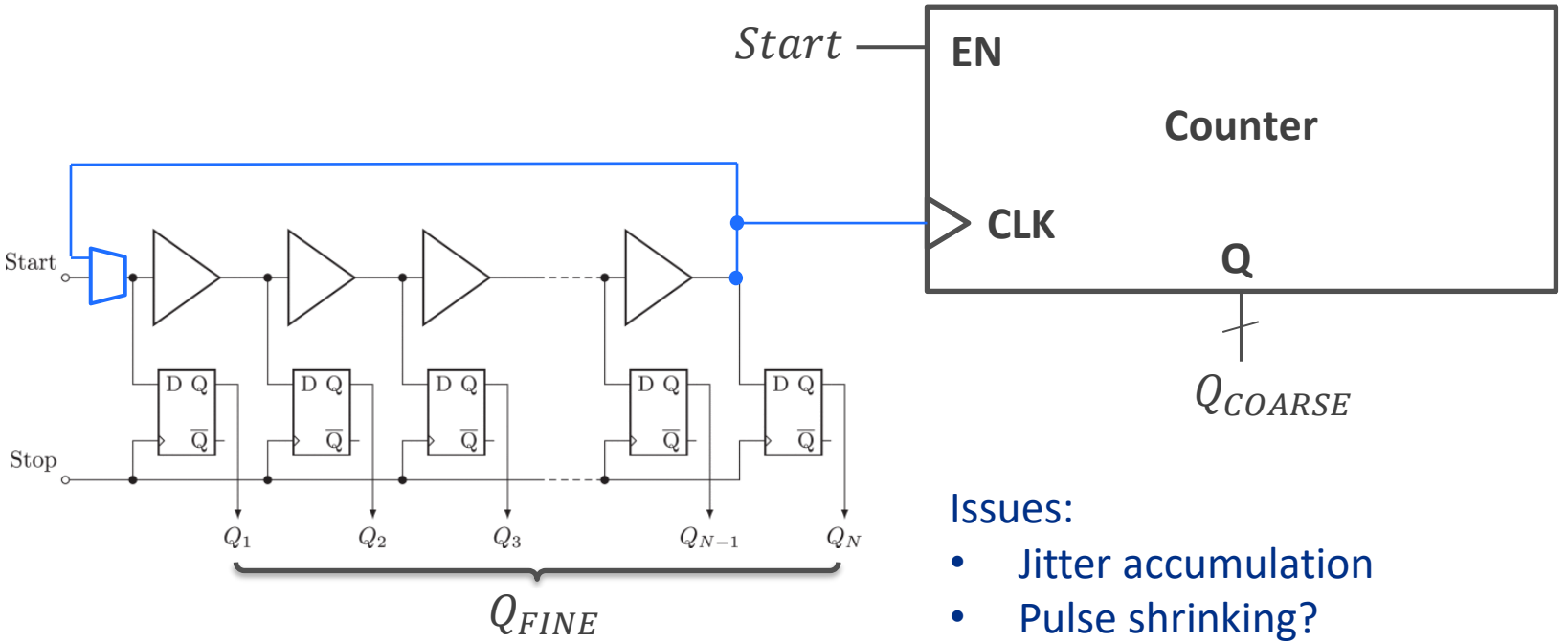
Loop the TDC?



Issues:

- Jitter accumulation
- Pulse shrinking?
- Non-linearity ($C_{parasitic}$ on the CLK line?)

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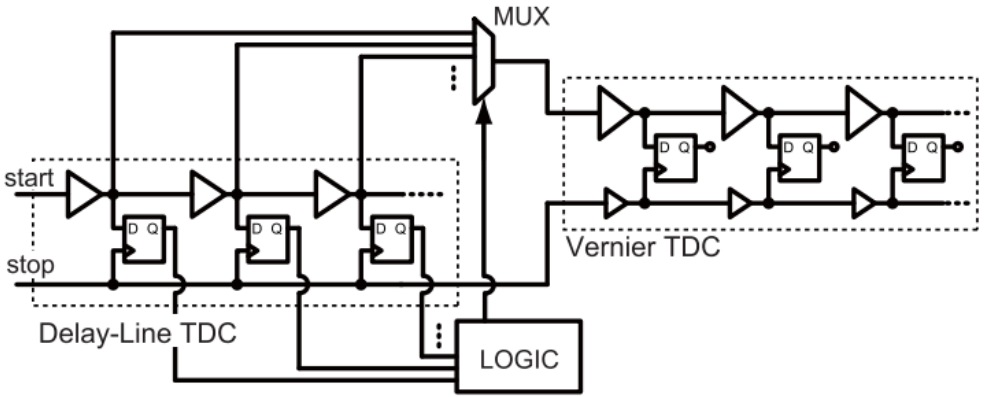
Two-Step TDC?



Enomoto [7]

Big Idea: Fine TDC for resolution, Coarse TDC for dynamic range.

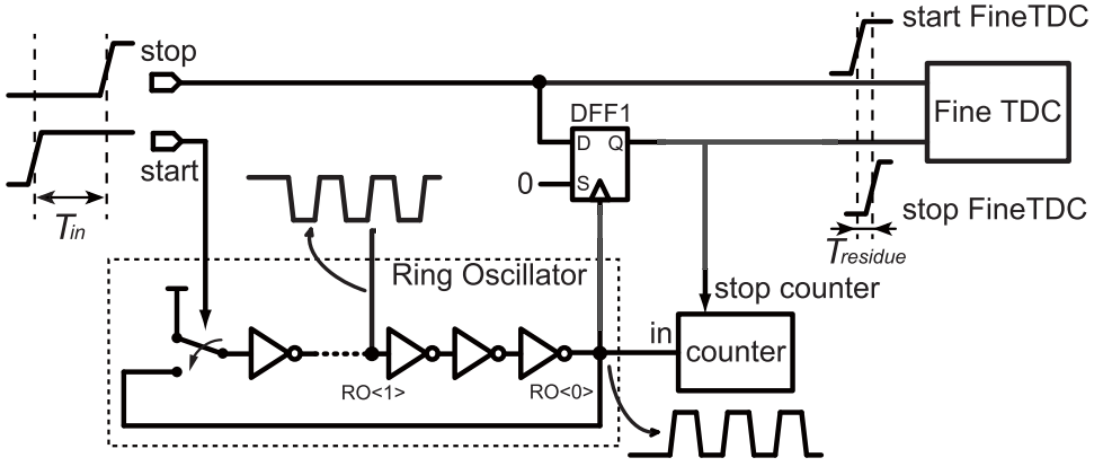
Two “Steps”:

1. START propagates through coarse TDC.
2. When STOP arrives, START is coupled to fine TDC to digitize residual.

Routing complexity $\propto N_{coarse}$

- Area still grows linearly with dynamic range…
- What about MUX/logic delay?

DFF Interlock?



Enomoto [7]

DFF1 aligns STOP_FINE_TDC to the next clock edge.

Now:

$$T_{in} = T_{coarse} - T_{residue}$$

Signal path is always the same → no variable delay.

* But what's the timing relationship between RO<0> and STOP?

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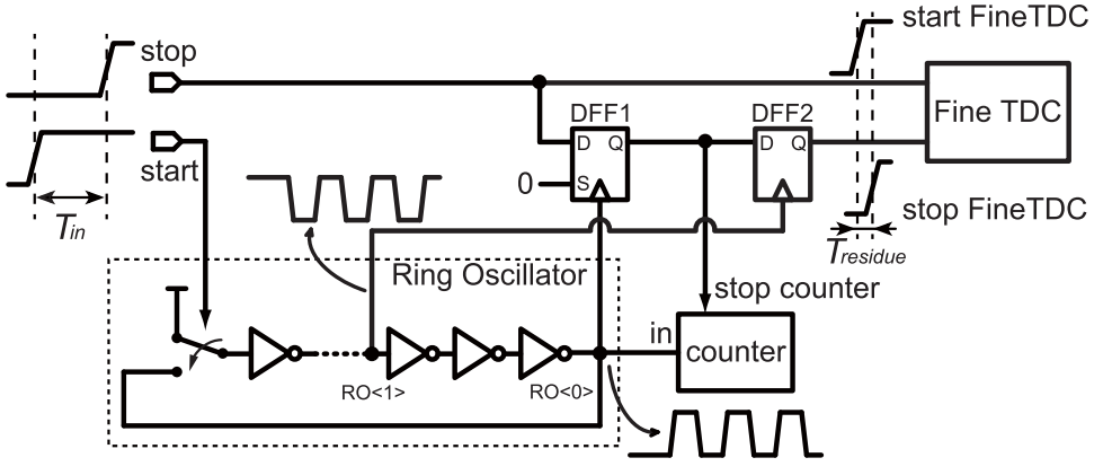
A Better DFF Interlock



Enomoto [7]

DFF1 has the same function as before.

DFF2 suppresses metastability of the halt signal.

Doesn't this introduce delay?
→ Constant, can be calibrated.

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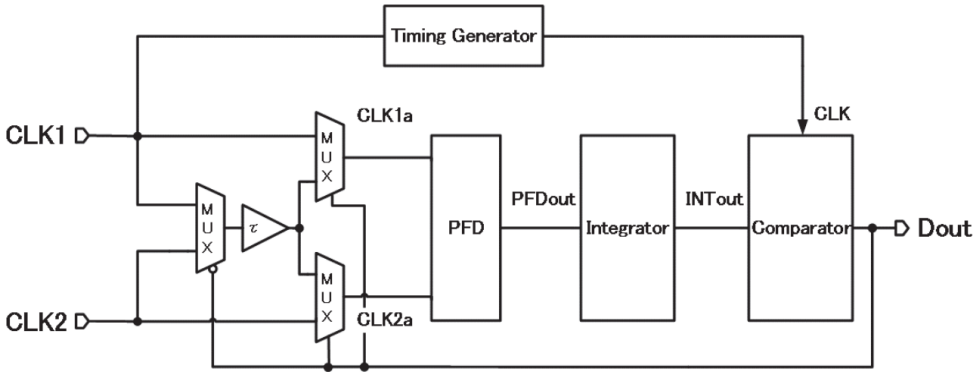
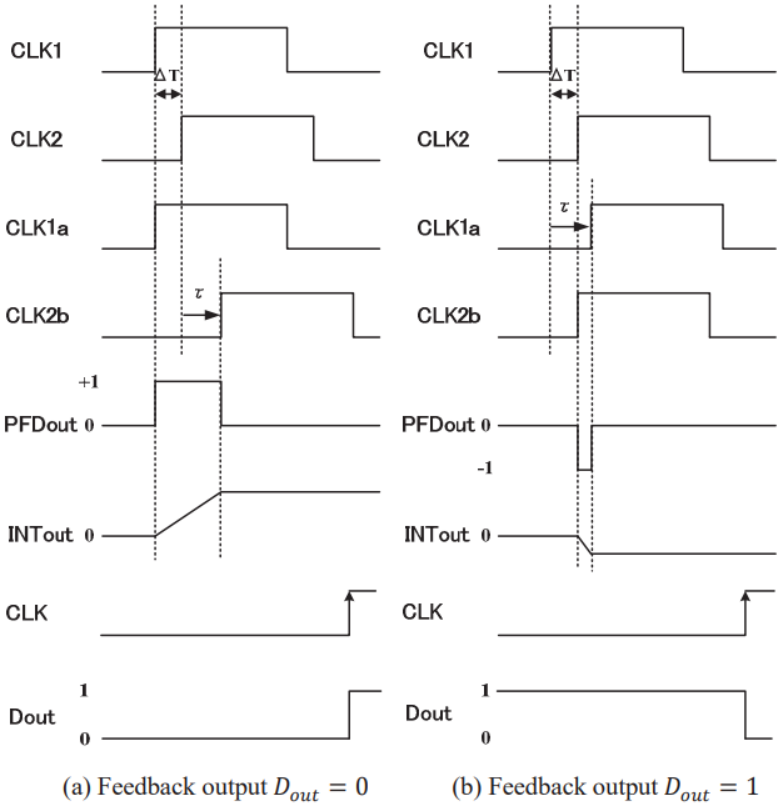
An Aside: Delta-Sigma TDCs





Measure delay offset between clocks:

- One clock signal is delayed, depending on feedback from output.
- Resulting phase difference is integrated.

Excellent resolution, but requires oversampling
→ not very applicable to our application.

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