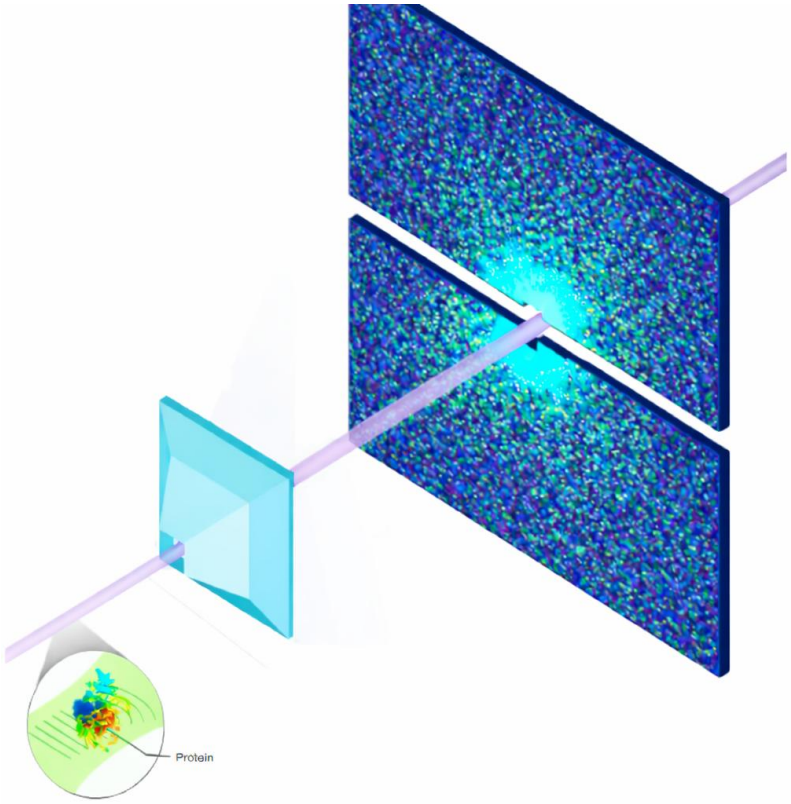

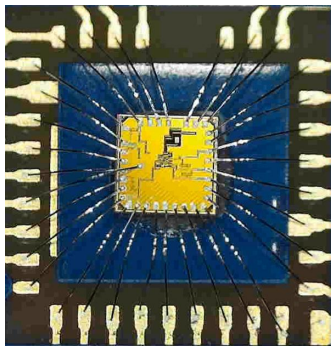

Design and Experimental Validation of a Front-End Stage for Future XFEL Detectors

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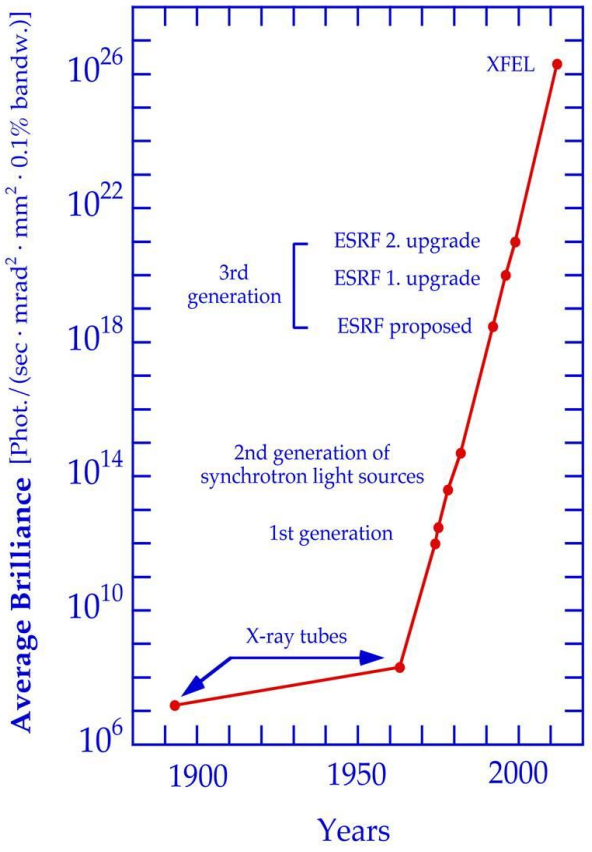
[2]Istituto Nazionale di Fisica Nucleare, Sezione di Milano, Milano, Italy

[3]European XFEL, Schenefeld, Schleswig-Holstein, Germany

[4]Ca' Foscari University of Venice, Department of Molecular Sciences and Nanosystems, Venice, Italy

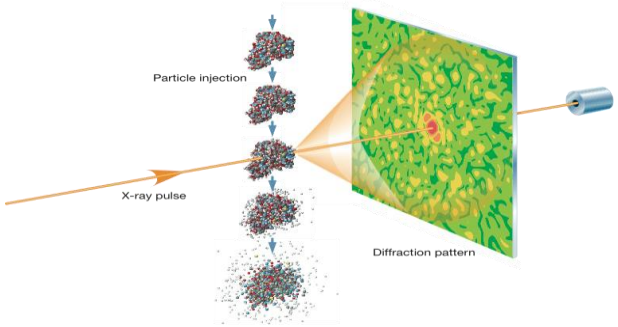
The European XFEL

- The European X-ray Free Electron Laser is a research facility able to generate **ultrashort X-ray flashes—27 000 times** per second and with a brilliance that is a billion times higher than that of the best conventional X-ray radiation sources

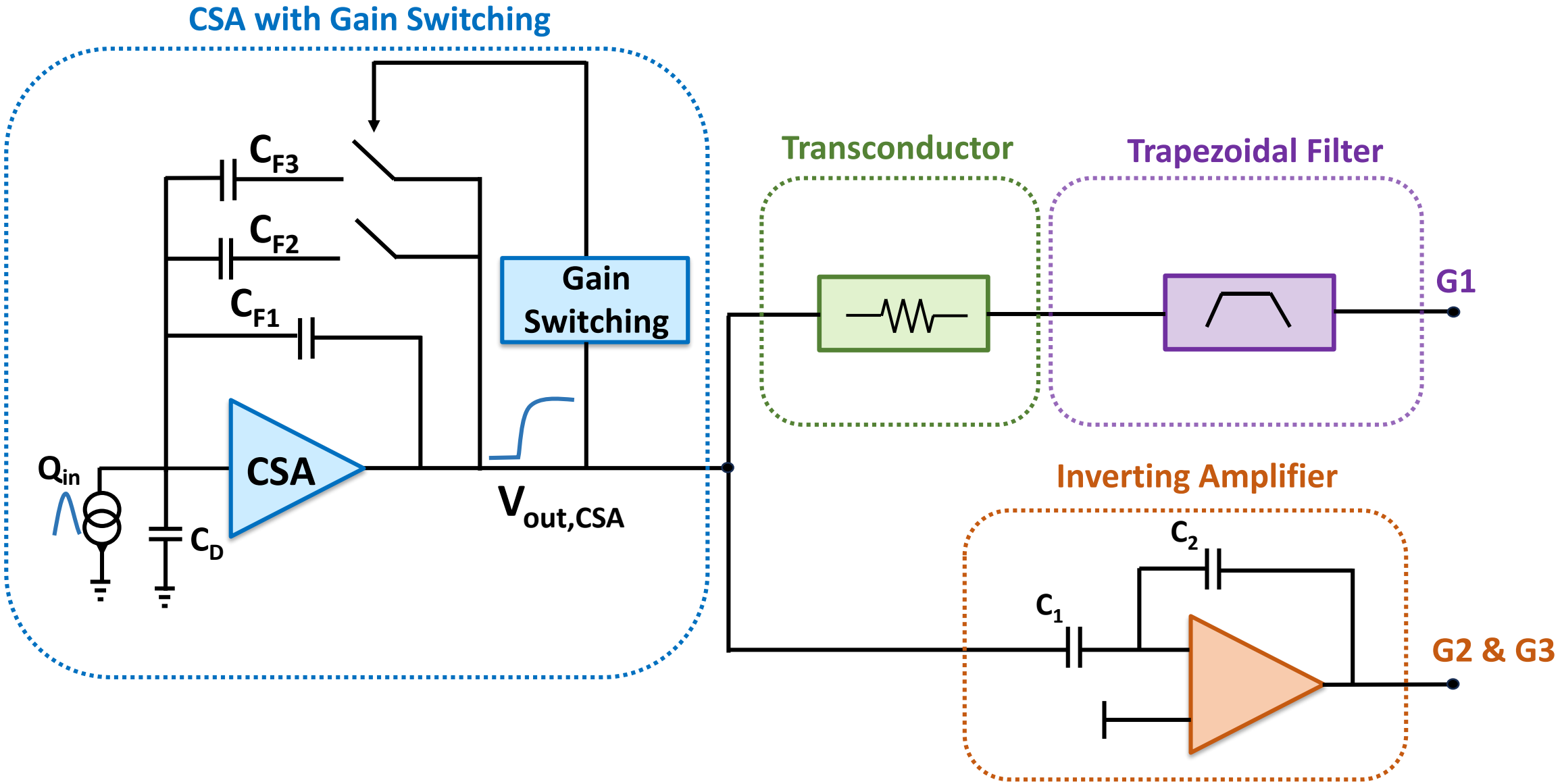


Requirements:

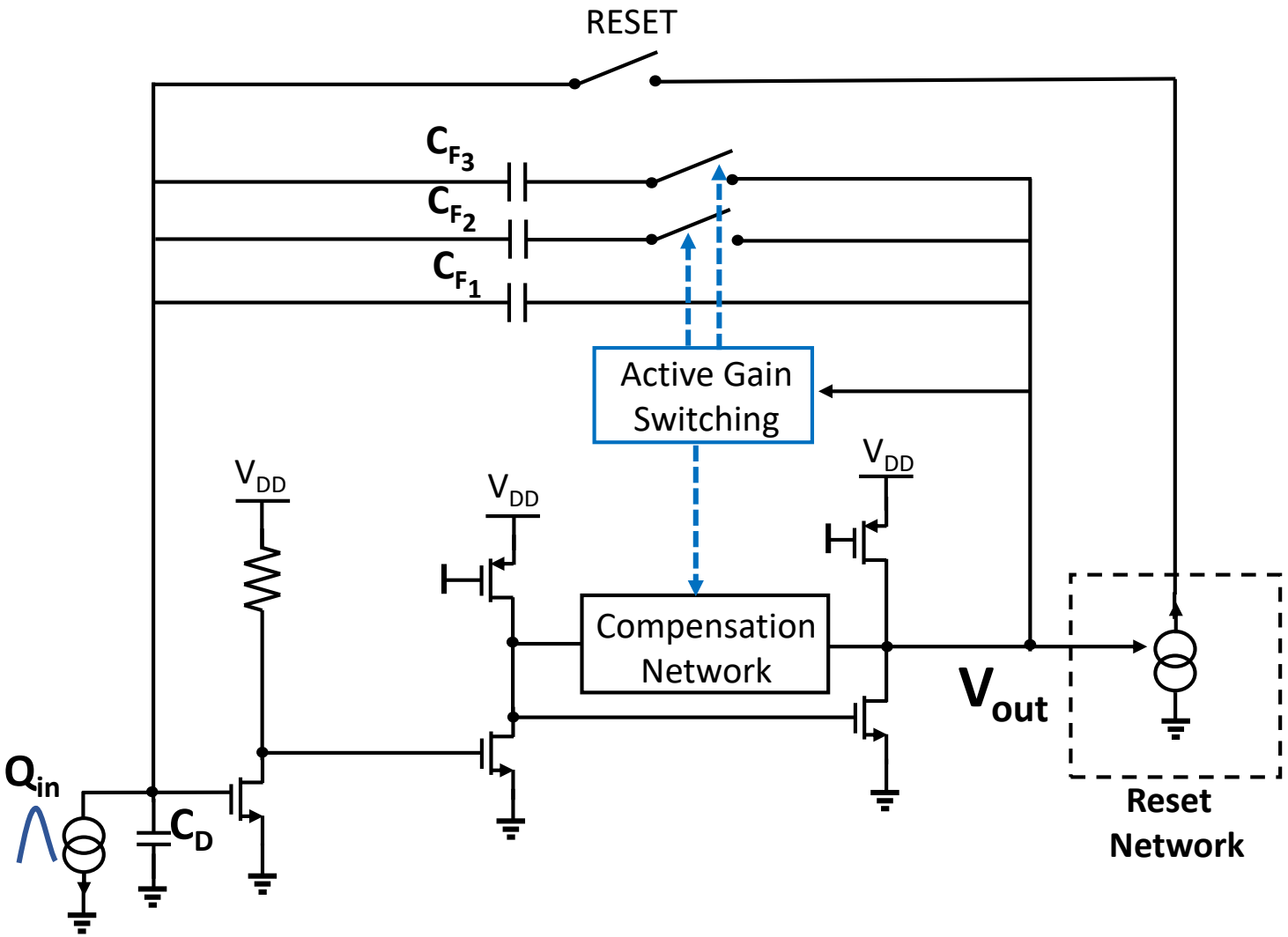
- **Single photon** resolution @ 1keV
- Dynamic range: **1–10⁴** ph/px @ 1keV
- Pixel size: **100** µm pitch
- Compatible with higher energy range (up to 20 keV)
- Readout speed 1MHz



Readout Electronics: Front-end architecture

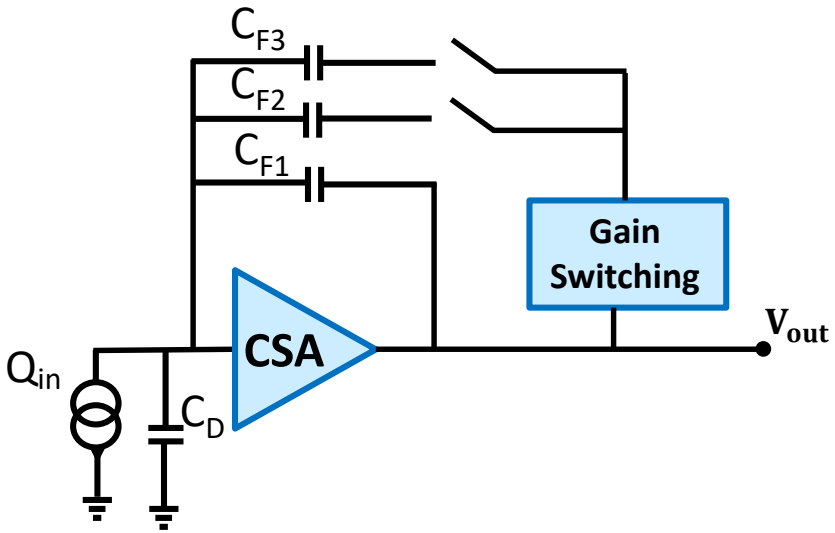


Charge Sensitive Amplifier



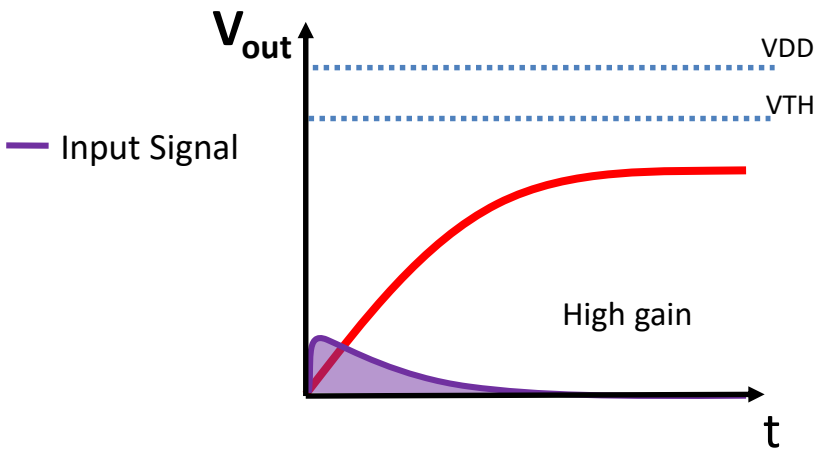
- Three-stage amplifier
- Dynamic **input range**:
  - Range 1: **1**-55 ph @ 1keV
  - Range 2: 55-800 ph @ 1keV
  - Range 3: 800-$\mathbf{10^4}$ ph @ 1keV
- Selectable **feedback** capacitance: 1,5 fF to 355 fF
- Adaptive compensation capacitance
- The **reset network** operates as a controlled current source
- Large **output dynamic** voltage : 0,95 V to 2,3 V
- CSA current consumption of 200 µA

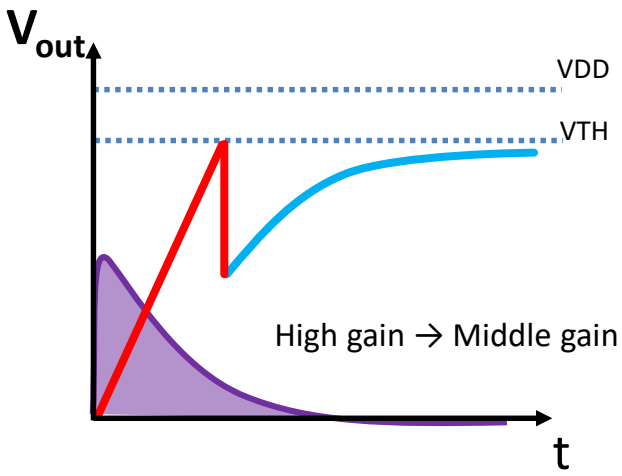
Gain-Switching: Standard Approach

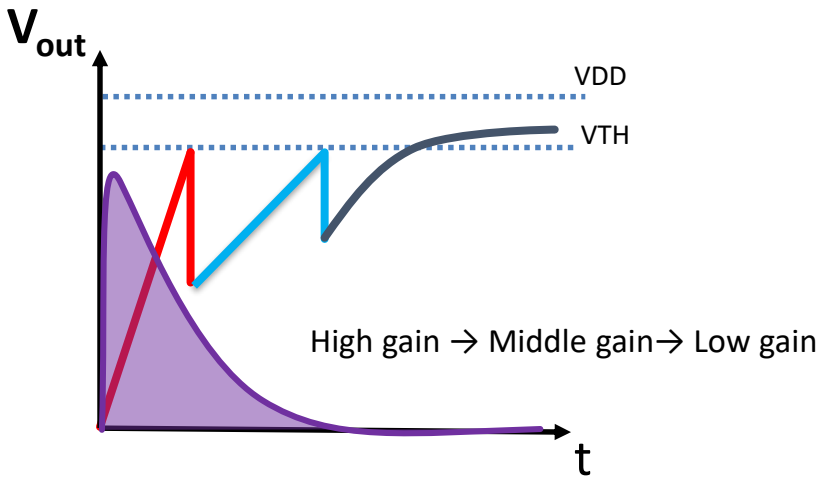


Features:

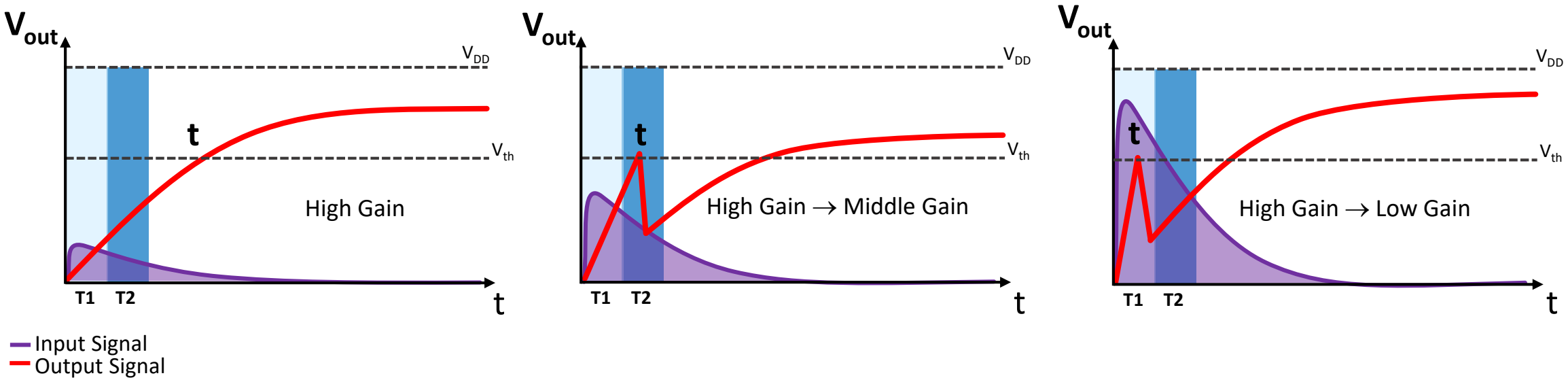
- The CSA output is compared with a threshold voltage and depending on the input charge, the gain is dynamically adjusted using a logic chain
- The threshold value is set close to the power supply







Gain-Switching: Predictive Approach

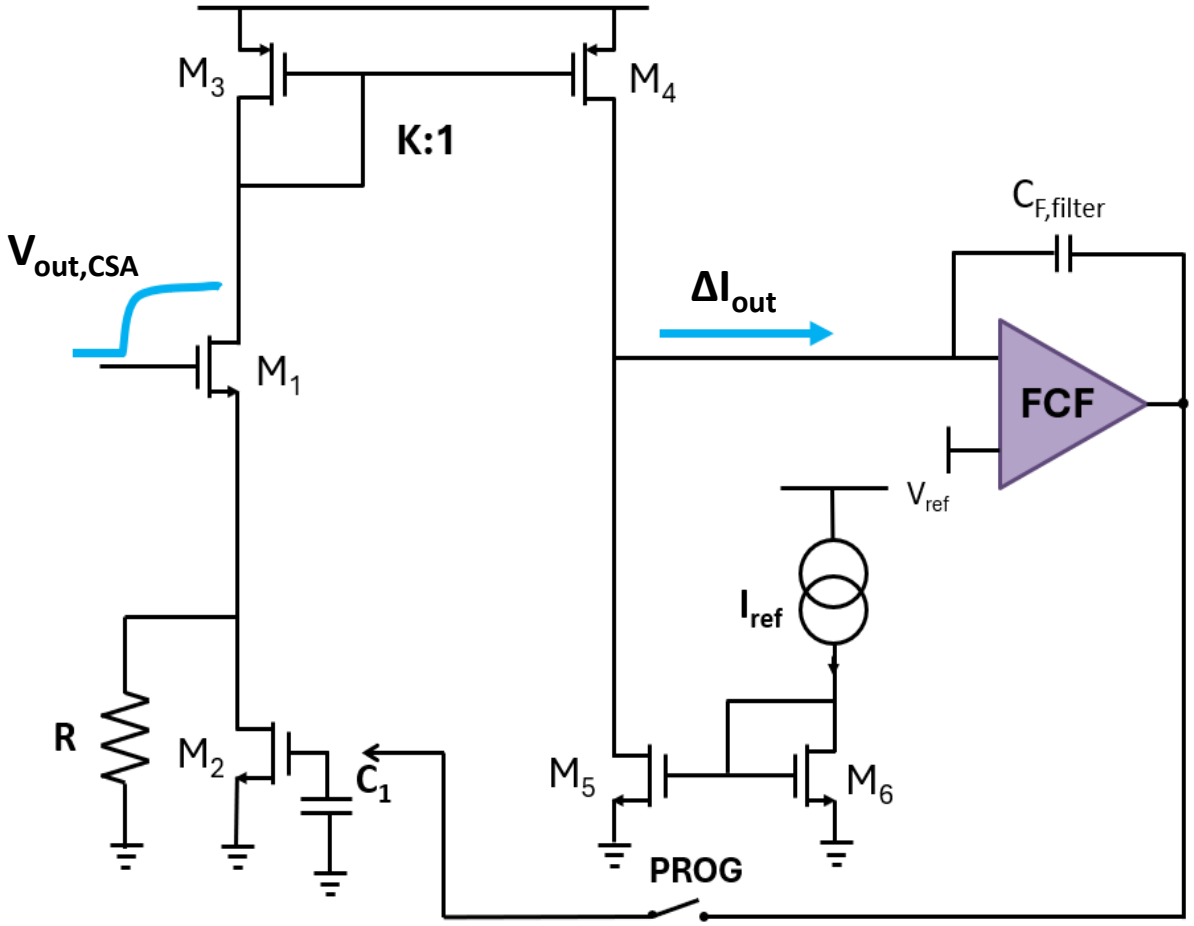


Features:

- Only one gain transition among multiple gains
- The threshold value can be arbitrarily chosen, not necessarily close to the supply value
- Gain-switch decision taken quite early with respect to the integration time
- The time windows are programmable using a 3-bit current DAC

Ref: Buonanno, et al. Gamma: A 16-channel spectroscopic asic for sipms readout with 84-db dynamic range. IEEE Trans actions on Nuclear Science, 68(10):2559–2572, 2021.

Transconductor



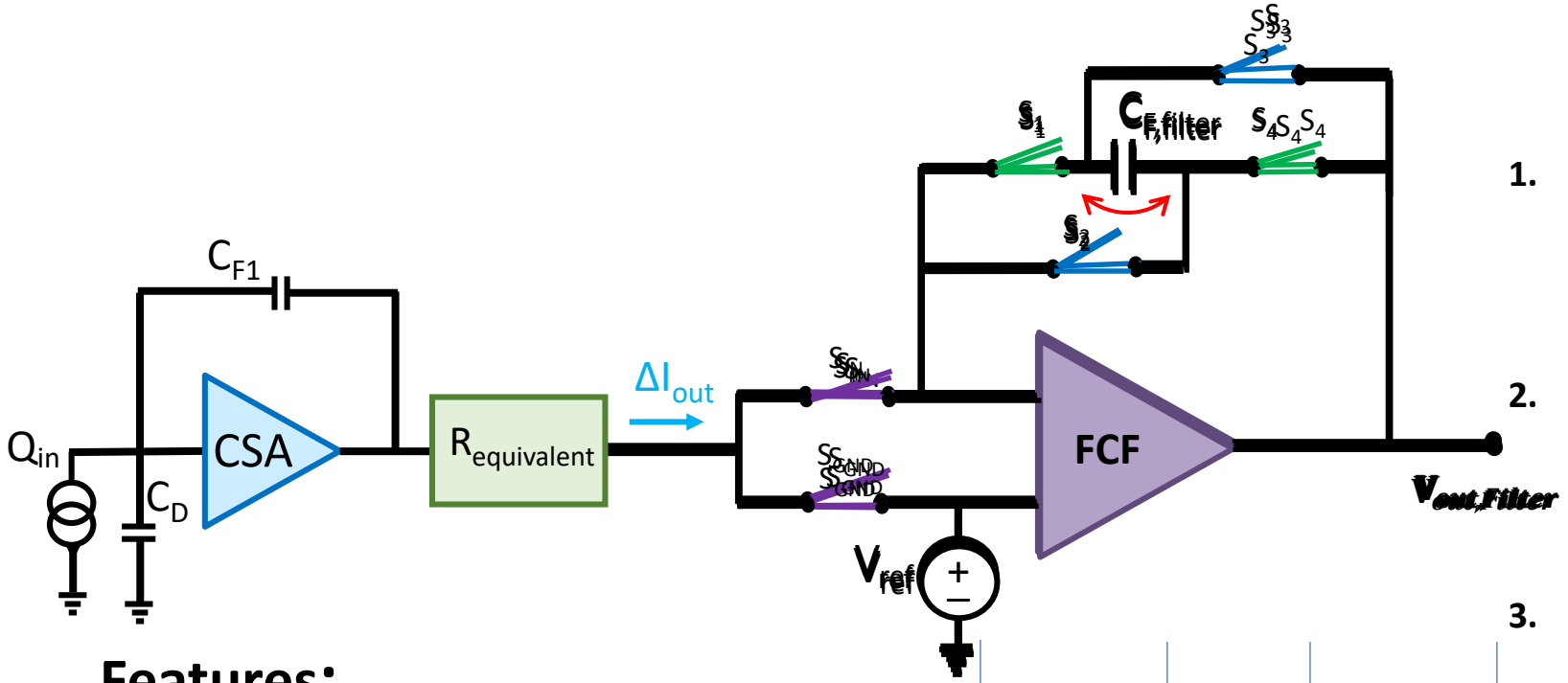
GOAL:

- Convert **linearly** the voltage step at the output of the CSA into a current, which will be integrated in the Flip-Capacitor Filter

FEATURES:

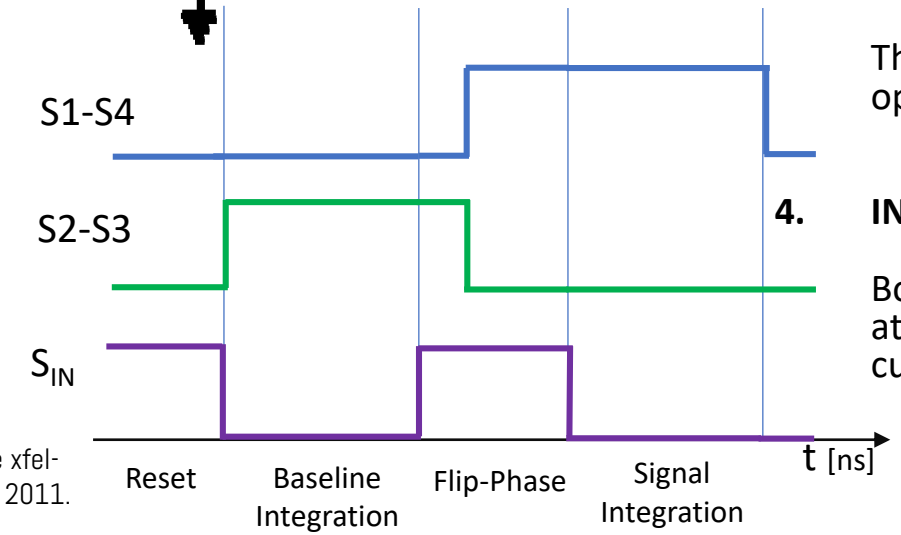
- Total equivalent resistance of K·R=310 kΩ
- **Wide input range** : 0,95 V to 2,3 V
- The **offset compensation** of the output current has been done implementing a control loop with the filter (programming phase)

Flip-Capacitor Filter



Features:

- **Trapezoidal** weighting function
- Selectable **integration time** :
  50ns, 100ns, 150ns



1. **RESET PHASE**

   All the feedback switches are closed, the current flows in the current generator

2. **INTEGRATION**

   The switch S_{IN}, S_1, S_4 are closed and the baseline current will be integrated

3. **FLIP PHASE**

   The capacitance is flipped closing $S_2 - S_3$ and opening $S_1 - S_4$ and the pulse arrives

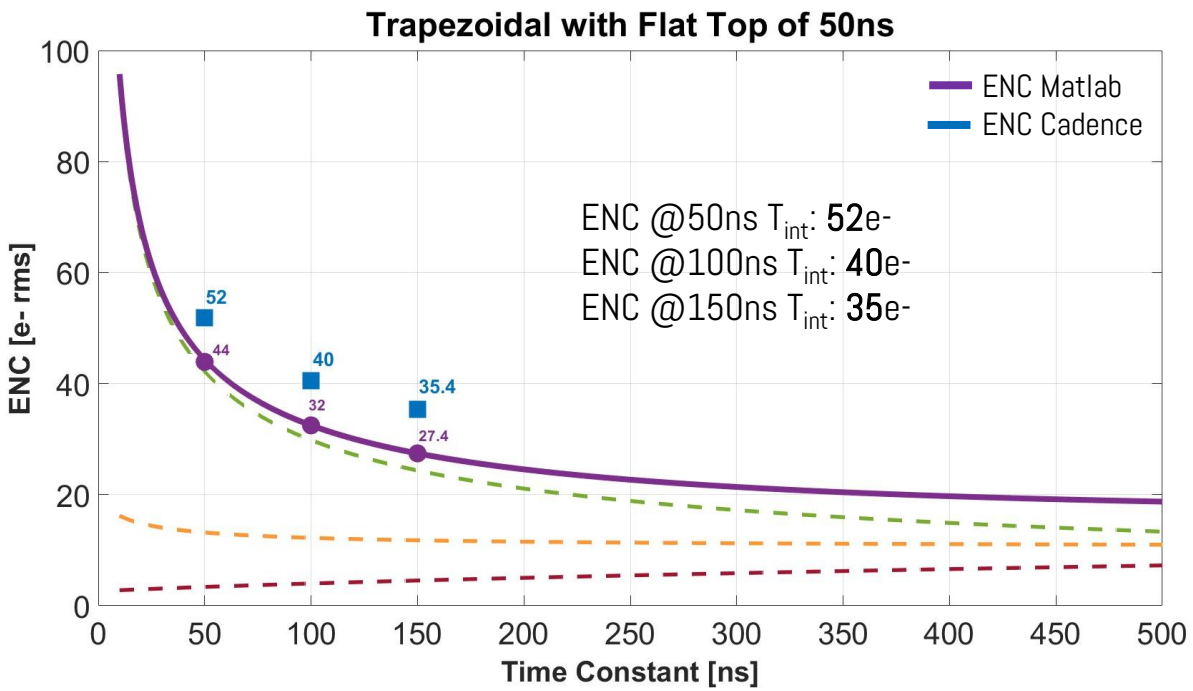
4. **INTEGRATION**

   Both signal and baseline will be integrated, so, at the end of this phase, only the signal current contribution remains.

Ref: Facchinetti, et al. Characterization of the flip capacitor filter for the xfel-dssc project. IEEE Transactions on Nuclear Science, 58(4):2032–2038, 2011.

Noise Simulations

RANGE 1



$$ENC^2 = C_T^2 \cdot a \cdot \frac{1}{\tau} \cdot A_1 + C_T^2 \cdot c \cdot A_2 + b \cdot \tau \cdot A_3$$

τ: shaping time

A_1, A_2, A_3: filter coefficients

a, b, c : are respectively the series white noise, the parallel noise and the flicker noise

C_T: Includes the detector capacitance, the feedback capacitance and the gate capacitance of the input transistor: 0,34pF

RANGE 2

$$ENC = Q * \frac{\sigma_{n,out}}{V_{out,peak}} = 0{,}5 \text{ ph @1keV}$$

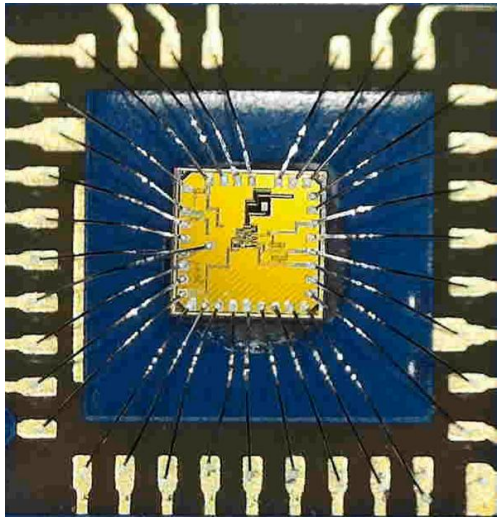
This value has been simulated without the filter

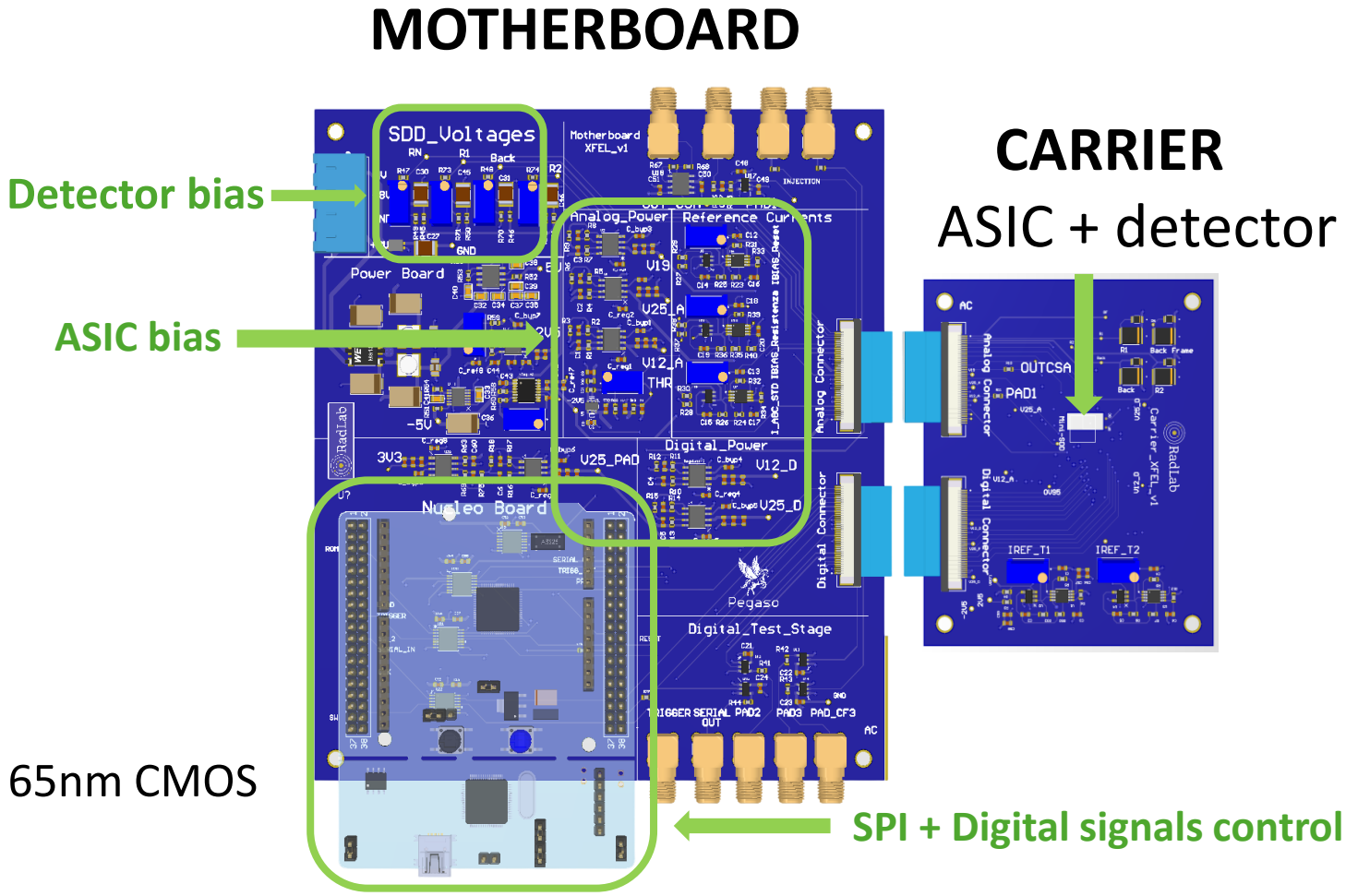
RANGE 3

$$ENC = Q * \frac{\sigma_{n,out}}{V_{out,peak}} = 3{,}7 \text{ ph @1keV}$$

This value has been simulated without the filter

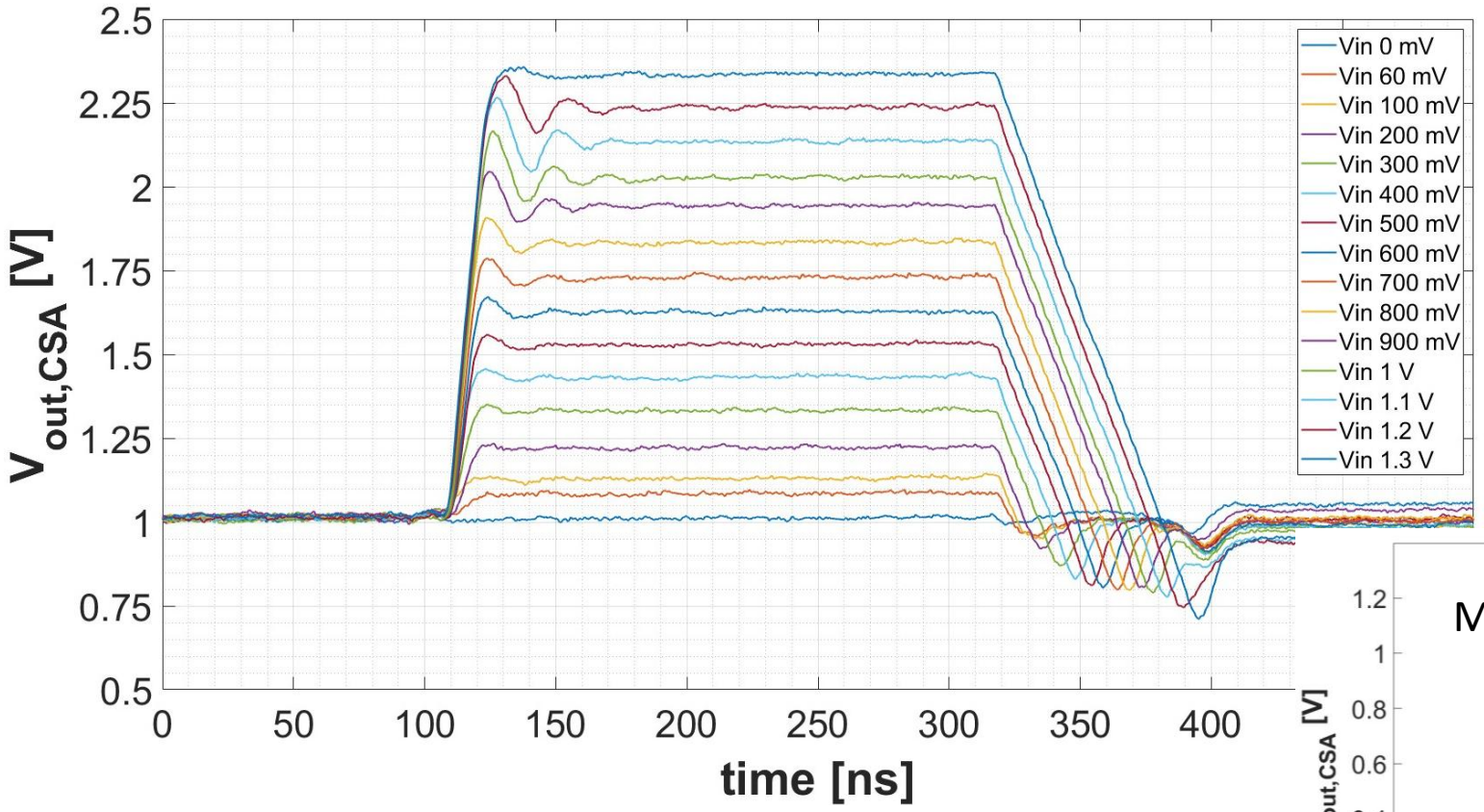
First prototype & Experimental Validation



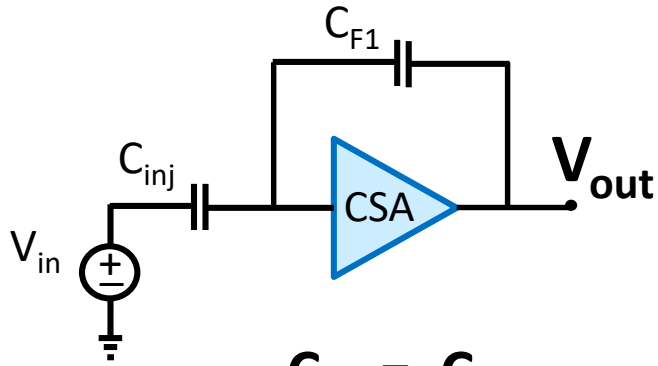


- The first prototype was designed in 65nm CMOS technology
- The FE power consumption is around 800 µW
- PCB assembly for ASIC tests

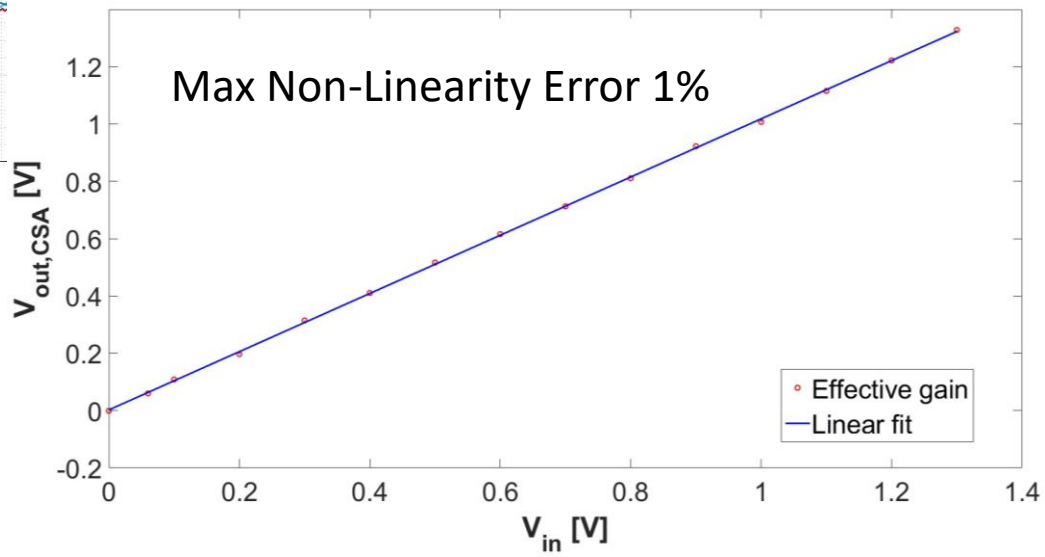
Transient Signal Measurements: CSA Output



RANGE 1 (high gain)



$C_{inj} = C_F$



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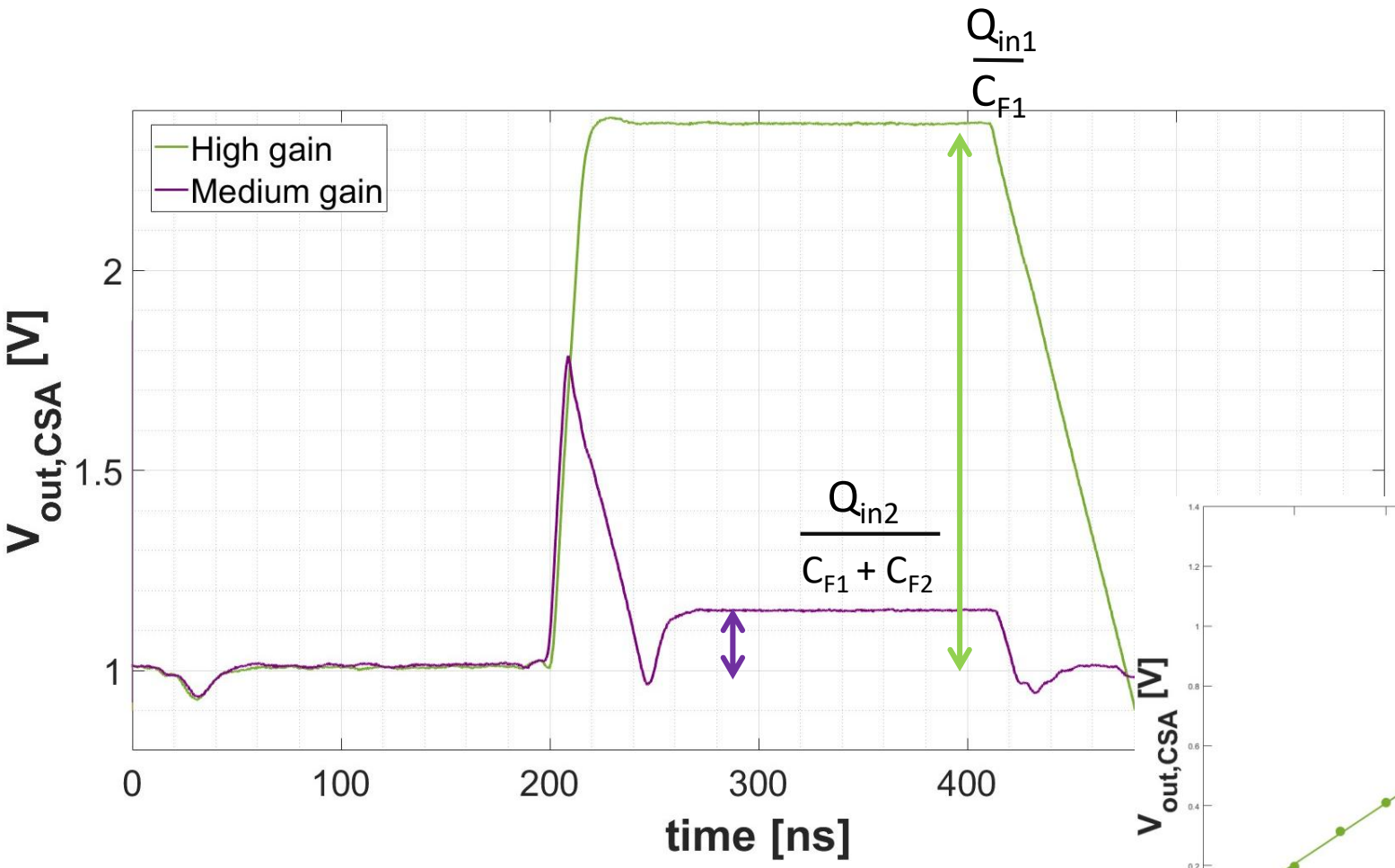
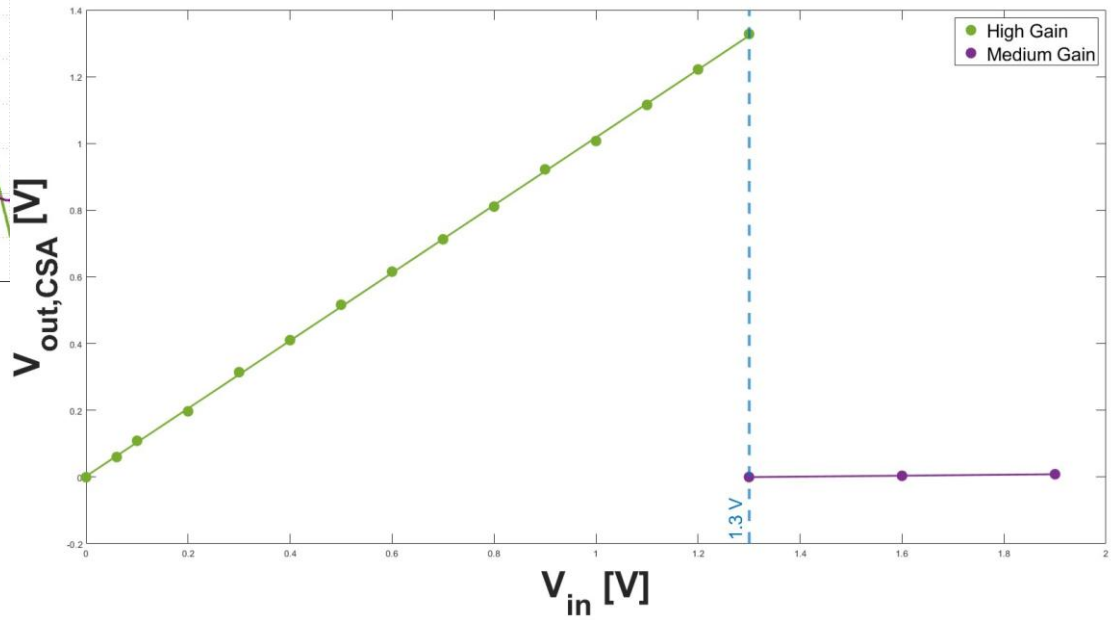
Predictive Gain Switching



Gain switching

- High gain $= \frac{C_{inj}}{C_{F1}} = 1$
- Medium gain $= \frac{C_{inj}}{C_{F1} + C_{F2}} = 0.11$



$Q_{in2} \gtrsim Q_{in1}$ to switch the gain

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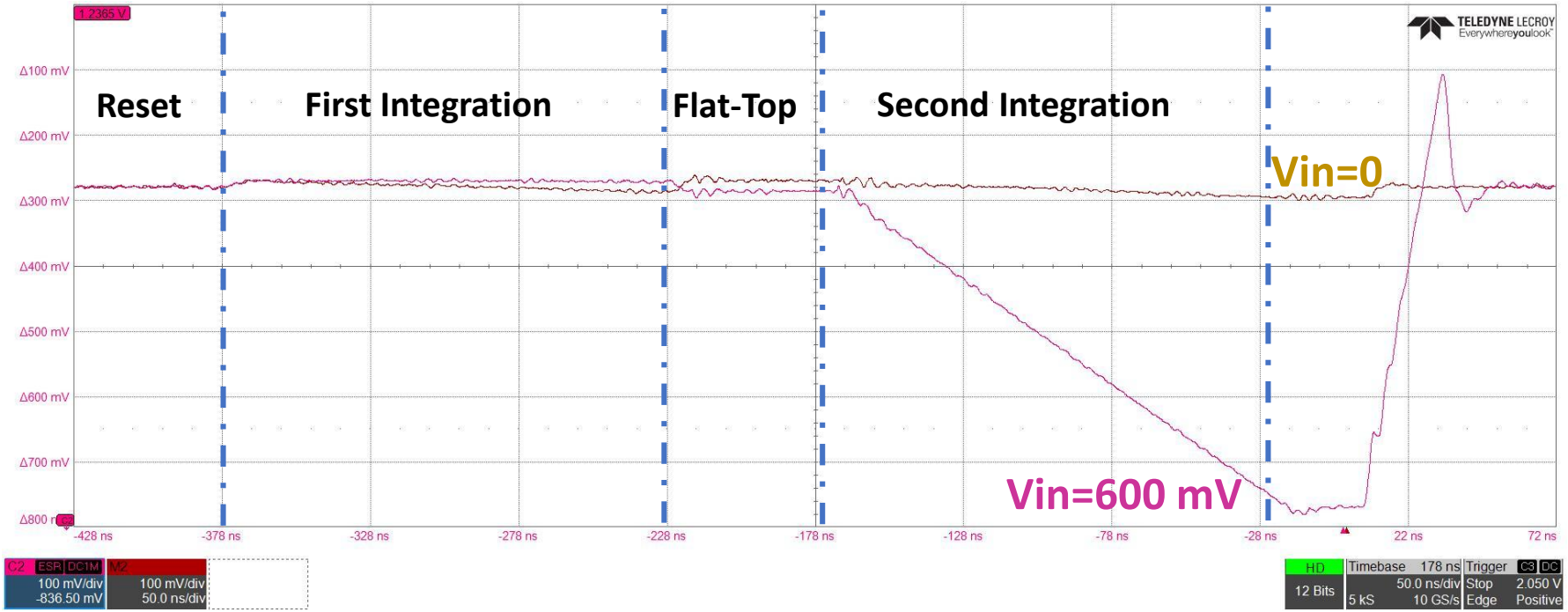
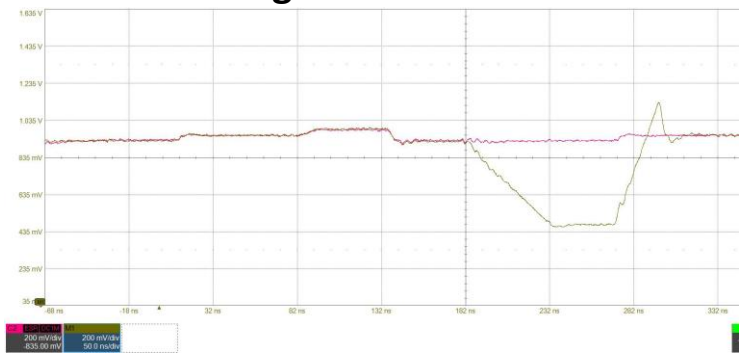
Transient Signal Measurements : Filter Output

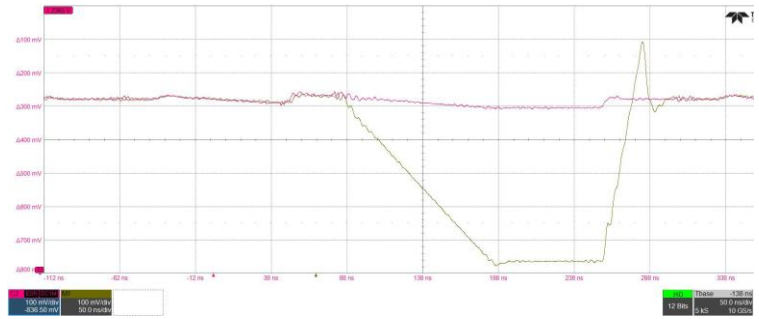
Integration time 150 ns



Integration time 50 ns



Integration time 100 ns



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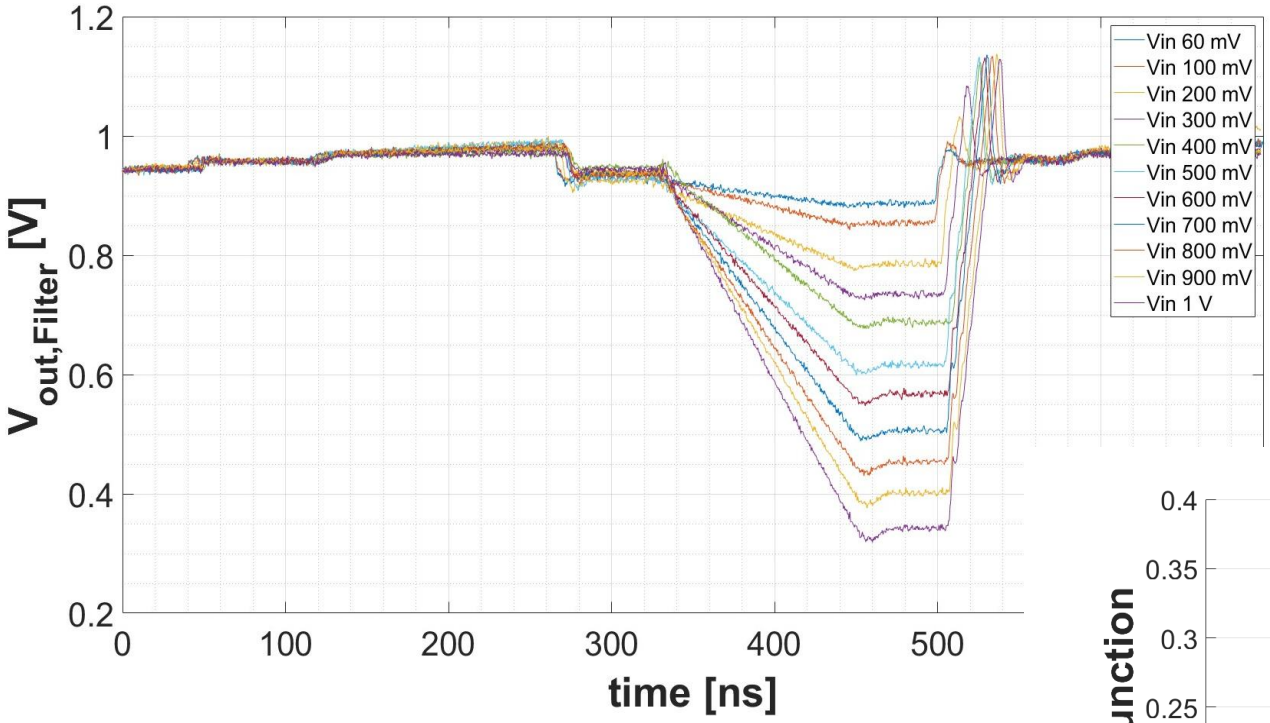
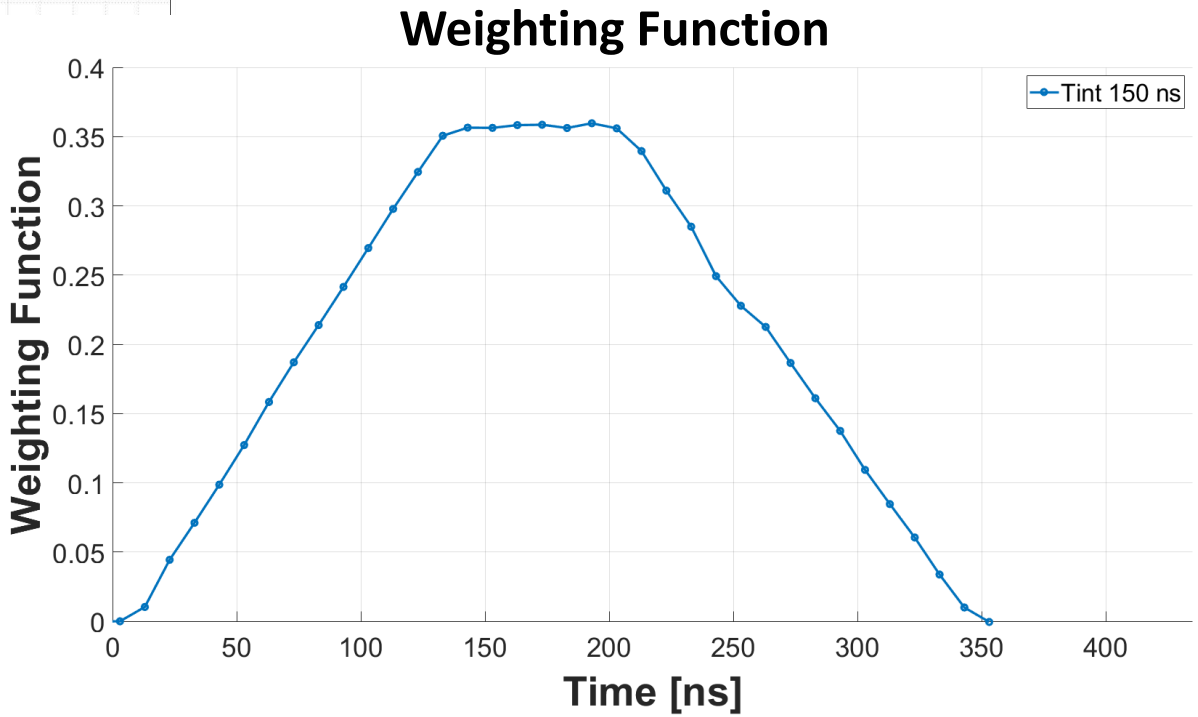
Transient Signal Measurements : Filter Output



- Integration time = 150 ns
- Flat-Top = 50 ns
- Max Non-Linearity Error 1.5%



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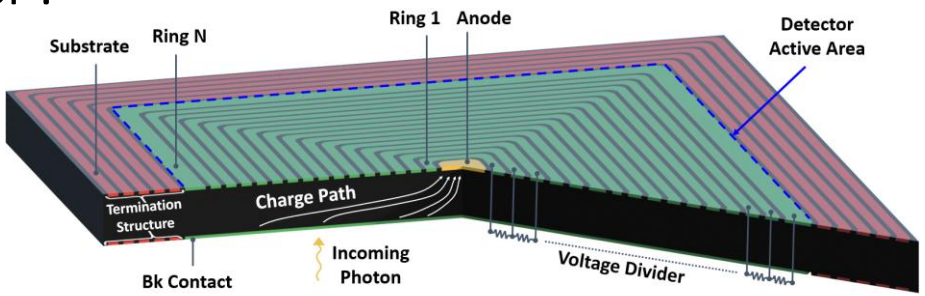
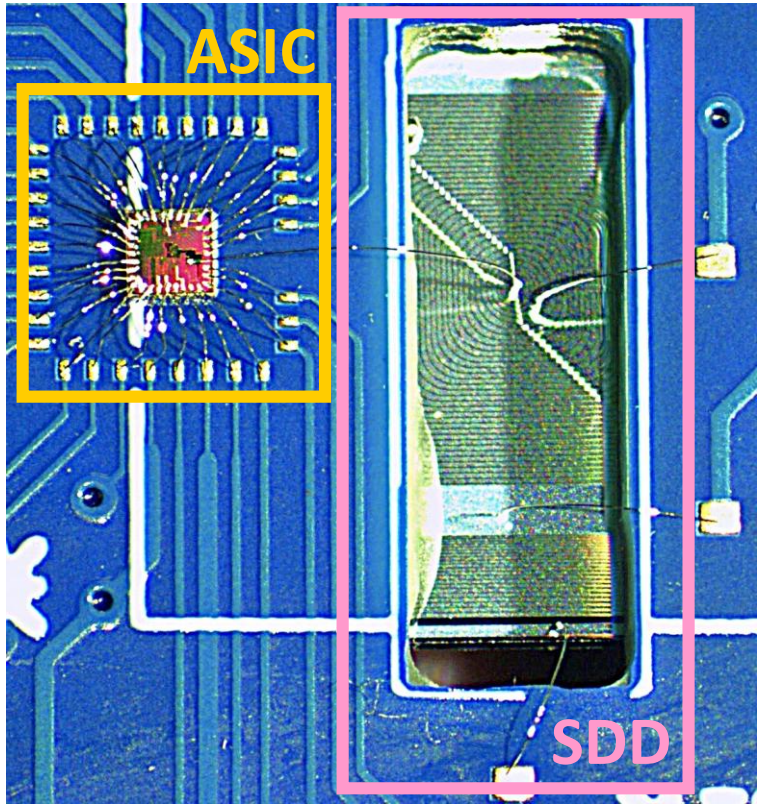
Preliminary Measurements with a Detector

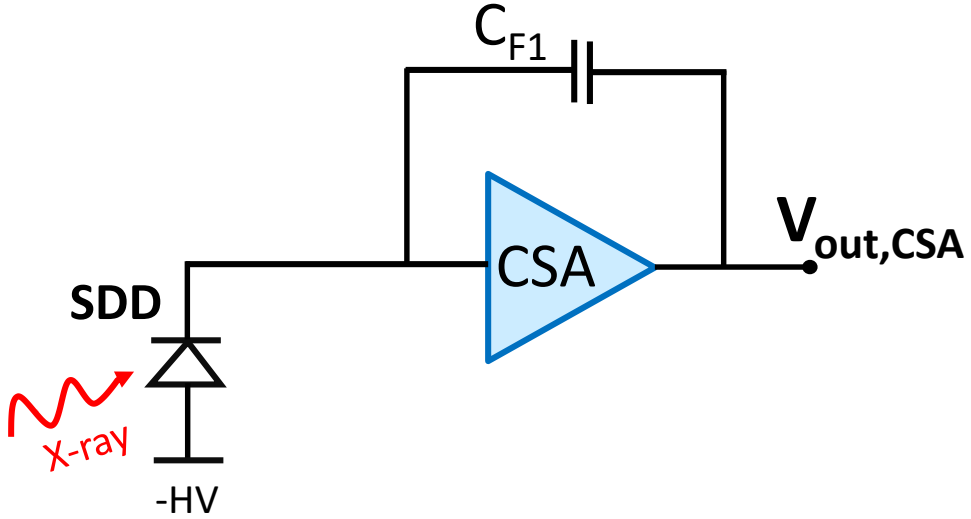
Silicon **D**rift **D**etector :

(FBK, Trento, Italy)

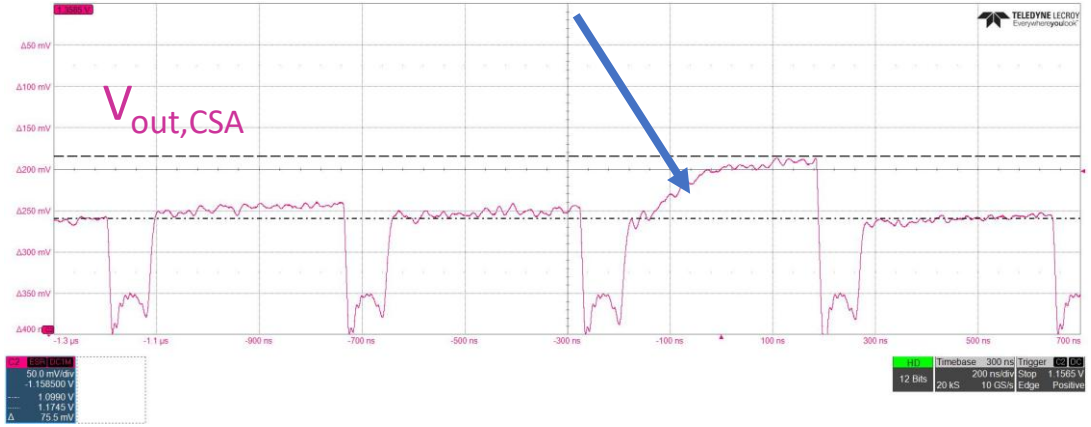




Active area: 5 mm^2



Measurement by irradiating with a **^{55}Fe source**

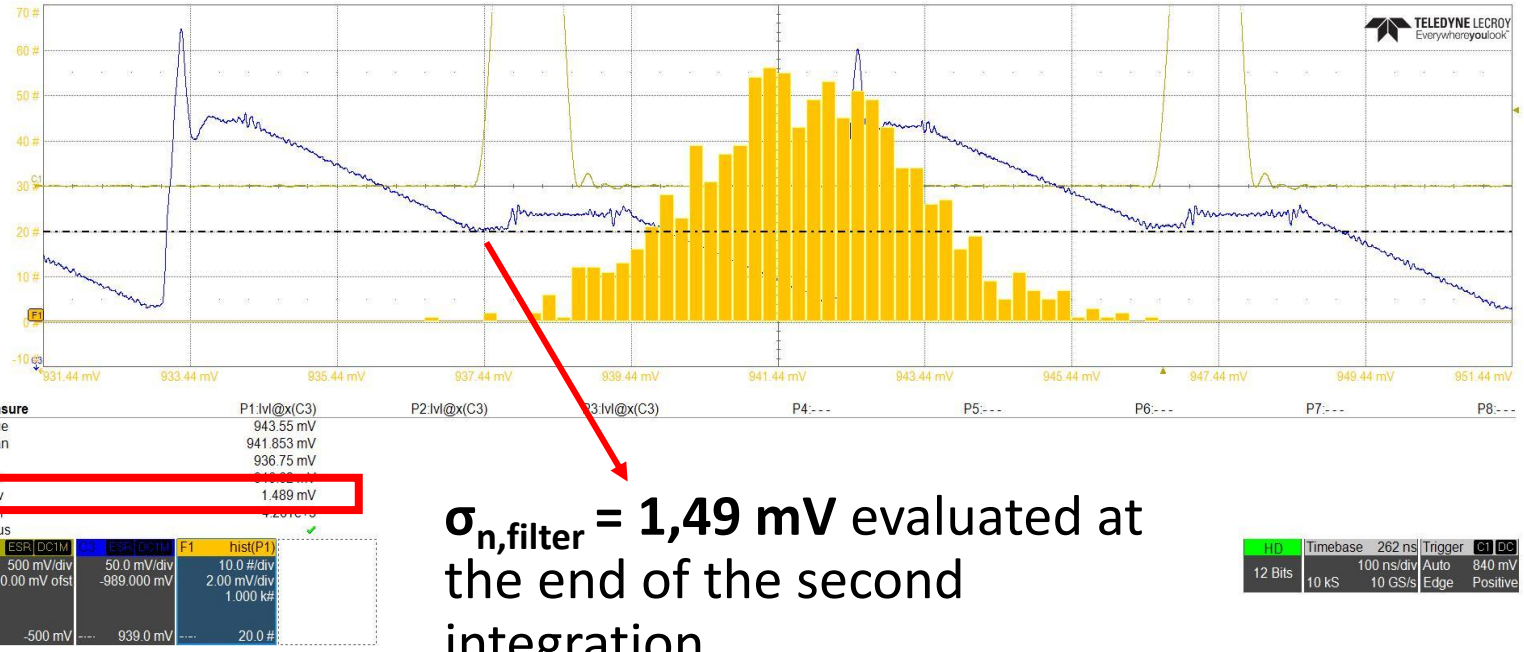


Rise time in the order of 100 ns due to the charge diffusion time in the SDD

Actual Gain: 47 µV/e$^-$

Preliminary Noise Evaluation

Noise evaluation at **room** temperature with the SDD connected



$\sigma_{n,filter}$ = **1,49 mV** evaluated at the end of the second integration

- Integration time: 150 ns
- Flat-Top: 50 ns
- Detector Area: 5 mm^2

Considering the calibration with the ^{55}Fe source

ENC = 44 e-

ENC values		
Tintegration	Measurements	Simulations
50 ns	60 e$^-$	52 e$^-$
100 ns	48 e$^-$	40 e$^-$
150 ns	44 e$^-$	35 e$^-$

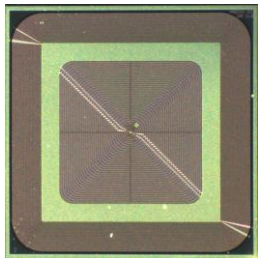
Test Setup with a focused laser

Pulsed Laser
with a spatial resolution of 5 um

Filter lens

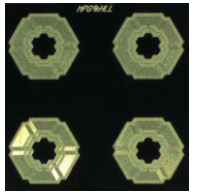
Motherboard

SDD
(FBK, Trento, Italy)

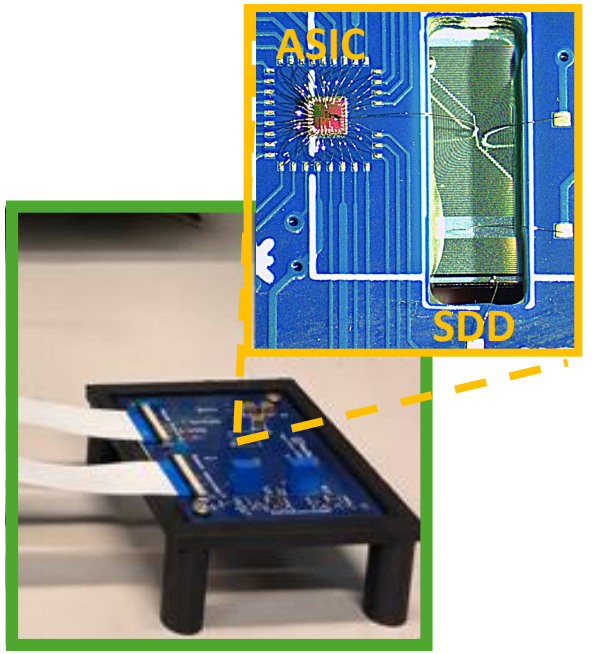


Active area 5 mm^2

Mini-SDD
(MPI-HLL , Germany)



Exagonal pitch 200 um



Carrier

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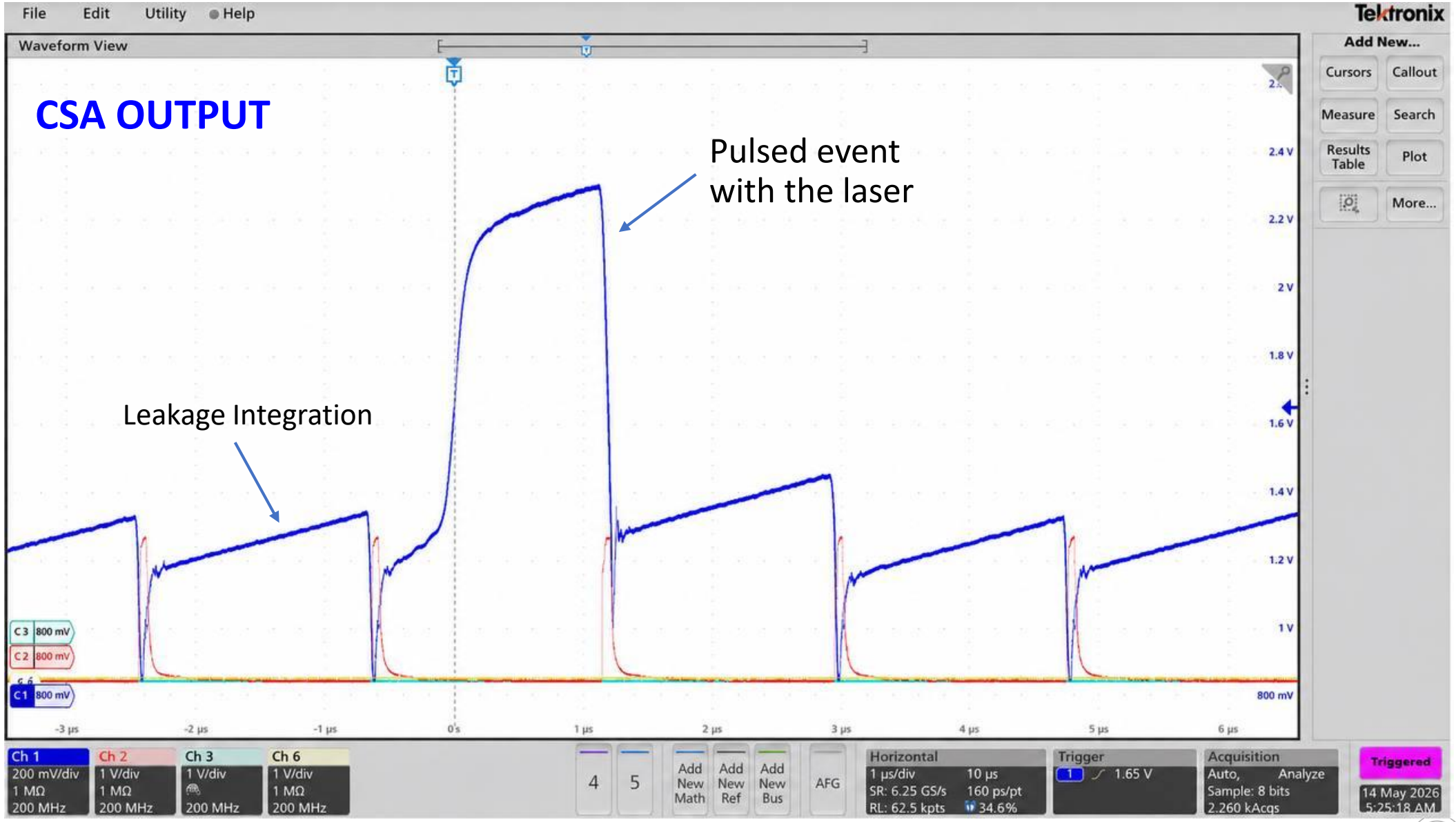
First Gain Operation



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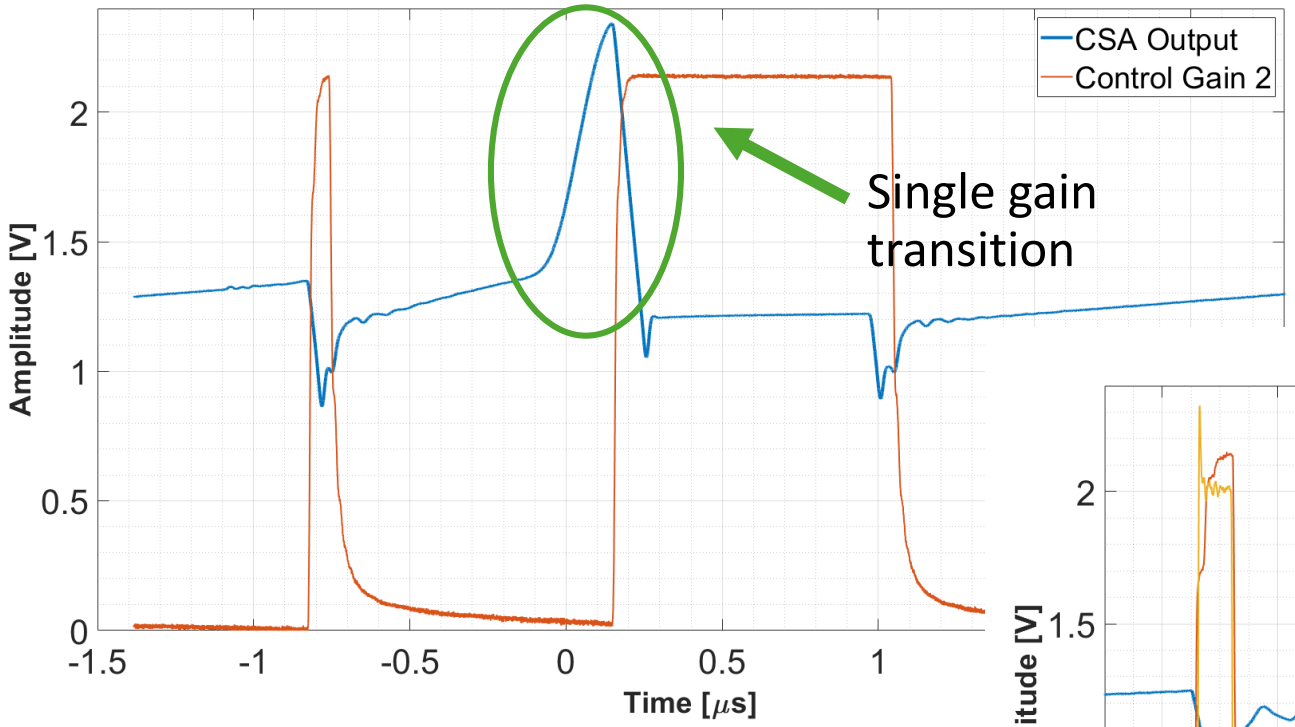
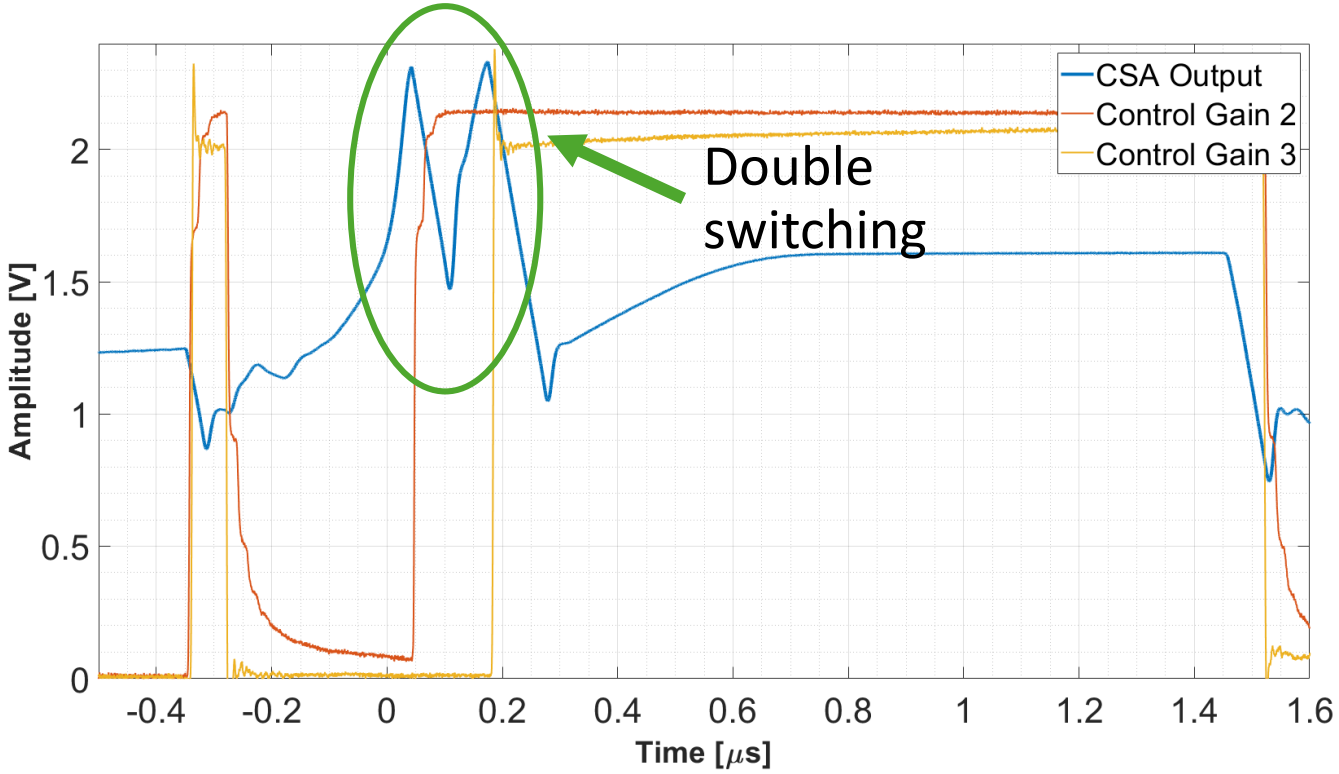
Standard Gain Switching





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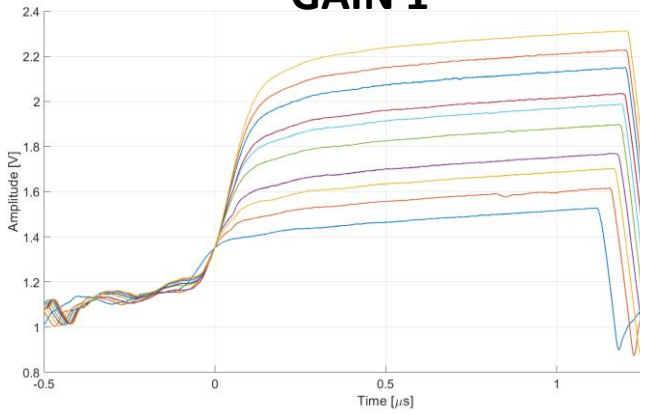
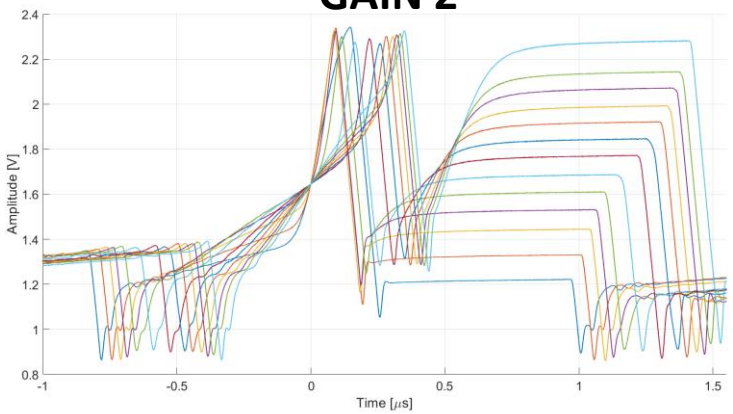
Gain Characterization

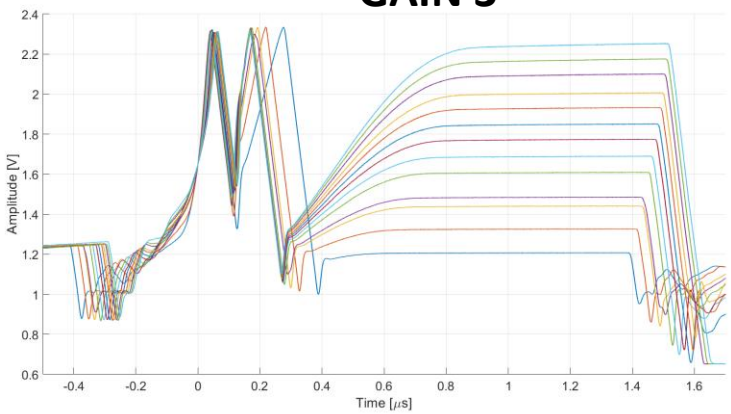
GAIN 1

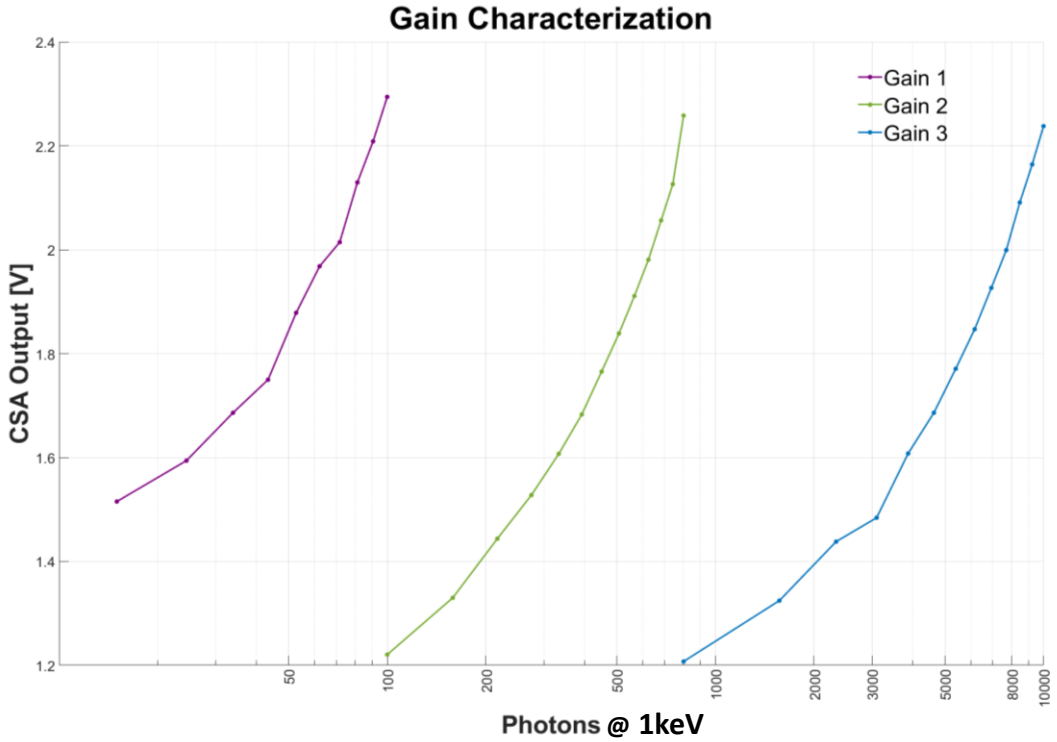


GAIN 2



GAIN 3



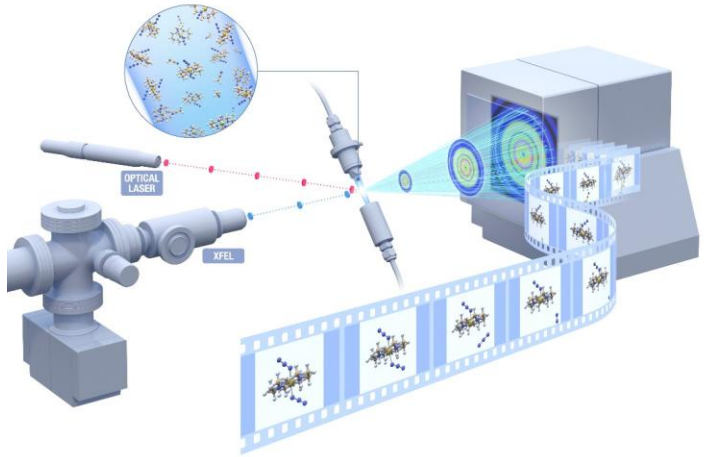


Conclusions

- A new front-end for future Eu-XFEL detectors has been developed
- Predictive AGC allows for single photon resolution and high dynamic range
- First experimental measurements show correct functioning
- Noise measurements with detectors prototype and gain characterization with predictive switching on going

Future step:

- A new version compatible with hard X-rays will be realized with a more scaled technology that will be proposed for the XSTREAM Pathfinder



Thank you for your kind attention !!

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