中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

Developments of Pixel Detector Readout ASICs for Photon Science at IHEP

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Institute of High Energy Physics, Chinese Academy of Sciences
FEE 2026, 18 May
XIII FRONT-END ELECTRONICS WORKSHOP, PARIS, France
On behalf of the detector group, IHEP

Advanced Light-Sources in China

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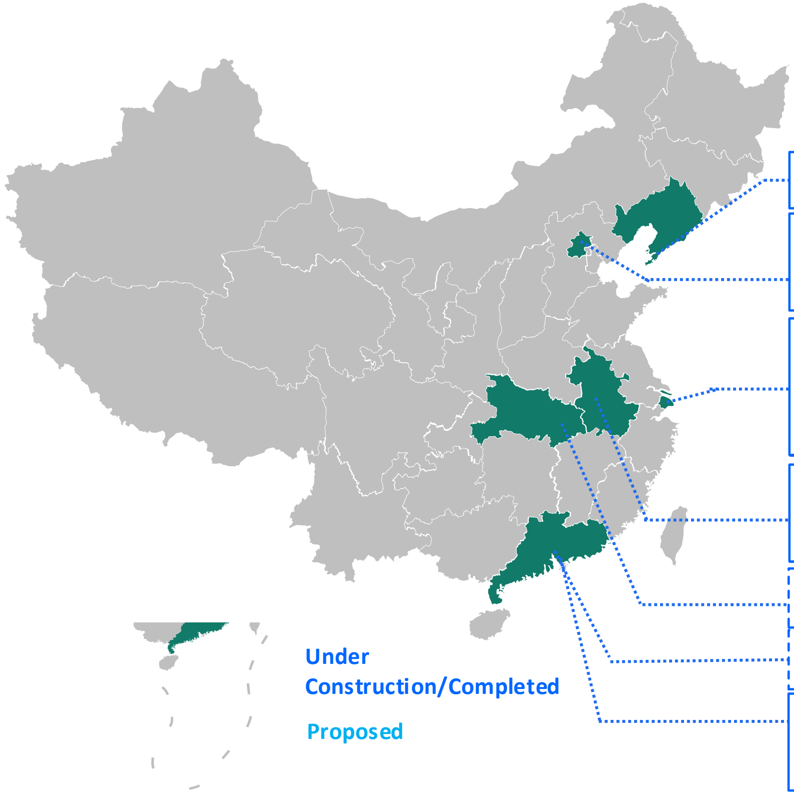

- Dalian Coherent Light Source
- Beijing Synchrotron Radiation Facility (BSRF)
  High Energy Photon Source (HEPS)☆
- Shanghai Synchrotron Radiation Facility (SSRF)
  Shanghai soft X-ray Free-Electron Laser facility
  Shanghai HIgh repetitioN rate XFEL and Extreme light facility (SHINE)☆
- National Synchrotron Radiation Laboratory
  Hefei Advanced Light Facility (HALF)☆
- Wuhan Light Source☆
- Southern Advanced Light Source☆
- Shenzhen Superconducting Soft-X-ray Free Electron Laser (S^3FEL)☆

Light Source Facilities in China (4^{th} Gen with Star)

HEPS: 2025

SHINE: 2027

HALF: 2028

Outline

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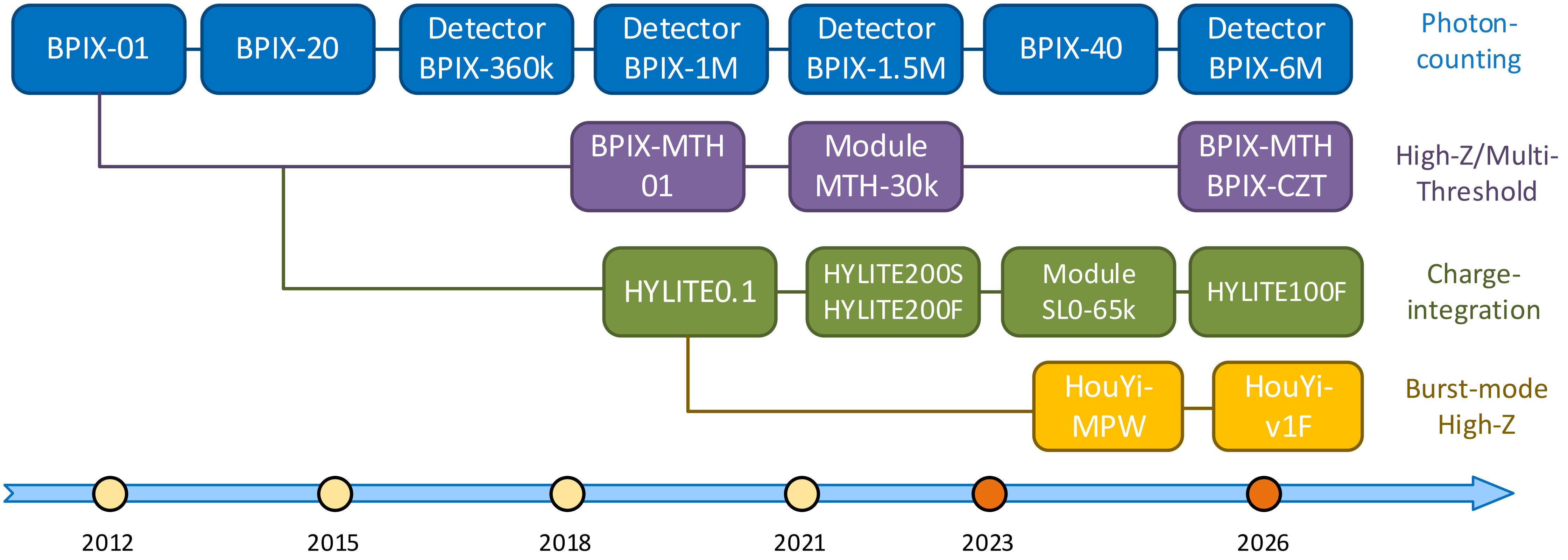

Outline

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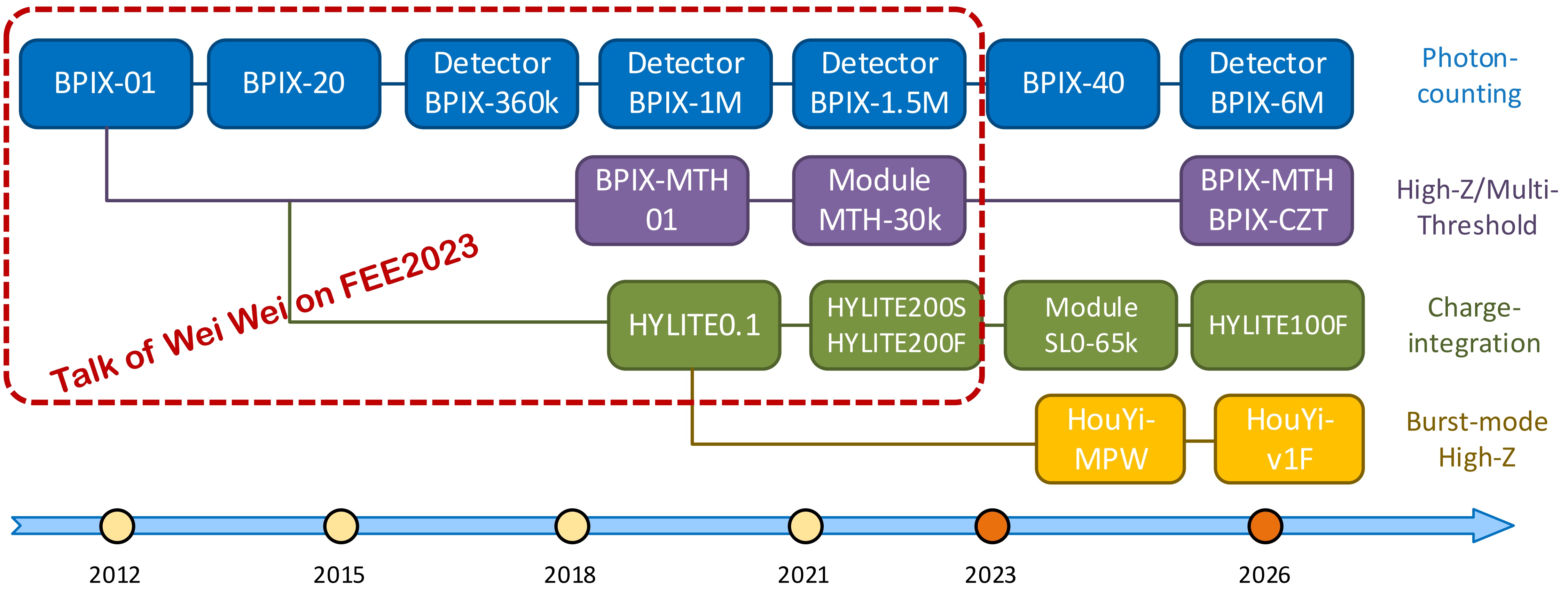

Outline

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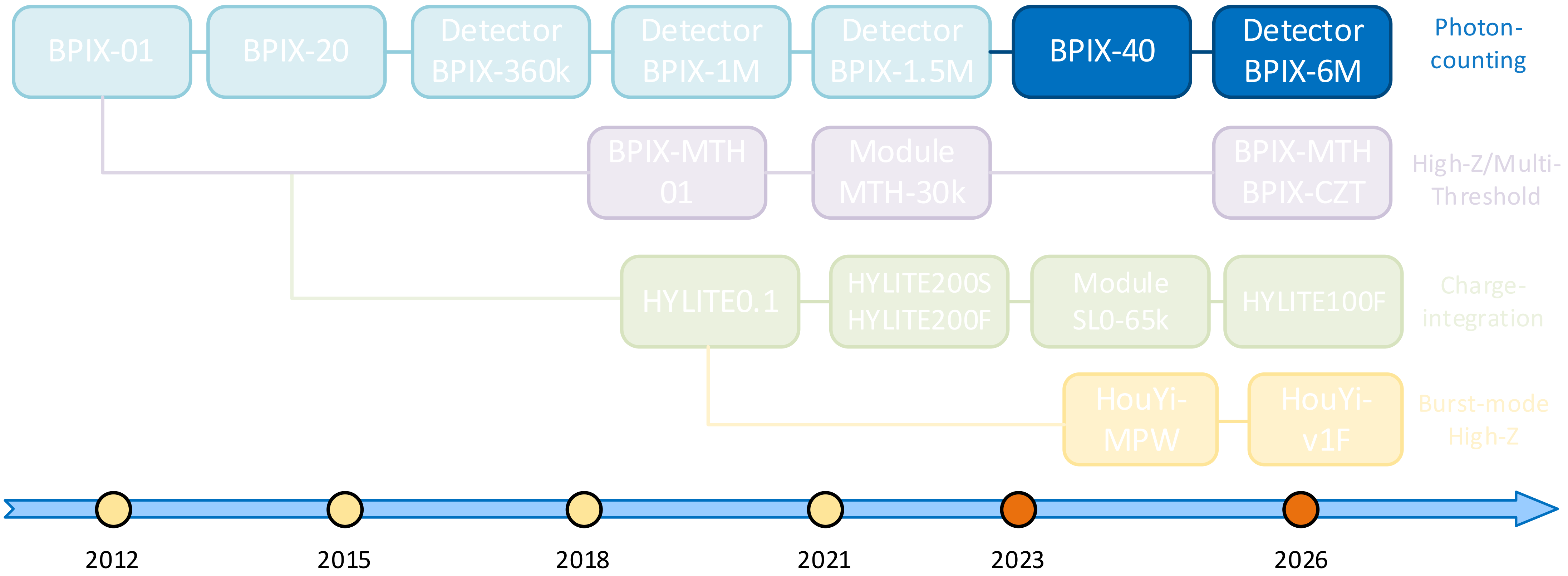

Photon-Counting: BPIX

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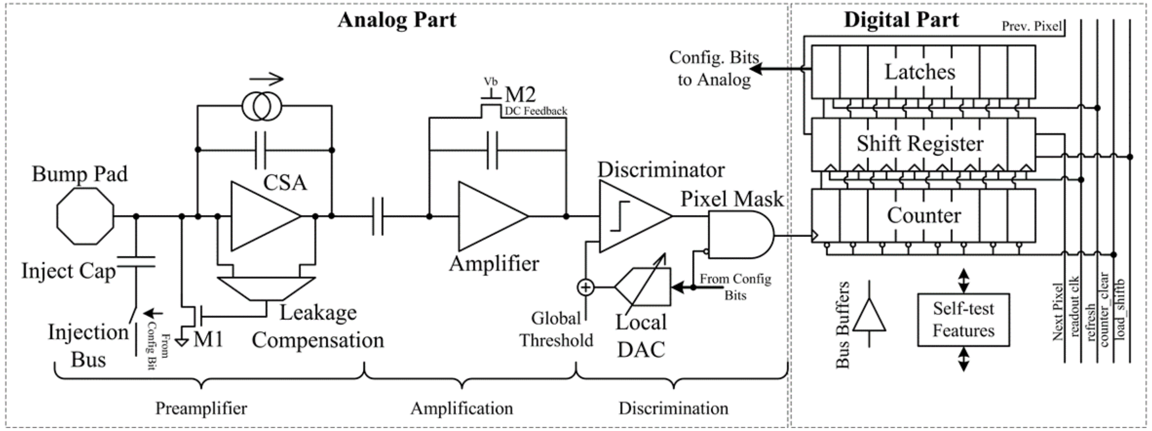
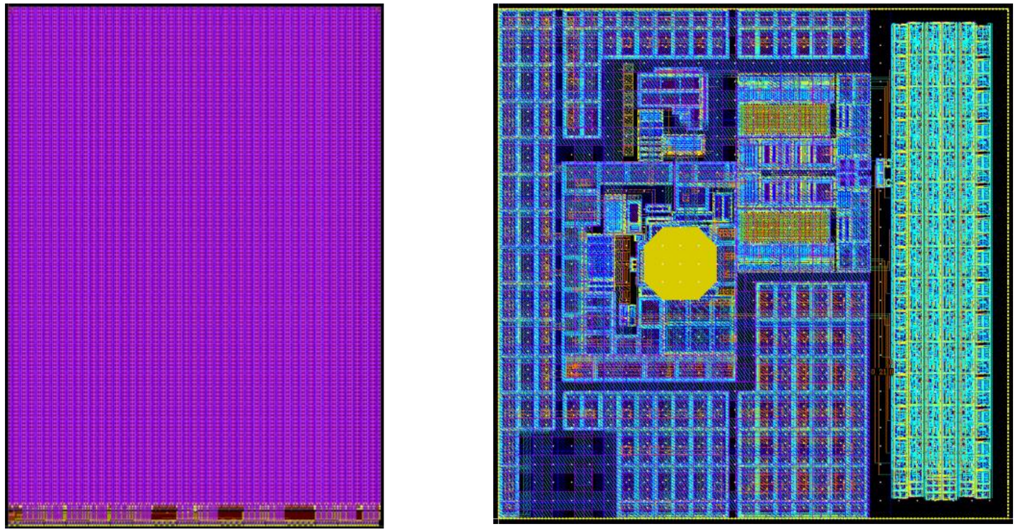
- A photon-counting pixel detector for synchrotron radiation end stations (HEPS).
- New BPIX-40: A 6M system assembled for the HEPS beamline BA.
- A series of detectors in different dimensions (2M/1M …) are also scheduled

Specs	BPIX-20	BPIX-40
Pixel size	150 µm × 150 µm	140 µm × 140 µm
Pixel Array	104×72	128×96
Threshold	1	2
Gain	Fixed	2 bits tunable
Counting rate	> 2 Mcps	> 2 Mcps @ Med gain
Frame rate	1.2 kHz	2 kHz
Counting Depth	20 bit	14 bit
Detector Module	2×4 (208×288)	2×6 (256×576)
Module Gap	3 mm by TSV	2.7mm by WB



Pixel Structure of BPIX



Chip and Pixel Layout of BPIX-40

Evolution of BPIX Detector System

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	1st BPIX (2015-2016)	2nd BPIX (2017-2018)	3rd BPIX (2019-2024)	4th BPIX (2024-2026)
Pixel size	150 μm × 150 μm	150 μm × 150 μm	150 μm × 150 μm	140 μm × 140 μm
Modules	6	16	24	40
Module Array	104×72×2×4	104×72×2×4	104×72×2×4	128×96×2×6
Pixels	360K	1M	1.4M	6M
Energy range	10~20 keV	8~20 keV	8~20 keV	6~20 keV
Bump Bonding	Indium	CuSn	CuSn	CuSn
Packaging	Wire bonding	Wire bonding	Through Silicon Via (TSV)	Wire bonding
Assembly Scheme	Rigid-flex PCB	Rigid-flex PCB	Rigid-flex PCB with low CTE	HTCC
Dead Area	26.3%	26.3%	11.8%	9.3%
Backend Readout	Spartan6 + SFP	Kintex7 + DDR3 + Molex Nano-Pitch I/O™ Cable	Kintex7 + DDR3 + Molex Nano-Pitch I/O™ Cable	UltraScale Kintex Plus + DDR4 + MicroTCA.4
DAQ interface	1G Ethernet x12	1/10 G Ethernet x4	40G Ethernet	100G Ethernet
Cooling	Air cooling	Air cooling	Water cooling + air cooling	Water cooling + air cooling
Power	100W	370W	500W	<2500W

BPIX-6M Detector System

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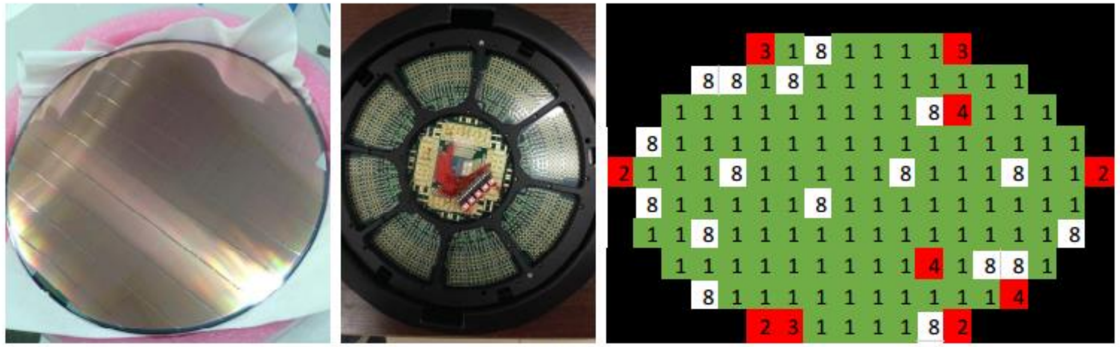
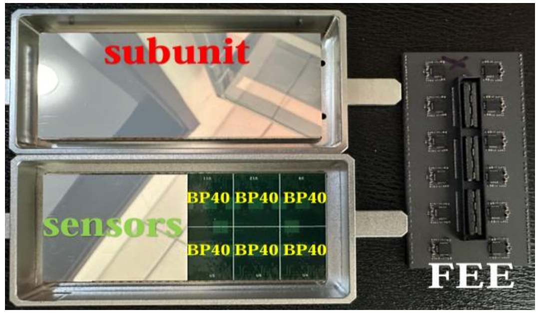
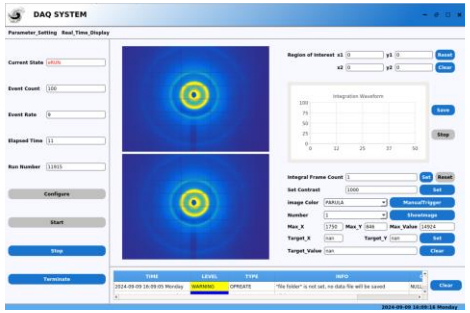


an 8-inch ASIC wafer | Probe card for ATE test | A wafer map of an 8-inch wafer

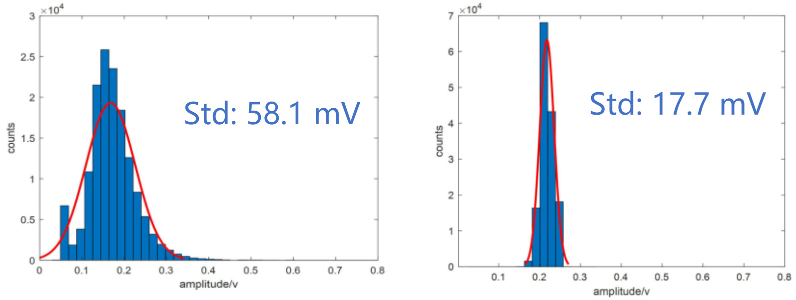
Probe Card Test – ATE: Yield > 95%



BPIX Detector Module



User DAQ Platform



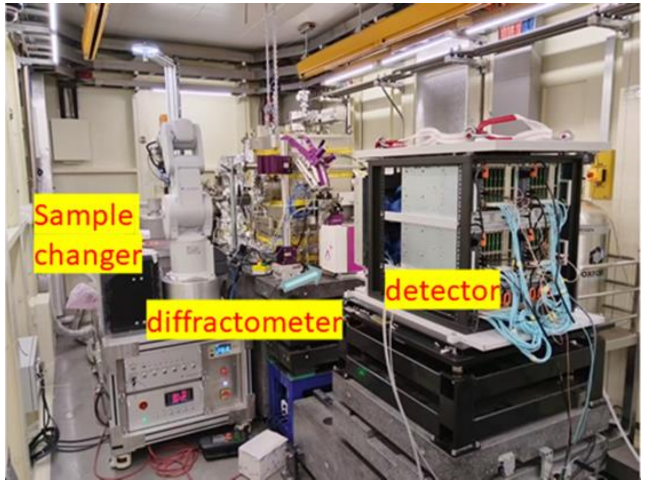
Distribution of thresholds before and after calibration.
Minimum threshold: 3 keV

6M-pixel BPIX Detector Installation

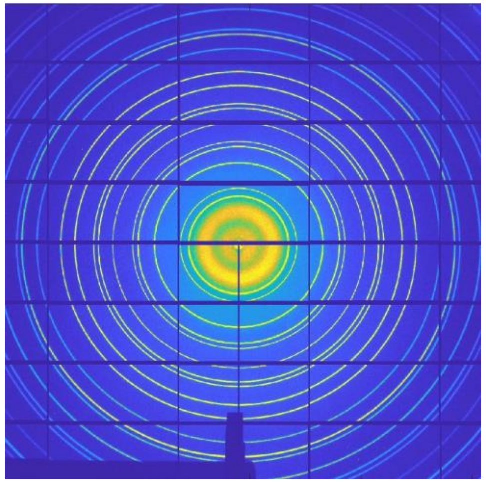
BPIX Back-end Electronics

BPIX-6M

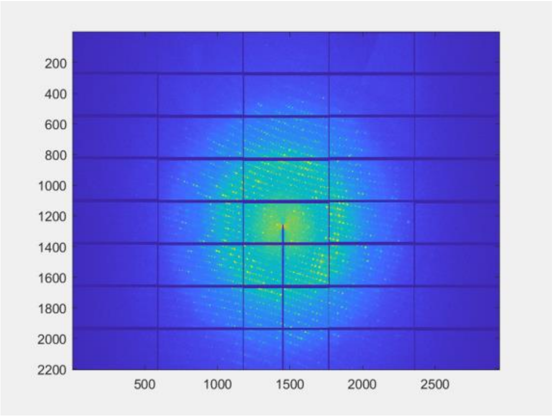
- For the BA beamline station pilot operation, 31 projects were ultimately completed.
- As the main detector of the BA beamline station, the BPIX detector enabled stable operation of user experiments.

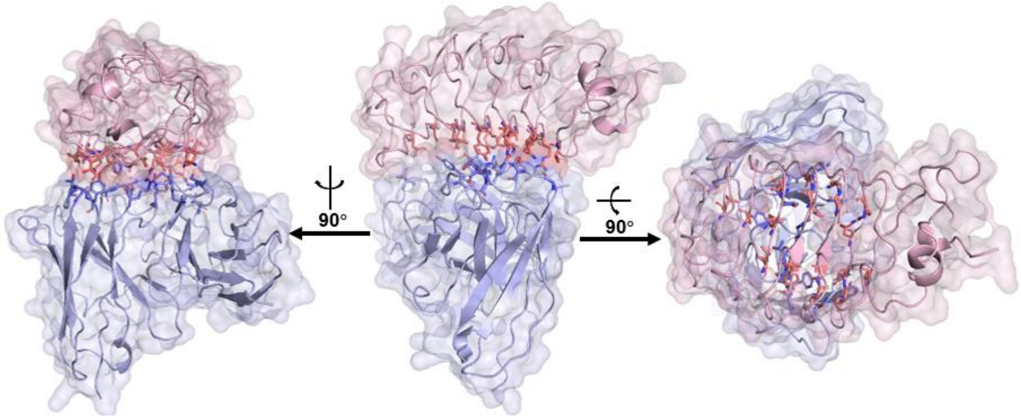


6M BPIX pixel detector



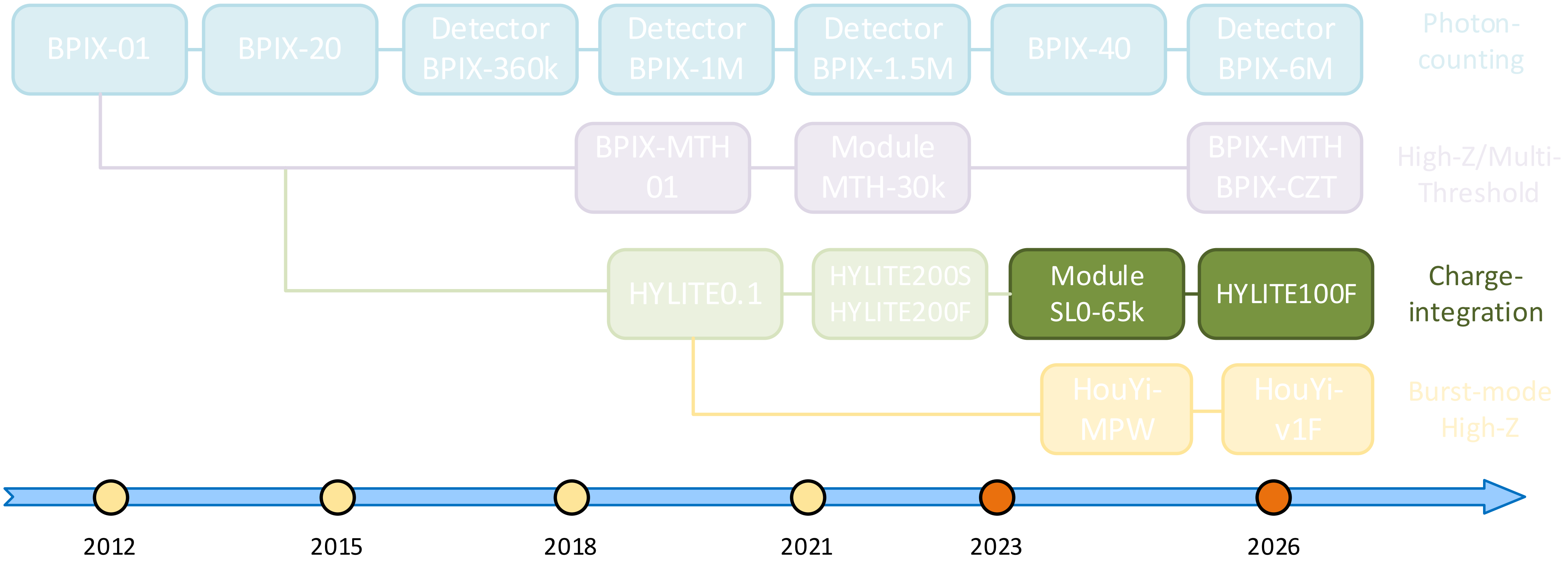
6M pixel detector Imaging



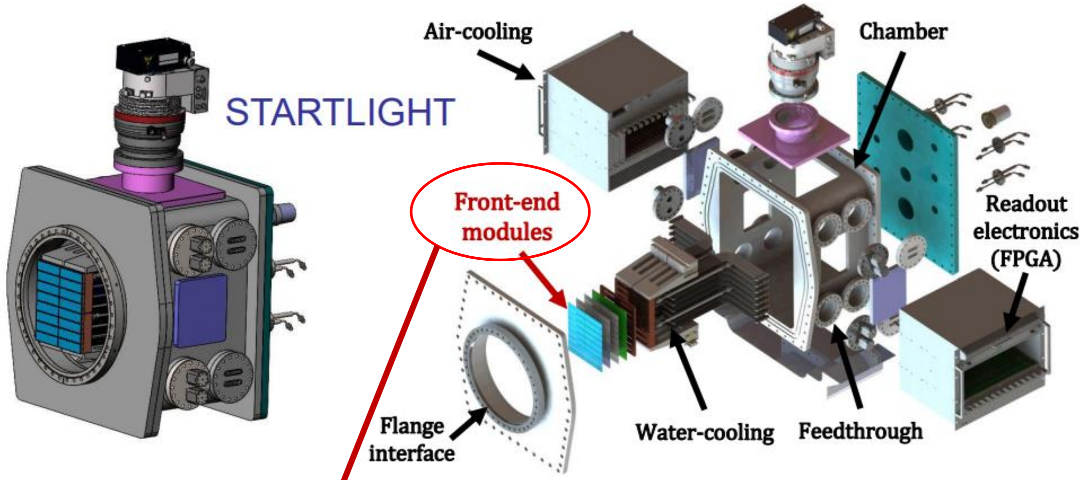


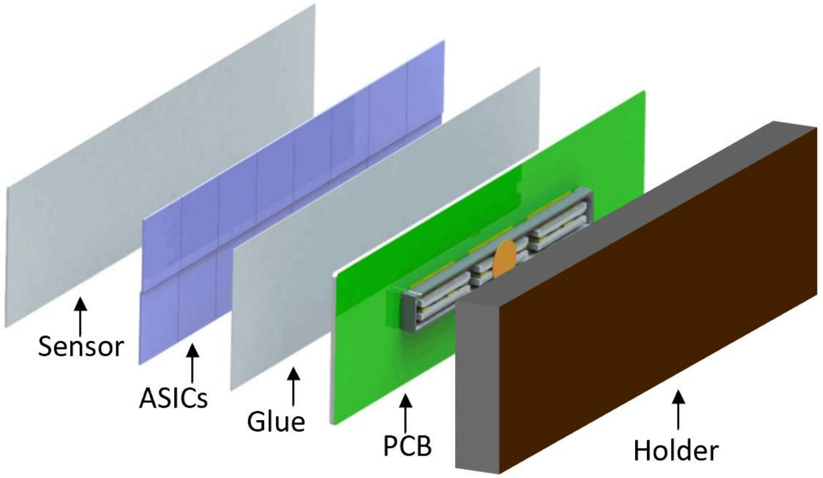
User Experiment: Protein-protein Complex

Outline


BPIX-01
BPIX-20
Detector BPIX-360k
Detector BPIX-1M
Detector BPIX-1.5M
BPIX-40
Detector BPIX-6M
Photon-counting
BPIX-MTH 01
Module MTH-30k
BPIX-MTH BPIX-CZT
High-Z/Multi-Threshold
HYLITE0.1
HYLITE200S HYLITE200F
Module SL0-65k
HYLITE100F
Charge-integration
HouYi-MPW
HouYi-v1F
Burst-mode High-Z
2012
2015
2018
2021
2023
2026

STARLIGHT Detector





Front-end Module Structure

- **HYLITE** (**H**igh d**Y**mamic range free electron **L**aser **I**maging de**TE**ctor) is a charge-integration pixel detector readout chip designed for SHINE XFEL (Detector: STARLIGHT).
- SemiconducTor Array detectoR with Large dynamIc ranGe and cHarge inTegrating readout

Specs	STARLIGHT0	STARLIGHT1
Sensor	500 µm silicon p-in-n	/
Pixel Size	200 µm × 200 µm	100 µm × 100 µm
Array Size	64 × 64	128 × 128
Dynamic range	1~10000 ph./pulse/pixel @ 12 keV	/
Frame rate	1 kHz	10 kHz
Detector	2×8 ASIC module	A 4M pixel detector in vaccum, quadrant movable

HYLITE Development Timeline

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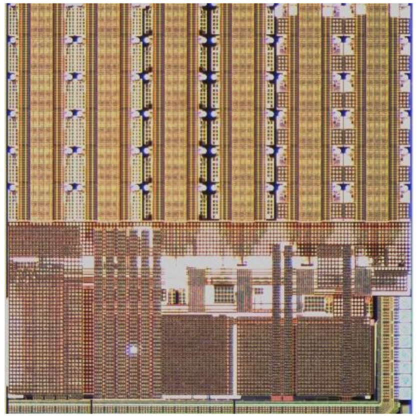
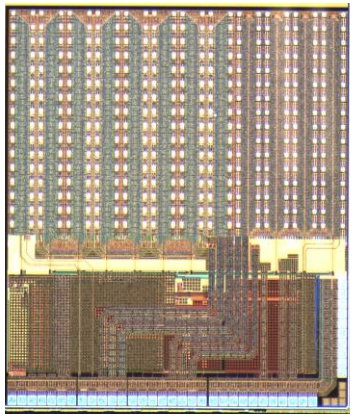
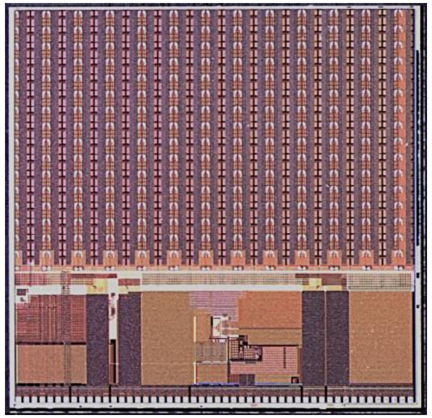


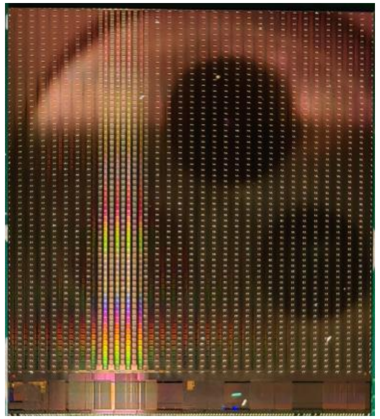
- HYLITE0.1
- First small-scale array for basic functions verification
- Date: 2020.10



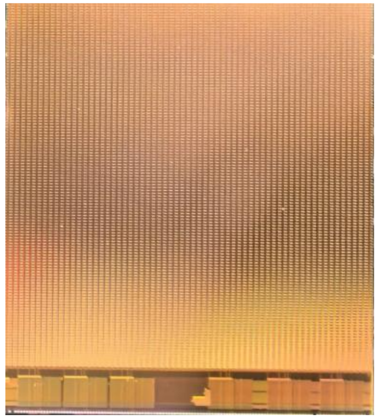
- HYLITE0.2
- Small-scale array with distributed LDO
- Date: 2021.4



- HYLITE200S
- Small-scale array with PLL and high-speed serializer
- Date: 2022.2



- HYLITE200F
- First full-scale array
- Bump-bonded with sensor
- Date: 2022.8



- HYLITE100F
- 100-µm pixel full-scale chip with PLL and high-speed serializer
- Date: 2026.1

Under testing

HYLITE: Architecture

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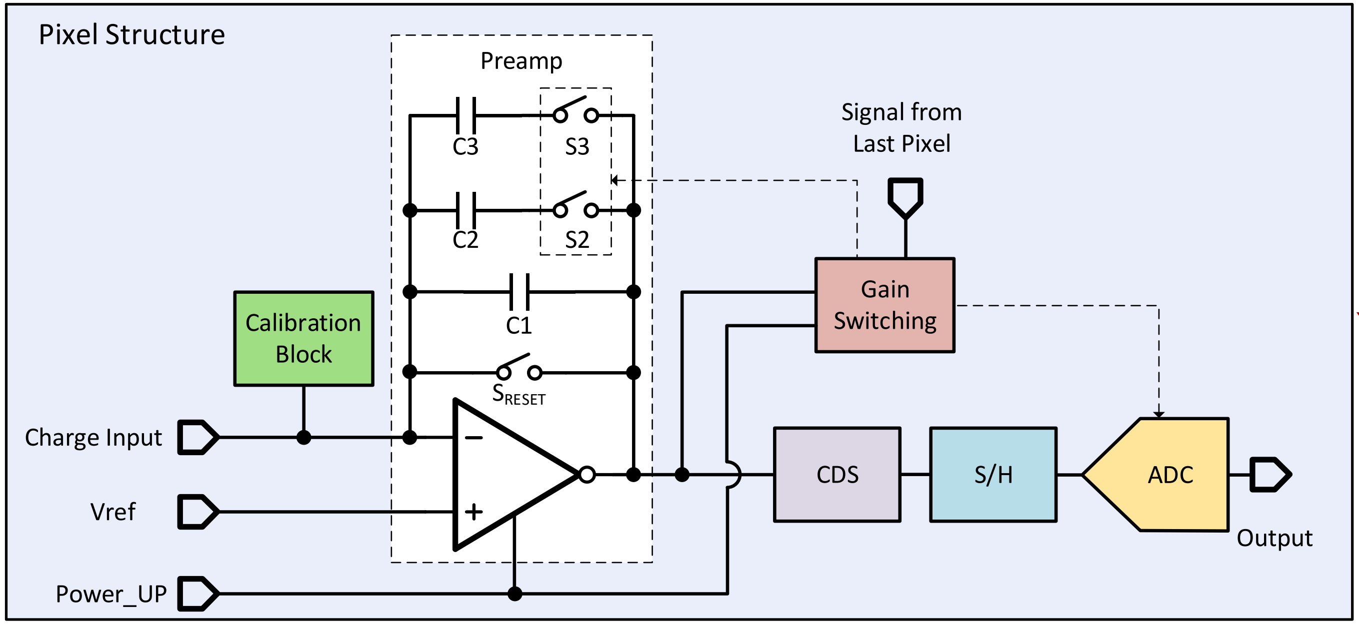

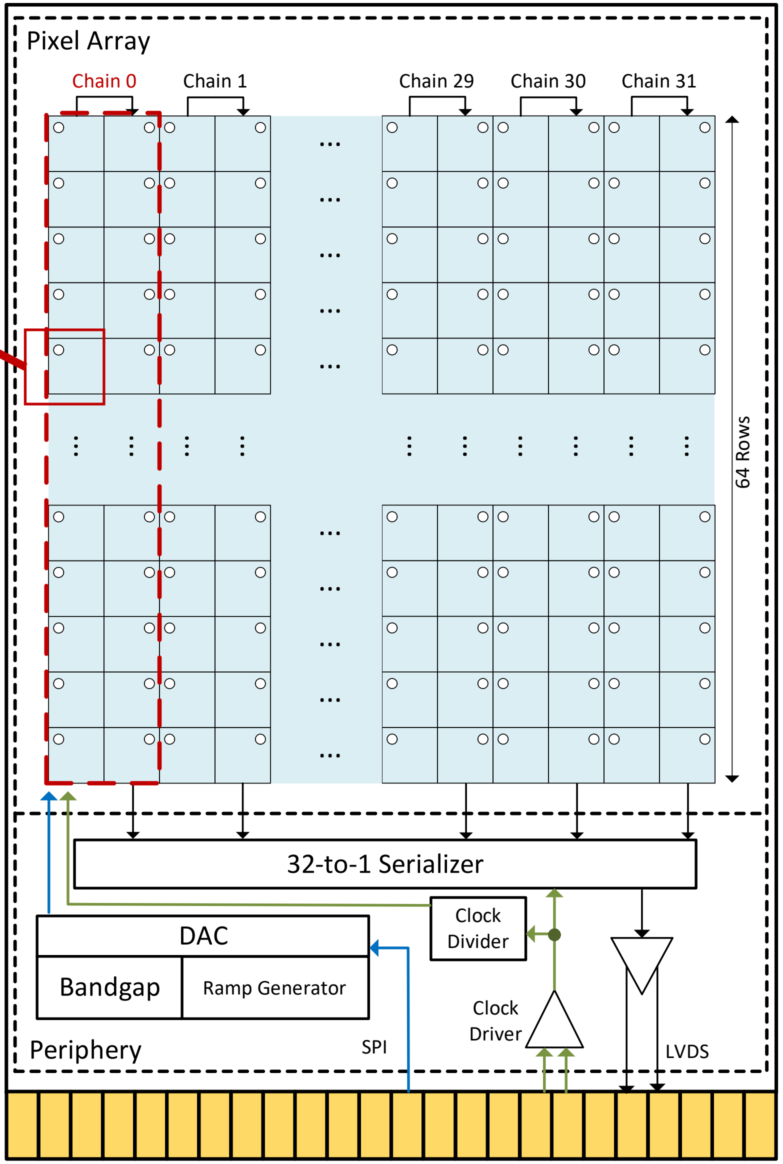

- Technology: 130 nm 1P8M CMOS
- Pixel Pitch: 200 µm -> 99 µm （110nm process compatible）
- Array Size: 64 × 64 -> 128 × 128
- In-Pixel ADC: 10 bits
- Automatic gain switching with 3 gains
- Frame Rate: 6.3 kHz Maximum (@ 400 MHz clock)->10 kHz
- Power Consumption: <50 µW/pixel

HYLITE100F: Data Interface

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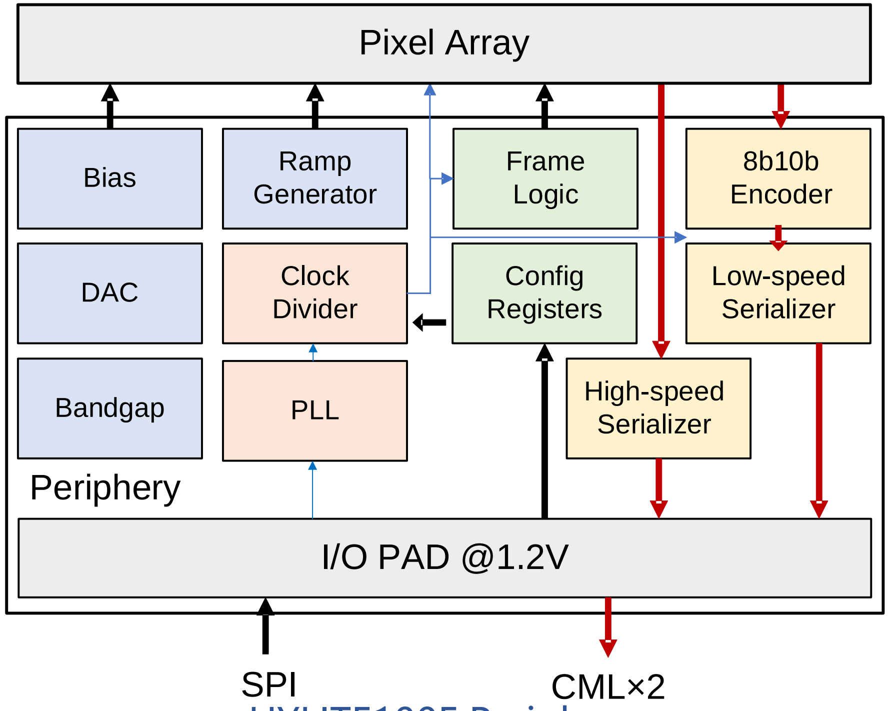


HYLITE100F Periphery

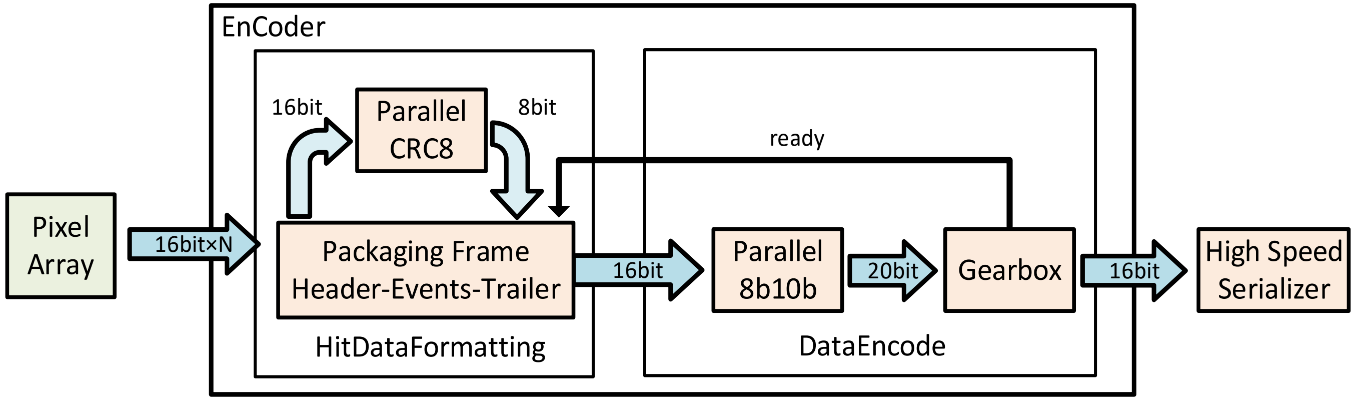
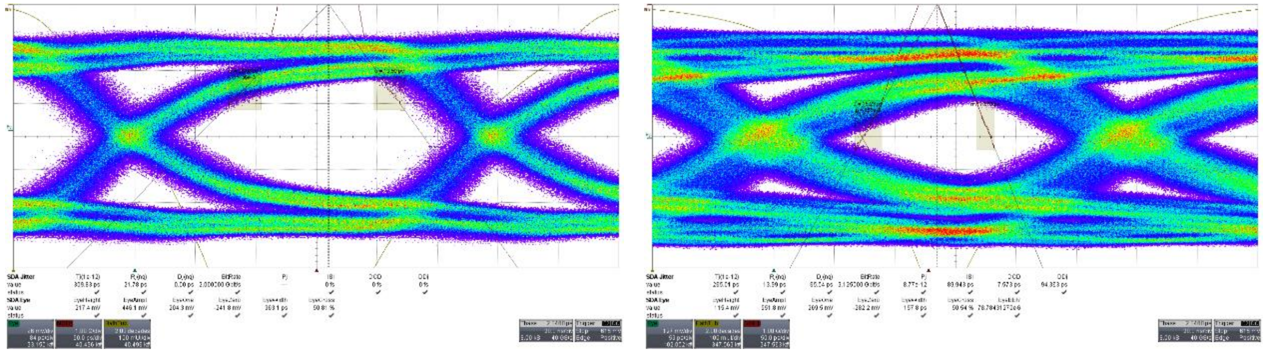


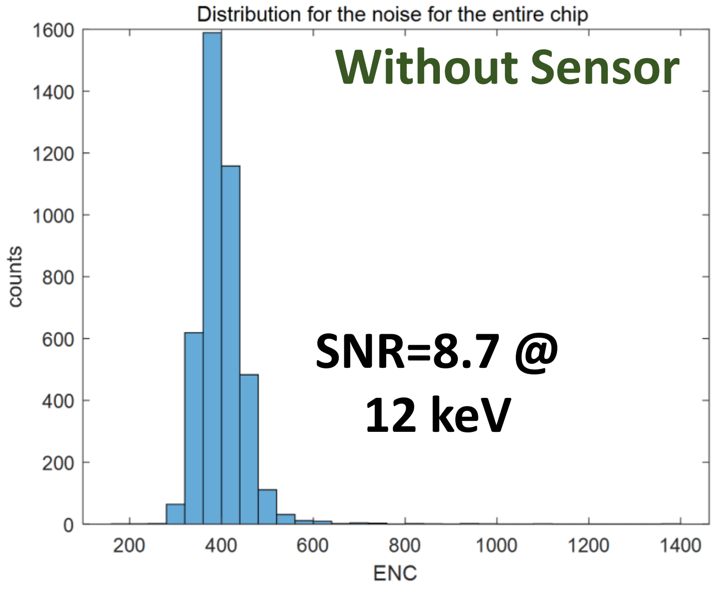
Diagram of the 8b10b Encoding Block

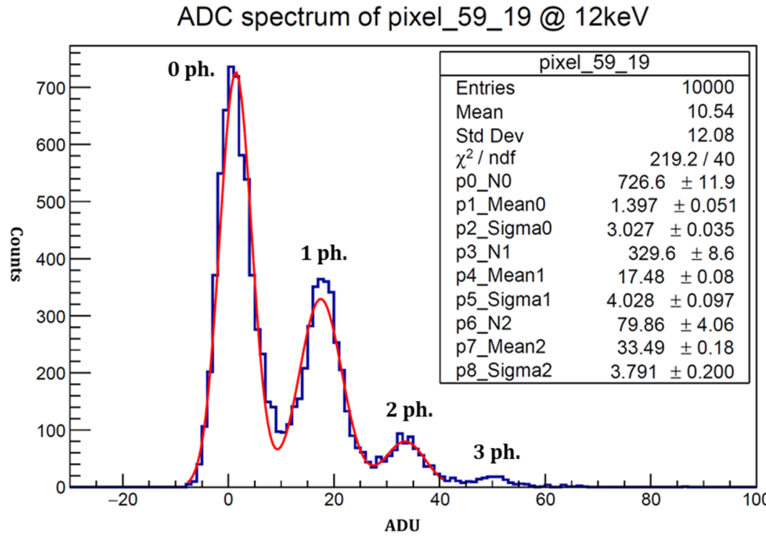
- Single Chip Data Rate:
  - ~3.2 Gbps @ 8b10b
  - ~2.56 Gbps @ no encoding



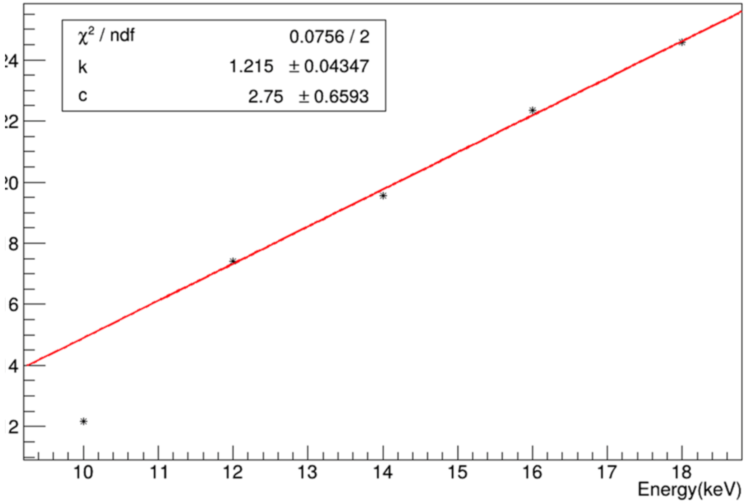
Eye grams of two different data rates with 30-cm cable
(a): 2 Gbps. (b): 3.125 Gbps. (By. Xiaoting Li)

Noise and Linearity

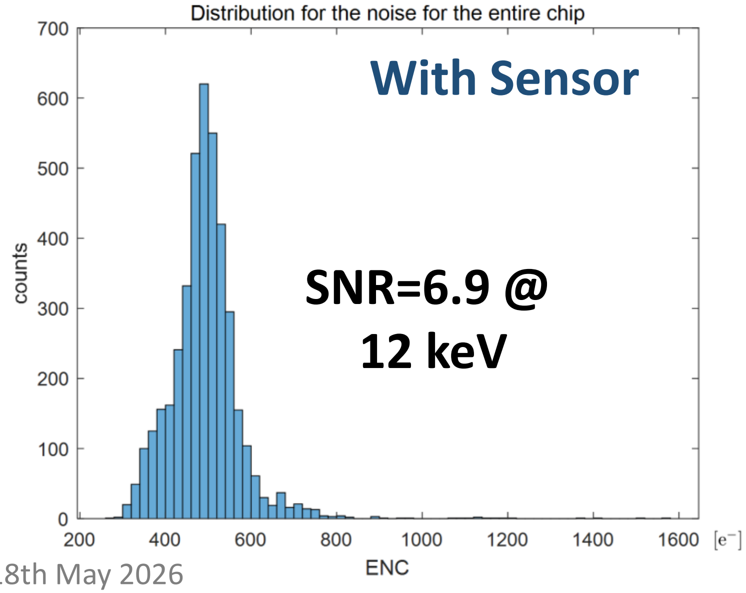




Statistics of counting on SSRF@12keV



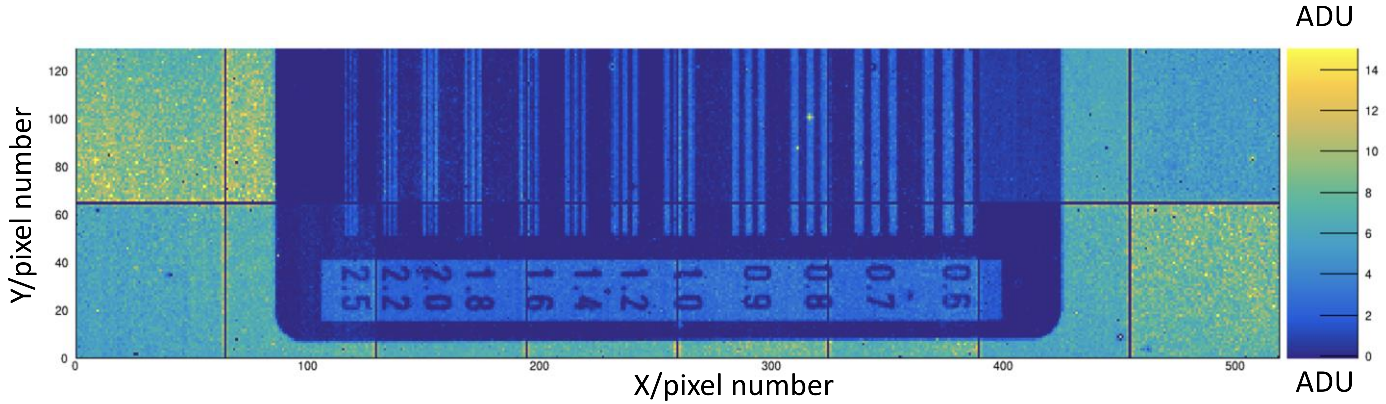
Gain-Energy linearity on SSRF

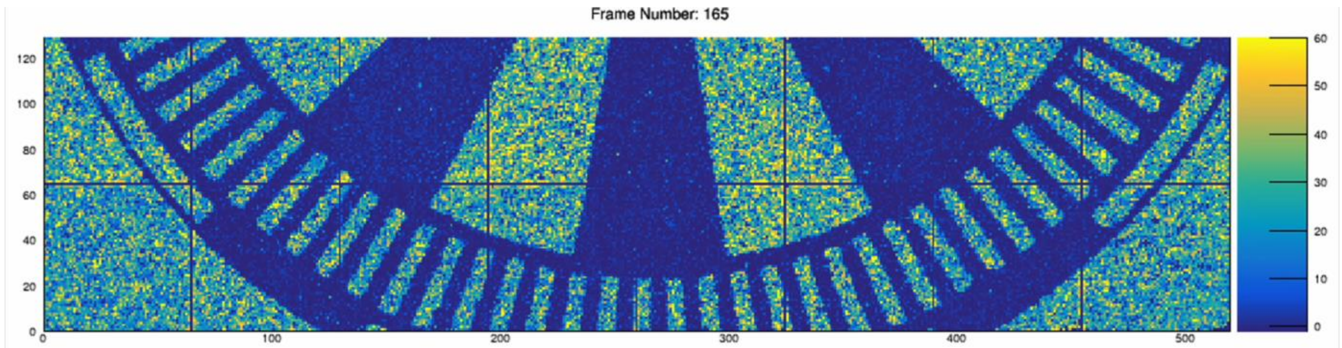


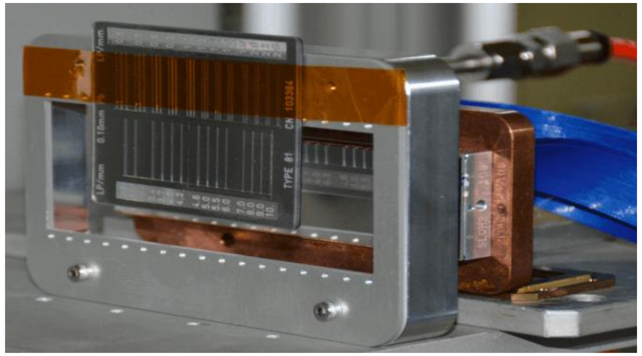
- ENC: 386 e- vs. 487 e- @ single photon injection.
  - Improved design (unpublished): ~100 e-
- 12 keV synchrotron： single/double/triple-photon peaks
- Good gain-energy linearity (sensor damage @ 10 keV)

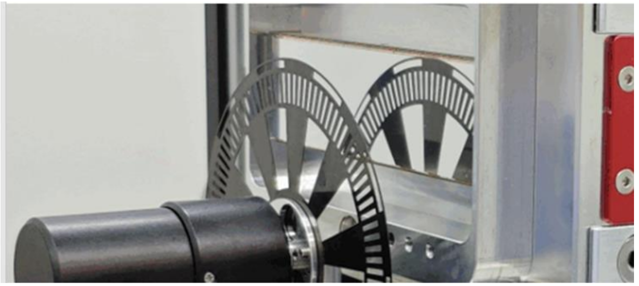
- Average yield of wafers: 83.7%

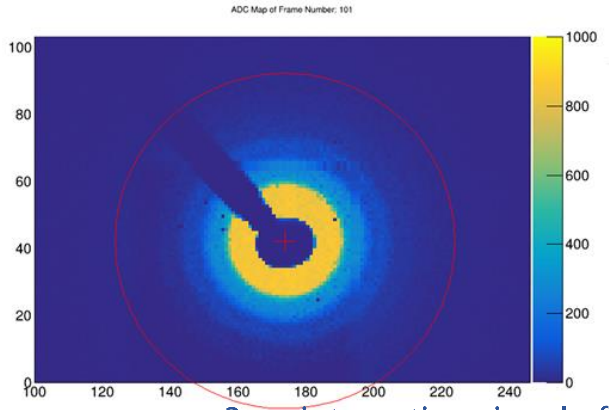
Module Performance

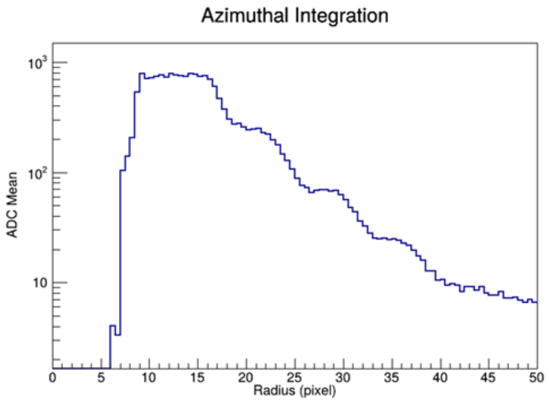












3-μs integration signal of silicon powder SAXS experiment

- Frame Rate: 1 kHz
- Chopper Rotation Frequency: 100 Hz
- **SAXS @ HEPS-SDB (Structure Dynamic Beamline)**

Outline

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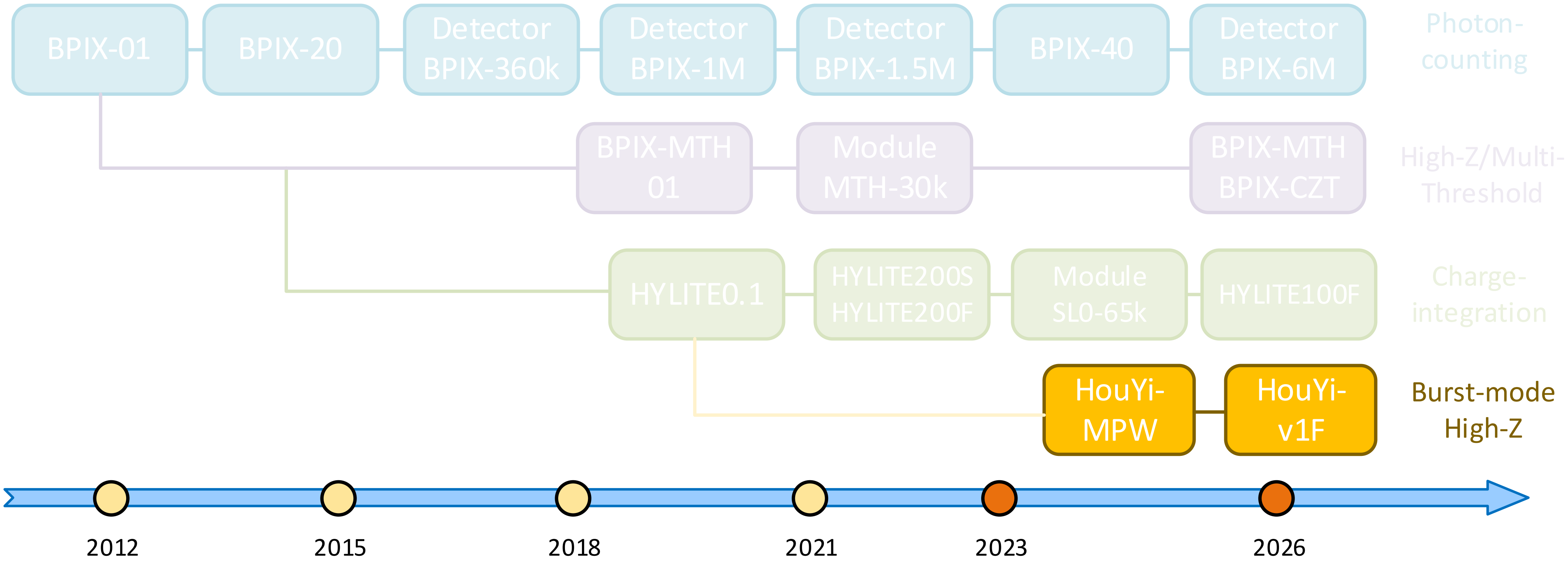

HouYi: Burst Mode Charge-integration

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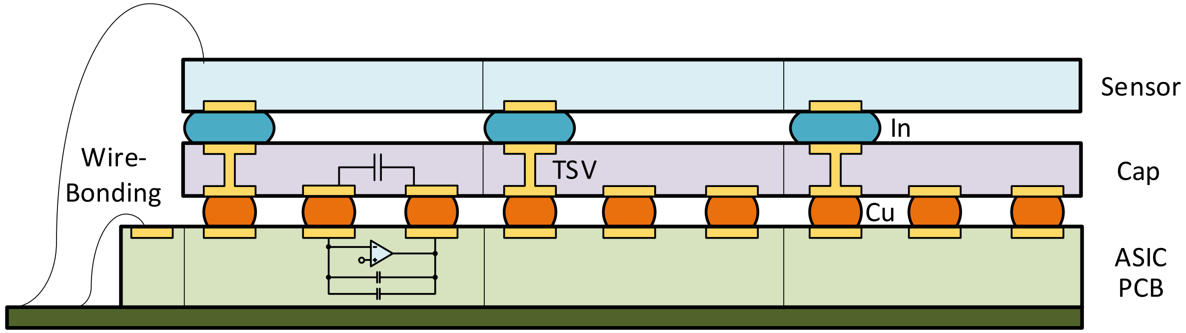
HouYi Shoots the Suns

- Start R&D in 2025
- Aiming for High-Z detector with large dynamic range
- Inherited and optimized the design of HYLITE



3D Integrated Structure of HouYi

Items	Specs
Sensor	CZT (Electron Collection)
Pixel Size	150 µm × 150 µm
Array Size	64 × 64
Dynamic Range	1 ~ 4000 ph./pulse/pixel @ 30 keV
Frame Rate	1 MHz ~ 4.7 MHz @ burst mode
Buffer Depth	32

- Extendable dynamic range via reserved pads for 3D integrated structure
- Sensor: Top Layer, In bump
- Cap: ~25 pF/pixel, PIP Capacitor, 350 nm Process
- ASIC: 130 nm Process, Cu pillar

HouYi: Pixel Design

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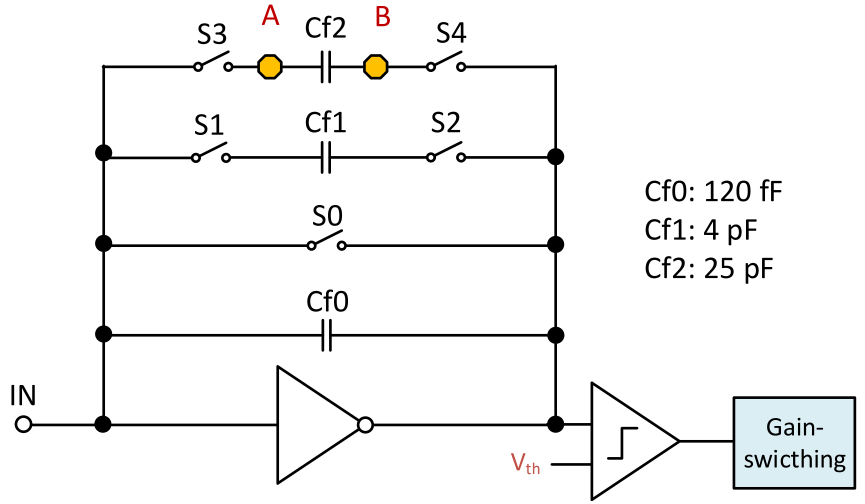
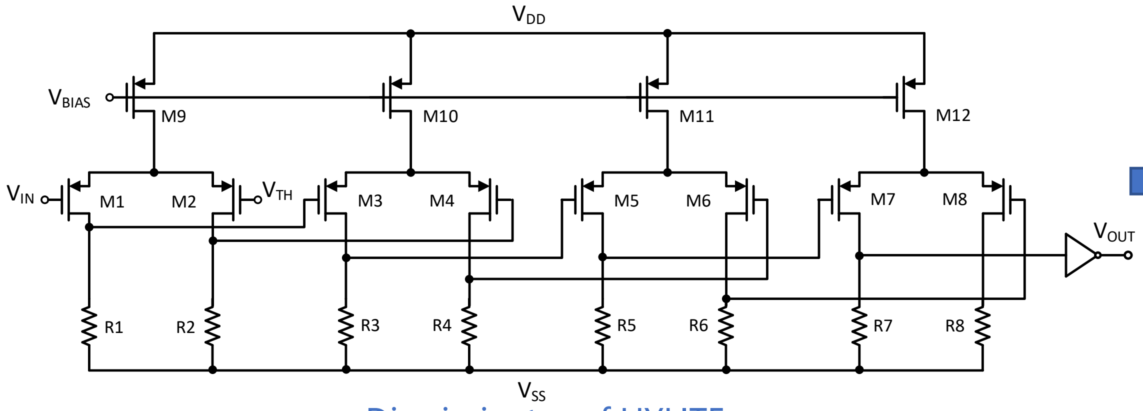
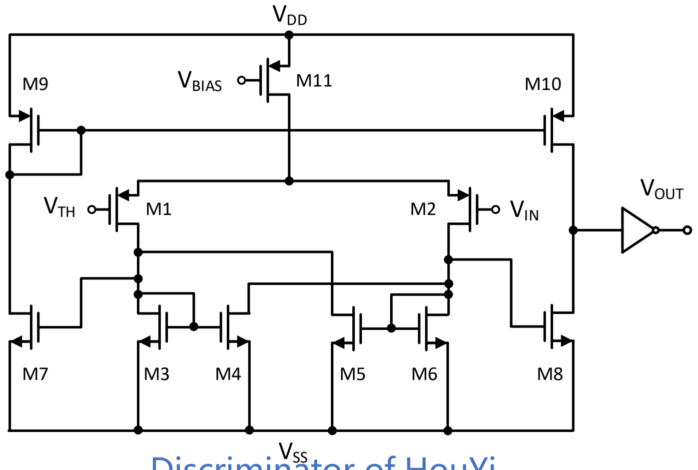


Front-end of HouYi

- Put Cf2 in a separate CAP chip.
- Improved design of the Front-end inherited from HYLITE:
  - Polarity modified
  - Front-end circuits with lower power consumption: e.g: discriminator:
    - HYLITE: ~ 280 μW(Power on)
    - HouYi: ~ 10 μW



Discriminator of HYLITE



Discriminator of HouYi

HouYi: Architecture

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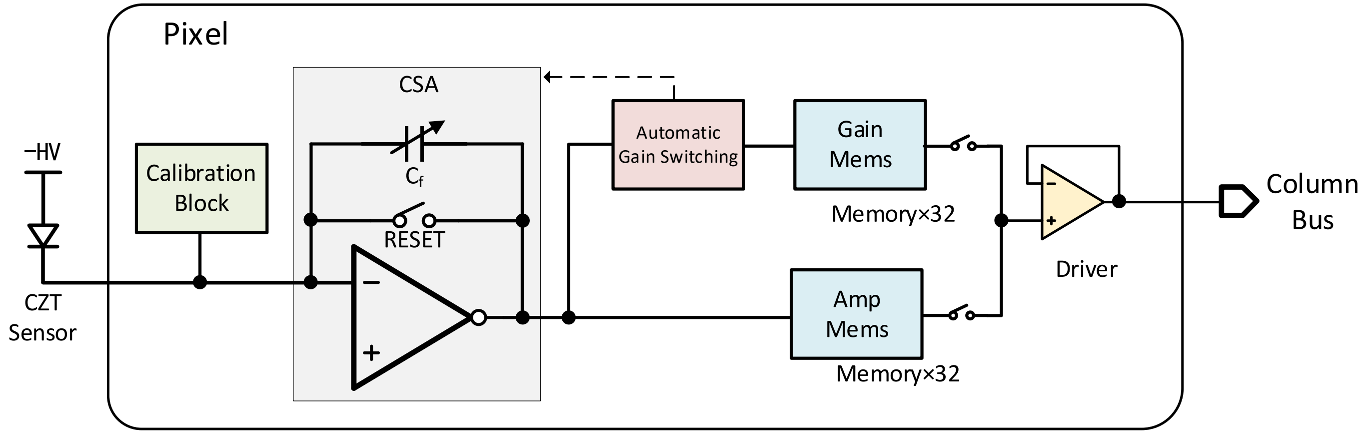
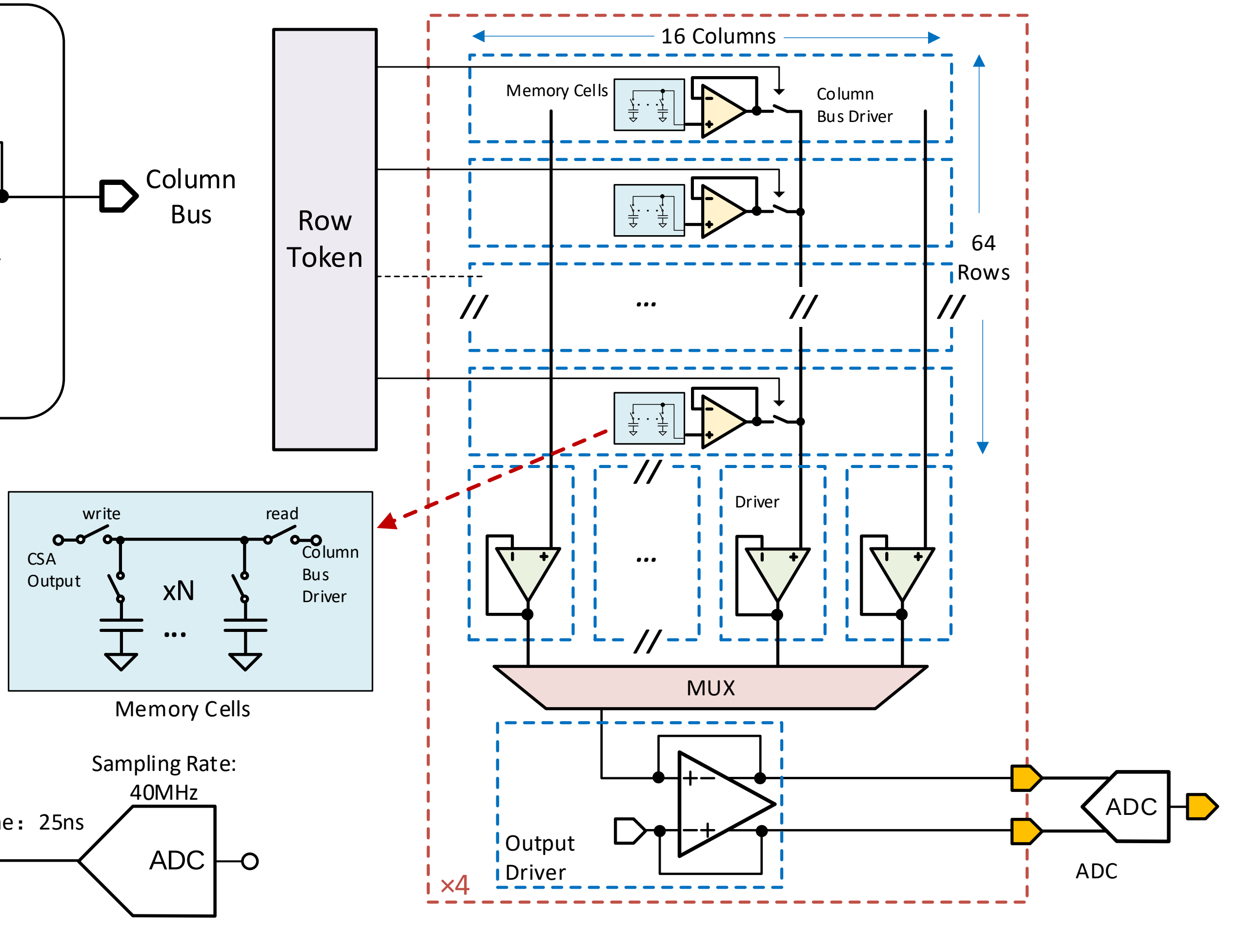
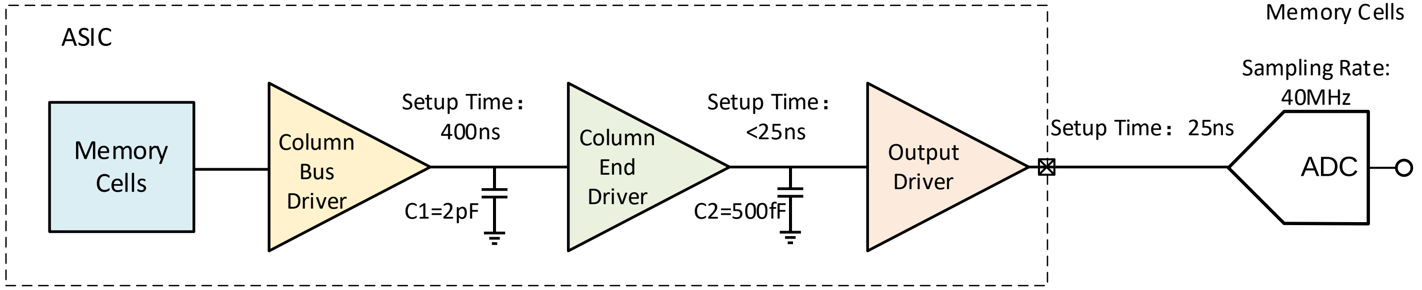


Pixel Structure of HouYi

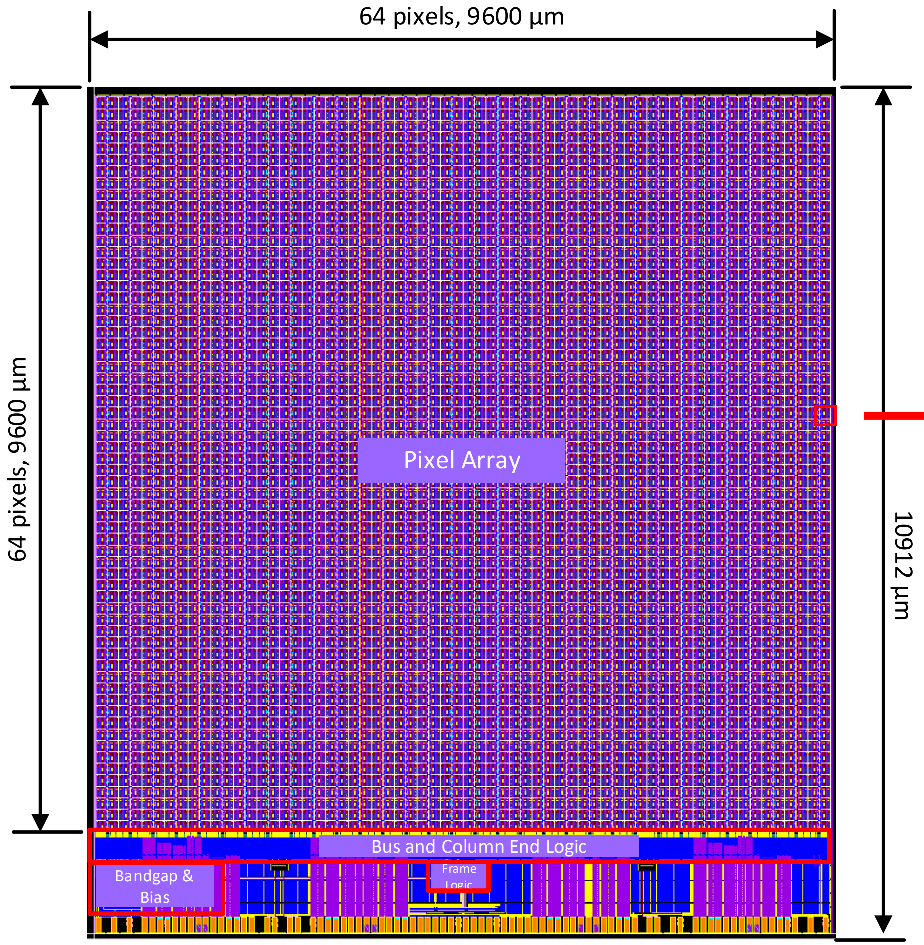


Readout Structure of HouYi

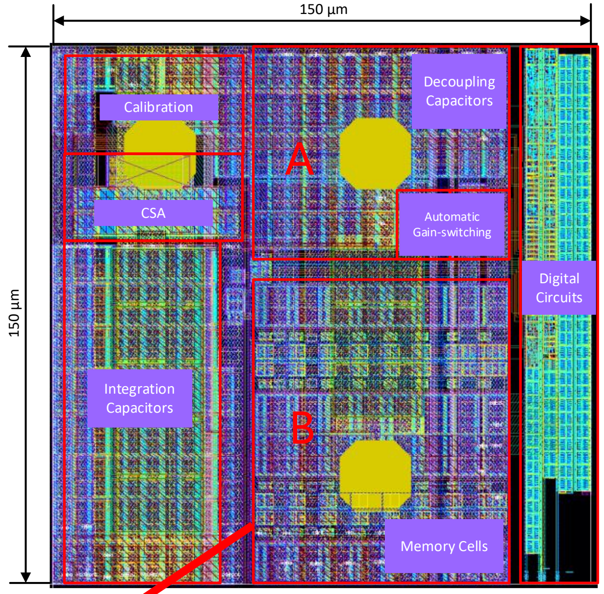


Signal Chain of HouYi

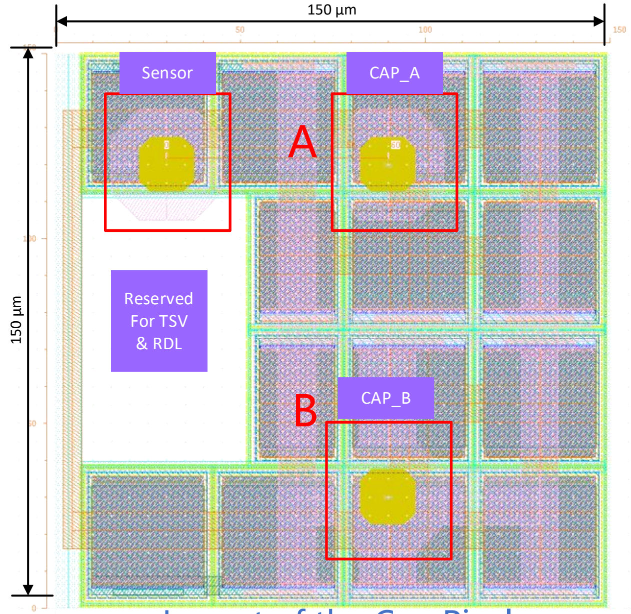
Layout of HouYi



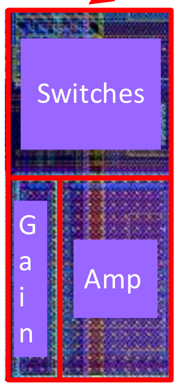
Layout of the HouYi_v1F Chip

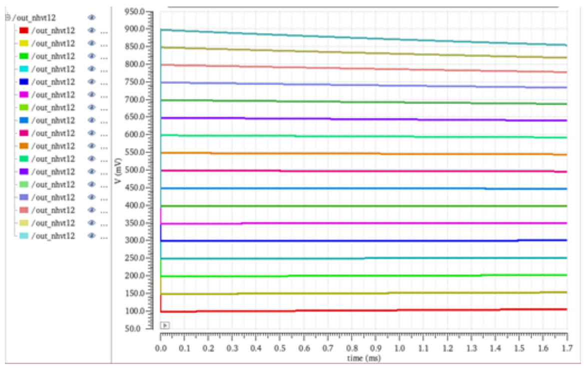


Layout of the HouYi Pixel



Layout of the Cap Pixel





Layout of the Memory Cell

- Thick gate oxide layer transistor for capacitor
- HVT MOS as the switch for lower leakage

Test Results of HouYi_MPW

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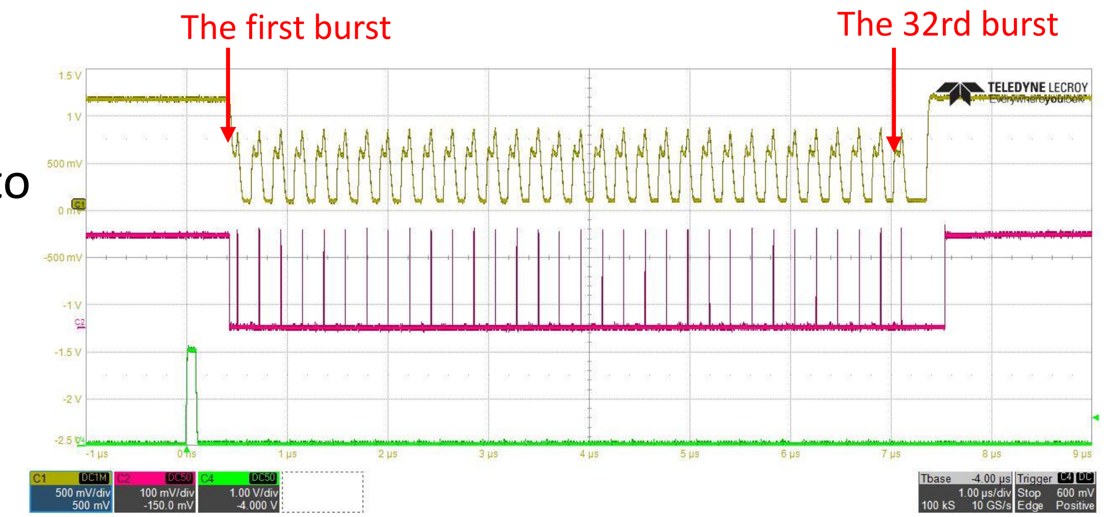
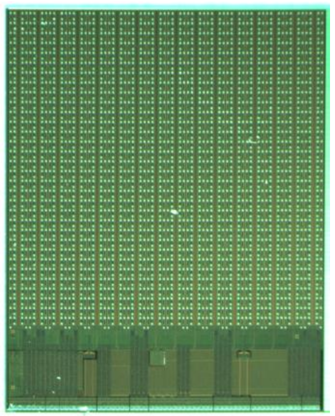
- Achieved 4.7MHz readout for 32 frames
- ADC sampling rate can reach up to 40 MHz
- Dynamic range of up to 4000 photons @ 30 keV
- Non-linearity is about 3.1%
- SNR at high-gain stage: 7.72 vs 6.14 @30 keV (leakage caused)

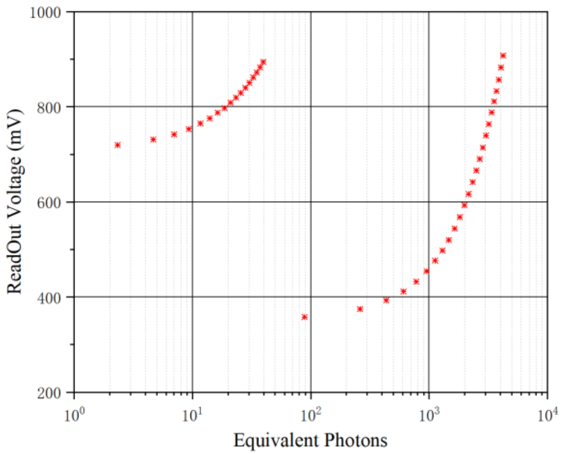


Output waveform of the Pre-amp: 4.7 MHz

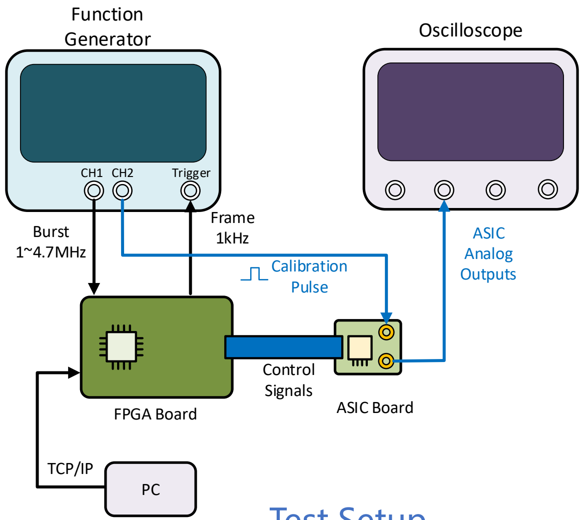


HouYi_MPW: 32×32 pixels

Pixel Position	Gain Stage	Gain /(mV/ph.)	Non-linearity
1st Burst_pix1	High	4.65	0.91%
	Low	0.135	2.49%
32rd Burst_pix256	High	3.70	1.53%
	Low	0.101	3.08%



Dynamic Range of HouYi



Test Setup

Sensor-ASIC Joint Test

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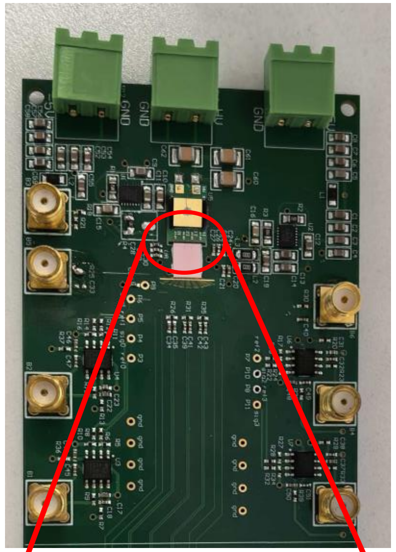
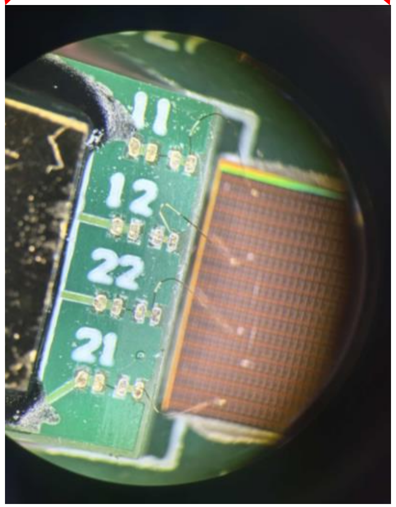
- Sensor: 2×2 pixels CZT, wire bonded with the ASIC
- The output shows a clear response to light, indicating that the entire signal chain from the sensor to the ASIC readout is working correctly

Outputs under the Weak Light

Outputs under the Strong Light



Test PCB



Sensor is wire bonded with ASIC

Outline

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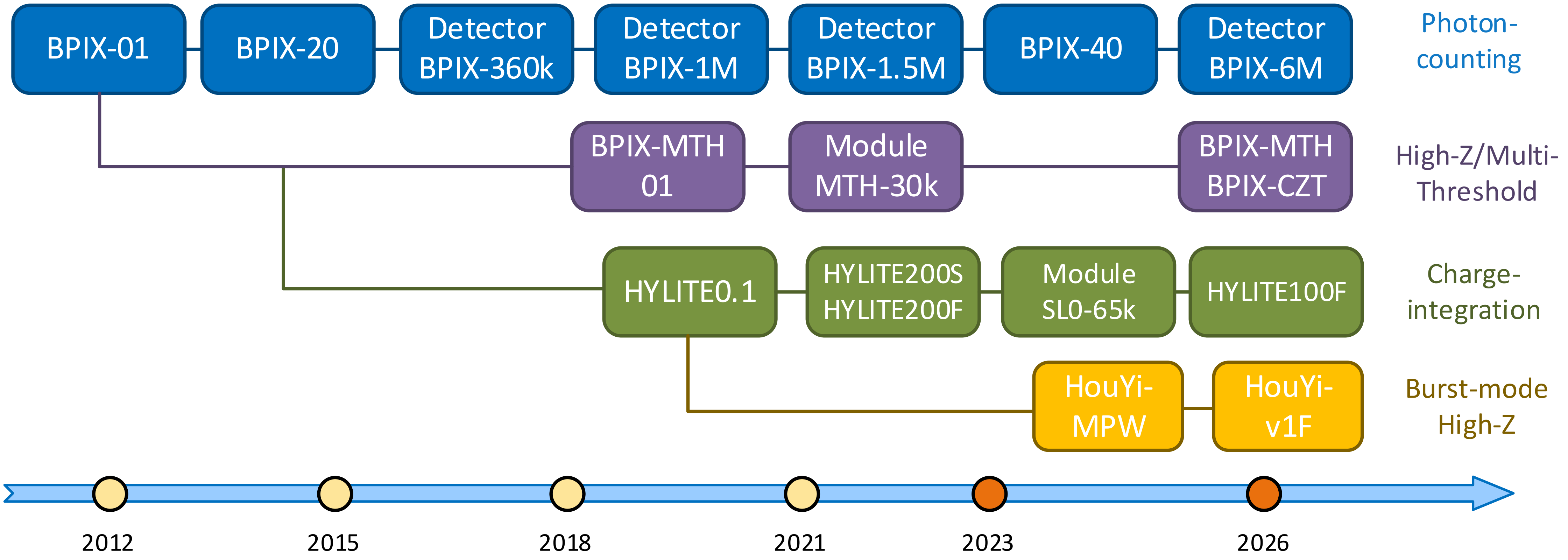
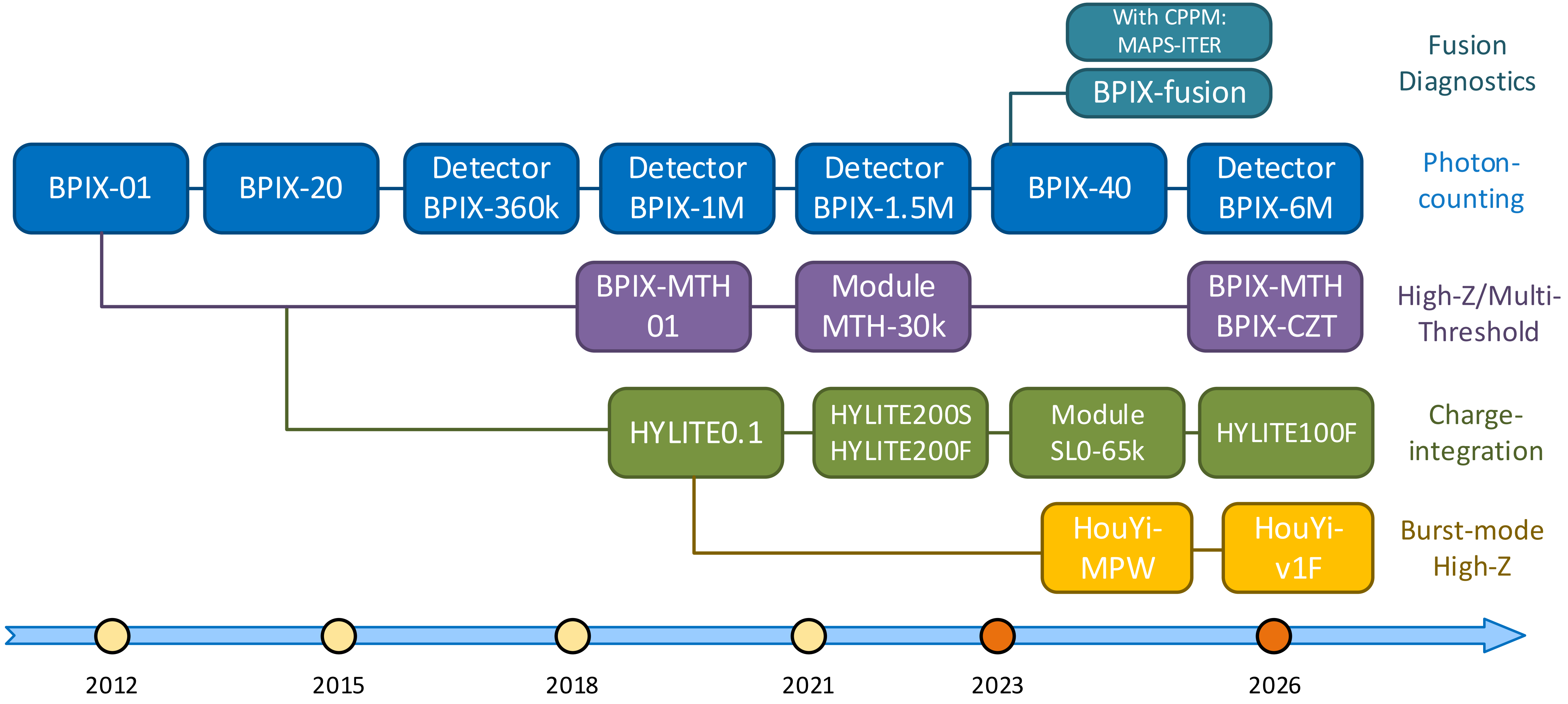


Outline



With CPPM: MAPS-ITER
BPIX-fusion
Fusion Diagnostics
BPIX-01
BPIX-20
Detector BPIX-360k
Detector BPIX-1M
Detector BPIX-1.5M
BPIX-40
Detector BPIX-6M
Photon-counting
BPIX-MTH 01
Module MTH-30k
BPIX-MTH BPIX-CZT
High-Z/Multi-Threshold
HYLITE0.1
HYLITE200S HYLITE200F
Module SLO-65k
HYLITE100F
Charge-integration
HouYi-MPW
HouYi-v1F
Burst-mode High-Z
2012
2015
2018
2021
2023
2026

Fusion Diagnostics

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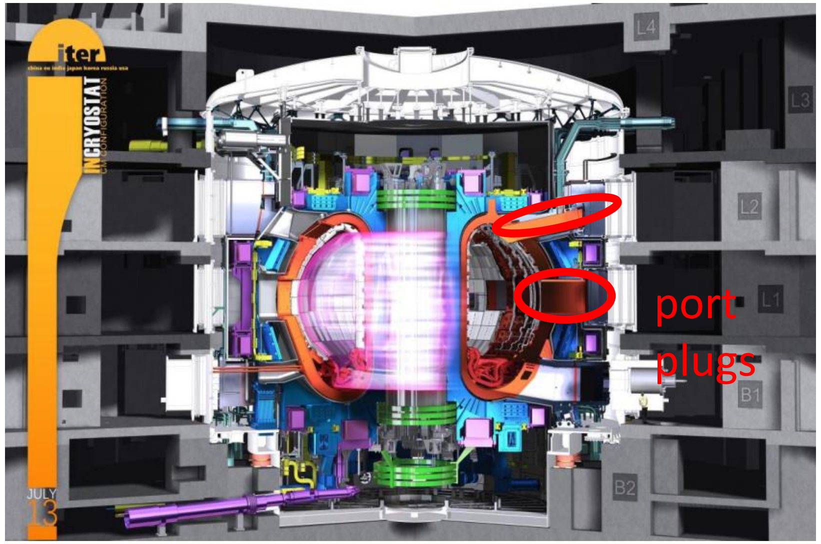
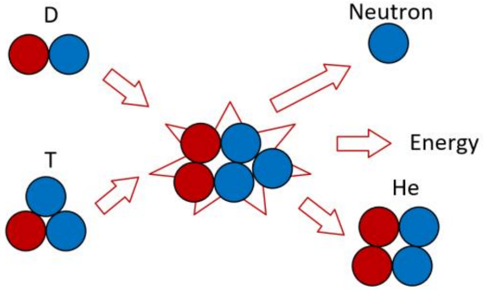
- Fusion diagnose system： “Multi-messenger” (Visible/UV/X-ray/neutron…)
- **XRCS: X-Ray Crystal Spectrometer: Temperature and rotate speed of plasma, first wall material…**
- ITER 7 Cooperators：CN, EU, IN, JA, KO, RF, US
- **Construction of fusion facilities was approved in China. E.g.: BEST**



ITER Vacuum and Port Plugs

ITER: International Thermonuclear Experimental Reactor



D-T Fusion Process


BEST: Burning plasma Experimental Superconducting Tokamak

Ref: Raphael TIEULENT, TWEPP2023, Sardinia Italy, October 2023

Specifications of ITER XRCS Pixel Detector

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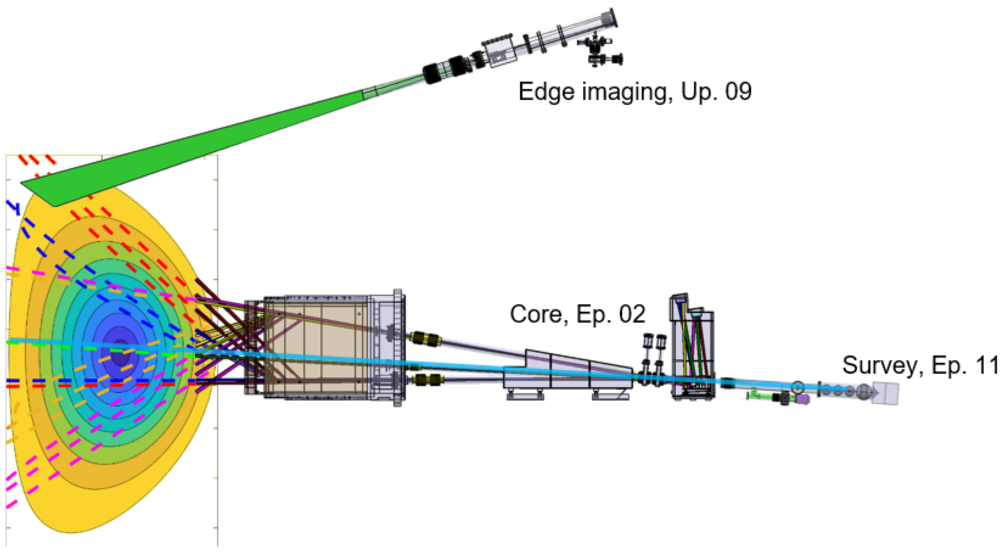

Red, Green-1 and **Magenta** Sights: Xe^{44+} **(2.5525Å)** and **Xe^{47+} (2.5572Å)** from 0a to 0.85a
Blue and **Yellow** sights: Xe^{51+} 2.1899Å for 0~0.55a
Green-2 View: W^{64+} (1.354Å) passing through plasma center

- XRCS：Core/Edge/Survey：Different Detection Energy
  - Core & Edge：Single-photon resolution @ 3 keV
- Detector Panel Neutron Flux：10^6 / s·cm^2
  - Separated front-end and back-end
- Panel Size：180 mm × 85 mm
- Vacuum： UHV (10^{-5}~10^{-6} pa)
- Magnet：0.2 T
- Run-time control latency：<10 ms
- Maximum Counting Rate：10^7 counts/s/mm^2

Sub-system	XRCS Core	XRCS Survey	XRCS Edge
Wavelength (Å)	2.555 (4.852keV) 2.189 (5.663keV) 1.354 (9.156keV)	1-100 (0.12keV - 12keV)	3.97 (3.12keV) 3.73 (3.32keV)

Ref: Zhifeng Cheng, ITER Spectroscopic Diagnostics and Atomic Data Needs, 2023 Vienna

BPIX System Test for ITER

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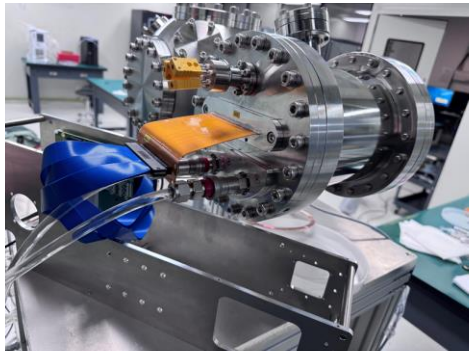
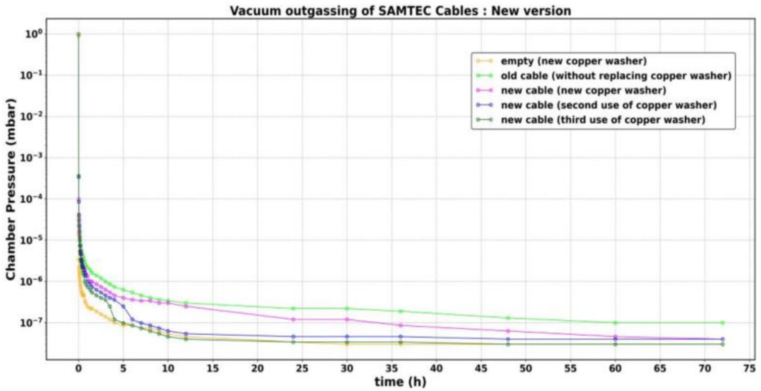
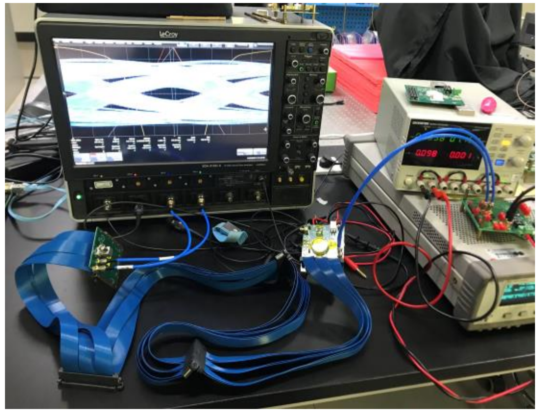
- Vacuum Compatibility
  - All components must meet ITER VQC-1 vacuum quality requirements.
  - Test result: < 10^{-7} mbar
- X-ray Energy Sensitivity
  - Target: 3 keV
  - Test result: 6 keV
- Magnetic Field Resistance:
  - Target: 0.2 T
  - Test result: pass
- Neutron Radiation Tolerance
  - To be specified
  - Long-cable data transfer test: 2.56 Gbps via 1.6-m cable

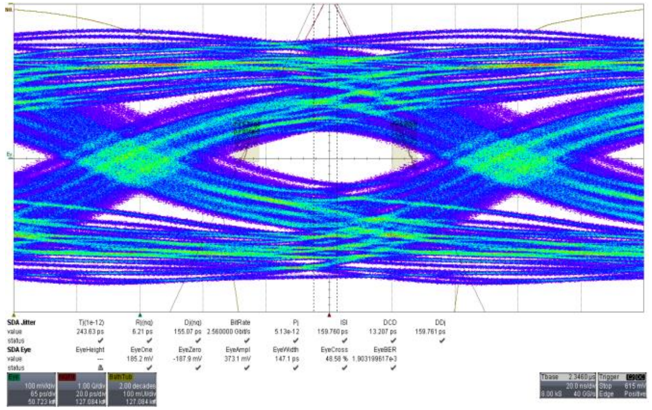


Vacuum feedthrough and test structure



Vacuum outgassing of the feedthrough cables

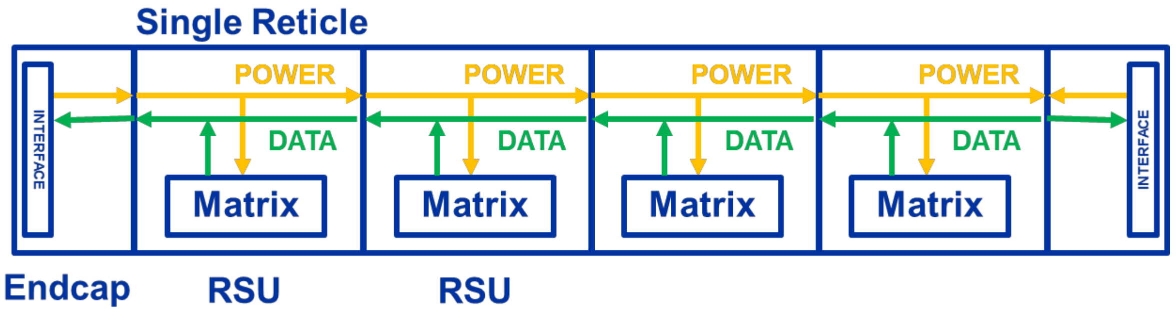




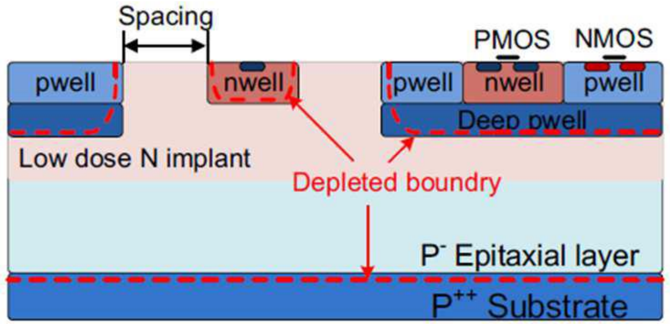
Test setup and eye gram of the data port on the speed of 2.56 Gbps via a 1.6-m long cable

MAPS Architecture

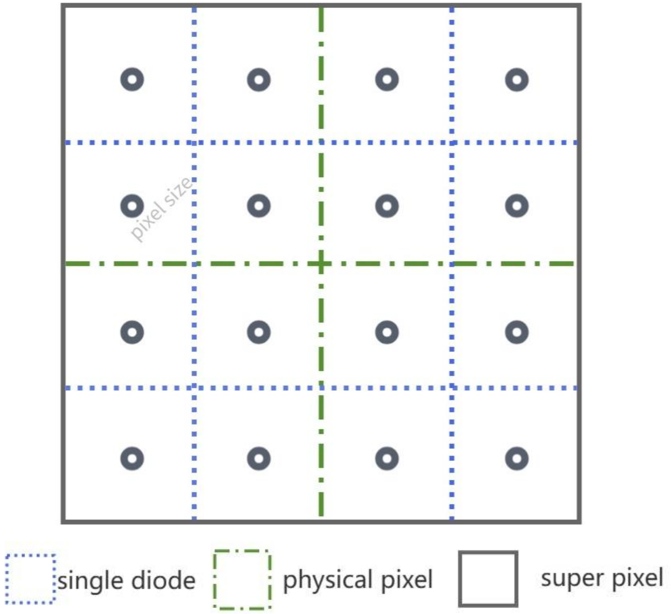
- **Cooperation with CPPM: Patrick Pangaud, Marlon Barbero, Danwei Xu**
- Single-photon resolution @ 3keV
  - MAPS + photon-counting
  - C_{in} < 1 fF / diode
  - Energy of threshold: 1.5 keV -> ENC < 40 e- (SNR of 10)
- Large-area panel and less dead area
  - Stitching
- Pixel Size: 100 μm × 100 μm
  - Physical pixel：25 μm × 25 μm
  - 16 diodes per pixel
- High flux of neutron
  - Double threshold to reject neutron hits
- Latency: < 10 ms
  - Frame rate>100 Hz -> 200 Hz
  - Two Counters/pixel，ping-pang



Stitching Structure



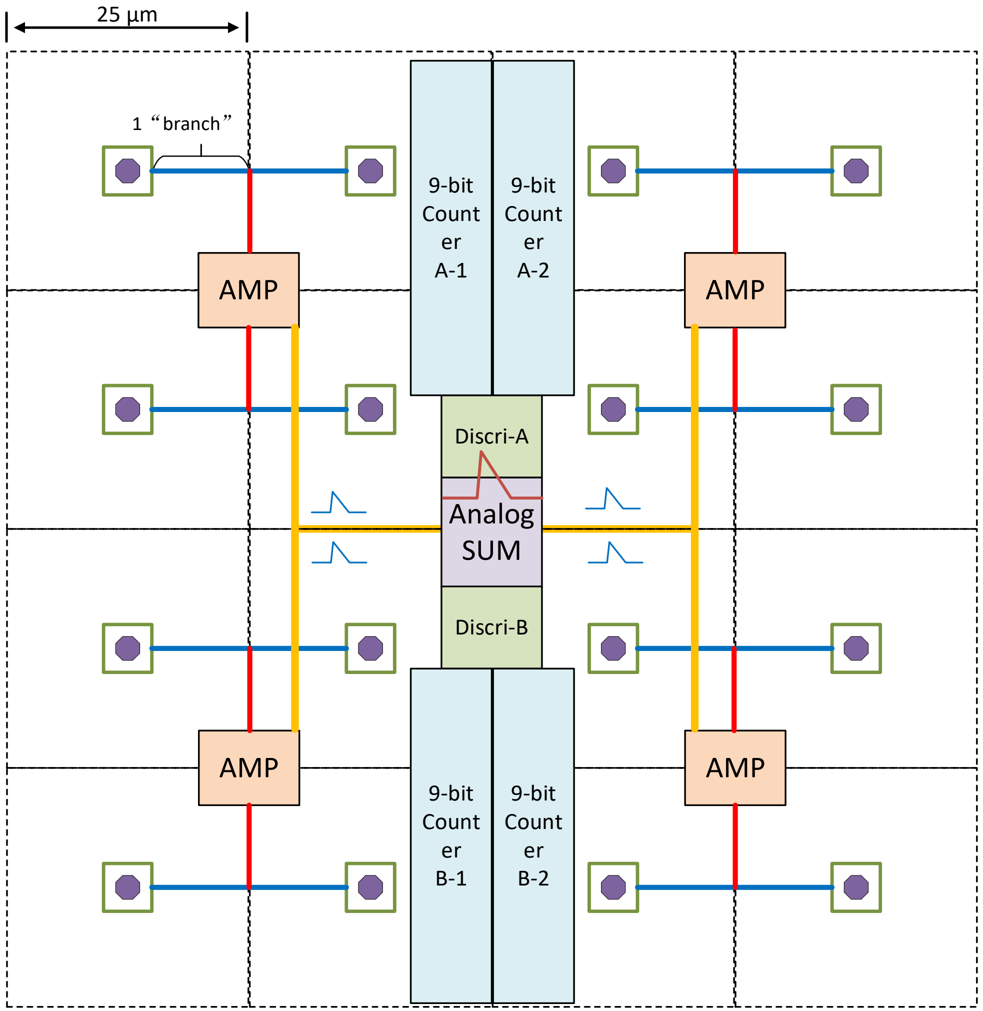
CIS Process Cross Section



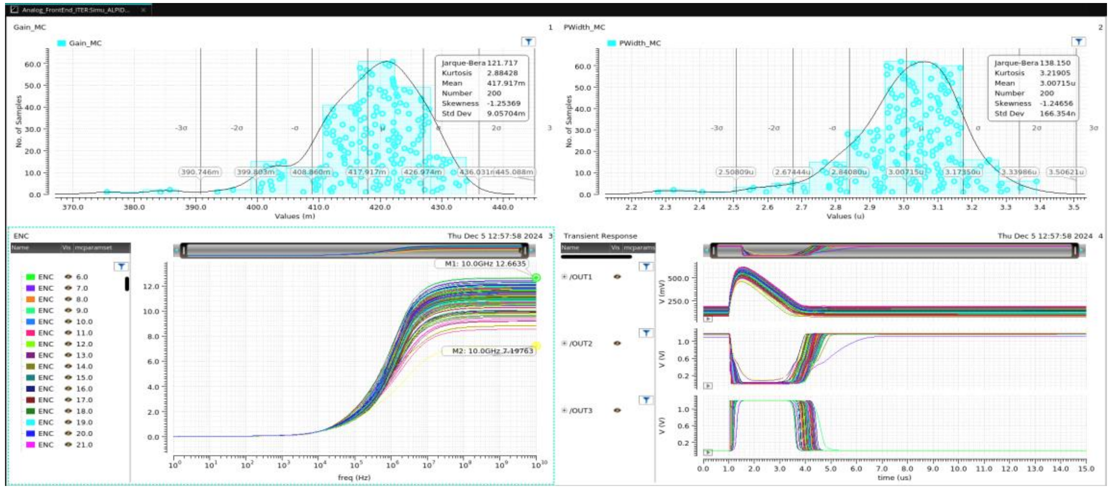
Pixels Scale Illustration

CSA + Analog Sum

- Classical CSA structure
  - 4 diodes/CSA， PEX and modeling of the input network
- Double threshold, de-offset discriminator
  - Depth of the counter: 9-bits (10-bits with ovf bit)
  - 4 counters/pixel
- Arriving time difference: 10 ns maximum
- Power Consumption： ~7.5 μW
- ENC: < 33 e-



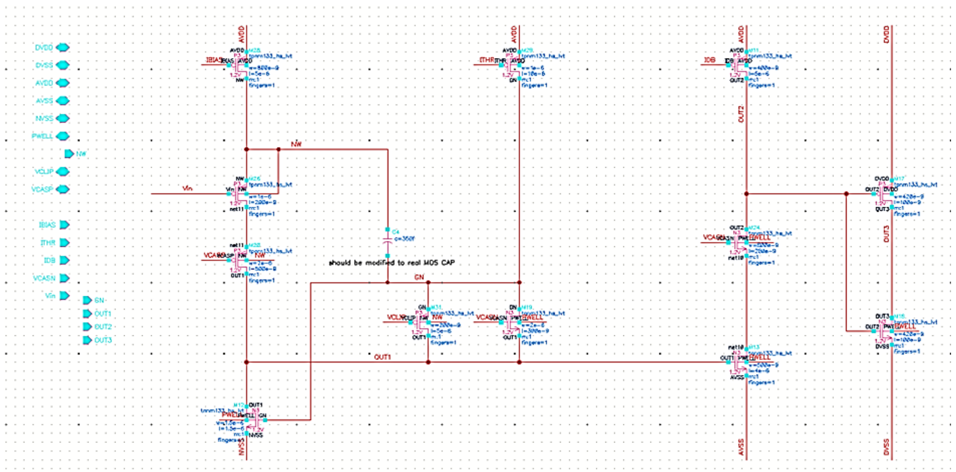
Analog Sum Scheme



Noise and Transient Simulations of 15 corners

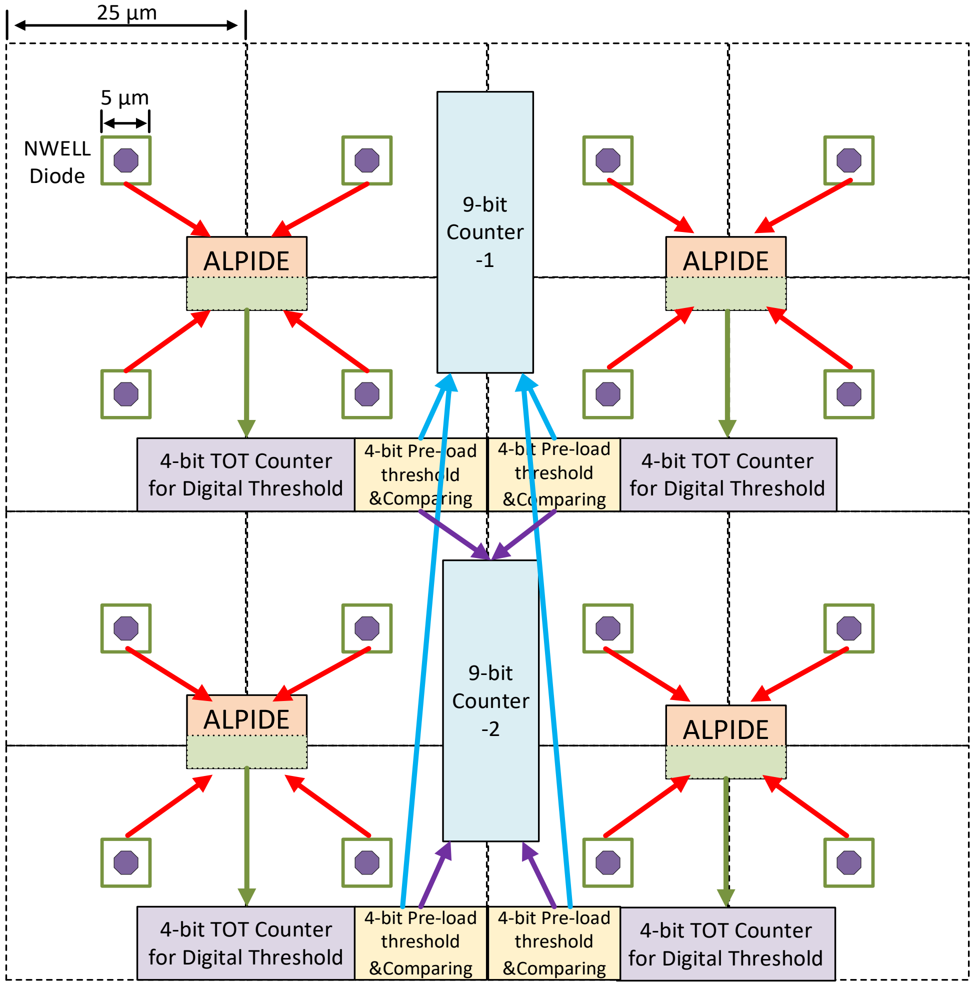
ALPIDE-like + Digital Sum

CNRS NUCLÉAIRE & PARTICULES | CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM | Institute of High Energy Physics, Chinese Academy of Sciences



ALPIDE-like Frontend

- Cannot take advantage of low C_{in} by adopting CSA
- ALPIDE-like front-end
  - Low noise, compact
- How to achieve double threshold?
  - Low threshold: ALPIDE charge threshold
  - High threshold: TOT （Digital threshold）
  - Set different threshold by different counting depth and clock frequency



Digital Sum Structure

ALPIDE-like + Digital Sum

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CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

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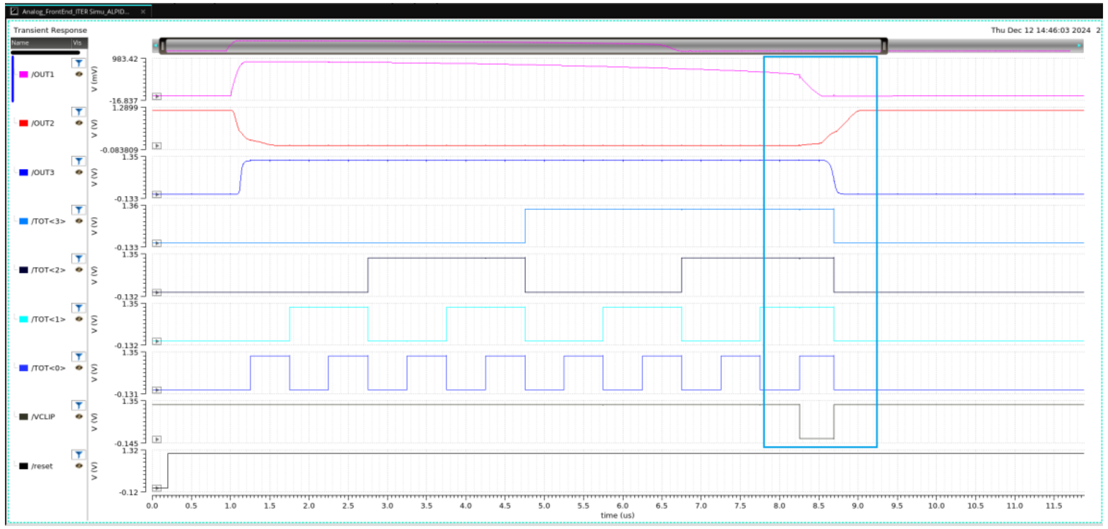
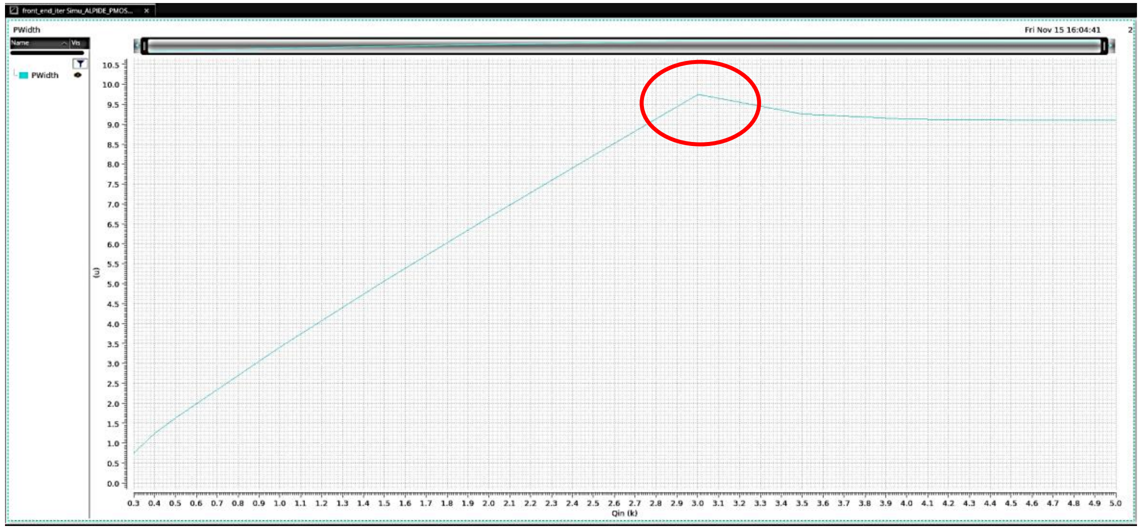
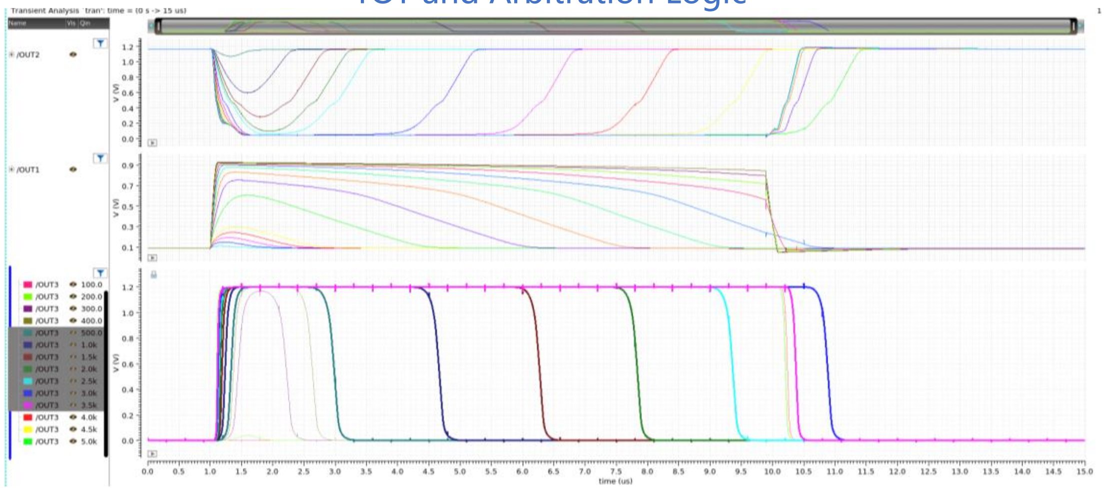


TOT and Arbitration Logic



Qin-TOT Linearity (300e-~5ke-)



Qin 800e-~3000e- Transient Simulation

SPEC	Mean	Standard Deviation
Charge Gain/ (mV/ke-)	417.9	9.057
Pulse width/us	3.007	0.166

- Power consumption: ~7 μW
- ENC Monte Carlo (Qin=800 e-):
  - maximum: 12.66 e-
  - minimum: 7.20 e-

Prospects-Next 5 years

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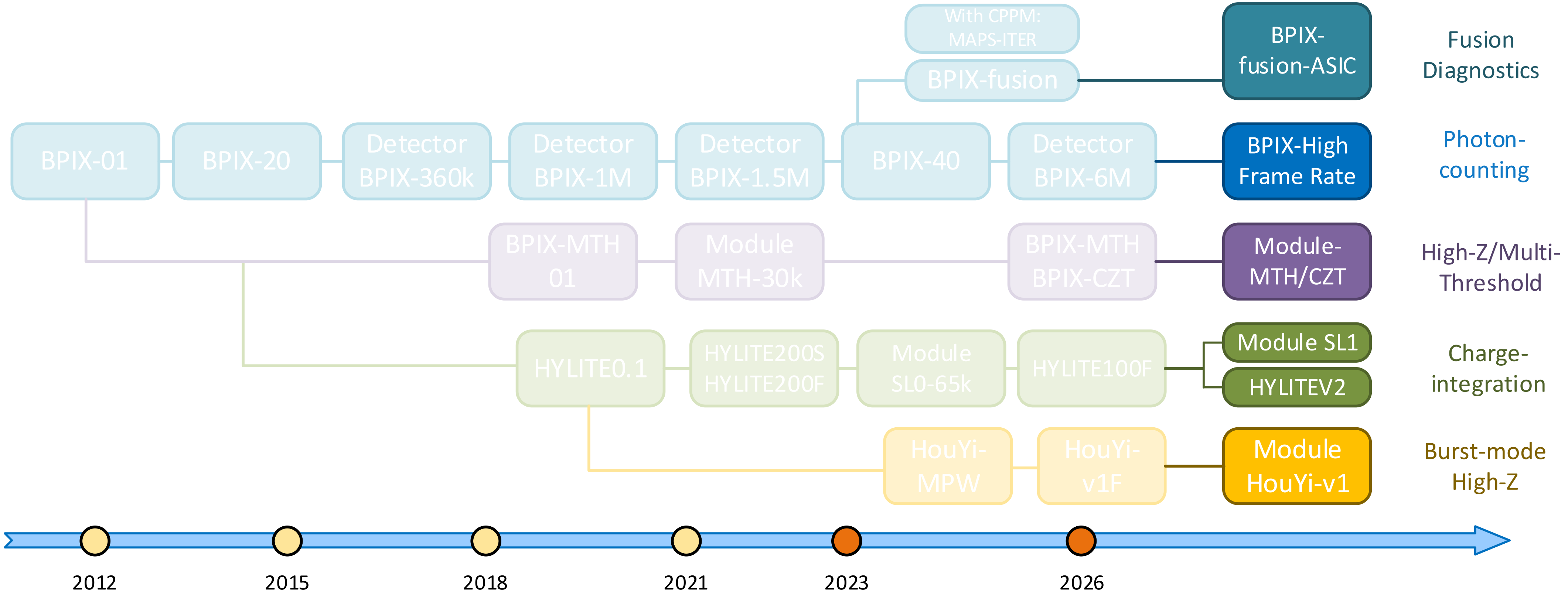


- Detectors of HEPS phase II and other new light sources in China: new ASIC design and system
- Fusion Facilities: ITER, BEST...

Our Team

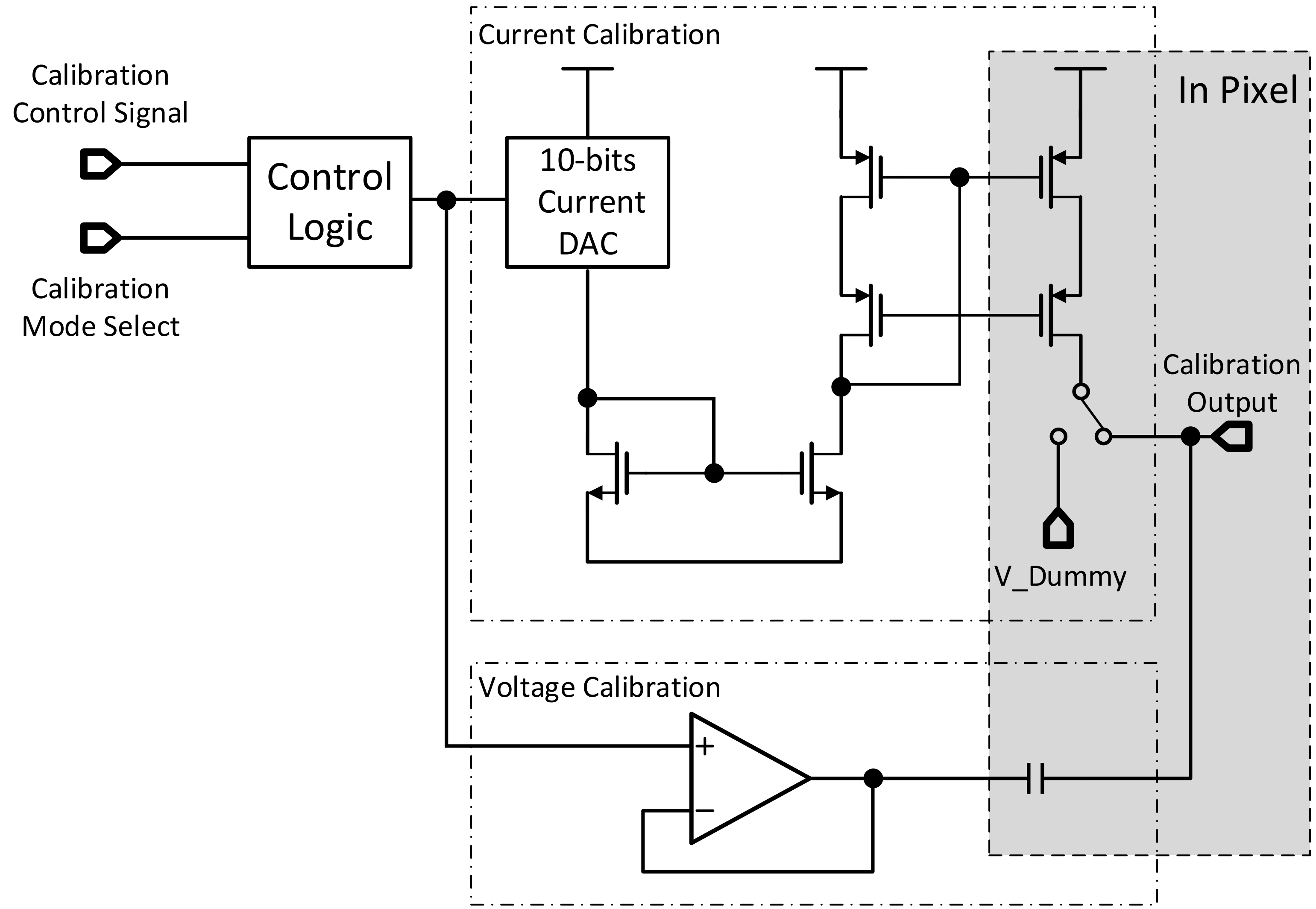
Institute of High Energy Physics
Chinese Academy of Sciences

- Thanks to our team members for their hard work:
  - Sensor and System Integration: Zhenjie Li, Yaoguang Liu
  - ASICs: Wei Wei, Mujin Li, Shanshan Cui (Postdoc), Chenzhuo Chang (Stu.)
  - Backend Electronics: Jie Zhang, Hangxu Li
  - DAQ: Xiaolu Ji, Xuanzheng Yang(Stu.)
  - Calibration: Yan Zhang, Xueke Ma
  - Mechanics： Zhe Li

Thanks!

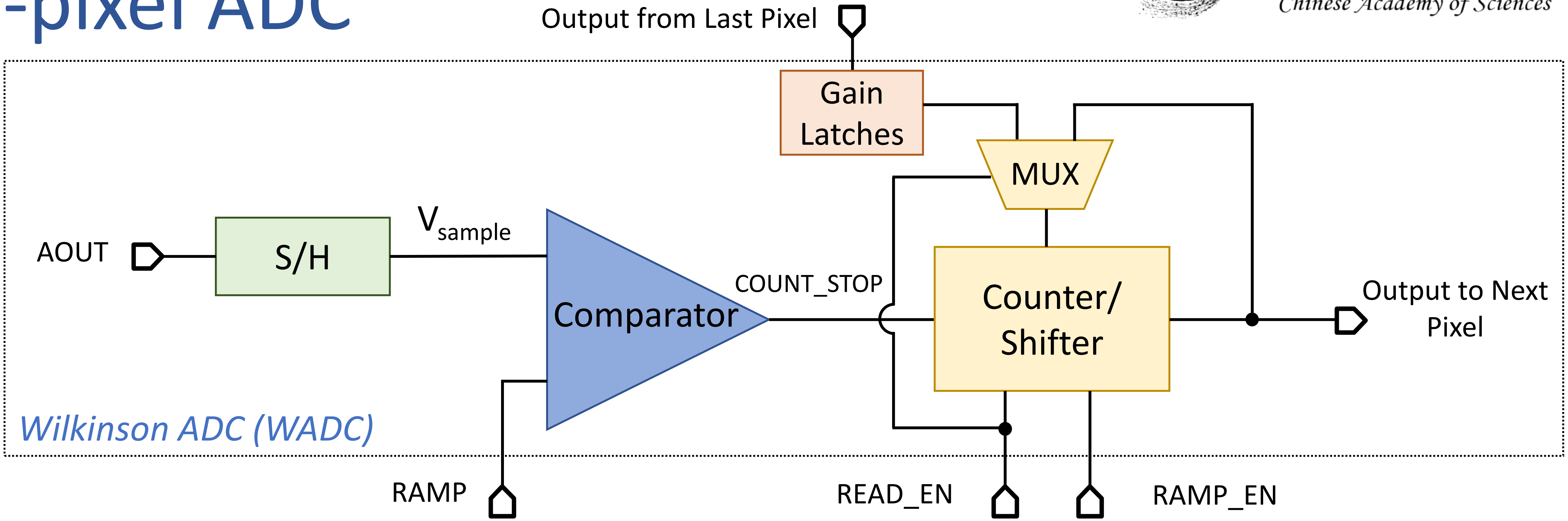
Back Up Slides

Calibration Block



- Covers Full Dynamic Range of 10000 photons @12 keV
- Voltage Mode
  - High Linearity
  - Small Input Range
  - 8 mV amplitude voltage pulse -> a 12 keV Photon ("equivalent photons" by calculating input charges)
- Current Mode
  - Large Input Range
  - Worse Linearity
  - DAC Code=1, 150 ns width digital pulse -> 10 12 keV Photons

In-pixel ADC



- S/H: Sample and Hold Circuit
- Comparator: Generates the stop signal of counting
- Counter/Shifter: Based on a 10-bit Linear Feedback Shift Register (LFSR)
- MUX: Switches modes between counting and shifting
- Gain Latches: 2-bits registers latches gain, located in gain-switching circuits
- Power Consumption: 7.5 µW

Module Mounting: preparation

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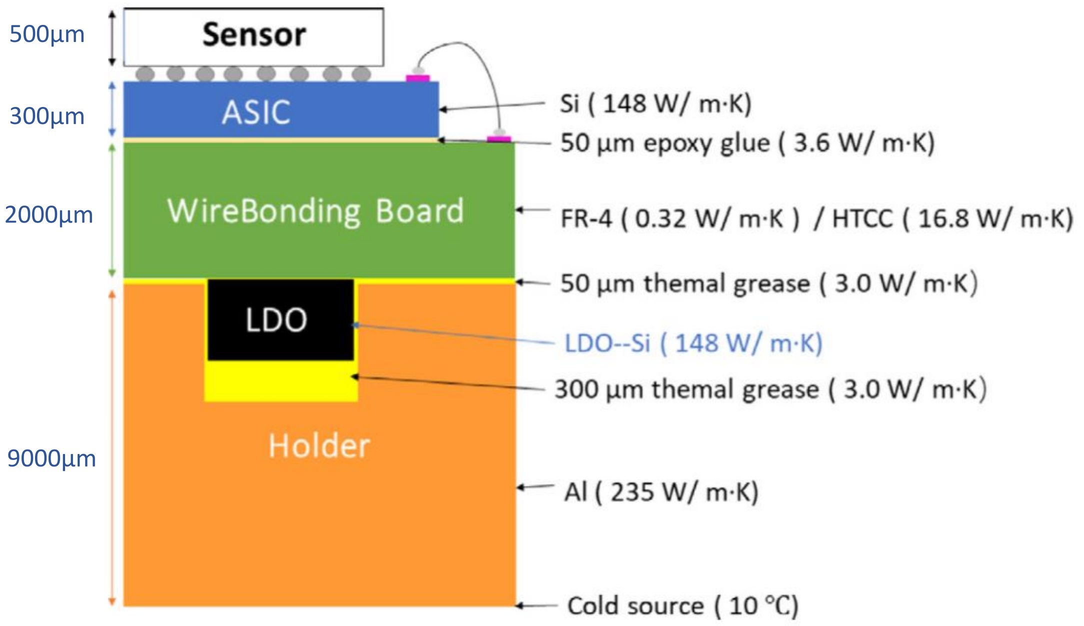
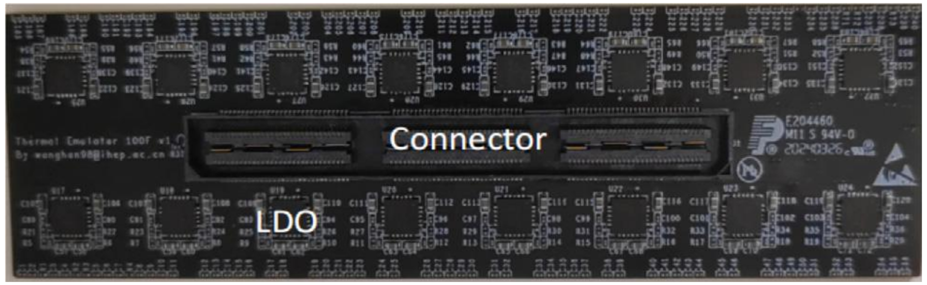
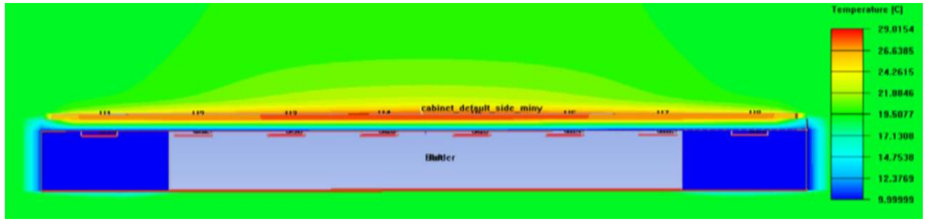


Module Structure and Corresponding Temp. Factors

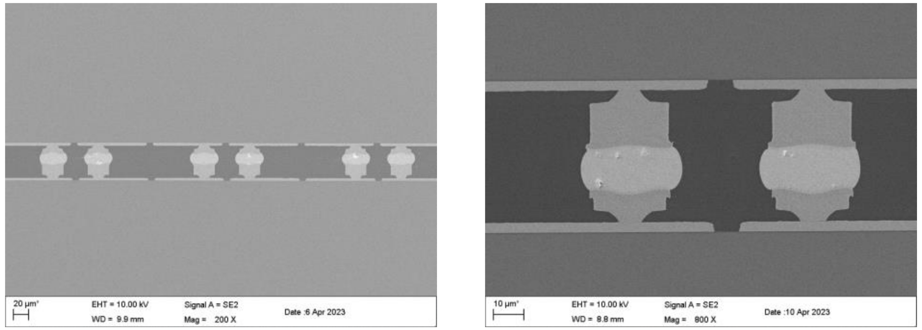


Wire-bonding board



Thermal simulation of the wire-bonding board

Bump Bonding Process Verification with Dummy Dies



Bump Quality Verification

Ref: doi:10.1016/j.nima.2024.169676

Module Mounting

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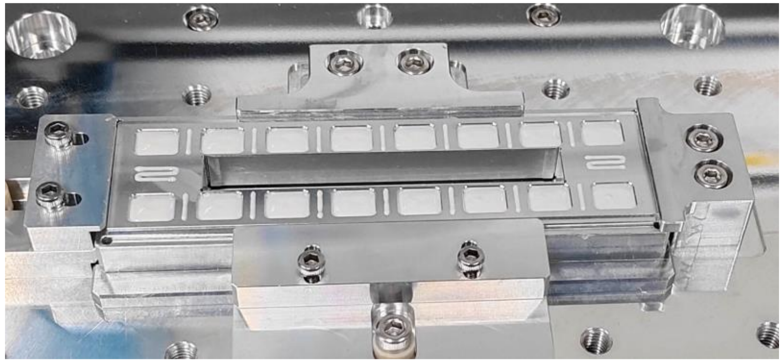
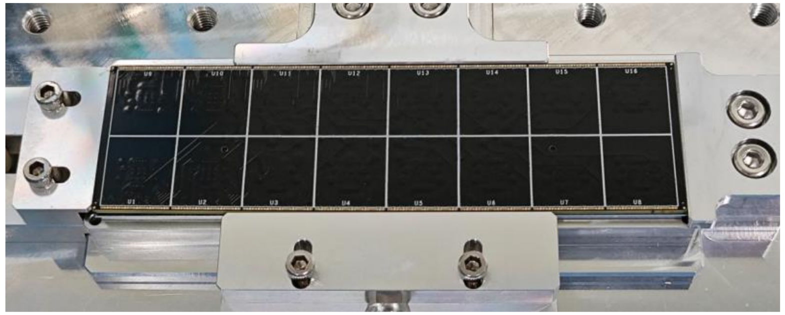
Dispense Glue on the Holder

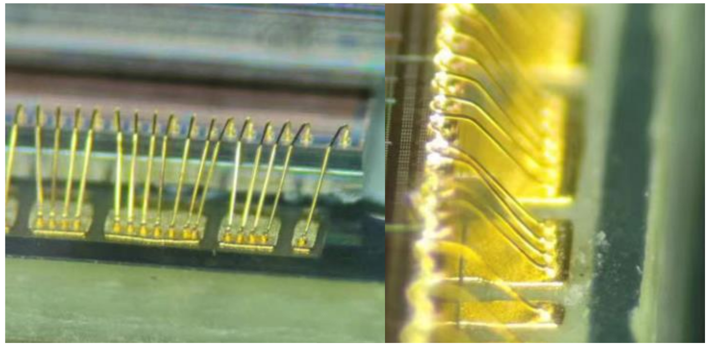


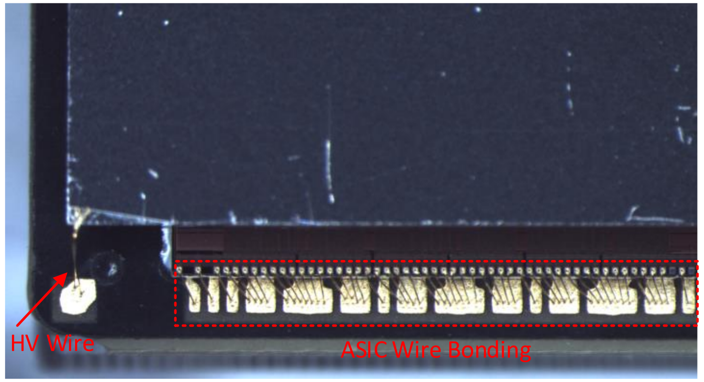
Bonding the Wire-Bonding Board and Holder



Dispense Glue on the Wire-Bonding Board

Mount the sensor and ASICs





Wire Bonding

CSA-Pixel Structure

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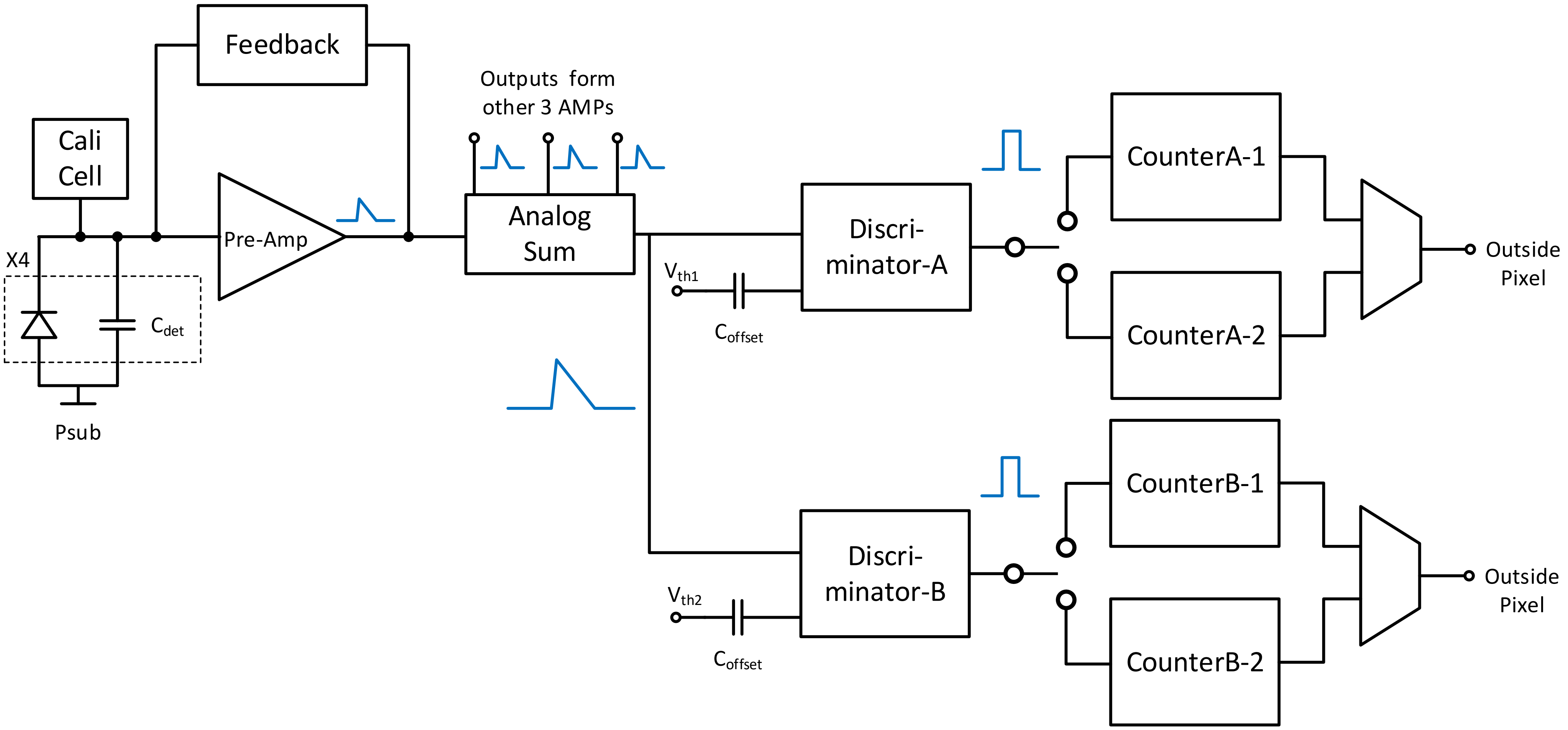

SHINE XFEL

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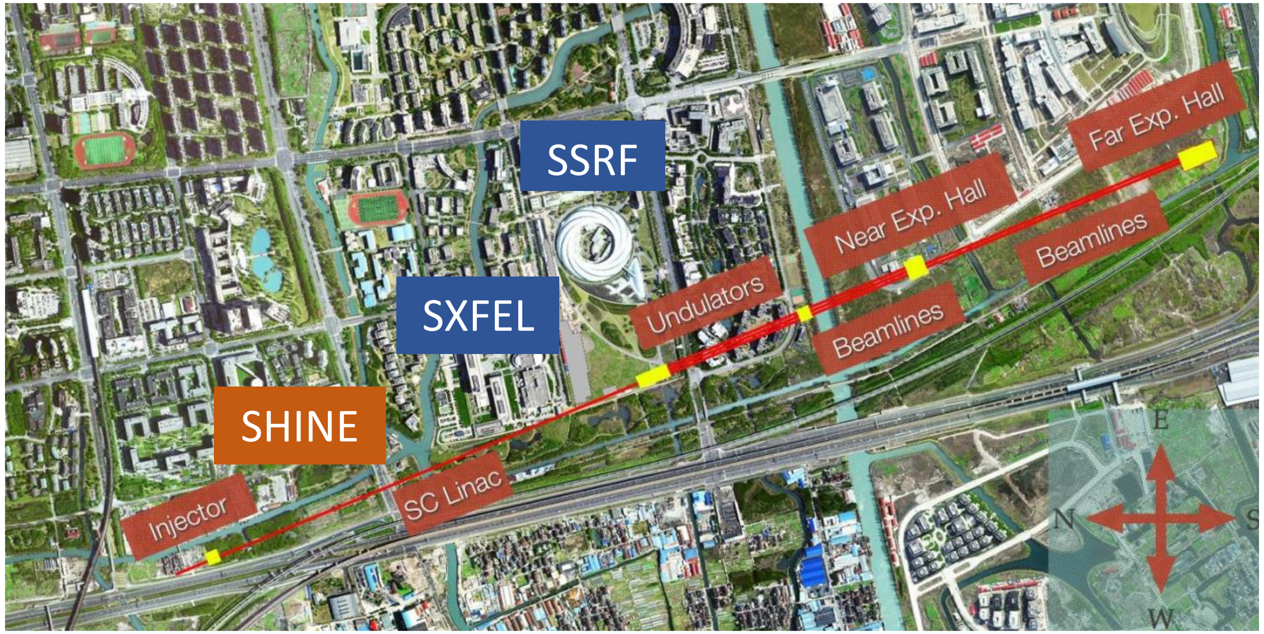
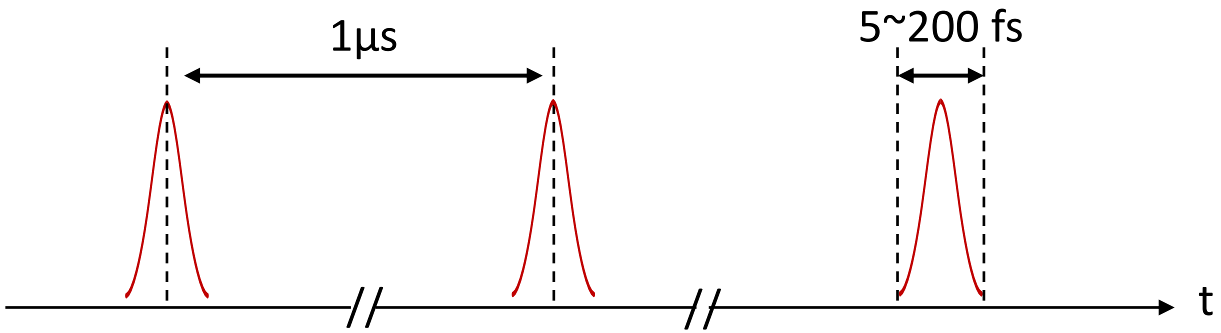
Shanghai HIgh repetitioN rate XFEL and Extreme light facility

- 3 FEL beamlines: FEL-I, FEL-II, FEL-III
- Photon Energy: 0.4~25 keV
  - FEL-I: 3~15 keV
  - FEL-II: 0.4~3 keV
  - FEL-III: 10~25 keV
- Pulse Duration: 20~50 fs (5~200 fs)
- Repetition Frequency: 10kHz (1MHz)
- Peak Brightness: 10^{32} ~10^{33} photons/μm^2/rad^2/s/0.1%BW





Typical Time Structure of the SHINE Photon Beam

Ref:doi:10.18429/JACoW-FEL2017-MOP055