RD53: CHALLENGES AND LESSONS LEARNED

Flavio Loddo - I.N.F.N. Bari

flavio.loddo@ba.infn.it

RD53 COLLABORATION

- **RD53 Collaboration** is a joint effort established in 2013 of ~24 ATLAS and CMS Institutes to develop readout chips for the HL-LHC pixel detectors

Initial mandate:

- Characterization of **65nm CMOS** technology in radiation environment (initially 500 Mrad, then 1 Grad)
- Design of a **rad-hard IP library** (Analog front-ends, DACs, ADCs, CDR/PLL, high-speed serializers, RX/TX, ShuntLDO, …)
- Design and characterization of a pixel chip demonstrator: **RD53A**
  - half-size (reticle shared with other ASICs): 440 columns x 192 rows
  - 50 x 50 μm^2 pixels
  - design variations (3 Analog Front-Ends, 2 pixel readout architectures)
  - architecture designed to be easily scalable to a full scale chip
  - extensively used to characterize sensors
  - thorough Analog FE characterization and review
- RD53A was successful and the feasibility of pixel chips for HL-LHC in the chosen technology was demonstrated

2018: Mandate extended to design the full-scale chips for the two experiments

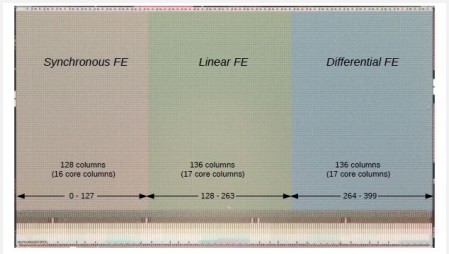
- Due to different mechanical constraints, ATLAS and CMS required the two ASICs to have different size

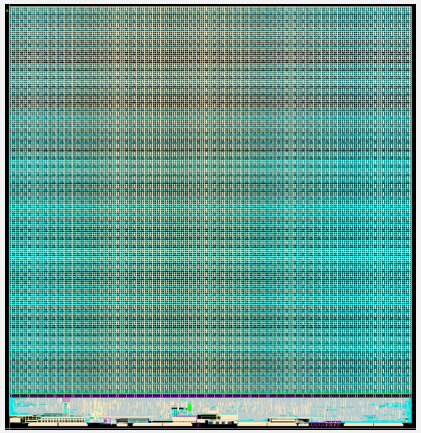
ATLAS and CMS chips are two instances of the same common design, having different size and Analog Front-End, according to specific requirements of the experiments

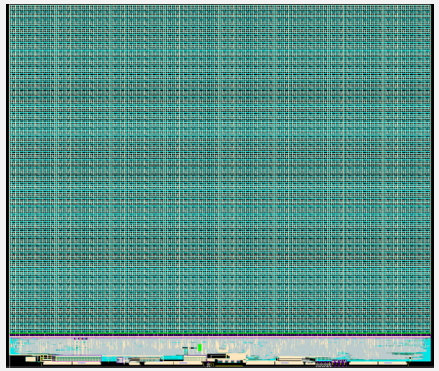
DESIGN REQUIREMENTS

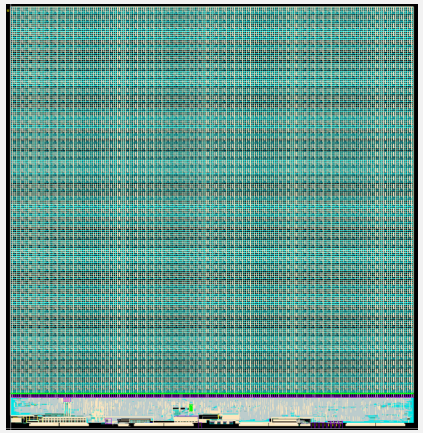
Parameter	Value (ATLAS / CMS)
Technology	65 nm CMOS
Max. hit rate	**3.5 GHz/cm²** ←
Trigger rate	**1 MHz / 750 kHz** ←
Trigger latency	**12.5 µs** ←
Pixel size (chip)	**50 x 50 µm²**
Pixel size (sensor)	50 x 50 µm² or 25 x 100 µm²
Pixel array	400 x 384 pixels / 432 x 336 pixels
Chip dimensions	20 x 21 mm² / 21.6 x 18.6 mm²
Detector capacitance	< 100 fF (200fF for edge pixels)
Detector leakage	< 10 nA (20nA for edge pixels)
Min. threshold	**< 1000 e-**
Noise	< 150 e- RMS with sensor
Charge measurement	4-bit ToT
Dead time	< 1% at 3.0 GHz/cm2
Radiation tolerance	**1 Grad** over 10 years at -15°C ←
SEE tolerance	**SEU rate, innermost: ~100Hz/chip** ←
Power	**< 1W/cm², Serial powering** ←
Readout data rate	1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s
Temperature range	-40°C ÷ 40°C

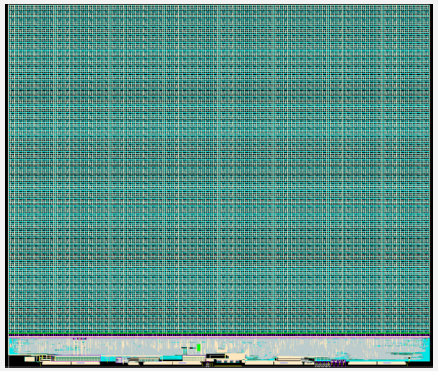
RD53 TIMELINE











RD53A
(2017)

RD53B-ATLAS (ItkPix1)
(March 2020)

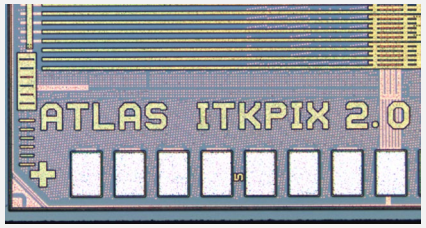
1.1

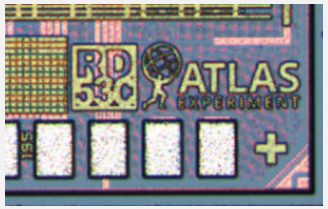
RD53B-CMS (CROCv1)
(June 2021)

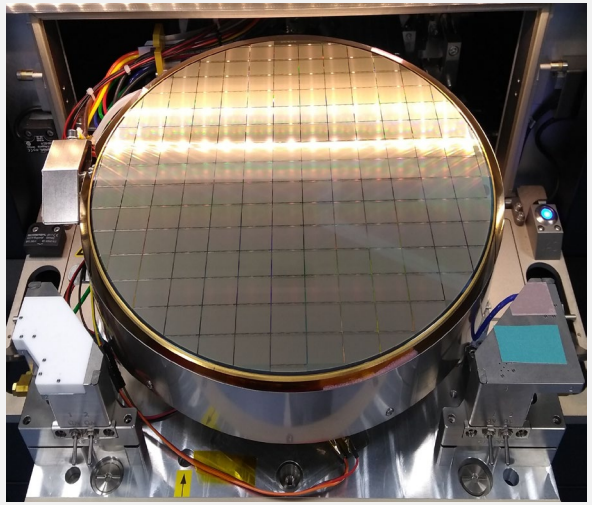
RD53C-ATLAS (ItkPix2)
(March 2023)

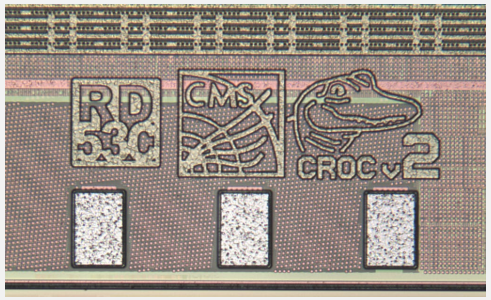
RD53C-CMS (CROCv2)
(Sept. 2023)

The mass production is complete and tested in various sites using custom Wafer Probing setups









❑ **ATLAS ItkPixv2** → 700 wafers

❑ **CMS CROCv2** → 345 wafers

A QUICK OVERVIEW

- **RD53 ASICs are large and complex pixel readout chips for the HL-LHC pixel detectors embedding:**
  - Power regulation to use the innovative Serial Powering technique
  - Signal amplification and discrimination
  - Data compression and Event building
  - Capability of data aggregation from other chips for cable reduction
  - Very large number of Mixed/Signal IPs, all developed inside RD53 (PLL, DACs, ADC, Temp. and Rad. sensors, …)
  - Minimal I/O interface

- The design represented a **challenge** in terms of:
  - **Implementation**
    - Power distribution
    - Long trigger latency (12.5 µs) combined with high hit rate (3.5 GHz/cm^2) → In-pixel buffering
    - Complexity of implemented features
    - Unprecedented radiation hardness (proven to work reliably even more than 1 Grad)
    - SEE tolerance with fast recovery capability
    - Timing closure
  - **Verification**: Verification effort spanned over 7 years, involved 10 people, used 2 different frameworks
  - **Human resource management**: large collaborative ASIC (> 30 designers)

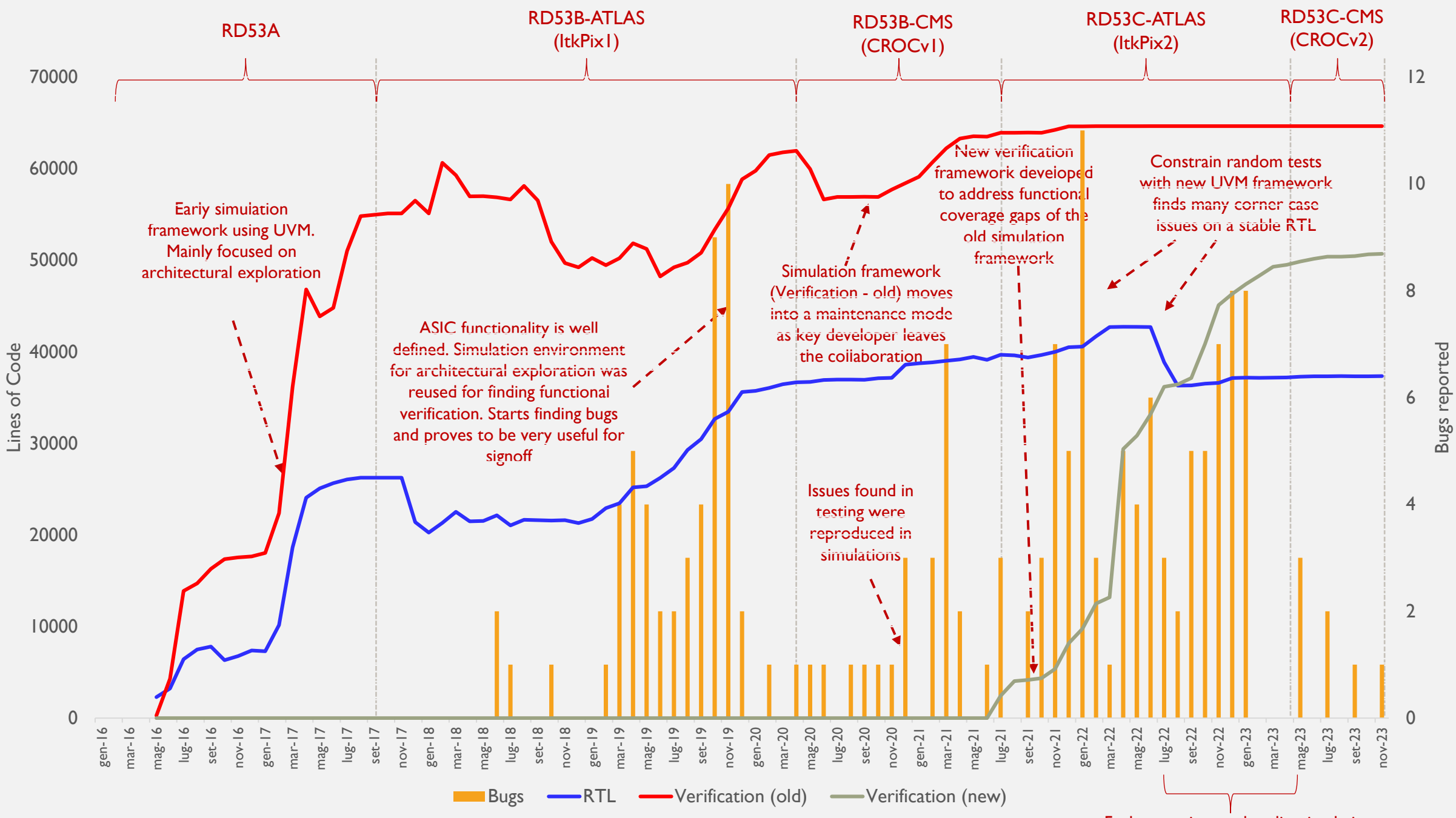
RD53 VERIFICATION FRAMEWORK

- **RD53 verification framework**
  - verify that chip outputs match outputs predicted by the framework, for randomised configurations and inputs
  - **U**niversal **V**erification **M**ethodology (IEEE Std. 1800.2-2020)
  - Industry standard, well-supported by tool vendors

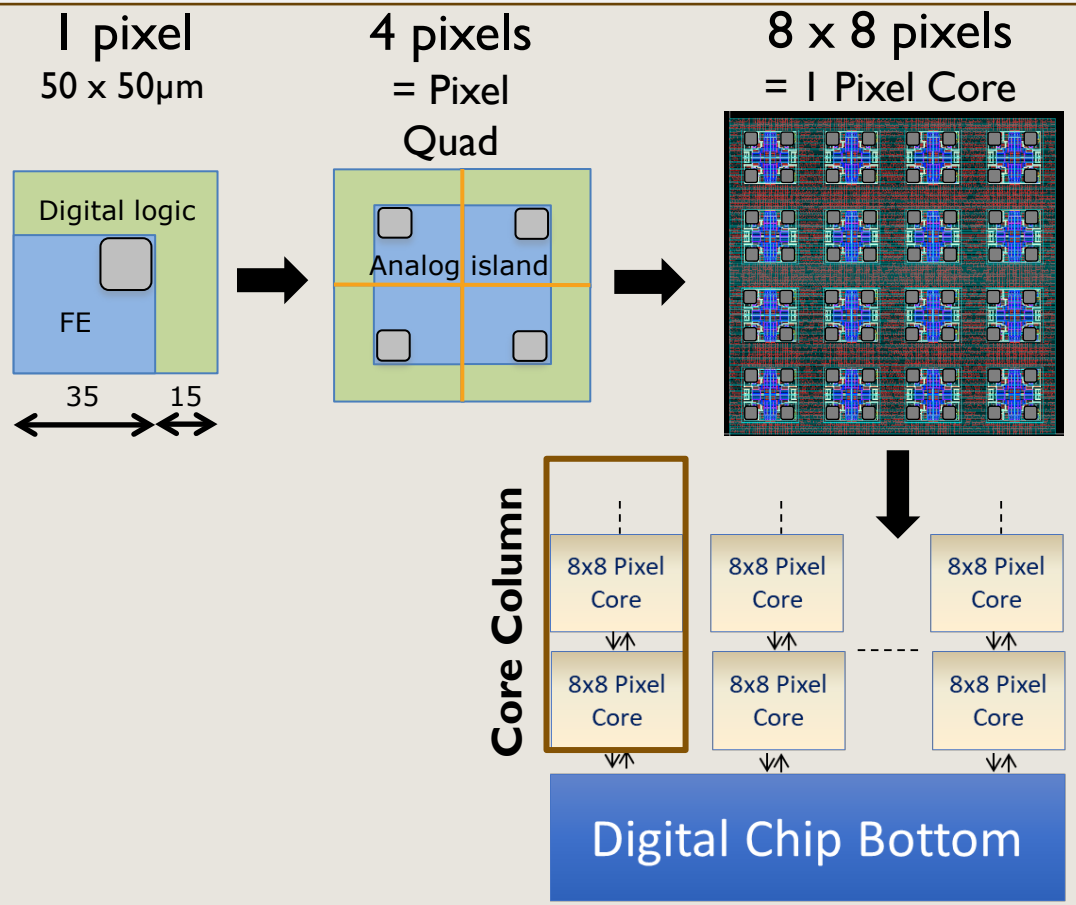
- **Metric-driven verification: simulate until the desired coverage is reached (goal is 100%)**
  - **Functional coverage**: have I exercised the DUT with all interesting inputs?
  - **Code coverage**: have I exercised all lines of code? Have I used all possible branches? Have I toggled all the signals?

- Initial framework version used for architecture studies and RD53A-RD53B verification
- Improved version implemented for final functional and SEE verification of RD53C production chips

- Use **constrained randomization** to test all feasible combinations of configuration and inputs plus some directed tests for specific block verification
- Regressions with **> 1700 tests** to reach coverage goals
- **Also used for SEE injection simulations, although only in the very last few months due to lack of manpower with expertise**

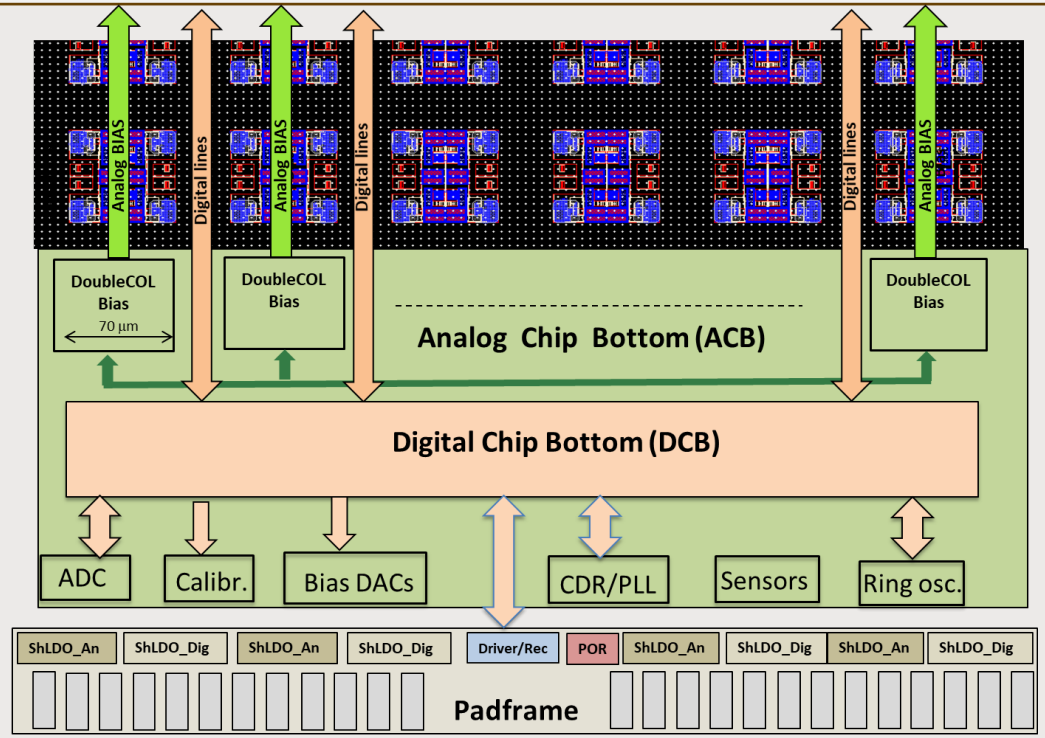

RD53A
RD53B-ATLAS (ItkPix1)
RD53B-CMS (CROCv1)
RD53C-ATLAS (ItkPix2)
RD53C-CMS (CROCv2)
Early simulation framework using UVM. Mainly focused on architectural exploration
ASIC functionality is well defined. Simulation environment for architectural exploration was reused for finding functionai verification. Starts finding bugs and proves to be very useful for signoff
Simulation framework (Verification - old) moves into a maintenance mode as key developer leaves the collaboration
New verification framework developed to address functional coverage gaps of the old simulation framework
Constrain random tests with new UVM framework finds many corner case issues on a stable RTL
Issues found in testing were reproduced in simulations
Lines of Code
Bugs reported
Bugs
RTL
Verification (old)
Verification (new)
Fault campaigns and netlist simulations

FLOORPLAN



Pixel array

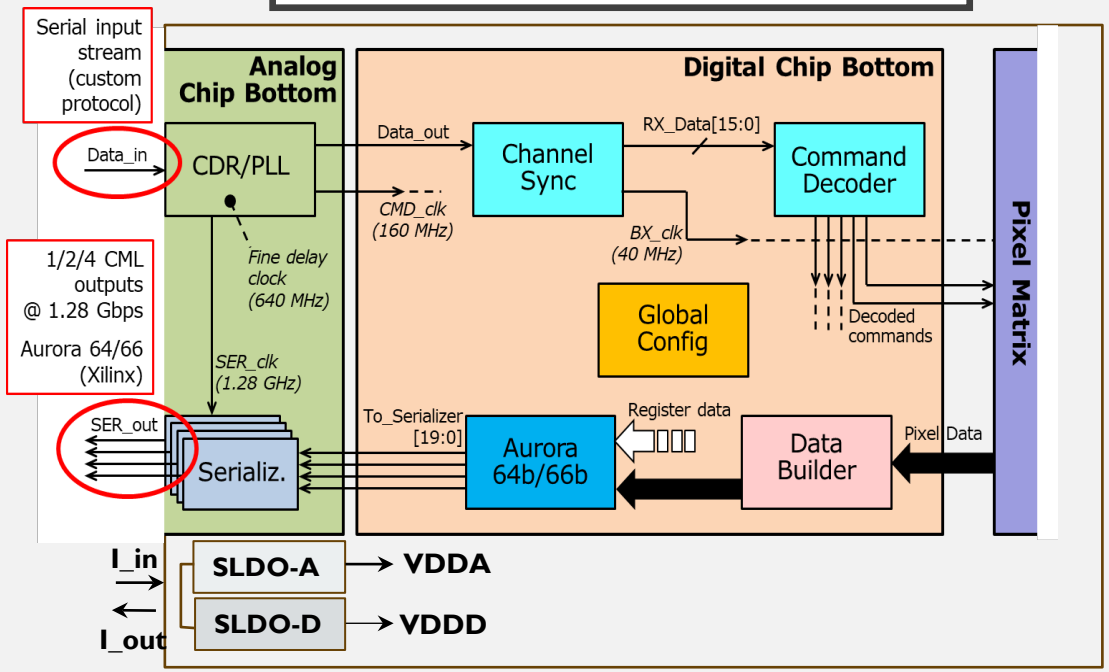
- Digital logic synthesized for 8 x 8 pixels to form a **Pixel Core**
- All Cores are identical → efficient hierarchical implementation and verification
- **The number of Cores is a parameter of the common RTL netlist**



Chip periphery

- **Analog Chip Bottom (ACB)**: contains all analog and mixed/signals building block for Calibration, Bias, Monitoring and Clock/Data recovery
- **Digital Chip Bottom (DCB):** synthesized logic for communication to/from chip, readout and configuration
- **Padframe (common to ATLAS/CMS)**: complex macro containing all I/O blocks with ESD protections and distributed ShuntLDO regulator for serial powering

I/O INTERFACE



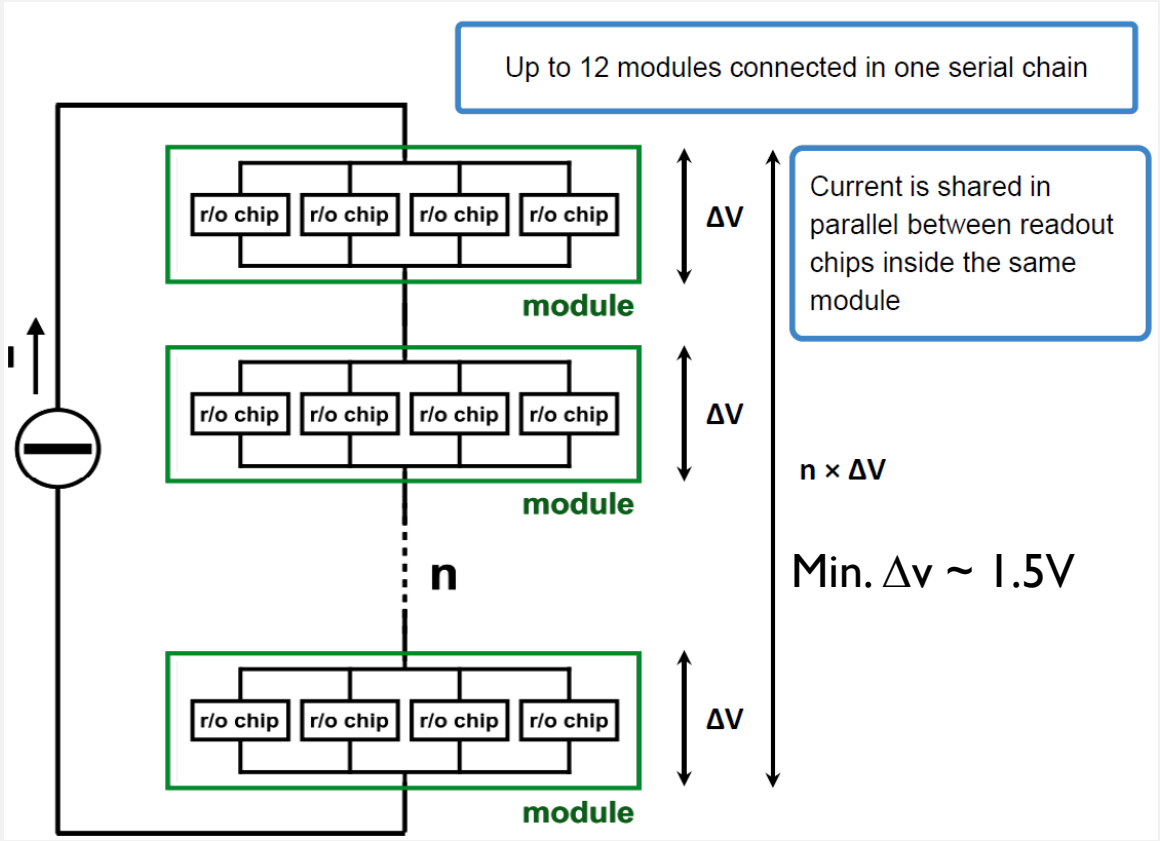
Extremely complex pixel readout ASIC designed to have a minimal I/O interface:

- **Input: command, control and timing**
  - **One single 160 Mb/s differential serial link**, driving up to 15 chips (4 bit addressing + broadcast)
  - Custom protocol, implementing deadtime-less communication for continuous reconfiguration
  - CDR/PLL recovers Data and Clock
- **Output:**
  - **Up to 4 x 1.28 Gb/s CML serial links** for data readout (hit data + service data) compatible with LpGBT and using Aurora 64b/66b encoding
- **Power:**
  - Input/output currents for **serial powering**

POWER STRATEGY AND DISTRIBUTION

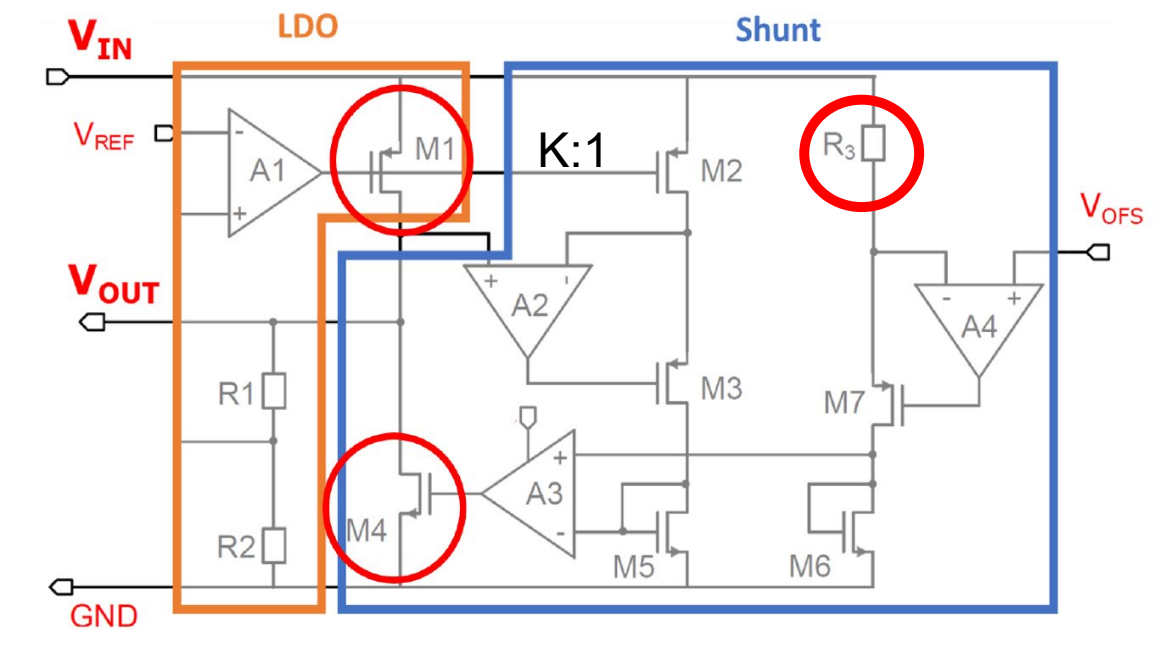
SERIAL POWERING

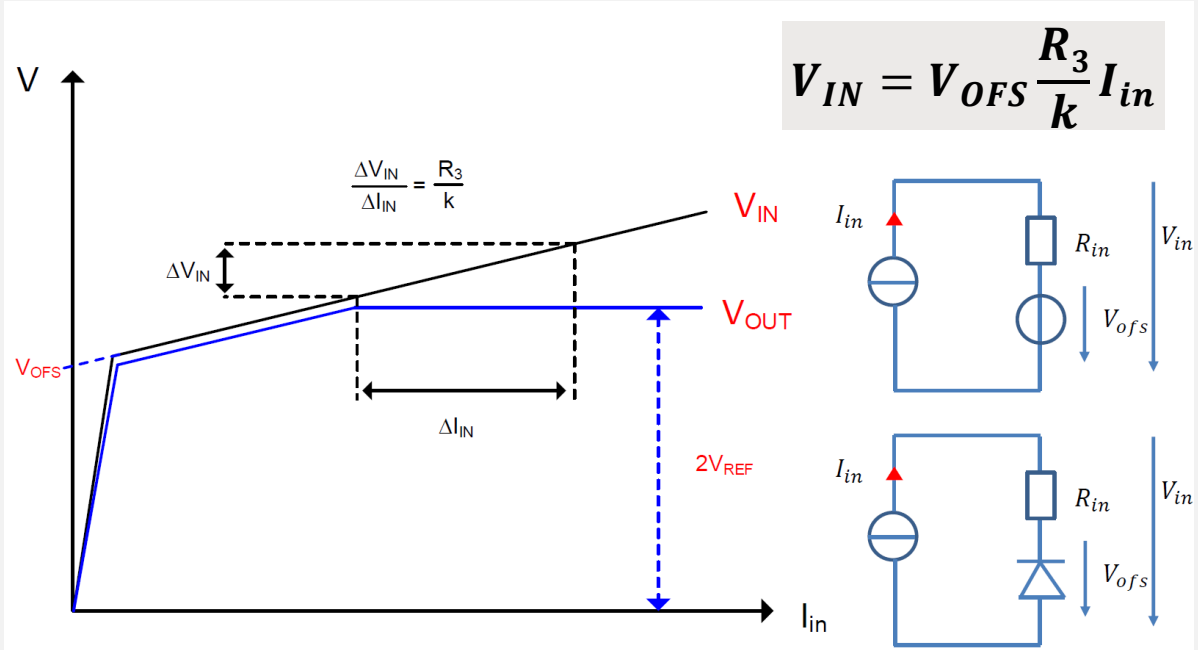
- ATLAS and CMS will adopt the innovative **serial-powering scheme** for pixel modules
  - modules are connected in **serial chain**: “recycle” current from one module to another
  - chips on the same module (up to 4) connected in parallel
  - based on the ShuntLDO (SLDO) regulators integrated in the RD53 chip
  - 1 SLDO for the analog domain, 1 SLDO for the digital domain operating in parallel in each chip



- Not sensitive to voltage drops
- Low mass & compact power routing
- On-chip regulated supply voltages, low noise
- Radiation hardness (1 Grad)
- Only ROCs on the modules

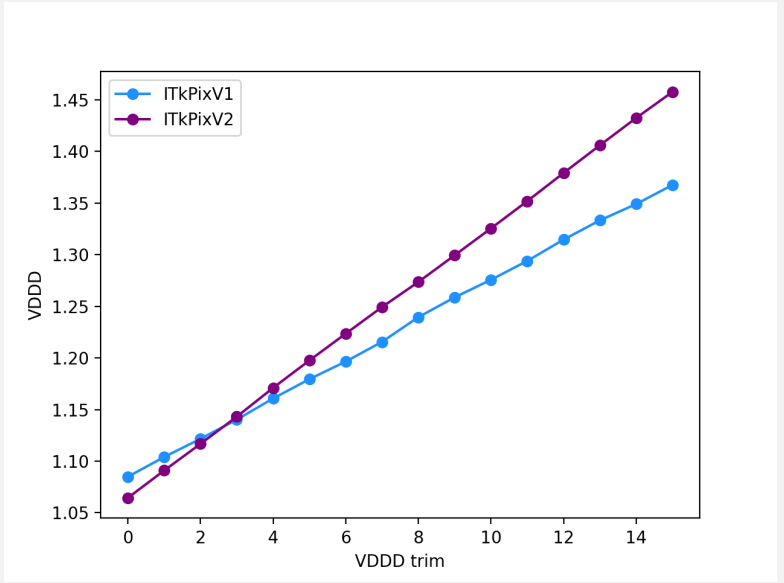
SLDO FOR SERIAL POWERING





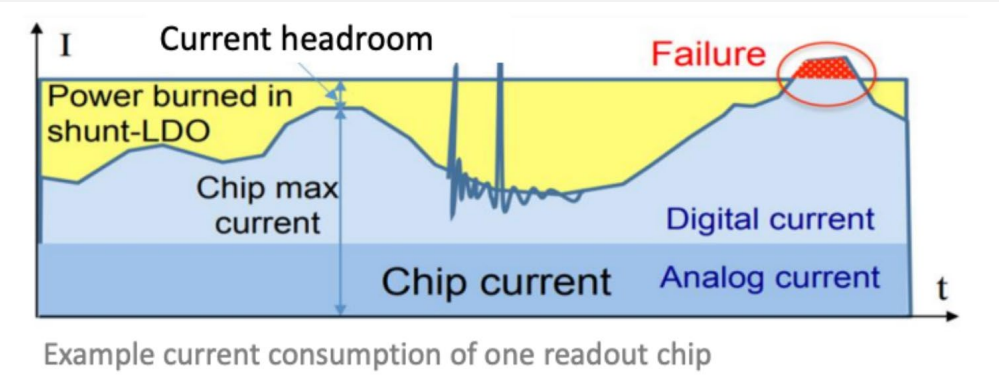
$$V_{IN} = V_{OFS}\frac{R_3}{k}I_{in}$$

- V/I curve parameters (Voffset, slope) and current sharing defined by **external resistors** (no SEU)
- V_{OUT} tunable by chip configuration (1.05V ÷1.4V, 4 bits)

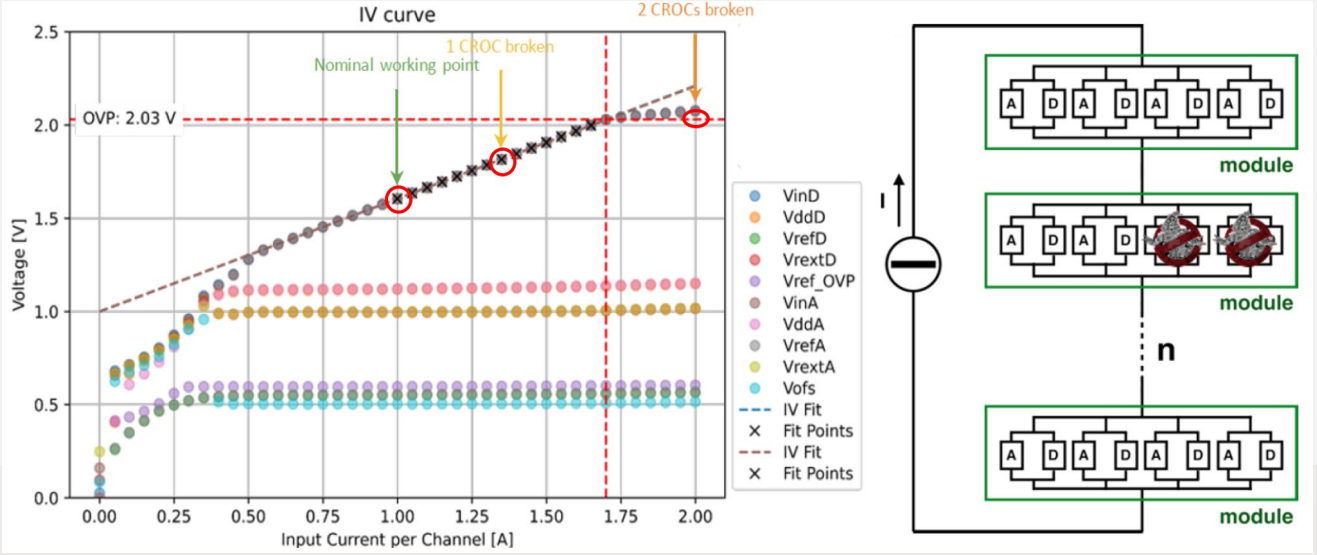


SLDO FOR SERIAL POWERING

- **Input current** dimensioned to satisfy the highest load, with ~15-20% headroom for stable operation to be absorbed by the Shunt device
- In case of chip failure, its current must be absorbed by the other chips (shunts) of the module: the SLDO shunt current capability is designed to be up to 200% of normal operation current to assure, in case of 1-2 chip power failures on a module, that remaining chip(s) can correctly pass the serial chain current
  - I_{IN} increases → V_{IN} increases → Need protection mechanisms
  - The excess current is absorbed by the shunt devices → **hot spots**



Example current consumption of one readout chip

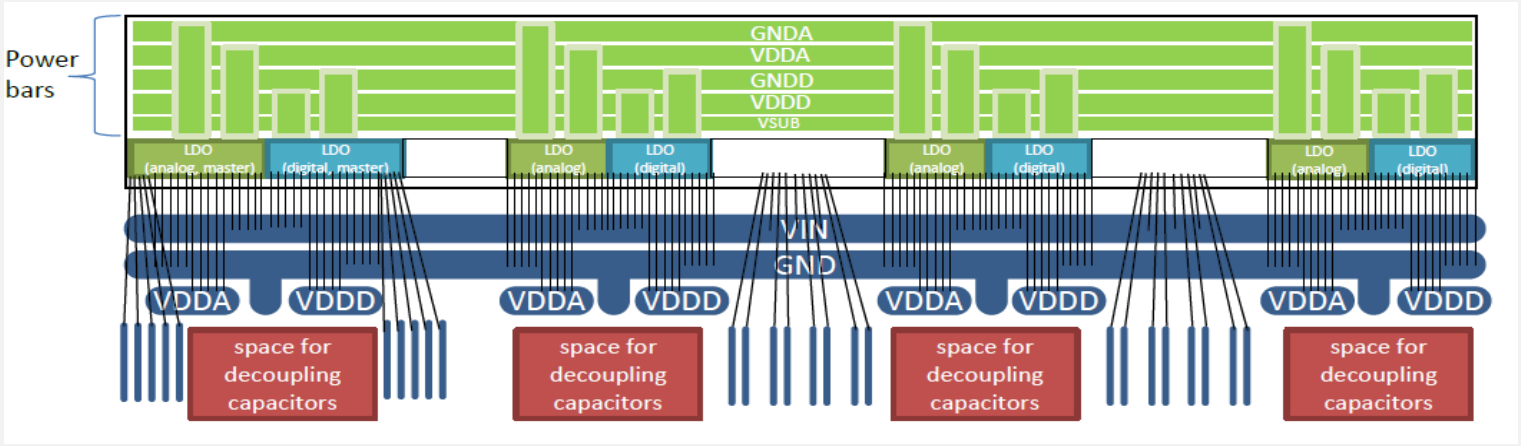


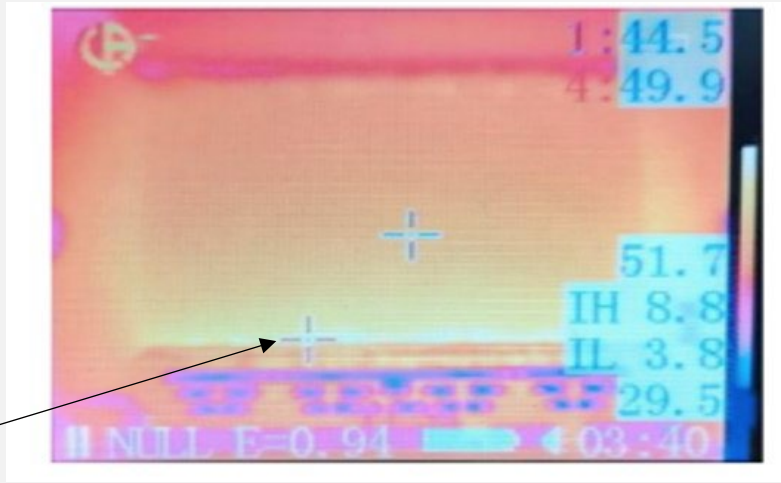
Protections:

- *Over-voltage protection*: **V_{IN} clamped to 2 V**
- *Overload (under-shunt) protection*: V_{OUT} decreased in case shunt current goes below a certain threshold (~11 mA) due to excess load current. Disabled by default, can be enabled by chip configuration

POWER DOMAINS AND ISOLATION METHODOLOGY

- ShuntLDOs are located in the Padframe and distributed along the full chip width (~ 20 mm)
- Two power domains → two ShuntLDOs
- 4 blocks with sets of 5 Wire Bonds per power net





- Hot spots in the shunt devices, **to be properly cooled**
- Temperature sensors located near the Analog and Digital ShuntLDOs

- Analog and digital circuitry in separated deep N-wells for maximum possible substrate isolation
- Throughout the chip no active device on the global p-substrate
- Global p-substrate biased by VSUB
- GNDA-GNDD-VSUB connected off-chip

SUPPLY AND GROUND VARIATIONS

Due to limited routing resources and the constraints given by the ShLDO location, RD53 chips show analog and digital supply and ground variations both between columns and along them

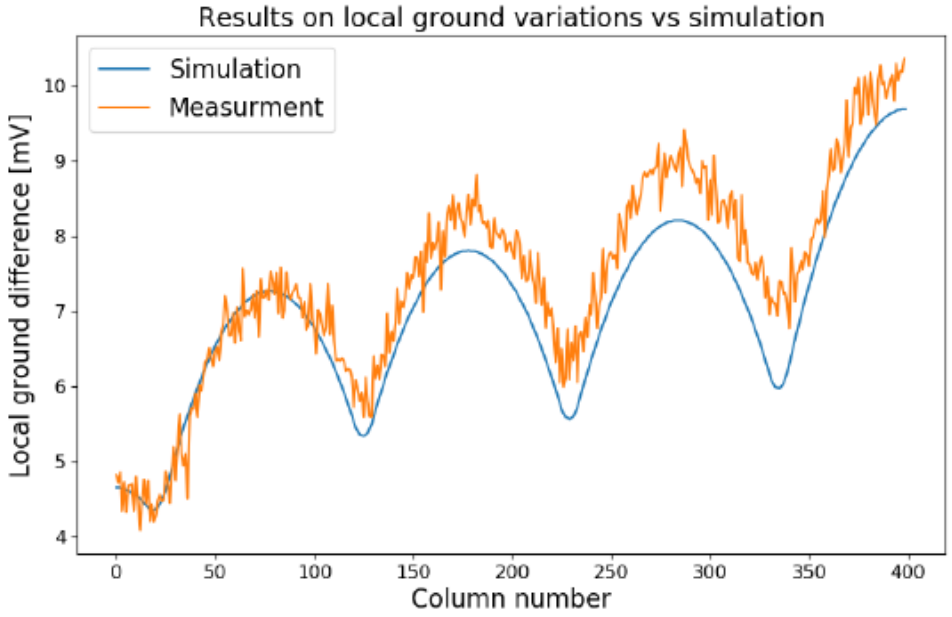
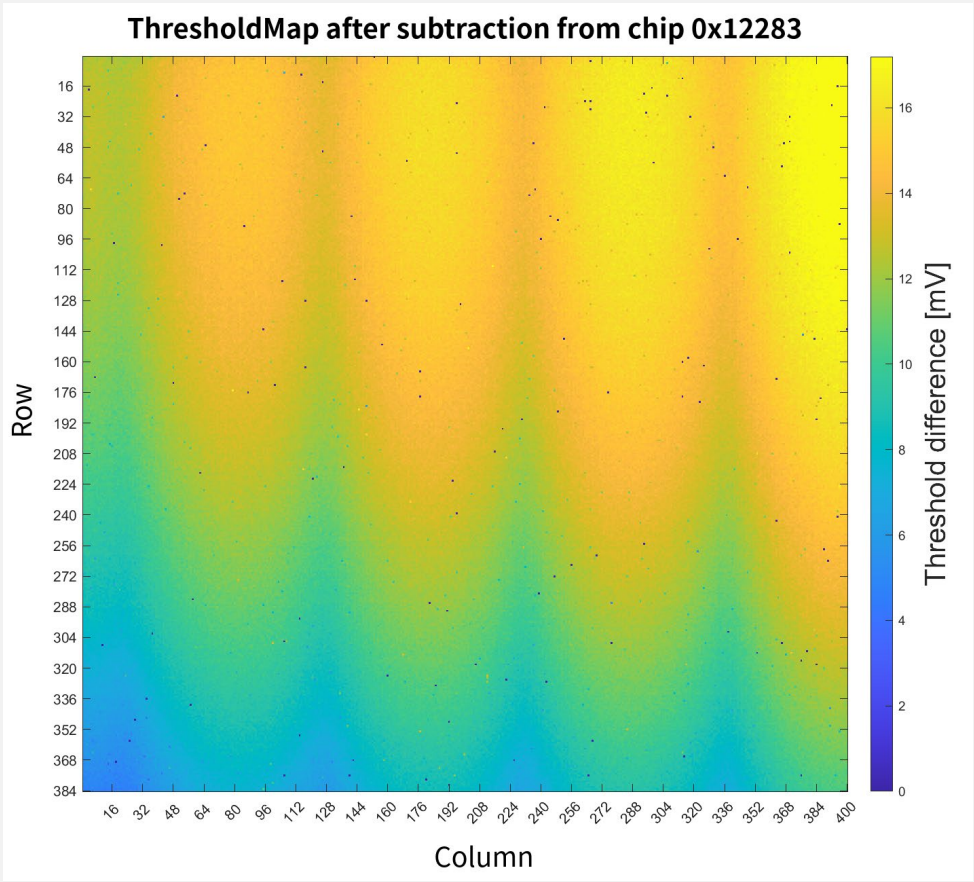


Figure 3.25: Local ground variations from measurements and simulations are shown as a function of column number for row 384 of the RD53B chip, measured in millivolts (mV). The measured data is shown in orange, while the simulated results are in blue.



- The range of threshold tuning is capable to compensate the feature and achieve excellent threshold dispersion (~50e-)
- Full chip digital power analysis (static + dynamic) not feasible due to memory limitation (>> 512 GB required): executed on 1 core-column + periphery: max DVDD+DVSS dynamic IR drop ~ 110 mV

LESSON LEARNED ON POWER MANAGEMENT

- Power Management represents a crucial aspect of High-Energy Physics apparatuses from multiple points of view:
  - Reliability
  - Radiation hardness
  - Material budget
  - Cooling
  - Power distribution
  - …

- **The system-level validation of a serially powered system is even more critical than the single chip testing**:
  - Proper evaluation of ShLDO parameters (Voffset and Slope) for an efficient current sharing → BOM of modules
  - Definition of current headroom, to absorb load current variations without an excessive shunt current
  - Assessment of start-up reliability of serial chains, especially at cold (-40ºC)
  - Stress tests to validate the protections
    - As an example, during the wafer test of CMS chips we provided up to 4x the maximum expected current (8A instead of < 2A)
    - Emulate the failure of 1-2 chip of a module (by removing wirebonds)

- Serial Powering is an uncommon approach but demonstrated to be feasible. ATLAS and CMS pixel detectors for HL-LHC are the first large systems to adopt it. Under evaluation for other large sub-systems (ALICE3, LHCb U2)

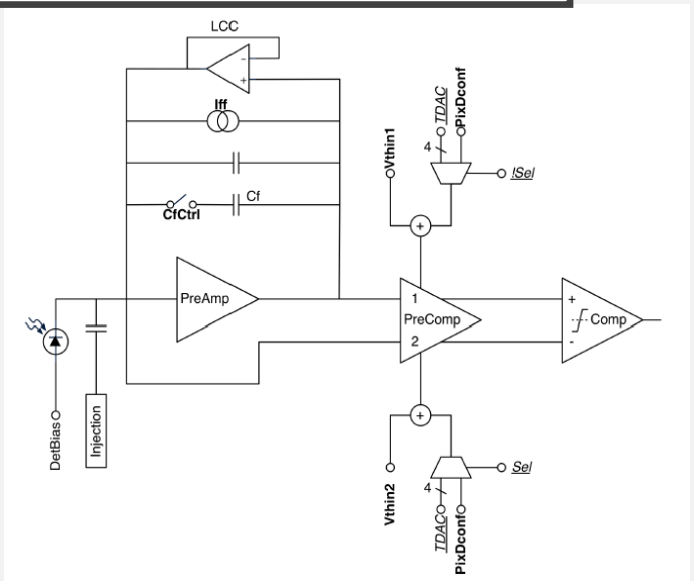
ANALOG FRONT-END

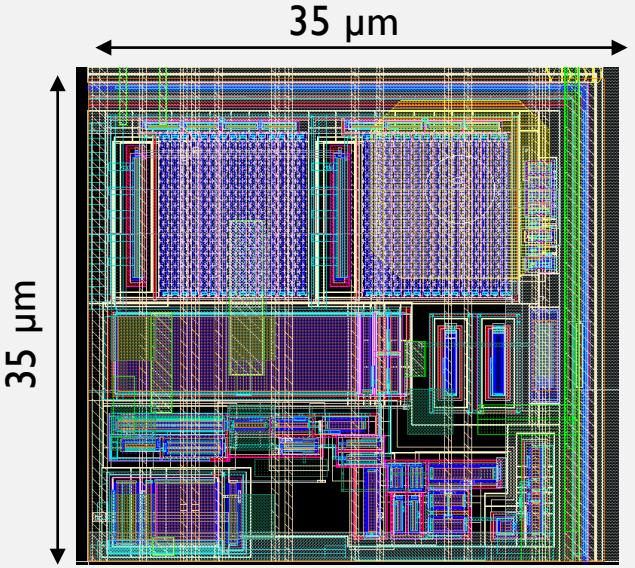
DIFFERENTIAL FRONT-END (ATLAS)

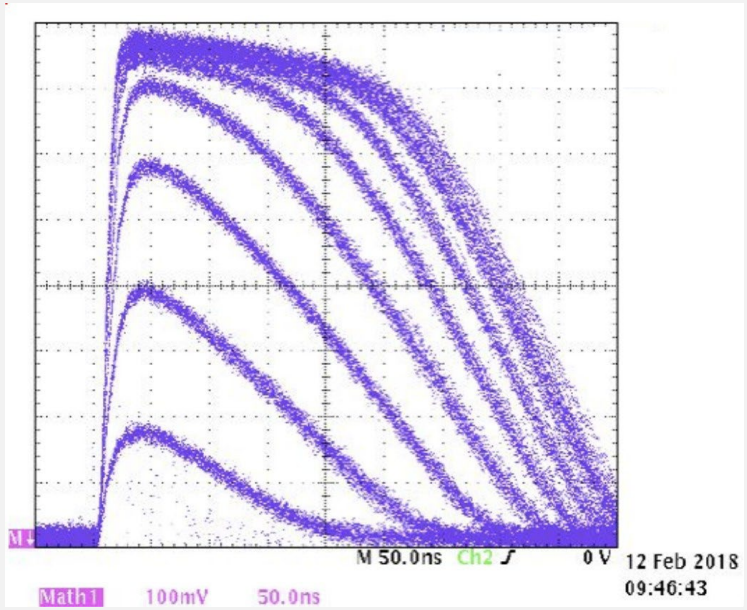
- Continuous reset integrator first stage with DC-coupled pre-comparator stage
- Leakage current compensation circuit (LCC) for additional optional feedback in case of $I_{leakage}$ > 2 nA
- Very low power: nominal current 3÷4 uA
- Two-stage open loop, fully differential input comparator

❖ 10-bit DAC for global threshold

❖ 4+1 bit local trimming DAC (TDAC) for threshold tuning

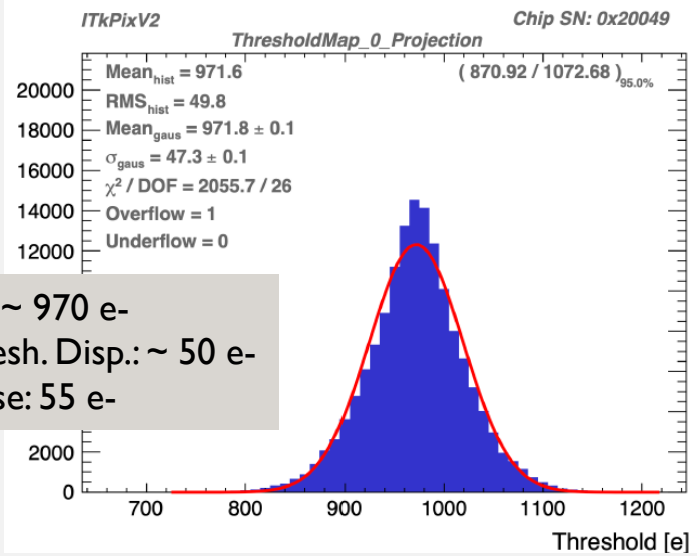




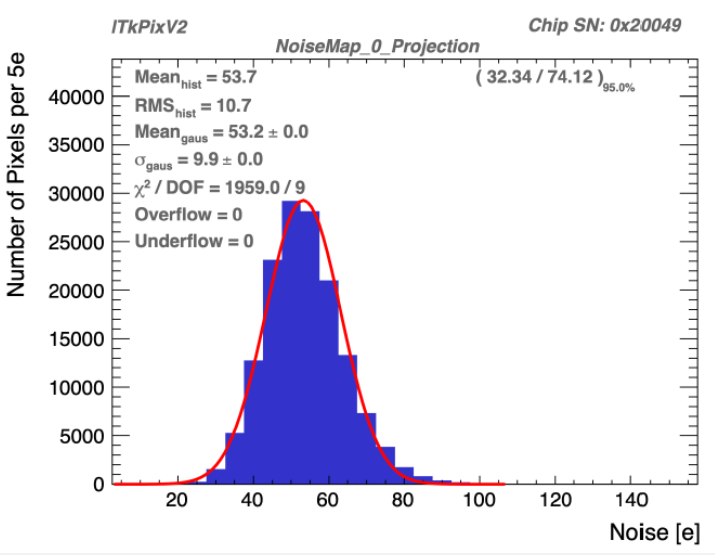


- Thr. ~ 970 e-
- Thresh. Disp.: ~ 50 e-
- Noise: 55 e-

Threshold distribution

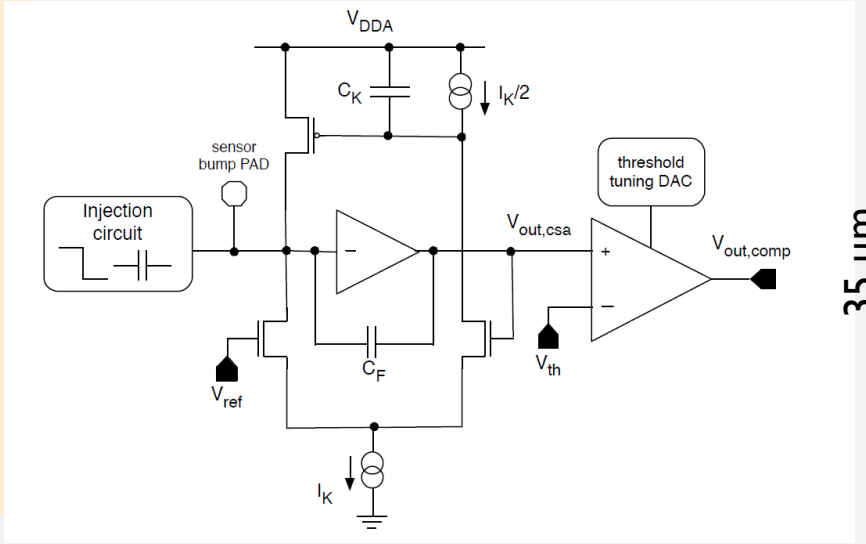


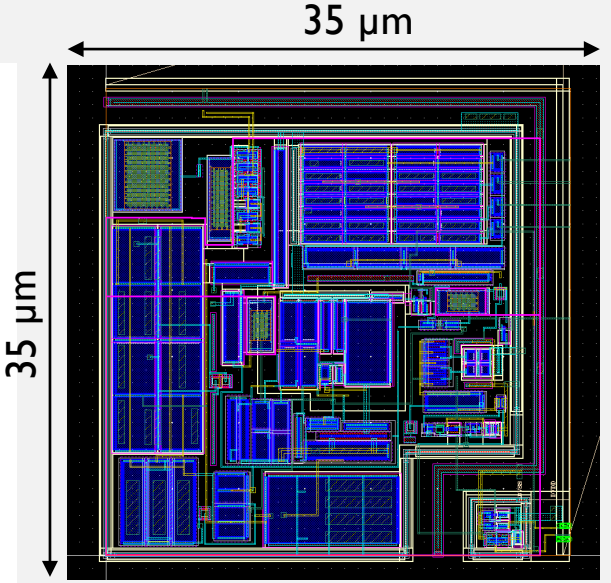
Noise distribution

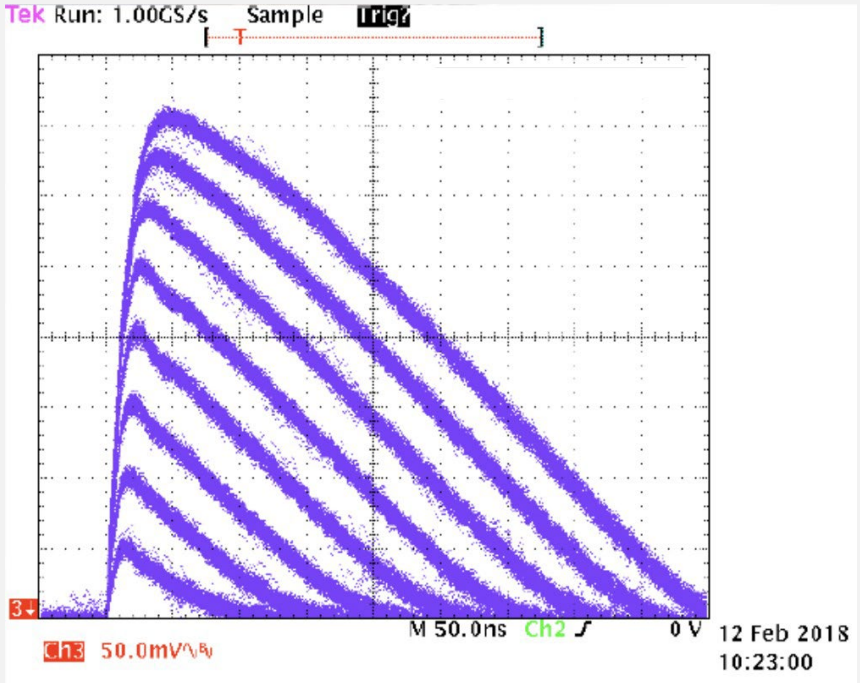


LINEAR FRONT-END (CMS)

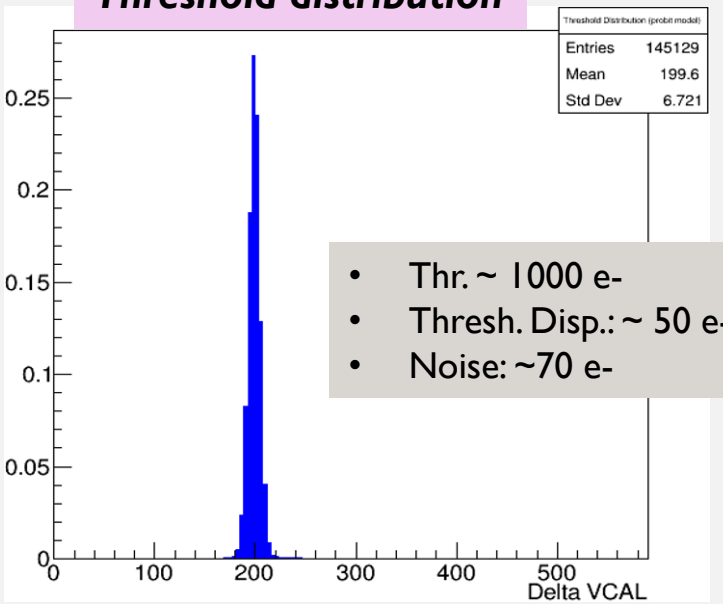
- Charge sensitive amplifier
- Krummenacher feedback for return to baseline and leakage current compensation
- Operating current: 5 uA
- Comparator
  - ❖ 10-bit DAC for global threshold
  - ❖ 5-bit local trimming DAC (TDAC) for threshold tuning





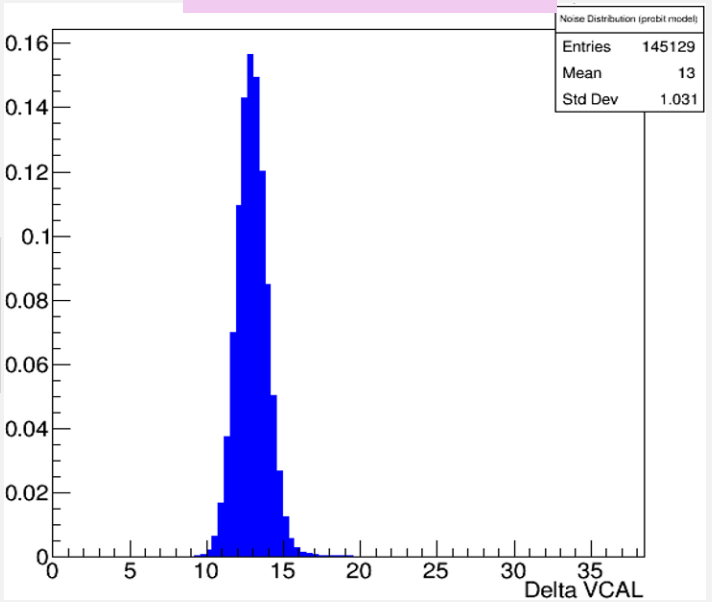


Threshold distribution



- Thr. ~ 1000 e-
- Thresh. Disp.: ~ 50 e-
- Noise: ~70 e-

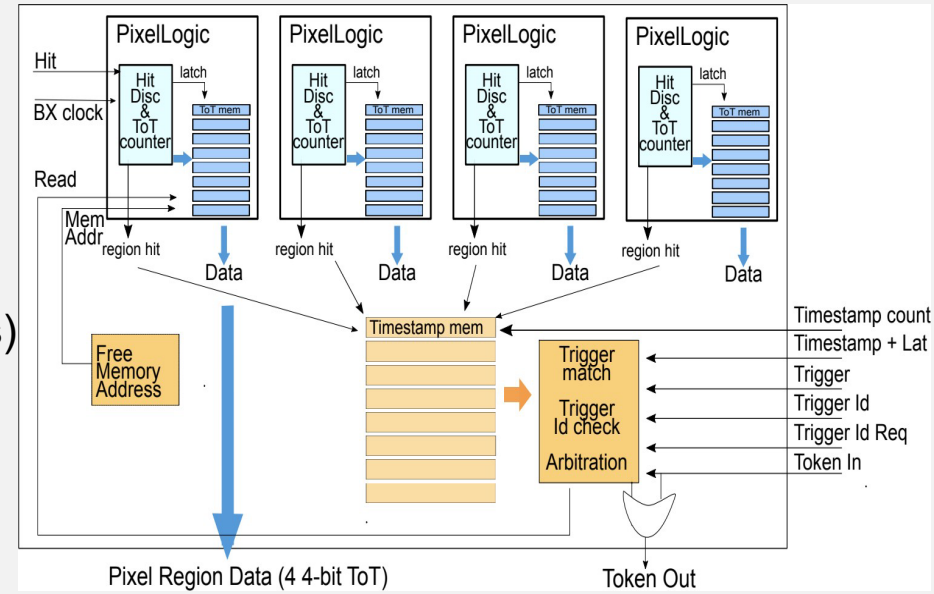
Noise distribution

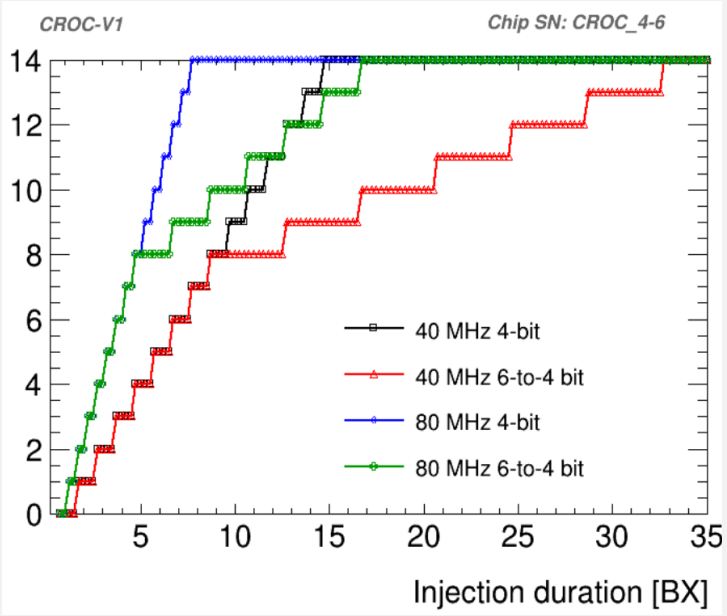


DIGITAL ARCHITECTURE

PIXEL DIGITAL ARCHITECTURE

- Hits are stored as **Time-over-Threshold**, associated to a time stamp
- 6-bit ToT counter, but only 4 bits are stored and read-out
  - ➢ Selectable ToT dual-slope 6-to-4 mapping for charge compression
  - ➢ Selectable counting clock: 40 MHz single or dual edge (80 MHz)
- **Each pixel has 8x4-bit ToT memories**
- The time stamp memory is shared among 4 pixels of the same 4x1 **Pixel Region**
- Trigger-matching performed with programmable 9-bit trigger latency (max. 12.5 μs)
- Hit-OR network for:
  - Programmable self-triggering
  - 11-bit Precision ToT (PTOT) + 5-bit ToA counters at 640 MHz in the chip periphery for precise AFE measurements and sensors characterization

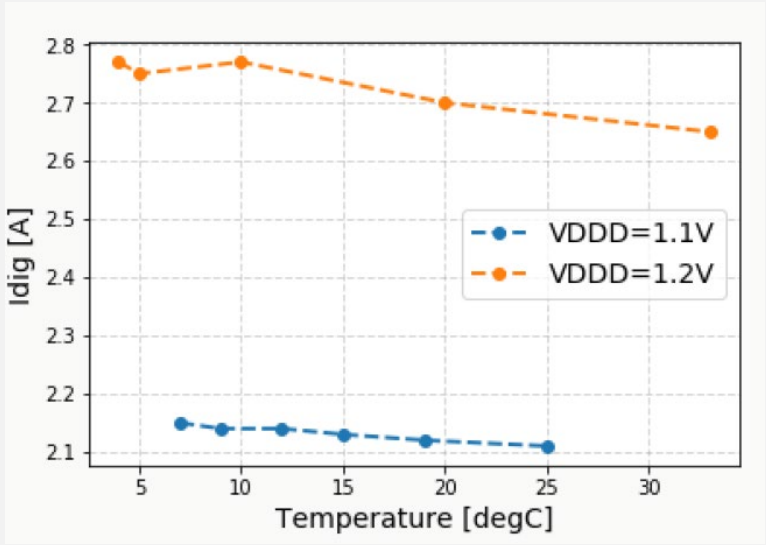


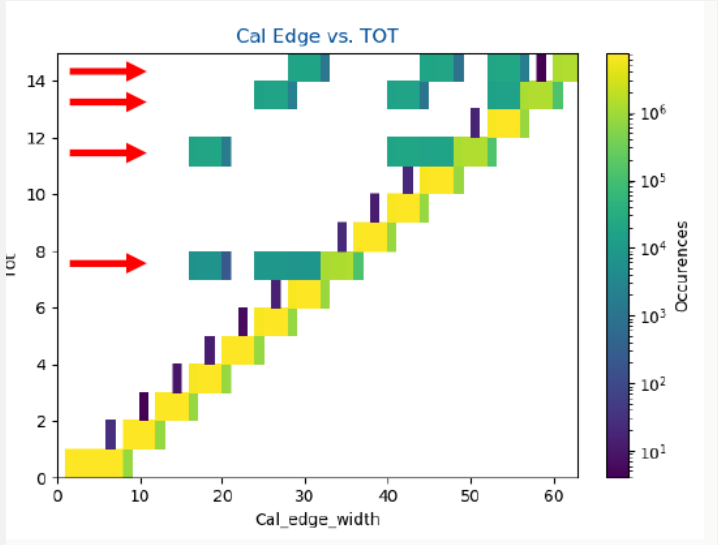


Output 4-bit code	True ToT bin (low edge) [BX]			
	40 MHz speed		80 MHz speed	
	4-bit (DEF)	6-to-4 bit	4-bit	6-to-4 bit
0	0	0	0	0
1	1	1	0.5	0.5
2	2	2	1	1
3	3	3	1.5	1.5
4	4	4	2	2
5	5	5	2.5	2.5
6	6	6	3	3
7	7	7	3.5	3.5
8	8	8	4	4
9	9	11	4.5	5.5
10	10	15	5	7.5
11	11	19	5.5	9.5
12	12	23	6	11.5
13	13	27	6.5	13.5
14	≥14	≥31	≥7	≥15.5

THE "BUG" OF TOT MEMORY

- In order to fit the 8x4-bit ToT memory in each pixel, after RD53A a custom 4-bit latch was developed and integrated in RD53B-ItkPixV1 to save ~50% area with respect to latch of the std cell library
- When we started testing RD53B-ITkPixV1, a digital current about 10 times larger than the expected was observed, together with the wrong storage of ToT information and missing hits for some ToT codes: 7, 11, 13, 14

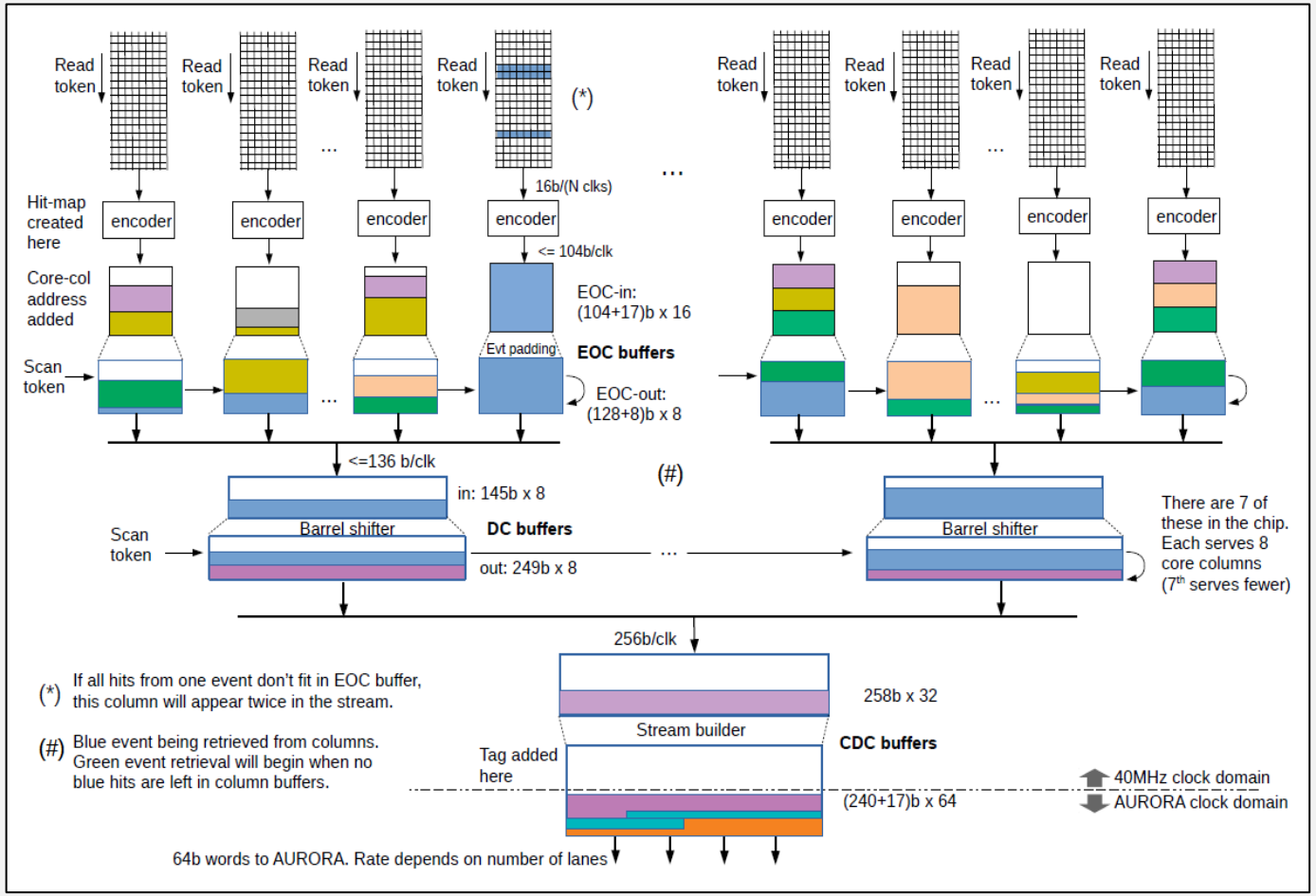




- Based on these symptoms, we realized that the bug was in the 4-bit latch, whose design was too simplified by sharing some enable lines and removing internal buffers, causing level conflicts when 3 bits were all at "1"
- But the killing factor was that **the latch had not been deeply simulated for all the input values!**
- A quick mask respin was submitted with fixes to M1 and VIA12 masks to "deactivate the bug" by transforming the 4-bit latch into a 1-bit latch, and have binary readout instead of ToT storage
- In RD53B-CROCv1 and V2 ASICs a less compact but well designed 4-bit latch was used to have back the ToT

DIGITAL DATA FLOW

- **Token based readout** of hits **in parallel** for each Core Column as soon as a valid Trigger is received
- Data are stored in a FIFO at the end of each column and compressed using **Binary Tree Encoder** (up to factor of 2)
- Data are collected from all **Core Columns** and formatted in order to form a full event.
- **Multiple levels** of data processing, event building, data buffering and formatting
- Each event is full contained and referenced by the associated Trigger Tag
- Registers **("Service data")** are read-out on command and periodically interleaved with Physics data in a programmable ratio (default: 1 in 50)
- **Aurora frames are built** and sent to the high speed serializers



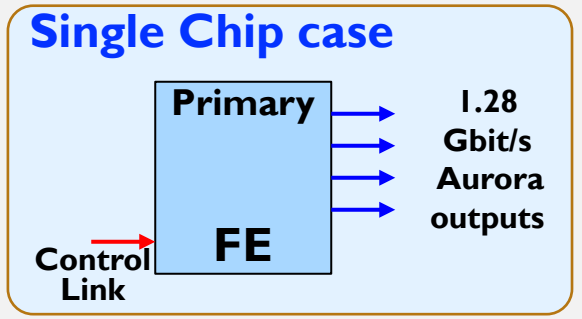
MULTI-CHIP DATA AGGREGATION

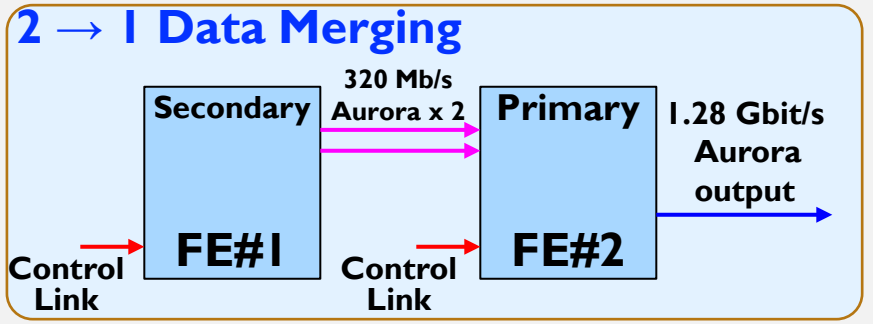
Data merging is used to optimise the number of e-links sent off a module.

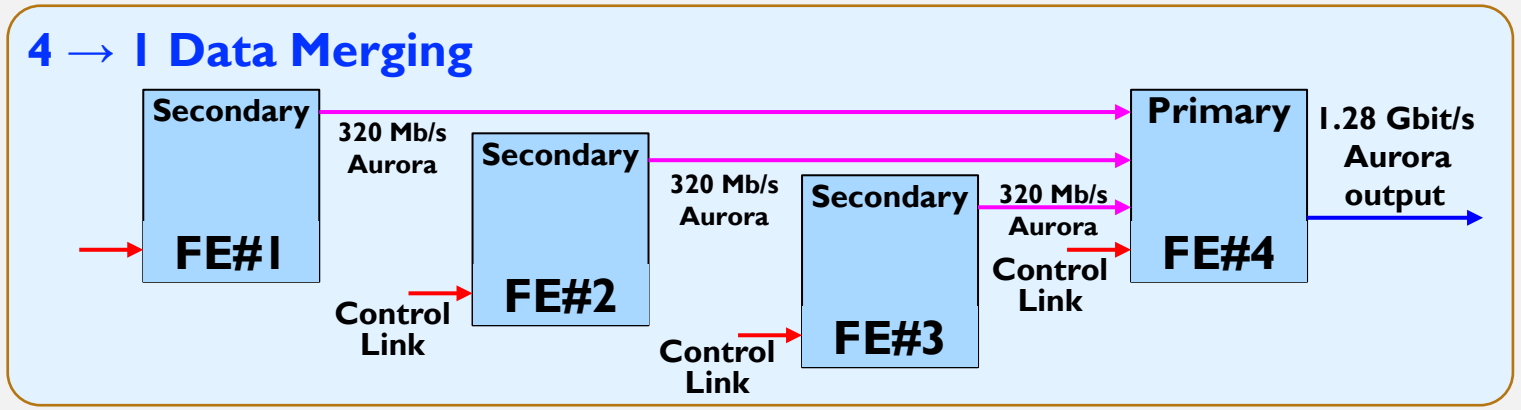
In the outer layers, one chip of the module can be configured as “primary” to aggregate serial data from one or more other “secondary” chips and merge them with its own output

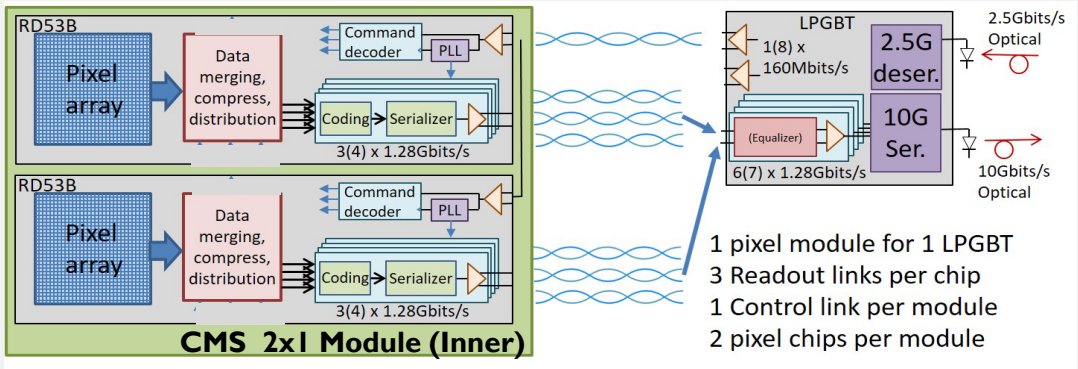
Data from the secondary chip(s) is merged with data from the primary chip using **round robin**

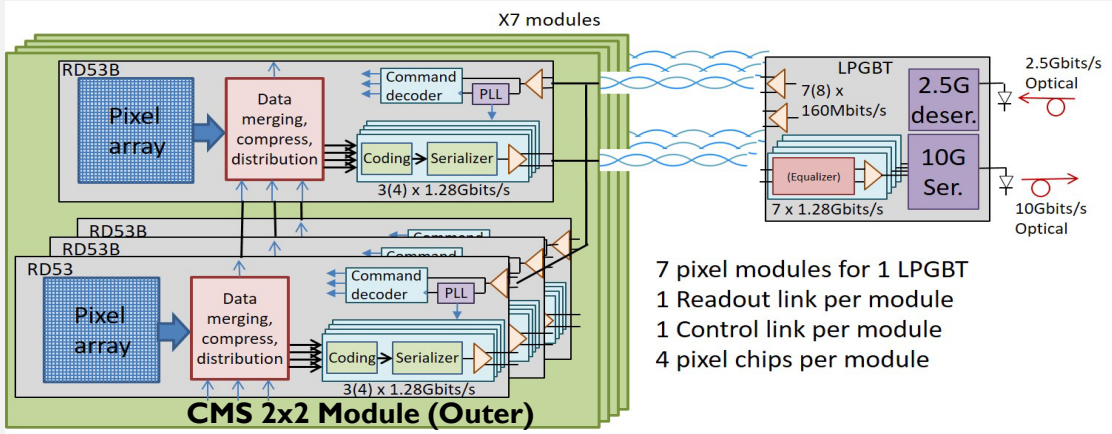
Input serial data, running at 320 Mbps, are oversampled by the primary chip and an automatic mechanism to find the best phase is implemented











AURORA AND DATA MERGING: FEATURES AND LESSON LEARNED

- Aurora Encoder: the chip sends two special Aurora blocks
  - CB: channel bonding
  - CC: clock compensation
- **A bug was introduced in RD53C (to fix some other bugs),** such that the two configuration registers CBWait and CCWait cannot contain 3N+1 codes, otherwise the link drops periodically
  - avoid those values
  - disable CC mechanism in the Aurora RX (not needed in ATLAS/CMS, since TX and RX used the same clock source)

- Data Merging is working fine and is extensively used in ATLAS and CMS modules
- However, its implementation contains **a feature discovered only during chip testing**
  - Header search: primary chip needs to identify 2-bit header position in data from secondary chips, but 2 out of 66 (3%) possible header positions result in frame alignment failure
  - Workaround: all chips of the module must be reset at the same time or deterministic delay should be applied

- These bugs have a common root cause: **shortcuts in the verification**
  - Simplified Aurora RX model, not implementing all functionalities to save simulation time
  - Inter-chip communications not explored enough (in the direct test, primary and secondary were reset at the same time!)

- Some of these bugs introduced in RD53C in the process of fixing other bugs
  - **Never assume that a simple change cannot cause damage and its verification is just a waste of time**
  - **Every change, even a trivial one, always requires careful verification**

PHYSICAL HIERARCHY: LESSON LEARNED

- The periphery was synthesized and implemented flat
  - Synthesis: ~ one day
  - Physical implementation + Eco + signoff: ~days

- Core-column controller block is replicated 50/54 times in the periphery
- It would have been more efficient to implement the core-column controller block and then instantiate it 50/54 times
  - It was tried in a later phase, but it would have required major modifications at RTL and in the flow, not compatible with the urgency to go in production

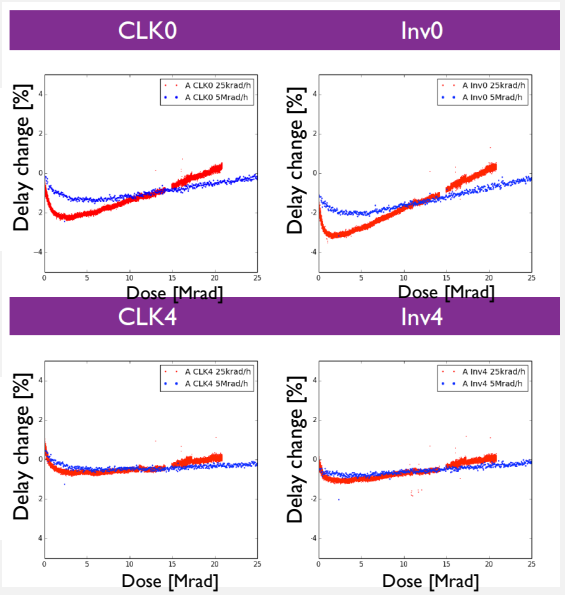
- Define the hierarchy since the beginning for a more efficient implementation and verification

RADIATION TOLERANCE

TID

- **The TID damage mainly concerns the digital design because of the small area devices (min L, small W) → more severe for "strength 0"**
- **Gate delay degradation larger at low dose-rate (LDR): more severe for "strength 0"**

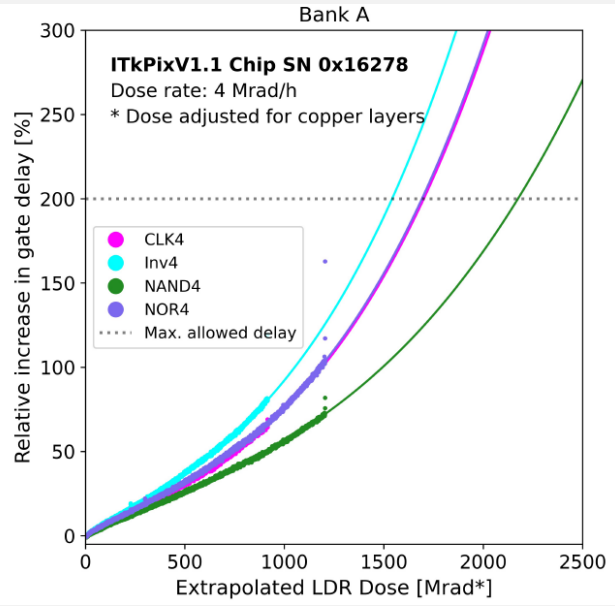
Delay change at 5 Mrad/h and 25 krad/h



Ratios of damage at low and high dose rate

Gate	LDR/HDR damage
CLK 0	4.8
CLK 4	2.4
Inv 0	4.6
Inv 4	2.5
NAND 0	3.2
NAND 4	1.7
NOR 0	2.7
NOR 4	1.8

Estimated behaviour at LDR of strength 4 gates



Design strategy:

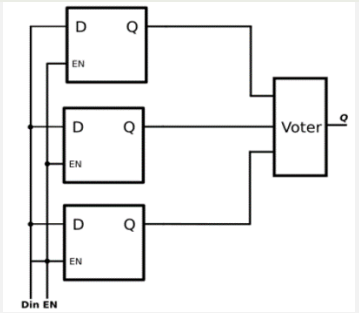
- **No minimum size digital cells → 9-track library everywhere (12-track in PLL and serializer). No strength 0.**
- **Irradiation corner models and extreme corners** from the foundry used to predict the TID effect and design to guarantee good timing for the digital design → **Timing closure extremely challenging**
- **Tests done at low temperature (-20°C) and high dose-rate, extrapolating the behaviour using the LDR/HDR correction factor, give confidence that RD53 chips will meet TID specifications (at least 1 Grad) if operated at cold temperature**

SINGLE EVENT EFFECT PROTECTION

- ❑ **The expected rate per chip of Single Event Effects (SEEs) is ~ 100 Hz in the innermost layer**
- ❑ **Target behaviour:**
- Stable operation: bias and the Clock and Data Recovery are critical for the overall chip functionality and must be very SET robust
- No power cycling: need to recover without power-cycling (detrimental for a serially powered system)
- Occasional hit/event is allowed to be lost
- ❑ **Principle:** protect with triplication vital circuitry (configuration registers, state machines, memory pointers) as far as feasible within space and power budget limits → cannot protect everything!
- a **CLEAR** command for fast recovery from residual SEE or operational issues
- provision for **continuous reprogramming** of global registers and pixel configuration

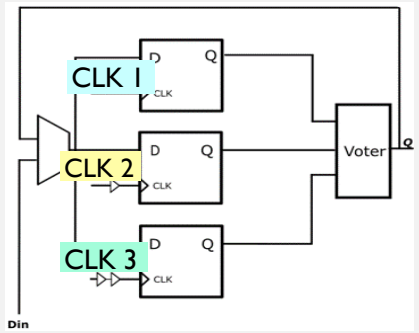
Pixel Configuration

- 8 bits → 1.28 Mbit/chip
- 5 more relevant bits protected with TMR without self-correction
- Need to continuously refresh
- ➢ **With protons: 100 x more SEE tolerant than unprotected**

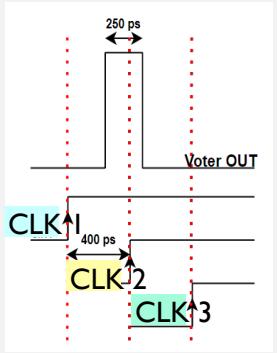


Global Configuration and state machines

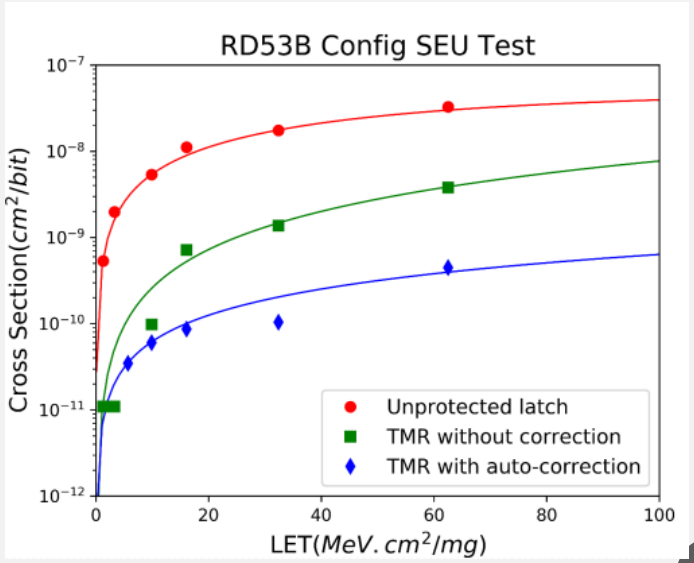
- ~90 kbit/chip
- TMR with self-correction and triplicated clock with skew (ΔT ~ 400ps) for **Single Event Transient** filtering
- ➢ **With protons: 400 x more SEE tolerant than unprotected**



SET filtering



SEU cross-section from heavy-ion testing



SINGLE EVENT EFFECT PROTECTION

- The adopted triplication is functionally correct, with advantages compared to full TMR in terms of power and area
- Drawbacks:
  - SEU cross-section ≠ 0
  - Additional complexity in timing closure, especially for a large and flat design
    - Reduced setup margin
    - Requires significant buffering for hold fix
- **Both SEE simulations and tests (Heavy ions, protons, laser) are needed** to identify vulnerabilities
  - As an example, a critical fault condition, causing the chip readout to get stuck, was not properly evaluated with SEU testing because depending on high trigger rate, high hit rate, and a high SEU rate simultaneously → identified and fixed with SEU simulations
- SET injection simulations on critical IP blocks, like Bandgap, PLL, SLVS RX/TX are also crucial to identify weakness that cause problems in operation: bias drops, link drop-out, …

CONCLUSIONS

- RD53 ASICs are large and complex pixel readout chips for the HL-LHC pixel detectors
- **The final chips were submitted to foundry in 2023 and mass production is complete**
- Representative example of a large-scale collaborative ASIC project in high-energy physics, involving approximately 24 institutes worldwide and more than 30 designers
- Beyond the challenging specifications, also the implementation and verification represented a challenge in terms of human and computing resources
- Known bugs caused by shortcuts in verification or missing simulations. However effective workaround exist and the chips can be used without limitations
- 10-year development: too many?
  - Requirements evolved over time
  - In-depth technology characterization
  - In-house development and qualification of all the IPs (~20)
  - Two “customers” requiring design variations with overlapping schedules and extreme pressure
  - Departures of key designers also had to be addressed, and finding adequate replacements took some time
  - The importance of verification was considered crucial since the beginning, but it had to face the difficulty in finding the right skills in the field → great support from CERN-ESE in the last years

THANK YOU FOR YOUR ATTENTION!

BACKUP

Jinst

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RD53 pixel readout integrated circuits for ATLAS and CMS HL-LHC upgrades

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The RD53 collaboration

G. Alimonti,[11] A. Andreazza,[11] F. Arteche,[22] M.B. Barbero,[1] P. Barrillon,[1] R. Beccherle,[16] G. Bonomelli,[20] G.M. Bilei,[15] W. Bialas,[3] D. Bortoletto,[5] G. Calderini,[26] A. Caratelli,[3] A. Cassese,[9] J. Christiansen,[3,*] E. Conti,[3,15] F. Crescioli,[26] M. Daas,[35] L. Damenti,[9,10] S.D'Auria,[11] F. De Canio,[13] G. De Robertis,[8] N. Demaria,[17] J. DeWitt,[31] Y. Dieter,[35] A. Dimitrievska,[25] W. Erdmann,[29] S. Esposito,[3] D. Exarchou,[3] D. Fougeron,[1] L. Gaioni,[13] M. Garcia-Sciveres,[25] D. Gnani,[25] C. Gozalez Renteria,[36] M. Grippo,[17,18] A. Guardino,[36] M. Hamer,[35] T. Heim,[25] T. Hemperek,[35] F. Hinterkeuser,[35] S. Hulberts,[34] L.M. Jara Casas,[3] J.J. John,[5] J. Kampkötter,[33] M. Karagounis,[33] I. Kazas,[27] Y. Khwaira,[23] R. Kluit,[28] D. Koukola,[3] A. Krieger,[25] H. Krüger,[35] J. Lalic,[3] M. Lauritzen,[34] F. Licciulli,[8] Peilian Liu,[21] F. Loddo,[8] E. Lopez Morillo,[6] A. Lounis,[23] F. Luongo,[17,18] M. Manghisoni,[13] S. Marconi,[3,15] F. Marquez Lasso,[6] C. Marzocca,[30] K. Mauer,[35] A. Mekkaoui,[4] Lingxin Meng,[24] M. Menichelli,[15] M. Menouni,[1] M. Minuti,[16] M. Mironova,[25] S. Miryala,[2] M. Missiroli,[29,32] E. Monteil,[17,18] K. Moustakas,[35] F. Muñoz Chavero,[6] G. Neue,[7] S. Orfanelli,[3] A. Paccagnella,[12] L. Pacher,[17,18] F. Palla,[16] F.R. Palomo Pinto,[6] A. Papadopoulou,[25] A. Paterno,[17,18] A.R. Petri,[11] P. Placidi,[15] R. Plackett,[5] A. Pradas,[22] A. Pulli,[3] B. Raciti,[19] L. Ratti,[14] V. Re,[13] A. Rehman,[34] P. Rymaszewski,[35] P. Sander,[20] M.C. Solal,[23] M. Standke,[35] B. Stugu,[34] E. Thompson,[25] G. Traversi,[13] D. Vogrig,[12] M. Vogt,[35] Tianyang Wang,[35] Hongtao Yang[37] and J. Zdenko[7]

[1]*Aix Marseille Université, CNRS/IN2P3, CPPM, Marseille, France*
[2]*Brookhaven National Laboratory, Upton, NY, U.S.A.*
[3]*CERN, European Organization for Nuclear Research, Geneva, Switzerland*
[4]*Clevert Systems LLC , West Henrietta, NY, U.S.A.*
[5]*Dept. of Physics, Oxford University, Oxford, United Kingdom*
[6]*ETSI, Universidad de Sevilla, Sevilla, Spain*
[7]*Faculty of Nuclear Sciences and Physical Engineering, Czech Technical University in Prague, Prague, Czech Republic*
[8]*INFN Sezione di Bari, Bari, Italy*
[9]*INFN Sezione di Firenze, Florence, Italy*
[10]*Università di Firenze, Florence, Italy*

*Corresponding author.

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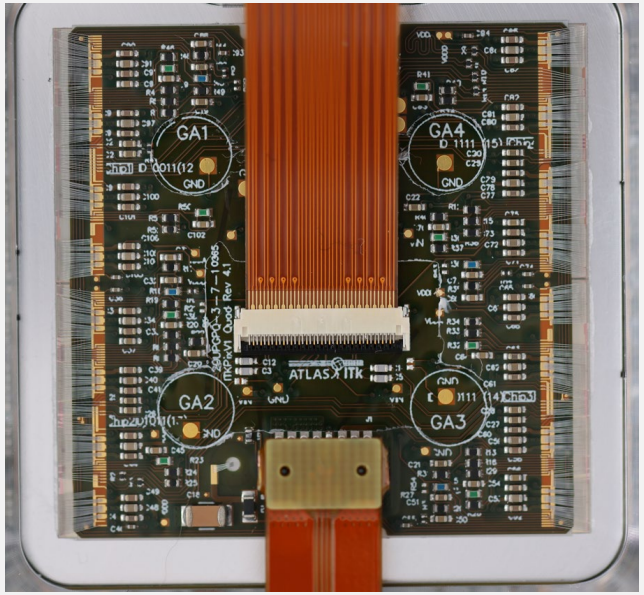
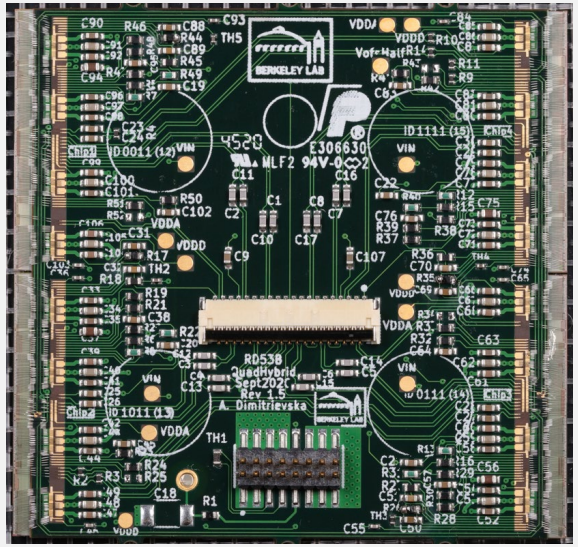
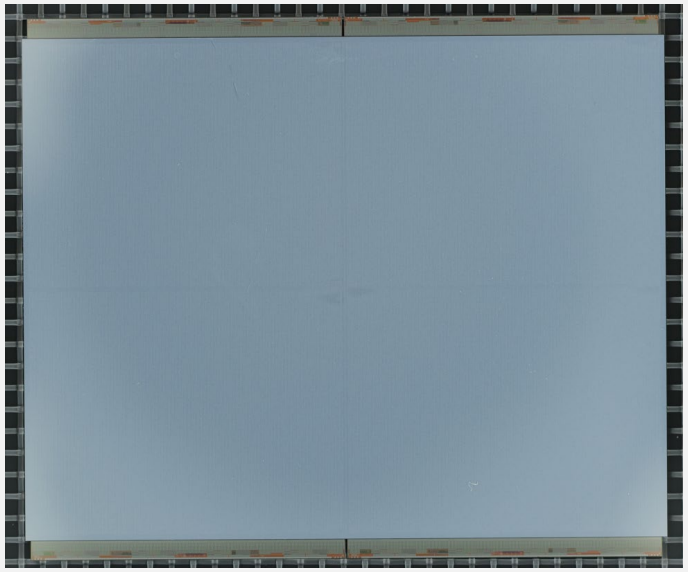
PHOTO GALLERY

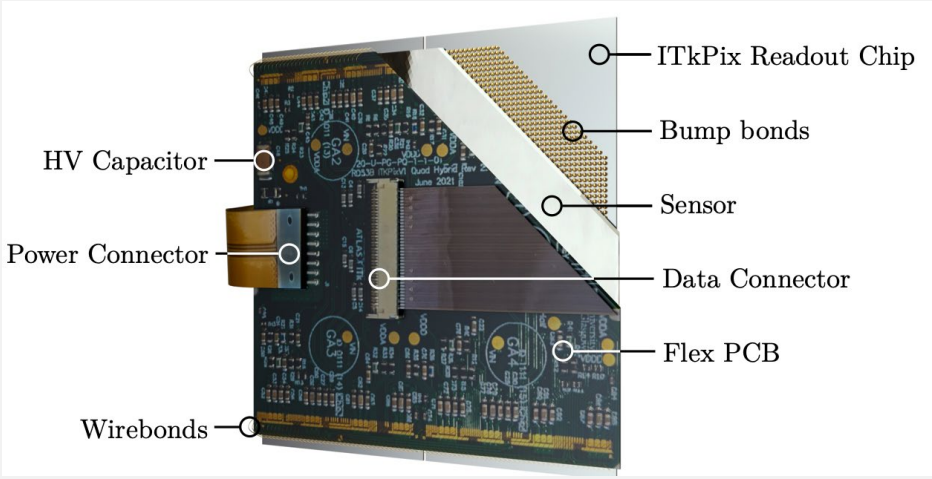


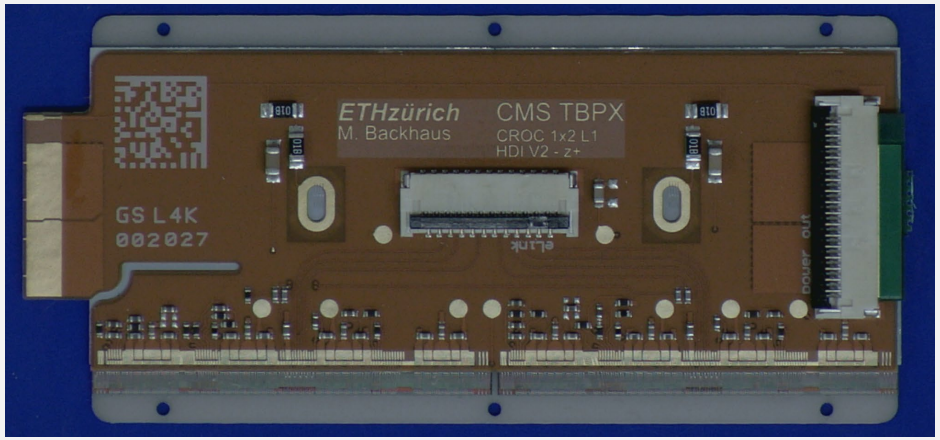


ATLAS ItkPix Quads



CMS TEPX 2x2 Bare module

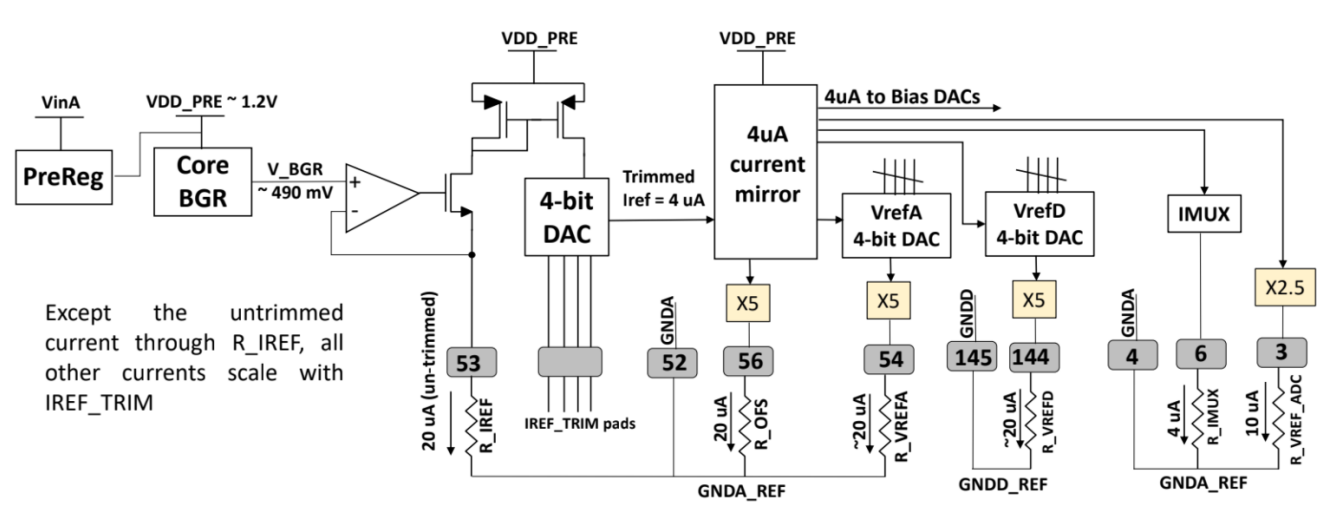


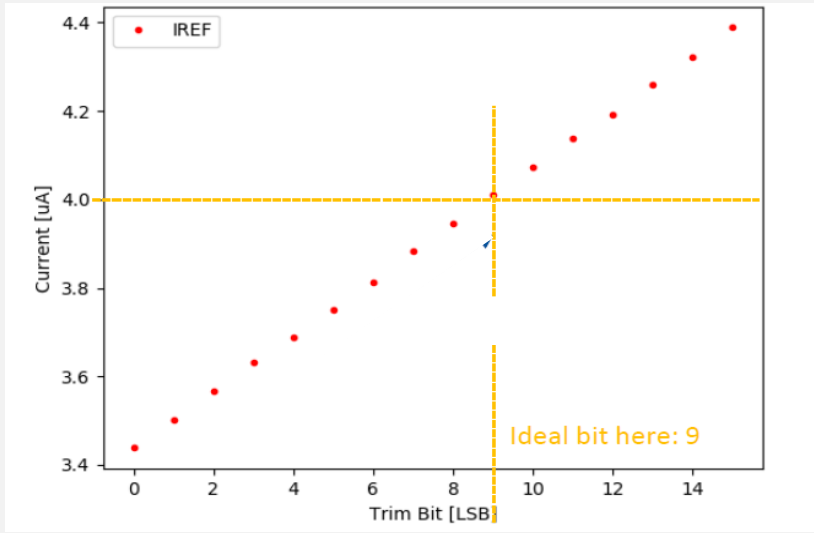


CMS TBPX 1x2 CROC module

BIAS, REFERENCES AND MONITORING

- BIAS and Reference network is based on
  - **PreRegulator** (2V tolerant) used to provide ~1.2V to power the Core bandgap
  - **Core Bandgap**, to provide precise reference voltage/current with low sensitivity to temperature variations
- Tuning by means of 4 wire-bond trimming pads (<u>no SEU</u>), whose optimal value is found during **<u>wafer probing</u>**
- The tuned current I_{ref} is used as reference to the ADC and more than 20 DACs to bias the analog Front-end, the CDR and all IPs

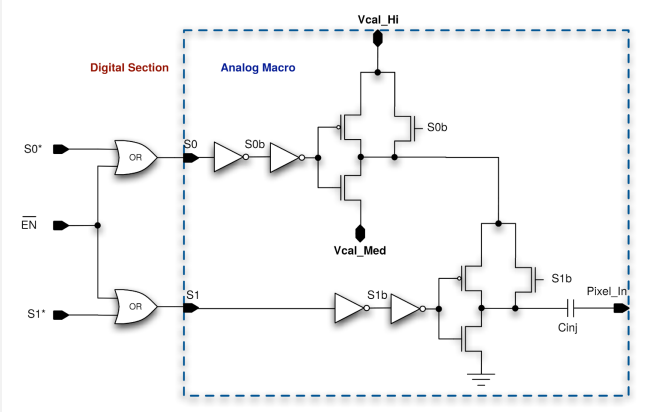


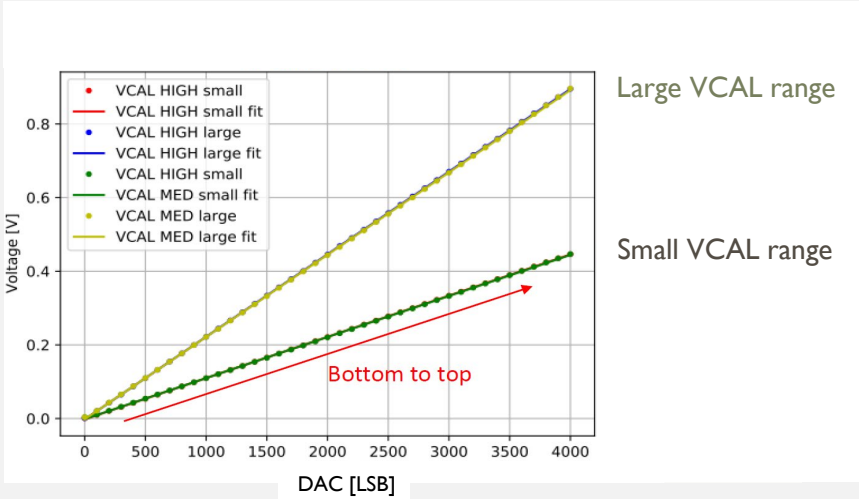


- The Monitoring block used to readout internal parameters (T, voltages and currents) based on a **12-bit ADC** (LSB ~ 220µV)
- **5 temperature sensors** in different positions (near the ShLDOs, in the centre of periphery, top/bottom of the matrix)
- **Ring oscillators** → measurements of digital cells speed degradation with TID

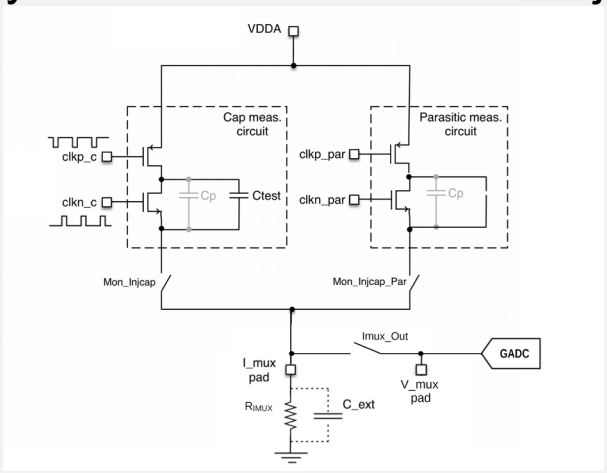
CALIBRATION

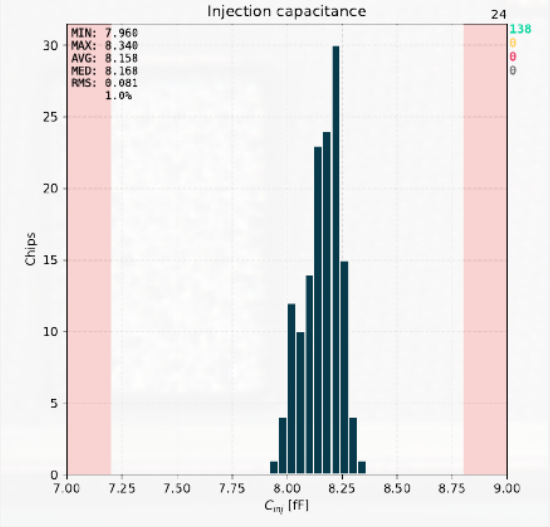
- Each pixel is equipped with a novel calibration injection circuit for test and calibration purpose capable to inject 2 consecutive hits of different amplitude (VCAL_High-VCAL_Low ; VCAL_Low – GND)
- The analog injection uses two distributed voltages, provided by two 12-bit voltage DACs, to generate a precise voltage step fed to an injection capacitor
- Two selectable ranges





- Possibility to measure the value of injection capacitor using a dedicated circuit to define precisely the injection step

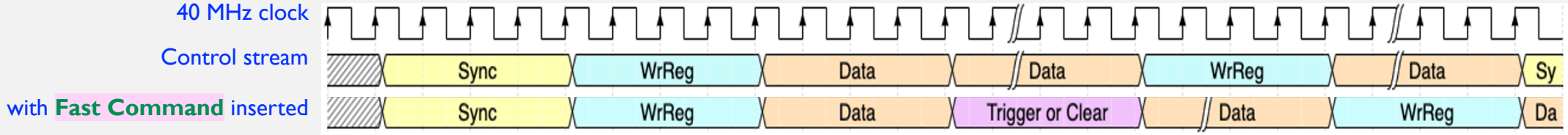




CONTROL LINK

The RD53 control protocol was designed to meet these requirements:

- **Minimise cabling and material in the detector:**
  - Both commands clock are recovered from a **single differential pair @ 160 Mbps**
  - The periodic Sync command guarantees sufficient transitions to recover the clock
- **DC-balanced → AC-Coupling**
- **Fast Commands** = 16 bits, 100 ns to send**; Slow Commands** = variable length, up to some ms to send
- **High trigger rate**
  - Trigger commands are **Fast Commands** with **high priority**
- **High radiation environment**
  - The symbols are separated by a Hamming distance of 2, allowing error detection
  - To speed up recovery from errors, the **CLEAR** command, which resets the data path, is a minimum-sized **Fast Command**
- **Deadtime-less communication**
  - Fast Commands can be interleaved by **Slow Commands** such as Read and Write Register



  - Write Register commands have features to auto-increment register addresses and to broadcast to up to 15 chips on a shared bus, to speed up chip configuration → **the chip can be continuously reconfigured in ~100 ms:**

SEE RATES

- **SEE rates at order of magnitude level: factor 10 – 100 uncertainty**

A. Non protected registers (3 out of 8 pixel config, memories):

Inner layer: 1 GHz/cm^2 * 1x10^{-14} cm^2/bit = ~1x10^{-5} Hz/bit

- **Memories: ~ 9 Mbit → ~ 100 Hz/chip → (fake or lost hits)**
- **Pixel conf (non-critical bits): 435 kbit → 4.35 Hz/chip**

B. TMRed pixel configuration registers without auto correction (5 out of 8 pixel config):

Inner layer: 1 GHz/cm^2 * 1x10^{-16} cm^2/bit = ~1x10^{-7} Hz/bit

- **Pixel conf : 726 kbit → ~ 0.1 Hz/chip (1 bit flip every 10 s)**

No error correction mechanism built in → Errors will accumulate and as soon as two flips affect the same register the wrong value will be stored. **To avoid error accumulation, the pixel configuration registers must be refreshed!**

C. TMRed global config, state machines, critical data with auto correction :

Inner layer: 1 GHz/cm^2 * 2x10^{-17} cm^2/bit = ~2x10^{-8} Hz/bit

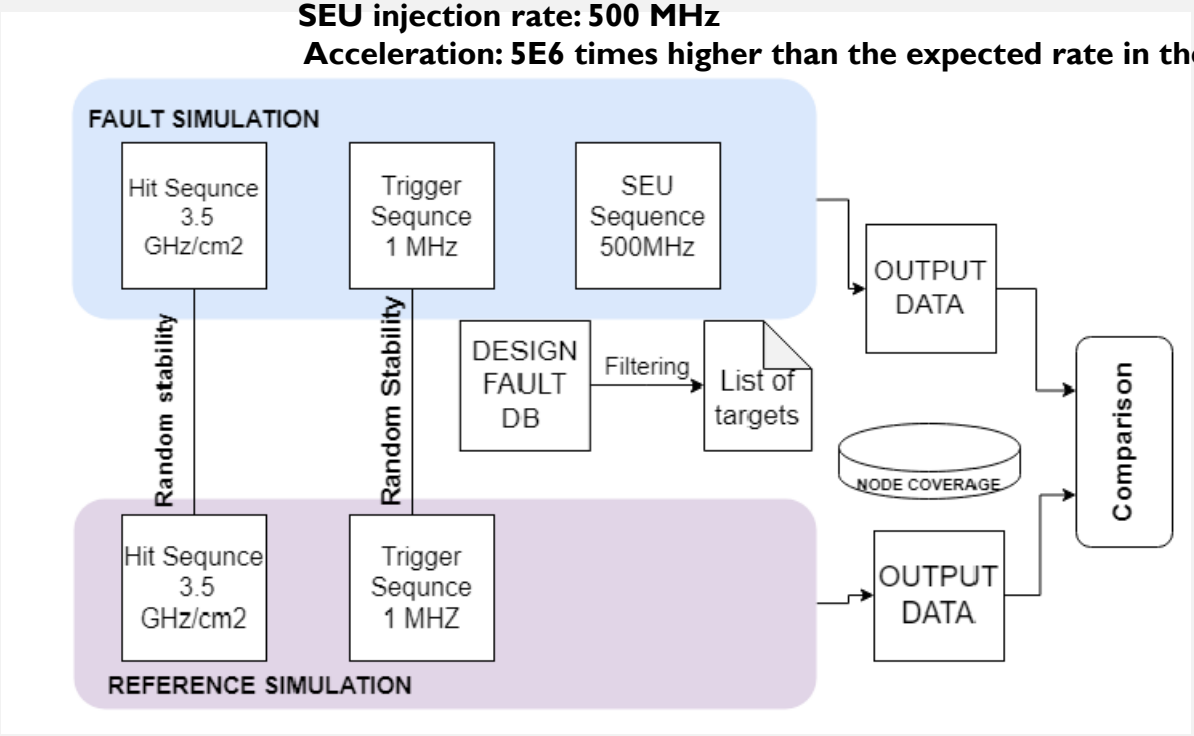
- **State machines: 90 kbit * ~2x10^{-8} Hz/bit = ~ 1.8 mHz/chip (1 bit flip every ~ 10 min)**
- **Global conf: 3.4 kbit → 0.07 mHz/chip (1 bit flip every ~ 4 hrs)**

❑ **Reconfiguration of Pixel and Global configuration registers (1.16 Mbit)**

- Assuming that only 50% of downlink available for this, with some margin it takes **~ 100ms/chip → max rate ~ 10Hz**
- A refresh every 10s (**0.1 Hz)** should be enough to avoid misconfigured pixels accumulation
- **Deadtime-less reconfiguration**: Slow Commands such as Read and Write Register are halted by Fast Commands with high priority (Trigger, CLEAR…) and then resumed

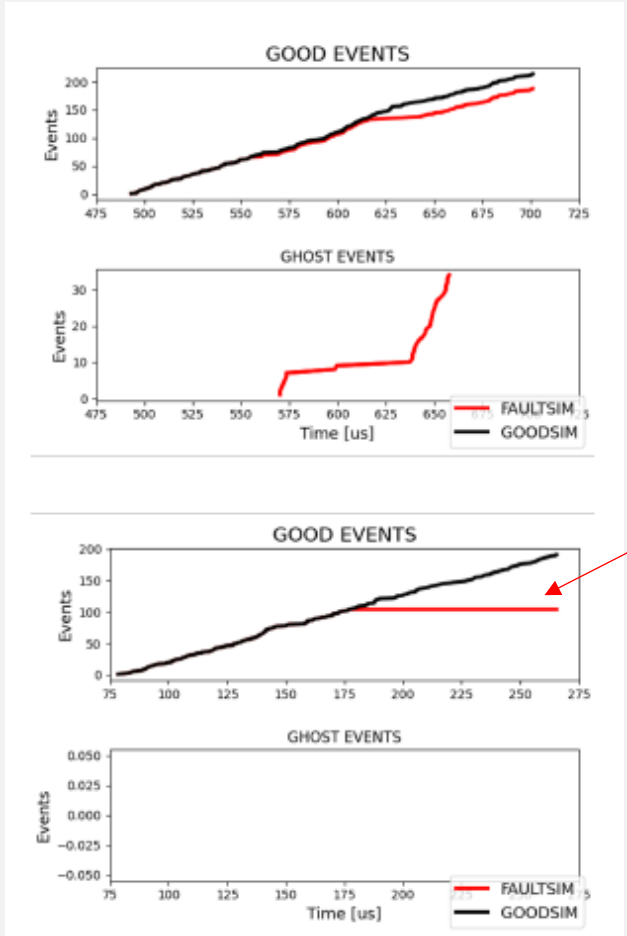
SEE VERIFICATION @ RTL

SEU injection rate: 500 MHz
Acceleration: 5E6 times higher than the expected rate in the inner layer



Fault injection and reference simulation are run together using the same SEED. They differ for SEE-induced:

- Lost hits
- Ghost hits
- Chip stuck → vulnerability identified in RD53B → fixed
- low cross-section chip stuck still present, but fast recovery with CLEAR command (no power cycle)



Chip stuck

Events comparison between fault and reference simulation for the same SEED

SEE SIMULATIONS: RTL VS GATE LEVEL

Verification task	Can be done @RTL	Can be done @GL	Comment
SEU injection on unprotected registers	yes	yes	Used naming to determine if register is triplicated or not
SET injection simulations	no	yes	Supported only at GL
Implementation of pixel config. bits TMR is OK?	yes	yes	Triplication implemented at RTL
Implementation of TMR with skew is OK?	no	yes	Triplication implemented during synthesis → GL
Disabling one of the triplicated clocks is OK?	no	yes	Triplication implemented during synthesis → GL

@RTL:

- Unprotected registers
- Pixel configuration registers

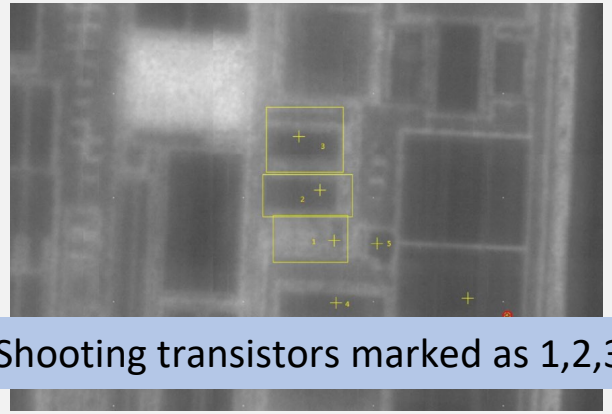
@GL:

- SEU injection on triplicated nodes to check that the triplication insertion was properly done by the synthesis tool
- SET (Single Event Transients) with fixed widths of 100 ps, 250 ps and 500 ps in voters output and FF inputs (the last gate of the combinatorial path driving a FF)

SET SIMULATIONS ON CRITICAL ANALOG BLOCKS

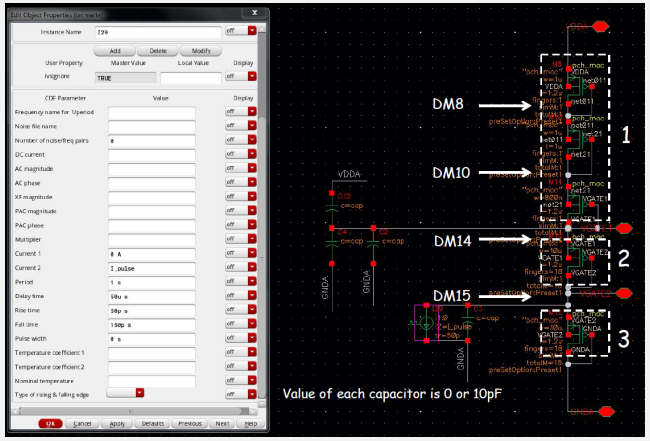
Example: SET improvement of CORE bandgap

- A high rate (~5Hz for inner layer) of link drop-outs have been seen in ion/proton tests on V1 chips. Extensive laser tests and SET injection simulations have identified the cause in the SET sensitivity of the bandgap reference circuit, controlling biasing of all analogue blocks and the PLL VCO → Fixed in RD53C

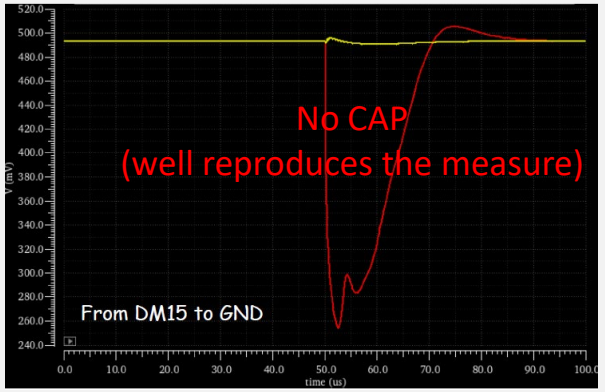


Shooting transistors marked as 1,2,3

Laser test →



Simulation →



Solution:

- add capacitors to some sensitive nodes
- Improvement implemented in RD53C and confirmed in SEE measurements