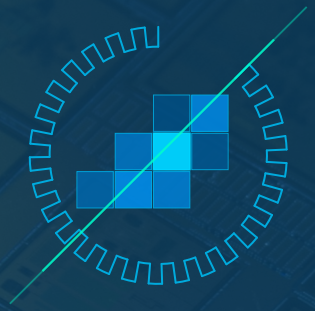
PICOPIX



PIXEL DETECTOR ASIC FOR HIGH-PRECISION PARTICLE TRACKING

Alessandro Caratelli on behalf of PICOPIX design team

alessandro.caratelli@cern.ch

Design team

- Project management — Xavi Llopart — CERN

- Architecture
- Digital design
- Physical implementation
- Signoff verification

  Xavi Llopart, Alessandro Caratelli, Gianmario Bergamin — CERN

- Analog design — Rafael Ballabriga, Jan Kaplon — CERN; Lucas Timmermans, Oi Ying Wong, Vladimir Gromov — NIKHEF

- Functional verification — Matteo Lupi, Adithya Pulli, Simone Scarfi — CERN

- Macro-blocks / Projects used by PICOPIX:
  - TFC (Timing and fast-control) — Federico De Benedetti — EP R&D WP1 / LHCb
  - ESB (Event-Sorter) — Francesco Brambilla — EP R&D WP5
  - SPRINT (Data serializer) — Stefan Biereigel, Gabriele Ciapri, Thiago Daros, Szymon Kulis, Gabriele Atzeni — EP R&D WP6
  - ROSA (RISC-V microcontroller) — Marco Andorno, Benoit Denkinger, Adrian Fiergolski, Anvesh Nookala — EP R&D WP5

PICOPIX

A large-area mixed-signal pixel detector ASIC for high-precision particle tracking designed targeting the requirements of multiple applications

LHCb collaboration

- VELO detector upgrade for LS4 | Primary target

SY - BI CERN group

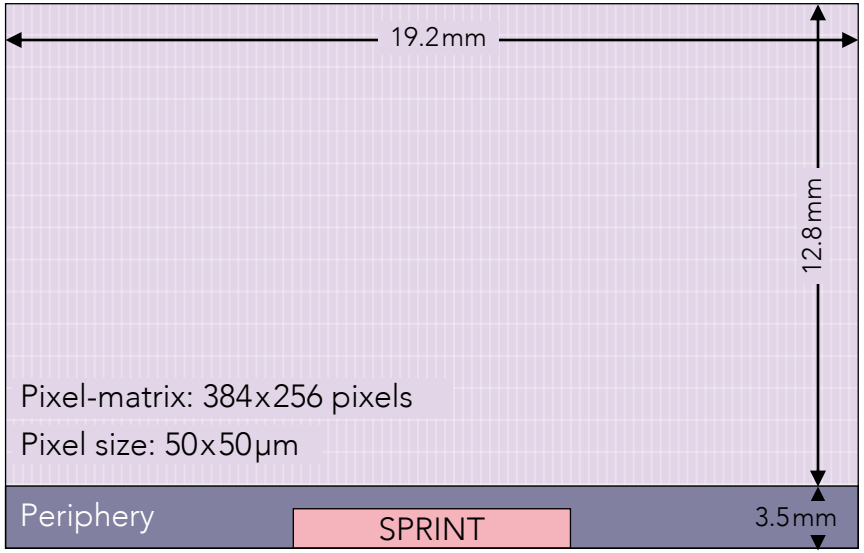
- Beam-loss monitoring
- Diagnostics for LHC

medipix collaboration applications

- Medical imaging: PET, SPECT
- Time-resolved photon science
- Mass spectrometry
- Radiation monitoring
- Electron microscopy for material science
- Beam diagnostics

PICOPIX

A large-area pixel detector ASIC for high-precision particle tracking



Data-driven mode

- For tracking applications
- Timing resolution → $30ps_{RMS}$
- ToT → 12bits each pixel
- On-chip clustering with ToT based centroid extraction
- On-chip time-correction
- On-chip time-walk correction
- On-chip auto-calibration
- On-chip cluster filtering
- On-chip packets sorting

Event rate

- Max event rate per matrix → $3.8 \cdot 10^9$ cl/s
- Max event rate per area → 10^7 cl·s^{-1} mm^{-2}
- Max single pixel rate → 20 MHz/pixel
- Max bit-rate → 102.4Gb/s (4 links)

Control and configuration

- Independent slow-control and synchronous control ports
- On-chip RISC-V microcontroller

Process

- 28nm bulk CMOS
- 10M 5x1y1z1u+rdl
- 0.9V + 3.6V supply

Radiation tolerance

- TID → > 1Grad
- SEE → protected control and configuration

Frame based mode

- For imaging applications
- Zero-suppressed
- ~Continuous readout window

Front-end

- Front-end for low-gain: planar, 3D, LGAD
  - ENC < $95e^-$ (100fF input capacitance)
  - $Q_{IN-THR} > 4ke^-$ → jitter < $25ps_{RMS}$
- Front-end for high-gain sensors: SPAD

The timing resolution challenge on a large array matrix

Track time resolution for VELO detector < 20ps $_{rms}$

↓

Single plane resolution of = σ^2_{sensor} + σ^2_{ASIC} < 50ps $_{RMS}$

↑ 40ps $_{RMS}$

↓

$\sigma^2_{analogFE}$ + σ^2_{clock} + $\sigma^2_{conversion}$ = σ^2_{ASIC} (< 30ps $_{RMS}$)

BIN size 40ps $_{RMS}$

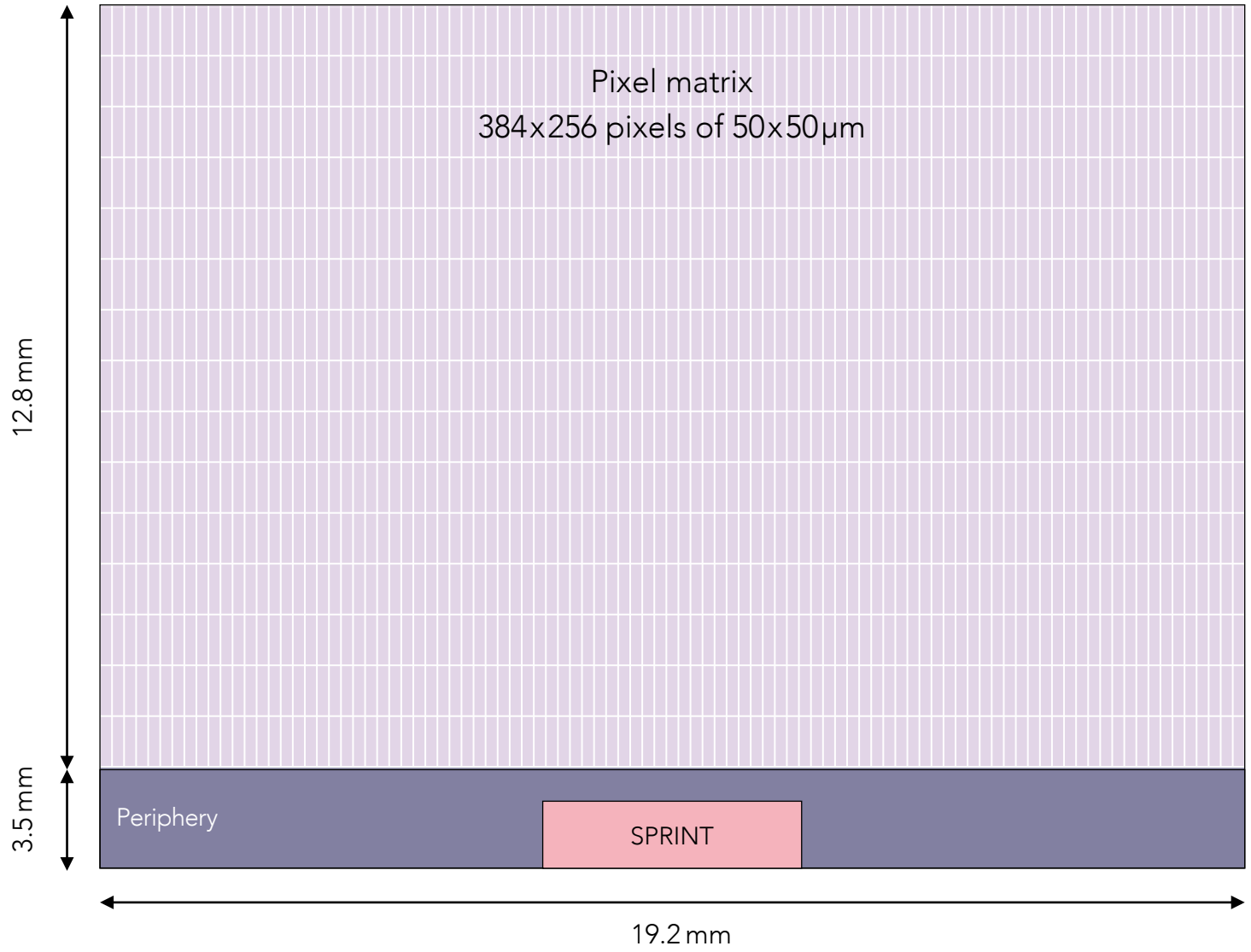
$\sigma^2_{conversion}$ = TDC_{BIN} / $\sqrt{12}$ = ~12ps $_{RMS}$ — Uncertainty of digitalization

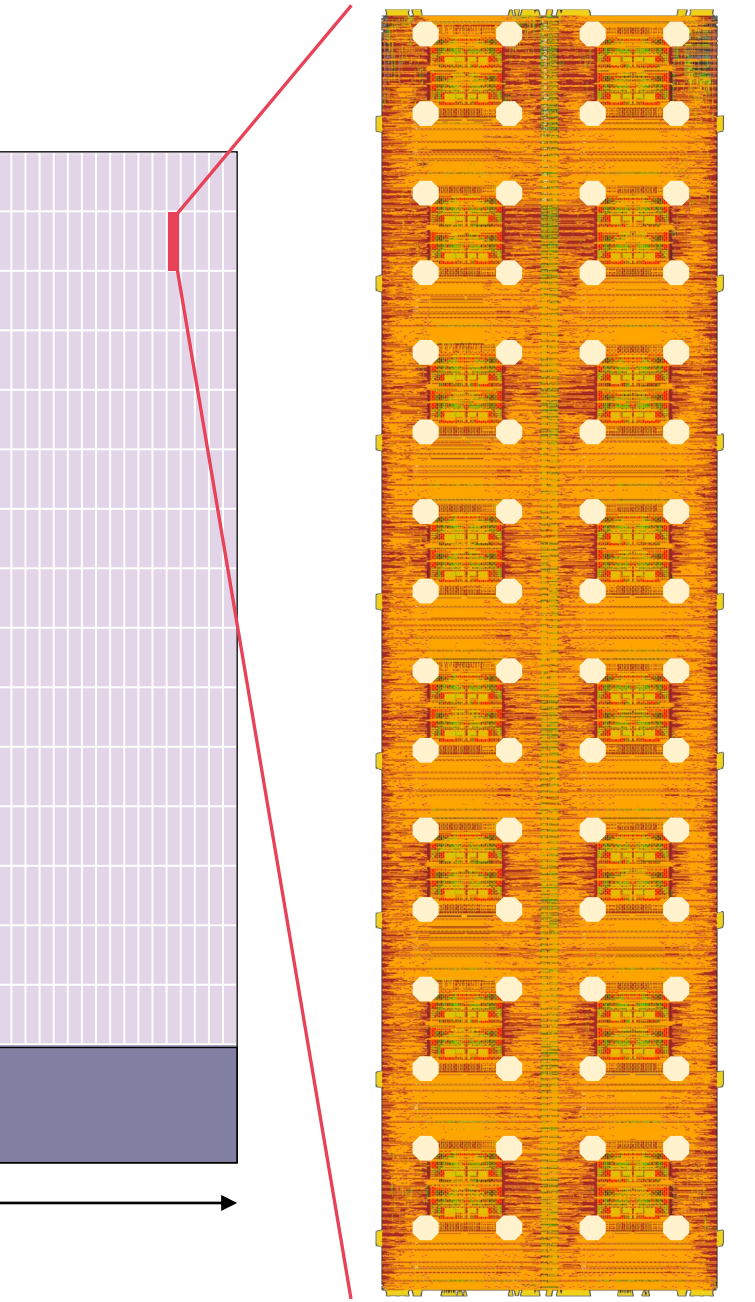
σ^2_{clock} → < ~10ps $_{RMS}$ — Reference-clock jitter at pixel level

$\sigma^2_{analogFE}$ → < ~25ps $_{RMS}$ — Analog Front-End jitter

On a matrix of 98 304 pixels

Picopix floorplan organization



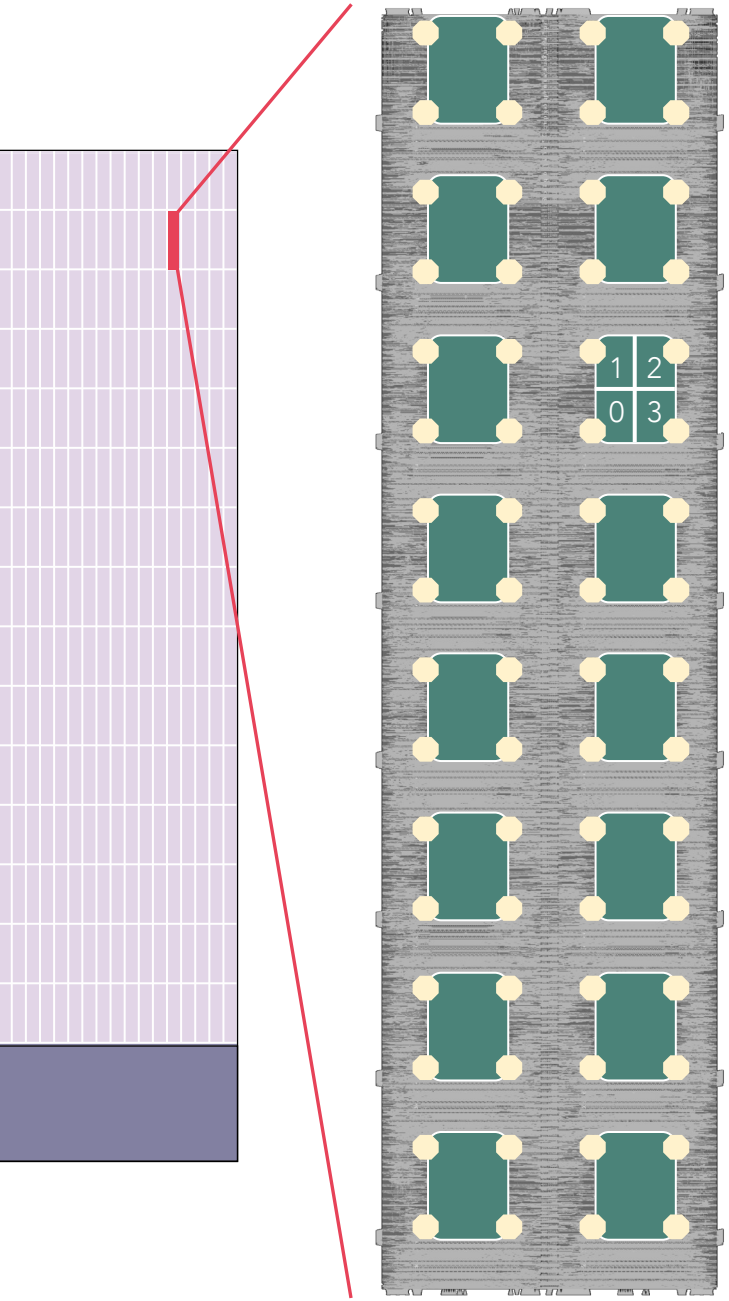


Pixels-Region | 4x16 pixels

- Replicated 16x96 times to form the pixel matrix.
- It Includes:
  - Analog Front-End
  - Clustering logic
  - Configuration regs
  - TDCs
  - DLL refence clock
  - Cluster-Veto logic
  - Calibration SMs
  - Data readout
- Complex physical design and timing closure
  - Fast-control, slow-control and data readout along the column pass through multiple clock domains. Each region has a clock shifted of 1/32 of clock period
  - Digital functionalities in pixel array allow optimizing bandwidth at the source
  - Intensive usage of clock gating and asynchronous logic

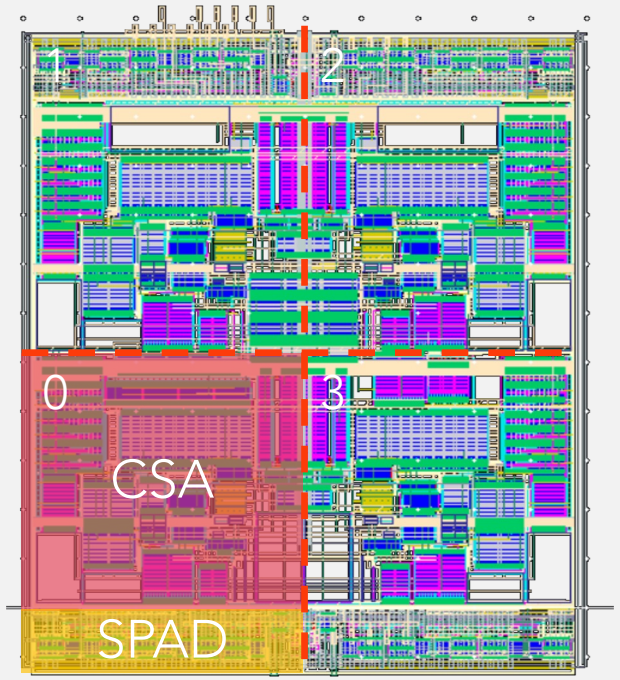
DESIGN COMPLETE

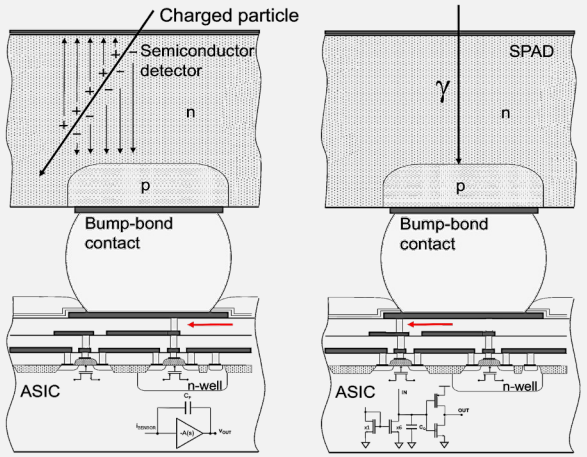
RESPIN <2 DAYS



Analog Front-end

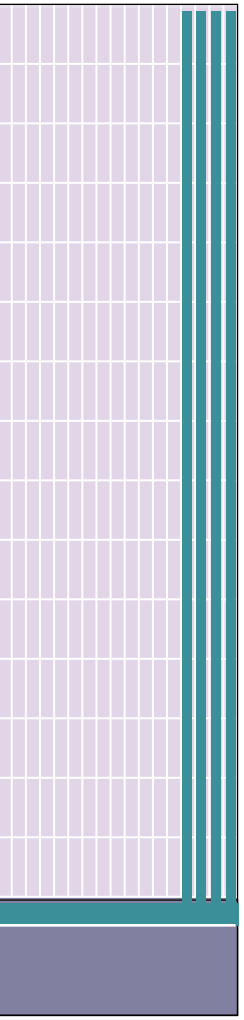
R. Ballabriga, J. Kaplon





- PICOPIX compatible with multiple sensors
- Different front-end circuitry for:
  - No amplification / low-gain: planar, 3D, LGAD
  - High-gain: SPAD (Single Photon Avalanche Diode)
- CSA with Krummenacher feedback
  - Timing optimized for negative polarity sensors
  - 7-bits sub-binary radix DAC
  - ENC < 95e⁻ (100fF input capacitance)
  - $Q_{IN-THR} > 4ke^- \rightarrow$ jitter < $25ps_{RMS}$
- On-pixel biasing power drop compensation
- Bias compensation for drop along pad edge
- Input bump opening size: 10.8um

DESIGN COMPLETE



Minimize Analog Front-End jitter $\sigma^2_{analogFE} < 30\,ps_{RMS}$ means:

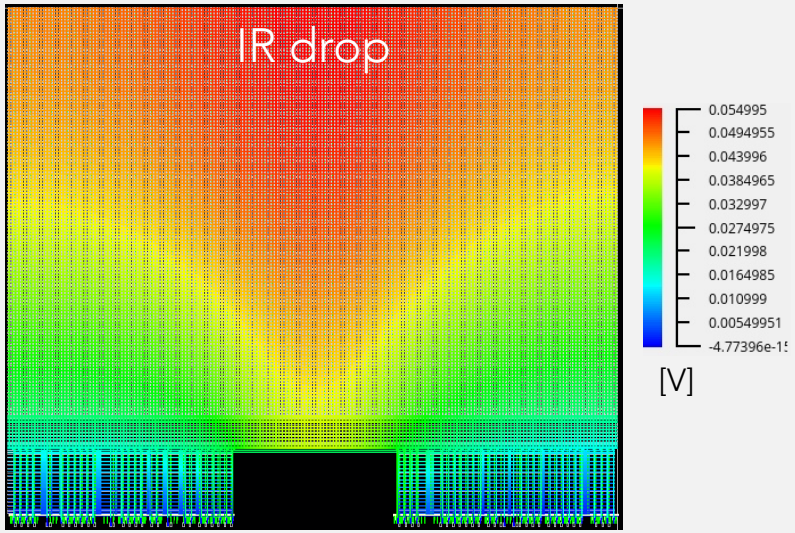
- Minimize input capacitance
- Maximize collected charge
- Optimize minimum threshold
- Maximize signal slew rate at discriminator
- Increase transconductance to improve bandwidth and noise

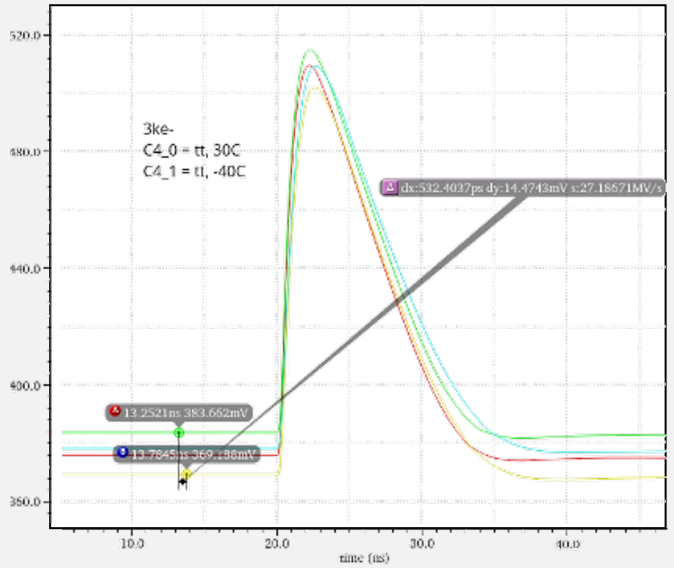
Reduce jitter → Increase g_m → increase power → higher power drop → worsen timing performances!

Study power distribution and account for voltage drops effects is a fundamental for achieving timing performance.

Analog power distribution and analysis

J. Kaplon, L. Timmermans





IR-drop: 25 mV over column (worst case)

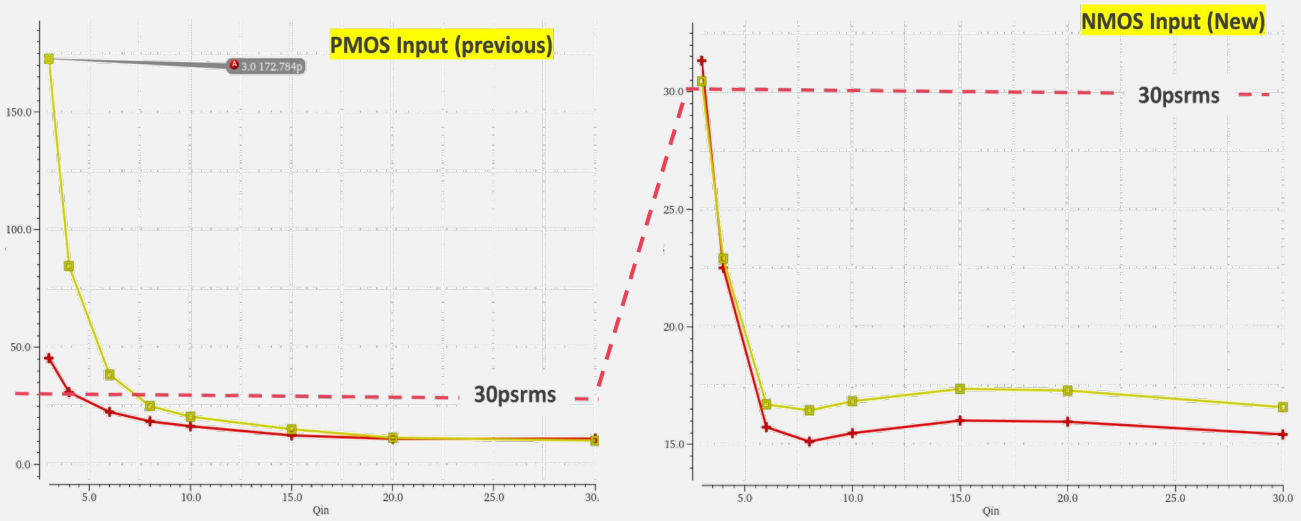
I density: 5.4 µA/µm

Power analysis feed back to analog simulation

Timing performance are maintained within the range.

Very important to check the performance in all corner cases, taking into account the on-chip voltage drop

For example: Identified a limitation of the front-end input stage at -40°C when 70mV drop



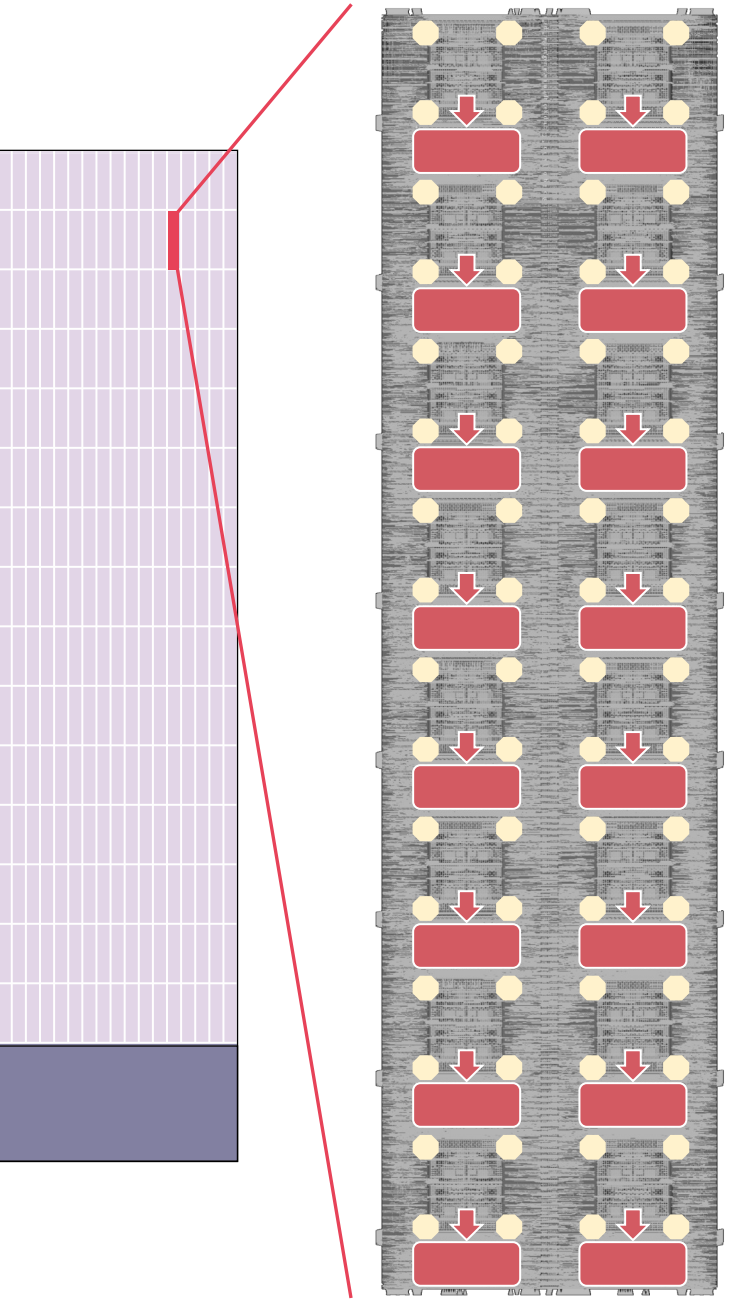
Front-end now corrected

Q_{THR} significantly reduced

$8ke^- \rightarrow <3ke^-$

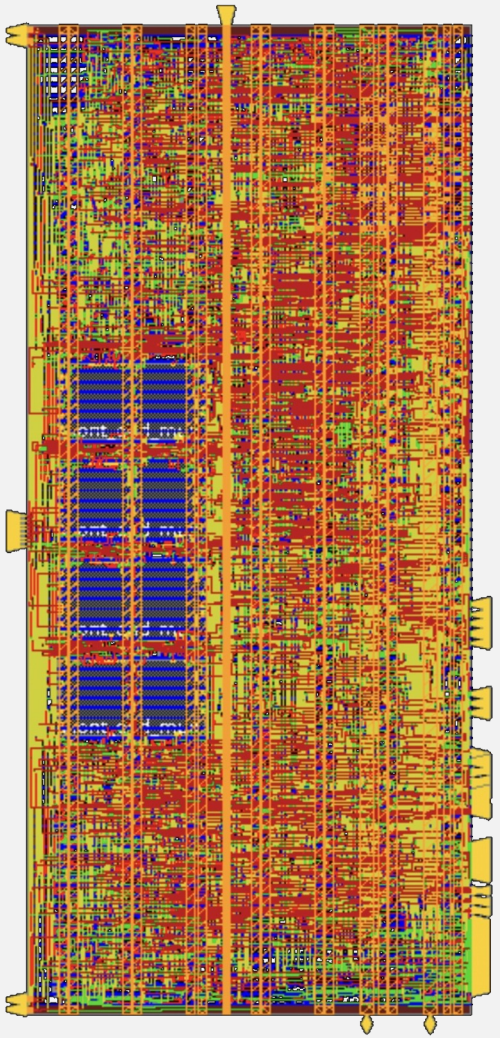
In worst corner at -40 °C and
VDD = (0.9 -10% -70mV drop)

Gain dispersion is restored → ENC is improved → Jitter balanced across corners

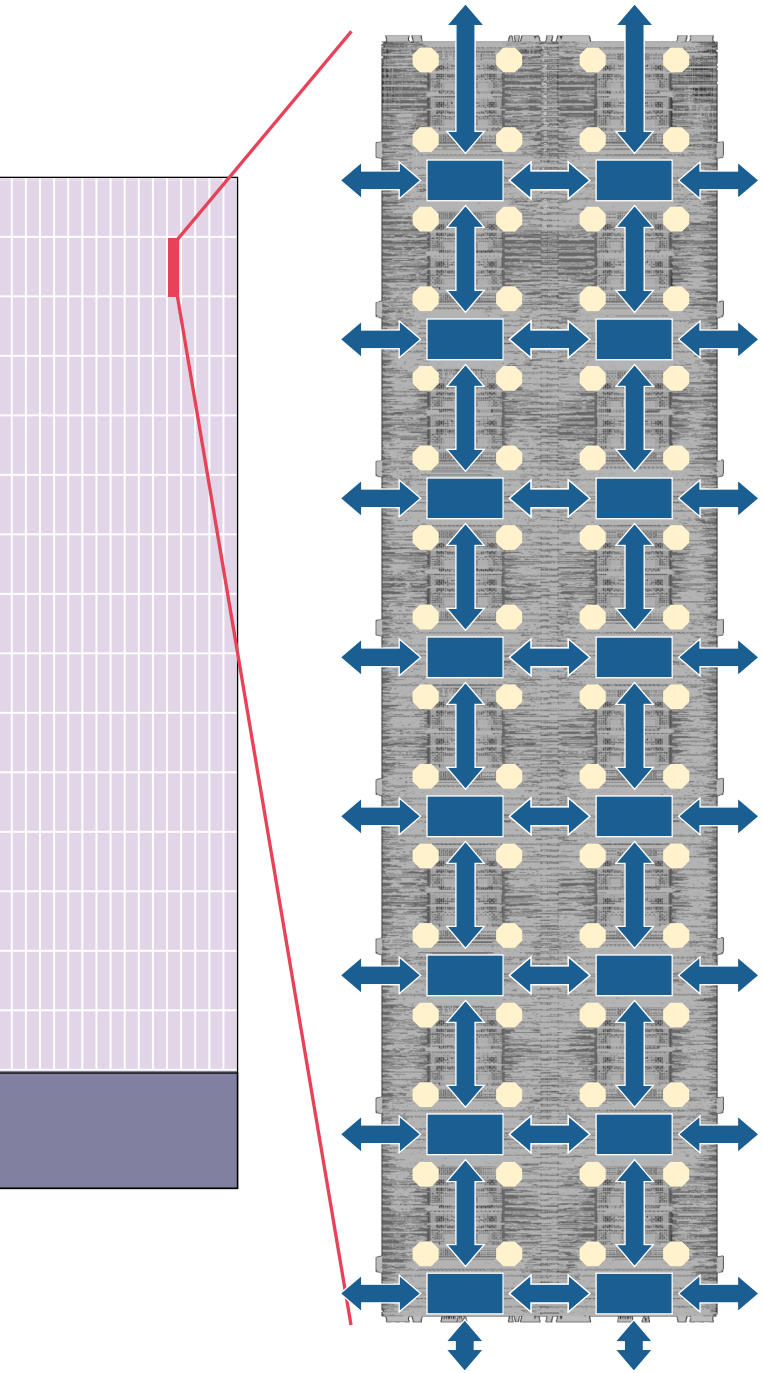


TDC (time measurement)

- Fully digital design based on free-running oscillator
- Ultra-Fine TOA → ~40ps bins
- 1 TDC for super-pixel (4 pixels)
- Digital auto-calibration at each measurement
  compensating P-V-T-Rad and mismatch on a large matrix
- On-chip correction of time reference
- On-chip correction of time-walk errors
- TOT 12-bit resolution per each pixel
  transmitted depending on operating mode
- Variable frequency clock 80MHz to 320MHz
  power vs blind-time
- Calibration pulse can be synchronized locally
  Compensate for propagation time and variability
  Single measurement for AFE time analysis and time-walk

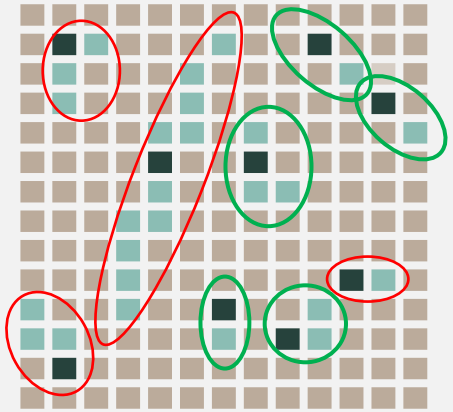


DESIGN COMPLETE
RESPIN IN <1 DAY

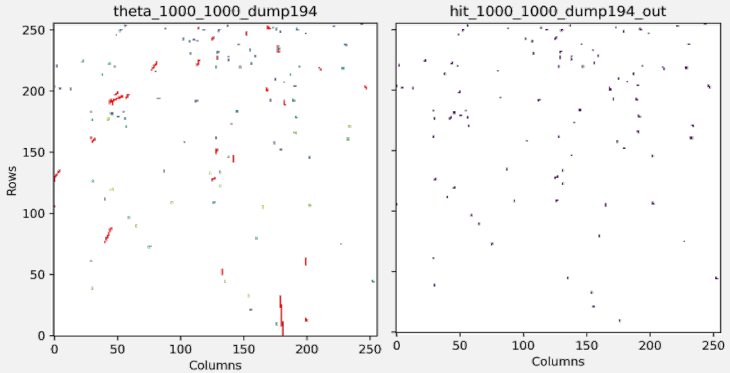


On pixel-matrix clustering and data reduction

- On-pixel clustering and ToT arbitration:
  - Single data-packet per cluster (can be disabled)
  - Cluster centroid → pixel with highest charge
  - Time of arrival only on the centroid pixel
  - For surrounding pixel can be transmitted: a binary Hit-Map or the ToT



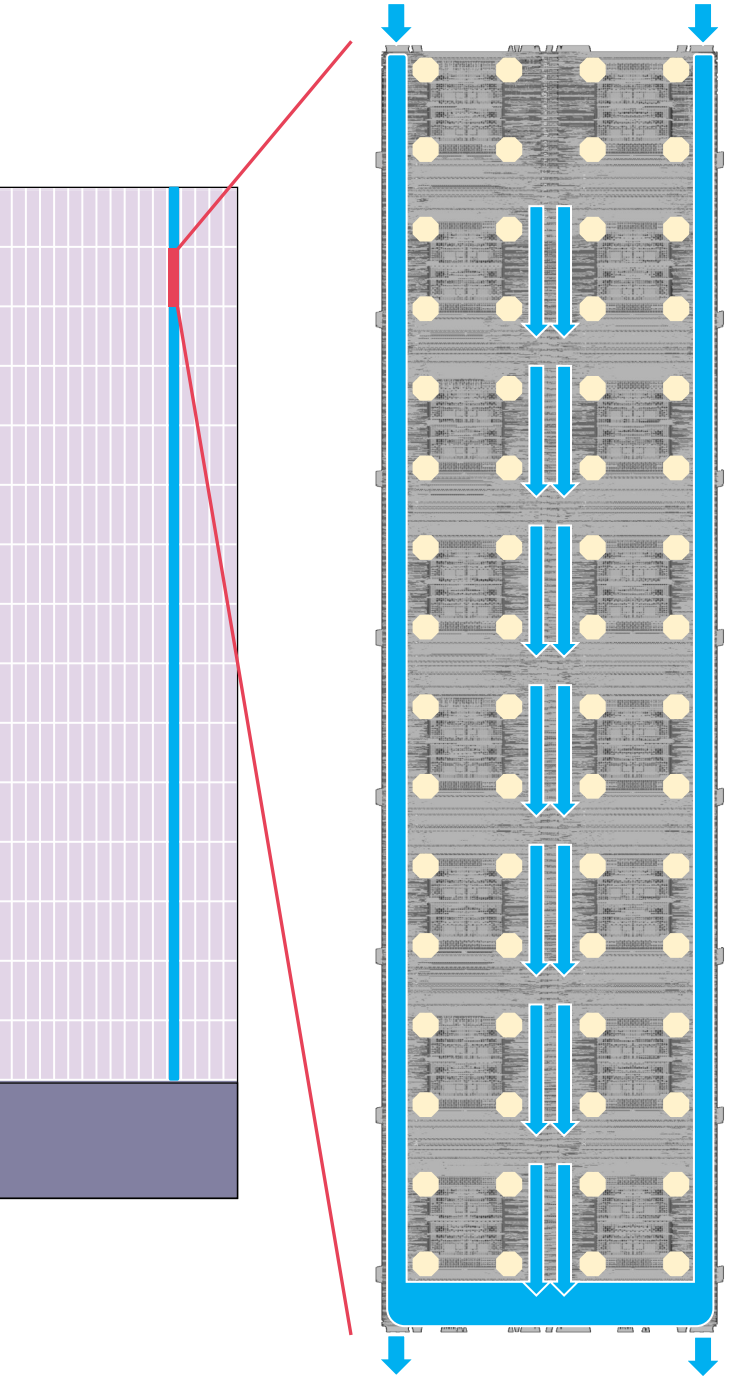
- Cluster filtering in pixel array:
  - Cluster size (small/large clusters)
  - 2 threshold ToT



Filtering disable | Filtering large clusters

- Cluster filtering in periphery:
  - ToT range / ToA range
  - Cluster shape / and others

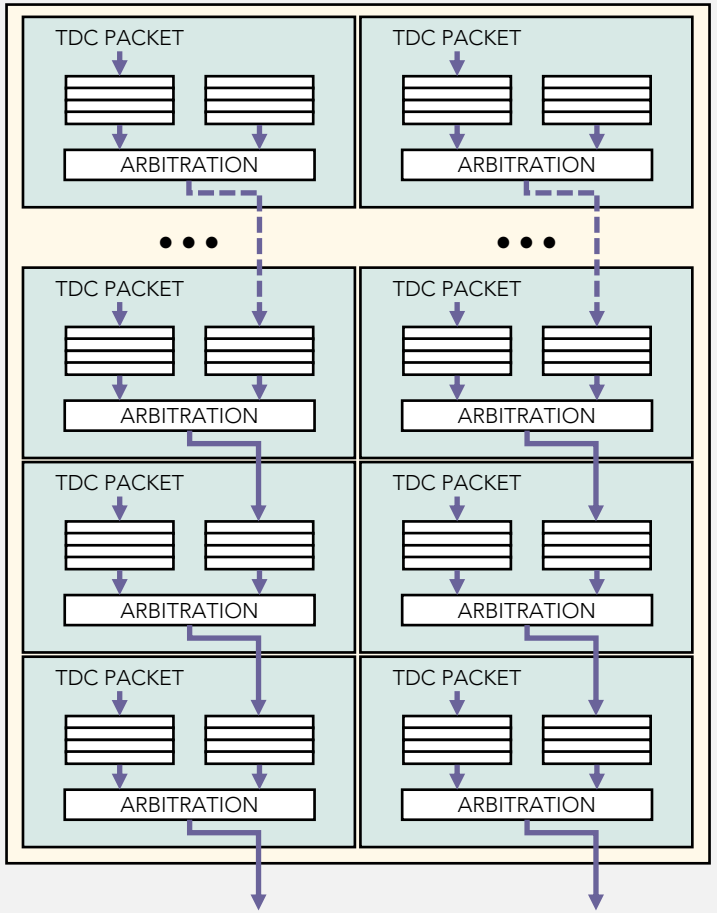
DESIGN COMPLETE



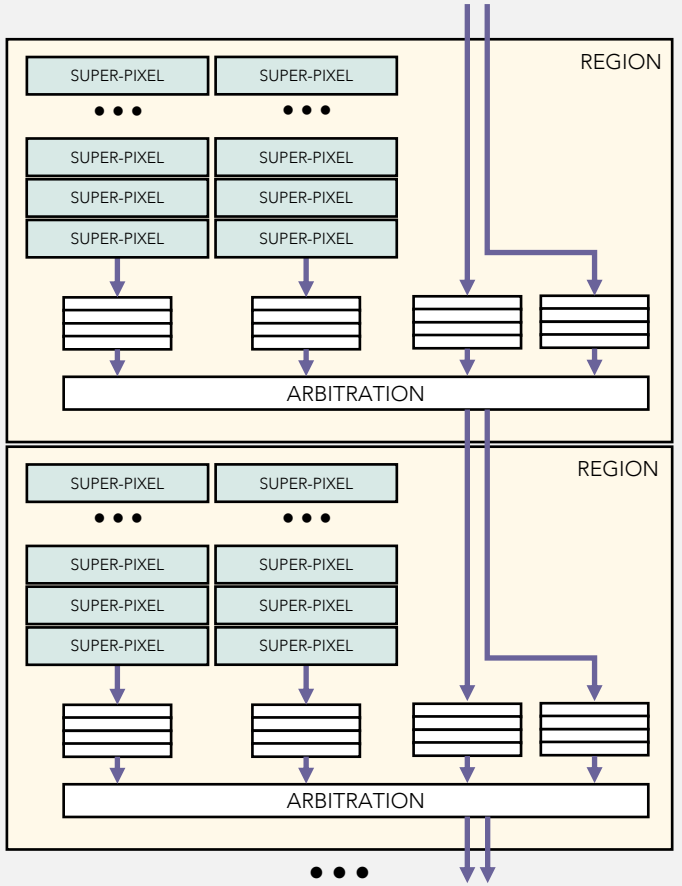
Data readout

- Readout by super-pixel, then jump by region: optimize latency

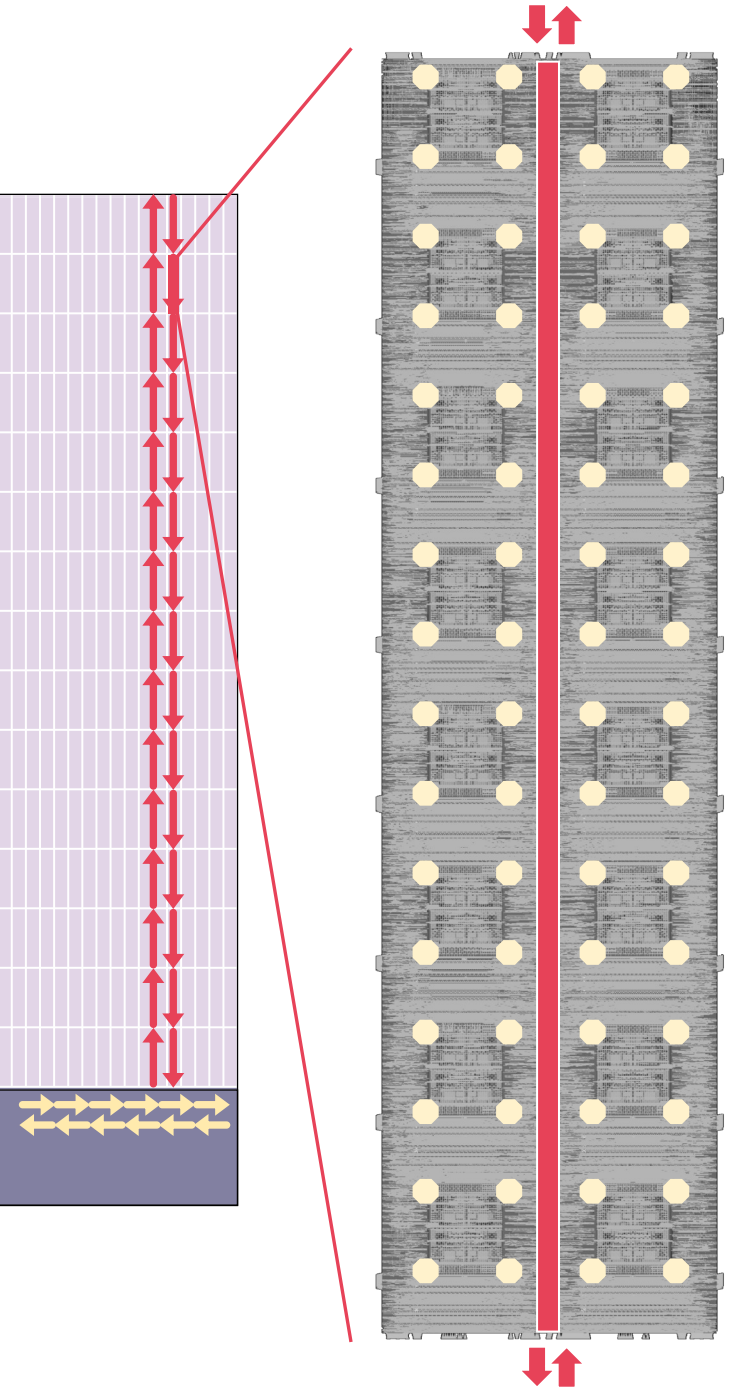
PIXEL REGION 4 x 16 pixels



PIXEL COLUMN 16 regions

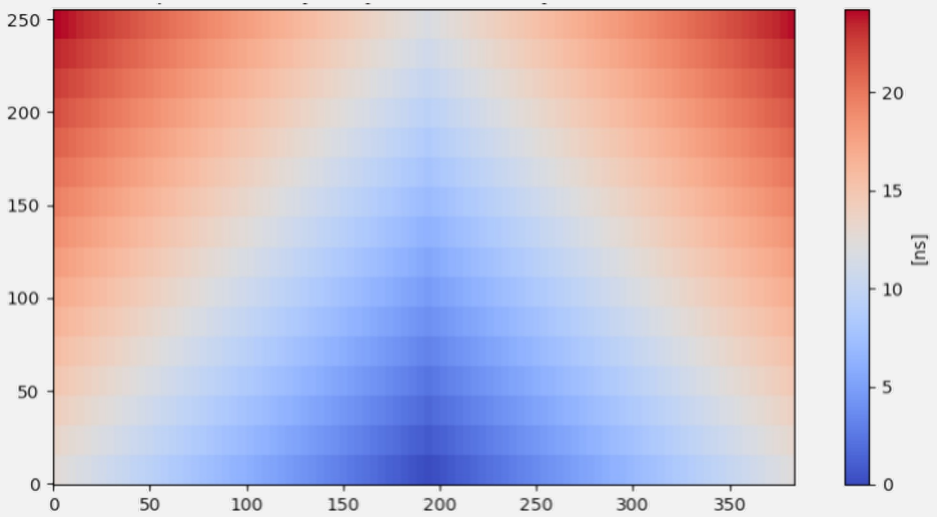


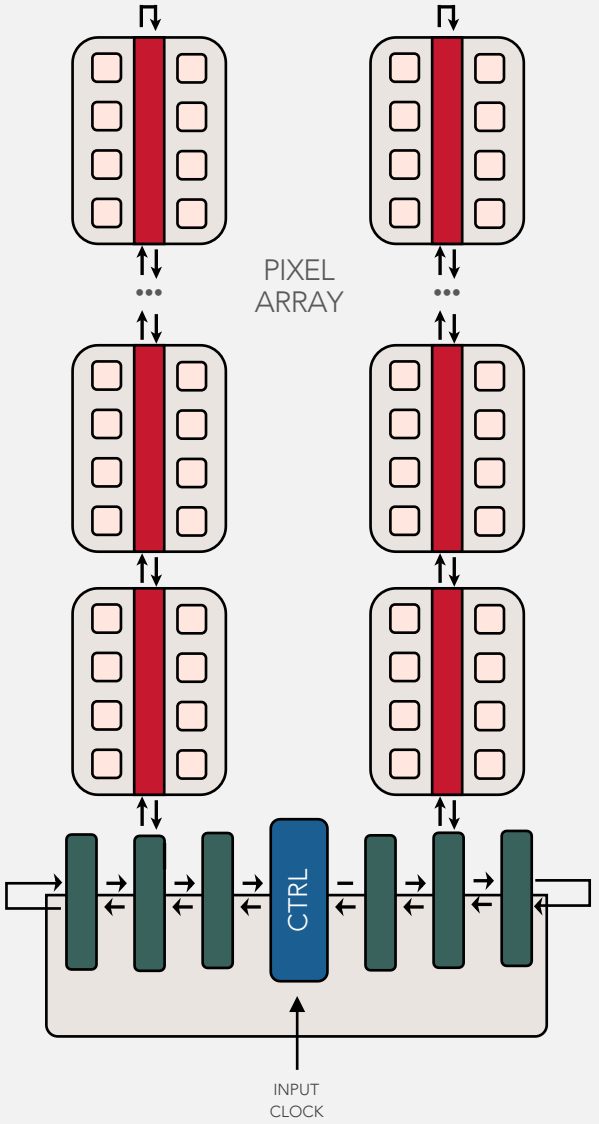
DESIGN COMPLETE

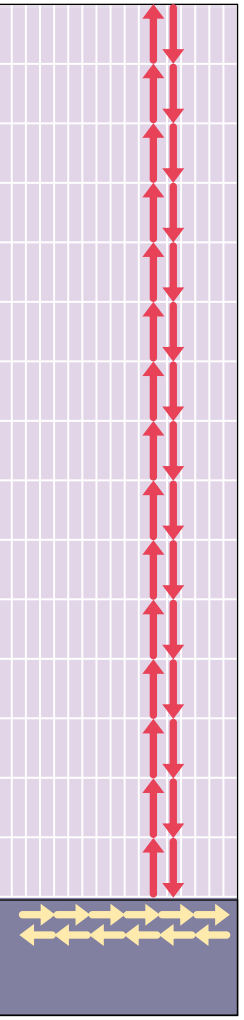


Full-chip controlled clock skewing through DLLs

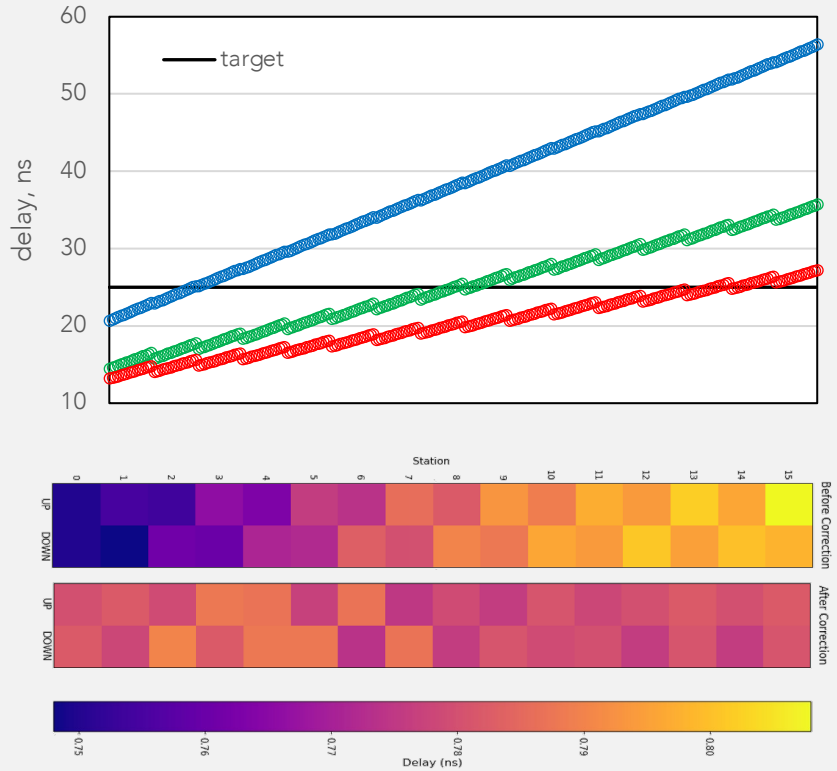
- 2 horizontal and 96 vertical DLLs.
- Control of clock phase with 3-5ps skew.
- Tracks Voltage – Temperature – Rad variations.
- Trimming for mismatch and voltage drops.
- TDC reference clock 320MHz | 160MHz | 80MHz
- Quasi-static consumption and voltage drop reduction







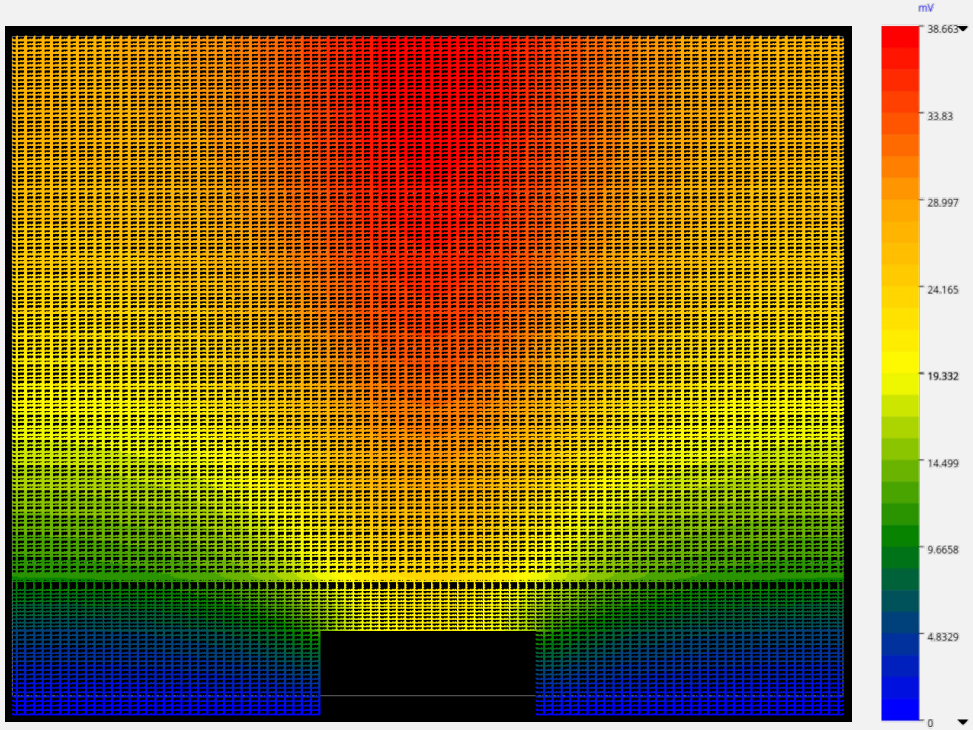
- Minimize Reference-clock jitter at pixel level
- Lock on target value for all design corners

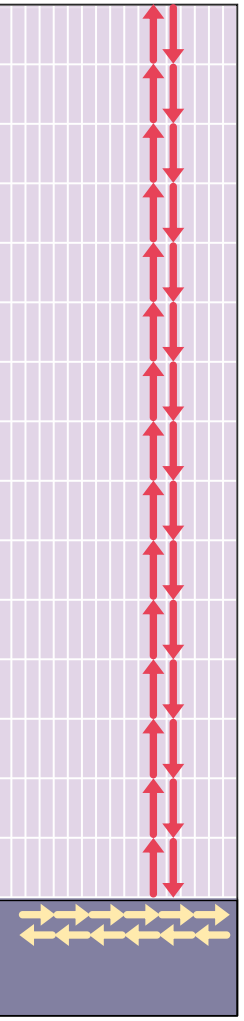


- IR drop studies on implemented DLL (full chip)
- Static IR drop at 160MHz: ~35mV in each column

  Analysis conditions: 0.9V, TYP w/ RCWORST extraction

  IR drop at 320MHz roughly doubles | at 80MHz roughly halves

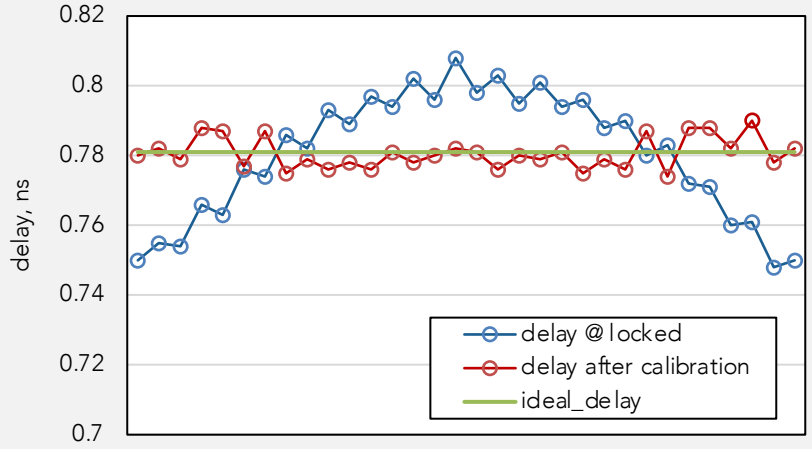




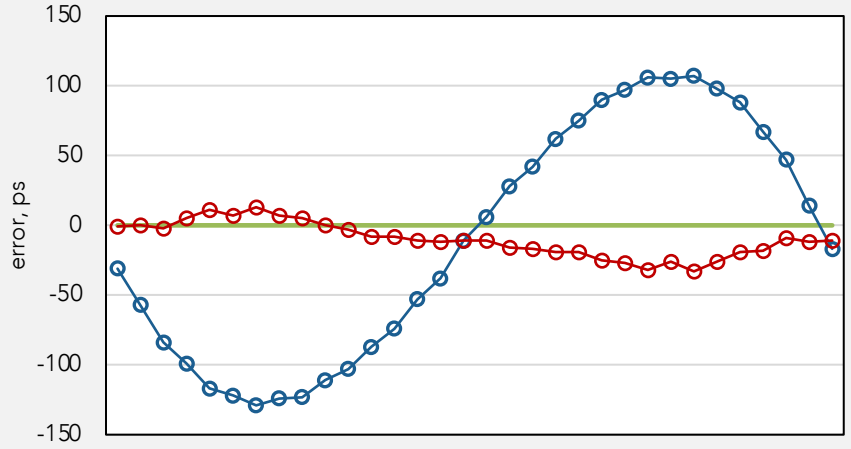
- Power drops (same as TID effects) and mismatch effects on delay cells are such to create large INL of the reference clock arrival time to the pixels TDC. If not corrected, is a very large timing error
- Autocalibration mechanism allow trimming each delay cell for IR-drop and mismatch correction

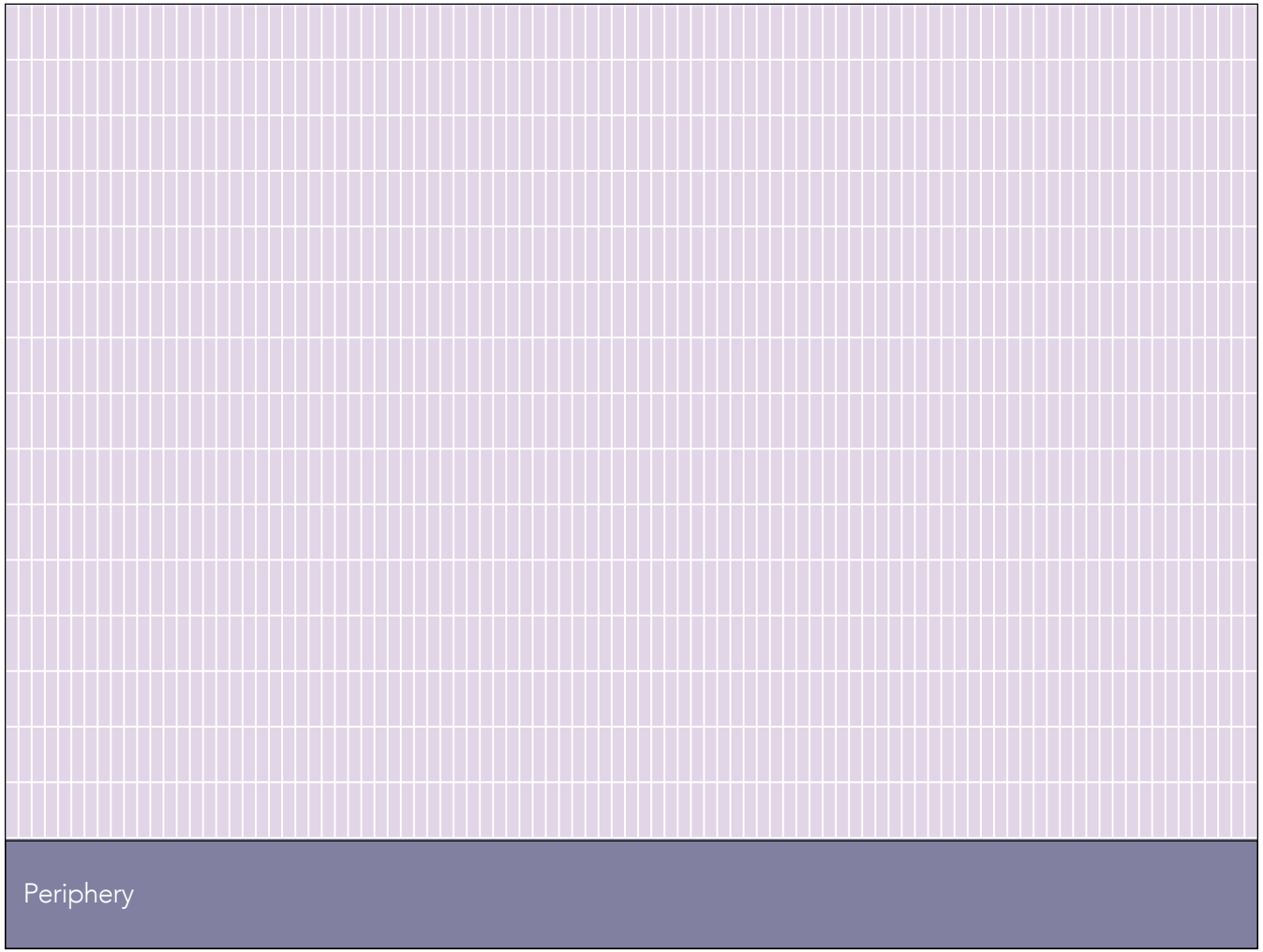
  Possible control via Slow-Control or via the RISC-V microcontroller
- IR drop analysis information used in analog simulation, and values extracted from analog simulation annotated back into digital for full chip timing analysis

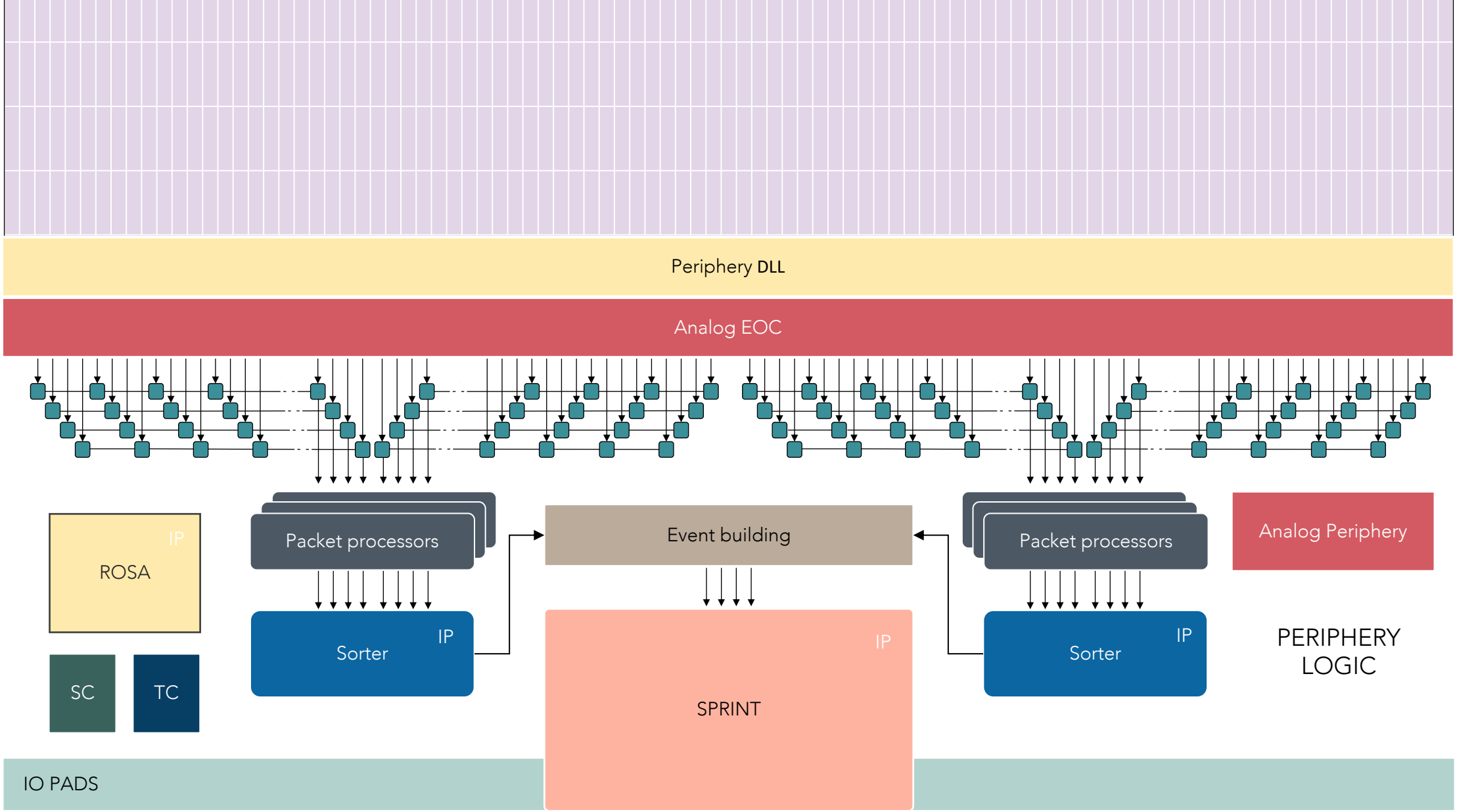
DLL stations delay at lock



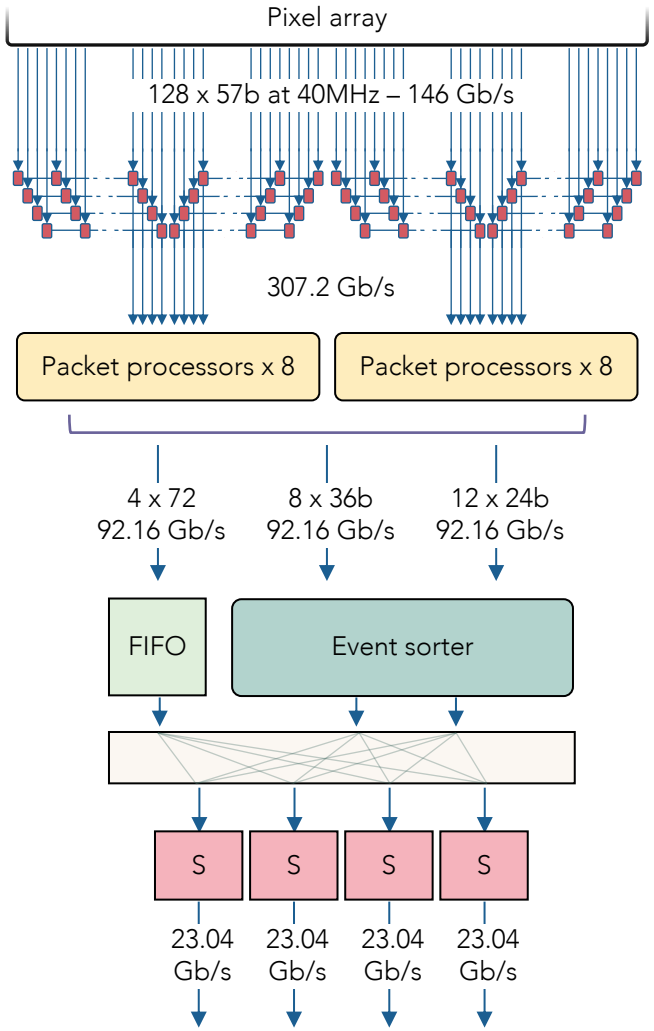
Arrival time error




Periphery


Periphery DLL
Analog EOC
IP
ROSA
SC
TC
Packet processors
Sorter
IP
Event building
IP
SPRINT
Packet processors
Sorter
IP
Analog Periphery
PERIPHERY
LOGIC
IO PADS

Periphery readout data-path



Digital End-of-Column

- Handle transmission of data packets from pixel array towards the packet processing units.
- Handle slow-control serial bus towards pixel-columns

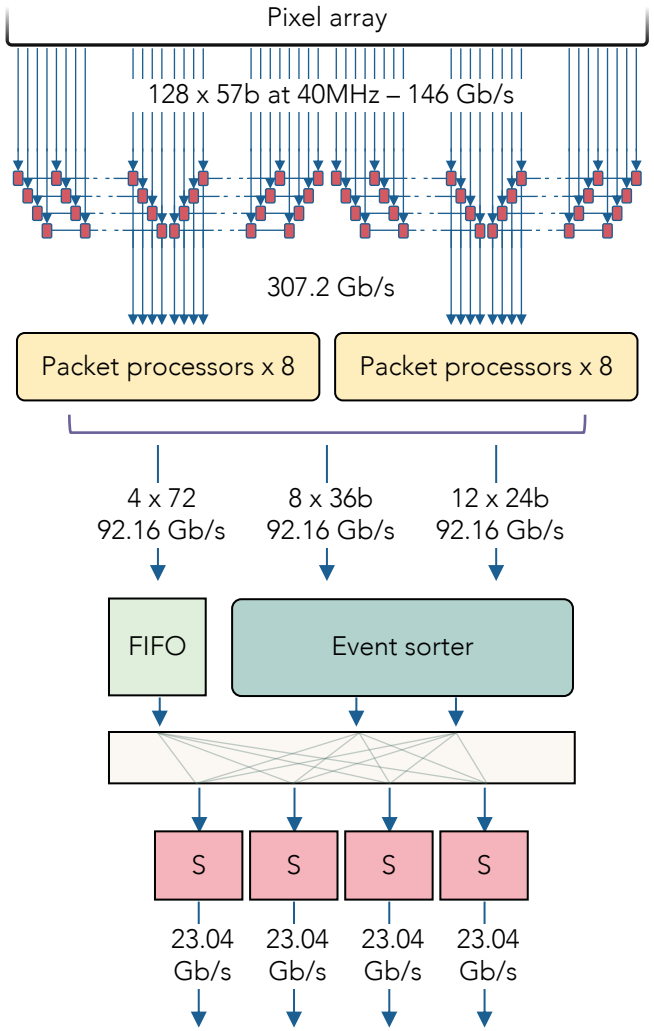
RTL COMPLETE – P&R COMPLETE

Analog End-of-Column

- Distribute bias and compensate for drop along distribution

DESIGN COMPLETE

Periphery readout path

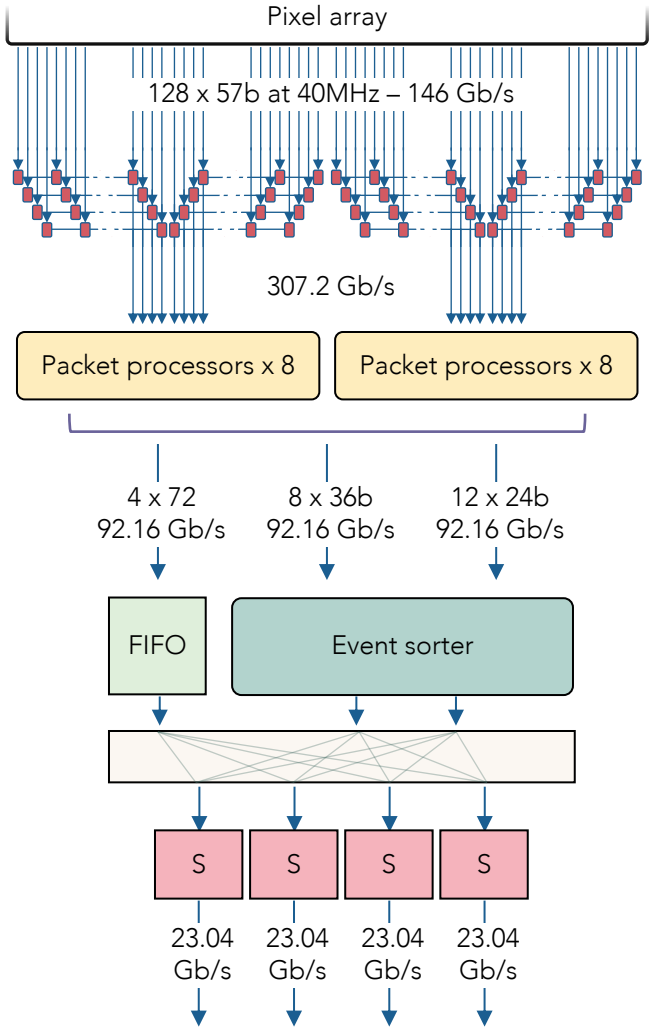


Packet processors

- Full Time calibration: TOA corrected without requiring any per-channel calibration outside of the chip
  - Clock skew calibration (Row and Column)
  - Unique time-walk correction (Based on TOT info)
  - TOA event calibration (24.4ps bin)
  - 10b or 6b fine-time output
  - Digital T0Sync shift adjust (24.4ps bin, 100ns range)
  - Built-in TOA extender up to 32-bits at 40MHz
- Event Filtering
- Build event packet 72b mode | 36b mode | 24b mode

RTL COMPLETE – P&R COMPLETE

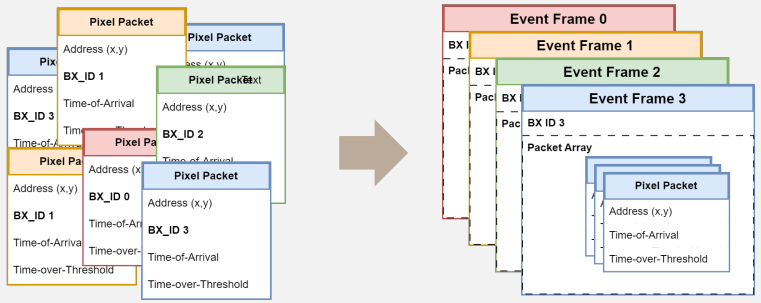
Periphery readout path



Events sorter

Francesco Brambilla

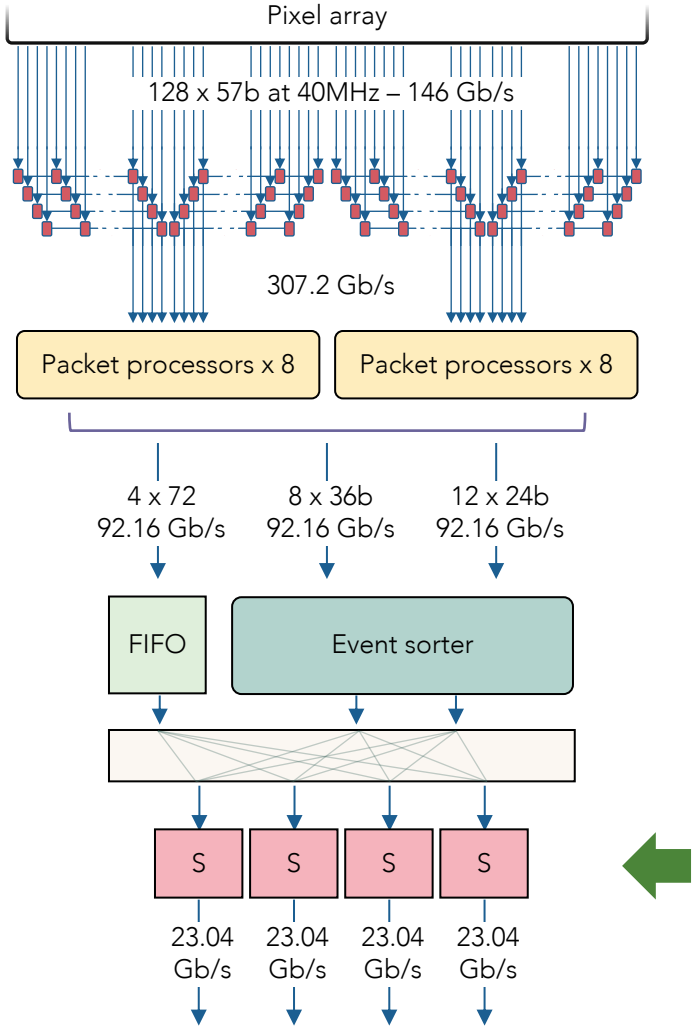
- Reorders the packets into frames containing data from each event



- Lossless if average occupancy < 60 clusters per event
- Event-ID (BX) in frame header (significant bandwidth optimization)

80% COMPLETE

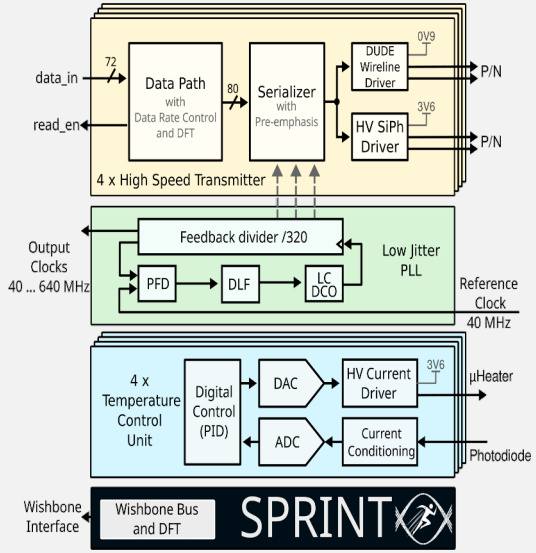
Periphery readout path

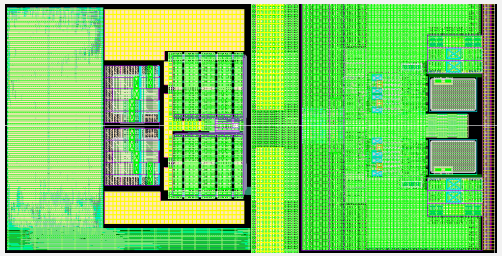


SPRINT – Silicon Photonics Radiation-tolerant Integrated Transmitter

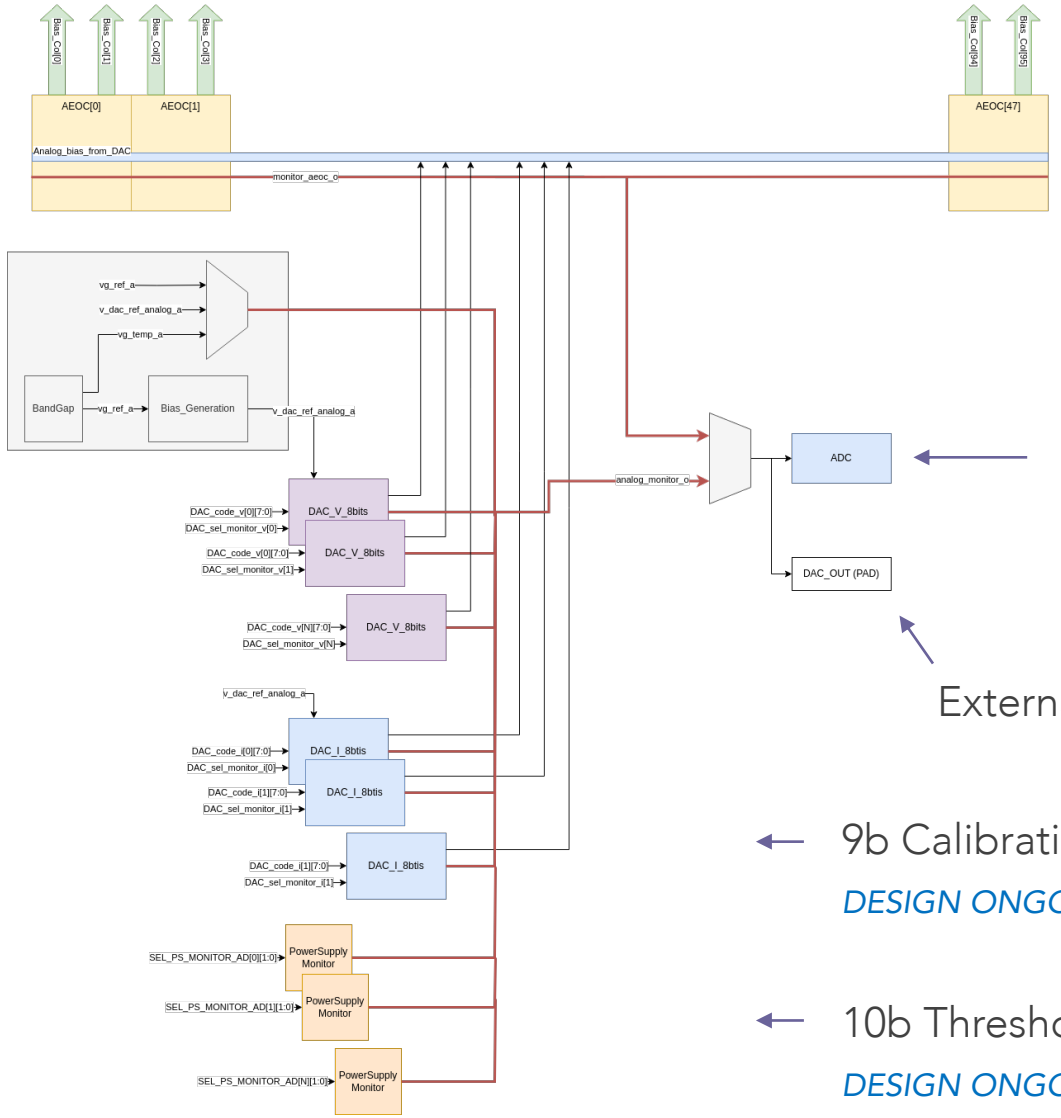
S. Kulis - S. Biereigel - G. Atzeni - G. Ciapri - T. Daros

- High-speed output interfaces:
  - Electrical: up to 4 x 12.8 Gb/s
  - Optical: up to 4 x 25.6 Gb/s (with SiPh IC and 3.6V supply)
- lpGBT-like frame and FEC: correct up to 30 bits
- Status:
  - High-voltage SiPh modulator driver: *READY*
  - High-speed serializer with pre-emphasis: *READY*
  - Electrical driver: *READY*; low-power variant *ONGOING AT NIKHEF*
  - Clock-generator subsystem (full-custom): *ADVANCED STATE*
  - Temperature control unit components: *IN LAYOUT PHASE*
  - Digital features: *RTL READY*
  - Functional verification: *NEARLY COMPLETE*
  - SEE verification (full-custom and digital): *ONGOING*





Analog periphery



Analog End-Of-Column

Bias compensation for drop along distribution

DESIGN COMPLETE ***(Jan Kaplon)***

Monitoring ADC

DESIGN COMPLETE ***(IP from external company)***

Prototype on MPW the 21st April 2024

External test pad

9b Calibration/Threshold DAC

DESIGN ONGOING ***(Rafael Ballabriga)***

10b Threshold DAC

DESIGN ONGOING ***(Sylvia Wong - NIKEF)***

Synchronous-control and slow-control

TFC Unit — Federico De Benedetti

- Fast command decoder and distribution
- Following LHCb VELO U2 specifications
- Synchronous to independent clock domain

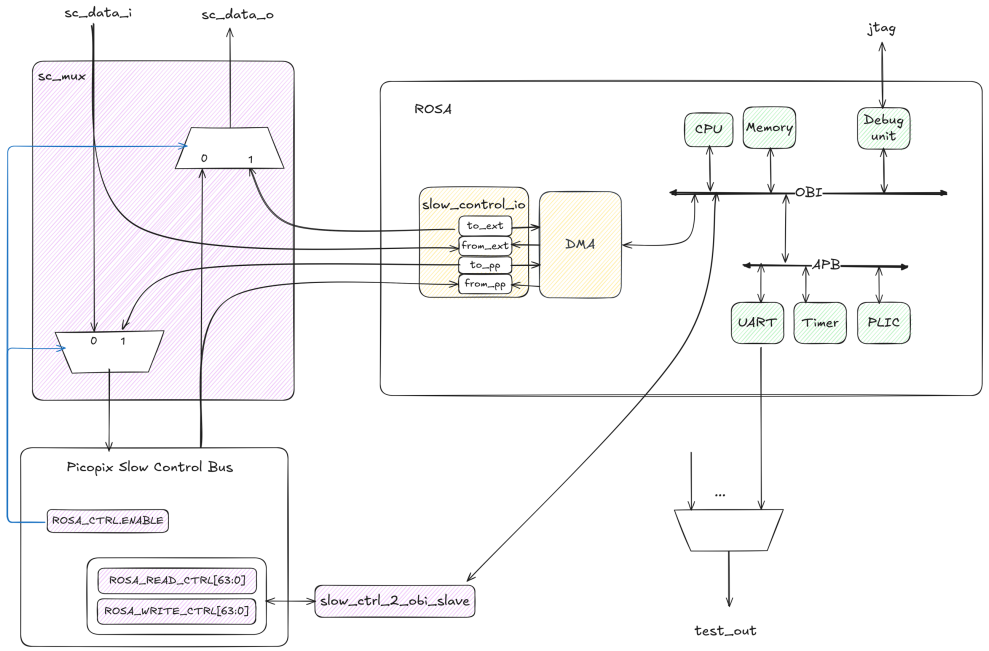
HEADER	2:0	3'b101
SHUTTER	3	1: Shutter Opened; 0: Shutter Closed
SYNC	4	1: Sends sync packet
CAL	5	1: Start Test Pulse calibartion
RESET	6	1: FE Reset (Configurable)
BX_RESET	7	1: BXID Reset

Independent and fully-asynchronous ports

Slow-control

- Custom serial control protocol
- Same as in Medipix4 and Timepix4
- Scripted generation of configuration registers
  - Instantiate and route registers in RTL
  - Generate documentation
- Parallel bus in periphery
- Serial bus in pixel-column
- Independent clock, up to 160 MHz

On-chip RISC-V Microcontroller

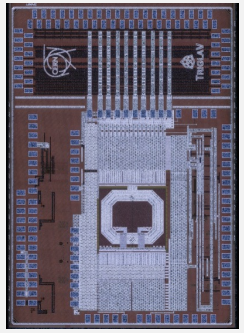


RISC-V On-chip Slow-control Accelerator (ROSA)

Marco Andorno, Benoit Denkinger, Adrian Fiergolski

DESIGN ONGOING

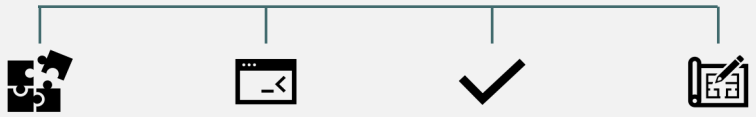
- Taps slow control
- Can extends slow control capabilities
- Algorithm set at runtime
- Automatize on-chip recurrent operations:
  - Threshold equalization
  - Trimming of distributed clock DLL
  - Tuning of Photonics IC Temperature Control
  - Calibration of the BIAS voltages



Based on TRIGLAV, a radiation-tolerant microcontroller prototyped and tested in 2025

Marco Andorno, Benoit Denkinger, Alessandro Caratelli, Davide Ceresa, Kostas Kloukinas, Anvesh Nookala

Generation via SOCRATES: A toolset for automatizing system-on-chip hardware and software development



PICOPIX operating modes

Data-driven

- For tracking applications
- A data packet is generated for each event
- TOA → $30\,ps_{RMS}$
- On-chip time-correction
- On-chip time-walk correction
- On-chip auto-calibration
- On-chip clustering / filtering
- On-chip packets sorting

Frame based

- For imaging applications
- Counting particles hits when the shutter is open
- Zero-suppressed readout
- ~Continuous readout window

Data-driven (tracking) operation

Packet type	Size	Sorted	Calibrated UF-TOA	Coarse TOA (Bx)	Ultra-Fine TOA	Hit-Map	Additional fields	Max rate (clusters/s)
Tracking Short	24b	✓	✓	* 16b	5b	–	• Sub-pixel Address • TOT [1b] + Pileup flag (P) • TOT [2b]	3.84 $\cdot 10^9$ cl/s
Tracking	36b	✓	✓	* 16b	9b[1] 10b[2]	✓	• TOT [1b] + P • TOT [2b][1] / [1b][2]	2.56 $\cdot 10^9$ cl/s
Tracking Extended	72b	✓	✓	* 16b	10b	✓	• TOT [9b] (all pixels) + P	1.28 $\cdot 10^9$ cl/s
Tracking Unsorted	72b	–	✓	28b	10b	✓	• TOT [9b] (master) + P	1.28 $\cdot 10^9$ cl/s
Tracking Jumbo	144b	–	✓	32b	10b	✓	• TOT [12b] (all pixels) + P	0.64 $\cdot 10^9$ cl/s
Raw	72b	–	–	14b	10b	✓	• TOT [8b] (centroid)+ P	1.28 $\cdot 10^9$ cl/s
Raw Jumbo	144b	–	–	14b	10b	✓	• TOT [12b] (all pixels) + P	0.64 $\cdot 10^9$ cl/s

Frame-based (imaging) operation

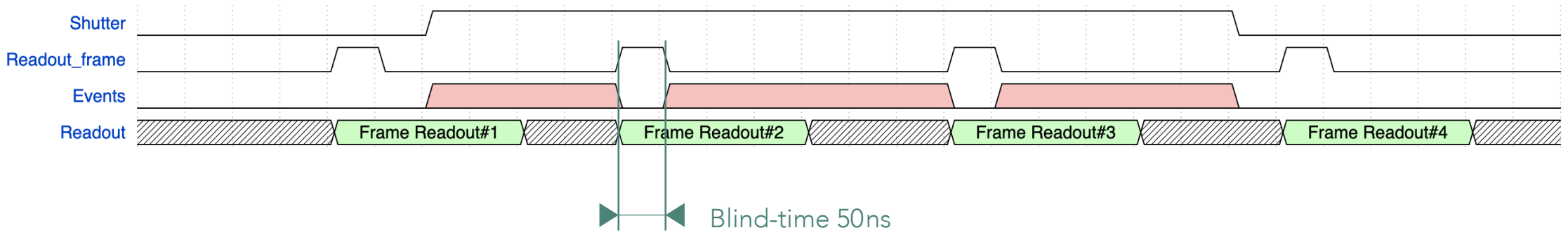
Accumulates the particle counts of each event when the shutter is active

Programmable shutter: Duration, Repetition

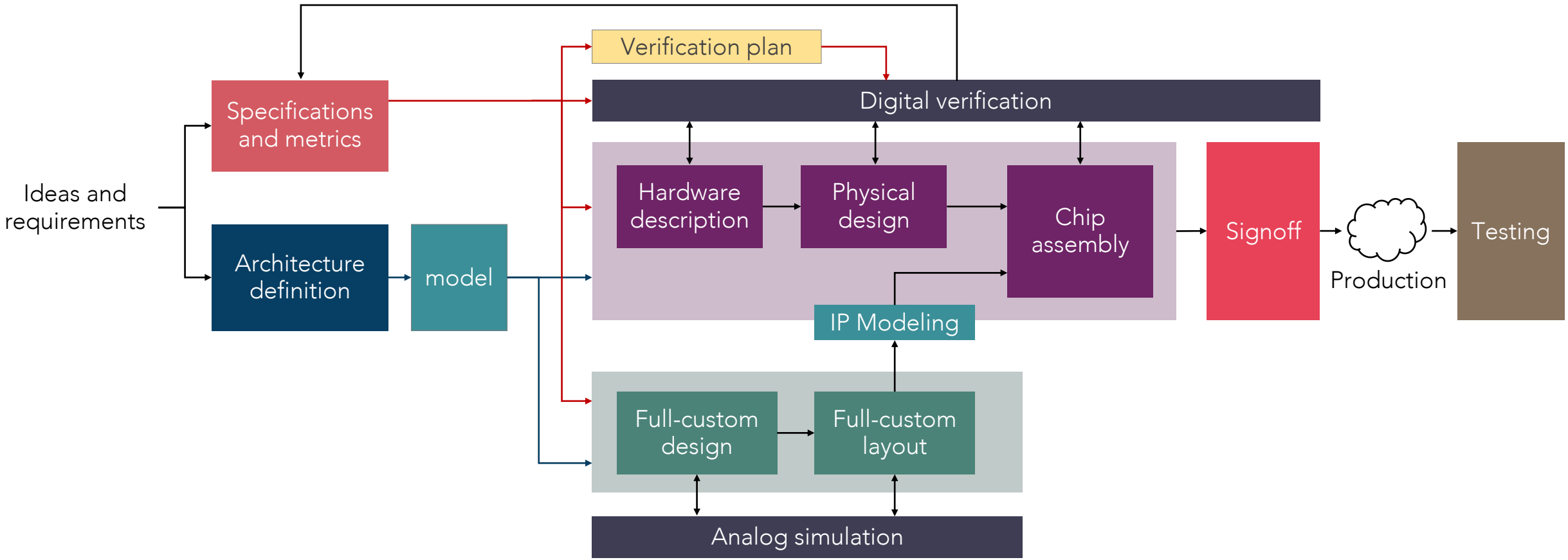
Frame-based readout can be initiated by:

- Automatic at end of shutter-opening period
- Dedicated command (TFC interface)
- Asynchronous trigger (dedicated pin)

Readout can be initiated during active acquisition approximating a Continuous Readout Window



PICOPIX design flow



SEE hardening

SEE hardening strategy

- Full-TMR in control and state-machines
- Data path not protected
- Triplicated clock-tree in periphery and locally in pixel region
- Triplicated configuration latches with asynchronous error signal to update value
- State encoding and auto-reset in SMs without a triplicated clock
- Gated logic outputs isolation and reset at clock enable
- Hamming encoding in ROSA
- Glitch filters on asynchronous resets

Physical implementation

- Instantiate triplicated FF/latches: 10µm
- Spacing for clock and reset buffers: 5µm

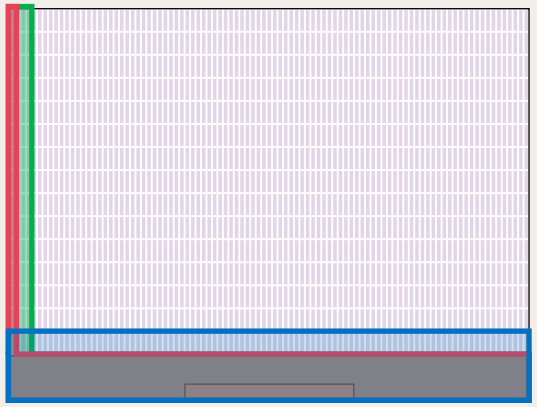
Checks

- SEU and SET injection simulation
- Various scripts to check that:
  - placement distance
  - voters connection
  - logic optimization
  - clock-tree separation

Verification

Matteo Lupi | Simone Scarfì | Adithia Pulli

DUV variants for simulation



- Periphery + 1 region
- Periphery + 1 row
- Periphery + 1 column
- Periphery + 4 columns
- Full chip

IP blocks handling

- IPs verified standalone (SPRINT, ESB, ROSA, etc)
- Only integration tested in Picopix

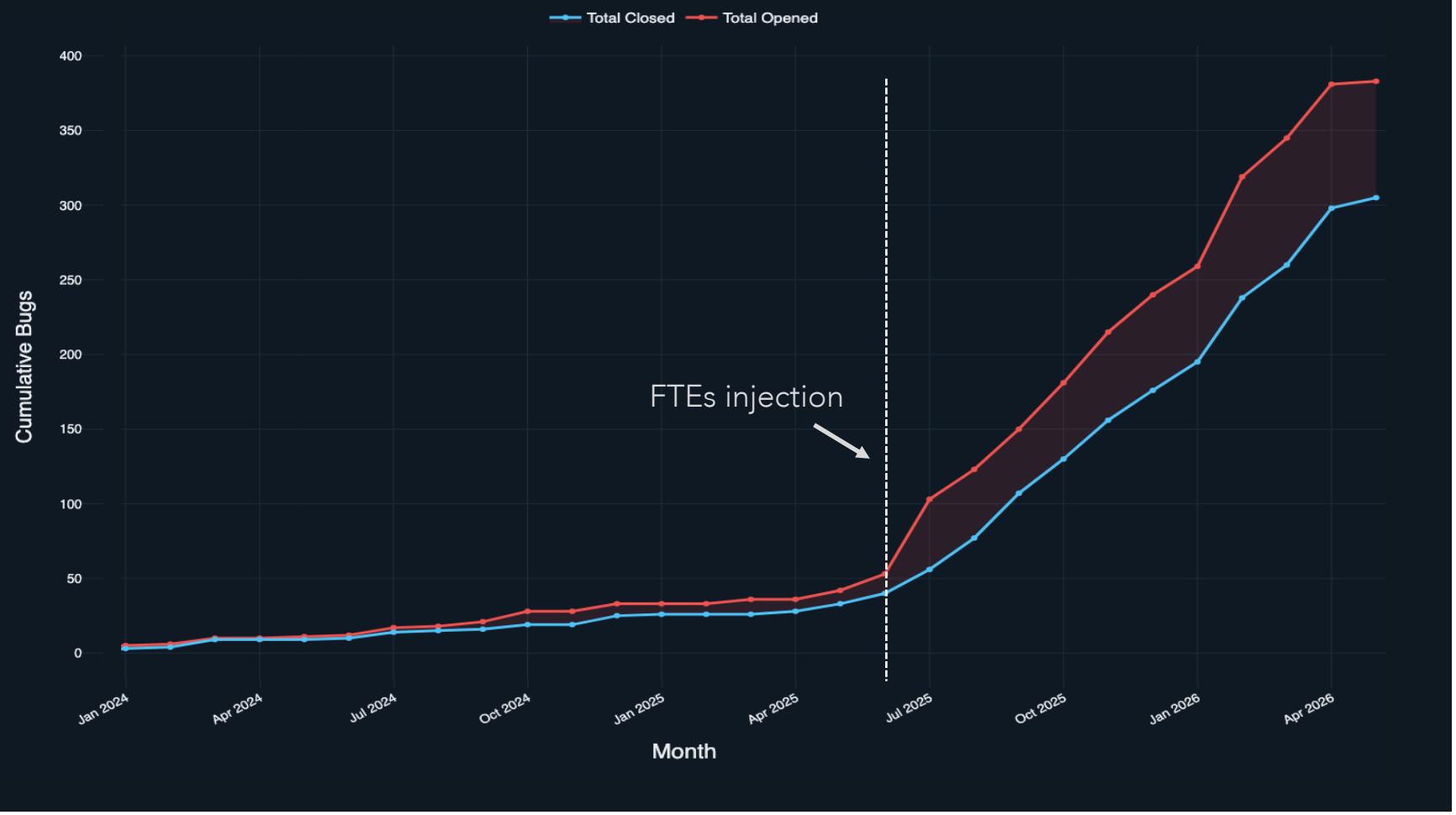
Test classes

- Slow-control tests: *READY*
  - Random ▪ Opcode ▪ Bit Bash ▪ Watchdog
- Readout tests *ONGOING EST. ~16 WEEKS*
  - TOA: random hit are injected checking the TOA
  - HIT: Stress the readout and uses an approximate scoreboard
  - TP: test pulses are injected and read out
  - PC: the ASIC is configured to run in the Imaging mode
- Auxiliary features tests: *ONGOING EST. ~8 WEEKS*
  - TFC Lock ▪ TFC random ▪ DLL locking ▪ E-Fuses
  - DLL stress test ▪ Data Fabric Injector ▪ Threshold Scan
- SEE injection *ONGOING*
- Analysis: *ONGOING*
  - TDC Resolution ▪ Readout Performance ▪ Latency ▪ etc.

Verification

Matteo Lupi | Simone Scarfì | Adithia Pulli

Design bug tracking



Sign-off checklist

1. Functional correctness

Ensure the design still does what was intended according the specifications and requirements

- Full-chip functional verification
- Reset and initialization verification
- Power-up sequence
- Clock-domain crossing (CDC)
- Reset-domain crossing (RDC)
- Metastability risk review
- X-propagation / unknown-state analysis
- Functional and code overage closure
- Bug closure/waiver review with colleagues

2. Timing correctness

Static timing analysis across all process / voltage / temperature / radiation corners and modes

- Setup timing
- Hold timing
- Recovery / removal
- Minimum pulse width checks
- Asynchronous paths
- Max transition
- Clock skew and clock uncertainty
- False-path and multicycle-path validation

3. Signal integrity and noise signoff

Important for dense and high-speed designs, in particular if timing affects performances

- Crosstalk delay analysis
- Noise propagation checks
- Crosstalk glitch analysis
- Signal integrity

Sign-off checklist

4. Equivalence and consistency checks

Prove that the design phase transformation did not change functionality

- RTL vs netlist logical equivalence check (LEC)
- Netlist consistency
- Formal checks of connectivity
- LVS (layout versus schematic / netlist)

5. Analog-Digital interface checks

Picopix is digital on top with distributed analog macros

- Digital-to-analog interface connectivity
- Validate the liberty files (Model consistency)
- Level compatibility
- Mixed-signal simulations

6. Power signoff

Critical in large pixel detector matrix ASICs. Most of failing designs underestimated power analysis

- Static IR drop analysis
- Dynamic IR drop analysis
- Electromigration checks
- Power-grid integrity
- Voltage-drop impact on timing?

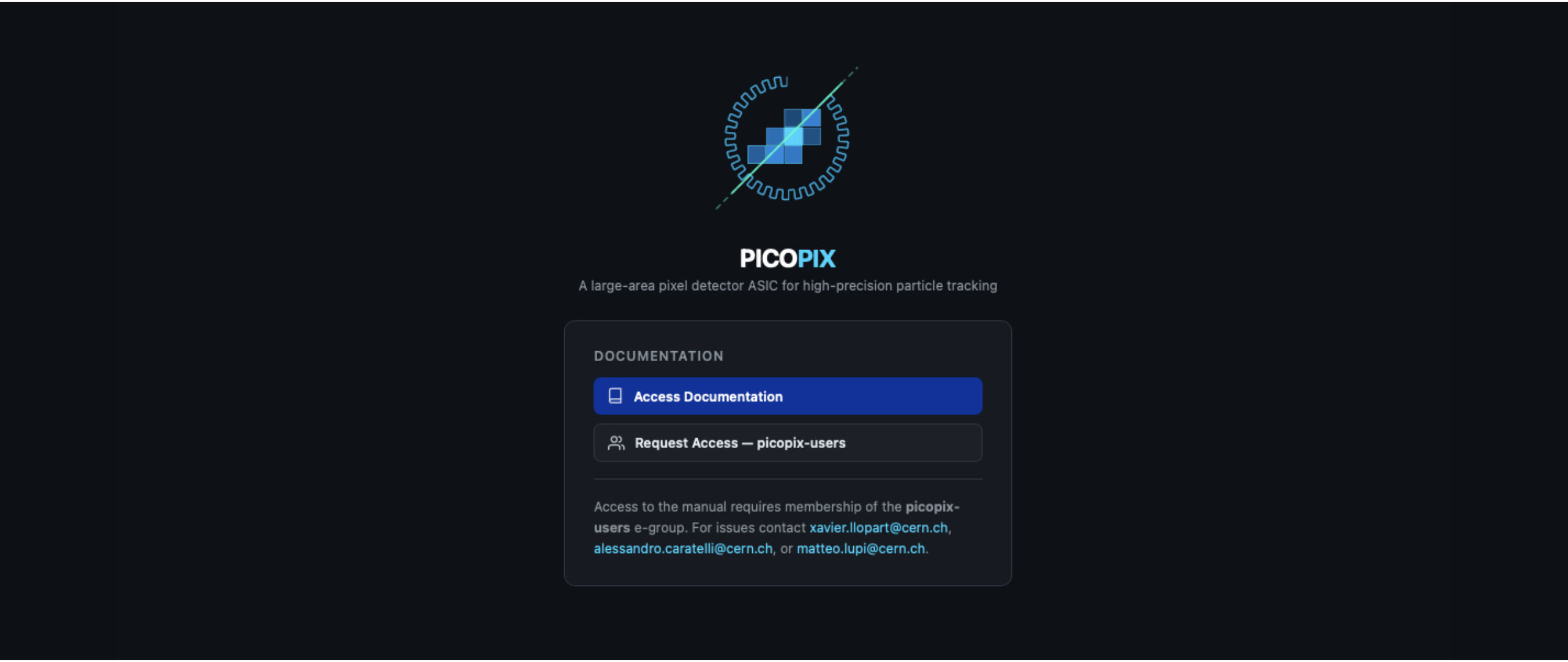
7. Physical verification

Check design manufacturability

- DRC (design rule check)
- Antenna checks
- Density / fill checks
- Latch-up checks

Documentation

https://cern.ch/picopix



Design submission plans

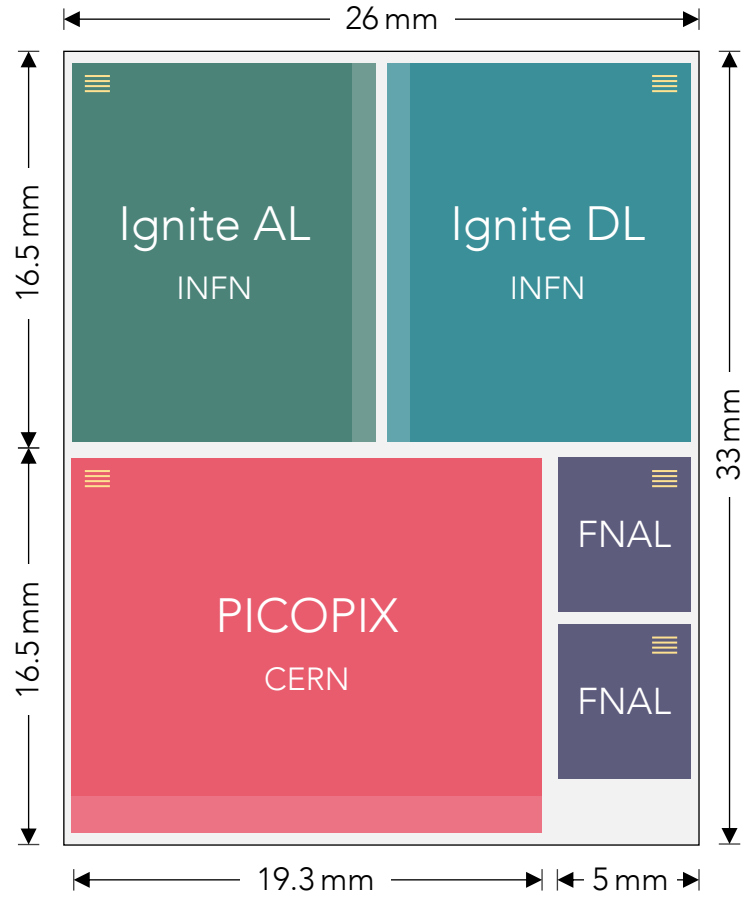
Status evaluation meeting held on 7th May 2026 among PICOPIX designers and IP-blocks designers.

Current estimates suggest submission by Q4 2026 in the hypothesis of not cutting corners.

Next assessment will take place end of June.

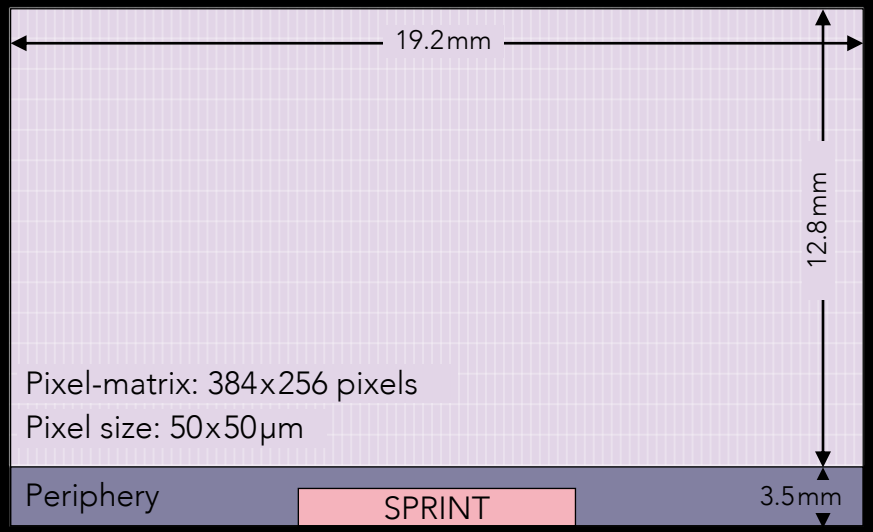
Shared mask-set among PICOPIX, IGNITE and FNAL.

Immediate plan to perform a short-loop submission with the agreed reticle (including only the top metal layers and passivation opening).



PICOPIX

A large-area pixel detector ASIC for high-precision particle tracking



Data-driven mode

- For tracking applications
- Timing resolution → 30ps$_{RMS}$
- ToT → 12bits each pixel
- On-chip clustering with ToT based centroid extraction
- On-chip time-correction
- On-chip time-walk correction
- On-chip auto-calibration
- On-chip cluster filtering
- On-chip packets sorting

Event rate

- Max event rate per matrix → $3.8 \cdot 10^9$ cl/s
- Max event rate per area → 10^7 cl·s^{-1}mm^{-2}
- Max single pixel rate → 20 MHz/pixel
- Max bit-rate → 102.4Gb/s (4 links)

Control and configuration

- Independent slow-control and synchronous control ports
- On-chip RISC-V microcontroller

Process

- 28nm bulk CMOS
- 10M 5x1y1z1u+rdl
- 0.9V + 3.6V supply

Radiation tolerance

- TID → > 1Grad
- SEE → protected control and configuration

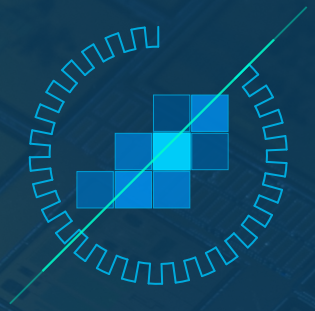
Frame based mode

- For imaging applications
- Zero-suppressed
- ~Continuous readout window

Front-end

- Front-end for low-gain: planar, 3D, LGAD
  - ENC < 95e$^-$ (100fF input capacitance)
  - Q_{IN-THR} > 4ke$^-$ → jitter < 30ps$_{RMS}$
- Front-end for high-gain sensors: SPAD

PICOPIX



PIXEL DETECTOR ASIC FOR HIGH-PRECISION PARTICLE TRACKING

Alessandro Caratelli on behalf of PICOPIX design team

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