The FPMROC ASIC Development

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Institute of High Energy Physics, CAS

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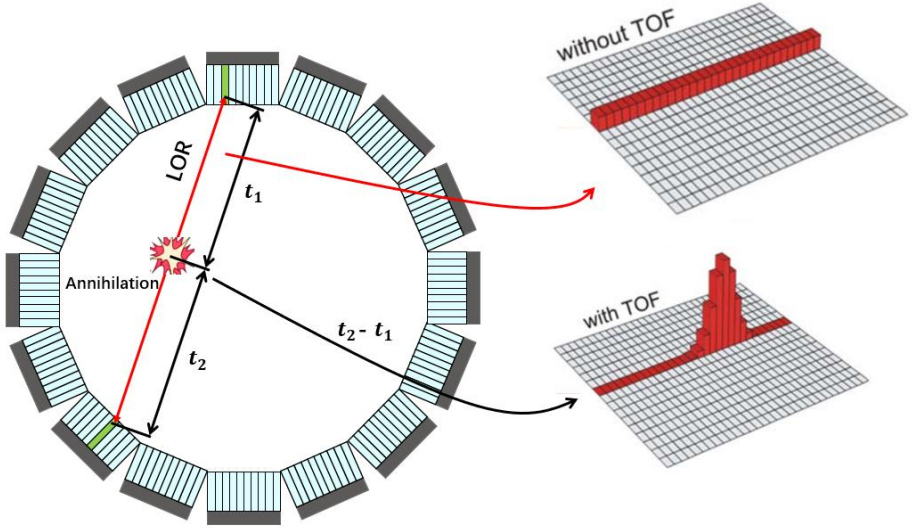
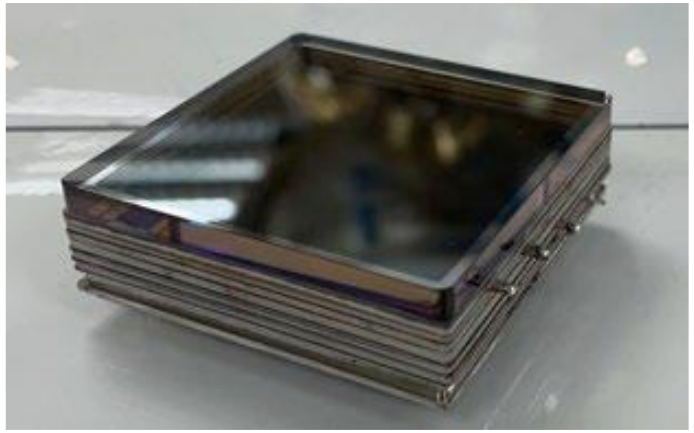
Lyon France, 29 June – 3 July 2026

Outline

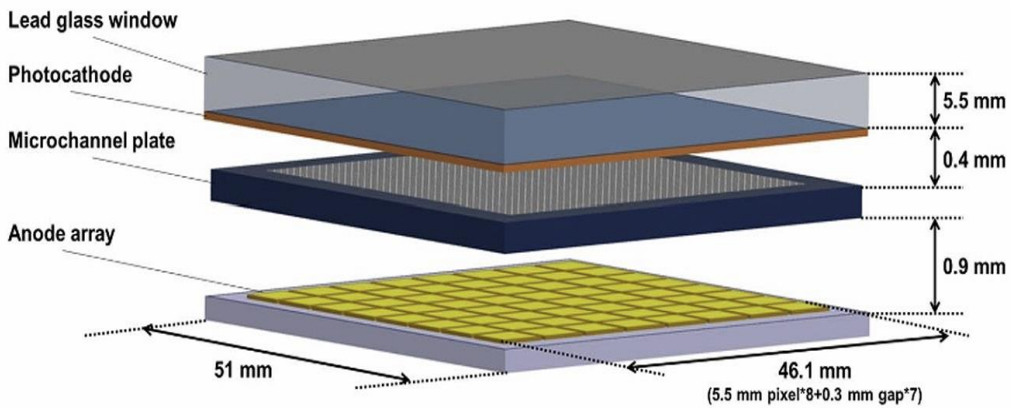
- The intended application of this FPMT-Read-Out-Chip, FPMROC
- The design of the 1- and 16-channel ASICs
- The Status:
  - FPMROC1 and iPMT1
  - FPMROC16 and iPMT64 (or 128, 256, …)
- L'avenir
  - The tape-out this October
  - Possible engineering-run in 2027
  - Plan to go down to sub-10ps resolution

The intended application, PET with MCP-PMT



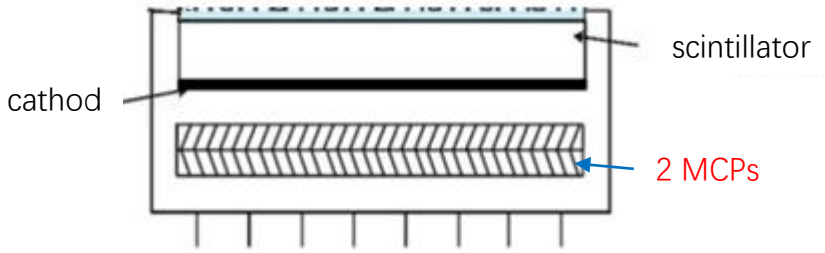


- FPMT（Fast timing MCP-PMT）, 8x8 array, detects Cerenkov photons generated in its front window, in a TOF-PET (Time-of-flight Positron-Emission-Tomography) system.
- FPMROC reads out FPMT, providing digital timing information.

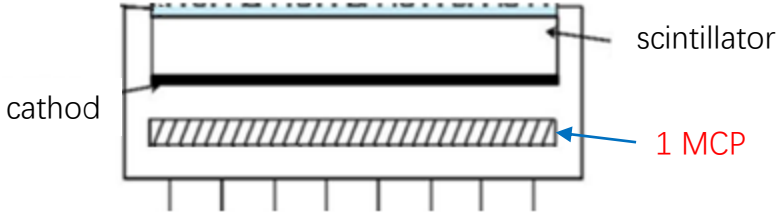


FPMT output characteristics

- **For FPMT with 2 MCPs：**
  - **gain：~1x10^6**
  - **Pulse leading：~300ps**
  - **Pulse trailing：~500ps**
  - **Pulse width(FWHM)： ~0.7ns**
  - **Amplitude@50 Ω：~60mV**
  - **Capacitance at each cell: ~4pF**
  - **TTS: ~ 30ps**



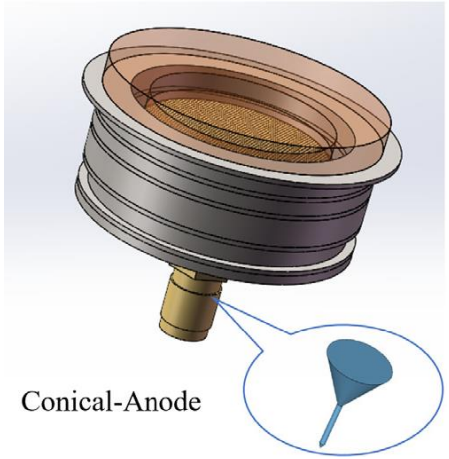
- **FPMT with Single MCP(in development)**
  - **Gain expected: ~10^5 (16fC)**
  - **Pulse leading edge: ~200ps**
  - **Amplitude@ 50Ω : ~2.5mV**

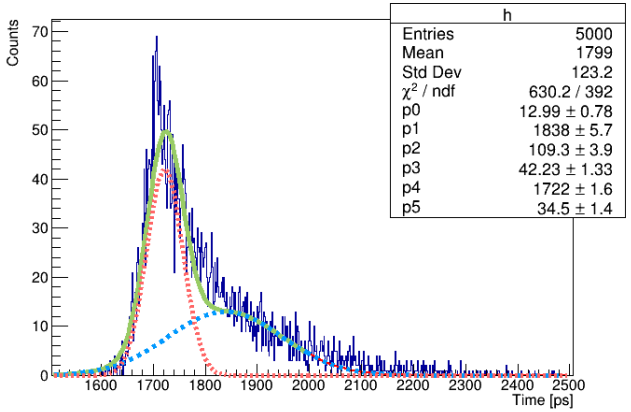


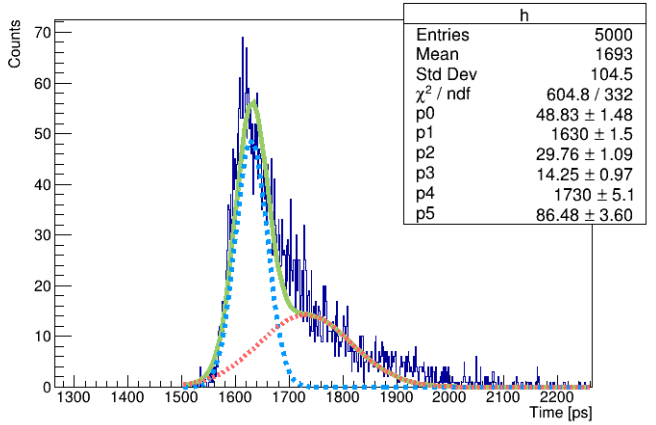
There is also the single-anode version of FPMT

The MCP-PMT From NNVT

- Features a conical anode
- Terminates with an SMA connector

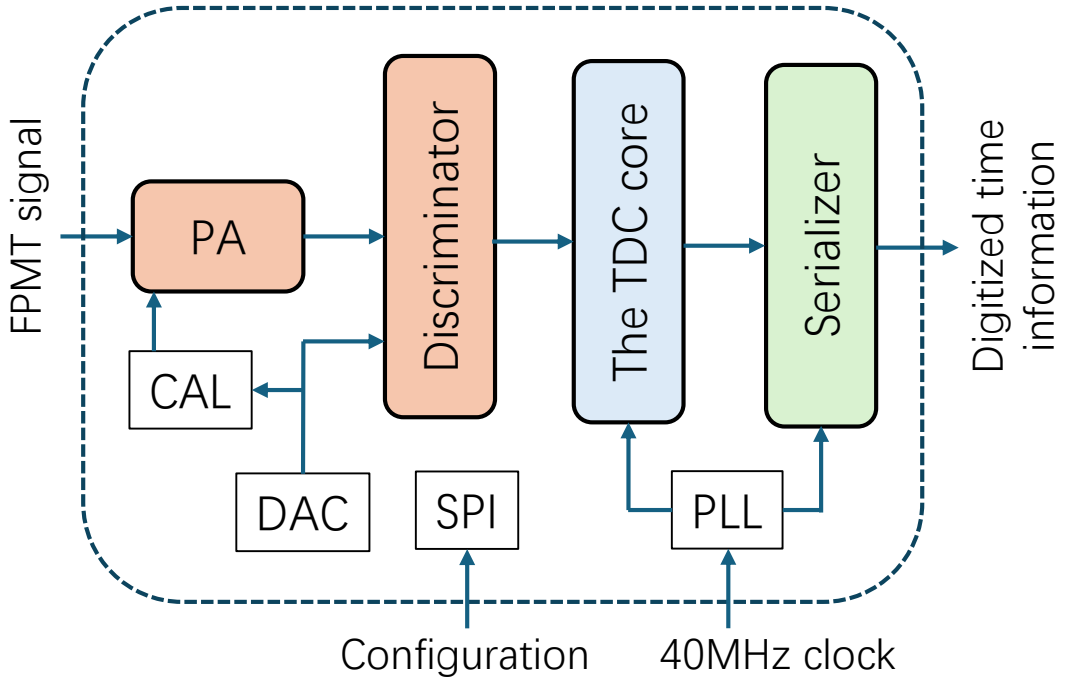




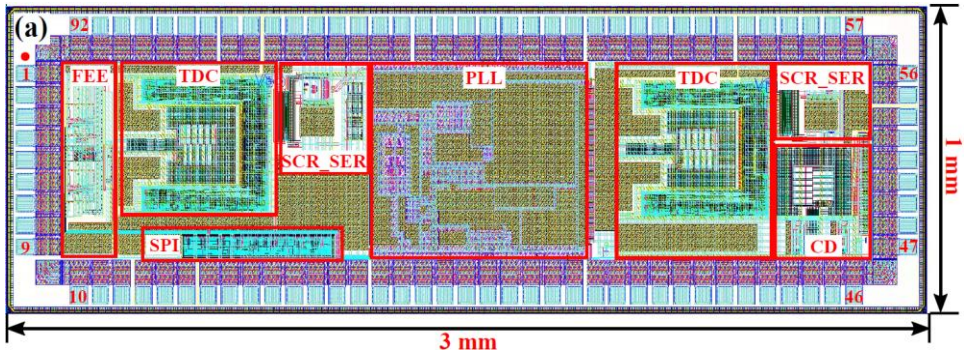


	HV	RT	FT	Peak	Pulse_wid	Gain	P/V	TTS@SPE
2505-5011	1950	253.4 ps	625.7 ps	23.5 mV	471.3 ps	1.9E6	1.5	34.5 ps
2506-5013	2000	219.6 ps	291.1 ps	19.7 mV	414.1 ps	3.8E5	1.1	29.8 ps

The design of the 1-channel, FPMROC-1



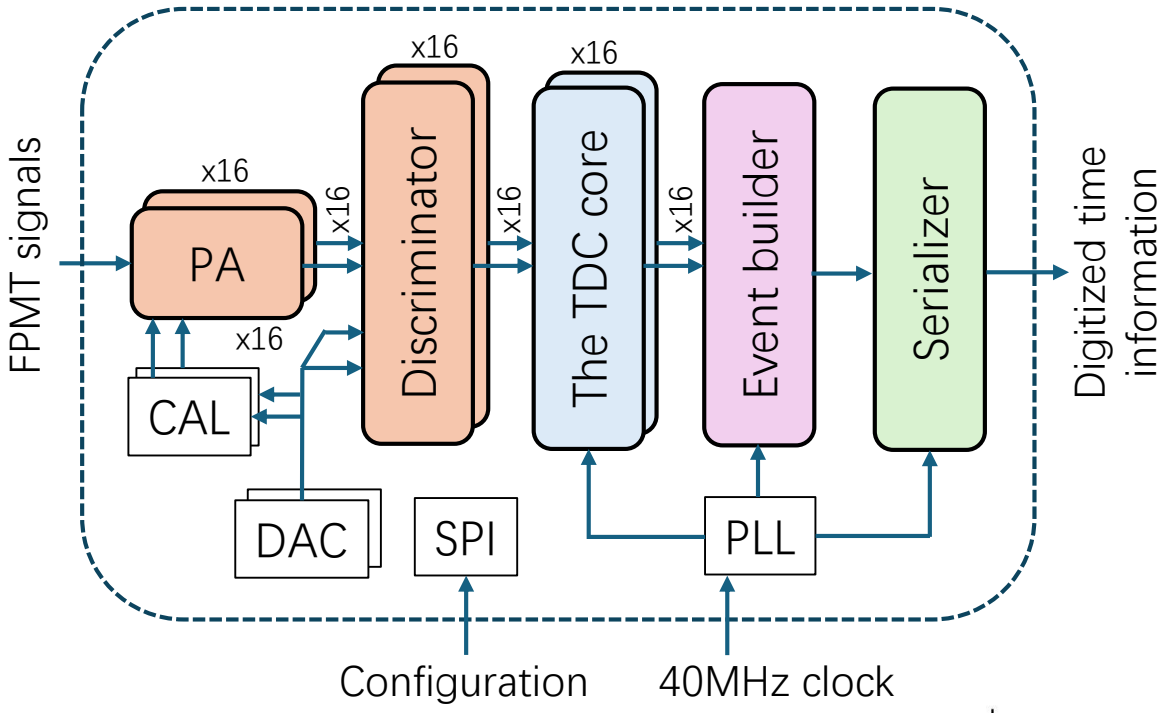
FPMROC1 block diagram



- **Process:** SMIC 55 nm CMOS
- **PA：** pre-amplifier
- **Discriminator:** pick up the time information.
- **DAC:** 8 bits, set the threshold and the charge for self test
- **TDC：** measure the TOA (time of arrival) w/ respect to the 40 MHz clock, TOT (time of threshold), digital calibration, and attach clock time stamp.
- **PLL:** provide clock for **TDC** and **Serializer**
- **Serializer**： **2.56 Gbps serial data output.**
- **SPI：** configure the chip

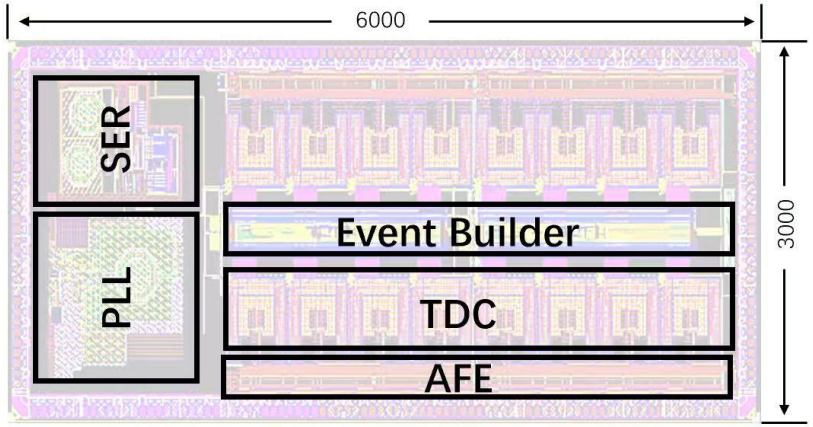
FPMROC1 die (Apr. 2026 tape-out version), two chips, one w/ FEE (PA+Disc), one w/o FEE, share 1 mm x 3 mm

The design of the 16-channel, FPMROC-16



FPMROC16 block diagram

- 16 copies of **PA, Discriminator, TDC.**
- **PLL:** provide clock for **TDC, Event builder** and **Serializer.**
- **Serializer**: **2.56, 5.12, 10.24 Gbps programmable serial data output.**
- **Event builder**: dynamic event construction from channels that have FPMT signals.

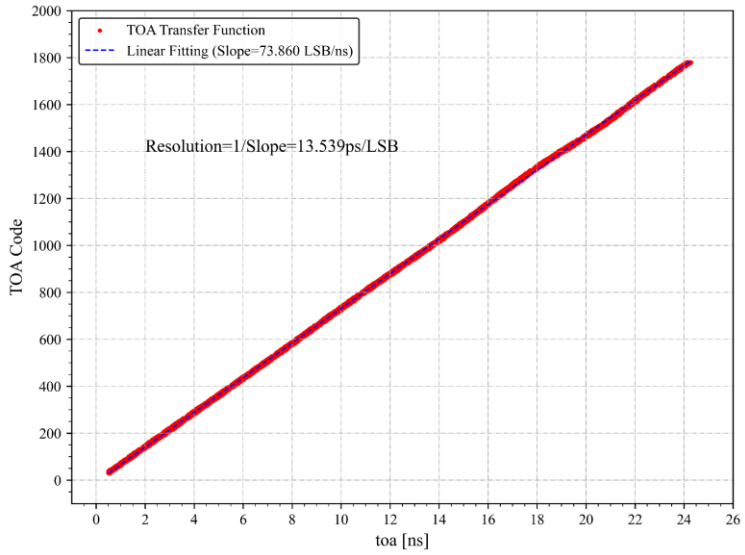


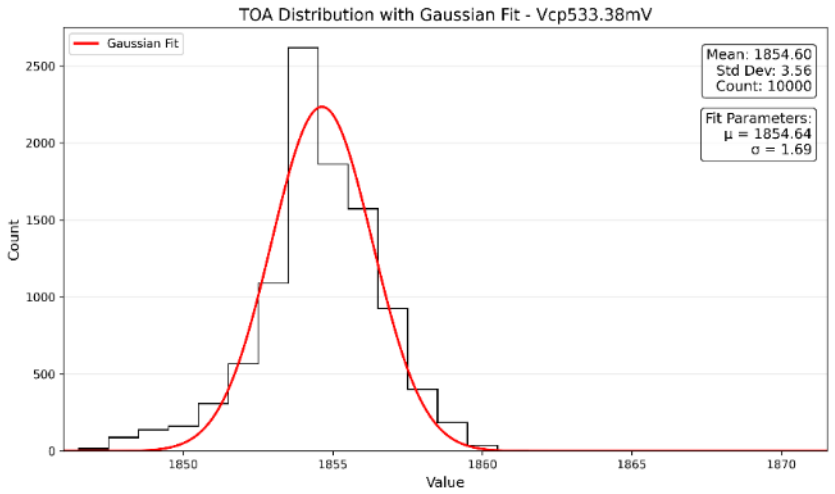
FPMROC16 die (Oct. 2026 tape-out version, preliminary), 3 mm x 6 mm

The status

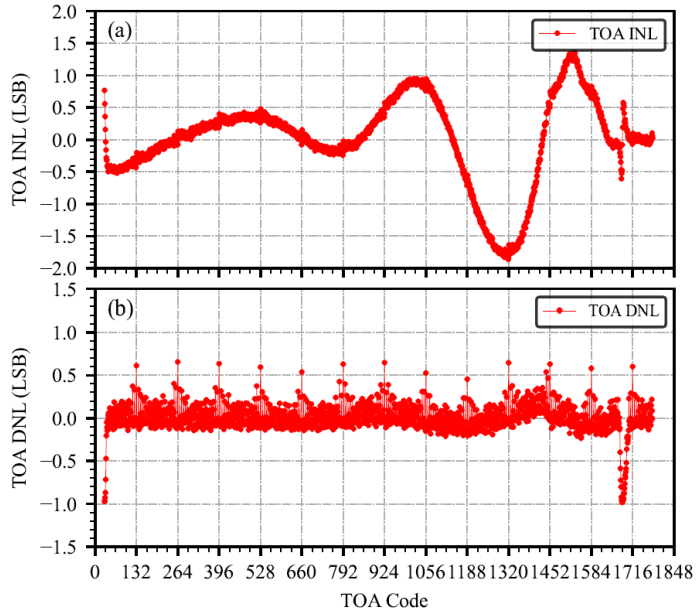
- **FPMROC1** taped-out **Oct. 2025**, verified the design with LSB = 13.6 ps, but the precision about 2 LSBs.
- The **Apr. 2026** tape-out fixed all known bugs, including the precision issue. We treat this version to be **a user-chip**, i.e., not a testing-only chip. We expect 100 chip in Aug.-Sep. 2026.
- We plan to submit the final version (before the engineering run) with enhanced TOT range (from 3 to 25 ns), in **Oct. 2026**.
- FPMROC8 taped-out **Oct. 2025**, verified the design, LSB about 14 ps, other measurements are still on-going.
- The current serializer marginally runs at 10 Gbps, its peaking inductors may have interference with the PLL's VCO, which has an inductor. We decide to use another silicon-verified serializer in future designs.
- We plan to submit the first **FPMROC16**, with all known bugs fixed, and up-to-date requests answered, in **Oct. 2026**, provided that the Apr.2026 tape-out FPMROC1 tested well in August and September.

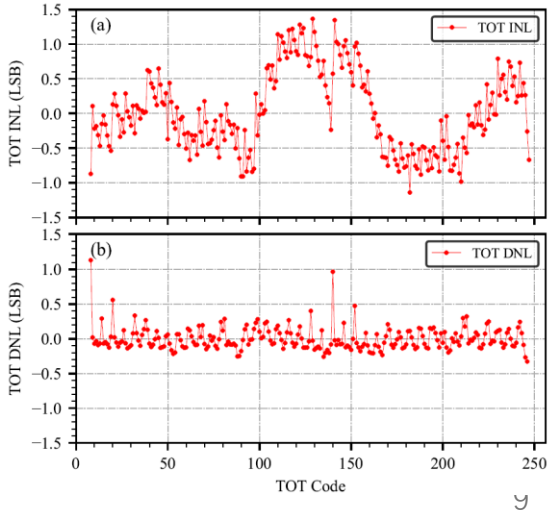
FPMROC1 test results



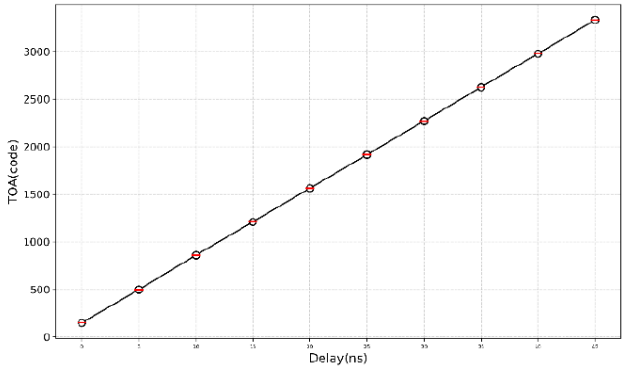


parameter	performance
LSB	13.6 ps
SSP	23.2 ps
TOA DR	0.2 ns-24.8 ns
TOT DR	0.15 ns- 3.3 ns
TOA DNL TOA INL	±1 LSB ±1.9 LSB
TOT DNL TOT INL	±1.2 LSB ±1.5 LSB
Power	20mW

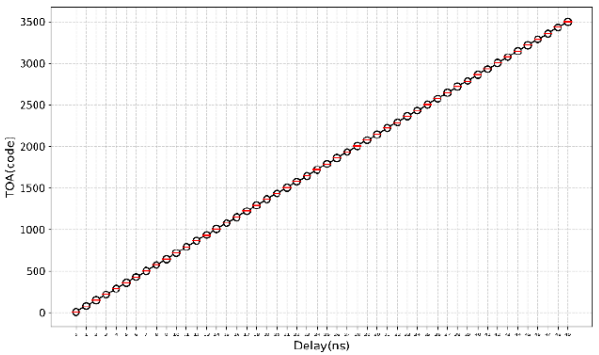




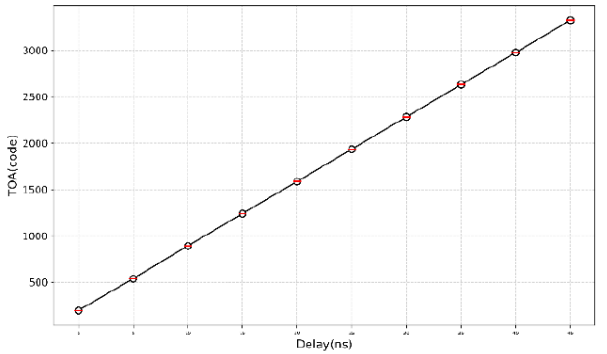
FPMROC8 preliminary test results



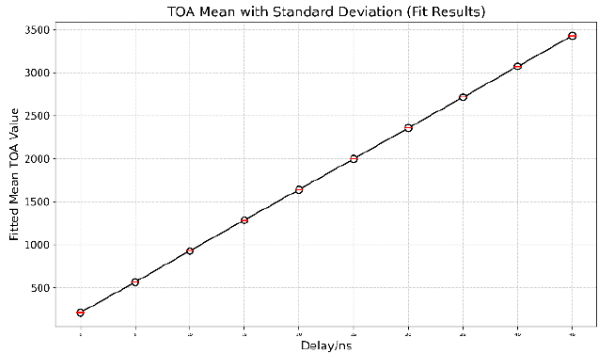
IN0 step: 5ns LSB: 14.14ps



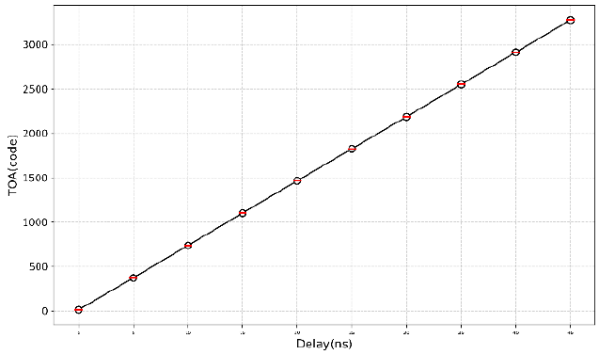
IN1 step: 1ns LSB: 14.04ps



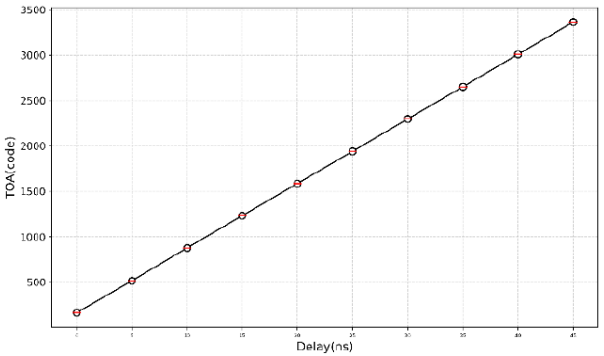
IN2 step：5ns LSB: 14.30ps



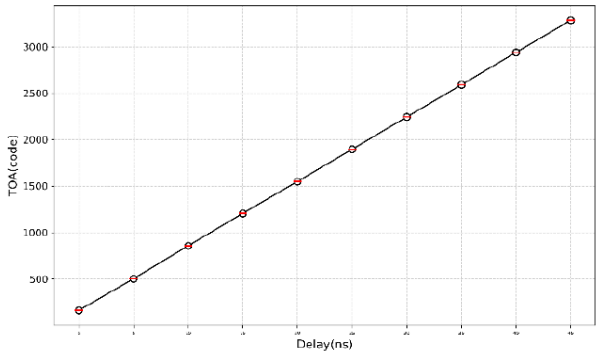
IN3 step：5ns LSB: 13.96ps



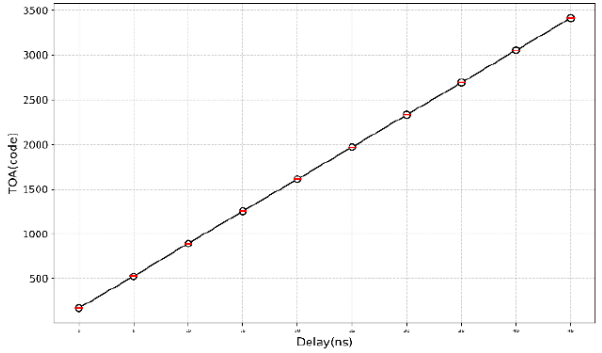
IN4 step：5ns LSB: 13.78ps



IN5 step：5ns LSB: 14.07ps



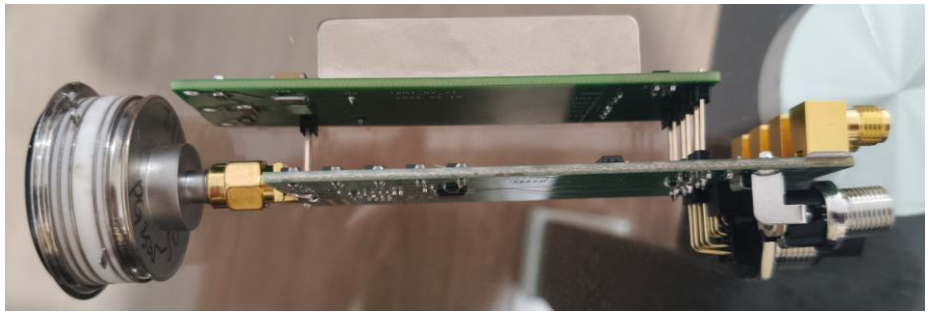
IN6 step：5ns LSB: 14.41ps

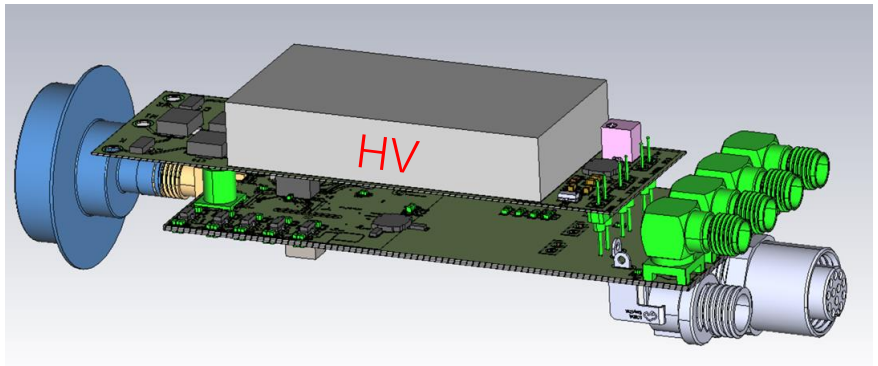


IN7 step：5ns LSB: 13.87ps

L’avenir

- **FPMROC1** is very close to be a user-chip. We expect to have 100 – 200 chips this autumn to winter, and thousands from the engineering run in 2027.
- **iPMT1**, as the first application, we use FPMROC1 to read out the single-anode FPMT, providing users with digitized timing information.
- FPMROC1 is also used in tests of the **PICMIC** project (the next presentation).
- We have several designs aiming to improve the resolution to sub-10 ps. Stay turned.





L’avenir

- **FPMROC16** is planned to be taped out Oct. 2026. We expect 100 chips spring of 2027. If all goes well, this design will also go into the 2027 engineering run.
- **iPMT64:** as the intended application, integration of FPMROC16 with the 64-channel FPMT has started, at this moment, mostly mechanical work about how to attach the readout PCB with the base of FPMT.

If you have a use of the above two ASICs, please let us ( ) know.

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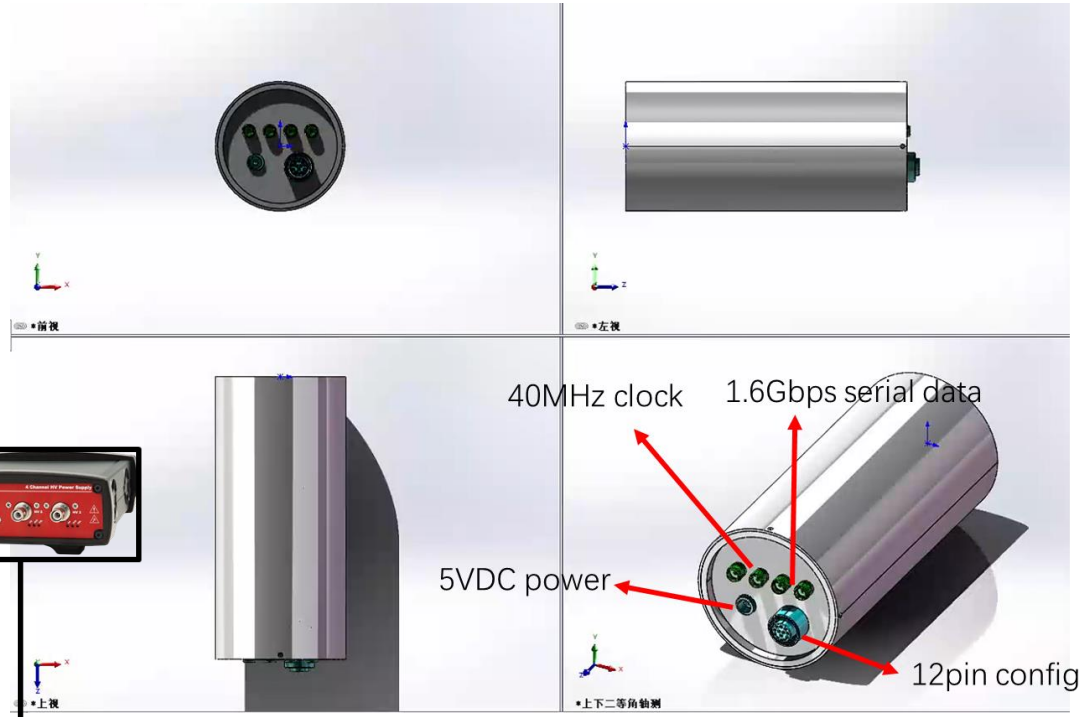
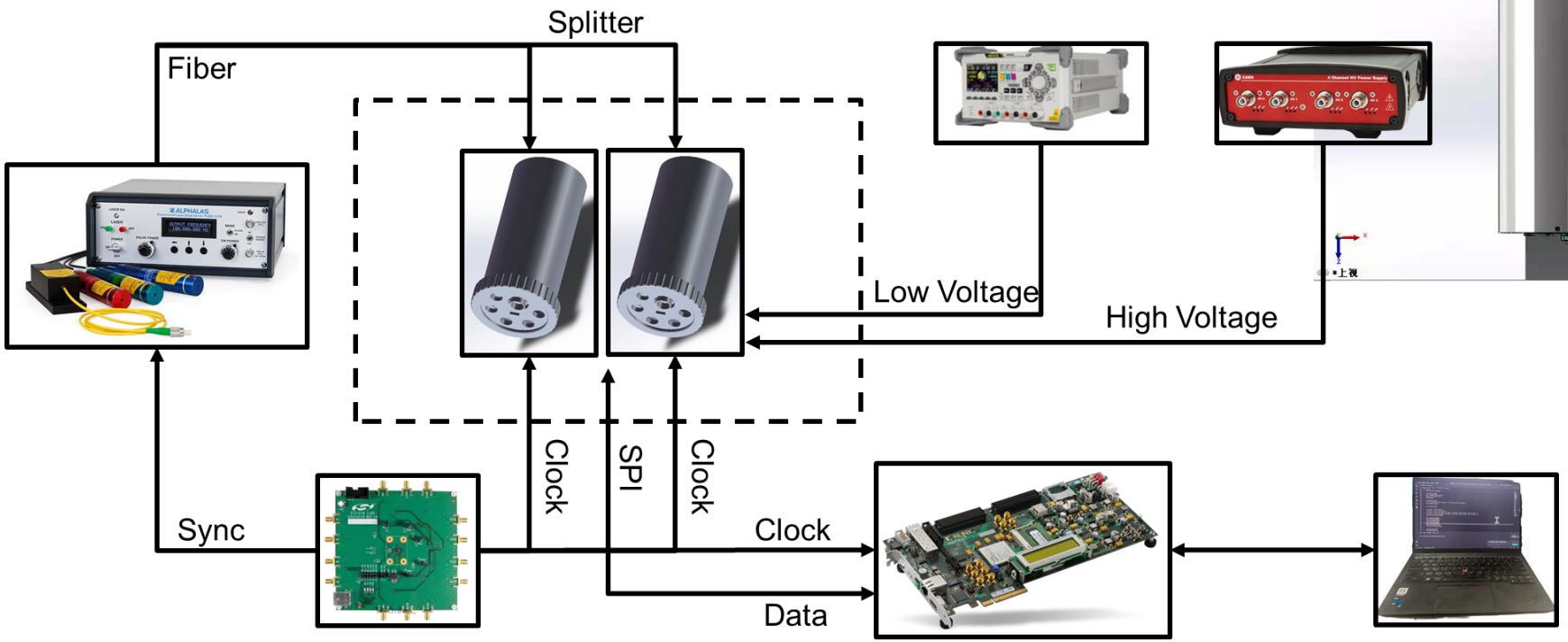
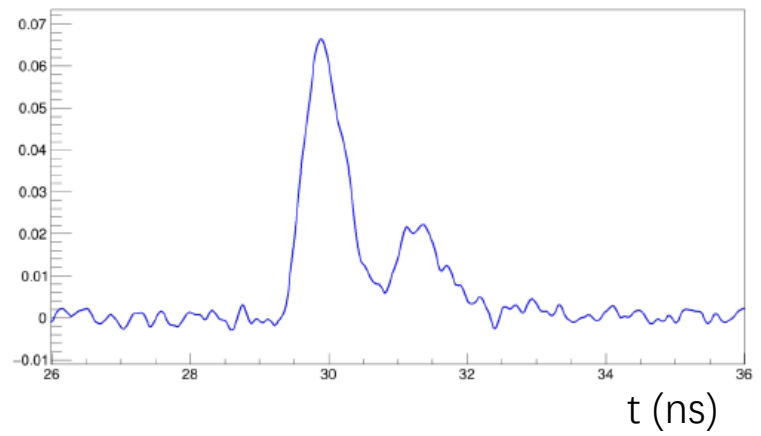
Backup slides

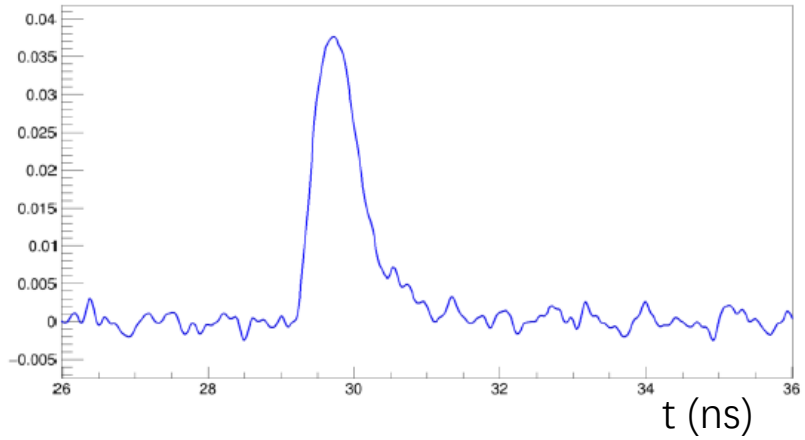
iPMT1

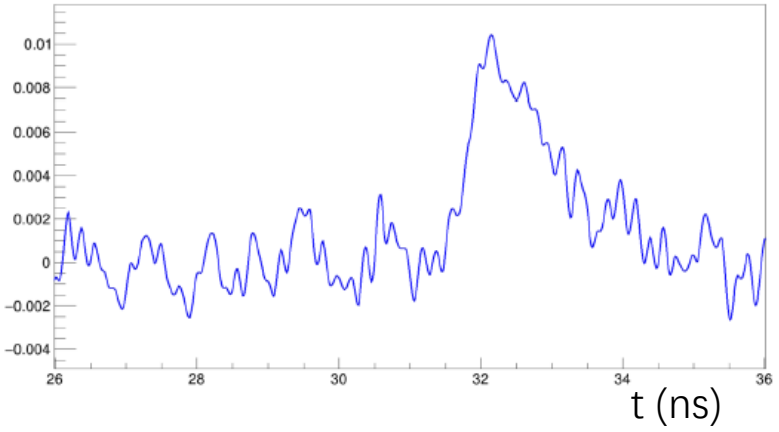

40MHz clock
1.6Gbps serial data
5VDC power
12pin config

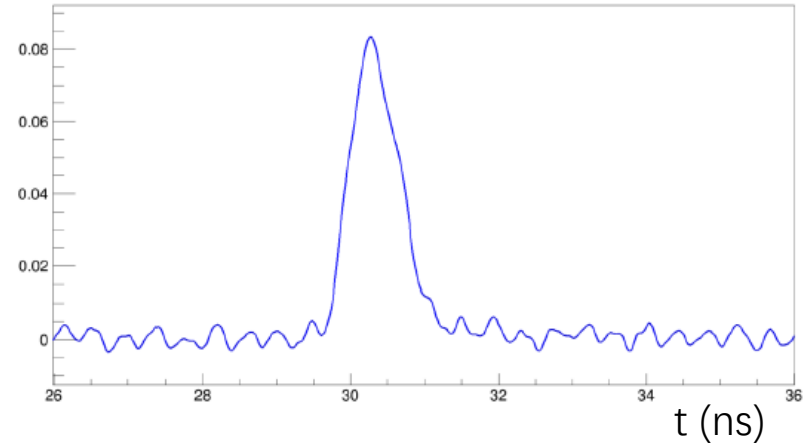

Splitter
Fiber
Low Voltage
High Voltage
Clock
SPI
Clock
Sync
Clock
Data

Typical signals from FPMT with 2 MCPs



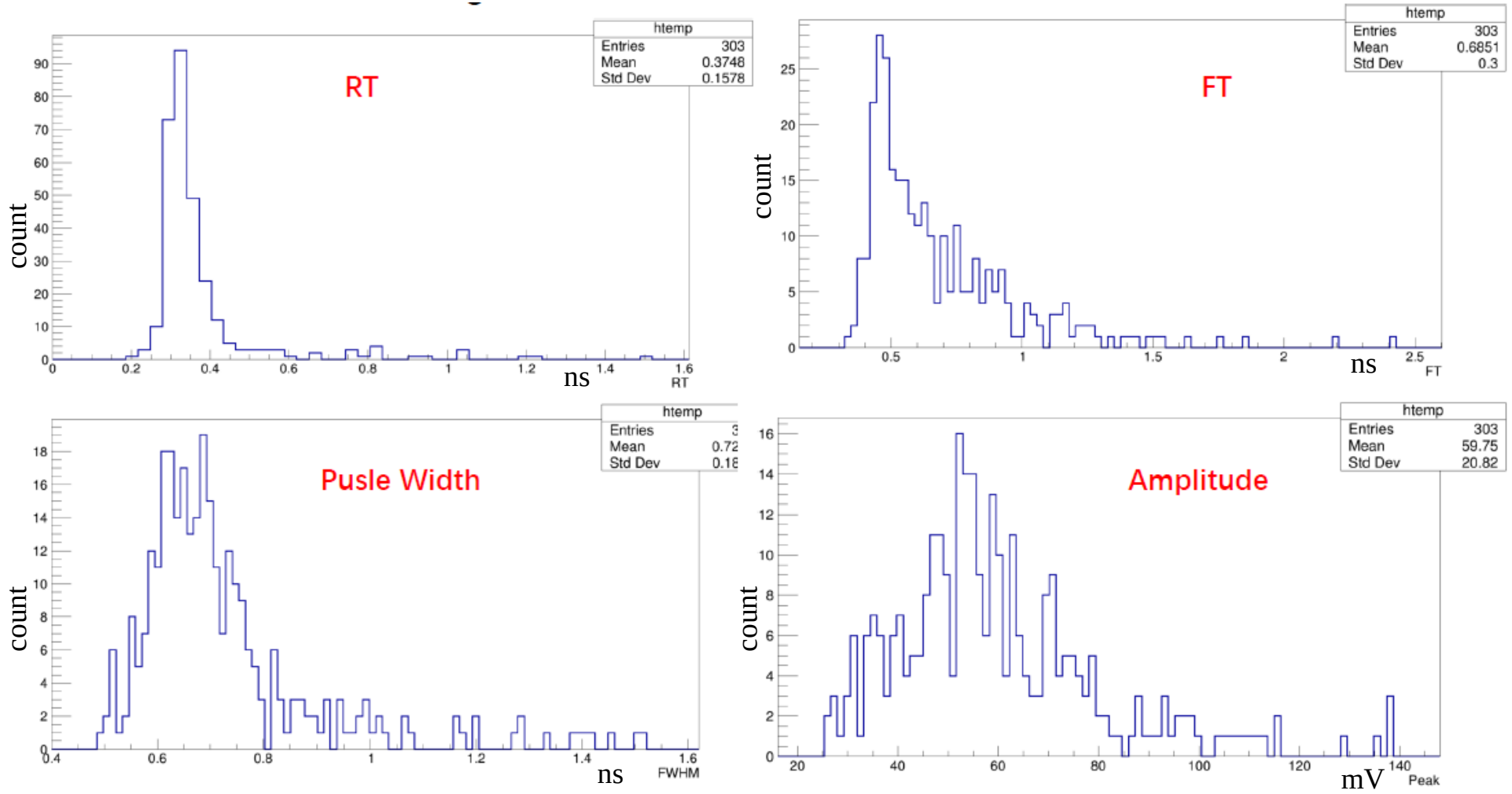






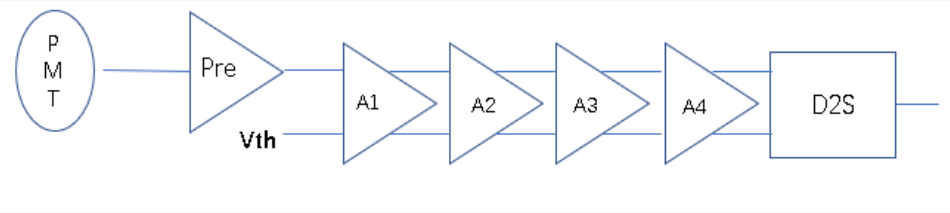
- FPMT gain: ~$1*10^6$

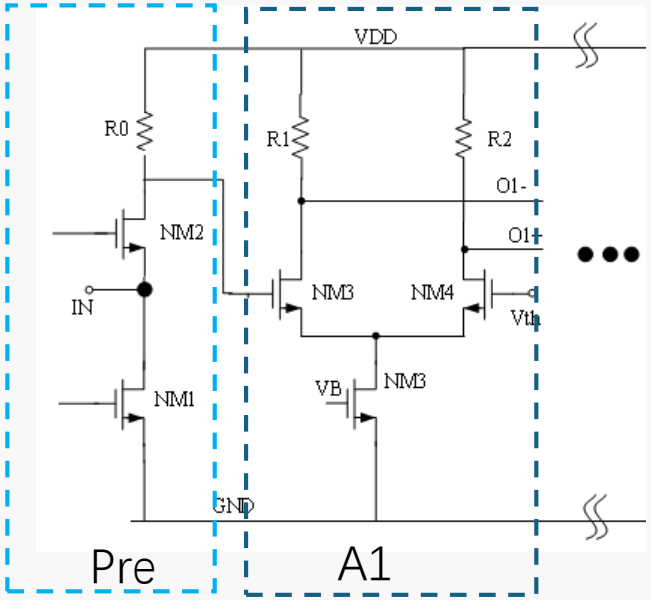
Signal parameter statistics, FPMT with 2 MCPs



Front-end scheme

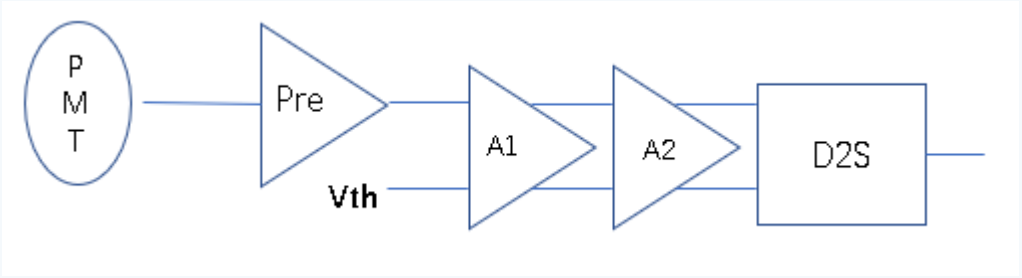
Scheme 1





- Higher BW： ~3 GHz
- Gain： 50.9dBΩ
- Input inpedance： 51Ω @900MHz
- Power: 3.8mW

Scheme 2



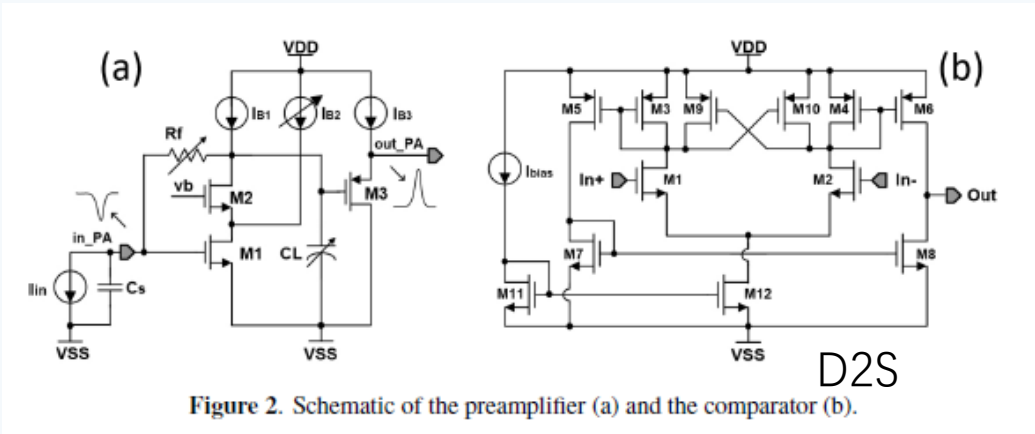
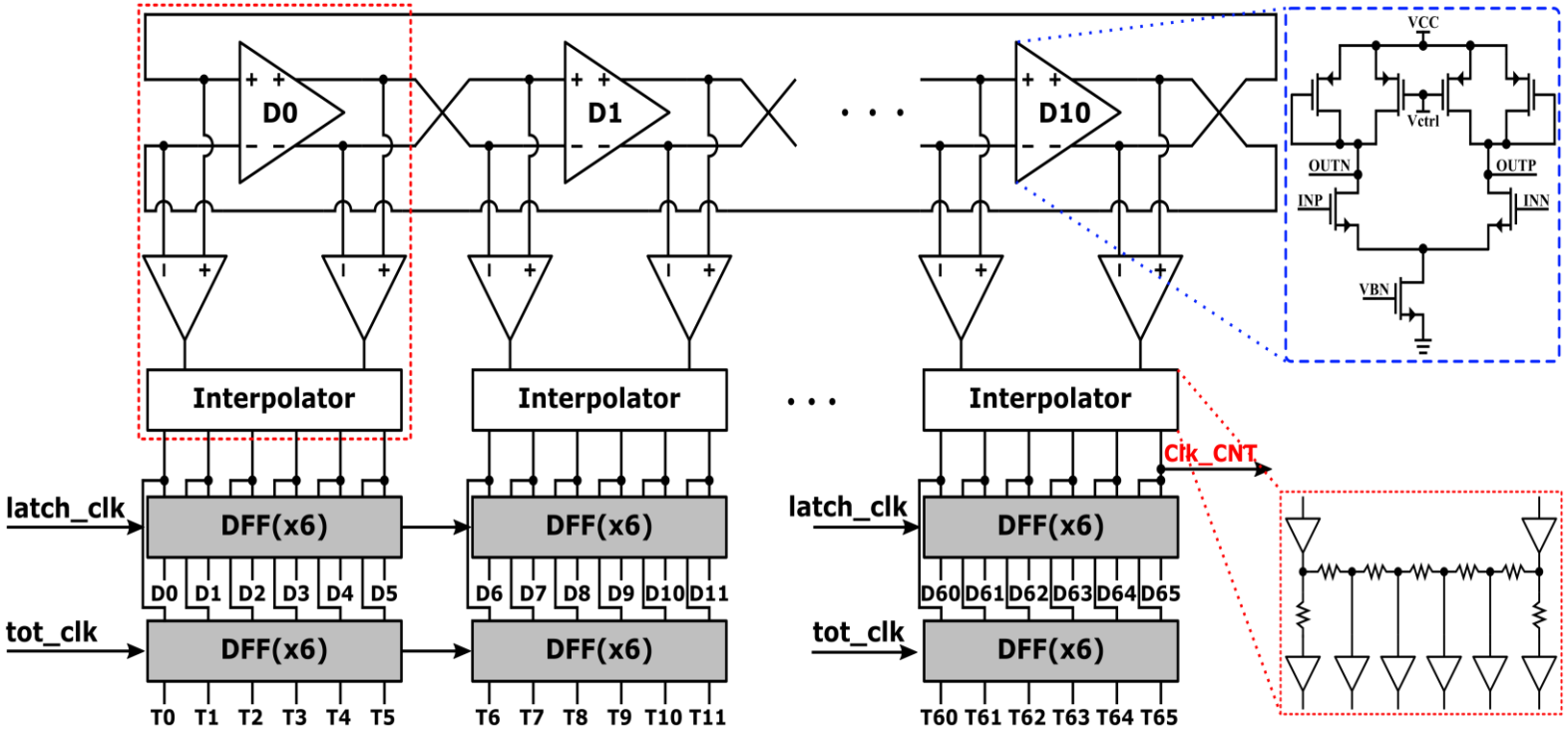


Figure 2. Schematic of the preamplifier (a) and the comparator (b).

- BW~1.4 GHz
- Higher gain： 67.5 dBΩ
- Input impedance ： 42 Ω@2MHz， 48Ω@100MHz
- Power: 4.2mW

Block diagram of the Delay Line



- 11 voltage controlled differential delay cells as a ring oscillator
- 6 stage passive interpolators as fine time
- The Clk_CNT signal is utilized to trigger the ripple counter to generate coarse time.

Event builder