CPPM pixel developments
R&D On Future Colliders

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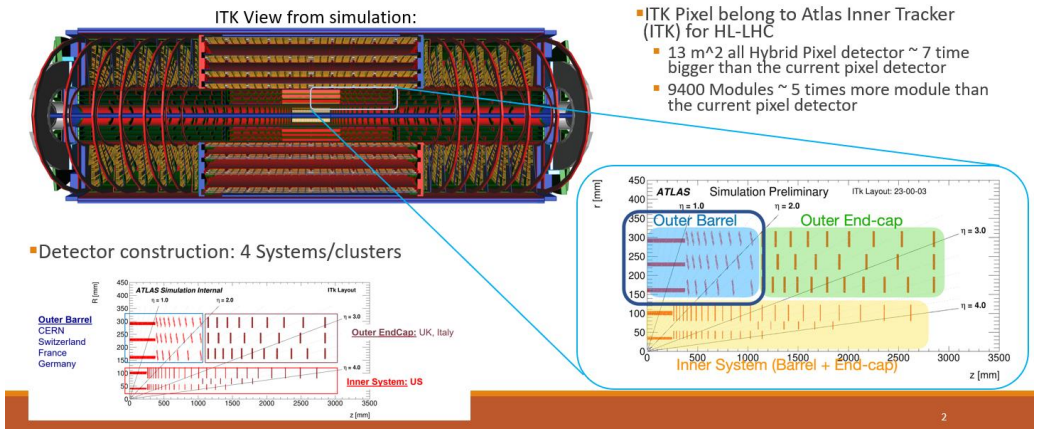
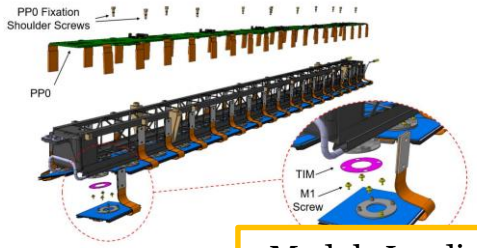
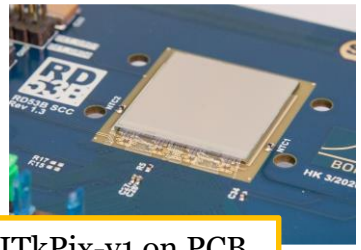
Pixels for HEP at CPPM

- ATLAS and ITk project

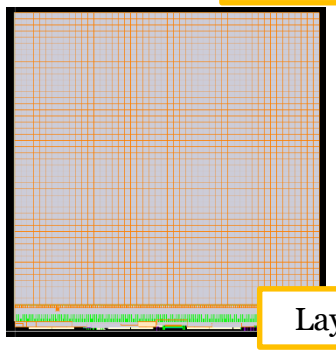




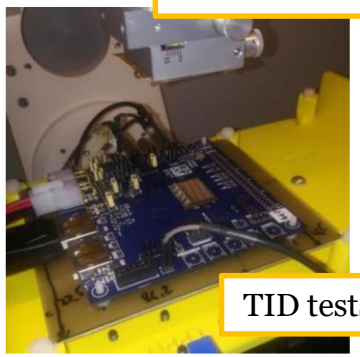
Module Loading



ITkPix-v1 on PCB

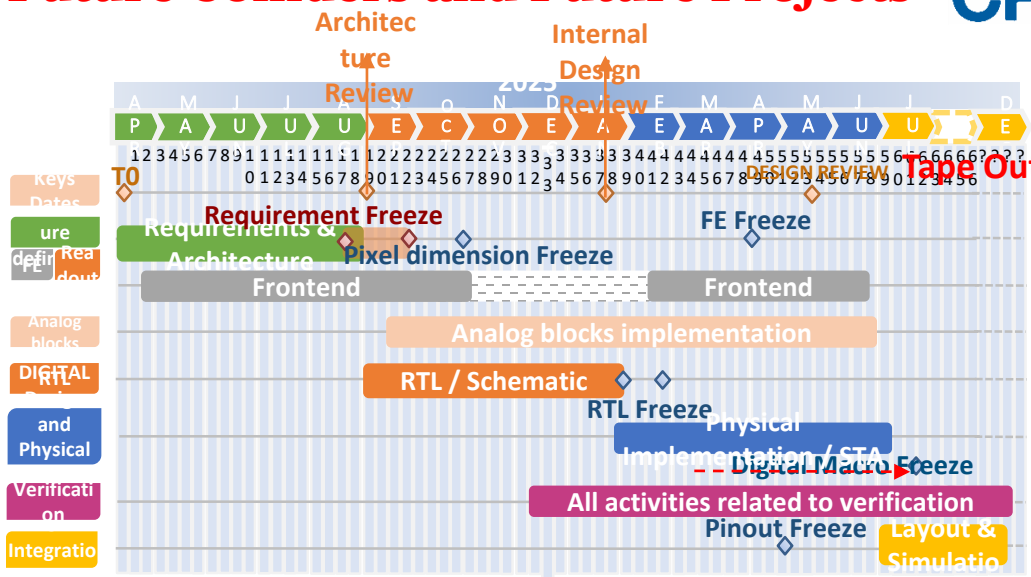


Layout ITkPix-v1

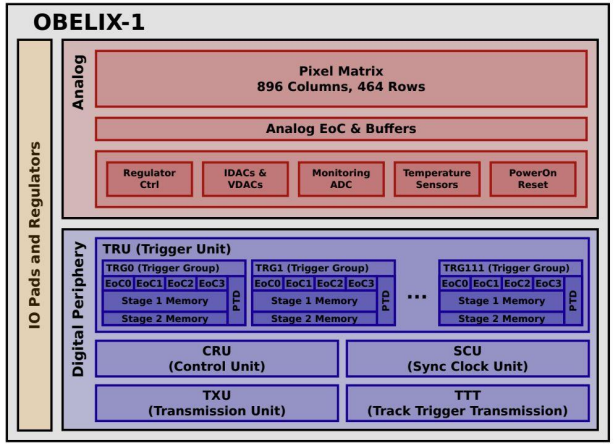


TID tests in Marseille

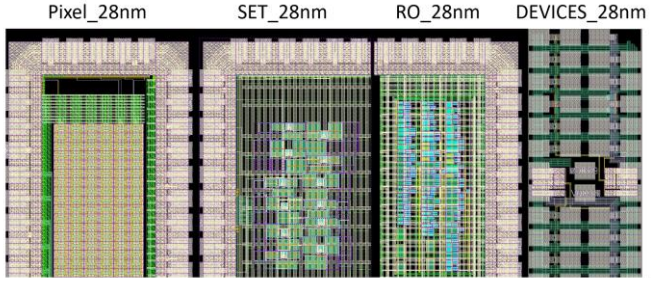
- **Future Colliders and Future Projects**



TPSCo 65nm OCTOPUS plan



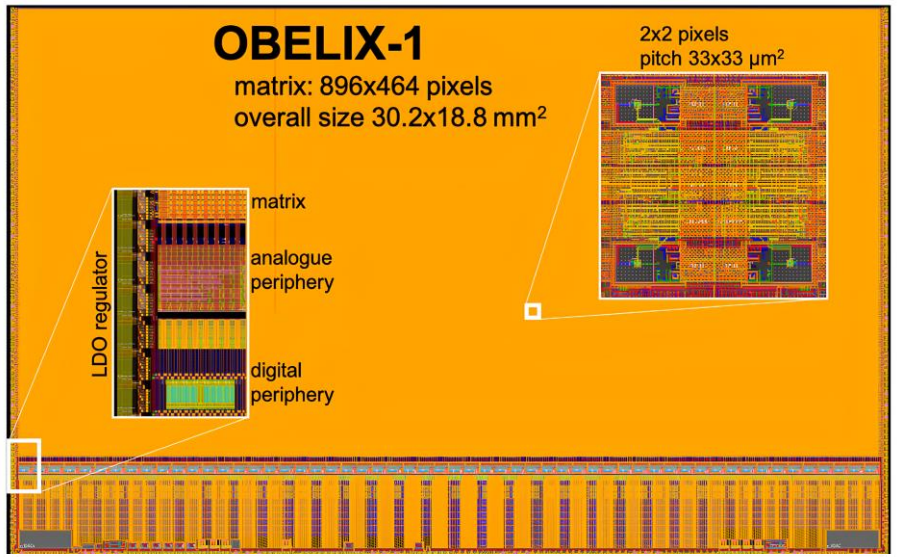
OBELIX for Belle-II upgrade

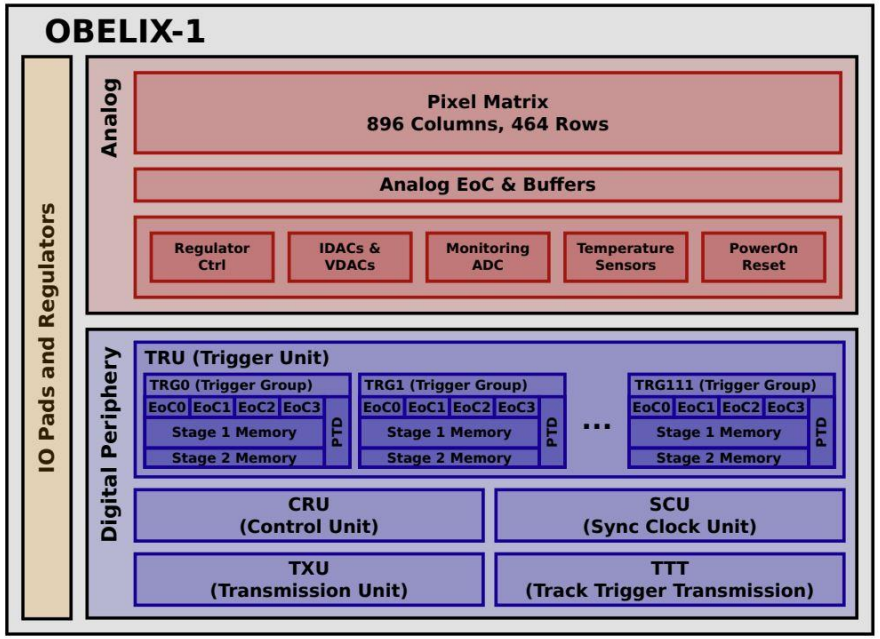


R&D activity for TSMC 28nm

VTX Upgrade for Belle II
OBELIX-1 - TowerJazz 180nm

OBELIX for VTX upgrade



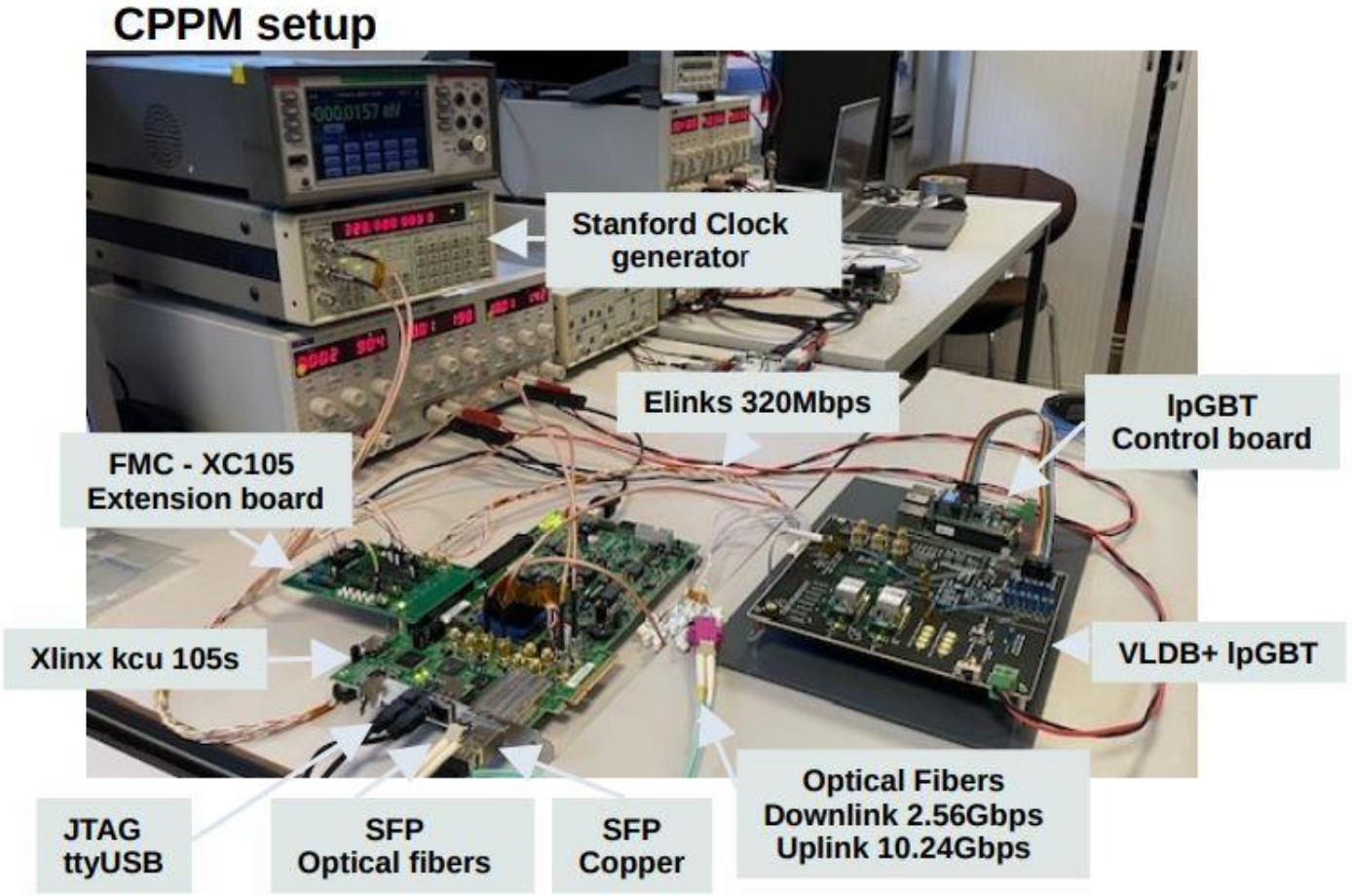


The **O**ptimized **BEL**le II p**IX**el sensor

- Main design **based on the TJ-Monopix2 chip** in TJ180 technology
- **Pixel Matrix**
  - **Hit rate up to 120MHZ/cm²**
  - TID tolerance : 10 MRad/year, NIEL tolerance: $5x10^{13}n_{eq}/cm^2/year$
  - **Power < 200mW/cm²**
  - 464 rows and 896 columns, active area 29.60 x 15.33 mm²
- **New digital periphery -- CPPM**
  - **New EoC adapted to Belle II trigger** – average frequency 30KHz
  - Trigger latency 5-10µs
  - Main Clk at 160MHz, Single output at 320Mb/s
  - Signal digitization: ToT (7 bits, 20 MHz)
- **Power Pads**
  - **Power management system added – LDO -- CPPM**
  - **Overall sensor dimensions around 30.2x18.8mm²**

OBELIX-1 is submit in May, and it supposed to be back in October
Documents under preparation for TDR at the beginning of 2027
OBELIX-2 design task list under discussion.
IHEP will join the OBELIX-2 design.

VTX DAQ Organization



LpGBT setup status at CPPM

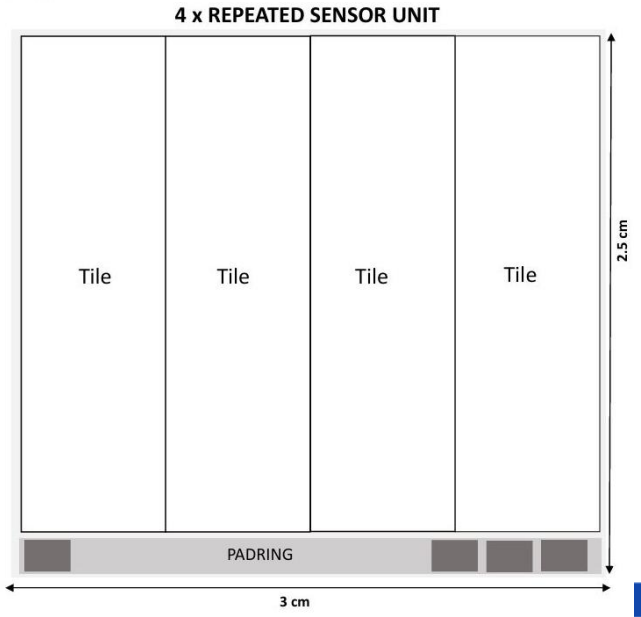
- Belle II VTX WG5: System Integration
- CPPM participates to:
  - Work Packages: Readout
  - LpGBT evaluation HEPHY + **CPPM**
  - iVTX LpGBT integration **CPPM** + QMUL(?)
    - Chip location, PCB, cables and connectors, mechanical integration
- Test work for OBELIX-1
  - Joined the test training at Pisa
  - Re-test all the scripts & setting at CPPM
  - More engineers and institutions are still needed
  - TB for OBELIX-1 is in the planning stage
- More details, look at Patrick BREUGNON's presentation

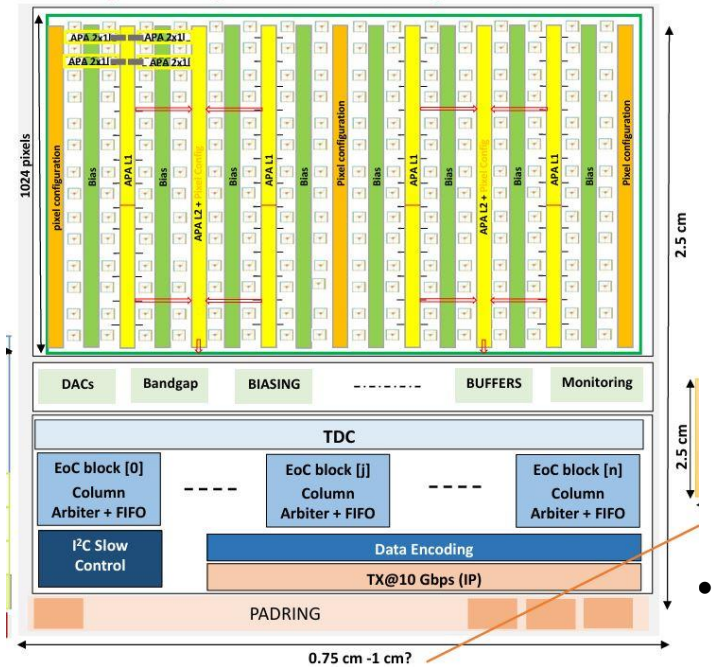
R&D For Future Monolitic Collider
OCTOPUS - TPSCo 65nm

DRD3.1 Project: OCTOPUS

Optimized **C**MOS **T**echnology f**O**r **P**recision in **U**ltra-thin **S**ilicon

- Concerns monolithic fine-pitch pixel sensors implemented in the **TPSCo65 process (DRD7.6)**, targeting the vertex-detector requirements of future Lepton Colliders
- **Key final development goals** include:
  - **3µm** single-point resolution
  - Down to **5ns** time resolution
  - Average power consumption below **50 mW/cm²**
  - Minimal inactive periphery area

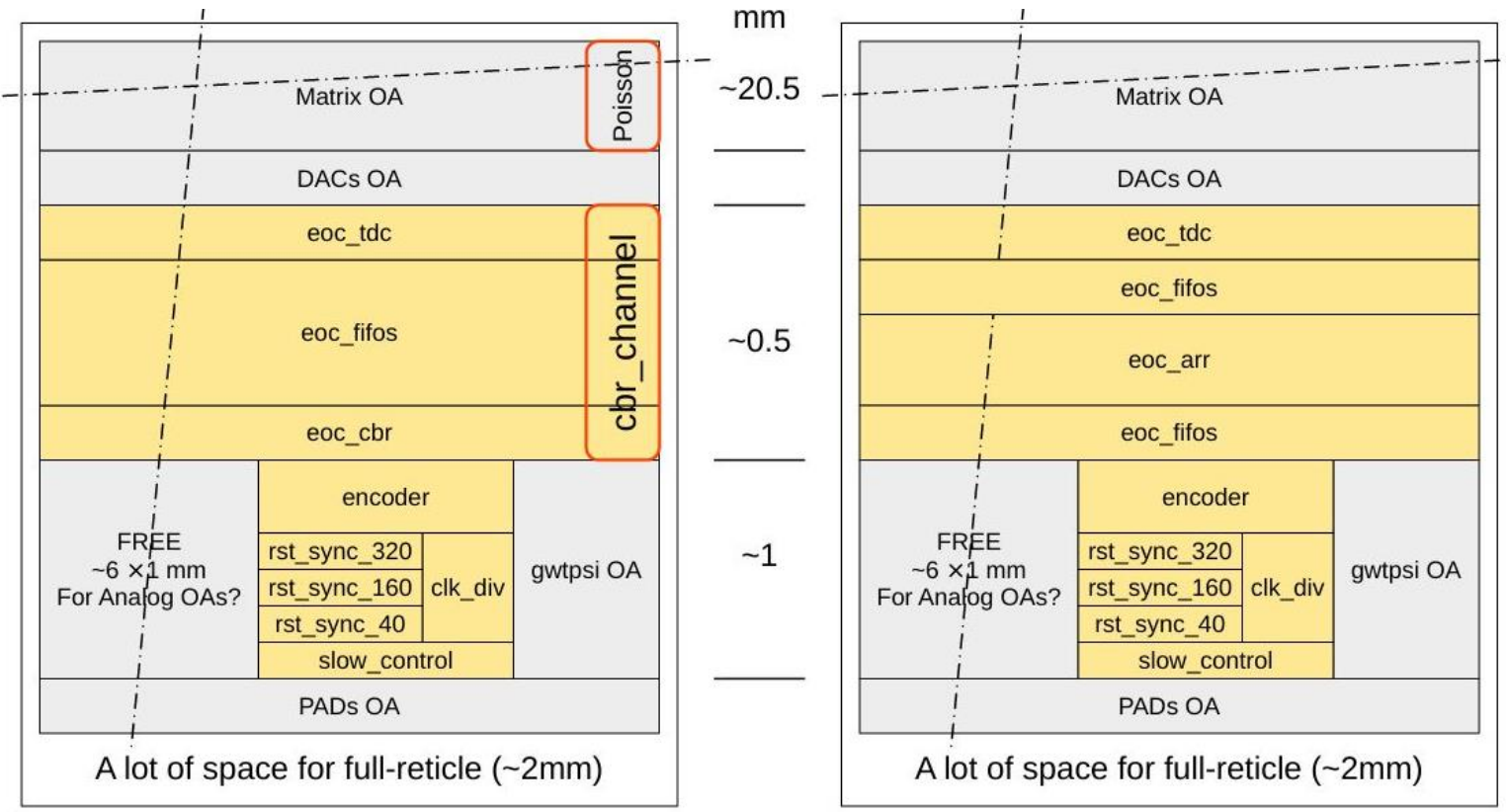




Architecture (Designs for reference):

- First prototype:
  - Full reticle chip: 2.5cm x O (3cm)
  - 3-side buttable
  - Divided to 4 tiles
    - A tile feeds 1-high speed link TX@10Gbps
    - Better IR drop management
    - Tile: fully independent sensor
  - OCTOPUS-1 : MPR2, Q4 2027
  - Size: ? X Tile unit
  - For each tile:
    - Matrix max: 1024 rows * 360 columns
    - In-pixel APA matrix
    - Digital periphery
- **CPPM: new FE & EoC Design**

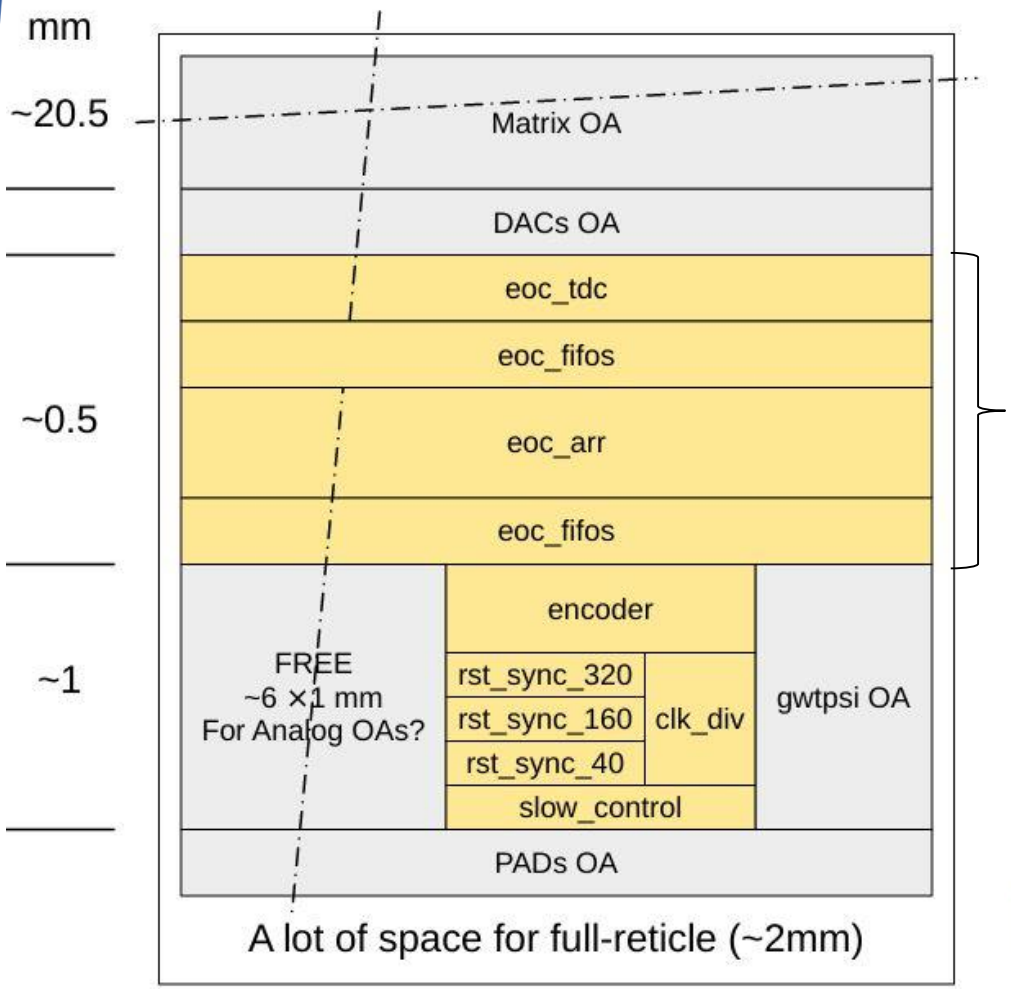
EoC & Periphery

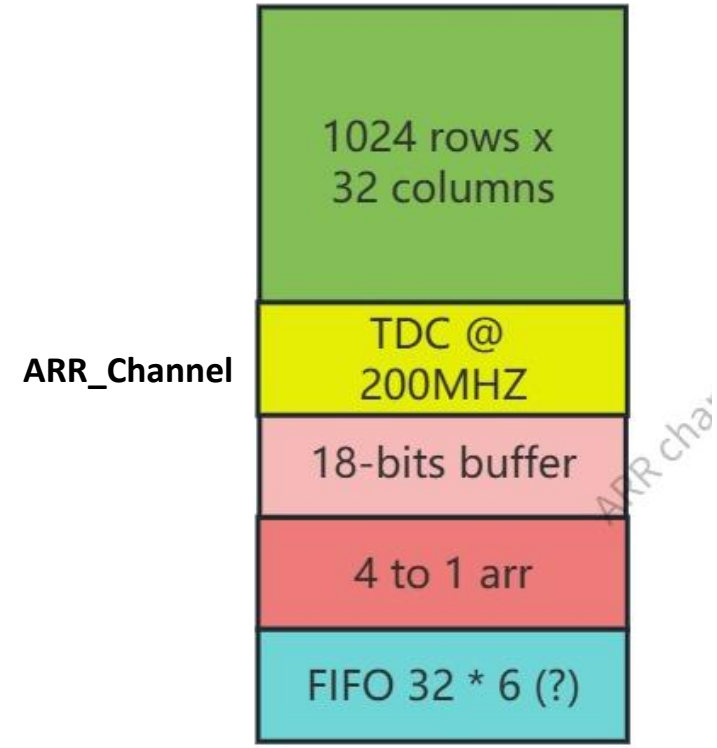


ARR_EOC -- CPPM

- **General parameters**
- Active matrix: 3 * 2 cm
- Pixel size: 20 * 20 µm , 1024 rows * 1440 clmns
- Pixel rate : 100MHz/cm^2 , 600MHz/chip
  - Rising and falling edge ~ 1.2GHz/chip
- Two different EOC
  - CBR: Column Bitmap Readout
  - **ARR: Asynchronous Round Robin**
- Raw data rate
  - CBR: 21 bit/event ~ 25.2 Gbps
  - ARR: 18 bit/event ~ 21.6 Gbps
- RO efficiency ~ 80%
- Coding efficiency ~ 80%
- On-chip lpGBT Encoder & TX@10G24
  - Some problem with IP sharing

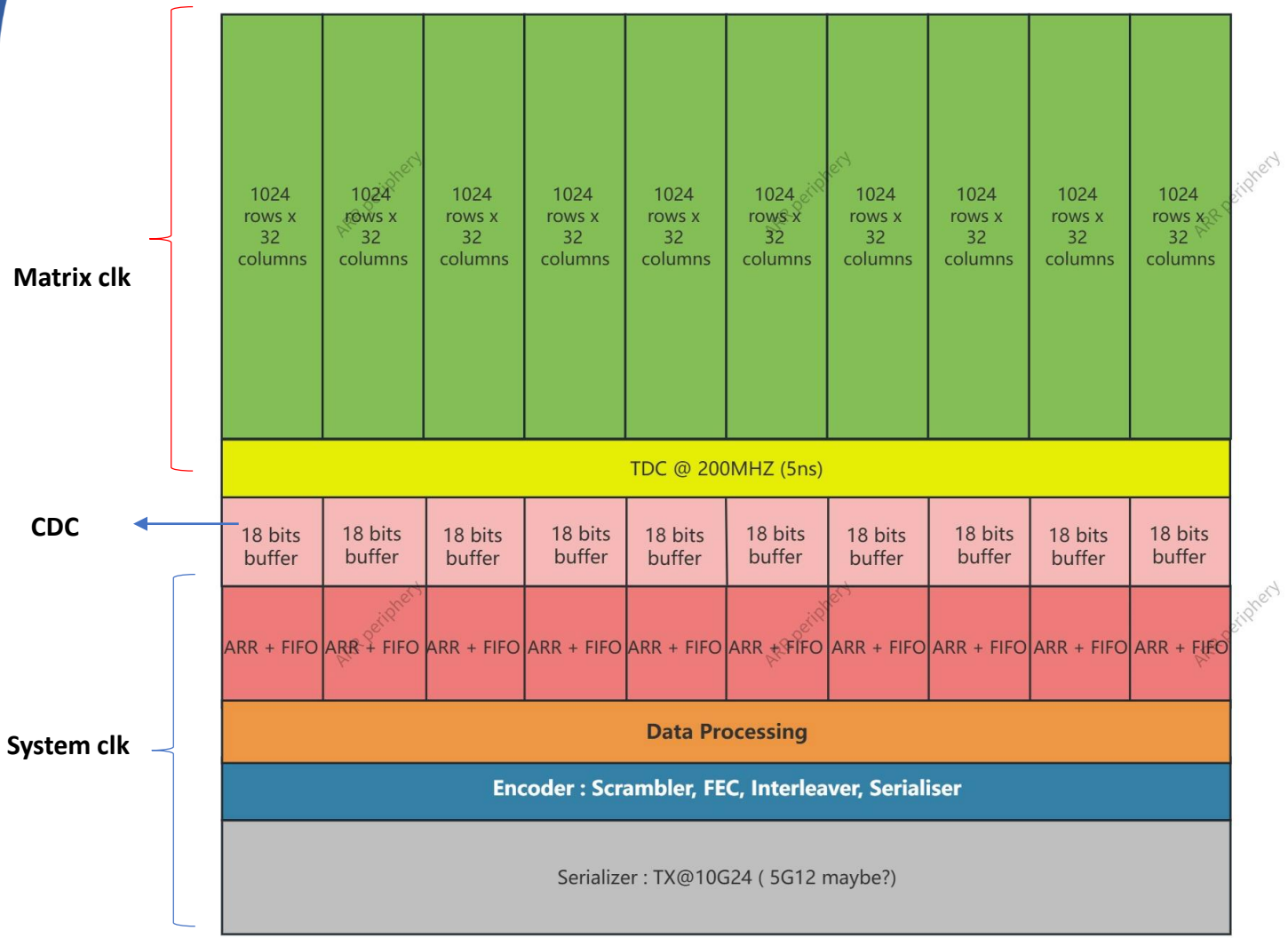
ARR_channel





- ARR_channel
- Module basic: 1 subframe
- Matrix 1024*32
- TOTAL_ROWS: 1024
- NUM_ARR_CLMN: 32
- TDC: 200MHz? 160MHz?
- 18-bits Buffer
- 4 to 1 ARR EOC
- Sync FIFO 32bits * 6 (need sim)
- Data path

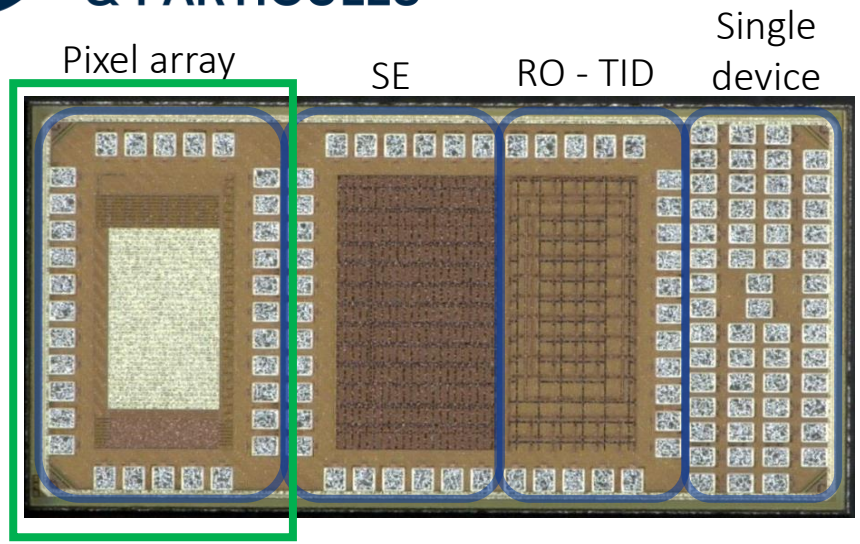
OCTOPUS – ARR EOC

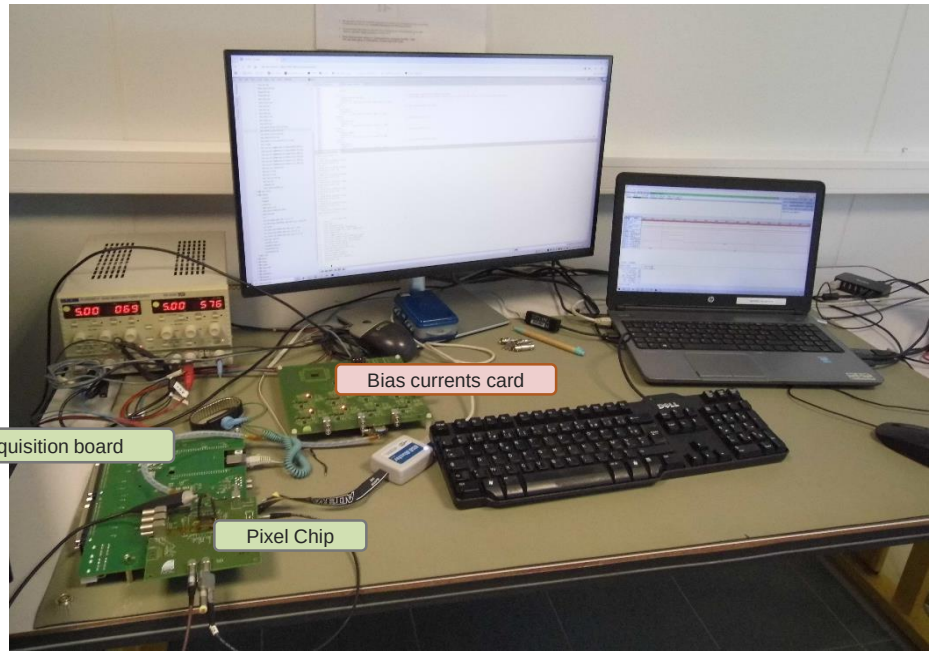


- **My work so far**:
- OCTOPUS: ARR_EOC channel
- RTL codes writing, simulation
- Asynchronous Priority Arbiter
- In-pixel APA, 4*2 to 1 used
- Async Buffer size – 18bits (reserved more?)
- TDC use common module
- Round-Robin Arbiter used
- First combine column data (4 to 1)
- Sync FIFO after EOC : 32 *6 (not fix)
- Adapted to lpGBT protocol
- Output TX@10G24 (5G12 maybe, need sim)

Developments for future pixel hybrid detectors
TSMC 28nm R&D

Latest test setup

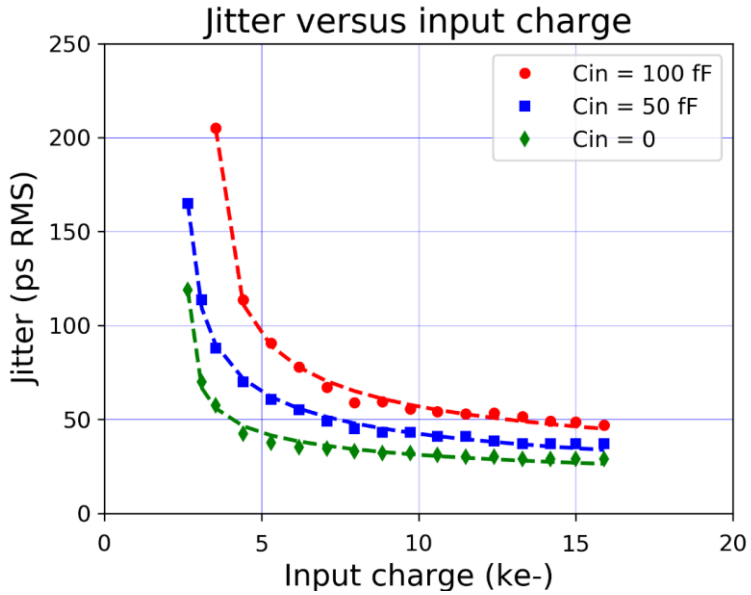




- Latest test started from July, 2025
- The test set-up based on a mini PC board
  - An FPGA deals with the low level interface (clock, IO. . .)
  - 16 bit DAC, 14 bit ADC implemented
  - High level programming framework (C++)
  - Easy Ethernet interface
  - Up to 50 m link
- 16 bit DAC controlled by the nano PC board
  - The threshold voltage
  - Feedback transistor bias
  - Injection charge level
- The injection circuit is integrated in the DAQ board
- The bias currents for the chip are generated from a dedicated card
- Large bandwidth oscilloscope used for jitter measurements

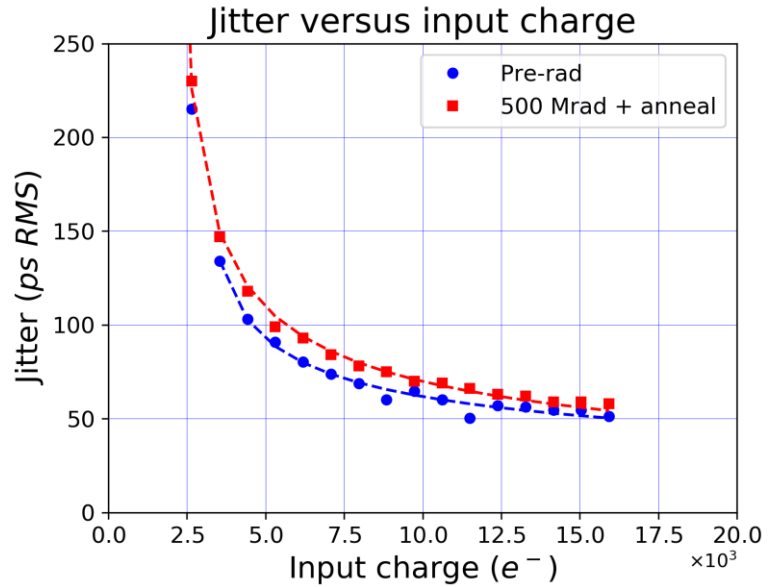
Pixel array test

- The measurements based on the histogram of **the time delay between the injection charge and the pixel output**
- For large charge (> 15 ke-),
  - the jitter level is lower than **50 ps RMS** for Cin = 100 fF
  - The jitter is **37 ps RMS** for Cin = 50 fF
- Measurements showed that the jitter level **depends** substantially on the **applied threshold** especially for small charges



Comparison of timings between different charged chip

- **TID tests** was done in close collaboration with TU-Graz
- Tests carried out at ambient temperature
- Total dose of 500 Mrad reached
- Good recovery during the annealing time
- **Shift of ~ 10ps after irrad + annealing**



Comparison of timings between pre-rad and irradiated chip

- <u>Continuation of the project :</u>
- A new 28 nm large pixel array under design and focused on :
  - TDCs implementation for time measurements (ToA and ToT)
  - Digital pixel
  - Bump bond the readout chip with sensor array
  - Submission of a 2nd pixel matrix including TDC in pixels (end of 2026)

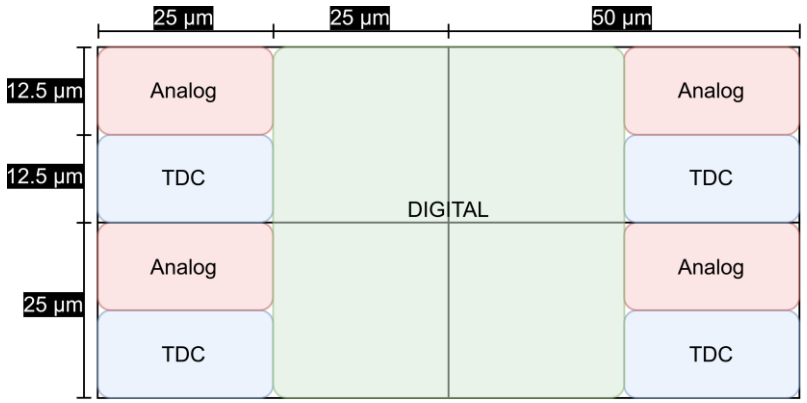
Prototype Pixel Reader 28nm

Digital Architecture

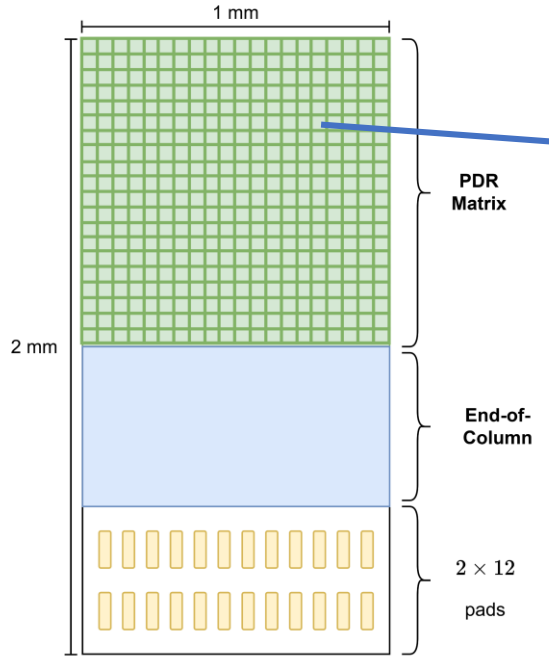
Digital Architecture 28nm:

Goal: For Extract, filter, and temporarily store precise timing (TOA) and energy (TOT)

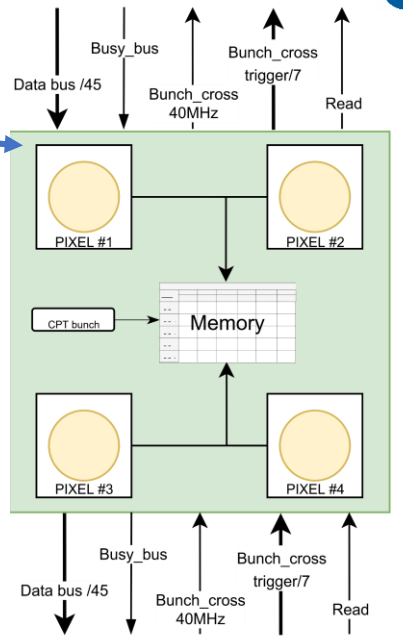
- Mutualized digital logic (Pixel Digital Region - PDR) managing 4 pixels (50x25 µm each) simultaneously to save space
- 6-bit Time of Arrival (TOA) at 50 ps precision and 8-bit Time Over Threshold (TOT) at 1ns.
- Local FIFO buffering designed to hold up to 5 events during the 12.5 µs trigger latency, statistically validated via Poisson distribution to cover >99.9% of cases
- For now current RTL synthesis occupies only 1071.7 µm², utilizing less than half of the 2500 µm² allocated budget



Floorplan of a 50 µm × 50 µm Pixel Digital Region (PDR)



Physical Layout Overview



Functional Block Diagram of the PDR

Next Steps:

- Physical Implementation: Transition to the Back-end flow (Place & Route) using Cadence Innovus and the CERN Flowkit
- Sign-off: Perform post-layout simulations, parasitic extraction, and physical verifications (DRC/LVS)
- Tape-out: Generate the final GDSII file for foundry submission

Conclusions

- The CPPM team works on hybrid pixel technologies, either for the ATLAS ITk project (RD53), the upgrade of BeIIe II proposal (TJ 180nm) or in R&D for future colliders in TPSCo 65 nm & TSMC 28 nm
- Beautiful developments have occurred in Depleted MAPS technologies **in CPPM**, with prototypes produced in 10 different technologies
- CPPM is now focusing on monolithic prototype with TJ 180nm, TPSCo 65nm technology
- Good developments and progress made by the CPPM group and others on **DRD3.1, DRD7.6, TPSCo 65 nm**
- Obtained good results for future hybrid pixel developments by the CPPM group and **in TSMC 28nm**
- **CPPM has always had very close cooperation with China. Exchange activities were resumed in 2024, and there will be more cooperation plans in the future**

Thanks for your attention

Back up slides

Proposed design

Structure based on voltage amplifier + discriminator :

- Folded cascode amplifier
- Comparator based on common source amplifier
- Ireset current source to return to the base line
- DC coupling between sensor and the FE

Folded cascode stage

- Miller effect on the gate drain capacitance reduced
- The contribution to the input capacitance reduced

DC feedback

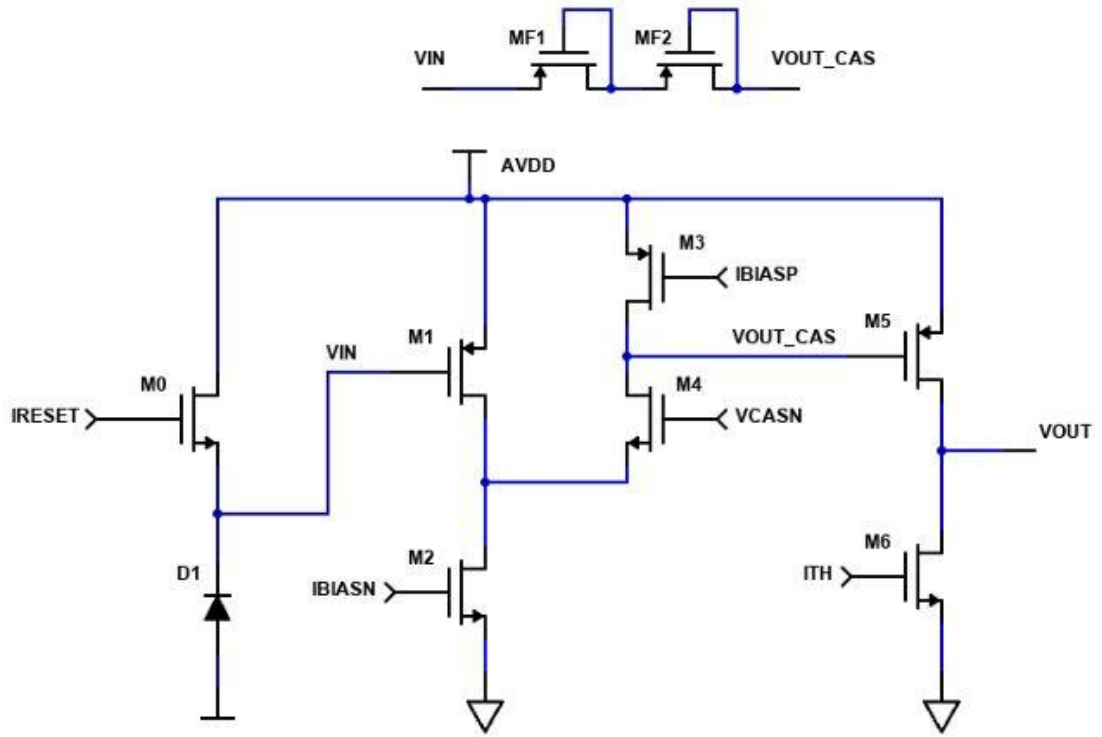
- High resistance value realized by transistors

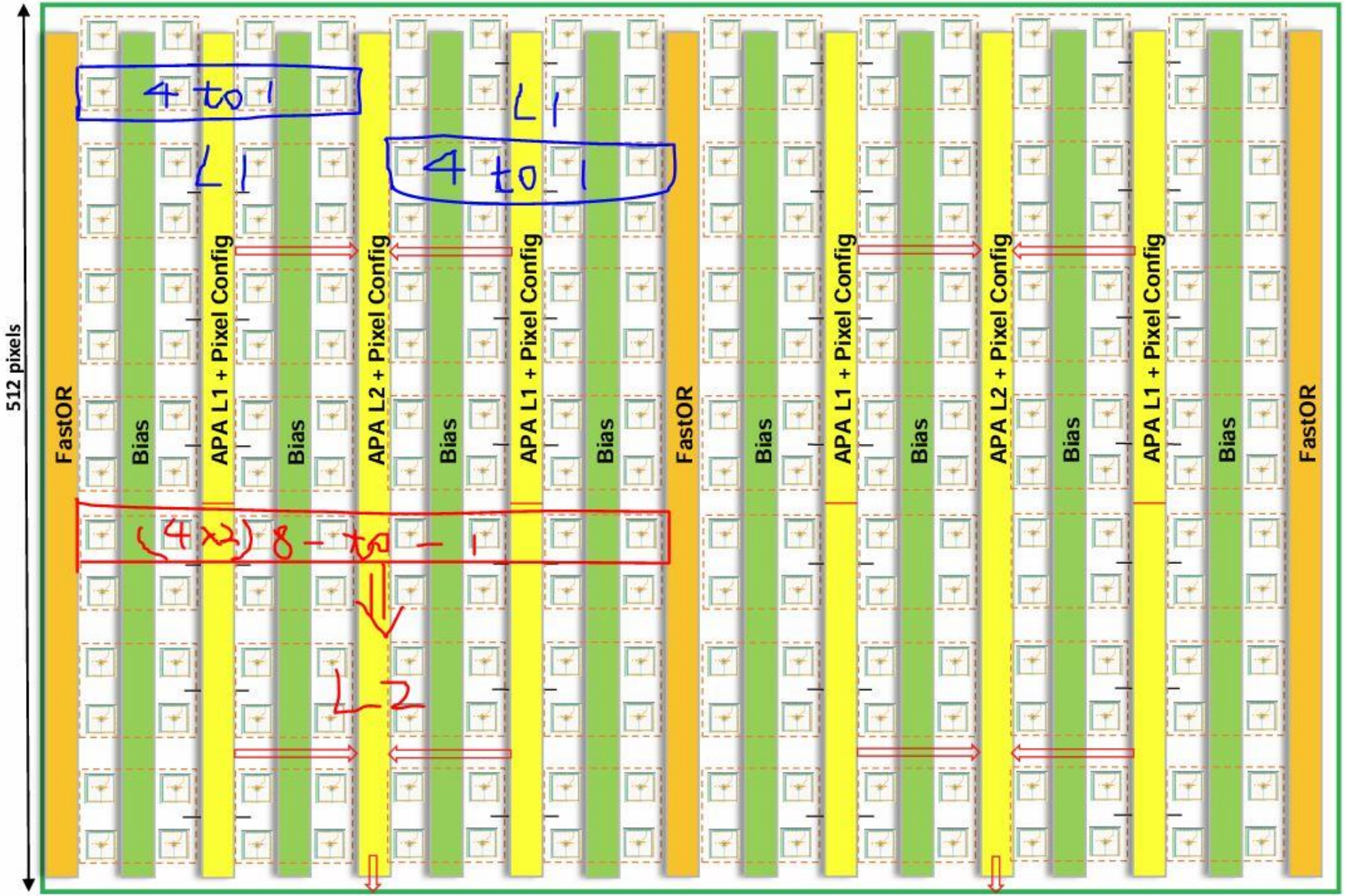
Pixel size

- 9 transistors (5 with minimum size)
- W/L from 200nm/100nm -> 200 nm/1µm

Sensor capacitance under the chosen bias is 4.5 fF

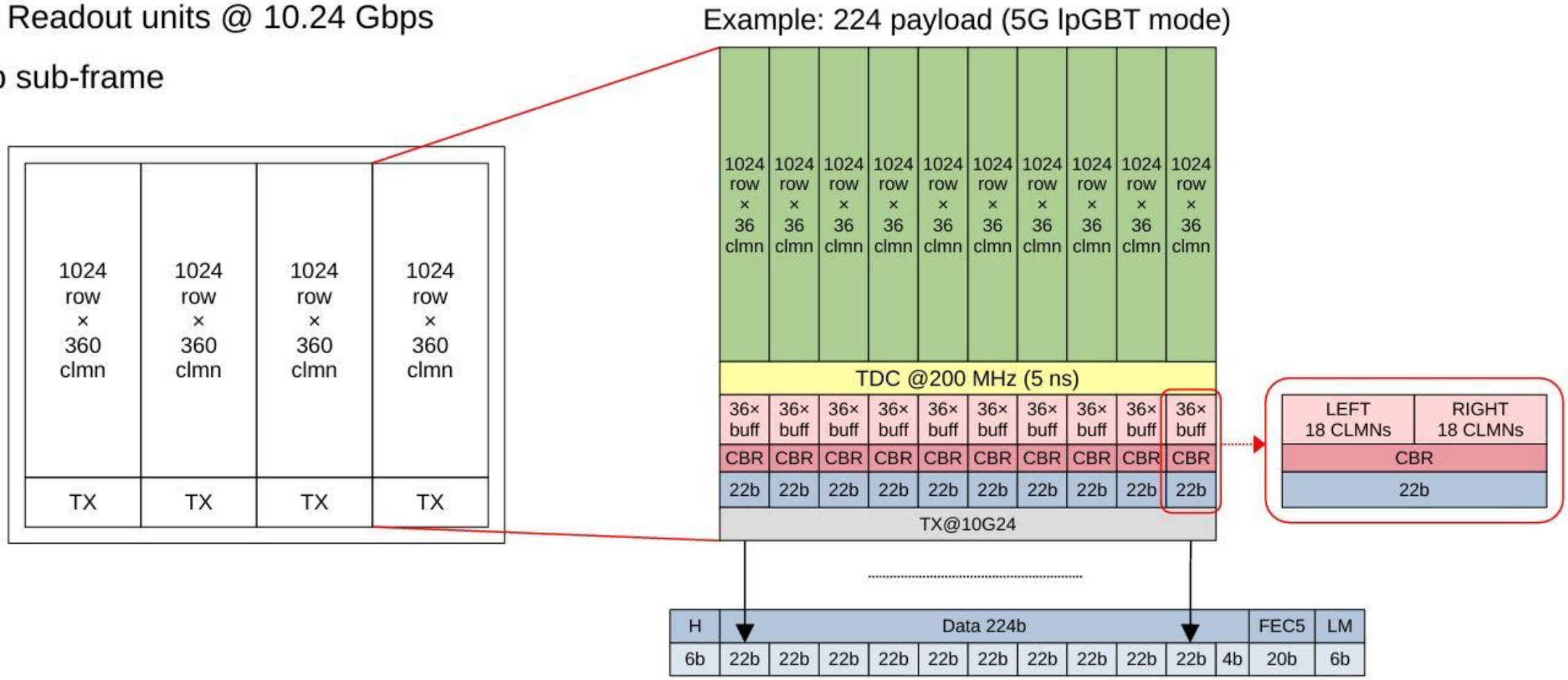
- The theoretical conversion ratio at the input is ~ 35 µV/e
- Need a high overall gain




512 pixels
FastOR
Bias
APA L1 + Pixel Config
Bias
APA L2 + Pixel Config
Bias
APA L1 + Pixel Config
Bias
FastOR
Bias
APA L1 + Pixel Config
Bias
APA L2 + Pixel Config
Bias
APA L1 + Pixel Config
Bias
FastOR
4 to 1
L1
4 to 1
L1
(4x2) 8 to 1
L2

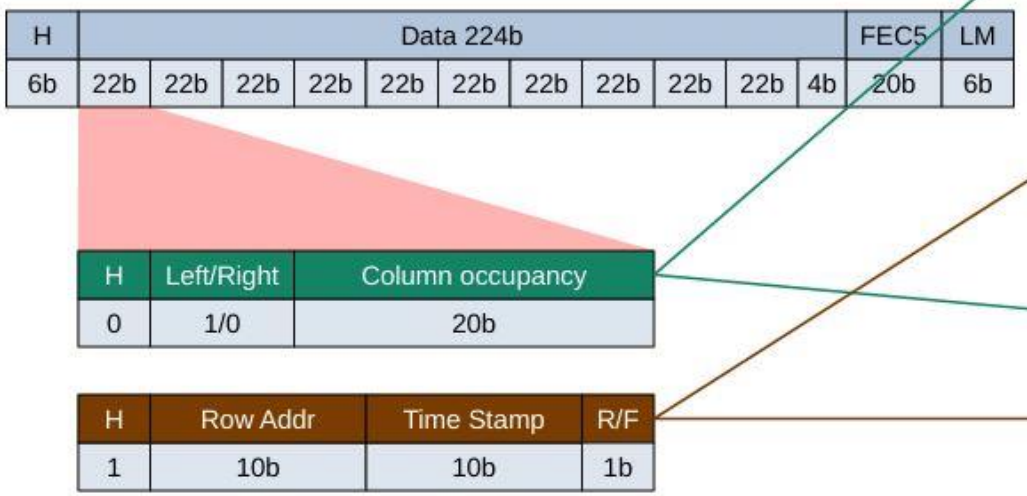
EoC – ColumnBitmapReadout (CBR)

- Matrix of 1024 × 1440 pixels
- 4 × Readout units @ 10.24 Gbps
- 22b sub-frame



EoC – ColumnBitmapReadout (CBR)

- *First:* **Full/Empty column** information
- *Then:* **Only active columns** & **Only row address**
- **Pros**:
  - CBR wins > 100 MHz/cm^2 vs. APA/ARR
  - @ 40 MHz, Fewer bits ~> Only 4 × 10.24 Gbps
- **Cons**:
  - Buffer (21b) for each column



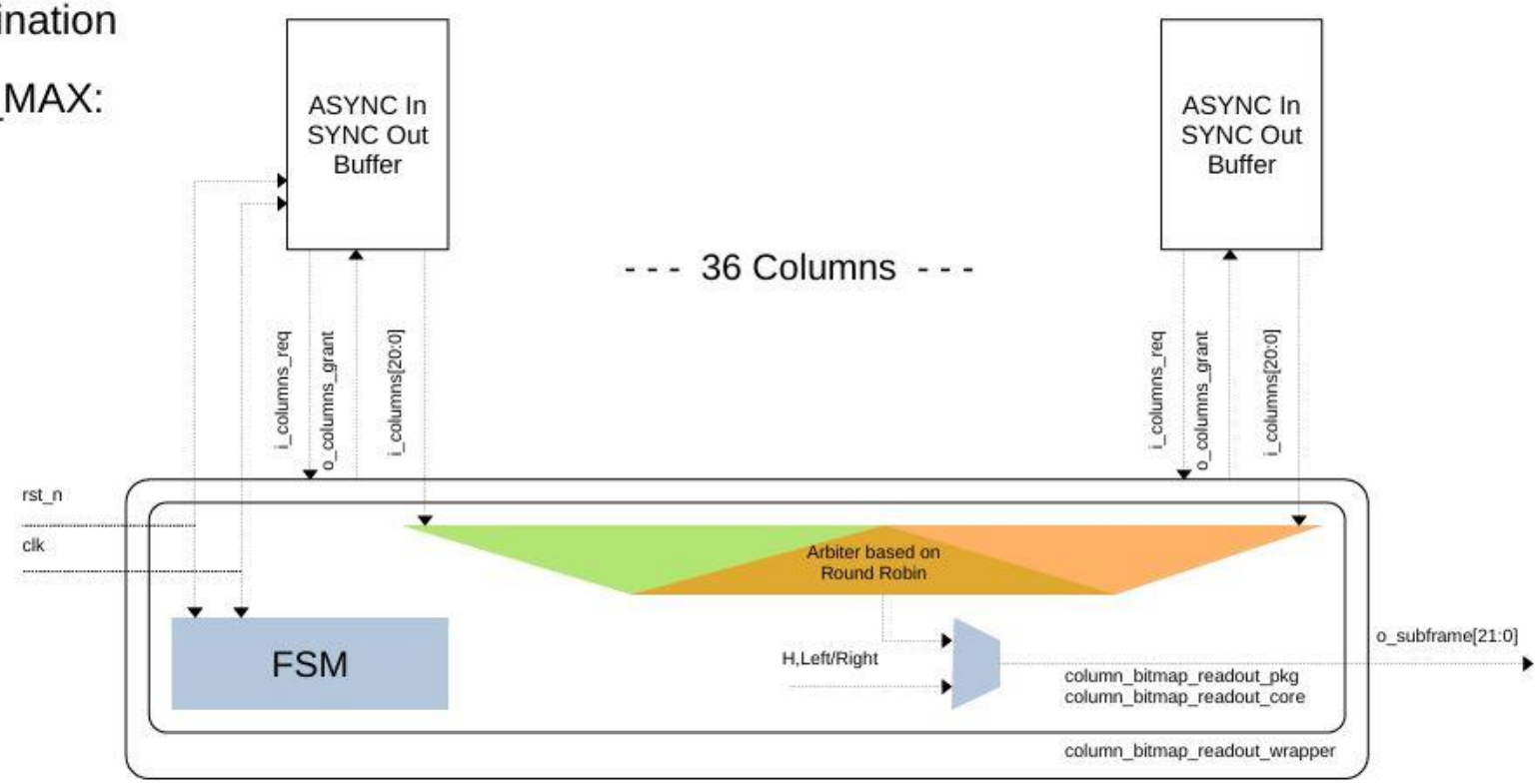
Example:

```
CLMN[35:0]=
000110011101000100000001001101100000
```

```
Time(ns)      State                Data
15591525    RIGHT  000000100110110000
15591550    LEFT   000110011101000100
15591575    GRANT  col=4  (depth=1)
15591600    GRANT  col=5  (depth=1)
15591625    GRANT  col=7  (depth=1)
15591650    GRANT  col=8  (depth=1)
15591675    GRANT  col=11 (depth=2)
15591700    GRANT  col=20 (depth=2)
15591725    GRANT  col=24 (depth=1)
15591750    GRANT  col=26 (depth=2)
15591775    GRANT  col=27 (depth=1)
15591800    GRANT  col=28 (depth=1)
15591825    GRANT  col=31 (depth=3)
15591850    GRANT  col=32 (depth=1)
15591875    RIGHT  000100010000110000
15591900    LEFT   000101110001000001
15591925    GRANT  col=4  (depth=1)
15591950    GRANT  col=5  (depth=2)
15591975    GRANT  col=10 (depth=1)
---
```

EoC – ColumnBitmapReadout (CBR)

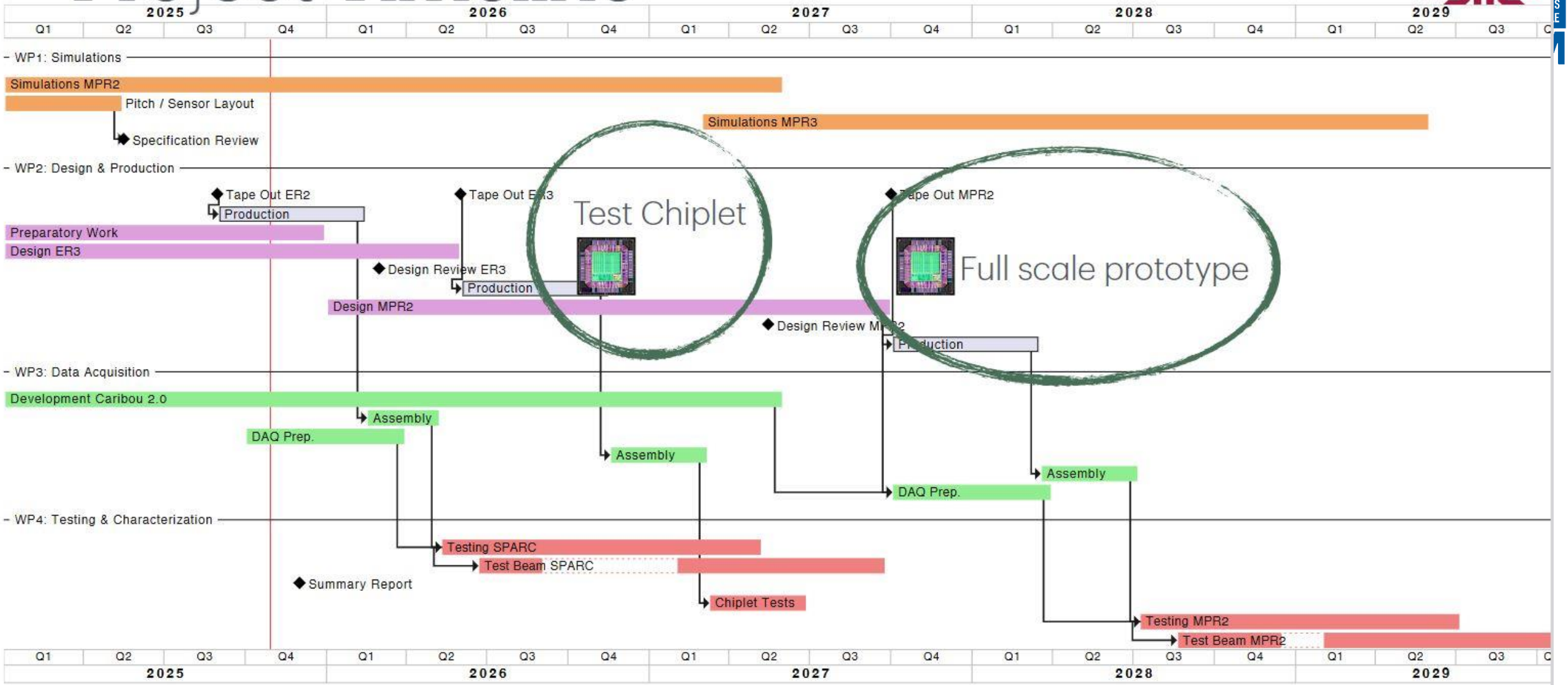
- **Done at RTL and Gate level**
- Parameterized – Any payload combination
- TPSCo65 Synthesis - sc_12T_LVT_MAX:
  - CLK: @ 40 MHz
  - Slack: +16 ns
  - Cell-Count: 974
  - Total Area: 5634 um2
    - 36clmn x 20um = 720 um
    - <10 um height



column_bitmap_readout_wrapper module
Merge 36 columns into one subframe (22 bits) of lpGBT frame (256 bit, payload data 224 bit)

Done at RTL and Gate level
eoc/doc/architecture.md

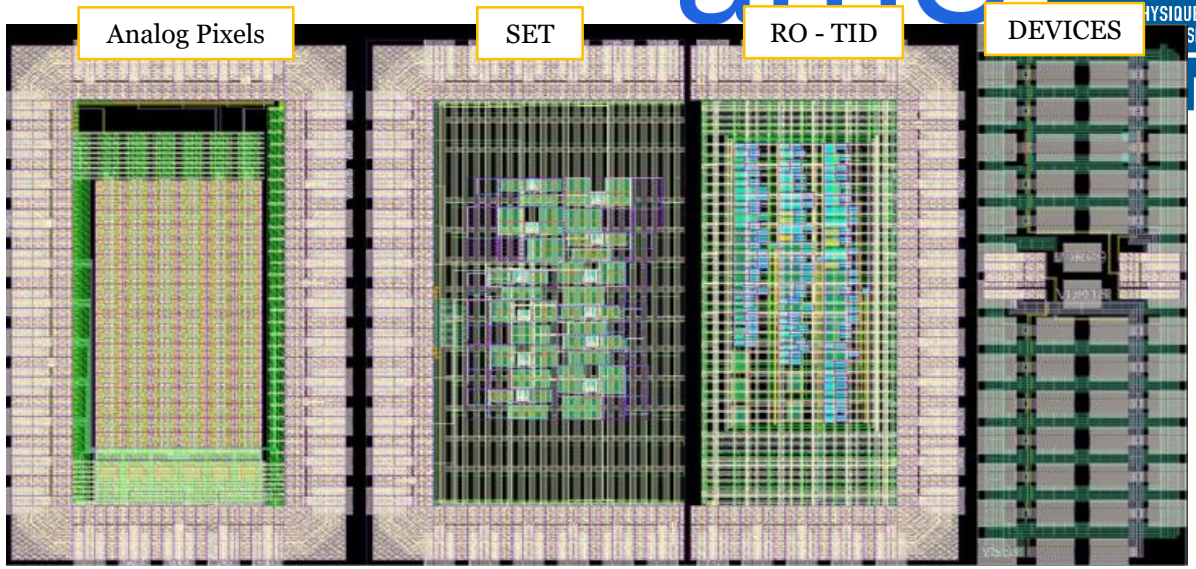
Project Timeline



S. Spannagel

TSMC 28nm activity

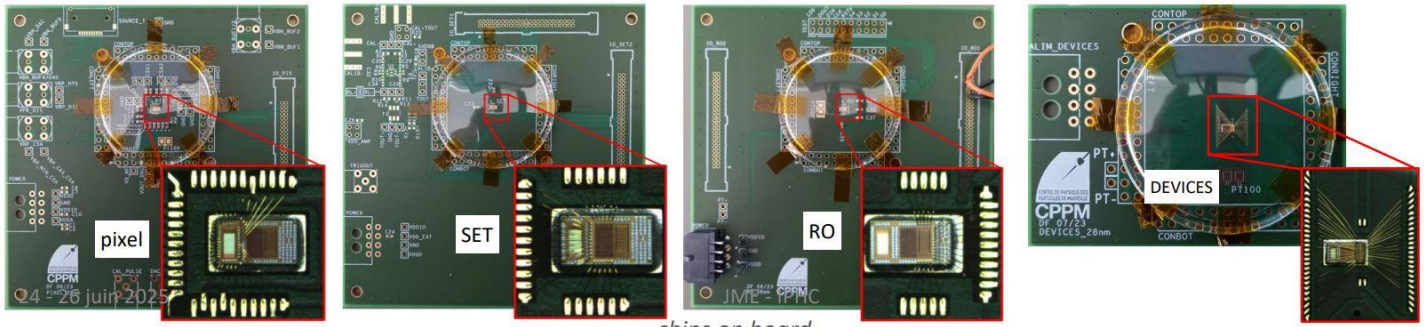
- Done **with the CERN R&D Program** on technologies for Future Experiments
- **CPPM is a member of two working groups within the DRD** (ECFA) projects: WG 7.3a & WG 7.4b
- **For future upgrades and future colliders**
- **Higher requirements**:
  - Time resolution,
  - High hit rate,
  - Larger data links,
  - Small pixel size, etc
  - New technologies need to be applied



4 sub-chips of 2×1 mm² submitted December 22

Implemented Structures:

- **Pixel_28nm**
- **RO_28nm**
- **SET_28nm**
- **DEVICES_28nm**
- **Each chip is bonded on its own board (ball bonding)**



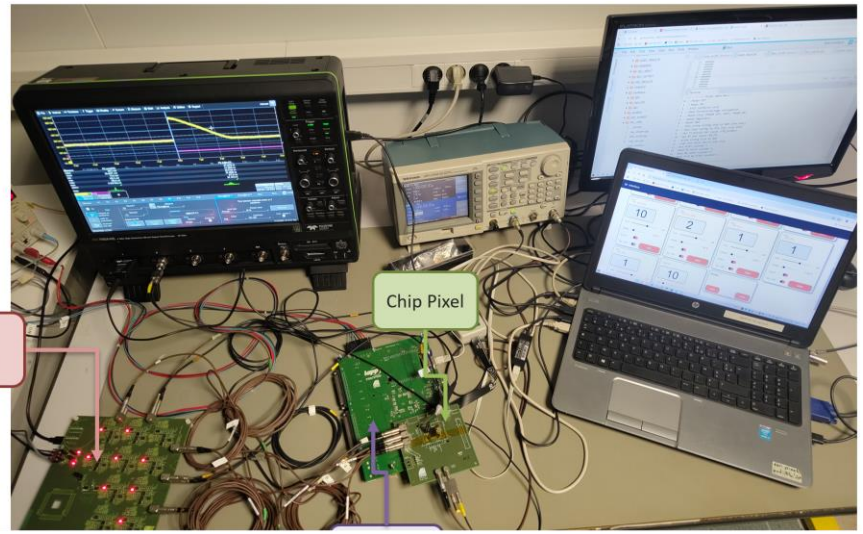
chips on board

The 28nm prototype was received in June, 2023

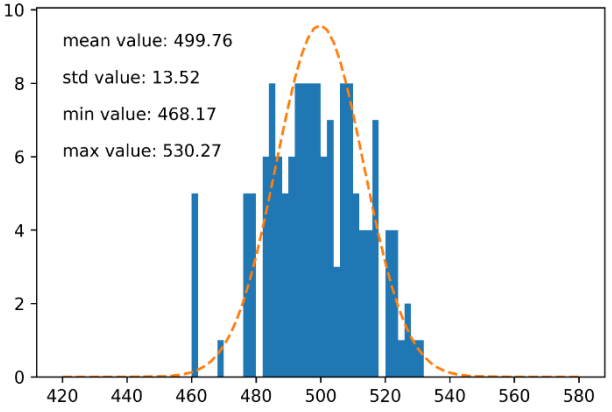
Test results for 28nm

Pixel_28nm

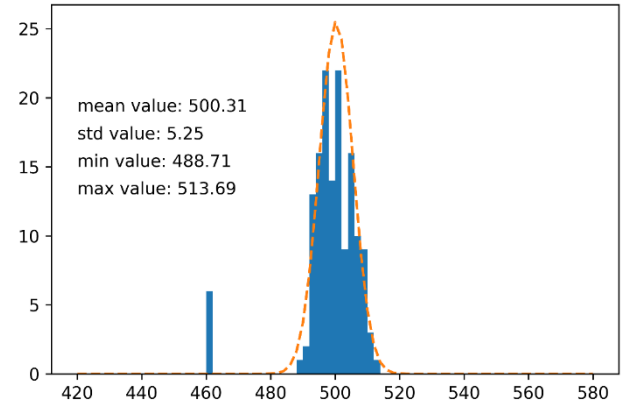
- Process qualification in terms of performance for analog, low power and low noise circuits
- **Goals of this pixel matrix design**
  - Study the limits to time resolution in analog front
  - Bandwidth, Noise, Current bias, power supply
- Threshold scan and tuning
  - CSA base line ~ 300 mV
  - After tuning : RMS value = 130 e^- -> 52 e^-
- Noise and time resolution measurement



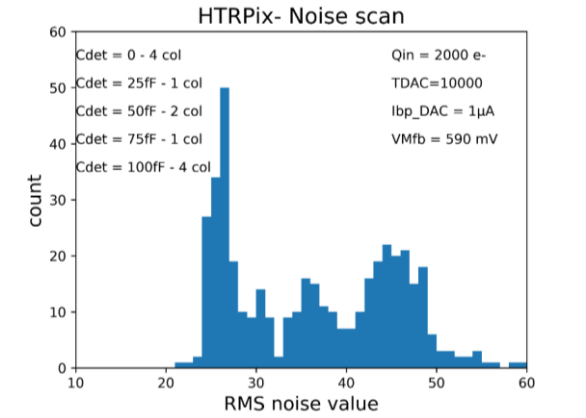
Pixel test bench



Before tuning



After tuning



•charge	•Jitter (simulated)	•Jitter (measured)
•Q > 4 ke-	•< 100 ps	•< 150 ps(*)
•Q > 10 ke-	•< 50ps	•< 100 ps(*)

Test Results for Pixel_28nm

SET_28nm

- 2 different parts in the SET chip: Target cells & Width measurement
- Same architecture used in the RD53_SEU chip
- Need a beam time (3 ~ 4 hours), test bench is ready now
- **Goal: define a time width to mask on sensitive nodes**

Test results for 28nm

RO_28nm

- **Goal: For TID effect Study of Digital Technology Cells**
- INV, NAND, NOR, and DELAY are implemented
- Bug on enable management: can't test it in static mode
- Each cell is connected to its proper counter

Time Propagation

Measurements on 10 chips

All digital cells: propagation time 5~20 ps

12T more faster than 7T (SVT)

VDD variation

Measurements on 1 chip

HVT cells more sensitive than LVT

7T cells show a VDD dependence higher than 12T

Test objects:

Cell Size 7T / 9T / 12T

Flavours SVT / HVT / LVT

Temperature variation

Measurements on 1 chip

Temp setting : -20 ~+50°C (step of 5 °C)

LVT cells show a higher variation

No difference between size

TID measurements

Measurements on 1 chip

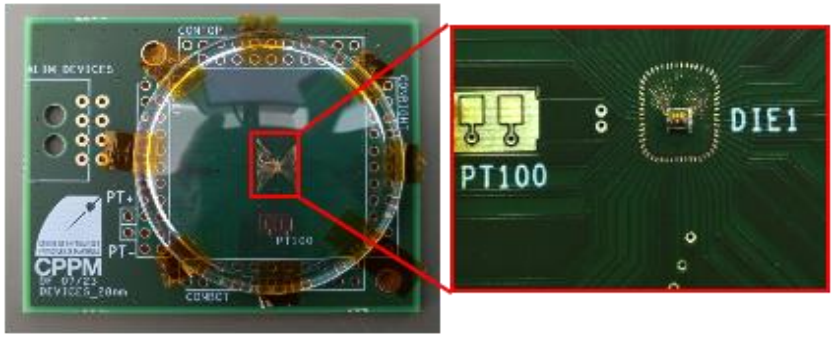
10 keV X-ray source calibrated with a PIN diode

HVT cells are more sensitive than others

Redo TID tests in 2025 on another chip

DEVICES_28nm

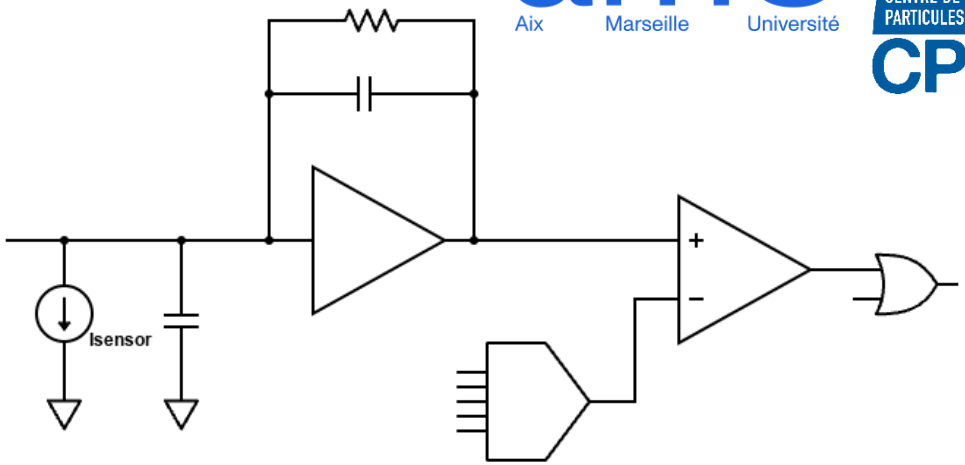
- **Goal: automatic extraction of transistors parameters for each channel valid**
- Transistors test bench includes:
  - 4 SMU's (Keithley - 4201+PA)
  - 4 switches matrix boards (Keithley-7174A)
- Devices implemented on the chip without ESD protections
- **New test just started from July, 2025**
- **28 chips will be tested**

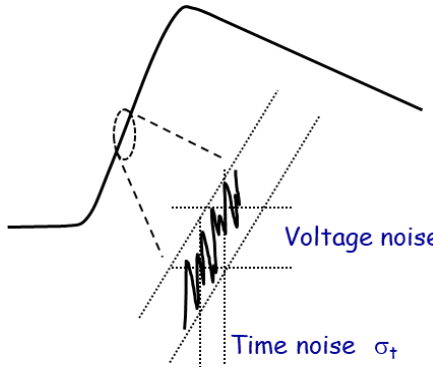


Pixel array prototype

- Study the **limits to time resolution** in the analog front- end designed with the 28 nm CMOS process
  - Effects of the Current bias, power supply, bandwidth, Noise
- The total jitter for the pixel output

- σ_{FE} is the jitter related to the **electronic** front-end including the **sensor**
  - Proportional to the voltage noise at the amplifier output
  - Inversely proportional to the output signal variation rate (slew rate)
- Minimizing the front-end jitter corresponds to :
  - Small C_{in} → small pixel area → minimize the noise of the charge amplifier
  - Small rise time → high amplifier bandwidth and high speed sensor
  - Large input charge Qin





$$\sigma_{jitter} = \frac{\sigma_{Vn}}{dV/dt}$$

$$\sigma_{jitter} = \frac{C_{in}}{Q_{in}} \sqrt{\frac{t_r^2 + t_s^2}{t_r}}$$

t_r : the amplifier rise time

t_s : the drift time of the charge in the sensor

Q_{in} : input charge

$C_{in} = C_s + C_{CSA\text{-}input}$