DAQ for upgraded Belle II vertex detector Front-End readout system 17th FCPPN/L workshop June 30 of 2026

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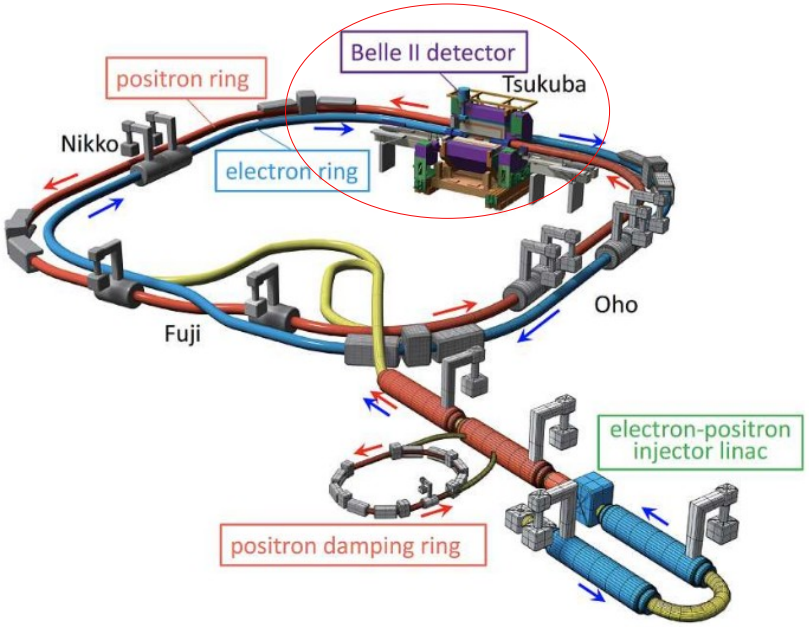
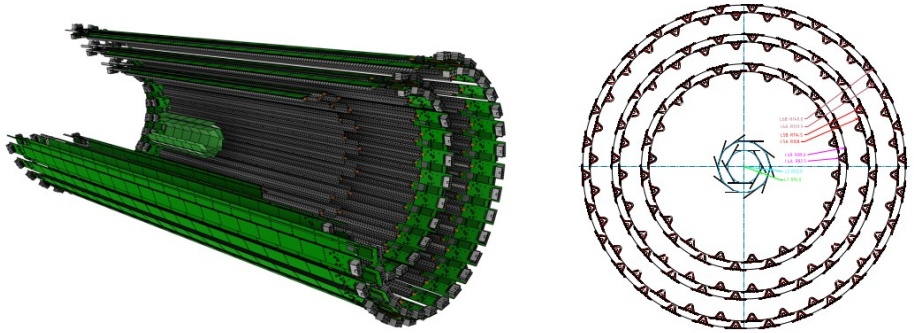
Introduction



Belle II experiment at SuperKekB collider

- Located at KEK, Tsukuba, Japan.
- Electron Positron accelerator.
- Plan to be upgaded to reach the target luminosity $L = 6\ 10^{35}\ cm^{-2}\ s^{-1}$
- Upgrade is plan during Long shutdown estimated in 2032.

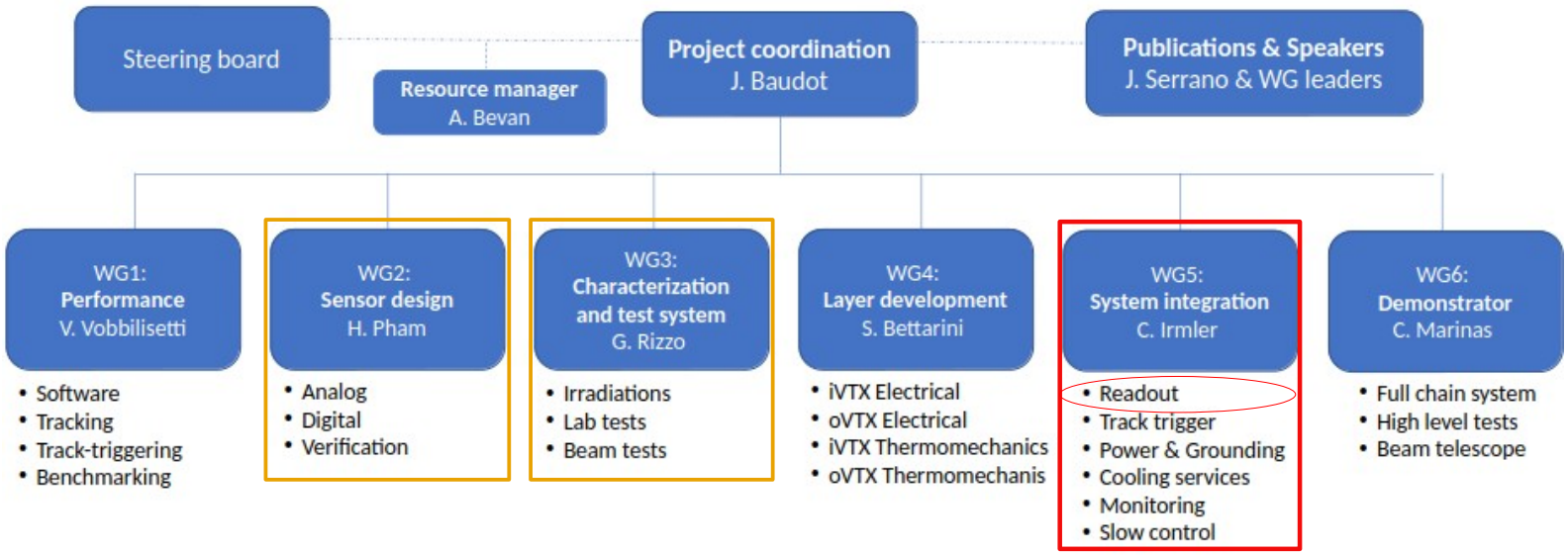
VTX Architecture of 5 detection layers



The upgraded vertex detector (VTX)

- Actual vertex detector (PXD+SVD) :
  - . 2 layers of Pixel Detector.
  - . 4 layers of Silicon Detector.
- Proposal to upgrade by a full DMAPS detector :
  - . Depleted Monolitic Active Pixels sensors.
  - . Geometry of 5 detection layers.
  - . Better resolution < 15um.
  - . Low material budget for perpendical tracks L1 & L2 0.3% X0/L, L4 to L6 0.6%X0/L.
- Obelix Chip in Tower Jazz 180nm technology is under development.
- A new readout system is under developement.

Belle II VTX organisation



Collaboration, 25 institutions of 9 countries.

CPPM contributions :

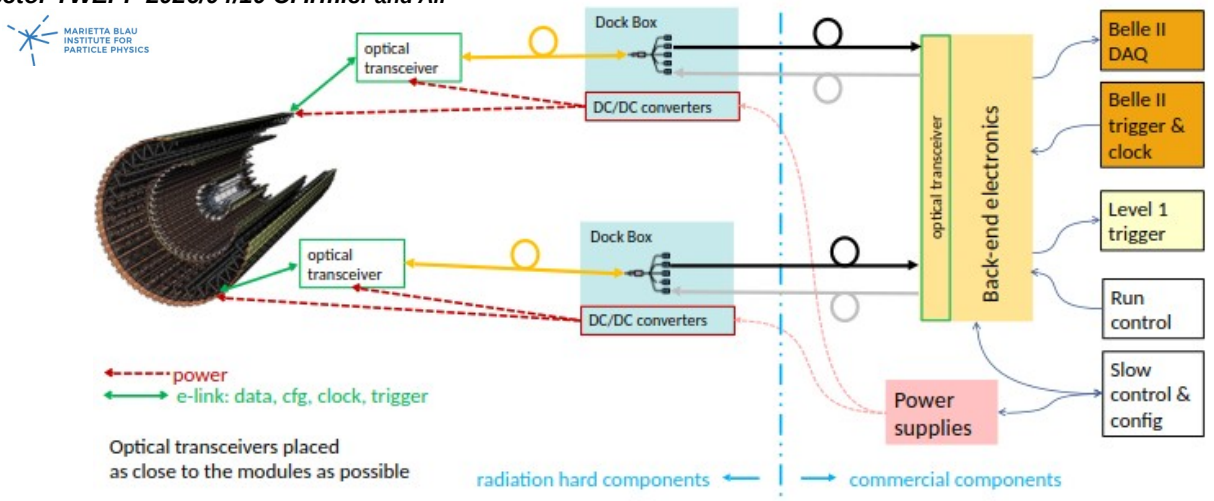
- WG2 : Sensor Design
  Development of Obelix Chip, see Danwei's talk.

- WG3 : Characterisation and system tests
  Test and characterisation of TJ-Monopix2 and Obelix chip.

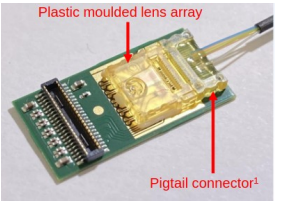
- WG5 : System integration
  Development of the front end readout for inner layers.

VTX readout concept

Ref : Readout concept of the future Belle II vertex detector TWEPP 2026/04/10 C. Irmler and Al.



VTRX+
4 VCELs TX
1 Photodiode RX



Front-end readout

- Place between the VTX and back-end system
- Close to VTX, should be Rad-Hard (TID of 100 Mrad)
- Supply clock and forward configuration to Obelix chips via copper links
- Acquire data from Obelix Chips via copper links (Hit and track trigger)
- Provide high speed links to back-end system using optical fibers.
- Provide monitoring features for temperature reading

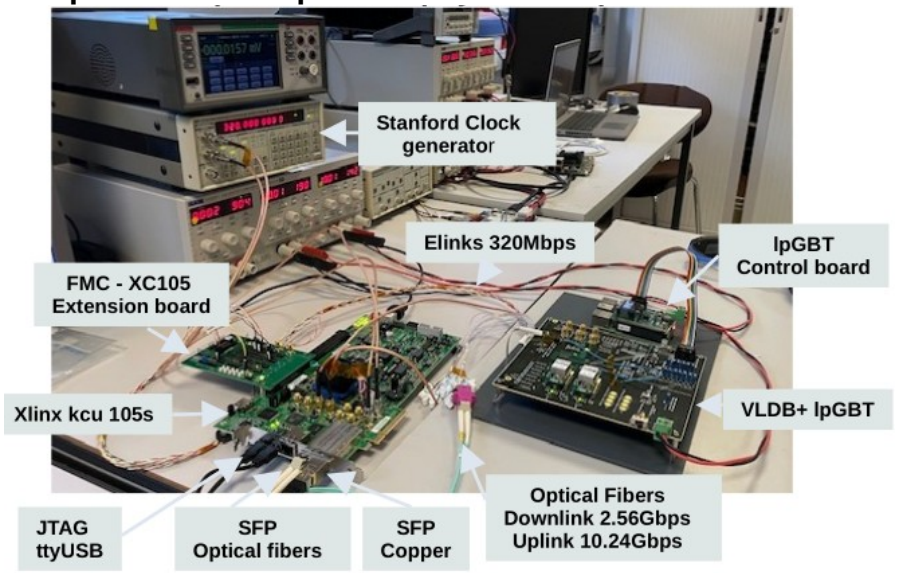
lpGBT chip associated to VTRx+ optical transceiver is a good candidate

- Developped by CERN in 65nm CMOS technology for LHC experiments
- Range of Ref Clock
  fmin = 39Mhz fmax = 41Mhz
- Belle II use a Ref Clock
  RF/12 = 508.887MHz/12
  = **42.40725 MHz**

Out of specs, need to be qualified to be used in Belle II

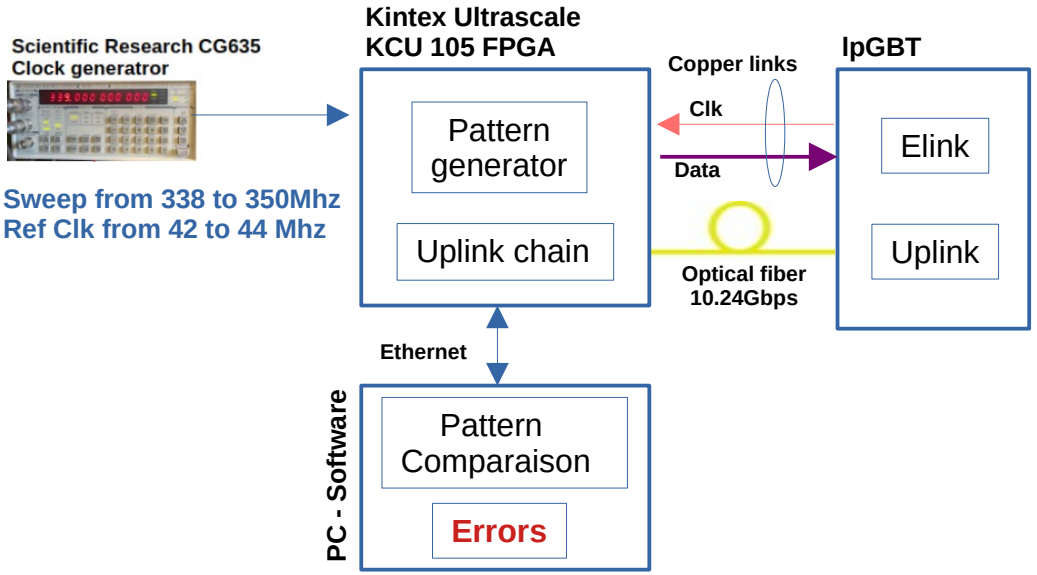
lpGBT qualification test setup

lpGBT test setup



Tests have been carried out using VLDB+ lpGBT evaluation board, developped by CERN, associated with Xilinx board kcu105, a Kintex Ultrascale FPGA.

A low jitter Stanford clock generator as a reference clock

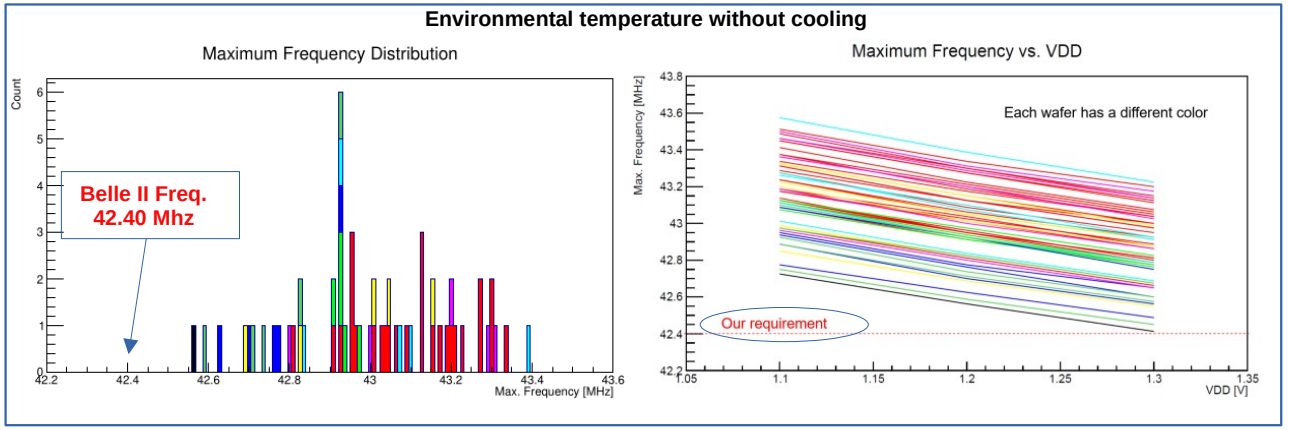


Loop back test : lpGBT and FPGA

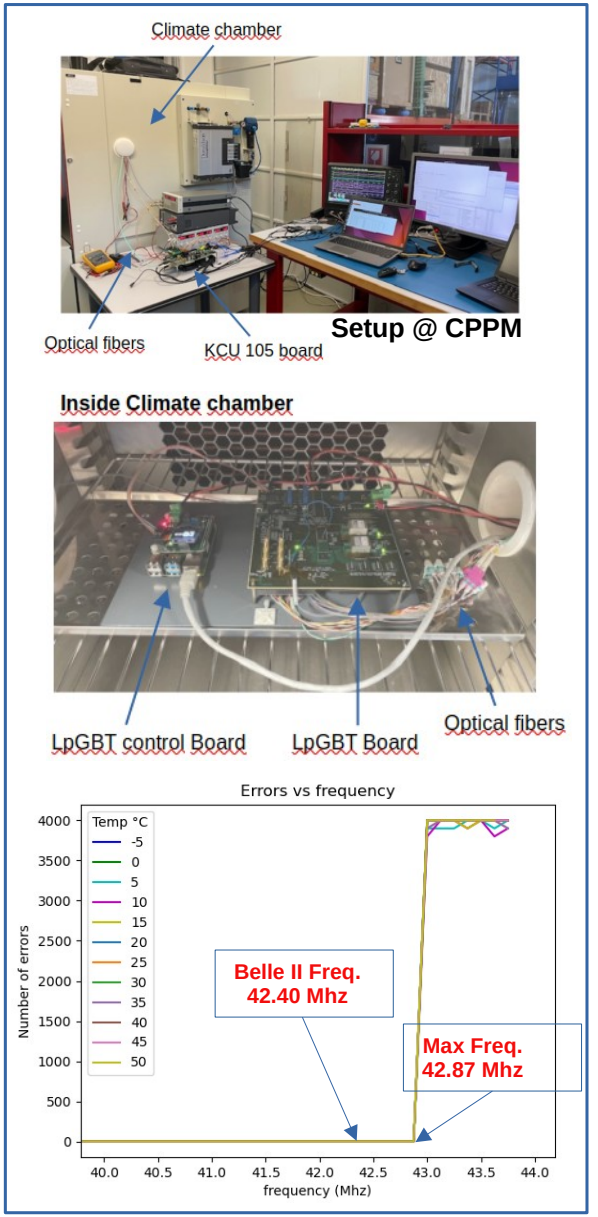
- Patterns are generated by the FPGA emulating Obelix data and sent to lpGBT via copper link.
- The lpGBT transmits data via high speed optical link @ 10.24Gbps (uplink) .
- PC reads data from FPGA via ethernet connection and makes comparison with original pattern
- If data is different from original pattern, errors are calculated.
- Test is made for different values of Ref Clk frequencies

lpGBT max frequency results

MBI lab measurements
Ref : Markus Friedl, Christian Irmler



Max Freq vs temperature tests @ CPPM



Test of 61 lpGBT chips from 8 differents wafers

- Test at ambient temperature without cooling.

- All chips achieved at a maximun frequency **> 42.55 Mhz**, which is above the required value.

- Tests made for values of VDD of 1.1V, 1.2V, 1.3V, show that maximum frequency improves when decreasing VDD.

Test of 1 lpGBT in a climate chamber

- Test from -5 to 50 °C step of 5°C.

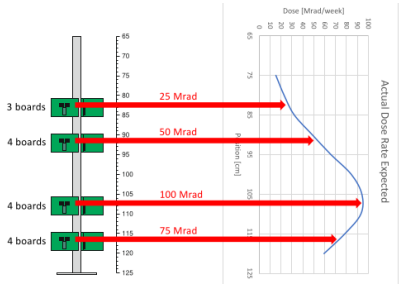
- Max frequency measured of **42.87 Mhz.**

- Temperature has no impact on the maximum frequency value.

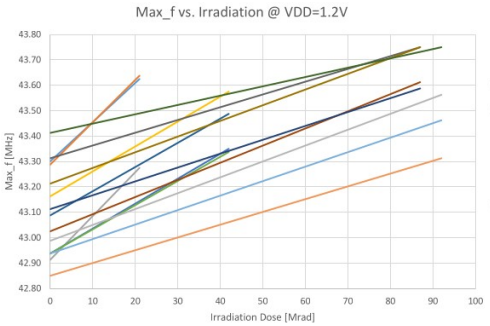
lpGBT irradiation results

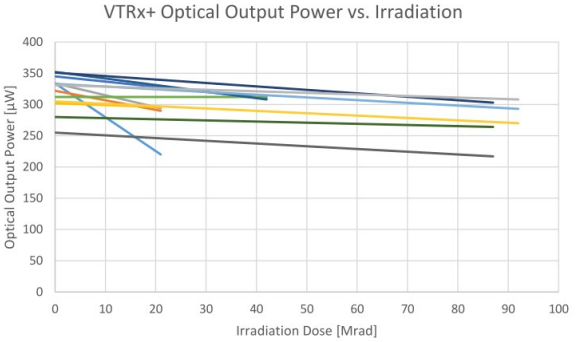
MBI measurements
Ref : Markus Friedl, Helmut Steininger, Christian Irmler

Gamma Irradiation @ SCK-CEN (Mol, Belgium)
- Cobalt-60 irradiation (up to) 100 Mrad (=1 MGy)
- 15 lpGBT under biasing and 8 VTRx+

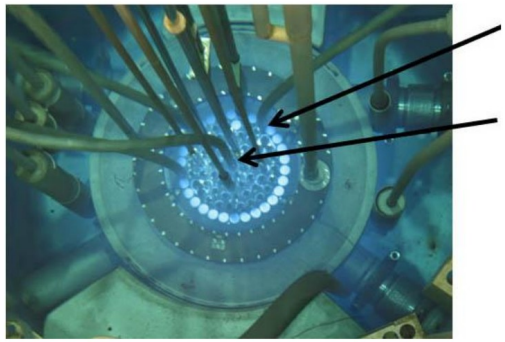


Max frequency of lpGBT getter better of 1 %
Optical power of VTR+ reduced by ~15%

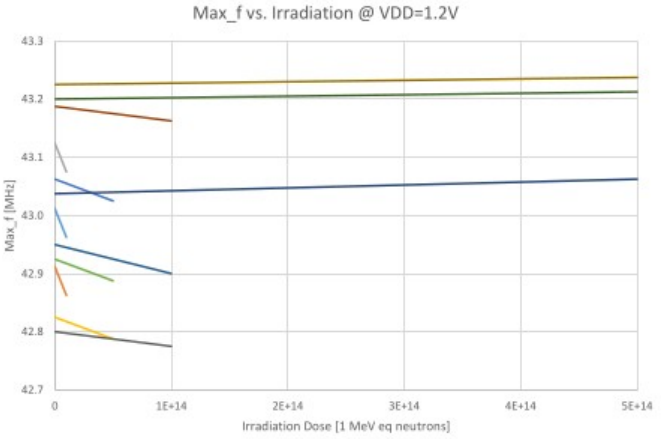




Neutron Irradiation @ Ljubljana (Triga Mark II reactor)
- 12 lpGBT bare chips without powering
- Dose of 1e13, 5e13, 1e14, 5e14 cm-2 1 MeV neutron equivalent



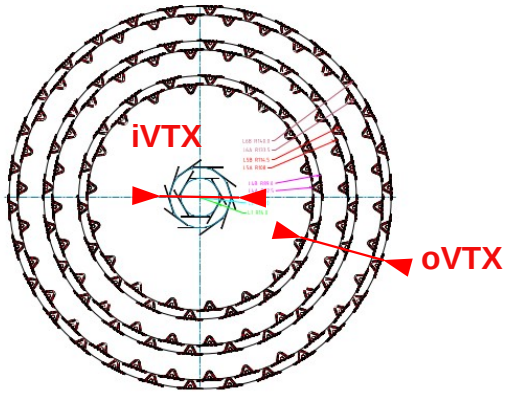
lpGBT maximum frequency decreased by ~0.1%

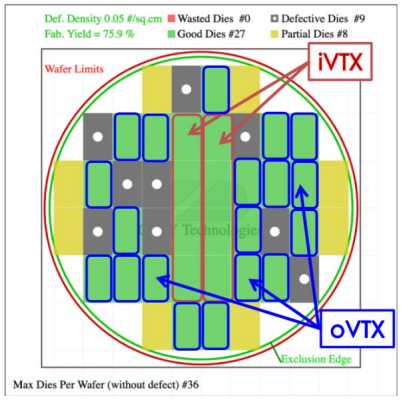


Integration of lpGBT in Belle II VTX

Layer	L1	L2	L3a/b	L4a/b	L5a/b
Configuration	iVTX		oVTX		
Radius	14.0	22.0	82.5/89.0	108.0/114.5	133.5/140.0
# Ladders	6	10	36	48	60
# Sensor/module	4	4	12/13	16/17	20

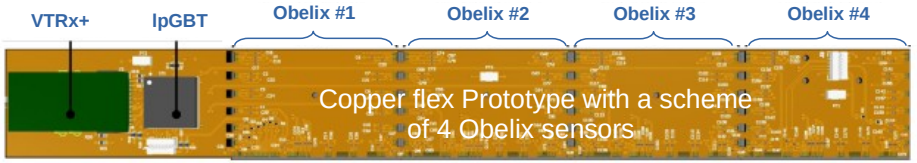
VTX design
Architecture of 5 layers



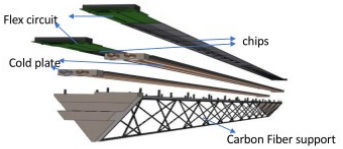


oVTX (3 outer layers): L3 to L5

Mounted on omega shaped carbon-fiber support, cooled by liquid.
Chips are Individually diced and placed on a flex, wire bonded then mounted on carbon support.
lpGBT chips and the VTRx+ tranceivers will be placed on a same flex.



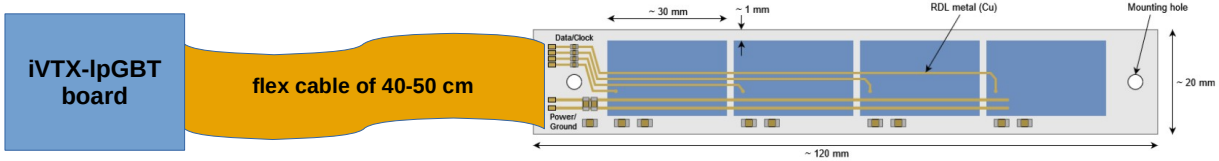
oVTX dummy flex design
Ref : INFN Pisa



Exploded view of the oVTX

iVTX (2 inner layers): L1 and L2

A ladder is a block of four consecutive Obelix chips placed on a flex.
Self supported with passive conduction cooling.
lpGBT and VTRx+ will be placed 40-50cm away from sensor, due to lack of space.



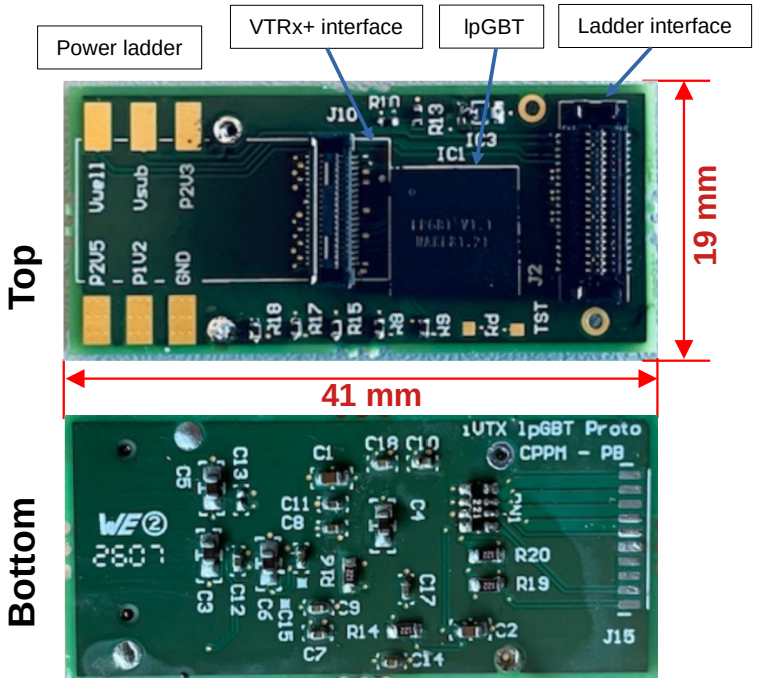
Front End readout board
place 40-50cm away

iVTX ladder demonstrator
Ref : Andreas Ulm, Univ. Bonn SiLab

iVTX lpGBT board prototype

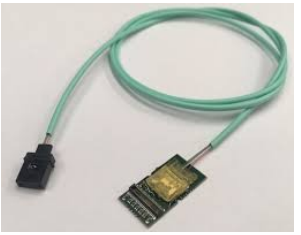
Current patch panel, PCB of 42 x 25 mm²

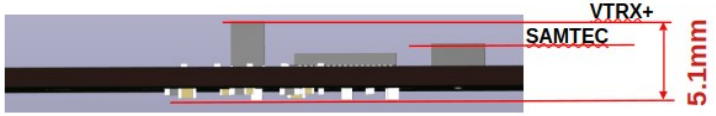
CPPM development



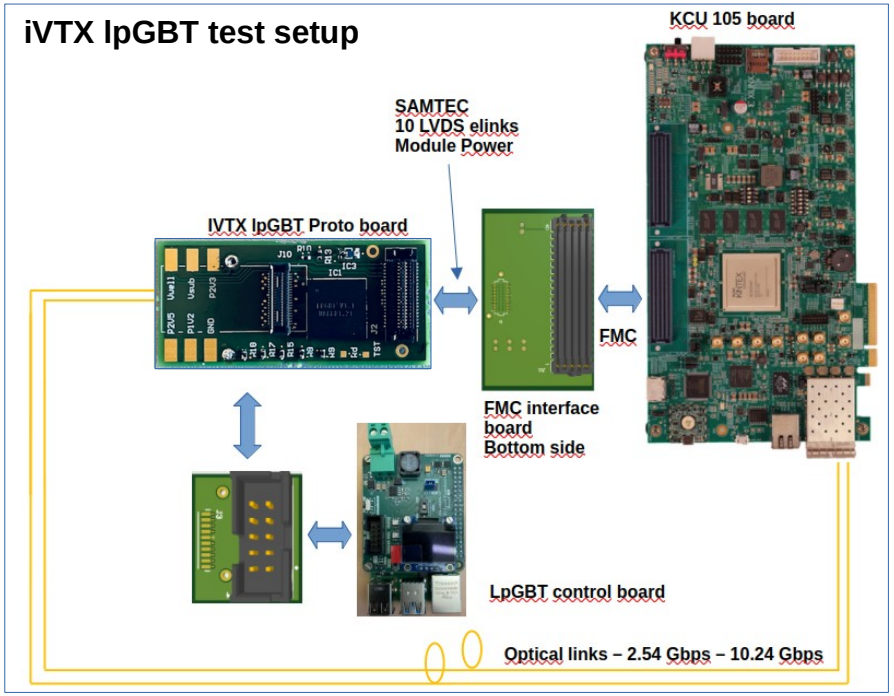
VTRx+
- 4 VCELS
- 1 Photodiode

High speed optical links





iVTX lpGBT test setup



Summary

- lpGBT associated to VTRx+ is a candidate for the Belle II readout system.

- Belle II Ref clock RF/12 = 508.887MHz/12 = **42.40725 MHz**

- lpGBT can be used in Belle II as front end system.
  . 61 lpGBTs operate at a maximum frequency > **42.55 Mhz.**
  . The temperature has no impact on the maximum frequency.
  . Gamma irradiation shows that the max frequency get better by 1 %
  . Neutron irradiation shows a max frequency degration of 0.1 %

- iVTX lpGBT Proto board has been developed and is still under test :
  - Consumptions are OK,
  - Downlink and uplink communications are validated
  - Still e-links communication under test.
  - The goal is to produce 16 iVTX_lpGBT boards + spares in a final version.