



Development of the upgraded Belle II vertex detector

**17th France–China Particle Physics Network/Laboratory Workshop
(FCPPN/L 2026)**

June 29 – July 3, 2026, Lyon

Yunpeng Lu

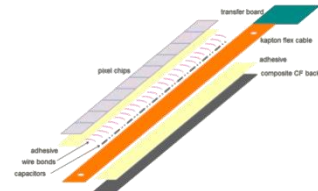
on behalf of the VTX development teams

Overview of collaboration

- Starting from 2010, common R&D efforts of MAPS for the e^+e^- collider experiments: **BES III upgrade, ILC/CEPC, BELLE II upgrade**

1、The prototype of CMOS pixel detector for the upgrade of BESIII-inner tracker

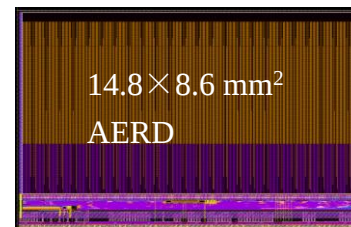
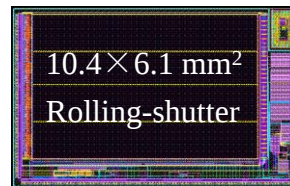
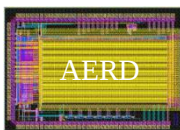
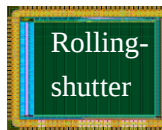
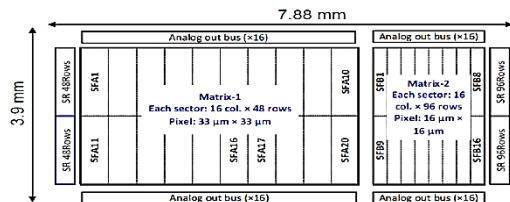
- ✓ Development of pixel detector ladder based on the MIMOSA28 sensors from IPHC
- ✓ common participation of beam test at DESY, to validate the ladder performance, space resolution, material budget, ...



Ref.: NIMA924(2019)287-292, NIMA986(2021)164810

2、CMOS Pixel Sensors R&D for future e^+e^- colliders: *pixel sensor and double-sided ladder development*

Since 2015, **four engineering runs** have been shared with TJ 180 nm CIS process



2015: JadePix-1

2017: JadePix-2/MIC4

2020: JadePix-3

2022: JadePix-4/MIC5

Development of the upgraded Belle II vertex detector

Outline

- Introduction
 - VTX upgrade proposal for Belle II
- Participation of China group
 - Physics performance
 - Optimized BELle II pIXel sensor (OBELIX)
 - Backend electronics and TDAQ system
- Summary

■ Physics program @ SuperKEKB with Belle II

- Thorough test of Std Model
- Direct/indirect search for New Physics
- Hadronic Physics

} with billions of $B\bar{B}$, $c\bar{c}$, $\tau\bar{\tau}$ pairs
In “clean” environment of B-factory

⇒ The Belle II physics book
[PTEP 12 \(2019\) 123C01](#)

- Based on accumulation of 50 ab^{-1} of e^+e^- at $\sqrt{s} = M_{Y(4S)}$
– requires instantaneous luminosity close to $6 \times 10^{35} \text{ cm}^{-2}\text{s}^{-1}$



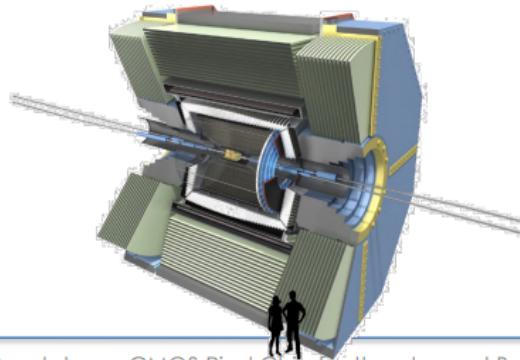
SuperKEKB collider implementing
the nano-beam scheme @ high currents



High collision rate High beam-induced bkg

■ The Belle II experiment

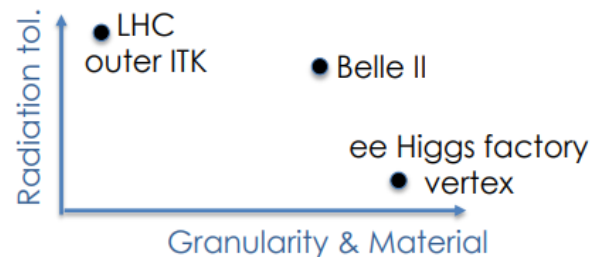
- “classical” B-factory detector + enhanced features



■ The vertex detector (VXD)

- Better vertexing ← lower boost
- Smarter tracking ← higher hit rate

+ Harsher radiation environment
+ Belle II trigger rate ~ 30 KHz

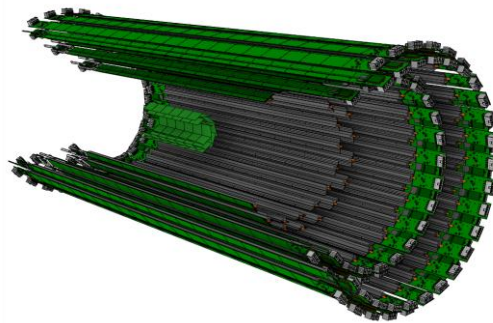
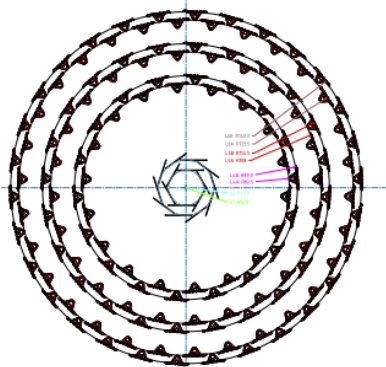


➔ Proposal for replacement of VXD = PXD (DEPFET sensors) + SVD(Double Sided Strip Detector) by VTX detector.

VTX proposal

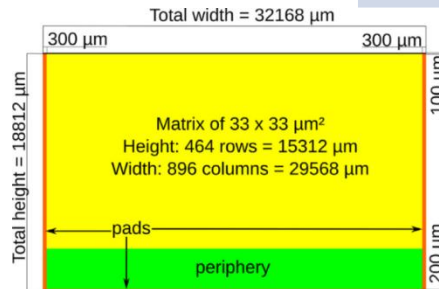
Proposed BELLE II VXT upgrade scheme

- 5 straight layers with **Depleted Monolithic Active Pixel Sensors**
- Identical chips on all layers: Optimized BELle II pIXel (OBELIX) sensor
- $\sim 1\text{m}^2$ silicon surface



OBELIX

- Tower 180 nm process
- Extension of TJ-Monopix2
→ OBELIX sensor
- $<40\ \mu\text{m}$ pitch, 100 ns integration



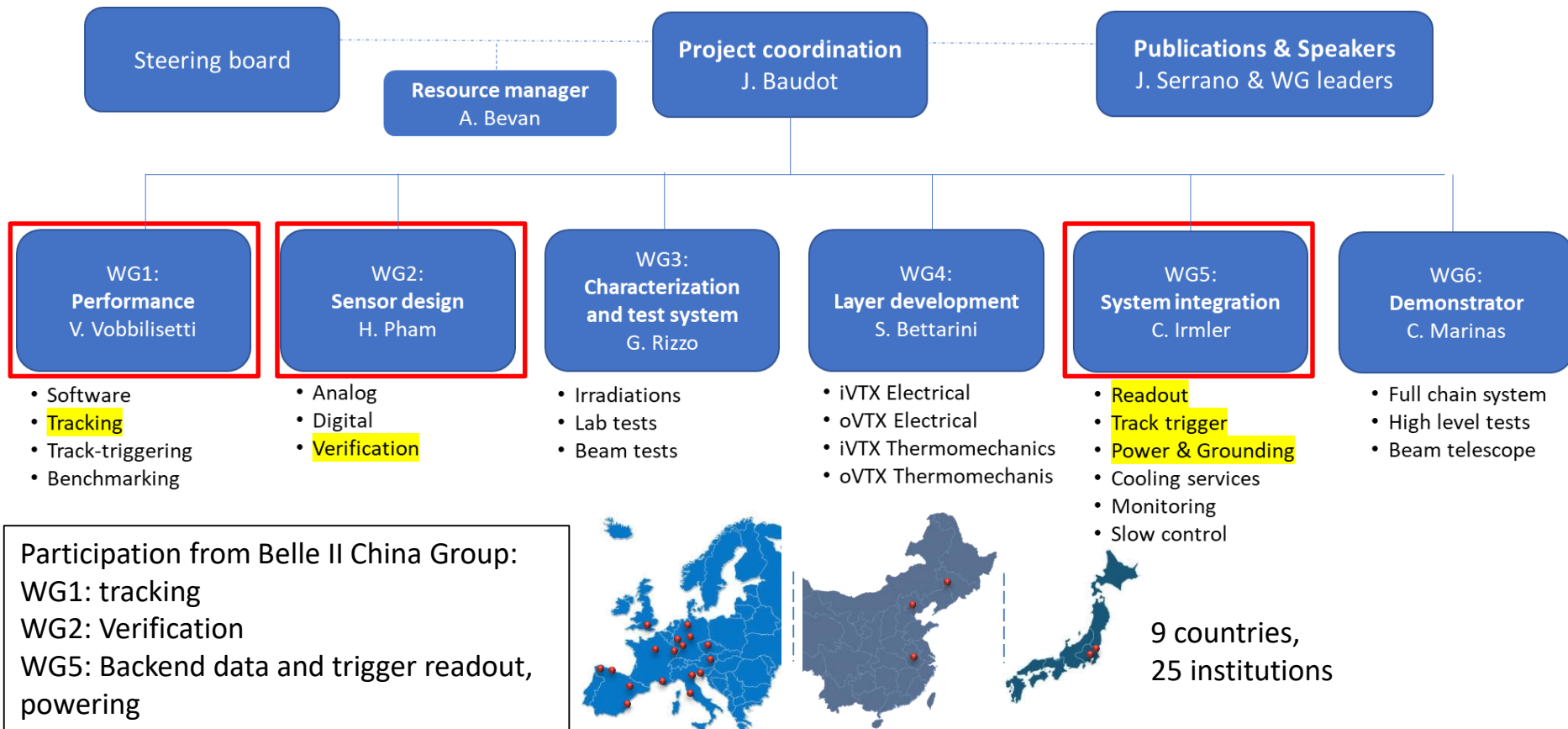
From simulations	Belle II VTX
Spatial res.	$<10\text{-}15\ \mu\text{m}$
Total material budget Inner-outer layers	$0.1 - 0.8\ \%\text{X}_0$
Max hit rate	$120\text{MHz}/\text{cm}^2$
Time precision	$<100\text{ns}$
Trigger (freq.) (delay)	30 kHz 5-10 μs
Rad. hard. (TID) (fluence)	$<100\ \text{kGy}/\text{year}$ $<50 \times 10^{12} n_{\text{eq}}\text{cm}^{-2}/\text{year}$
Power	$<200\text{mW}/\text{cm}^2$



Key sensor specifications:

- Pixel pitch: $30\text{-}40\ \mu\text{m}$
- Integration time: $\lesssim 100\ \text{ns}$
- Power dissipation: $\lesssim 200\ \text{mW}/\text{cm}^2$

Belle II VTX Organization

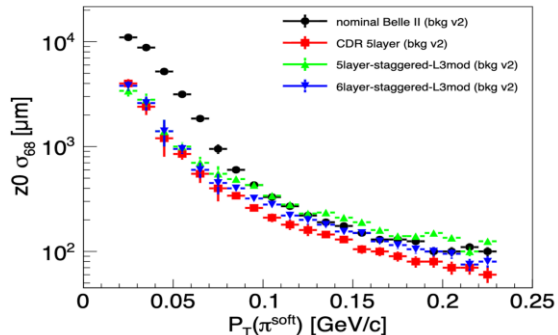
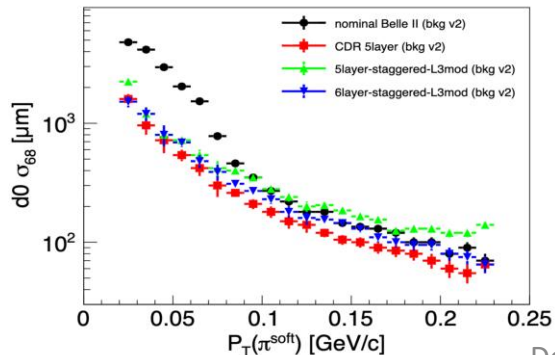
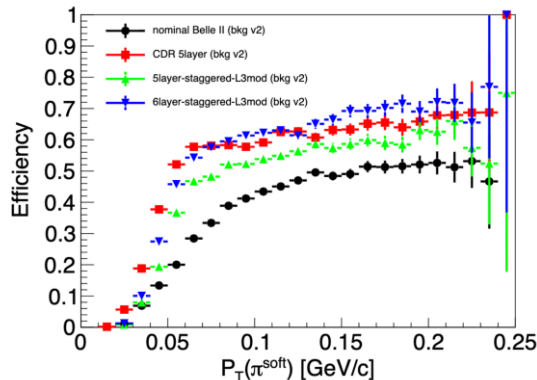
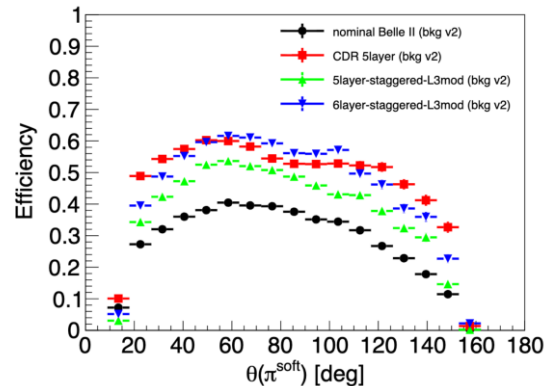


Slow pion performance study

Jilin University: Weiming Song

Study is based on the Monte Carlo samples of following two decay processes

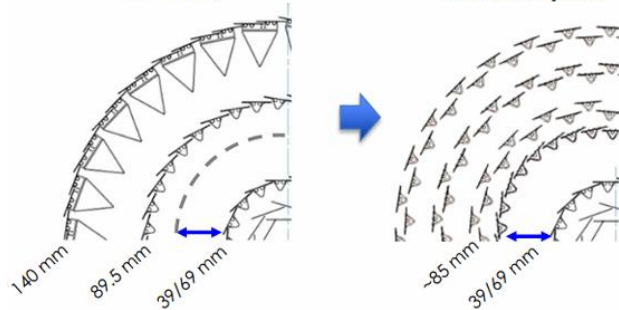
- $B^0 \rightarrow D^{*-} \mu \nu$ with $D^{*-} \rightarrow \bar{D}^0 \pi_{soft}^-$ and $\bar{D}^0 \rightarrow K^+ \pi^-$
- $B^0 \rightarrow D^{*-} \pi^+$ with $D^{*-} \rightarrow \bar{D}^0 \pi_{soft}^-$ and $\bar{D}^0 \rightarrow K^+ \pi^-$



Development of the upgraded Belle II vertex detector

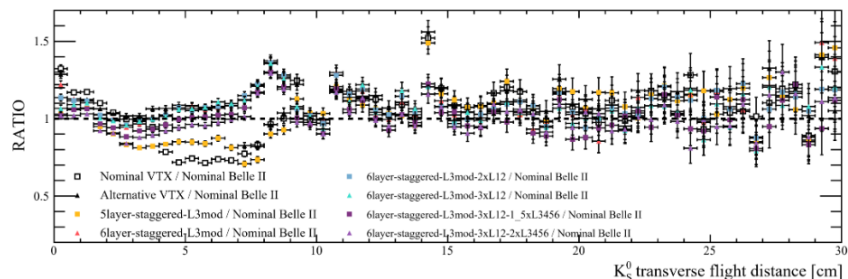
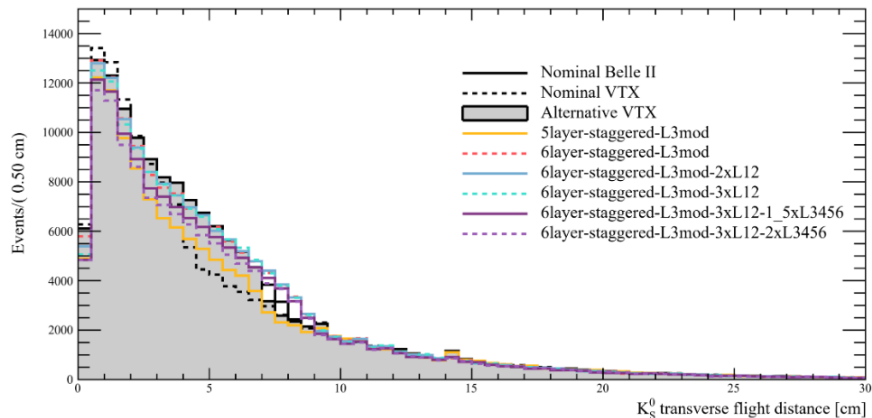
CDR 5 layers

New 6 layers



- Significant improvement in VTX compared by nominal Belle II
- Performance of 6 layer VTX is great than 5 layer in same conditions (but also constrained by the installation space)
- Details can be found at [this link](#)
- Useful in finalizing the VTX geometry, and checking the impact of different material budgets

With the Monte Carlo sample of $B^0 \rightarrow J/\psi K_S^0$ ($J/\psi \rightarrow e^+e^- \text{ or } \mu^+\mu^-$, $K_S^0 \rightarrow \pi^+\pi^-$)



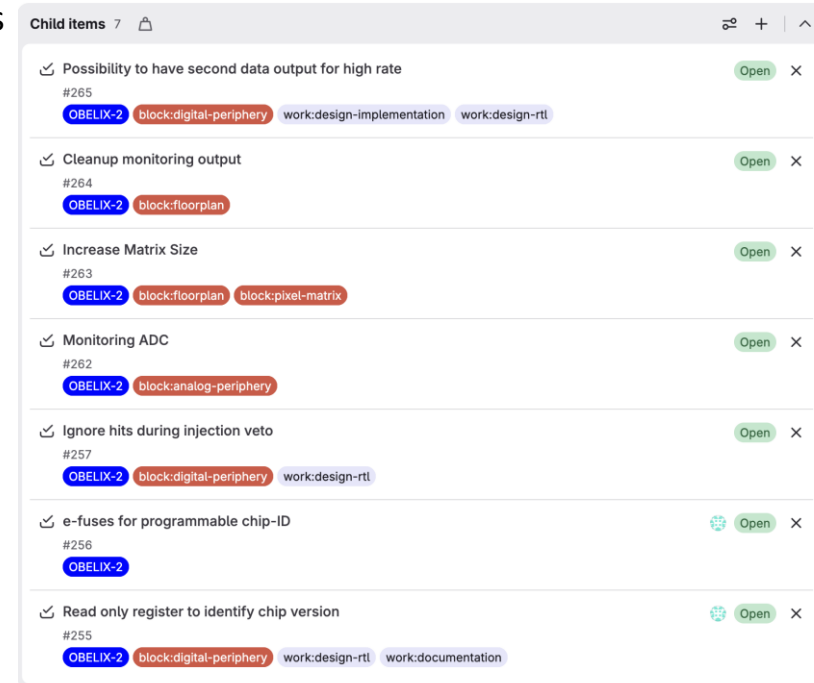
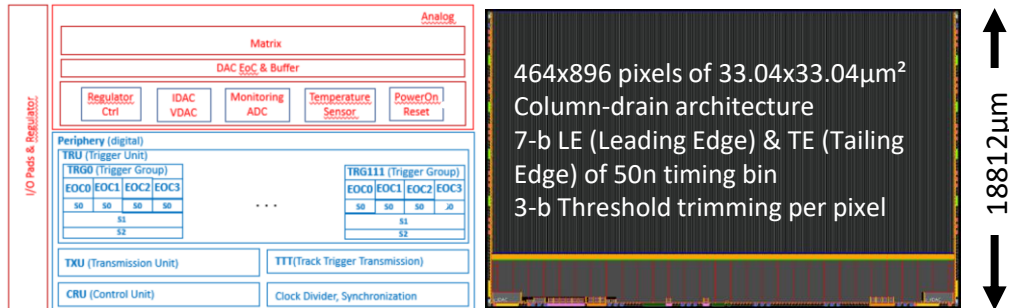
B_{sig} z vertex resolution (μm)	Bkg(v1)	Bkg(v2)	Bkg(v3)
Belle II	20.9	22.3	24.5
Nominal VTX	13.9	14.0	13.9
Alternative VTX	13.7	13.7	13.6
5layer-staggered-L3mod	16.7	16.9	17.1
6layer-staggered-L3mod	16.1	16.1	16.4
6layer-staggered-L3mod-2xL12		17.8	
6layer-staggered-L3mod-3xL12		19.0	
6layer-staggered-L3mod-3xL12-1_5xL3456		19.0	
6layer-staggered-L3mod-3xL12-2xL3456		19.1	

- Vertex resolution and K_S^0 efficiency are compared between different VTX configuration and Nominal Belle II performance.
- Material budget chosen: 0.3% X0 for L1 and L2; 0.8% X₀ for L3-6 to be realistic.
- Details are provided at this [link](#)

OBELIX (Optimized for BELle II pIXell)

- ❑ Developed from **TJ-Monopix2 sensor** (*Developed for ATLAS-ITK: [doi: 10.1016/j.nima.2020.164460](https://doi.org/10.1016/j.nima.2020.164460)*)
- ❑ Increase **active area** from 17x17 mm² to 15x29,6 mm²
- ❑ OBELIX-1 has been submitted now with wafers expected back around October 2026
 - ❑ the lack of person power to verify all the functionalities
- ❑ OBELIX-2 design is starting
 - ❑ a strong need for more verification
 - ❑ And more anticipated verification with new features

Design collaboration: IPHC, CPPM, MBI Vienna, KEK, INFN, University of Bergamo, University of Pavia, University of Pisa, University of Applied Sciences and Arts Dortmund, University of Bonn, University of Valencia



Development of the upgraded Belle II vertex detector

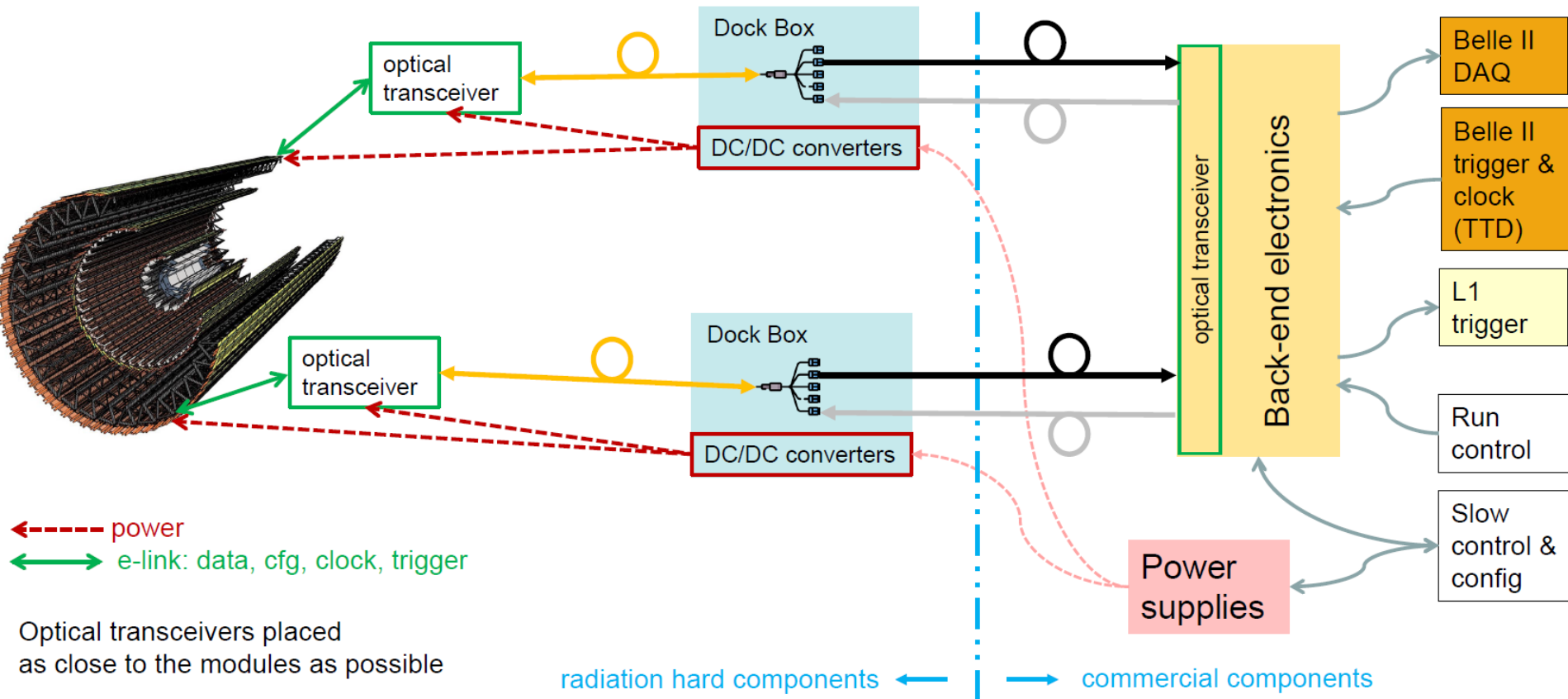
OBELIX-2 contribution from IHEP

- Possible activities: RTL, verification
- Solution for NDA and PDK (access to the process) confirmed
- **Design share agreement** under discussion
- A PHD student will work on the design and verification
 - EDA Tool chain ready for use
 - Hands on experience in digital design flow

- 【1】 Specification & Module Partitioning
- 【2】 RTL Coding $\leftrightarrow$ **UVM Verification (Environment/Testcase/Simulation/Coverage)**
- 【3】 Logic Synthesis $\rightarrow$ **Gate-level UVM Simulation** $\rightarrow$ Formal Verification $\rightarrow$ STA $\rightarrow$ DFT
- 【4】 Floorplan $\rightarrow$ Placement $\rightarrow$ CTS $\rightarrow$ Routing $\rightarrow$ Parasitic Extraction (PEX)
- 【5】 **UVM Post-Simulation (With RC Parasitics)**
- 【6】 Backend Analysis + Physical Verification (DRC/LVS/ERC)
- 【7】 ECO Revision $\rightarrow$ UVM Regression Test
- 【8】 Tape-Out (GDSII Export)
- 【9】 Wafer Fabrication & Packaging
- 【10】 ATE Test $\rightarrow$ Mass Production & Delivery

UVM in Digital Design flow

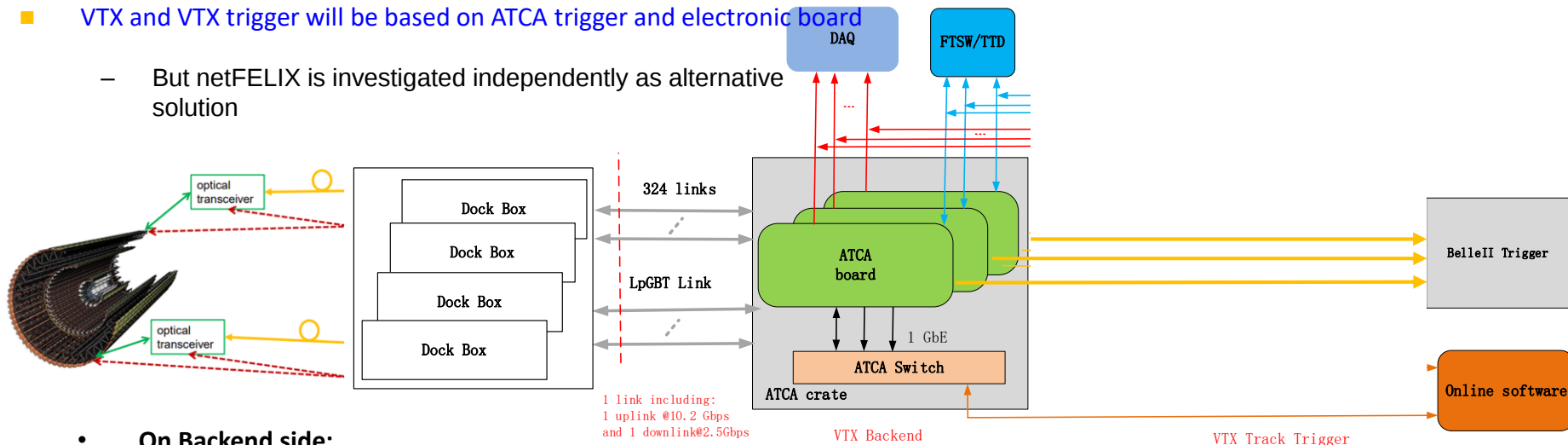
VTX Readout Concept



VTX Backend IHEP Proposal

VTX and VTX trigger will be based on ATCA trigger and electronic board

- But netFELIX is investigated independently as alternative solution

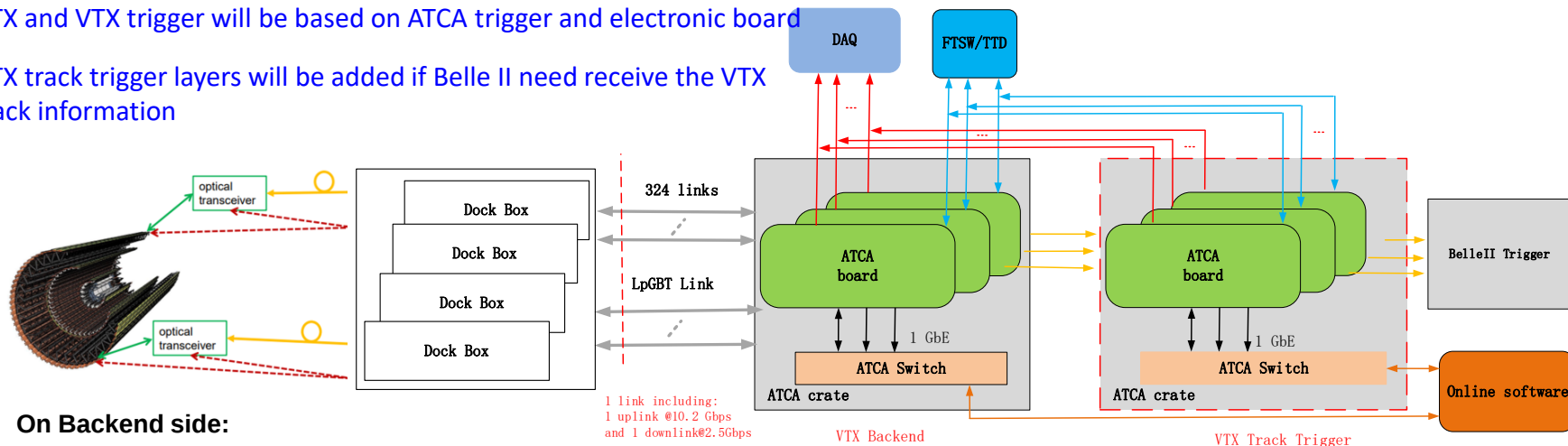


On Backend side:

- Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
- Separate the **hit data and trigger data**;
- Generate the cluster **Trigger Primitive(TP)**
- Send TP data to VTX tracker in pipeline way
- Package the hit data and TP data based on L1
- Send data package to DAQ via TPC/RDMA
- ATCA Switch board as a 1GbE Ethernet switch for Online connection with ATCA board for Slow control

VTX Backend IHEP Proposal (con't)

- VTX and VTX trigger will be based on ATCA trigger and electronic board
- VTX track trigger layers will be added if Belle II need receive the VTX track information



On Backend side:

- Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
- Separate the **hit data and trigger data**;
- Generate the cluster **Trigger Primitive(TP)**
- Send TP data to VTX tracker in pipeline way
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- ATCA Switch board as a 1GbE Ethernet switch for Online connection with ATCA board for Slow control

VTX Backend

On Track trigger side(If needed):

VTX Track Trigger

- Receive and decode TTC signals from FTSW and feedback BUSY and Error signal to FTSW
- Receive Cluster TP data and do **track finding in section**;
- Send track data to Belle II trigger based on BelleII trigger transmission Protocol
- Package the TP data and Track data based on L1
- Send data package to DAQ via TPC/RDMA
- ATCA Switch board as a 1GbE Ethernet switch for Online connection with ATCA board for Slow control

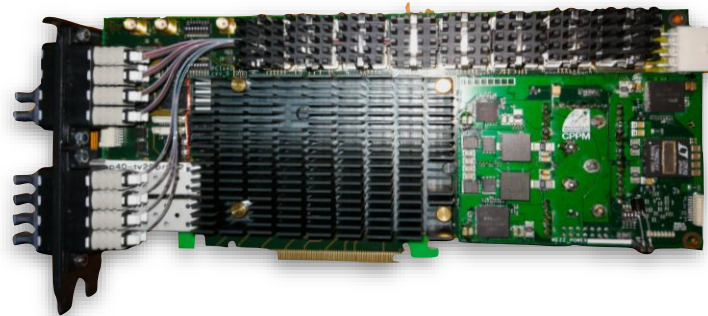
Firmware development for backend

IHEP: Jingzhou Zhao

Shandong University: Qidong Zhou

Jilin University: Weiming Song

- The link protocol of IpGPT from frontend to backend
- User logic on backend
- **Clustering algorithm (if needed on the backend)**
- **Trigger algorithm (interest, collaboration with trigger group)**
- A pocket DAQ system with [PCle40 at Shandong Univ.](#)
- It is planned to setup a testbench with frond-end and back-end boards



Power supplies for VTX

USTC: Lailin Xu, Jiajun Qin

◆ DC-DC Specific requirement

- Radiation dose (<56 Mrad), magnetic field (1.5 T)
- Output Current up to 8A

◆ Survey on DC-DC chips

- Commercial DC-DC converters (< 100 krad) cannot meet the TID requirement
- CERN radiation-hardened DC-DC converters
 - ✓ bPOL12V, bPOL2V5 and bPOL48V are widely applied.
 - ✓ bPOL12V has reliability issues in certain situations, particularly after irradiation, thermal cycling, and repeated enable/disable operations.

	Model	Vin	Vout	Output Current/Power	TID	MAG (Gauss)
CERN	FEAST2.1/FEAST2.3	5 ~ 12 V	0.9 ~ 5 V	0~4 A	>200 Mrad(Si)	40000
CERN	bPOL48V_V2	13 ~ 48 V	0.6 ~ 24 V	0~10 A	>50 Mrad(Si)	40000
CERN	bPOL12V_V6	5.5 ~ 12 V	0.63 ~ 5 V	0~4 A	>150 Mrad(Si)	40000
CERN	bPOL2V5_V3.3	2.1 ~ 2.5 V	0.6 ~ 1.5 V	0~3 A	>100 Mrad(Si)	40000
CERN	AMIS2	6 ~ 11 V	1.2/1.8/2.5/3.3/5 V	0~3 A	300 Mrad(Si)	40000
MAGICS	MAG-PSU00001-NP	5~11 V	0.9~5 V	0~4 A / 0~10 W	> 100Mrad(Si)	40000

Back-end power units

Manufacturer	Model	Output voltage	Output current	Output channels	Ripple
CAEN	A2551	0-8 V	12A	8	<5 mVpp
CAEN	A2552	0-16 V	6A	8	<5 mVpp
CAEN	A2553	0-32 V	3A	8	< 8 mVpp
CAEN	A2554	0-64 V	1.5 A	8	< 8 mVpp
CAEN	A3006	4-16 V	6A	6	<20 mV pp on 10 μ F // 0.1 μ F 10 Hz-15 MHz

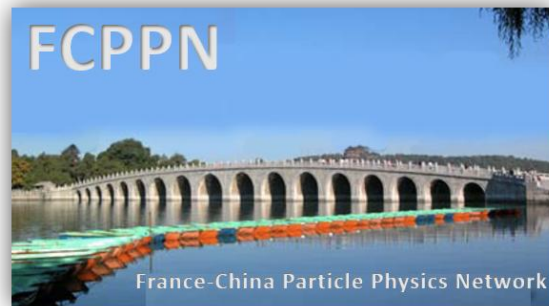
FCPPN/L joint project

- A dedicated channel to strengthen the VTX collaboration
 - Based on the participation of VTX upgrade from French and Chinese side
 - WG1: IPHC and Jilin University
 - WG2: IPHC, CPPM and IHEP
 - WG5: CPPM, IHEP, Shandong University and USTC

French Group			Chinese Group		
Name	Status	Affiliation (institute)	Name	Status	Affiliation (institute)
Leader BAUDOT JEROME	PR	IPHC	Leader LU Yunpeng	PR	IHEP
BARBERO Marlon	PR	CPPM	SONG Weimin	PR	Jilin University
PANGAUD Patrick	Ing.	CPPM	XU Lailin	PR	USTC
BREUGNON Patrick	Ing.	CPPM	ZHOU Qidong	PR	Shandong Univ.
XU Danwei	PhD	CPPM	OUYANG Qun	PR	IHEP
MARGUIN Jérémy	Master	IPHC	GAO Xu	PhD	Jilin university
MAUSHART Mattéo	PhD	IPHC	YU Han	PhD	IHEP
GOFFE Mathieu	Ing.	IPHC			

Summary

- 4 Chinese teams involved in the BELLE II VTX upgrade
 - Jilin University contributed to the physics performance study
 - IHEP is starting to participate the OBELIX-2 sensor design
 - 3 universities Shandong, Jilin, USTC and IHEP participated WG5 and devoted to the backend
 - Joint project and annual workshop in the FCPPN/L framework



Thank you for your time!