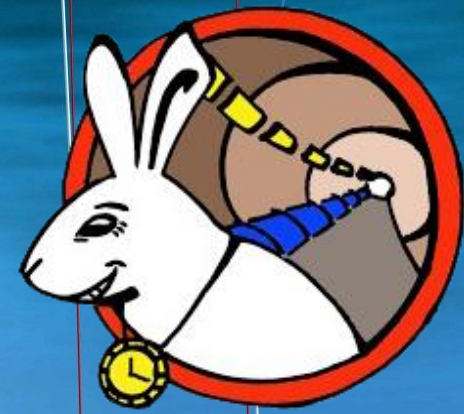


Logiciel

**WHITE RABBIT
PTP CORE
Broadcast**

OMAR GABELLA



SOMMAIRE

WRPC

À quoi ça sert

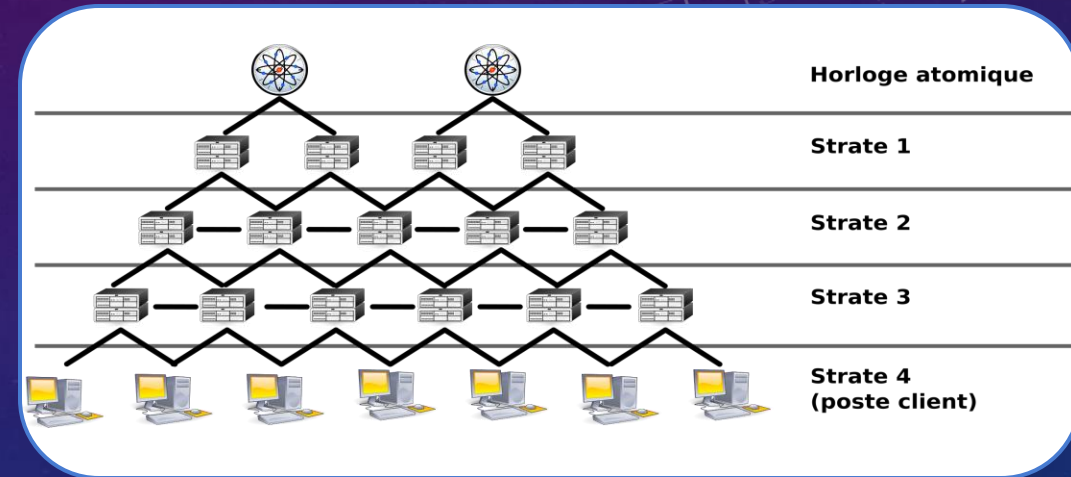
Qu'est-ce que c'est

Qu'est-ce que j'ai fait

INTRODUCTION

La **synchronisation d'horloges** est un mécanisme permettant à deux systèmes distincts d'être synchronisés, c'est-à-dire d'avoir une différence entre leurs temps subjectifs la plus faible possible.

Pour tous les traitements basés sur des mesures de temps et nécessitant une coordination des processus, la synchronisation est alors capitale pour éliminer les erreurs de résultats liées aux dérives des horloges individuelles mises en jeu.



La synchronisation d'horloges consiste à caler toutes les horloges mises en jeu sur une variation uniforme c'est-à-dire :

- qu'elles s'initialisent uniformément (démarrent au même moment avec la même heure absolue ou au pire avec une variation connue c'est-à-dire à une incertitude connue près) ;
- qu'elles présentent une dérive exactement au même instant. La dérive est d'autant plus importante que la précision des horloges est faible.

SCIENTIFIC CASES IN ASTRONOMY AND GEODESY

Clock comparisons

Geodesy

PAPER • OPEN ACCESS

First international comparison of fountain primary frequency standards via a long distance optical fiber link

To cite this article: J Guéna *et al* 2017 *Metrologia* 54 348

ARTICLE

Received 1 Mar 2016 | Accepted 1 Jul 2016 | Published 9 Aug 2016

DOI: 10.1038/ncomms12443 OPEN

A clock network for geodesy and fundamental science

C. Lisdat¹, G. Grosche¹, N. Quintin², C. Shi³, S.M.F. Raupach¹, C. Grebing¹, D. Nicolodi³, F. Stefani^{2,3}, A. Al-Masoudi¹, S. Dörscher¹, S. Häfner¹, J.-L. Robyr³, N. Chiodo², S. Bilicki³, E. Bookjans³, A. Koczwara¹, S. Koke¹, A. Kuhl¹, F. Wiotte², F. Meynadier³, E. Camisard⁴, M. Abgrall³, M. Lours³, T. Legero¹, H. Schnatz¹, U. Sterr¹, H. Denker⁵, C. Chardonnet², Y. Le Coq³, G. Santarelli⁶, A. Amy-Klein², R. Le Targat³, J. Lodewyck³, O. Lopez² & P.-E. Pottie³

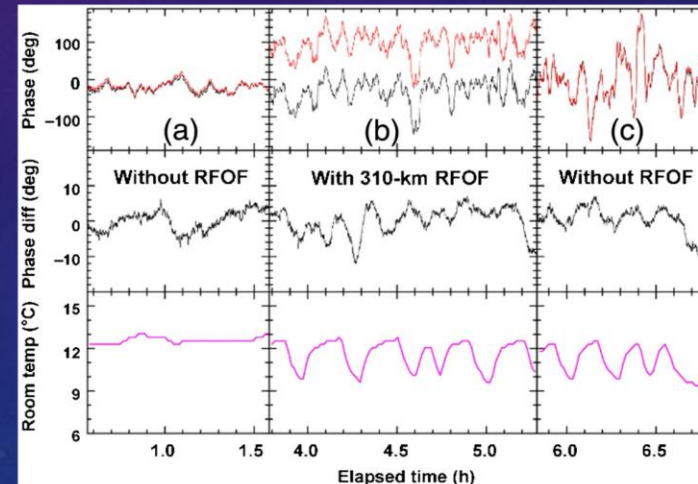
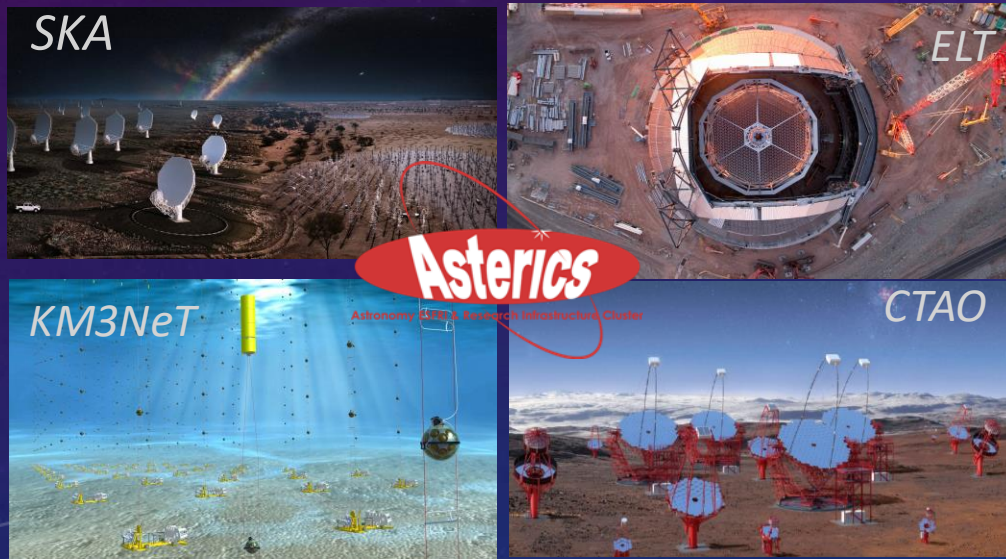
Determination of a high spatial resolution geopotential model using atomic clock comparisons

G. Lion^{1,2}, I. Panet², P. Wolf¹, C. Guerlin^{1,3}, S. Bize¹ and P. Delva¹

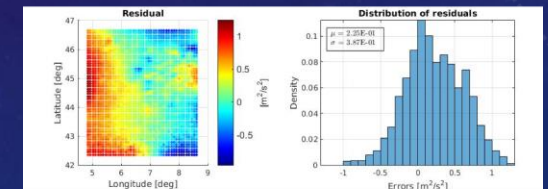
¹LNE-SYRTE, Observatoire de Paris, PSL Research University, CNRS, Sorbonne Universités, UPMC Univ. Paris 06, 61 avenue de l'Observatoire, F-75014 Paris, France

²LASTIG LAREG, IGN, ENSG, Univ Paris Diderot, Sorbonne Paris Cité, 35 rue Hélène Brion, 75013 Paris, France

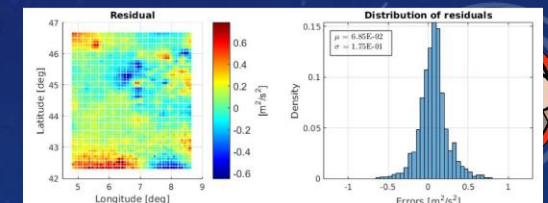
³Laboratoire Kastler Brossel, ENS-PSL Research University, CNRS, UPMC-Sorbonne Universités, Collège de France, 24 rue Lhomond, 75005 Paris, France



Y He et al., *Optica*, 5, 138–146 (2018). see also : C. Clivati et al., *IEEE Trans. on UFFC* 62, 1907–1912 (2015).



(a) Without clock data.

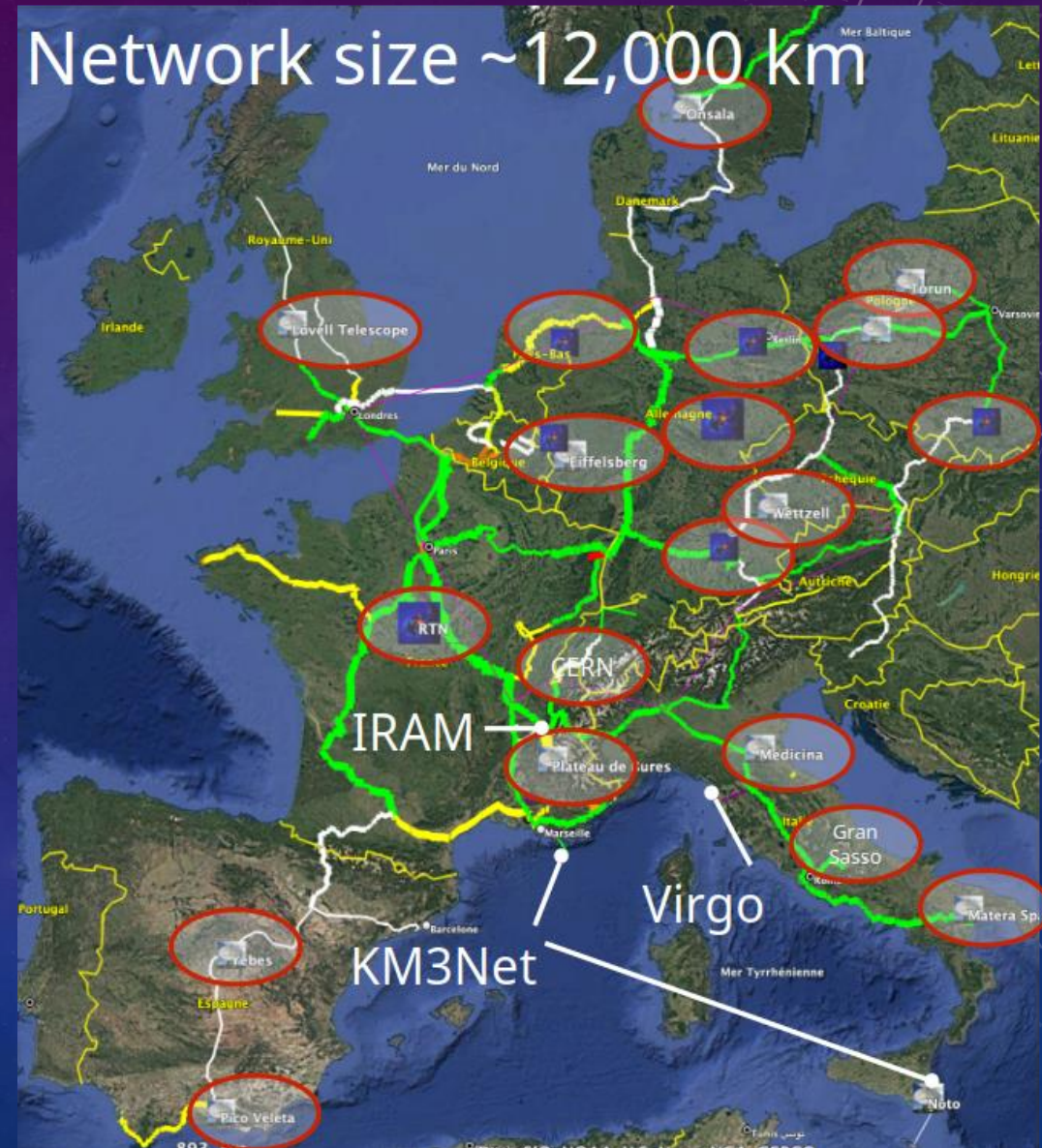


(b) With clock data.

see also : T. E. Mehlstäubler et al., *Atomic clocks for geodesy. Rep. Progress in Physics* 81, 064401 (2018).

EU FIBER NETWORK

- The prospect of the fiber interconnection between major research infrastructures/observatories with time frequency references "in common view"
- VLBI / LOFAR infrastructures
- CERN is connected to REFIMEVE
- **KM3Net**, EGO, Gran Sasso, subterranean laboratories
- Efforts in EU to interconnect the national networks (cf. FOREST candidacy to ESFRI)
- Connection Belgium and The Netherlands to be completed within next 2 years
- **WR deployment all over REFIMEVE happening now !**



Informations récupérées d'une présentation de P.Pottier Systèmes de référence temps-espace (SYRTE) / Observatoire de Paris, lors des J.O. IN2P3 2017

"Bringin Metrological Precision to Scientific Networks: Digital Solutions for Ultra-Scale Time and Frequency Transfer"





White Rabbit PTP Core

Alice: "How time is forever?"

White Rabbit: "Sometimes, just one *nanosecond*."



- **NTP (Network Time Protocol)**

- Historique

- V0 - RFC 958 (1985) <1s
- V1 - RFC 1059 (1988) ~ms
- V2 - RFC 1119 (1989) ~ms
- V3 - RFC 1305 (1992) <ms
- V4 - RFC 5905 (2010) <ms

- Protocole hiérarchique

- Horodatage logiciel

- **PTP (Precise Time Protocol)**

- Historique

- IEEE 1588-2002 (PTPv1) ~μs
- IEEE 1588-2008 (PTPv2) ~μs
- IEEE 1588-2019 (PTPv2.1) <μs

- Horodatage matériel

- + robuste

- BMCA (Best Master Clock Algorithm)

- Précision proche de la nanoseconde en conditions optimales

- Conception pour LAN / matériel dédiée

White Rabbit PTP Core

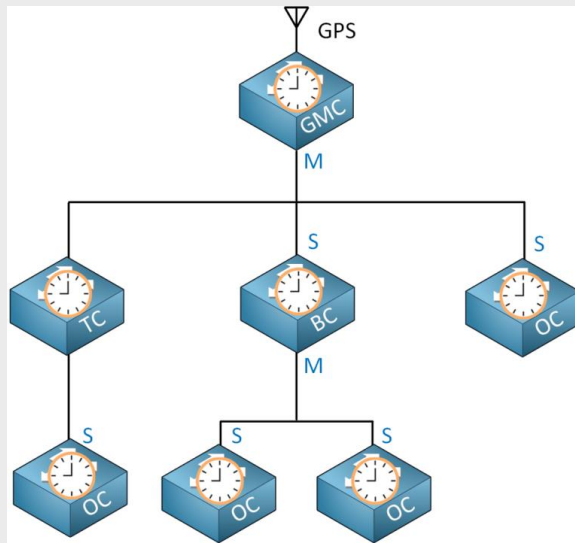


PTP – Precise Time Protocol

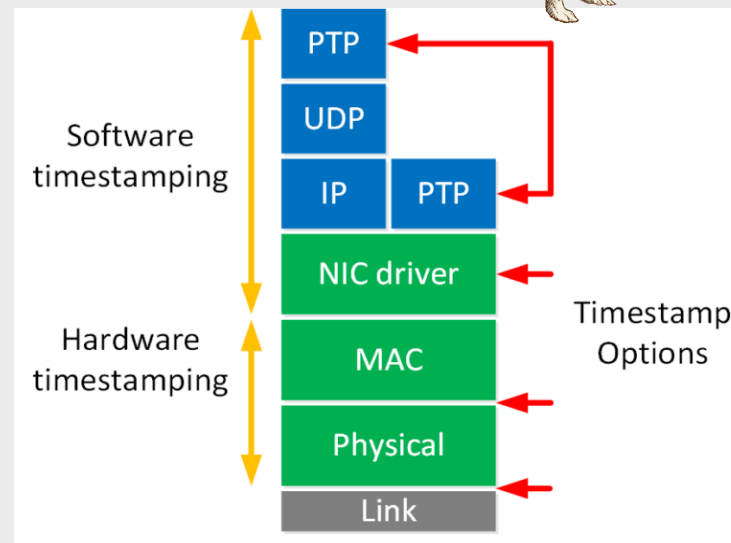


Simple calculations:

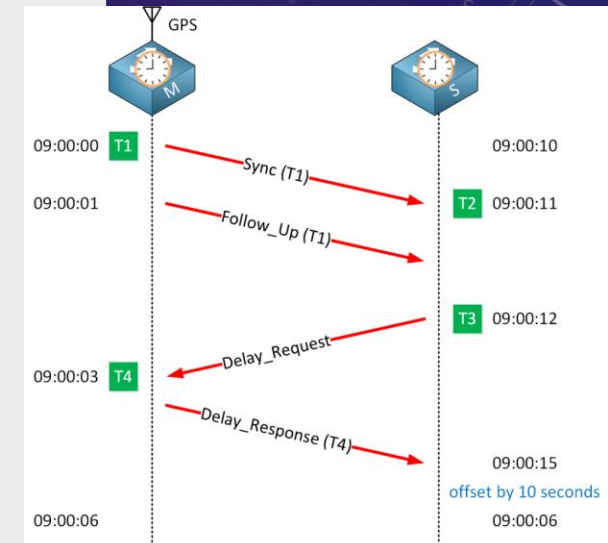
- link delay ms : $\delta ms = (t4 - t1) - (t3 - t2) / 2$
- clock offset compensation: $ms = t2 - t1 + \delta ms$



PTP Network topology



Options where PTP can timestamp. The closer to the physical layer, the more reliable and less delay.



IEEE 1588 synchronization mechanism and delay calculation

From PTP to WRPC

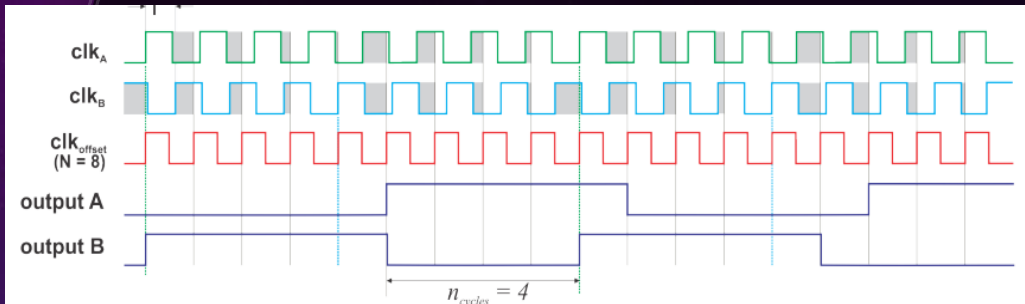


Figure 8: Signals generated by digital DMTD

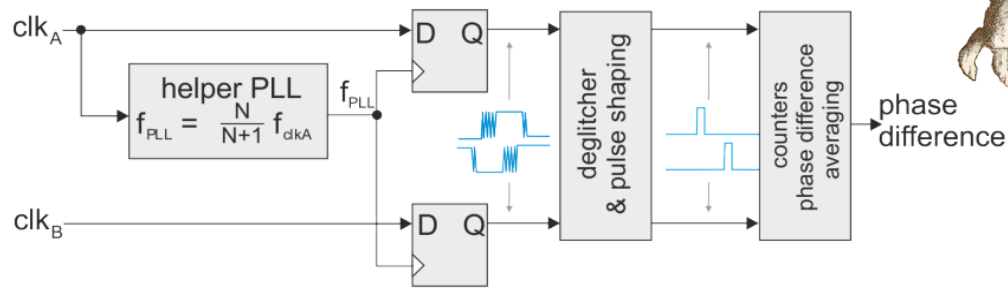
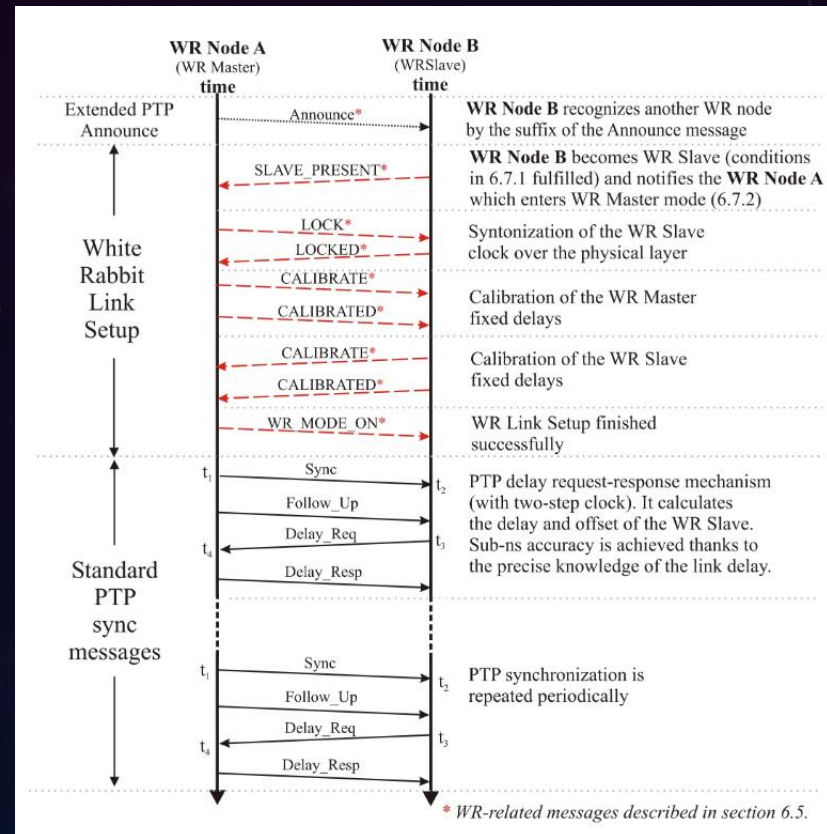
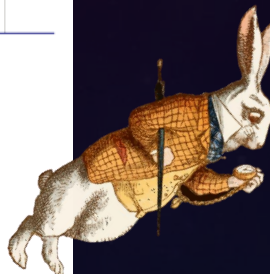


Figure 7: Digital DMTD phase detector

DDMTD – Digital Dual Mixer Time Difference
from G.Daniluk's Thesis



WRLS - White Rabbit Link Setup
from G.Daniluk's Thesis



WHITE RABBIT

- WR Main Elements
 - Precision Time Protocol V2 (IEEE1588-2008)
 - Synchronous Ethernet (SyncE)
 - DDMTD Phase tracking (Digital Dual Mixer Time Difference)



WHITE RABBIT

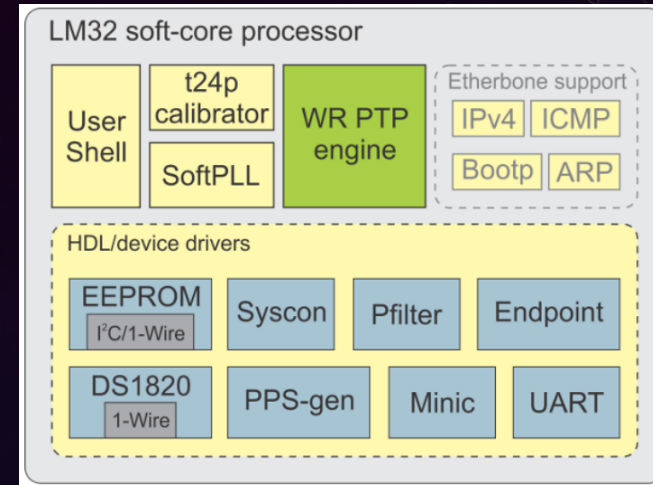
Gateway (VHDL / FPGA)

- PHY Ethernet + timestamping
- DDMTD
- Interfaces PPS, clocks, GPIO
- Support SyncE



Outils intégrés


- Monitor WR
- Diagnostics
- Calibration automatique



Firmware embarqué

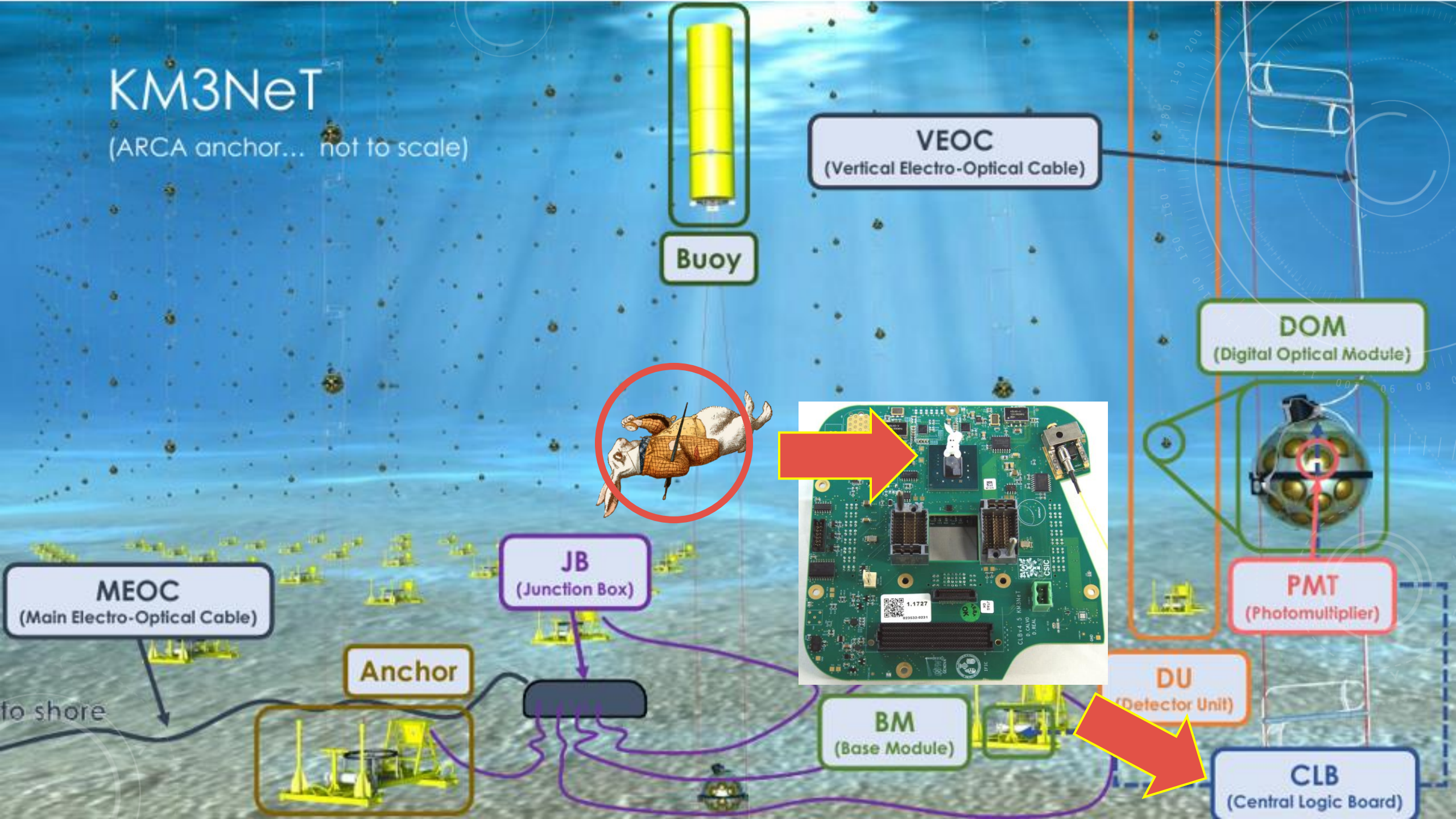
- Soft-CPU (LM32 → aujourd'hui RISC-V)
- Stack PTP White Rabbit
- SoftPLL
- Calibration (t2/t4) - t24p
- Shell de contrôle
- Etherbone, drivers

WHITE RABBIT

- Optical link
 - System synchronization
 - Time propagation compensation
 - Large area and node number (+1000)
- 
- Delivering signals
 - Synchronous clock : 10MHz
 - Pulse Per Second
 - Absolute Time Tagging : 1s
- Jitter stability+ (SyncE + DDMTD + sPLL + ts@PHY + fixed Δ calibrated)

KM3NeT

(ARCA anchor... not to scale)



Buoy

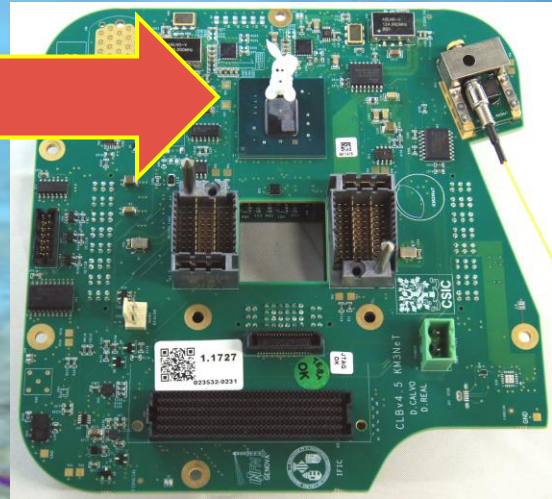
VEOC
(Vertical Electro-Optical Cable)

DOM
(Digital Optical Module)



PMT
(Photomultiplier)

DU
(Detector Unit)



BM
(Base Module)

CLB
(Central Logic Board)

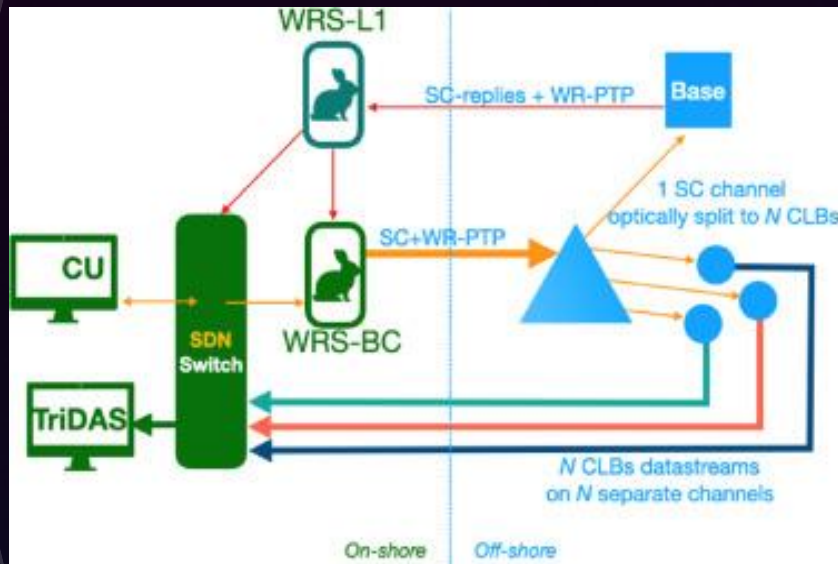
JB
(Junction Box)

MEOC
(Main Electro-Optical Cable)

Anchor

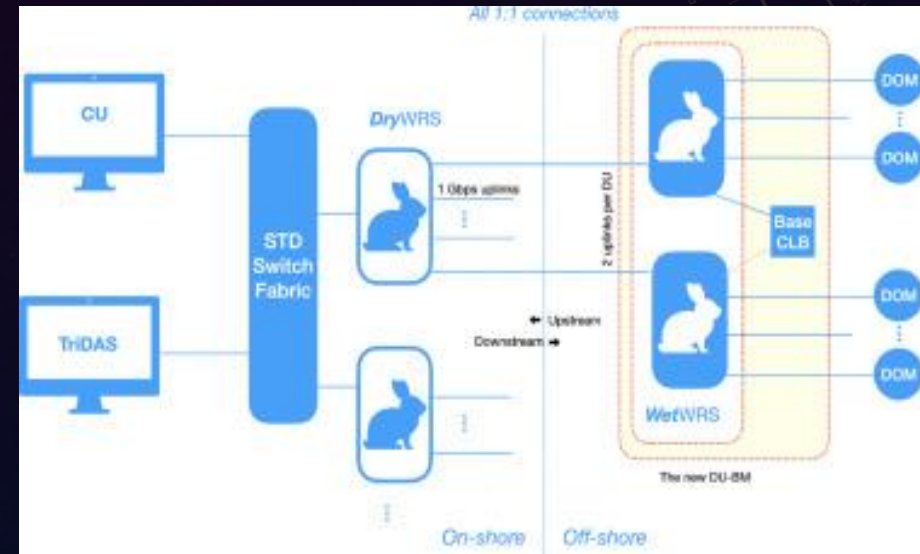
to shore

KM3NET-WR



Broadcast topology

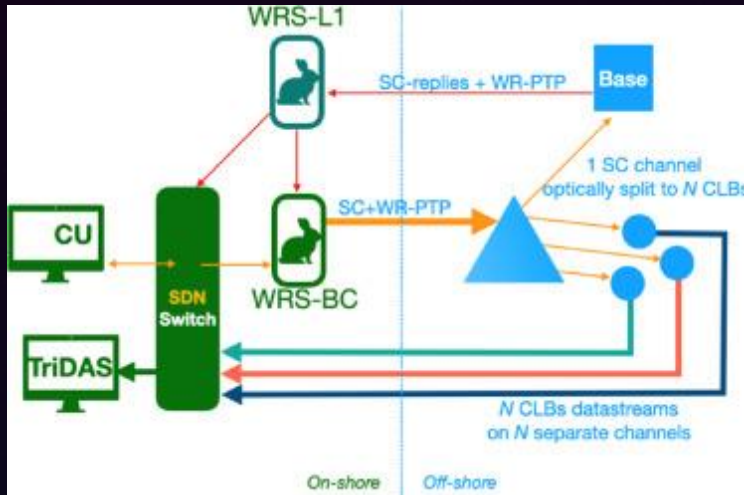
KM3Net "homemade" implementation



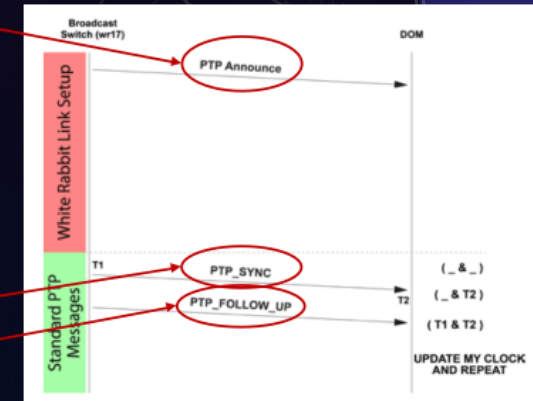
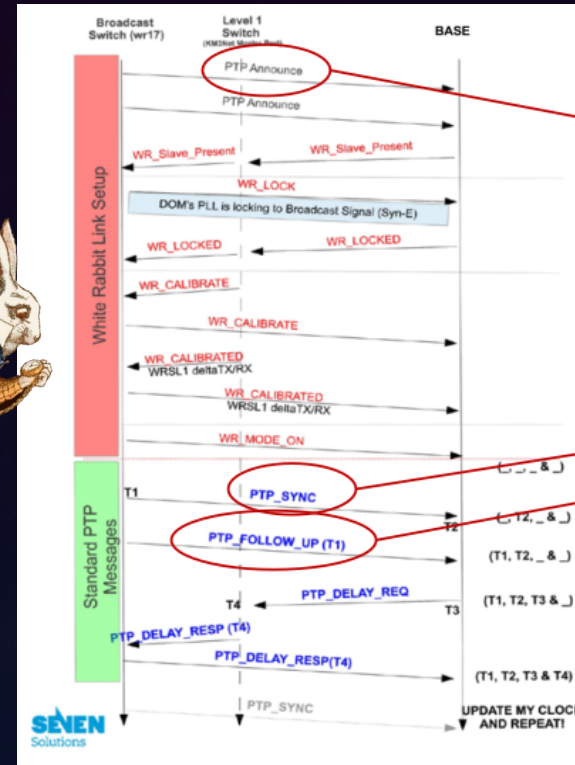
Unicast topology

WR "Standard" implementation

KM3NET-WR BROADCAST



Broadcast topology



KM3NET-WR BROADCAST

- *WRPC basée sur PTP V2 (IEEE1588-2008)*
- *J'ai réalisé le portage du code wrpc-sw de la V2.1 à V4.2*



- **V2.1**
 - *Stack ptp ptp-noposix*
 - *SVN*
- **V4.2**
 - *ppsi*
 - *t24p - Calibration (t2/t4)*
 - *Optimized BMCA*
 - *Git*

- *1^{ere} CSP février 2020*
- *4^{eme} CSP septembre 2022*

- **2,5 ans à 50% ETP**
- *Seul dev. sur wrpc-sw à KM3NeT et rattaché au WP-DAQ*
- *Courbe d'apprentissage raide*
- *2 versions livrées BMs et DOMs*

KM3NET-WR BROADCAST

- *WRPC basée sur PTP V2 (IEEE1588-2008)*
- *J'ai réalisé le portage du code wrpc-sw de la V2.1 à V4.2*
- *Trois dépôts de code.*
 - *ppsi (ptp daemon)*
 - *wrpc-sw*
 - *clb-sw*



```
WR PTP Core Sync Monitor wr-starting-kit-v3.1-36-g69931020ct 29 2021
Esc = exit

TAI Time: Tue, Nov 2, 2021, 09,30,18

Link status:
wrui: Link up (RX 1793, TX 518)
Mode WR Slave Locked Calibrated

Listening_state: 9
wr_link_on_state: 1
Slave_state: 2919
handle_announce: ann_pp_lib: 261
wrModeOn: 1: parentWrModeOn: 0
handle_followup: fu_st_com: 509
WR_SERVO: downlink: 509
timestamp: error++: 0: count>5: 5: no_converge: 0

SERVO_STATES: busy: 0: shw_pps_gen_busy: 0: spll_shifter_busy: 175: Before: 329
Uninitialized: 1: Sync_TAI: 1: Sync_nSec: 2
Sync_Phase: 2: Wait_offset_stable: 1: Track_phase: 323
ts_offset: secs: 0
ts_offset: nsecs: -1

BEFORE_TO_INIT: 509: TO_INIT: 0
Before_TO: 0: ANN_RECEIPT|TO_FAULT: 0

PTP status: slave

Synchronization status:
Servo_state: TRACK_PHASE
Phase_tracking: ON
Aux_clock_0_status:
Aux_clock_1_status: enabled
```

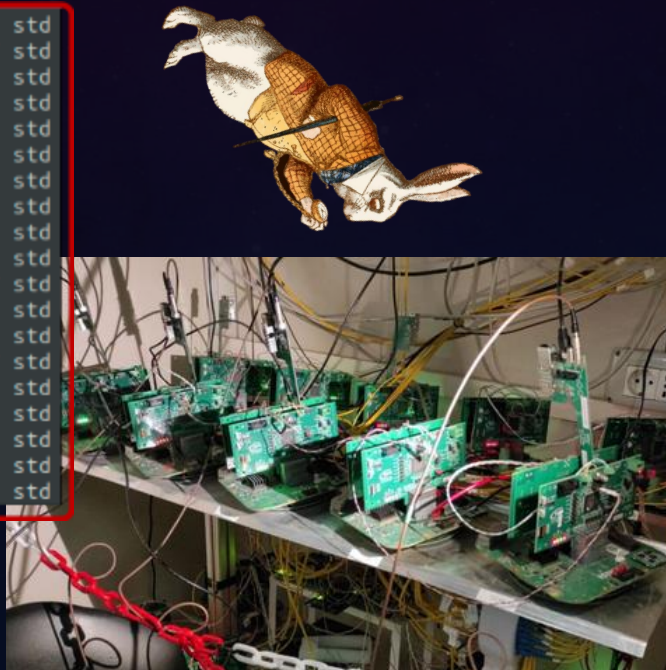
WR Monitoring tuned.

KM3NET-WR BROADCAST

- Firmware testé sur une *Unité de détection* (DU) installé au "*Bologna Common Infrastructure*" de KM3NeT.
- Contrôle des instruments (GBF, Oscillo 6GHz et fréquencesmètre) à distance (VPN, SSH...).

Channel 12:	255 hits,	594.714 ns +/-	1.952 std
Channel 13:	255 hits,	595.706 ns +/-	1.977 std
Channel 14:	255 hits,	595.714 ns +/-	1.952 std
Channel 15:	255 hits,	595.710 ns +/-	1.961 std
Channel 16:	255 hits,	595.714 ns +/-	1.952 std
Channel 17:	255 hits,	596.714 ns +/-	1.952 std
Channel 18:	255 hits,	596.714 ns +/-	1.952 std
Channel 19:	255 hits,	596.714 ns +/-	1.952 std
Channel 20:	255 hits,	596.714 ns +/-	1.952 std
Channel 21:	255 hits,	597.710 ns +/-	1.961 std
Channel 22:	255 hits,	597.706 ns +/-	1.977 std
Channel 23:	255 hits,	597.714 ns +/-	1.952 std
Channel 24:	255 hits,	597.714 ns +/-	1.952 std
Channel 25:	255 hits,	596.706 ns +/-	1.977 std
Channel 26:	255 hits,	596.710 ns +/-	1.961 std
Channel 27:	255 hits,	595.714 ns +/-	1.952 std
Channel 28:	255 hits,	596.710 ns +/-	1.961 std
Channel 29:	255 hits,	597.718 ns +/-	1.922 std
Channel 30:	255 hits,	597.710 ns +/-	1.961 std

BEFORE



Banc de tests à l'INFN de Bologne

Channel 12:	317 hits,	694.000 ns +/-	0.000 std
Channel 13:	317 hits,	694.000 ns +/-	0.000 std
Channel 14:	317 hits,	694.000 ns +/-	0.000 std
Channel 15:	317 hits,	694.000 ns +/-	0.000 std
Channel 16:	317 hits,	694.000 ns +/-	0.000 std
Channel 17:	317 hits,	695.000 ns +/-	0.000 std
Channel 18:	317 hits,	694.710 ns +/-	0.454 std
Channel 19:	317 hits,	695.000 ns +/-	0.000 std
Channel 20:	317 hits,	697.000 ns +/-	0.000 std
Channel 21:	317 hits,	696.000 ns +/-	0.000 std
Channel 22:	317 hits,	696.656 ns +/-	0.475 std
Channel 23:	317 hits,	697.940 ns +/-	0.237 std
Channel 24:	317 hits,	697.000 ns +/-	0.000 std
Channel 25:	317 hits,	695.000 ns +/-	0.000 std
Channel 26:	317 hits,	695.000 ns +/-	0.000 std
Channel 27:	317 hits,	695.000 ns +/-	0.000 std
Channel 28:	317 hits,	695.000 ns +/-	0.000 std
Channel 29:	317 hits,	696.000 ns +/-	0.000 std
Channel 30:	317 hits,	695.000 ns +/-	0.000 std

AFTER

KM3NET-WR BROADCAST

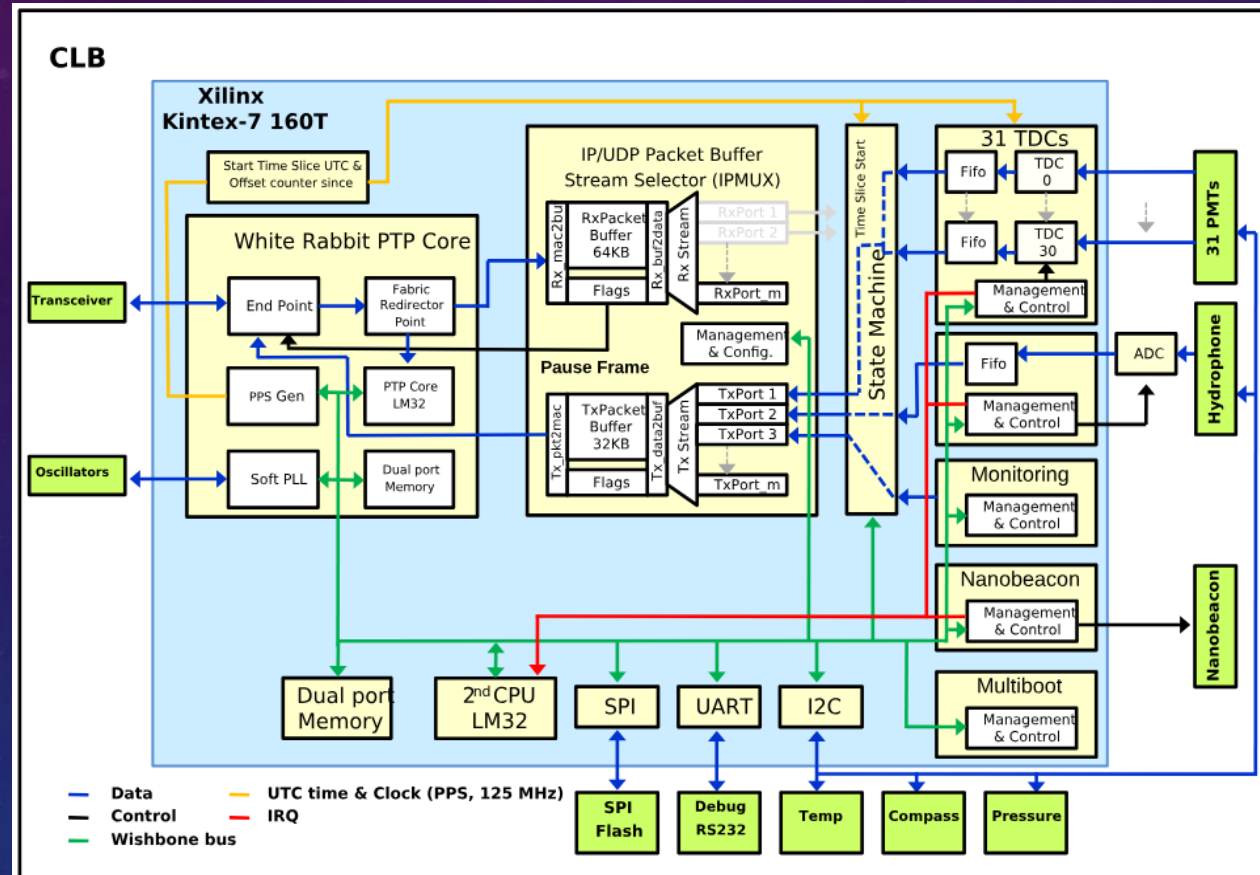


Fig. 3. Block diagram of the CLB. Optics, acoustics, instrumentation, front-end firmware and all the interfaces are shown.

[Embedded software of the KM3NeT central logic board](#)



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KM3NeT

