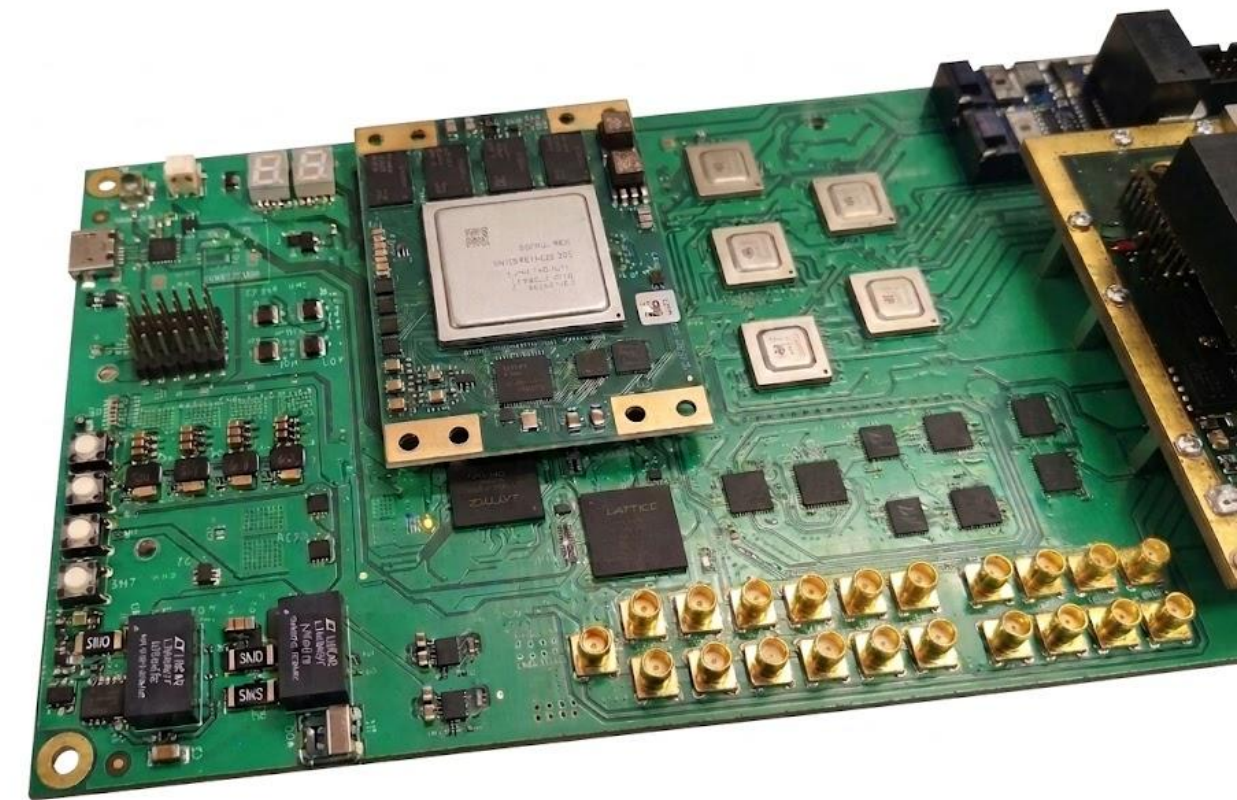


AGATA Phase 2 Electronics PACE-CAP Firmware



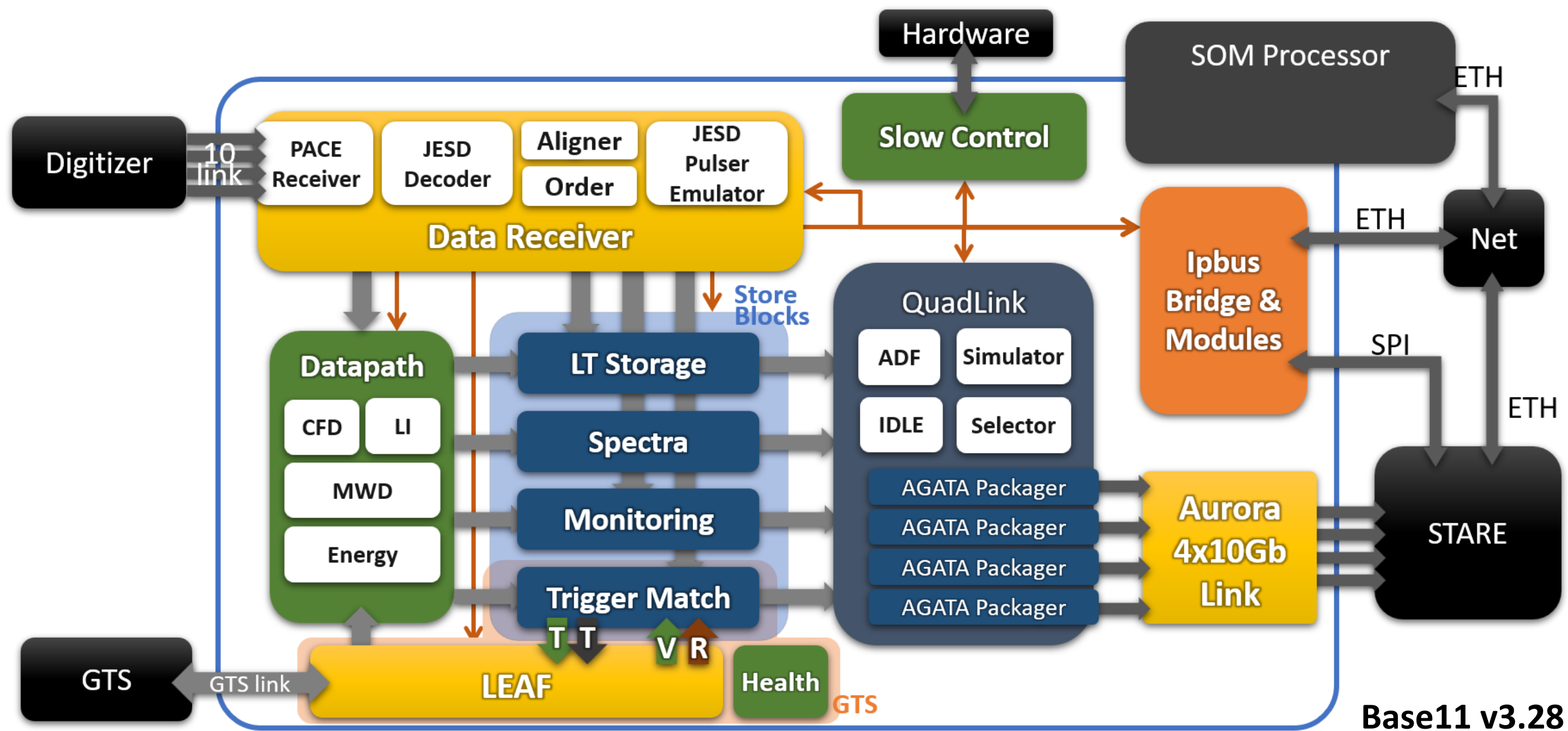
Firmware

Documentation

Updates

Status

- Firmware
- Documentation
- Updates
- Status



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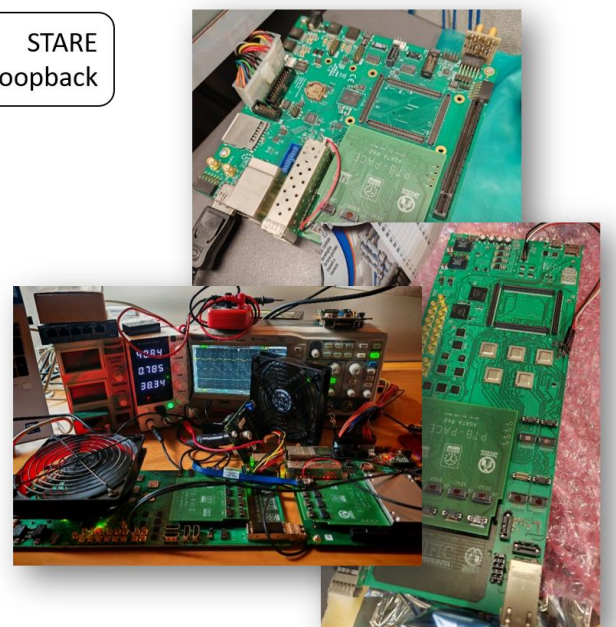
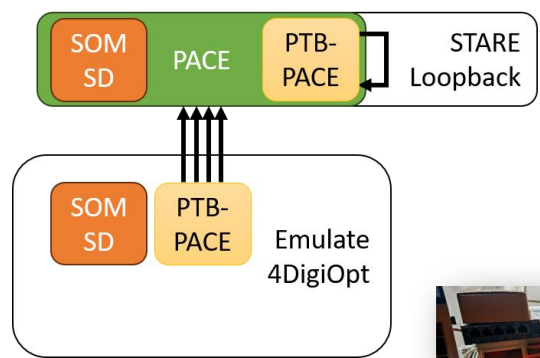
Status

PACE Production Test

New PLL Control System

Last Xilinx Platform. Base 11

```
0x440: 23.00 - Sensor OK 1/25
0x440: 26.00 - Sensor OK 2/25
0x440: 22.00 - Sensor OK 3/25
0x440: 24.00 - Sensor OK 4/25
0x440: 26.00 - Sensor OK 5/25
0x440: 22.00 - Sensor OK 6/25
1V0H: 0.99 V - 1.46 A - 1.45 W [1.20-0.90] - [OK]
1V0H: 0.99 V - 1.44 A - 1.42 W [1.20-0.90] - [OK]
1V0H: 1.00 V - 0.32 A - 0.32 W [1.20-0.90] - [OK]
1V0H: 1.00 V - 0.34 A - 0.34 W [1.20-0.90] - [OK]
PSU SV: 4.60 V - 4.61 A - 21.18 W [5.30-4.50] - [OK]
PSU SV: 3.18 V - 0.32 A - 1.00 W [3.50-3.10] - [OK]
1V0H: 1.03 V - 0.25 A - 1.00 W [2.00-1.05] - [OK]
2V0H: 2.51 V - 1.07 A - 4.19 W [2.00-2.40] - [OK]
3V0H: 3.09 V - 1.15 A - 3.50 W [3.50-3.00] - [OK]
SOM SV: 3.20 V - 2.42 A - 7.92 W [3.50-3.10] - [OK]
PM: 1V0H: 1.00 V - 0.20 A - 0.30 W [2.00-1.05] - [OK]
PM: 3V0H: 3.14 V - 0.41 A - 0.61 W [3.50-3.10] - STARE not connected [OK]
Total power: W
- Voltage ADC OK 1/25
- Current ADC OK 0/25
S100-A
SOM PLL found [9/25] OK
Programming SOM PLL to program 4 / 80MHz SOM PLL Programmed
MCS mux IN found [11/25] OK
MCS mux IN programmed
MCS mux ADC found [12/25] OK
MCS mux ADC programmed
MCS mux GTS found [13/25] OK
MCS mux GTS programmed
MCS PLL found [14/25] OK
MCS PLL programmed
DCS mux IN found [15/25] OK
DCS mux IN programmed
DCS mux OUT found [16/25] OK
DCS mux OUT programmed
DCS PLL found [14/25] OK
```

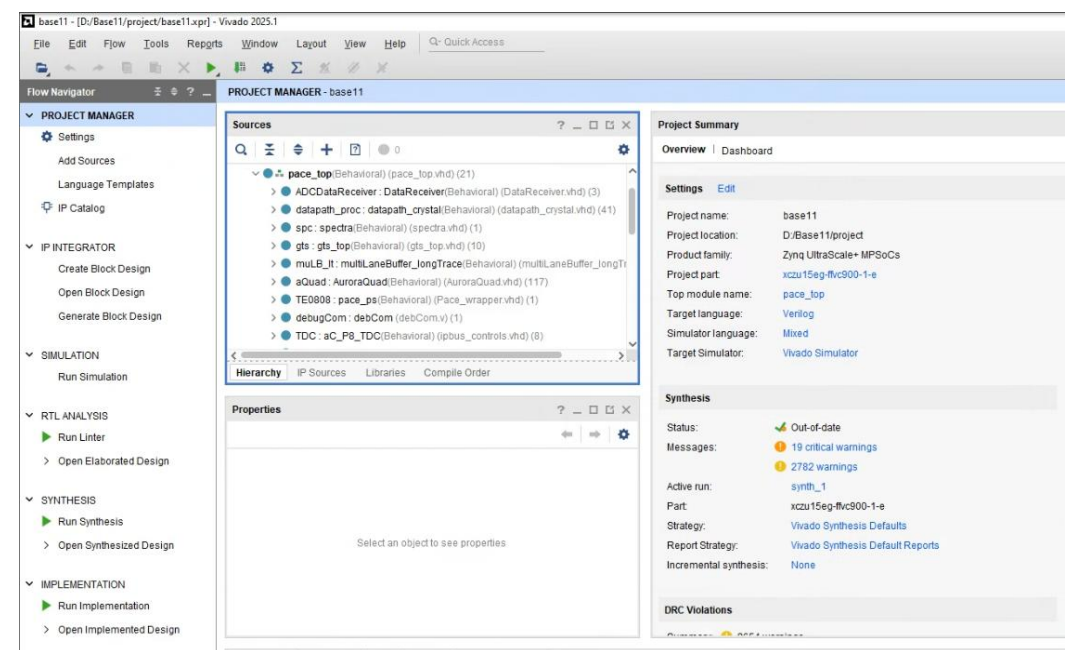


```
startClock
PACE OLD SOM version detected TE0808 v4 or lower
Programming TE0808 clock Rev B file: Si5345_GTS0 ***** [ok]
Main Clk Mux: In1001 ADC:0000 GTS:0000
Derived Clk Mux: In0030 - Out3000
---- Configure Clk measure ----
```

```
PACE v5 SOM version detected TE0808
Programming TE0808 clock Rev D file: Si5345_GTS0 ***** [ok]
Main Clk Mux: In1001 ADC:0000 GTS:0000
Derived Clk Mux: In0030 - Out3000
---- Configure Clk measure ----
```

Version B

V5 – SOM PLL version D



PACE Readout Firmware – Base10/11

Project Overview

The **PACE-CAP-SOM firmware** constitutes the digital backbone of the AGATA Phase 2 electronics. It manages the complete signal chain from the high-speed digitizers to the Ethernet readout, handling data reconstruction, feature extraction, synchronization, and system control in real time. The design follows the AGATA specifications for 100 MHz sampling, 14-bit resolution and global trigger synchronization via the GTS (Global Trigger and Synchronization) network.

Implemented on a **Zynq UltraScale+ XCZU15EG-1FFVC900E** (System-on-Module Trezz TE0808-05-BBE81-E), the firmware exploits both the programmable logic for high-speed DSP and the embedded ARM processors for slow control, diagnostics and monitoring. The PACE motherboard routes 10 aggregated JESD204B/C links from the *Digi-Opt12* ADCs, performs the 4-to-1 time-domain multiplexing using TLK aggregators, and reconstructs 38 parallel channels at 100 MHz.

Architecture and Functionality

Each PACE-CAP unit integrates the main firmware subsystems:

- **ADC Receiver / UpDownLink block:** performs JESD204B/C deserialization, re-ordering, and data reconstruction from the TLK aggregated lanes. It outputs 40 synchronized channels (16 bit @ 100 MHz) transferred to the datapath through elastic FIFOs for clock-domain crossing between 200 MHz and 50 MHz domains.
- **Datapath processing:** each channel carries a 14-bit flow combining baseline noise and HPGe pulses. Real-time digital processing includes a *dCFD* (digital Constant Fraction Discriminator) and a *Moving Window Deconvolution* (MWD) trapezoidal filter, selectable between Numexo2-based (v1) and IPHC/AGATA-based (v2) implementations. The firmware extracts trigger, energy, and timestamp (via linear interpolator in 3–10 cycles) to generate standardized **agt_evt** events.
- **Data Storage Blocks (DSB):** asynchronous dual-clock memories bridging 100 MHz (write) and 156.25 MHz (read) domains. They store event data, long traces, spectra, and monitoring flows. Each DSB outputs 64-bit frames to the QuadLink packager.
- **QuadLink Packager & STARE Readout:** the packager assembles AdF (AGATA Data Frame) formatted events and transfers them via four Aurora 10 Gb/s links to the Ethernet STARE mezzanine. STARE repackages the streams into UDP frames at up to 40 Gb/s aggregate throughput, with optional RUDP (reliable UDP) support.
- **Global Trigger System (GTS):** implements the GTS leaf, trigger matching and alignment protocols. It synchronizes local events with the global 100 MHz reference and exchanges validation messages with the trigger processor. The system is compatible with the upcoming SMART trigger protocol based on uTCA

Top-Level Modules

This grid shows all main modules of the PACE-CAP-SOM firmware. Each block is clickable and opens its own documentation page containing submodules, hierarchy, and implementation details.

Data Receiver

Receives 10 TLK digitizer links (8 Gbps each), deserializes JESD204B/C lanes, and outputs 40 parallel ADC streams. Integrates the UpDownLink JESD wrapper and pattern alignment logic.

Datapath Crystal

Implements pulse processing (MWD, CFD) and event building per ADC channel, providing processed data and triggers to GTS.

GTS

Controls global timing and trigger synchronization through the GTS optical uplink/downlink. Handles timestamping and calibration alignment.

QuadLink

Implements the CAP-STARE Aurora 4-lane optical link for DAQ readout. Manages aggregated long traces, trigger matches, and monitoring streams.

IPBus

Provides configuration and register-level communication across subsystems. Handles SPI, slow-control, and internal calibration fabric.

PatternGen

Generates JESD204 and ADC synchronization patterns for system calibration. Provides programmable sequence generation.

PACE PS

Embedded ARM-based Processing System running Linux. Manages high-level configuration, data transfer, and network interfaces.

Monitoring

Collects real-time link status, temperature, and throughput metrics. Exports structured reports to Aurora and IPBus.

LongTrace Buffer

Buffers extended ADC waveforms upon trigger events. Interfaces to Aurora for long-trace data readout.

Spectra

Builds histograms and spectra for energy distribution monitoring. Controlled via IPBus and synchronized to GTS timestamps.

PACE HW Bridge

Interfaces low-speed peripherals (I2C, GPIO, LEDs). Bridges PS to PL for hardware status and control via IPBus.

Definitions

General definitions and Formats for Agata PACE Bas9-11 firmware.

Firmware

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PACE Readout Firmware – Base10/11

Project Overview

The **PACE-CAP-SOM firmware** constitutes the digital backbone of the AGATA Phase 2 electronics. It manages the complete signal chain from the high-speed digitizers to the Ethernet readout, handling data reconstruction, feature extraction, synchronization, and system control in real time. The design follows the AGATA specifications for 100 MHz sampling, 14-bit resolution and global trigger synchronization via the GTS (Global Trigger and Synchronization) network.

Implemented on a **Zynq UltraScale+ XCZU15EG-1FFVC900E** (System-on-Module)

Top-Level Modules

This grid shows all main modules of the PACE-CAP-SOM firmware. Each block is clickable and opens its own documentation page containing submodules, hierarchy, and implementation details.

Data Receiver

Datapath Crvstal

GTS

PatternGen

LongTrace Buffer

Definitions



PACE Firmware – `pace_call` Class Documentation

[← Back to Software Overview](#)

The `pace_call` class provides firmware-level control for **ADC synchronization and calibration** within the *AGATA Phase-2 PACE system*. It directly accesses nodes under `N_SLV_aC_P0_calibration` and associated sub-registers to configure the JESD SYNC_N pattern generator, PLL synchronization of the ADCs, delay calibration, and Elastic Buffer bit-error measurement.

Command Reference

▼ PACE_CALL_pattern_pllSync — Set ADC PLL Synchronization

Enables or disables the ADC PLL synchronization signals for each DigiOpt channel (0–3). The function writes to `N_SLV_aC_P0_calibration.outConf.pllNsync` with a bit-encoded mask.

Arguments [ch0] [ch1] [ch2] [ch3] → 0=OFF, 1=ON

Register `N_SLV_aC_P0_calibration.outConf.pllNsync`

Purpose Controls whether each ADC channel receives a synchronized PLL reference.

```
s-pace > PACE_CALL_pattern_pllSync 1 1 0 0
Config: Ch0 ON Ch1 ON Ch2 OFF Ch3 OFF
```

► PACE_CALL_pattern_sync — Configure JESD SYNC_N Output

▼ PACE_CALL_pattern_gen — Configure ADC Pattern Generator

Switches the calibration output generator into predefined test patterns to validate ADC and JESD alignment.

Registers

- `N_SLV_aC_P0_calibration.outConf.syncSetSel`
- `N_SLV_aC_P0_calibration.outConf.patternSet`
- 0 – Off (Default)
- 1 – System Clock
- 2 – 10 MHz clock with missing edge

Patterns

- 3 – Negative System Clock
- 4 – 10 MHz Clock
- 5 – Negative 10 MHz with missing edge

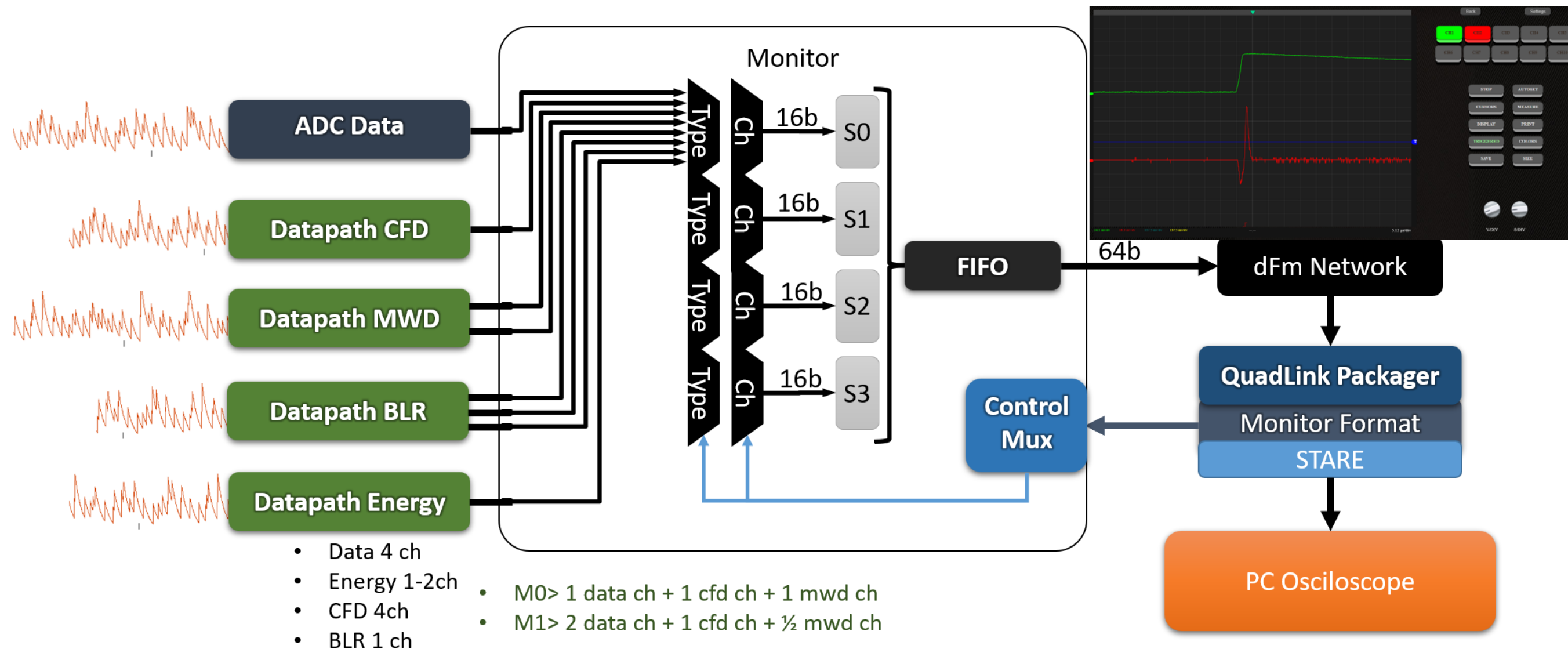
```
s-pace > PACE_CALL_pattern_gen 1
Pattern Generator for ADC: System Clock
```

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- T0 - Trigger Mode 0:** Channel 0 samples / Channel 1 samples / Channel 2 samples / Global trigger signals monitor
- T1 - Trigger Mode 1:** Channel 0 samples / Channel 1 CFD / Channel 2 MWD(28b msb) / Global trigger signals monitor
- T2 - Trigger Mode 2:** Channel 0 AGT Event information from datapath / Global trigger signals monitor
- S0 - TMS Mode 0:** Channel 0 / TMS(44b) / Global trigger signals monitor
- S1 - TMS Mode 1:** Channel 0 / MWD(32b) / TMS(16b)
- S2 - TMS Mode 1:** Channel 0 / Channel 1 / TMS(29b) / Global trigger signals monitor

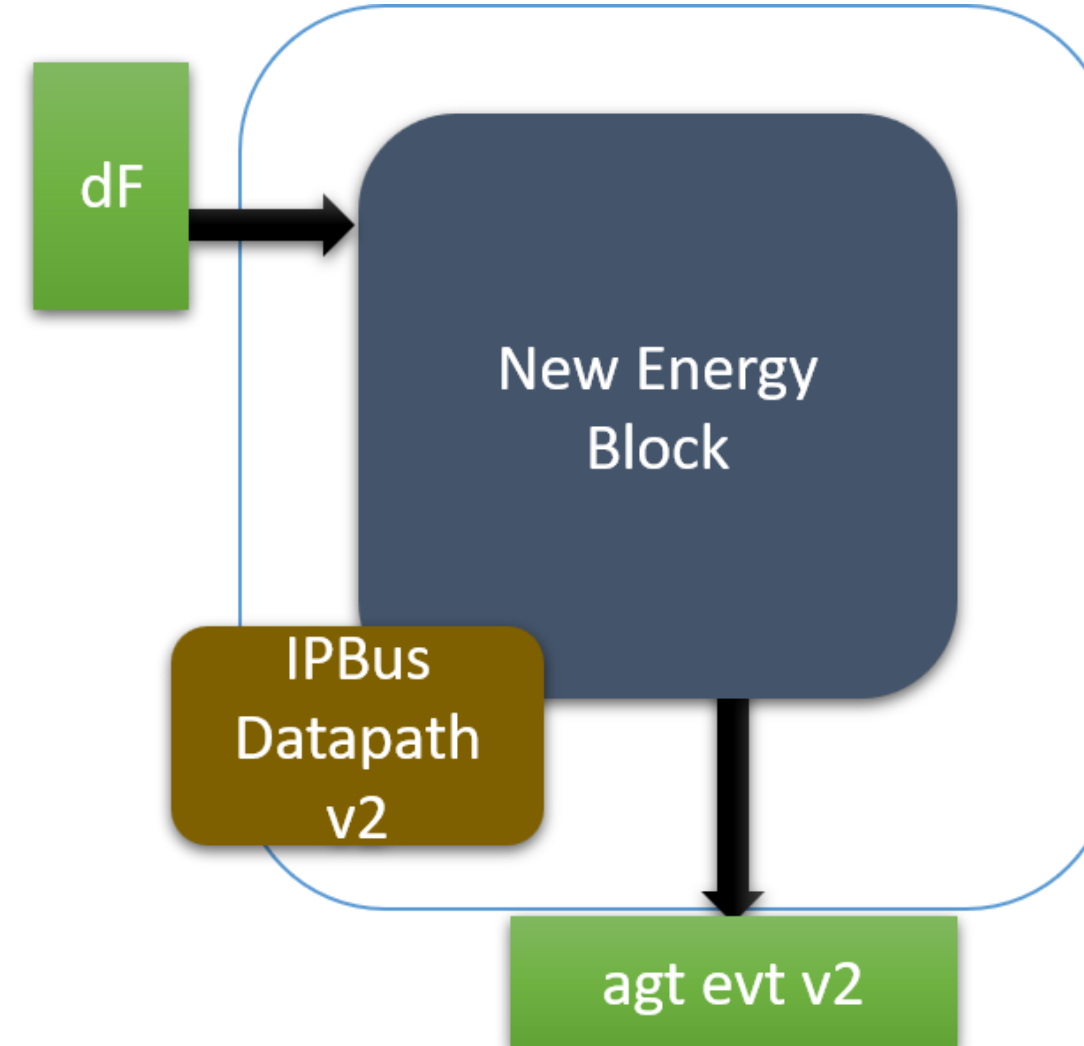
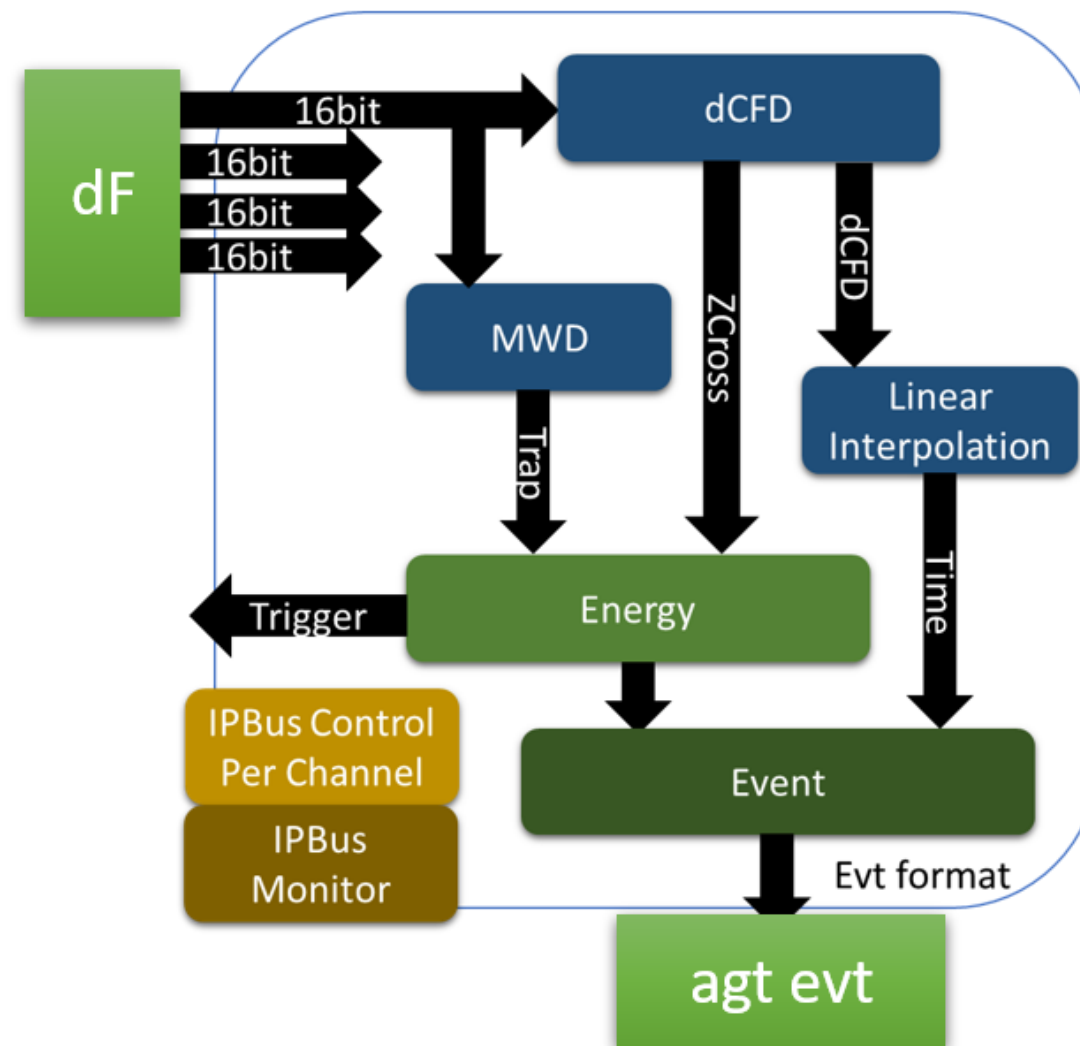
Global trigger signals monitor: GTS trigger + Local Trigger + External Trigger

Firmware

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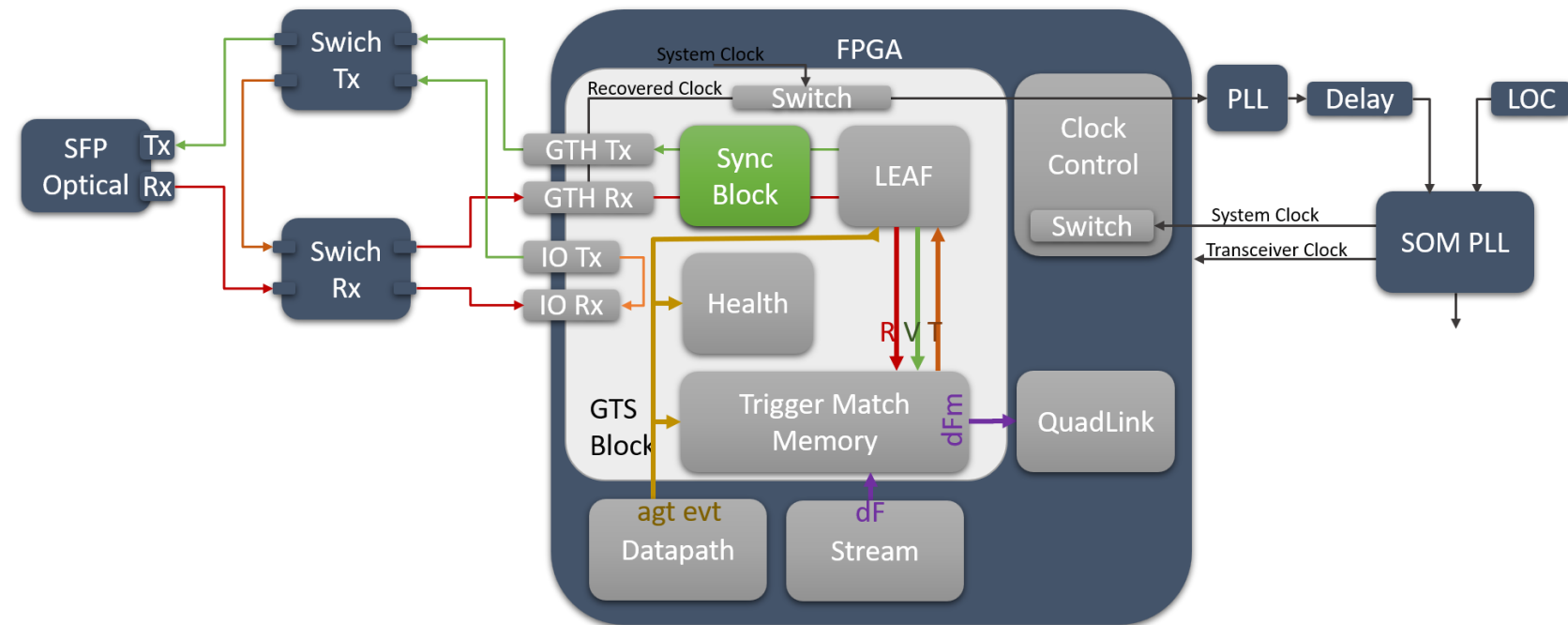


- Same Project
- Compilation Time Selected

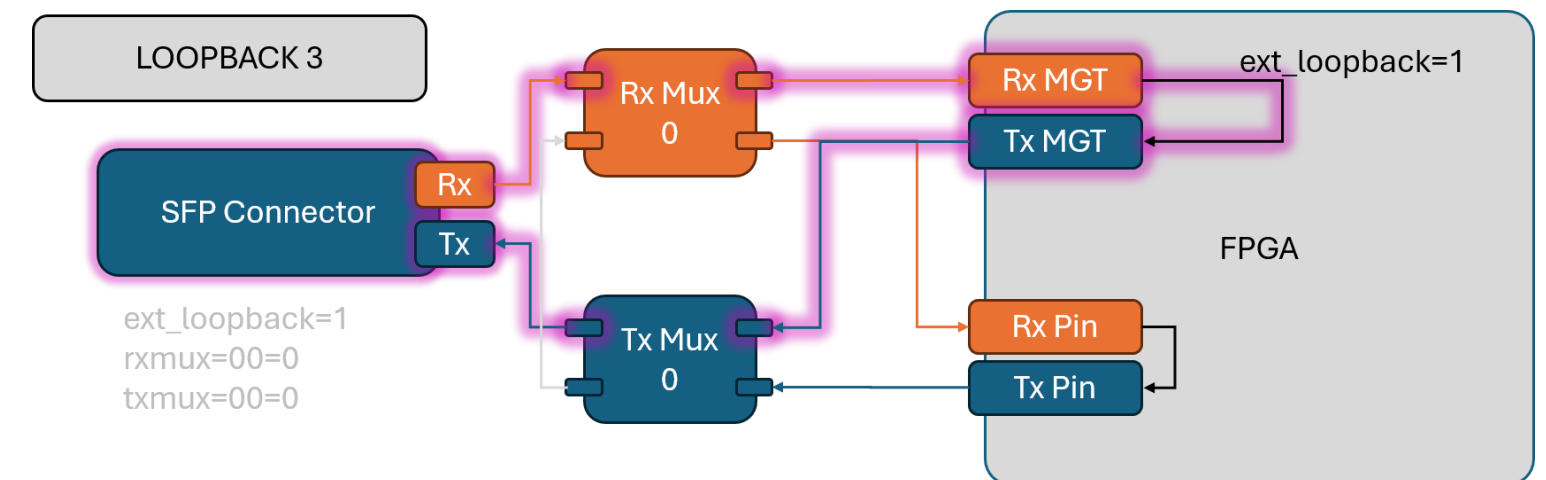
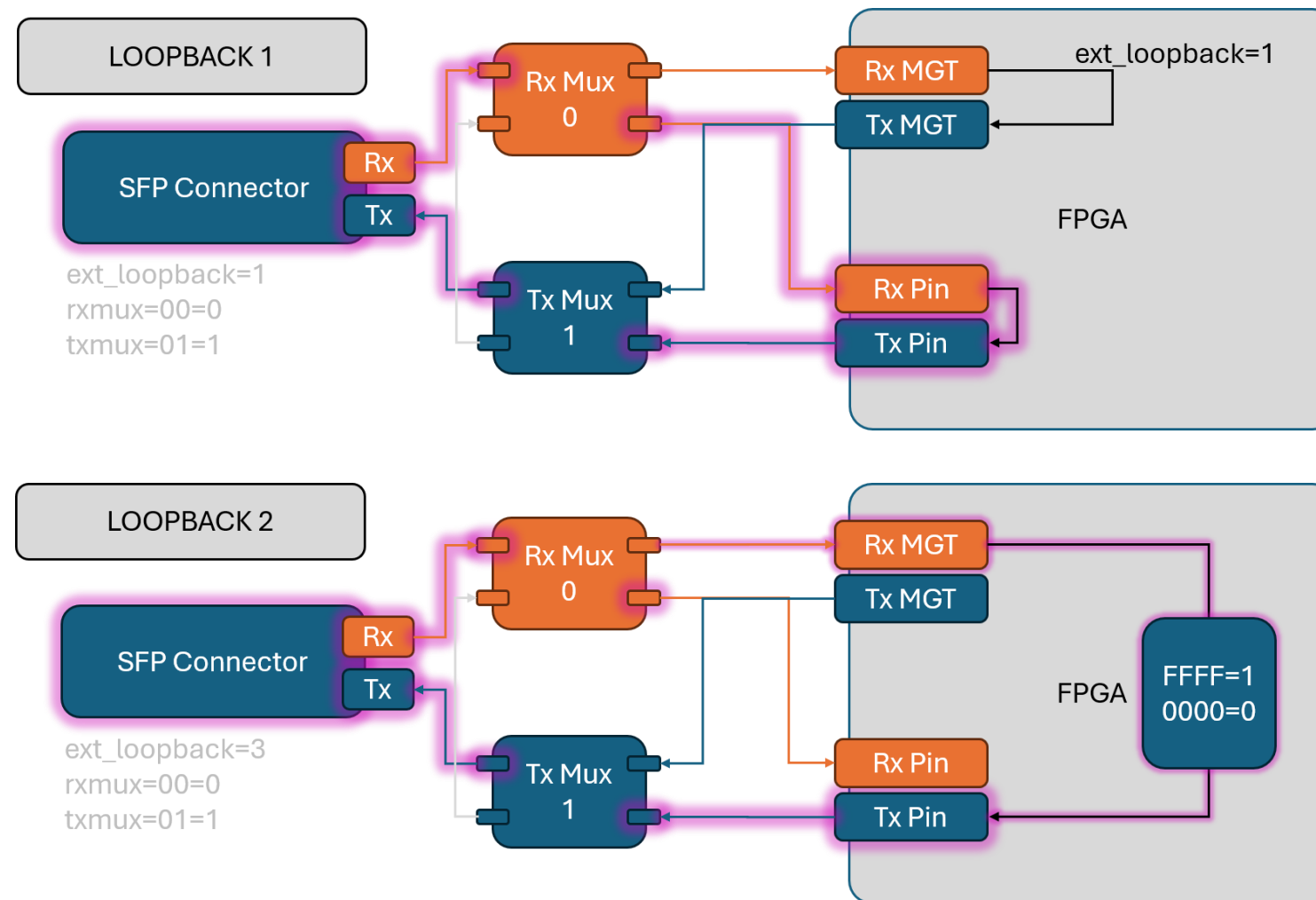
Firmware

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GTS

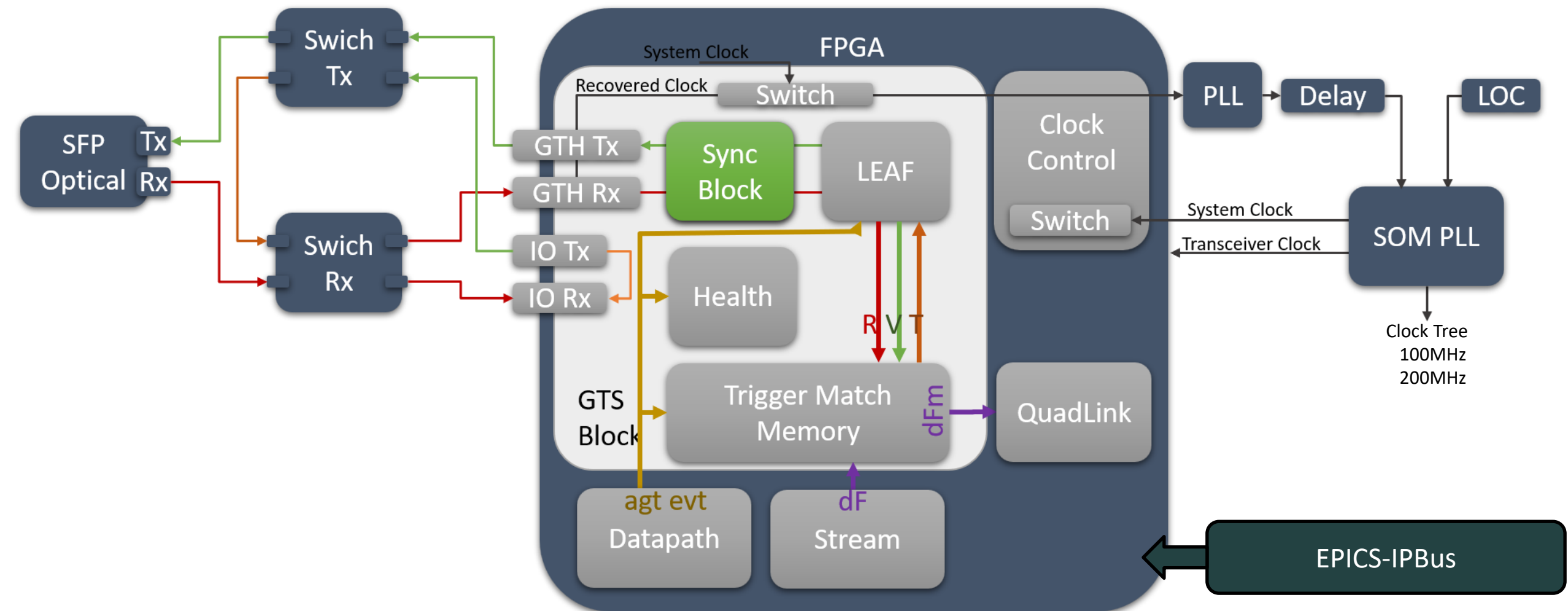


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Safe Selector

Clock Stable at startup

LEAF Update

Send Trigger and IDLE to TProcessor

Trigger Match Clear

Trigger Messages Update

External Trigger

Trg Ch 40

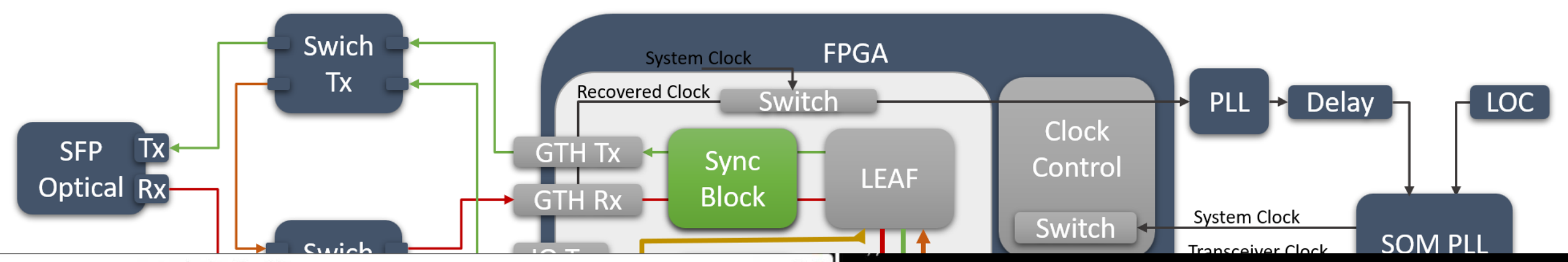
Trg Ch 41-79

Firmware

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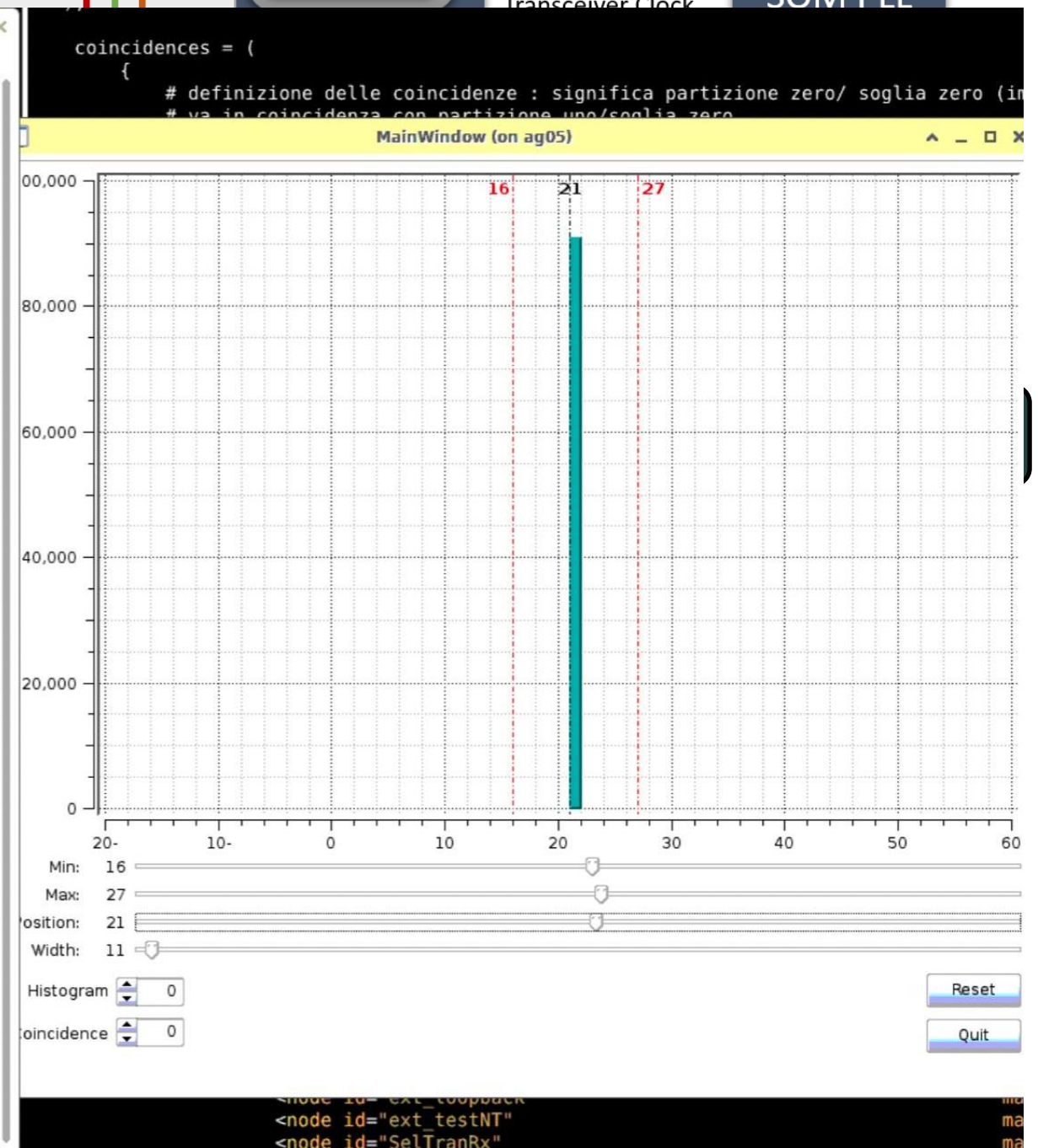
Updates

GTS



```
gammaDAQ@ag05: ~/bin
File Edit View Search Terminal Help

Aurora: CHANNEL UP      Input: RUN      Sort: RUN      t=100 k=0.5  V5      h: help
clock ..... 16.276.088.127  100.00 M      event number ..... 81.027  534.37
input trigger ..... 194.659  1.20 K      output reject ..... 32.598  130.17
input idle ..... 53.747.950  330.22 K      output validate ..... 162.054  1.07 K
sort trigger ..... 194.655  1.20 K
sort idle ..... 53.541.458  328.86 K
sumbus trigger ..... 108.126  664.54
sumbus idle ..... 53.533.804  328.83 K
sumbus under min ..... 0  0.00
transition ..... 108.126  664.54
gate reject ..... 27.099  130.17
gate validate ..... 81.027  534.37
threshold not reached ..... 0  0.00
threshold reached ..... 108.126  664.54
threshold equal ..... 108.126  664.54
sumbus trigger ..... 86.526  534.37
sumbus idle ..... 53.640.867  329.48 K
sumbus under min ..... 0  0.00
transition ..... 86.526  534.37
gate reject ..... 5.499  0.00
gate validate ..... 81.027  534.37
threshold not reached ..... 0  0.00
threshold reached ..... 86.526  534.37
threshold equal ..... 86.526  534.37
```

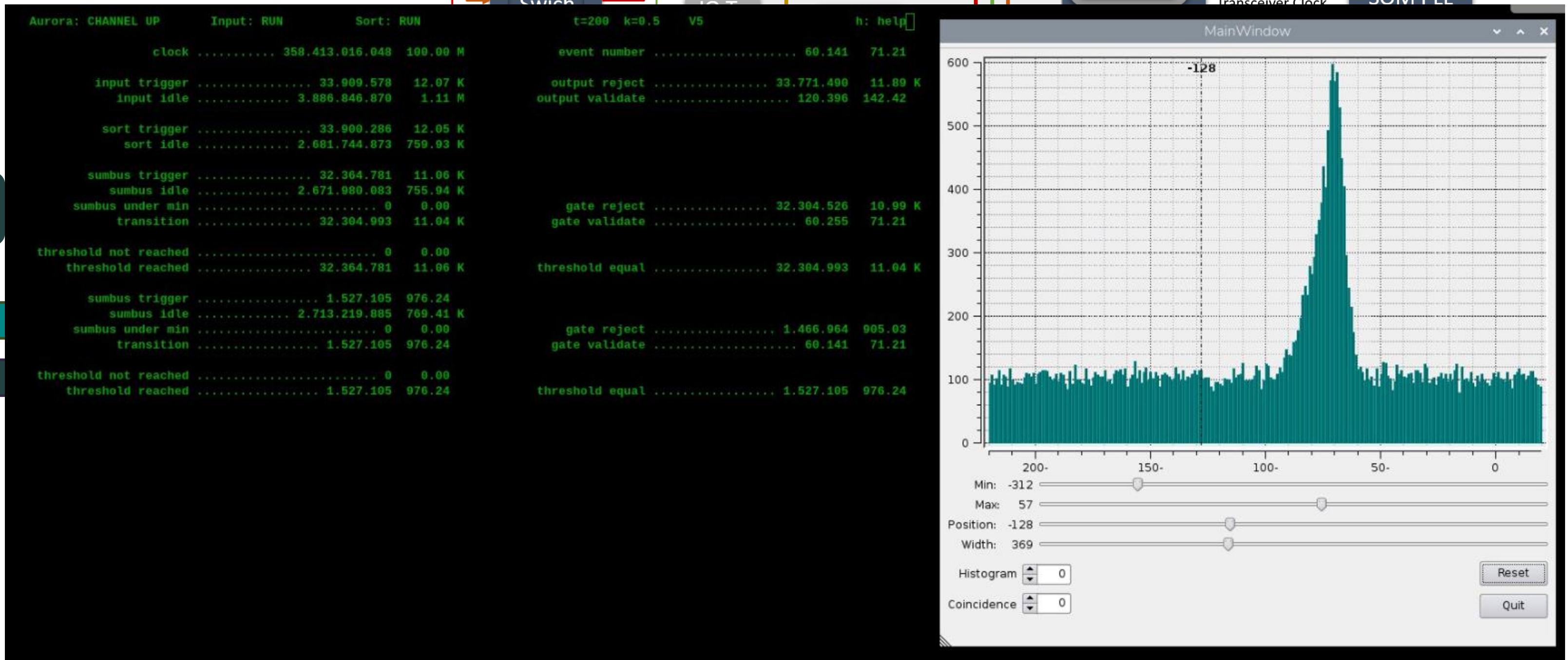
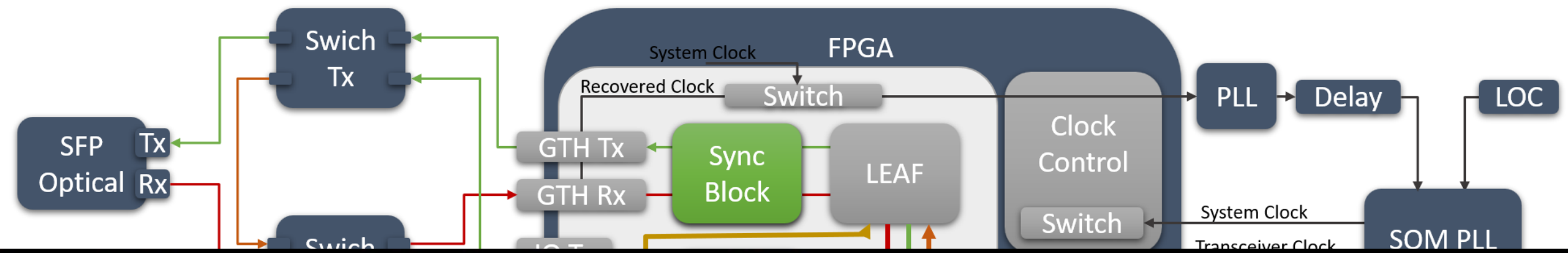


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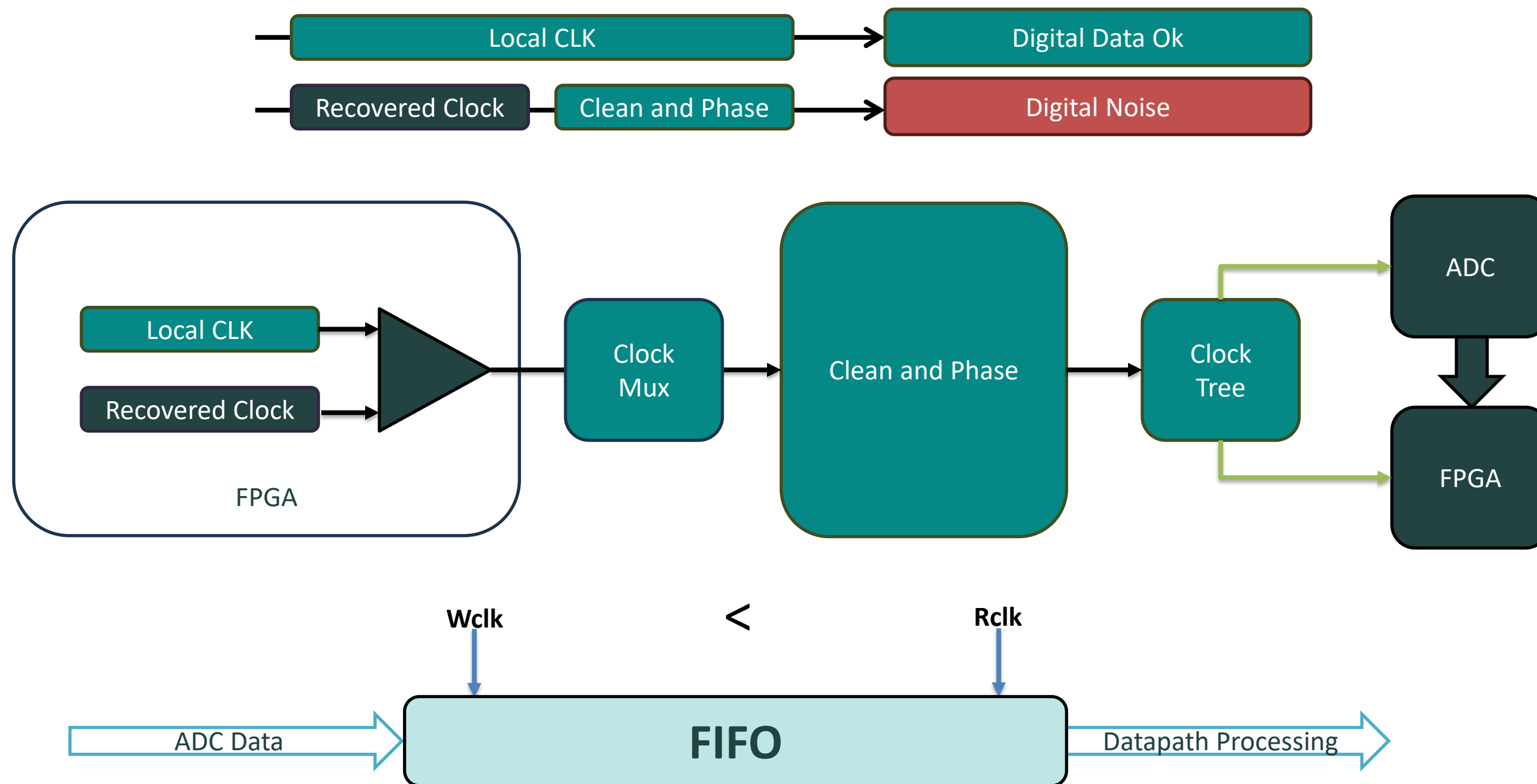


Firmware

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GTS



- Data incoming from ADC – Data losses ($BER > 10^{-8}$) depending on clock/board
- GTS Trigger Match Data framing (latest versions: energy or samples wrong)
- GTS link stability on some boards – clock start-up issue
- Slow control stability on some boards

Design Freeze

Script-based Project

Clean Data

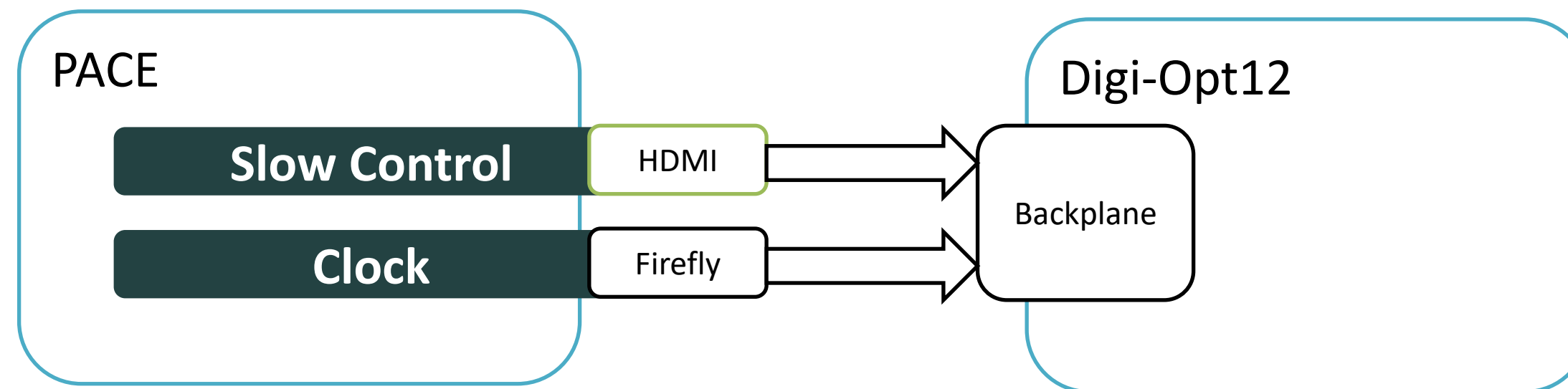
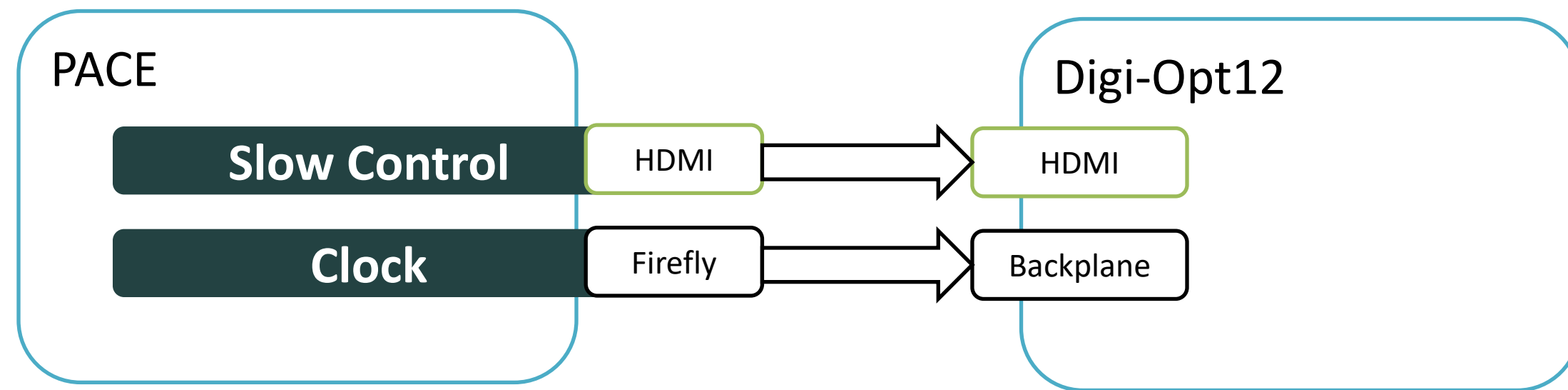
GTS

Design Freeze

Script-based Project

Clean Data

GTS



Design Freeze

Script-based Project

Clean Data

GTS

Stable

Reliable

Repeatable

Any Board

Design Freeze

Script-based Project

Clean Data

GTS

Stable

Clean Reset Status – Clock Issues

Reliable

Auto-diagnosis and recovery

Repeatable

Log System

Any Board

Error Diagnosis

Committed to Git

HDL sources .vhd / .v

Constraints .xdc

Build script build.tcl



One command

```
vivado -mode batch  
-source build.tcl
```

Creates the project, adds sources,
builds, writes reports

Design Freeze

Script-based Project

Clean Data

GTS

Communication protocol ADC-PACE-Readout

- Constant-phase problem correction
- FIFO update and self-test
 - Alt: Clean Clock Switch
- Auto-sync update

Design Freeze

Script-based Project

Clean Data

GTS



Communication protocol ADC-PACE-Readout

- Constant-phase problem correction
- FIFO update and self-test
 - Alt: Clean Clock Switch
- Auto-sync update

Design Freeze

Script-based Project

Clean Data

GTS



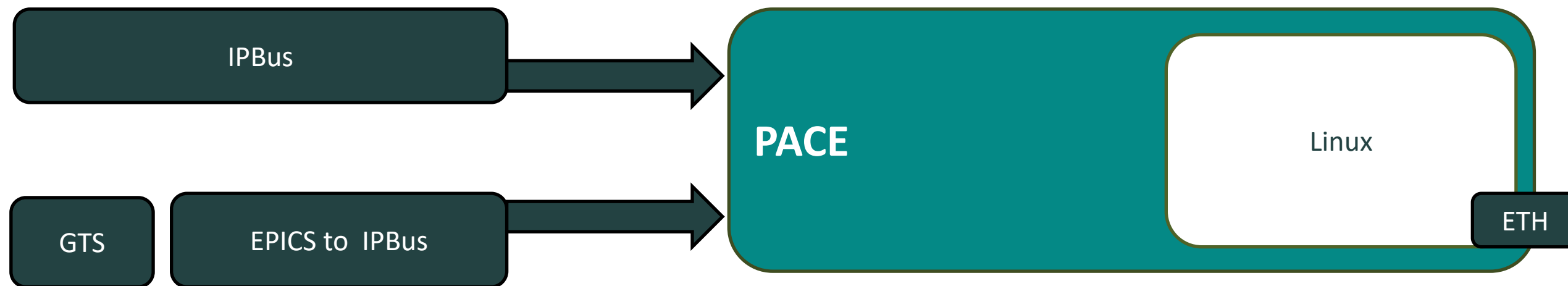
- ADF update and comparison with LTC
- Full simulation of different rates and response times (corner cases)
- Real test simulation of different rates and response times
- IPBus+EPICS to local PACE Linux

Design Freeze

Script-based Project

Clean Startup

GTS

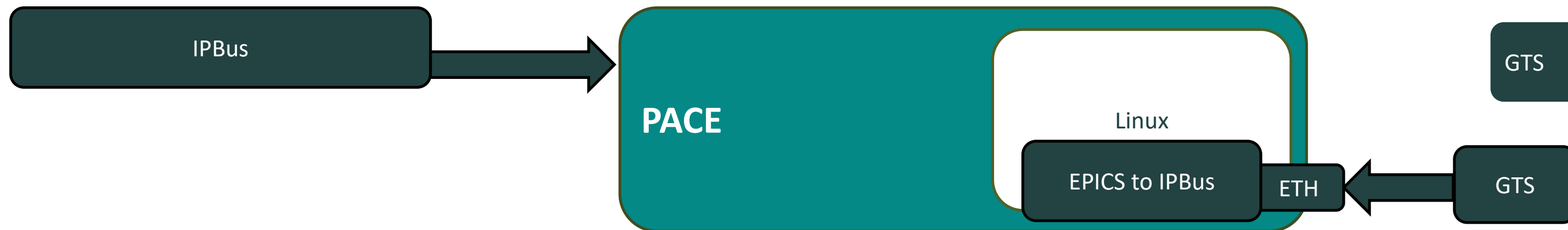


- ADF update and comparison with LTC
- Full simulation of different rates and response times (corner cases)
- Real test simulation of different rates and response times
- IPBus+EPICS to local PACE Linux

Design Freeze

Script-based Project

Clean Startup



SMART Implementation

AGATA Phase 2 Electronics PACE-CAP Firmware

