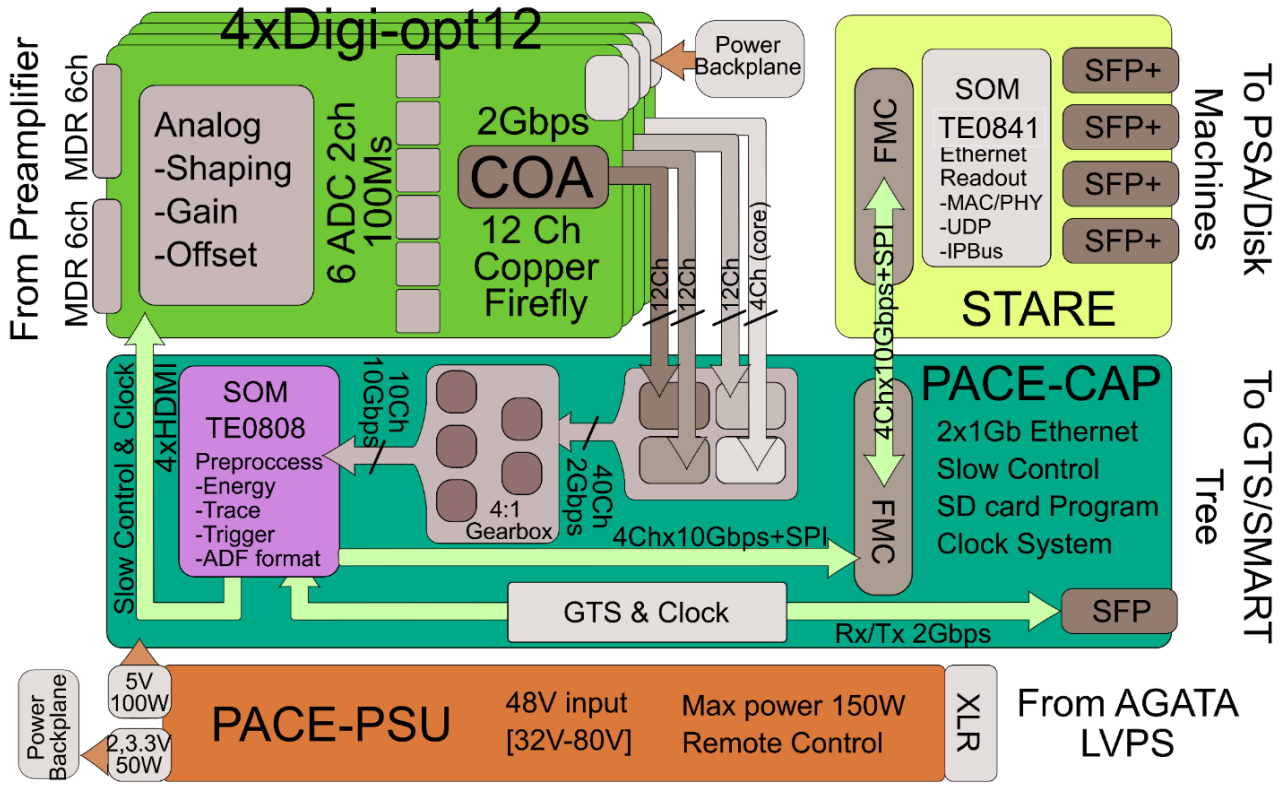
Front-end Electronics Working Group Plenary Session

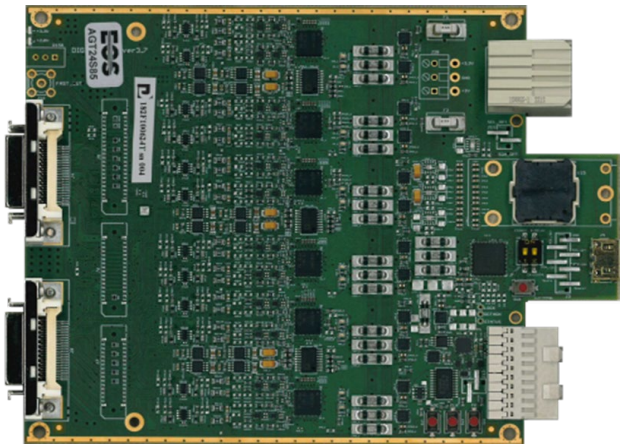
A.Gadea (IFIC, CSIC-University of Valencia, Spain)



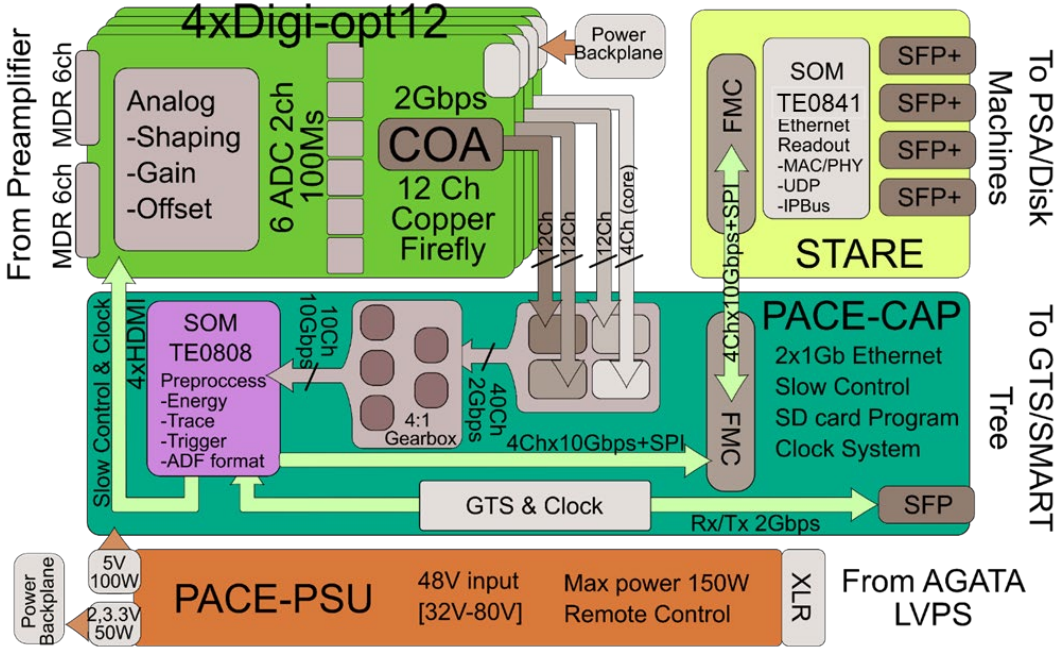
26th AGATA Week September 7th to 11th, 2025

HIL Warsaw, Poland

The AGATA Phase 2 Front-end Electronics

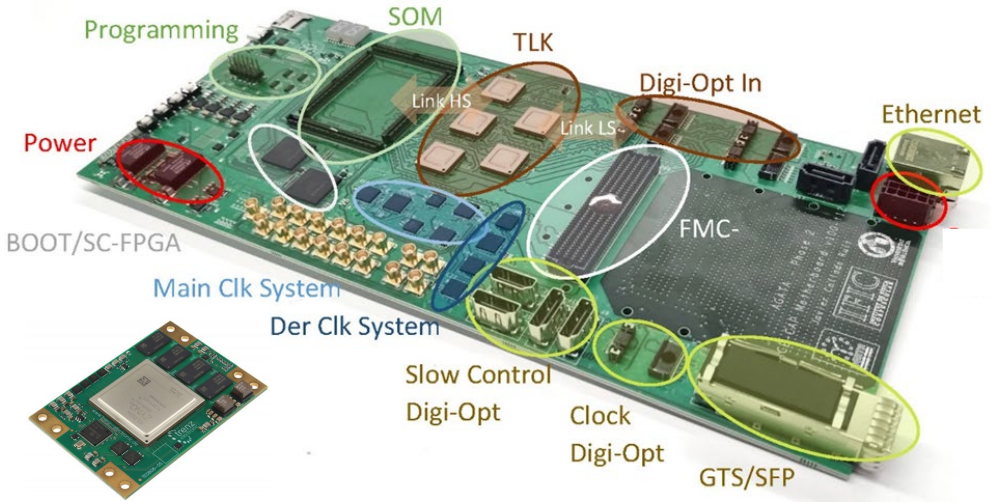


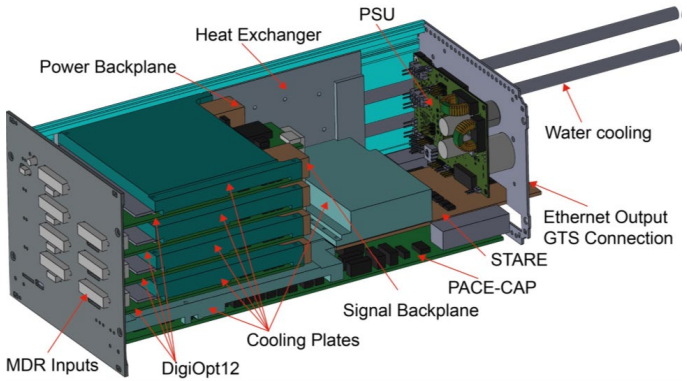
DIGIOPT12 v3.71

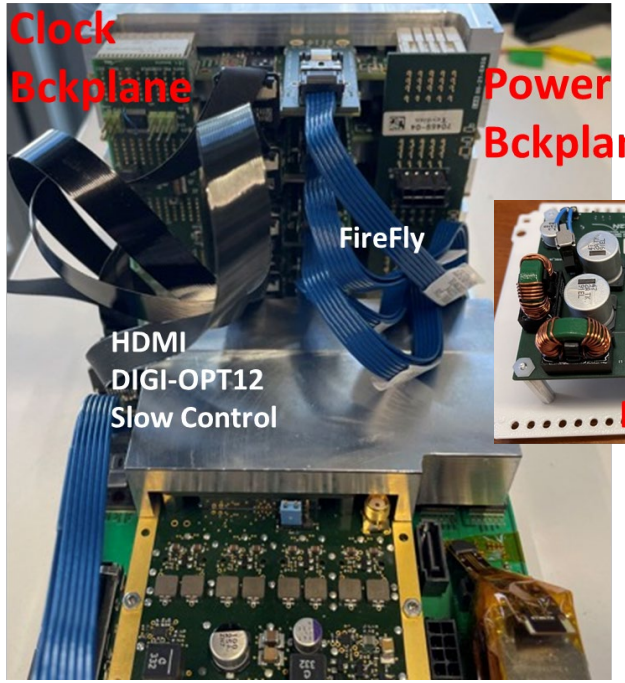


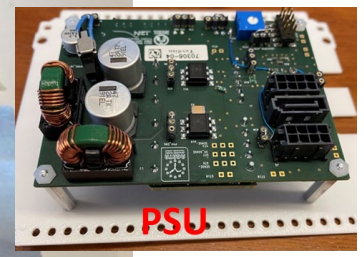
STARE

PACE-CAP-v100-t58

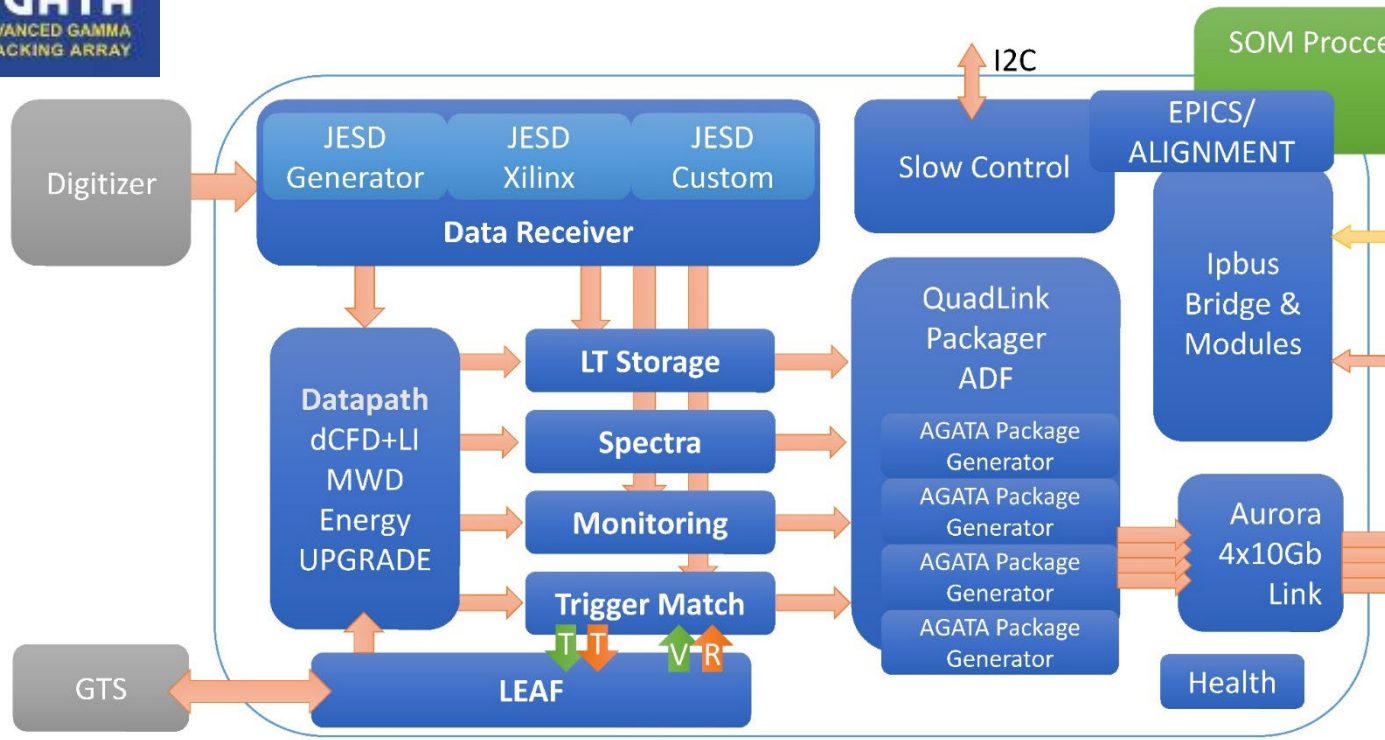








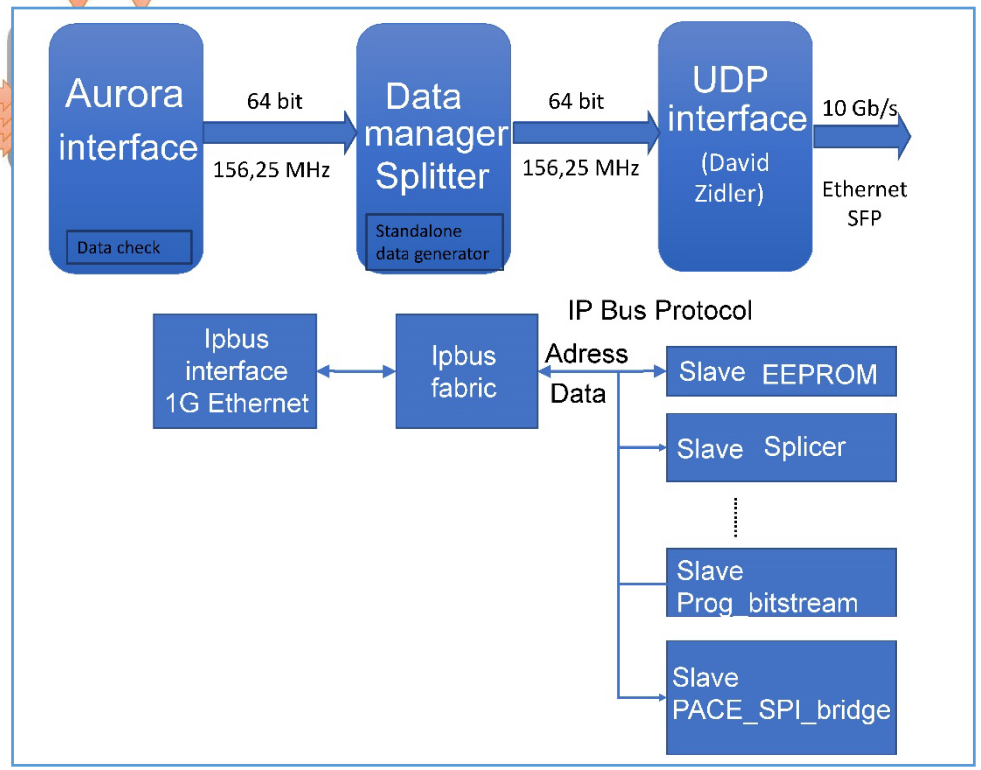
The AGATA Phase 2 Front-end Electronics



PACE Firmware

- All Firmware IP exists already
- STARE presently working with UDP, with good performance. Few upgrades done sine last AGATAweek
- PACE Firmware to be improved on Clock management, Data integrity, Start-up procedure, etc…

STARE Firmware



Schedule for the Hardware Delivery

- **DIGIOP12** 90 full sets in stock and 5 more cores (4 GSI, 1 Poland) , 14 more segments (10 GSI, 4 Poland) Segment boards modified for pre-amplifier gain control. Necessary to add new SPI/I2C control TE-cond. connector

- **STARE** 129 boards (hardware) are ready (Also 10 pre-production). SOM integration complete. Still few (4-5) STAREs have problems to be investigated. All SOMs Trenz TE0841 (135 plus spare) have arrived in Orsay.

- **PACE** 90 ordered. 57 delivered to Valencia; 3 with issues requiring repair; CAT performed for the GTS interface for 35 boards, 21 with the GTS ok, 14 with Rx/Tx issues or wrong PLL identification, system clock issues or power supply issues. All SOMs Trenz TE0808 (135 plus spare) have arrived in Valencia.

- **PSU** 50 early version existing 2 AGATA PSU-PH2 v2.13 pre-production tested and 60 under production

- **Cabling:** Firefly cables for 100 systems, HDMI cables are to be purchased because new connector in the DIGIOPT12 Existing COA adapters for 50 systems and connectors to complete the 135 + spare systems in fall 2026. Signal and Power backplanes existing for 135 + spare systems

- **Mechanics:** Existing cooling blocks: 240 digiopt12, 143 STARE, 135 PACE. 139 heat exchangers (84 to undergo alodine passivation) 81 front panels ready 25 ongoing and rear panels to be produced. Enclosures and crates existing for 105 systems.

Schedule for the Hardware Delivery

Schedule for the Firmware and Control

STARE Firmware: Full tested UDP firmware has been released already for sometime. New release with counters was sent to LNL for data transmission integrity tests and is integrated in the new test bench. STARE firmware has been updated to ignore PACE/STARE long messages that produced crash on the communications.
System test with 24 crystals and simulated data completed successfully over 100Gbit links at 95Gbits aggregate rate, concluding that RUDP might not be needed.

PACE Firmware: Progress in the context of the 1st contract with Zeptonova, with the collaboration of LNL, IFIC and ETSE and GANIL: AGATA Ph2 Trigger Firmware, Monitoring Block, Control System with the New PLL, PACE Test Setup, Implementation of a New Energy IP Block, Migration to the Latest Xilinx, Platform Firmware Documentation. The 2nd contract: GTS-to-Trigger Processor communication in the AGATA Ph2 PACE firmware, fine delay measurement in the Root TDC, Validation and verification of the external trigger input 3rd contract (ongoing) DIGIOPT12 slow control interfacing.
Proposal for a 4th contract **PACE-CAP Design Freeze Project:** Start-up reliability, Produce a Script mode project generator, Data-path integrity, Global System Time and event synchronization, including GTS and SMART,

Slow control Python 3 upgrade is complete and all working. Register changes from STARE and PACE have been incorporated into slow control. Ch. Bonnin is keeping his GUI interfqace version aligned to the development version STARE python 3 updates made to support latest version (including flashing firmware).

Future of the AGATA Front-End Electronics W.G.

- The long construction time and frequent component obsolescence oriented AGATA to follow cycles of R&D and production of electronics.

- Phase 2 Electronics concept developed from 2017 to 2019 (proof-of-concept). From 2021 to 2024 we lost key personnel for the firmware and hardware of PACE.

- Overcome by longer development period and outsourcing since 2025 to Zeptonova the completion and maintenance of the pre-processing firmware. We expect to complete the development late 2026/ early 2027.

- Considering the future developments of AGATA, we to rebuild teams with staff personnel taking over know-how of the AGATA pre-processing electronics, with the support of Zeptonova.

Front-end Electronics Working Group
Plenary Session

- Introduction and Schedule 10'
I.Lazarus (STFC Daresbury) / A.Gadea (IFIC Valencia)

- Digitizers (DIGOPT12) Status, Advancements and Production on V.3.7.1 20'+5'
A. Pullia (INFN and Uni. Milano) (Videoconference contribution)

- STARE Hardware and Production Firmware Status 20'+5'
X. Lafay / N.Karkour (IJCLab Orsay)

-PACE Hardware and Firmware Status 25' + 5'
J. Collado (ZeptoNova Boutersem, Belgium) (Videoconference contribution)

10:30 – 11:00 Coffee Break

AGATA
ADVANCED GAMMA TRACKING ARRAY

Front-end Electronics Working Group
Plenary Session

- Status of the mechanics, PSS, cooling, infrastructure 15'+5'
V. Gonzalez (ETSE Uni. Valencia)

- CAEN Digitizer test 15’+5’
A.Goasduff (INFN-LNL, Legnaro)

- Trigger for the ZeroDegree Campaign at INFN-LNL 15’+5’
A. Goasduff (INFN-LNL Legnaro) ,

- Status of the SMART Development 15'+5'
M. Bezard (GANIL, Caen) (Videoconference contribution)

-Status of the AGATA Phase 2 Control 15’+5’
Ch.Bonnin (IPHC, Strasbourg)

AGATA
ADVANCED GAMMA TRACKING ARRAY

Front-end Electronics Working Group
Plenary Session

MICIU, AIE and Generalitat Valenciana, Spain under Grants PID2023-150056NB-C4 and CIPROM/2022/54

Front-end Electronics Working Group
Plenary Session

Thank You

MICIU, AIE and Generalitat Valenciana,
Spain under Grants
PID2023-150056NB-C4 and CIPROM/2022/54

GENERALITAT VALENCIANA

GOBIERNO DE ESPAÑA
MINISTERIO DE CIENCIA, INNOVACIÓN Y UNIVERSIDADES
AGENCIA ESTATAL DE INVESTIGACIÓN

AGATA
ADVANCED GAMMA TRACKING ARRAY