DRD7 activities

-few selected topics-

November 27th, 2025

Marlon Barbero, CPPM (with many slides borrowed from: https://indico.cern.ch/event/1556239)

5th FCC / DRD France workshop

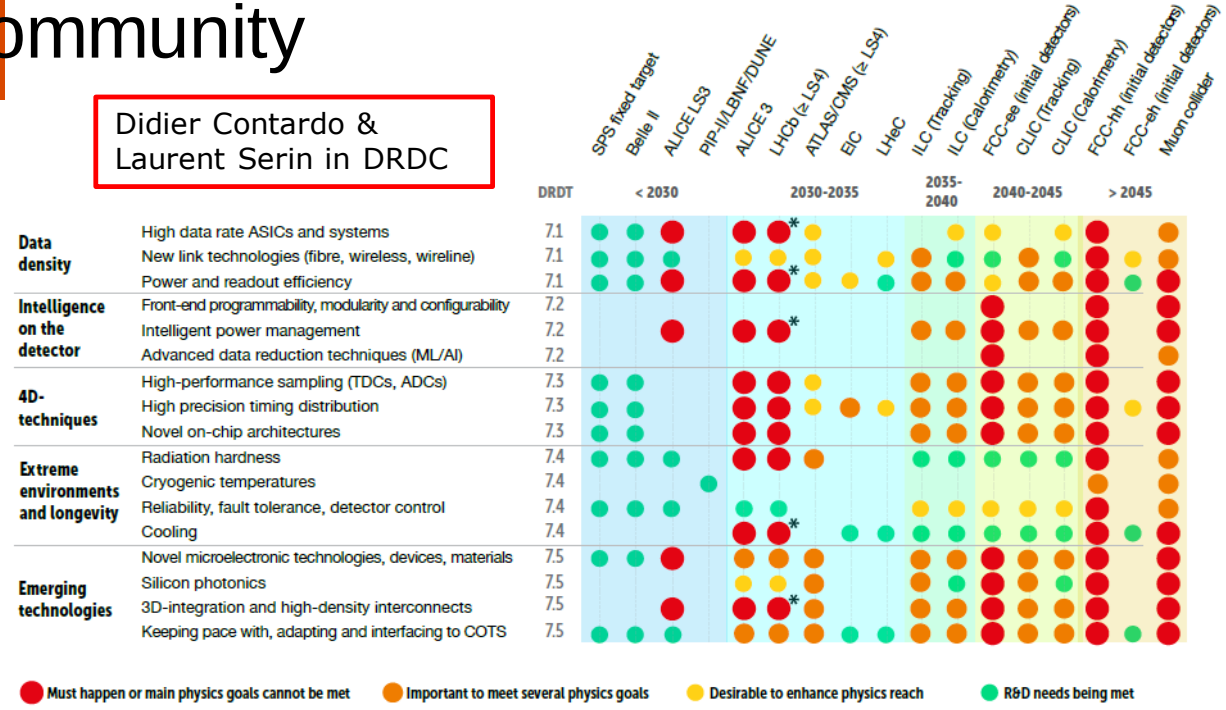
DRD 7 goals & french community

○ DRD7: Electronique

Electronics

- **DRDT 7.1** Advance technologies to deal with greatly increased data density
- **DRDT 7.2** Develop technologies for increased intelligence on the detector
- **DRDT 7.3** Develop technologies in support of 4D- and 5D-techniques
- **DRDT 7.4** Develop novel technologies to cope with extreme environments and required longevity
- **DRDT 7.5** Evaluate and adapt to emerging electronics and data processing technologies

Didier Contardo &
Laurent Serin in DRDC

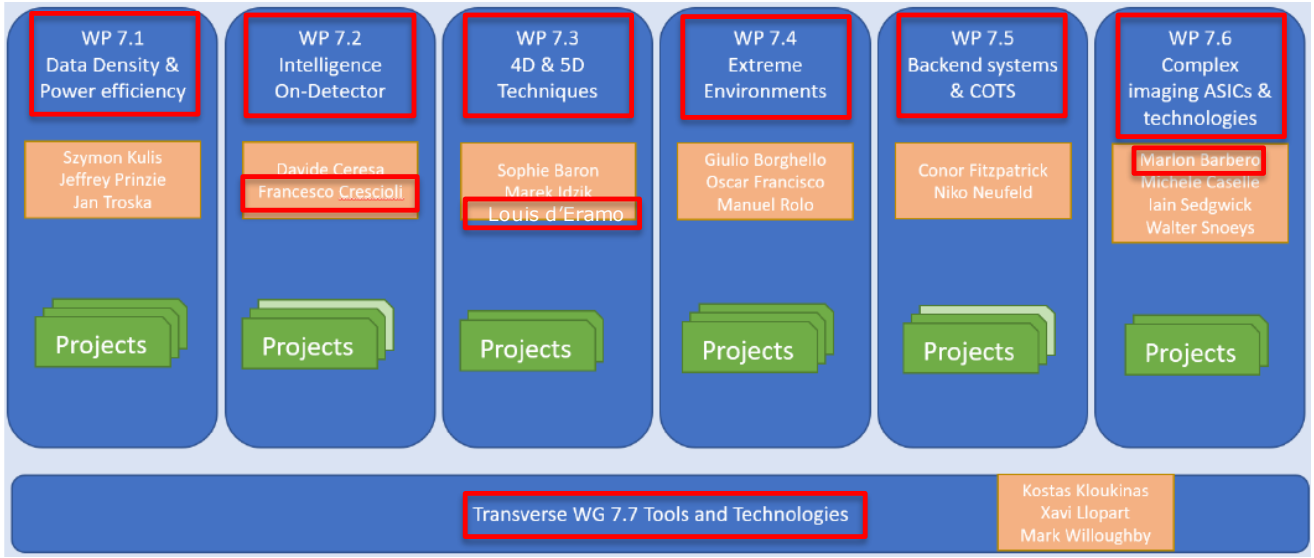


Goals: Follow strategic R&Ds in electronics, support access to technologies, tools and knowledge, and aim for the DRDT.

DRD7 is transverse by design, supports to other DRDs → Can sometime be at the interface to other DRDs.

DRD7 proposal 2024 → DRD7 approval June 5th 2024

Last workshop: Sept 2025
https://indico.cern.ch/event/1556239



DRD 7 : WP organisation

DRD7 Project Management:
Spokesperson: F. Simon
Deputy: A. Rivetti

→ **Collaboration Board**
Chair: A. Andreazza
Deputy: C. Fernandez Bedoya

Steering Committee
J. Baudot, M. French, D. Gascon Fora, K. Klein, R. Kluit, A. Rivetti, F. Simon, F. Vasey

Technical Committee

WG 7.7: Tools and technologies
A hub-based structure for ASIC developments
Conveners: K. Kloukinas, X. Llopart Cudie, M. Willoughby

	Projects / *Project leaders*
WP 7.1: Data density and power efficieny *Conveners:* S. Kulis, J. Prinzie, J. Troska	7.1.a: *Silicon photonics tranceiver development* | J. Troska 7.1.b: *Powering next generation detector systems* | M. Karagounis, S. Michelis 7.1.c: *Wireless power and data transmission* | E. Locci
WP 7.2: Intelligence on the detector *Conveners:* D. Ceresa, F. Crescioli	7.2.a: *Radiation tolerant RISC-V SoC* | K. Kloukinas, L. Marien 7.2.b: *Virtual electronic system prototyping* | D. Ceresa, M. Kachel
WP 7.3: 4D and 5D techniques *Conveners:* S. Baron, M. Idzik	7.3.a: *High performance TDC and ADC blocks at ultra-low power* | M. Idzik 7.3.b: *Strategies for characterizing and calibrating sources impacting time measurements* | L. d'Eramo, G. Zecchinelli 7.3.c: *Timing distribution techniques* | S. Baron, J. Galindo
WP 7.4: Extreme environments *Conveners:* G. Borghello, M. Da Rocha Rolo, O. A. de Aguiar Francisco	7.4.a: *Device modelling and development of Cryogenic CMOS PDKs & IP* | M. Da Rocha Rolo 7.4.b: *Radiation resistance of advanced CMOS nodes* | G. Borghello 7.4.c: *Cooling and cooling plates* | O. A. de Aguiar Francisco
WP 7.5: Back-end systems and commercial off-the shelf components *Conveners:* C. Fitzpatrick, N. Neufeld	7.5.a: *DAQOverflow* | A. Keshavarzi 7.5.b: *From FE to BE with 100 GbE* | F. Alessio, A. Pellegrino
WP 7.6: Complex imaging ASICs and technologies *Conveners:* M. Barbero, M. Caselle, I. Sedgwick, W. Snoeys	7.6.a: *Common access to selected imaging technologies* | M. Barbero, M. Da Rocha Rolo, I. Sedgwick, W. Snoeys 7.6.b: *Shared access to 3D integration* | M. Caselle, L. Andricek, S. Charlebois

DRD 7 : WP1→ Data Density and Power Efficiency

7.1.a: Silicon Photonics Transceiver Development

Develop high-speed optical transceivers based on Silicon Photonics technology for use in a wide range of future particle physics applications from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors.

Project Leader:
Jan Troska, CERN

7.1.b: Powering Next Generation Detector Systems

Develop power distribution schemes and their voltage/current regulators and converters for use in a wide range of future particle physics applications, from low-temperature neutrino detectors to high-radiation environment HL-HLC pixel detectors and beyond.

Project Leaders:
Michael Karagounis, FH Dortmund
and Stefano Michelis, CERN

7.1.c: WADAPT Wireless links and free-space optics

Develop wireless technology based on a millimeter wave transceiver IC as well as on Free Space Optics to connect neighboring detector layers, providing increased data rates, high power efficiency and high density of data links, with the aim of reducing mass and power consumption.

Project Leader:
Elizabeth Locci, DGIST

WP convenors:
Szymon Kulis, CERN
Jeffrey Prinzie, KUL
Jan Troska, CERN

DRD 7 : WP1b Powering

DC/DC Conversion

- GaN converter 48V -> 5V conversion (CERN)
- GaN converter 48V -> 2.5V conversion (Taltech)
- Fully integrated resonant 28nm 5V -> 0.9V (CERN)
- FCML with external air coil 28nm 5V -> 0.9V (FH Dortmund)
- GaN converter characterization (RWTH Aachen)

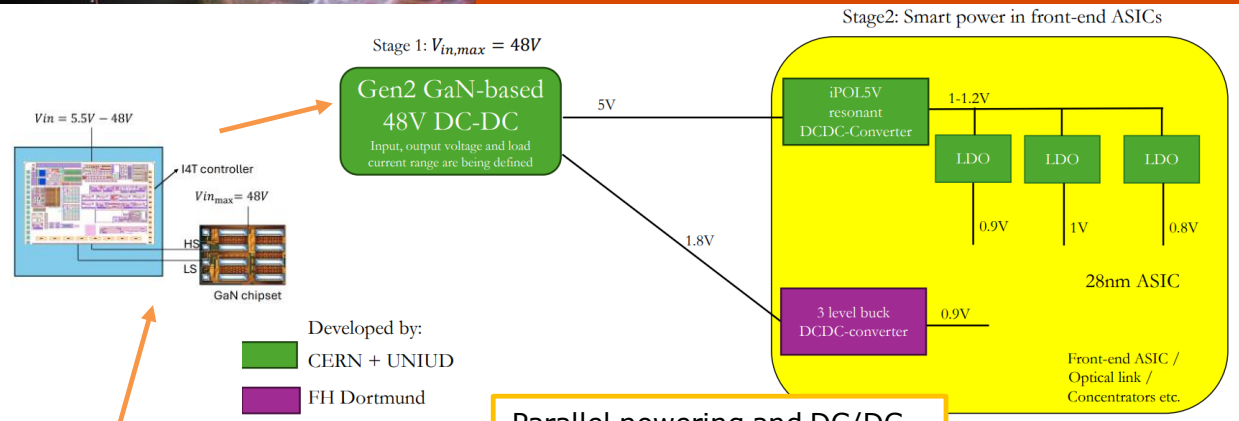
Serial Powering

- 28 nm porting of SLDO (FH Dortmund)
- High-Efficiency switch-mode SLDO (FH Dortmund)
- GaN Constant Current Source (ITANNOVA)
- Serial Power Pixel Modules (MILANO)

CERN – Stefano Michelis, Marta Macaluso, Antonio Ocarino, Sokratis Koseoglou
FH Dortmund - Jeremias Kampkötter, Hossein Tavakoli, Michael Karagounis
ITANNOVA - Fernando Arteche, Alvaro Pradas
University of Milano and INFN - Attilio Andreazza, Attilio Andreazza, Massimo Lazzaroni, Fabrizio Sabatini, Riccardo Zanzottera
RTWH Aachen - Lutz Feld, Katja Klein, Martin Lipinski, Joëlle Savelberg
TALTECH - Abdul Majid Bhat, Dr. Andrii Chub, Prof. Dmitri Vinnikov

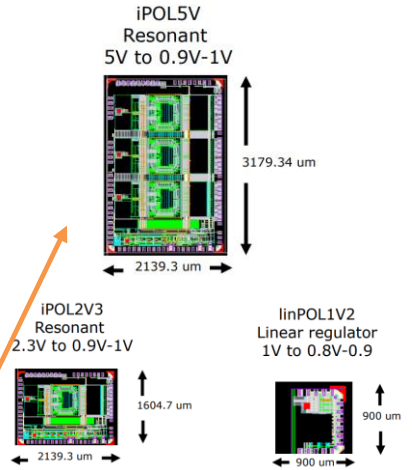
DRD 7 : WP1b Powering many activities

M.Karagounis©!
https://indico.cern.ch/event/1556239/

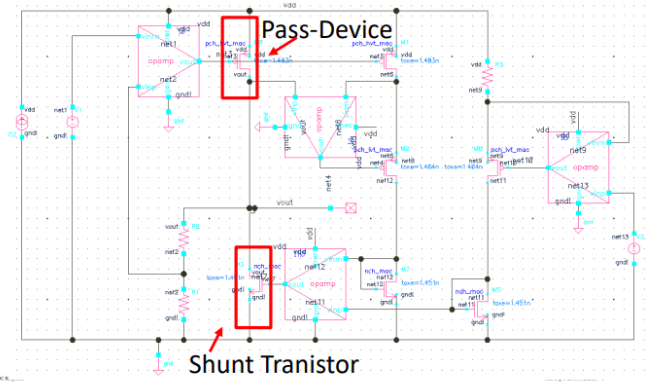


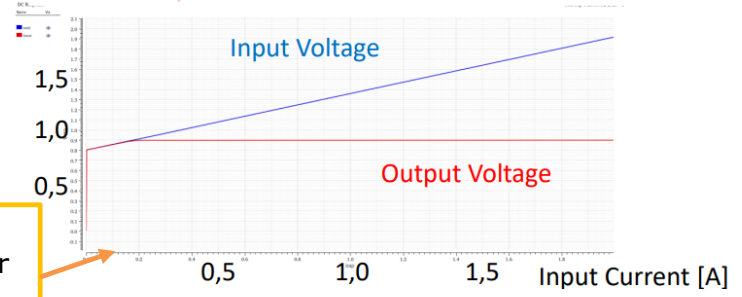
DC/DC converters 48V → 5V/1.8V at CERN.

Parallel powering and DC/DC converters 48V → 5V/1.8V



Today under testing





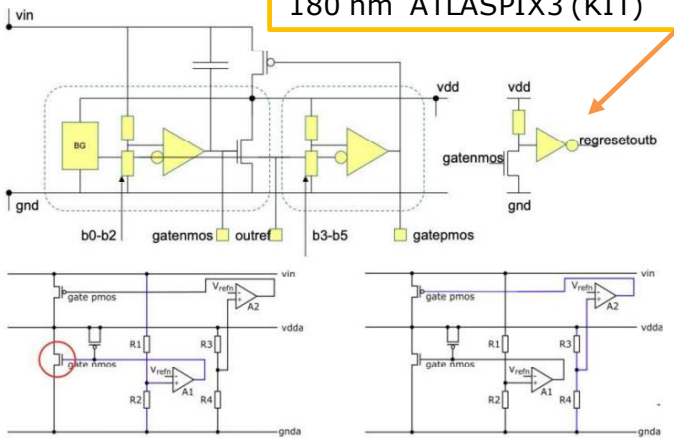
ShuntLDO design porting to 28 nm (Dortmund) improving power efficiency in regulator

ShuntLDO in HV CMOS TSI 180 nm ATLASPIX3 (KIT)

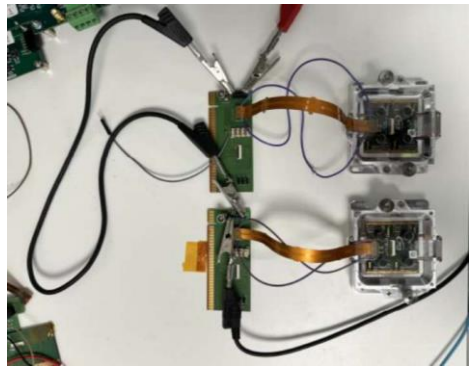
Version **ATLASPix3.1** has possibility for **serial powering** through **two shunt/low dropout regulators**

- **digital** and **analog** (VDDD/A)
- **3 bits** to tune threshold of shunt regulator
- **3 bits** to tune VDD
- gatenmos, outref, gatepmos are for monitoring
- regresetoutb can be used as power on reset

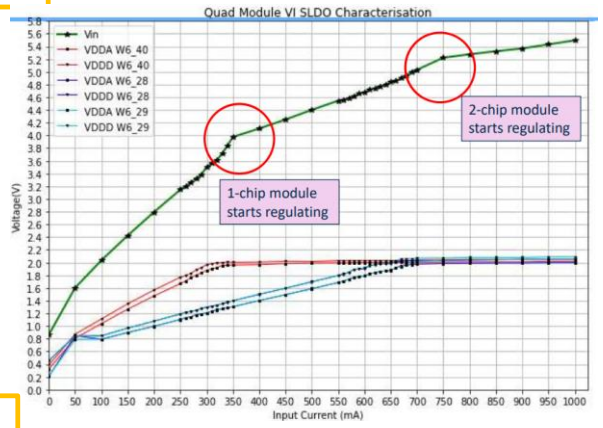
Possibility to use a **single power supply for all the 6 alimentation needed to operate the chips**



- First loop defines **shunt regulators**
- Second loop **regulates VDDD/As**



Powering a SP chain of 2 quad modules



Very active DC/DC serial powering activites within 7.1b

DRD 7 : WP2 → Intelligence on Detector

Two projects and one group of interest:

7.2~~c~~a : Virtual Electronic System Prototyping

Project Leaders: ***Davide Ceresa, CERN and Maciej Kachel, IPHC***

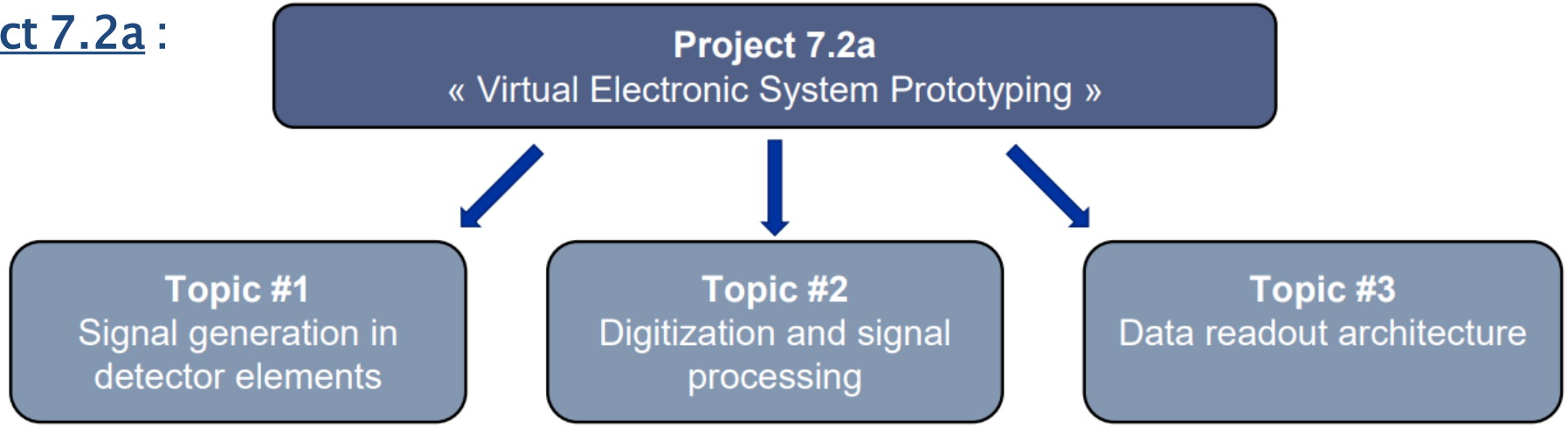
7.2b : Radiation Tolerant RISC-V System-On-Chip

Project Leaders: ***Kostas Kloukinas, CERN and Levi Marien, KU Leuven***

7.2c (not started and not in MoU) : Radiation Tolerant Embedded FPGA (eFPGA)

Conveners: Davide Ceresa and Francesco Crescioli

Focus on Project 7.2a :



The project aims to develop a simulation of the readout chain of a particle detector at a high level modelling the essential components and processes that occur from the moment particles interact with the detector to the digital readout of the collected data.

DRD 7 : WP2a → Virtual Electronic System Prototyping

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From the particle interaction with the sensor...

Simulation flow

... to the chip digital output

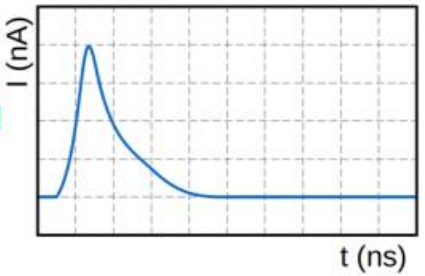
Allpix²: benefits from accuracy of both physical and electrical simulation https://gitlab.cern.ch/allpix-squared/libapx

Sentaurus TCAD SYNOPSYS

Sensing element design

ap² allpix squared

Charge deposition + collection (+ digitization)



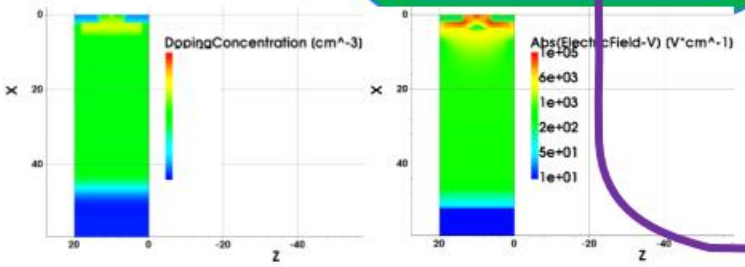
Digitization + signal processing

cadence

IPHC Institut Pluridisciplinaire Hubert Curien STRASBOURG

DESY.

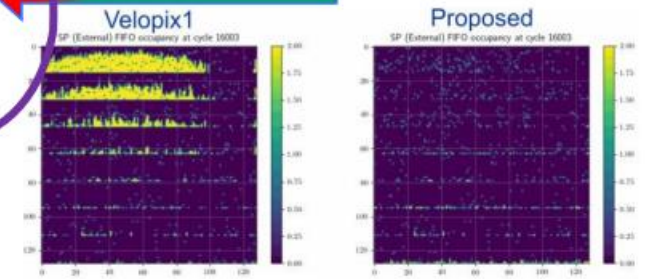
CERN



Doping concentration and electric field maps

Pix ESL

Readout architecture sizing



From "PixESL: A virtual Electronic System Level prototyping framework", Jashandeep Dhaliwal, 25/09/2023, p.5

Actual status of the project

Done

To be done…

PixESL: virtual prototyping framework for pixel detectors https://gitlab.cern.ch/iod/pixesl-group/pixesl-project-template

High level modelling readout chain simulation becoming available

DRD 7 : WP3 → 4D & 5D techniques

Number	Title	Description	Start date	End date
D7.3a	High performance TDC and ADC blocks at ultra-low power	Develop ultra-low power high performance TDC and ADC blocks for use in future particle physics experiments.	Sep.24	Jun.27
D7.3b	Strategies for characterizing and calibrating sources impacting time measurements	Study and propose generic data-driven calibration strategies for the time measurements in detectors requiring high precision timing	Nov.24	Jun.27
D7.3c	Timing Distribution Techniques	Study and propose strategies to optimize and assess ultimate precision and determinism of timing distribution systems for future detectors.	Mar.24	Jun.27

From the Annex…

- Many designs ongoing
- Various technologies
- Very promising results

- Progress on understanding impact of timing instabilities
- Portfolio of effects identified
- Practical tests started

- Better understanding on FPGAs performances
- Implementation of White Rabbit techniques on various platforms progressing
- First measurements with ASICs and PCs of generic solutions

DRD 7 : WP3a → ADC & TDC

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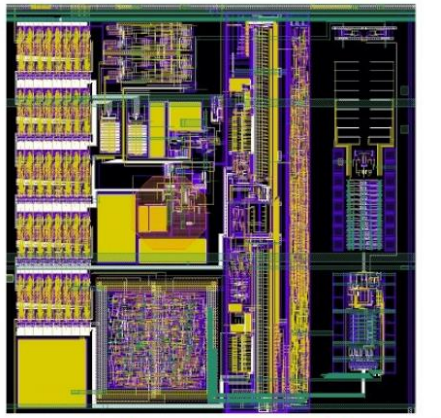
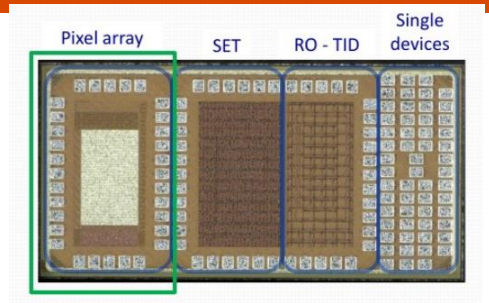


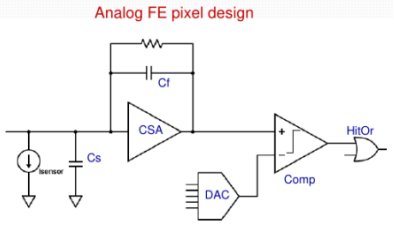
EICROC0
- Preamp, discri taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout : FIFO depth 8 (200 ns)

EICROC1 : 32x32
- Goal test full scale analog performance
- Tests with sensor

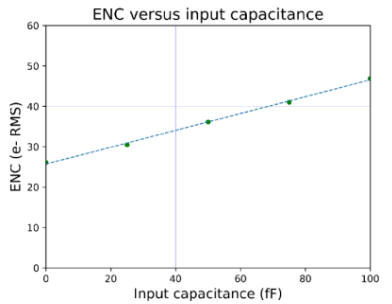
Omega has been coordinating development of several readout ASICs:
- HGCROC – collaboration with AGH, CEA, CERN, Imperial
- ALTIROC - collaboration with AGH, CERN, LPCF, SLAC
- HKROC - collaboration with AGH, CEA, CERN, Imperial

OMEGA : EICROC



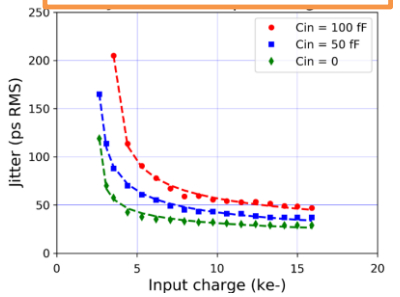


CPPM dvp in 28 nm



- Analog matrix in 28 nm technology :
  - Pixel pitch 25 µm
  - Gain charge/voltage : 95 mV / ke-
  - 8 µW / analog pixel
  - Threshold dispersion 130 e- RMS
  - Noise 47 e- ENC (for Cdet = 100 fF)
- jitter < 50 ps rms for C_{in} = 100 fF (and approx. 37 ps when C_{in} = 50 fF)
- TDC to be added in next proto (2026)

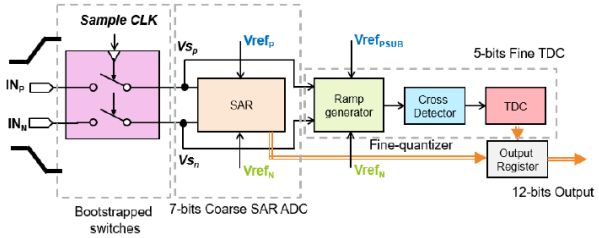
Jitter versus input charge

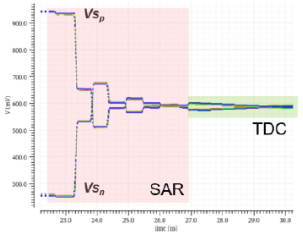


SAR-TDC ADC

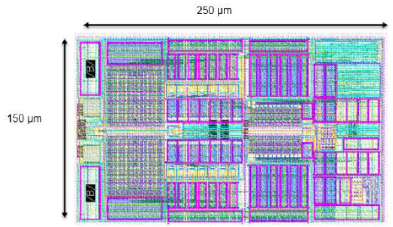
Architecture of 12-bit ADC :
Differential split switching (fast dynamic comparator settling time)
Asynchronous logic — no clock tree (low power)

CEA-IRFU 12b TDC assisted SAR ADC





ADC core layout :

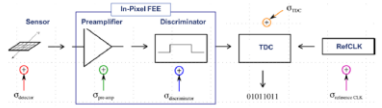


Performance summary	
Technology	CMOS 65 nm
Resolution	12 bits
Input range	1.9 Vpp.diff
Fs	50 MS/s (up to 70)
Power	0.95 mW
ENOB	9.8 bits
Area	0.037 mm²

FCCee trk & PID
≲ 10 µm
≃ 15
low*
≲ 100 ps
no
tbd
low
low

- Fine timing is needed for FCC-ee tracking and PID, as well as for Belle II and the LHCb UT, with a requirement of about 1 ns.
- In our proposal, we introduce an architecture designed to fully exploit the timing information provided by each pixel within the MANTA matrix.
- To achieve this, we propose integrating a **Time-to-Digital Converter (TDC)** at the **column level.**

- The technology is a good candidate to achieve both spatial and time precision
- The main challenge is to find an acceptable compromise between :
  - tolerable power consumption (tbd),
  - timing precision of the whole chain including : Sensor, Front End & Discriminator, column logic and TDC at the bottom of column (RefCLK also),
  - and affordable area.



TDC concepts/candidates
- TDC developed by SLAC : Vernier Delay Line (see Ariel Gustavo Schwartzman & Bojan Markovic 7.3a)
- Possible variants of TDCs developed by IP2I
  - Vernier Ring Oscillator with a Single Phase Detector
  - Vernier R.O with a Multi-Phase Detector
  - TDL (Tapped Delay Line) TDC

Submission of IP blocks in TPSCo65nm
- MPR2, possibly ER3

IP2I plans for TDC in TPSCo 65 nm (part of MANTA project)

- The target of our contribution to **DRD7-3** is to provide a **TDC with a time resolution of ≲ 20 ps RMS**
  - Not a stringent constraint to achieve a global timing resolution of **≲100 ps.**
  - The **20 ps** resolution could be further improved depending on the sensor, FE, digital architecture, and clock precision).

Lots of activities, joint ASIC designs …

DRD 7 : WP4 → Extreme environnements & longevity

Modelisation & developments of CMOS PDKs & IPs for cryogeny

Project Name	Device modelling and Development of Cryogenic CMOS PDKs and IP (WP7.4a)
Project Description	Device modelling from selected CMOS technology nodes, development of "cold" Process Design Kits (PDKs), design and characterisation of mixed-signal CMOS IP blocks and demonstrator chips for photon detection in (LAr, LXe) noble liquid experiments, quantum computing interface and sensing.
Innovative/strategic vision	The aggregation of the international research teams will create the critical mass needed for the construction of infrastructures and tools, needed for device characterisation and modelling , towards the development of cold PDKs and cold-IP blocks. These will be made available to a wider community working towards the construction of frontier particle and photon cryogenic detectors.
Performance Target	cold PDK for a deep sub-micron CMOS technology, with temperature corners at 165-87-77-4K, cold IP blocks demonstrated on board of a multi-channel mixed-mode demonstrator chip.
Milestones and Deliverables	**D7.4a.1** (M9) Deliever a specification and requirements document for a full-chip demonstrator. **M7.4a.2** (M18) Cold-PDK for TSMC28nm complete **M7.4a.3** (M26) Tapeout of full-demonstrator chip **D7.4a.4** (M38) Deliver a report of full-demonstrator silicon chip characterisation.
Multi-disciplinary, cross-WP content	The availability of reliable device models and PDKs for advanced CMOS technology nodes, qualified for operation at cryogenic temperatures, will pave the way for the development of cryo-qualified CMOS IP blocks suitable for integration on complex mixed-signal ASICs for DRD2 and DRD5.
Contributors	Graz University of Technology (Austria) University of Sherbrooke (Canada) Forschungszentrum Jülich (Germany) INFN (Italy) KEK (Japan) ICCUB, University of Barcelona (Spain) EPFL (Switzerland) RHUL (UK) University of Oxford (UK) Fermilab (US)

Radiation hardness of advanced CMOS processes

Project Name	Radiation Resistance of Advanced CMOS Nodes (WP7.4b)
Project Description	This project aims to evaluate the radiation response (total ionizing dose TID, single event effects SEE, and displacement damage DD) of commercial CMOS technologies more advanced than the 65nm node for use in the next generations of ASICs for particle detectors. Duration 4-5 years.
Innovative/strategic vision	Understanding the effects of radiation on CMOS technologies is essential for the design of ASICs used in particle detectors. This project represents a first and crucial step in evaluating the performance of advanced CMOS nodes for the unique environment of particle detectors.
Performance Target	Deepen the knowledge of the radiation response of 40nm and 28nm technologies and begin to study finFETs technologies.
Milestones and Deliverables	**D7.4b.1** (M12) Deliver a 28nm CMOS front-end (FE) circuits for pixel sensors prototype; TID test of IP-blocks in 28nm node **D7.4b.2** (M18) Deliver a chip in 28nm CMOS including matrices of FE channels for readout of pixel sensors **M7.4b.3** (M24) Radiation test of FE structures; Design and testing of rad-hard memory elements in 28nm node **D7.4b.4** (M36) Deliver a prototype in FinFET technology including IP blocks for pixel readout circuits.
Multi-disciplinary, cross-WP content	In order to ensure the success of projects involving ASIC design for particle detectors, it is imperative to consider the radiation resistance of the technologies used. On the other hand, the definition of radiation qualification would greatly benefit from the input of the designer. For example, ASICs developed in WP7.3a must be radiation tolerant and could also serve as valuable test vehicles to evaluate radiation effects.
Contributors	CERN AT: TU Graz IT: INFN Pavia, Uni. Bergamo, Uni. Padova, Uni. Pavia FR: CPPM

Cooling

Project Name	Cooling and cooling plates (WP7.4c)
Project Description	Development of the general purpose next generation of microchannels cooling structures to deliver excellent cooling performance, minimal material budget, and better electronics integration. Duration about 2+ years.
Innovative/strategic vision	Better integration of electronics features to the cooling plates especially in dense electronics applications. Better scalability considering alternative manufacturing techniques (more cost-effective). Thermal performance numerical simulation tools for new applications.
Performance Target	Different topics will explore different … s of the following parameters: … W/cm^2), material … /or cost. Different expe… … from the portfolio created and optim… …ions for their final application. The progress will be tracked via public reports in the form of presentations, public notes and/or papers.
Milestones and Deliverables	**D7.4c.3** (M15) Deliver a feasibility public note or paper (topic 3) **M7.4c.6** (M24) 3D printing public note or paper (topic 4) **D7.4c.5** (M27) Deliver a report summarising fluidic and thermal tests of demonstrators public note or paper (topic 1) **M7.4c.7** (M36) Bi-phase CO2 Thermo-fluidic models developed for microchannel, nuclear and annular flows, and thermal heat exchanger characterization and interconnection (topic 2).
Multi-disciplinary, cross-WP content	Communication with DRD8 (Mechanics) and DRD3 (Semiconductor detectors) via liaisons and workshops (e. g.: Forum on tracking mechanics) and 7.6b project (common access 3D and advanced integration) within the DRD7.
Contributors	CA: Sherbrooke CERN DE: DESY ES: IMB-CNM, IFIC-Valencia UK: Manchester FR: CPPM, LAPP, LEGI, LPNHE, LPSC

… moving to DRD8

DRD 7 : WP4b → Radiation Hardness

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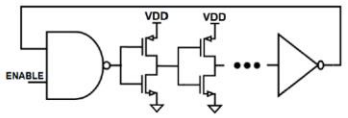
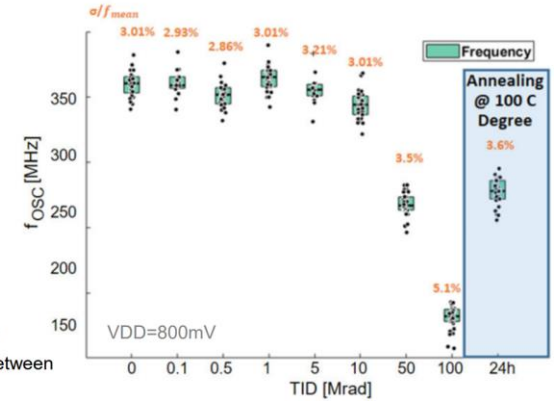
Very active domain, some studies on 40 nm but main focus on 28 nm technology

(A) Variability effects in scaled CMOS



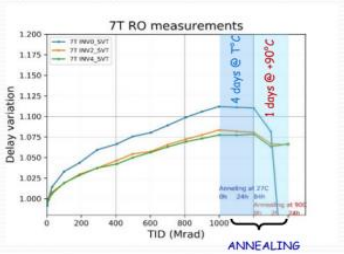
An array of 23 stages ring oscillators
P-channel 240nm / 40nm
N-channel 120nm / 40nm

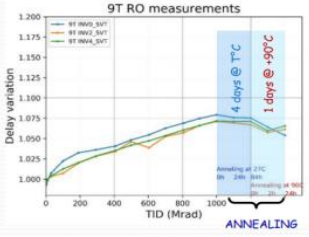


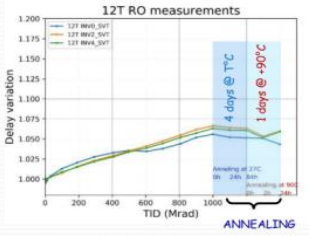
- Variability at the level of 3%
- Increasing around the rebound
- Variability anneals together with VTH recovery
- Observed differences variability after anneal between different VDD levels

Ring-Oscillator studies on 40 nm technology

TID test results







TID measurements have been done in close collaboration with Alicja from Graz institute - Austria

- X-ray source for 1 week to reach 1 Grad
- Annealing:
  - Several days @room T°C
  - At high temperature +90°C

Results show very good dose tolerance even at ambient temperature

- Better tolerance than 65nm or 130nm

TID tests at room temperature show a delay increase of less than 15% up to 1 Grad

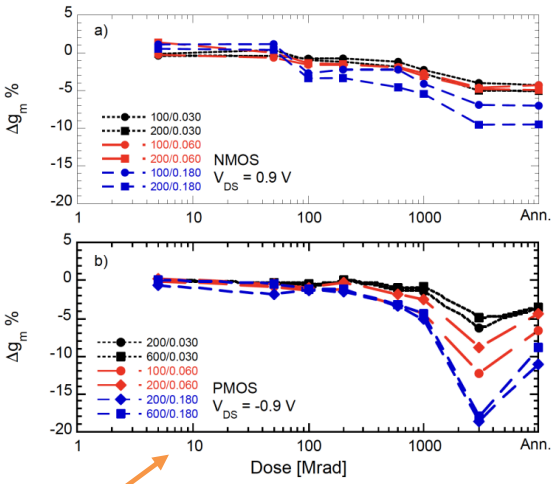
- Max delay increase of ~15 % measured on 7T-NOR0 cells (min strength drive)

12T and 9T more tolerant than 7T

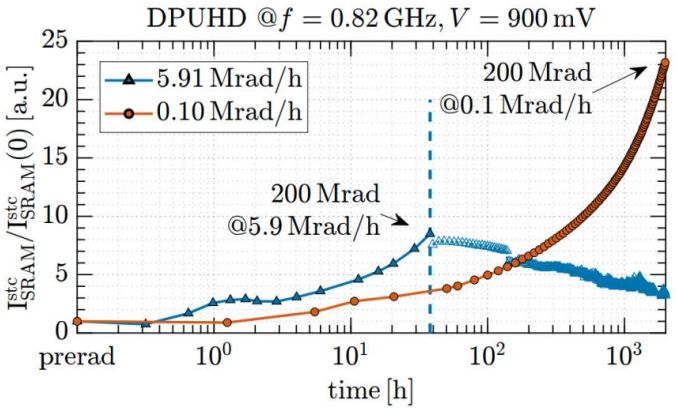
INV2 and INV4 have similar variation → same size for transistors are used

Results are in line with CERN results

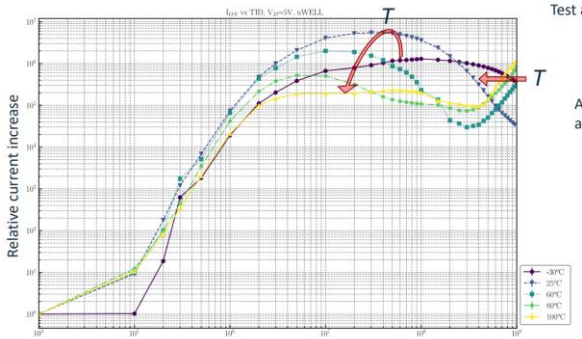
28 nm ring oscillator studies (HDR): max 15% increase at 1 GRad



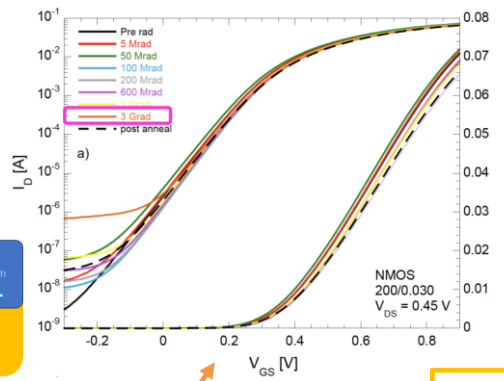
Transconductance vs. Dose: short channel more resistant! (Pavia)



28 nm : dose rate effect (CERN)



TID-induced leakage in pn junctions seen in 28nm DC-DC conv (CERN)



Id vs Vgs to 3 Grad (Pavia)

Practical question: methodology at ultra high dose?

G. Traversi et al., **Ionizing Radiation Effects of 3 Grad TID on Analog and Noise Performance of 28nm CMOS Technology**, IEEE Transactions on Nuclear Science, 10.1109/TNS.2025.3542230

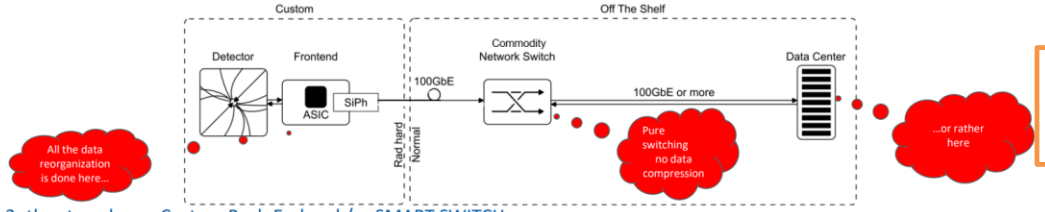
DRD 7 : WP5 → Back End systems & COTS

F.Alessio©!
https://indico.cern.ch/event/1556239/

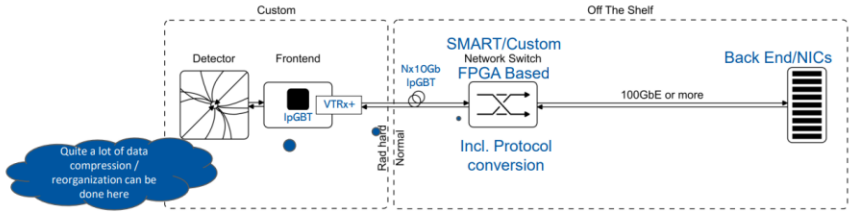
- WP 7.5a → common TDAQ developments with COTS
  - Main focus on triggering with various hardware platforms (FPGA, CPU, GPU…)
  - Sharing technological knowledge : soft/firmware framework , hardware devices, open-access git repository…
- WP 7.5b → Front-End to Back-End with 100 GbE

Two approaches:
1- the radical one: NO BACKEND

S.Baron, DRD7 workshop III

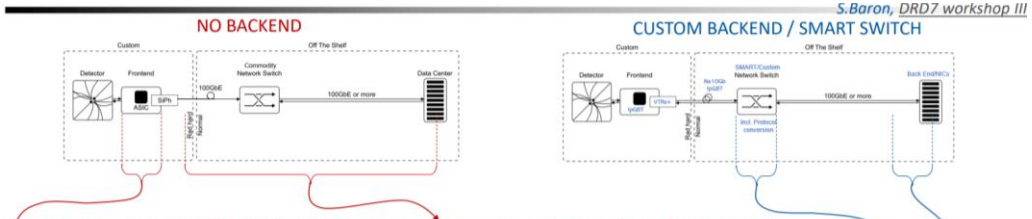


2- the staged one: Custom Back-End and /or SMART SWITCH



CPPM uses existing BE board solution adaptation → uses PCIe400 with 100 GbE links.

S.Baron, DRD7 workshop III



Theme 1 : using 100GbE COTS switches to handle data-streams from the Front-End to Network Interface Cards (NICs) or even DAQ processors (CERN LBC and ESE groups).

Theme 2: design of a COTS-based high-density switch bridging the detector environment to the COTS/DAQ world (Imperial College).

Theme 3 : to explore DAQ topologies (based on custom boards for DAQ, concentration and processing) (CPPM CNRS/IN2P3, Nikhef, Brookhaven National Lab)

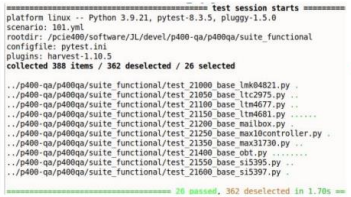
Theme 4 : study and design of the building blocks IPs necessary for 100Gb Ethernet cores implementation in future FE ASICs. (Rutherford Lab)

Theme 3

Develop «classical» approach with Back-End custom FPGA-based card (Intel version) – PCIe400

Two prototype boards received in December 2024

- 23 power rails satisfy DC level and ripple noise requirements
- Power supply sequence to power-up FPGA is OK
- Both FPGA programming paths, from JTAG and flash memory, are validated
- Low level control of board : over-heat protection, FPGA power cycle, reconfiguration is OK
- Access and configuration of all external peripherals has been validated
- PCIe interface slow control works on a PCIe Gen 3 server



A functional test suite performing over 400 measures using pytest developed and running

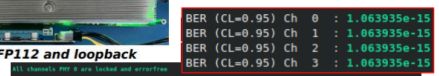
Progress Report – BackEnd FPGA-based

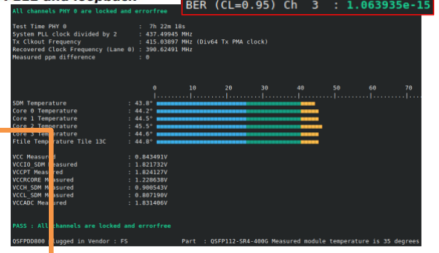
Theme 3

Agilex 7 F-tile transceiver has FHT interface with up to 116 Gbits/s PAM 4 links + 400GbE Hard IP provides physical and data link layer (PHY, MAC, FEC)

- Challenging implementation between the FPGA and a QSFP112 cage over ~50 mm
- Using Altera's PHY FEC RS(544,514) PRBS-31 external loopback
- Error free post FEC during 7h BER of < 1e-15 with pre-corrected FEC BER < 2e-10
- Opens the possibility to integrate a Network interface within the readout board Interface with a switch using 400GbE UDP

PCIe400 with QSFP112 and loopback





400G links post FEC BER

Next steps

- PCIe interface slow control and DMA access on Gen 4 and Gen 5 server
- Performance of the cooling solution
- Power supply ripple and transient noise at high FPGA logic occupation
- Front-end serial links at 10 and 25 Gbits/s
- Serial links at 100 Gbits/s
- Performance of the phase determinism of the Agilex 7 (synergies with DRD7.3)

FPGA Milestones

- December 2026 : Report on performance of lpGBT and phase determinism on PCIe400 prototypes
- July 2028 : Delivery of a ~100 PCIe400 cards

DRD 7 : WP6a → Access to selected imaging technologies

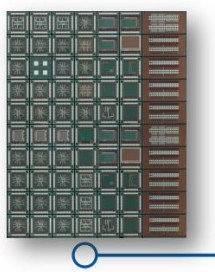
DRD 7.6a Goals:

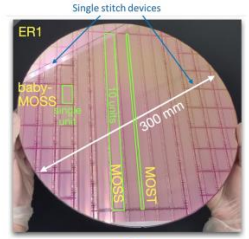
Provide framework to facilitate access to complex imaging technologies/ modified process through standard MPWs

- Support access to monolithic CMOS technologies
  - TPSCo 65 / TJ 180 → Single pt of interface to foundries
  - PDK support, design flow…
  - MPW / ER organization
  - Thinning & cutting
- Support IP development:
  - Many IPs available or in development…
- Implication of French community mainly on 2 technologies:
  - TJ 180nm, TPSco 65nm

Access through IPHC

IP dvps + link to DRD3 projects





W.Snoeys©!
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MPR2
Shared engineering run

WP 1.2 "rail"

ALICE "rail"

MLR1 (Multy-Layer Reticle, Dec 2020):

Learn about the technology, characterize pixels, transistors and building blocks

1.5 x 1.5 mm² test chips

>50 chiplets from: DESY, IPHC, RAL, NIKHEF, CPPM, Yonsei, CERN

ER1 (Engineering Run, Dec. 2022):

Prove we can design wafer-scale stitched sensors

MOSS (1.4 x 25.9 cm)

MOST (0.25 x 25.9 cm)

Hybrid-To-Monolithic (H2M)

51 chiplets from: DESY, IPHC, RAL, NIKHEF, SLAC, INFN, CERN

ER2 (August 2025):

Full-scale stitched sensor prototype for ALICE ITS3

MOSAIX (1.9 x 26.6 cm)

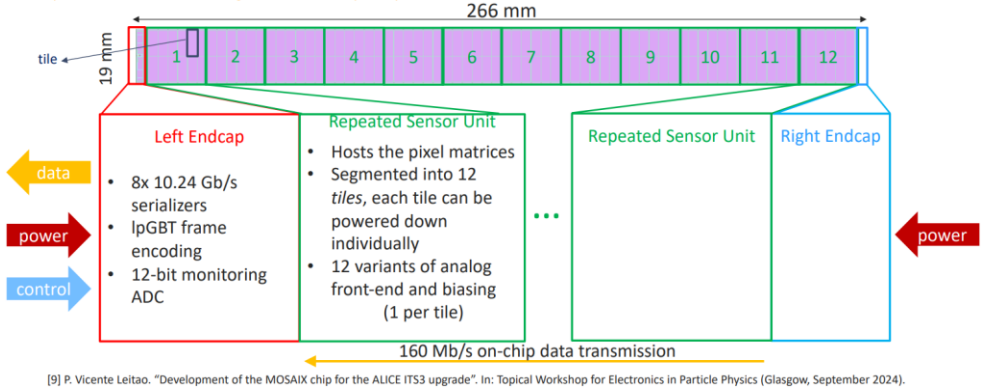
~30 chiplets from: IPHC, SLAC, CPPM, BNL, INFN, Universität Heidelberg, CERN

ER3 (2026):

Stitched sensor production for ITS3 (ALICE-specific)

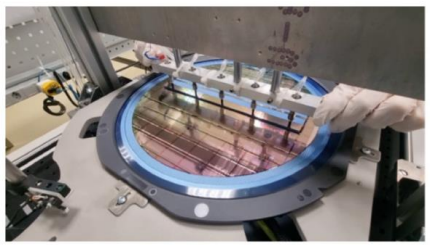
MOSAIX is the full-size, full-functionality, stitched sensor prototype for ALICE ITS3. 22.8 x 20.8 µm pixels, 9.97 Mpixels. MOSAIX inherits some of its features from MOSS (synchronous read-out, conservative layout) and MOST (power segmentation, data transmission on chip), but it includes many more complex functionalities. Attention to YIELD

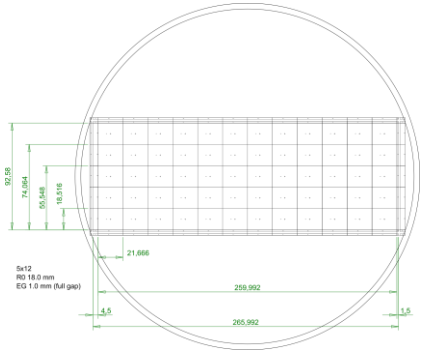
Unprecedented level of integration and complexity in HEP

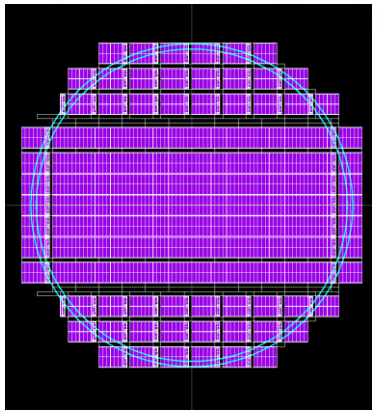


[9] P. Vicente Leitao. "Development of the MOSAIX chip for the ALICE ITS3 upgrade". In: Topical Workshop for Electronics in Particle Physics (Glasgow, September 2024).

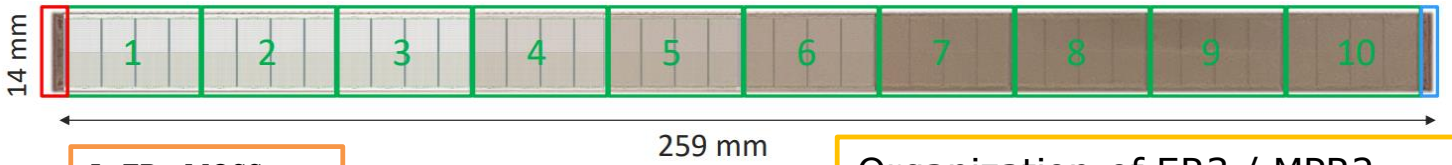
In ER2: MOSAIX stitched sensor for ALICE ITS3







In ER3 ALICE-driven, of order 6-7 chiplets 1.5 mm² available to community



In ER1: MOSS

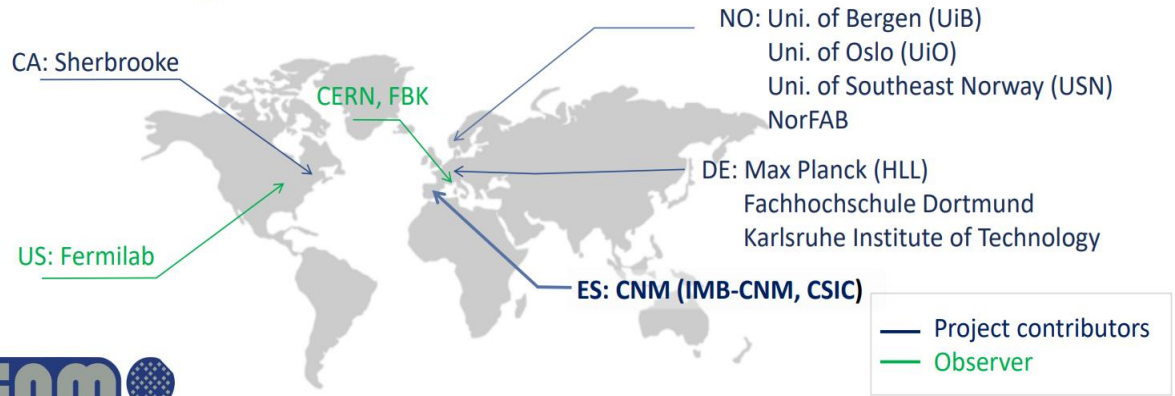
Organization of ER3 / MPR2 timing / process to access IPs in discussion with users.

DRD 7 : WP6b → Shared access to 3D integration

M.Caselle©!
https://indico.cern.ch/event/1556239/

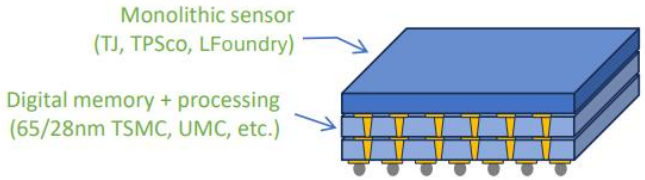
DRD 7.6b Goals:
Shared access to 3D integration.
- 2.5D chiplet architectures and 3D W2W
- Key enablers for future detectors

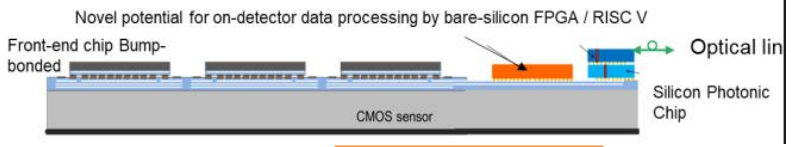
Collaboration Update



Centro Nacional de Microelectrónica IMB

3D integration



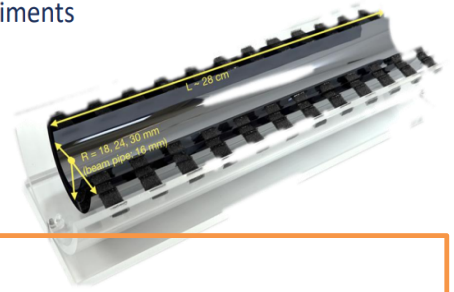


Silicon interposer

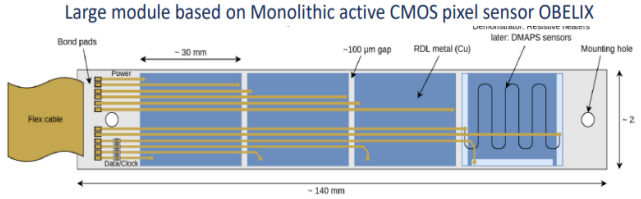
Community is developing and ambitious projects start to shape in DRD7.6b!

Detector packaging technologies for large-area detector modules

- Advanced packaging is vital to achieve ultra-low mass, precise assembly, and robust high-speed power/data links required for large-area detectors in future experiments
  - **From DRD 7.6a**: Fabrication of wafer-level dummy interposer structures, emulating state-of-the-art monolithic pixelated detectors
  - Featuring only the top metal layer, enabling interconnection testing, including of SiPh chip Integration



Large module based on Monolithic active CMOS pixel sensor OBELIX

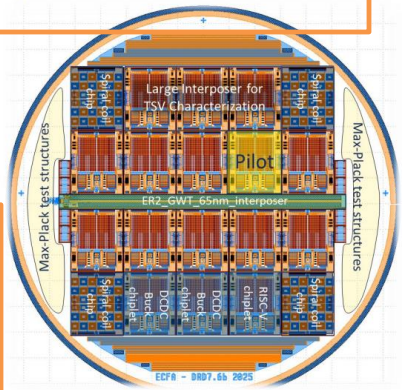


- All-Silicon Ladder Concept: Single silicon piece with 4 sensors cut from one wafer
- Post-Processing: Addition of redistribution metal layers for data and power

Pilot Project to validate and implement distributed workflow (ECFA-DRD7.6b-2025)

The Pilot Project is a full-wafer engineering run, entirely developed and fabricated in-house by DRD 7.6b contributors

- **Key Features**:
  - Simple enough to efficiently validate the distributed workflow
  - Sufficiently complex to assess chiplet integration, providing insights toward the development of TSVs and RDL capabilities
- **Approach**:
  - Design test structures suitable for multi-site fabrication
  - Coordinate process steps across institutes, including TSV formation, RDL fabrication, and interposer assembly
  - Collect performance and yield data to refine distributed production protocols



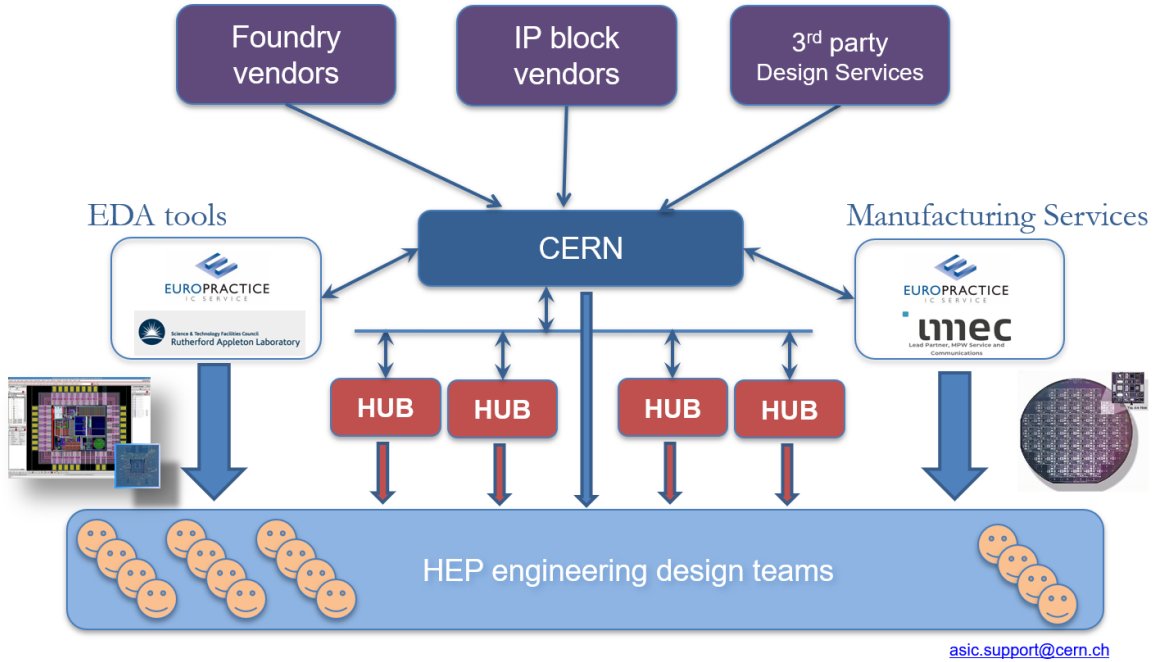
6-inch wafer size

DRD 7 : WP7 → Hub-based support

K.Kloukinas©!
https://indico.cern.ch/event/1556239/

In response to the DRD7 projects and in order to manage ASIC-related design risks in our distributed community, the Steering Committee invites Conveners of WG7.7 to create and steer a **task force** that will propose **an implementation solution for a hub-based structure for ASICs developments**

- WG7.7 Conveners
  - Xavi Llopart (CERN)
  - Mark Willoughby (STFC, UK)
  - Kostas Kloukinas (CERN)
- WG7.7 Task Force members by Geographical Location
  - Mark Prydderch, UKRI STFC, RAL, UK
  - Frederic Morel, CNRS/CEA, IPHC Strasburg site, FR
  - Gianni Mazza, INFN (Torino), IT
  - Ruud Kluit & Arseniy Vitkovskiy, NIKEF, NL
  - David Gascon, University of Barcelona, ES



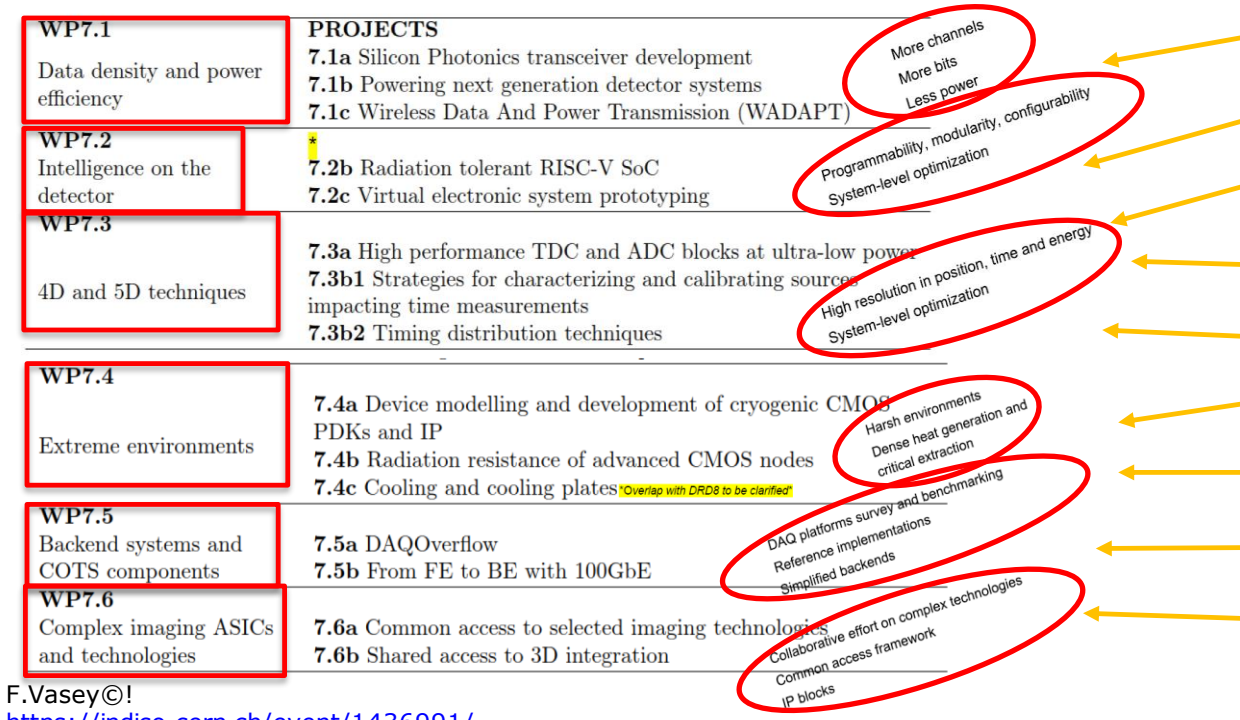
- Regional HUB operations:
  - **ASIC Design** service
  - **ASIC Verification** service
  - **Foundry Design Kit** support (PDKs, IP blocks, Design Methodologies)
  - **Foundry access** services (legal frameworks, commercial contracts)
  - **Administrative, financial and logistics** services

- Flexible and scalable model
  - HUBs to be classified by the number of services they offer (Tiered Model)
    - Design services
    - Verification services
    - Foundry Design Kit support and IP block sharing services
    - Foundry access services
  - HUBs can scale up the type of services they offer as necessary
  - Sharing of engineering resources between design projects and services
- Funding
  - Advocate to funding agencies on the critical importance of such infrastructure
  - Introducing a *levy system* where a portion of each project's budget contributes to funding the shared services
  - A mix of both funding models

Kostas Kloukinas (CERN)
Xavi Llopart (CERN)
Mark Willoughby (STFC, UK)

Conclusion

Good participation of IN2P3 teams in particular in this DRD with relatively transverse vocation, sign of the dynamism of our community!



WADAPT : **LPSC**

Virtual Electronic System Prototyping: **IPHC**

Co-conv: LPNHE

TDC/ADC: **CPPM / IP2I / Omega**

Time measurement: **LPCA**

Co-conv: LPCA

Timing distribution techniques.: **CPPM /IJClab**

Radiation resistance: **CPPM**

Cooling: **CPPM / LAPP / LPNHE / LPSC**

100 GbE: **CPPM**

Imaging technologies: **APC / CPPM / IP2I / IPHC / LPNHE**

Co-conv: CPPM

F.Vasey©!
https://indico.cern.ch/event/1436991/

DRD7 steering committee: J. Baudot

DRDC: L. Serin, D. Contardo

Many of these topics directly impacting / in line with FCC detector R&D