CMOS and Timing (LFoundry LF15A, 150 nm)

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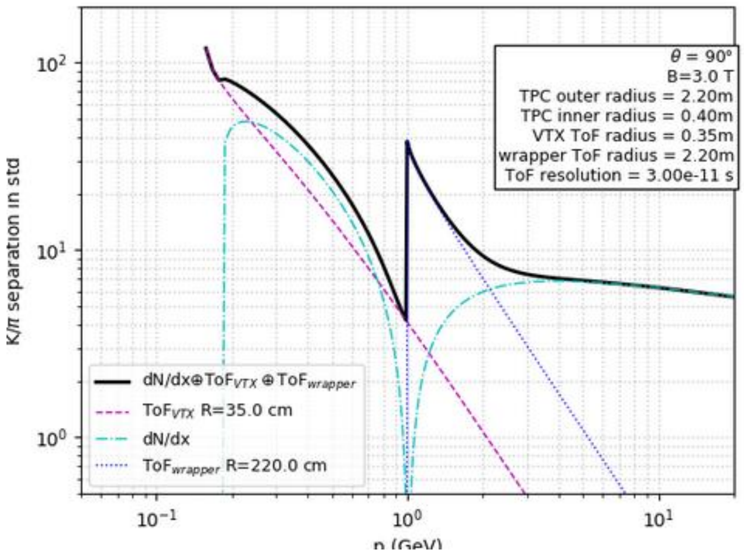
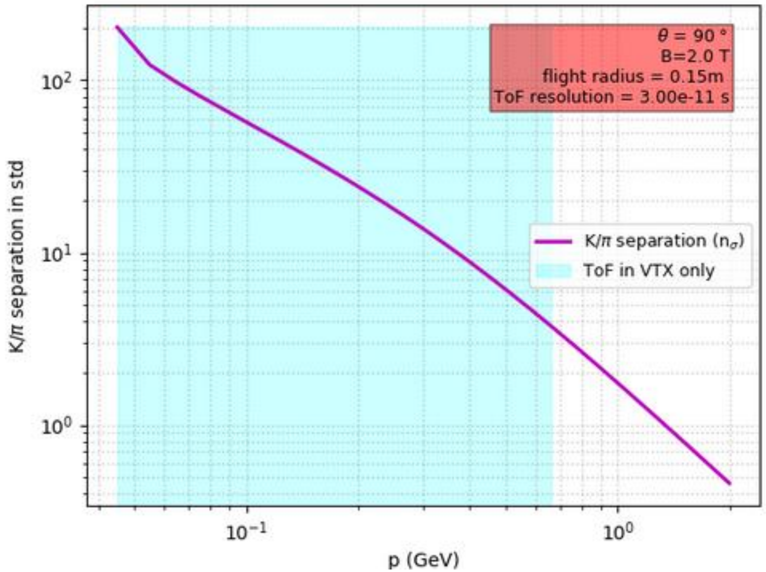
Motivations for a TOF detector



Improve π/K separation at low momentum
TOF wrapper radius 2.2 m



TOF wrapper could be complemented
by timing layer (radius 15 cm) for
0.045<p<0.66 GeV/C (not reaching the 2.2 m wrapper)

Physics cases :
H→fermions
Flavour physics
Heavy Neutral Leptons

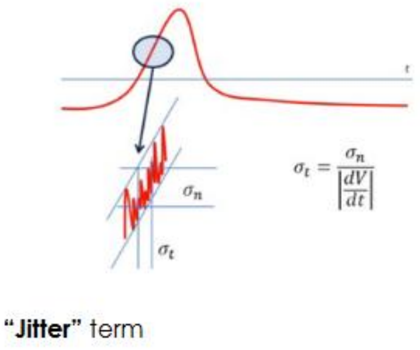
Expression of Interest
Toward MCMOS Time of Flight Tracking
Layers for a detector at FCC-ee, IP2I and Irfu

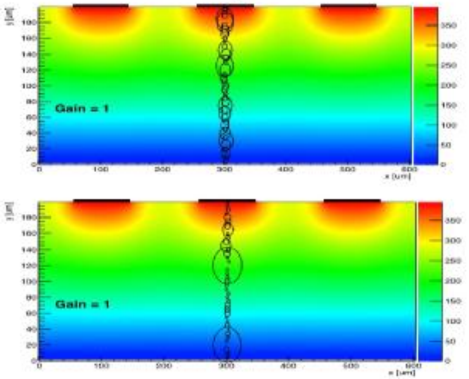
Features of monolithic CMOS sensors

- (Relatively) cheap high volume industrial technology
  - 2-3 k euro/8'' wafer, post-processing and dicing included → bare sensor cost for 100 m2 : 7-11 M euros
  - Bump bonding operation not needed for fully monolithic architecture
- Stable and easy operation
- HV-HR wafers available, allows charge collection by drift and not only by diffusion → favorable for fast collection and also for radiation hardness
- Can be designed as a complete SoC, from sensor to DAQ interface
- Presently available technologies are known to be rad-hard up to a few 10^{15} 1 MeV neq/cm
- Can be thinned down to < 100 µ

Time resolution ingredients

$$\sigma_t^2 = \left(\frac{Noise}{dV/dt}\right)^2 + (\Delta ionization)^2 + (\Delta shape)^2$$





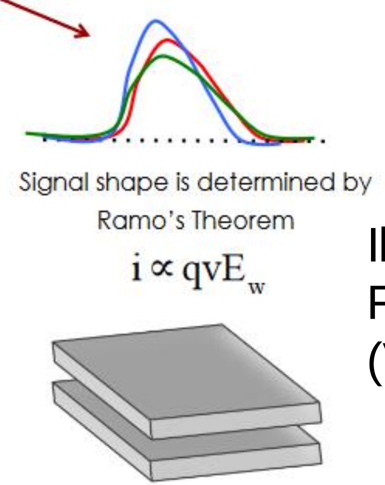


Illustration taken From N. Cartiglia (VCI 2022)

Small noise → choice of technology, small detector capacitance
High dv/dt →
High electric field (but Vd saturates around 1 V/µm)
Intrinsic amplification ?

Amplitude variation → Timewalk, corrected offline

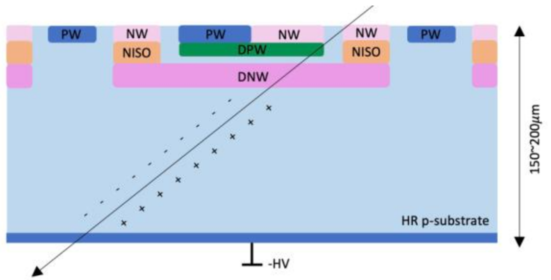
Non-homogeneous energy deposition → cannot be corrected, minimized by design (thin sensor)

Saturated drift velocity in sensor volume → Uniform weighting field

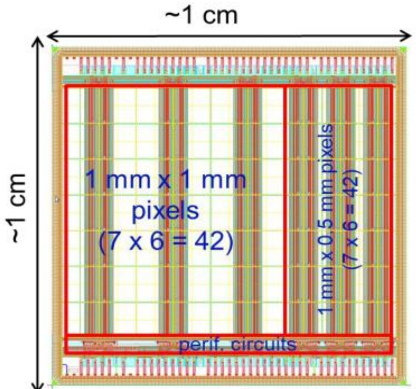
Parallel plate geometry, easier for big pixels → Large electrode designs

CACTUS sensor development line

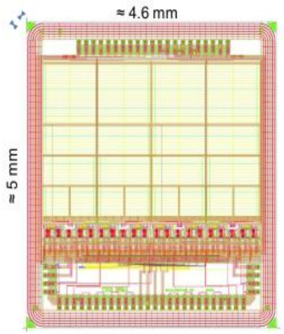
- Monolithic timing using Lfoundry 150nm HV-CMOS
- Large fill factor



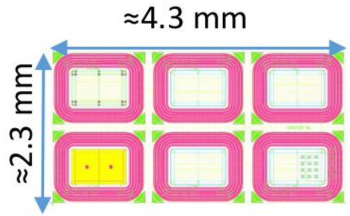
Cross section of the MiniCACTUS_v2



Layout of Cactus chip (~1cm x 1cm)



MiniCACTUS_v2
with gain
2025?



CACTUS Demonstrator 2017
- 500 ps resolution only (parasitic caps)
- high BV (>250 V)
- Good yield
- Good charge collection uniformiy

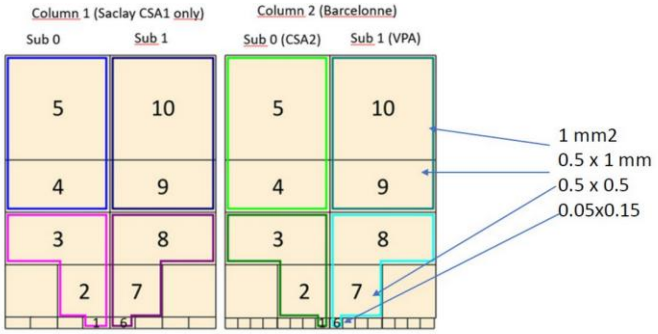
MiniCACTUS_v1, 2020
-65 ps time resolution
-Some digital/analog couplings

MiniCACTUS_v2 2023
-coupling problems solved
-new front-ends
-49 ps time resolution

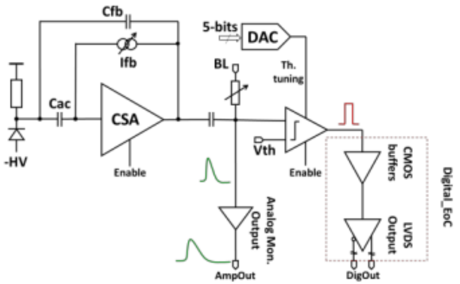
CACTUS-GL 2024

MiniCACTUS_v2

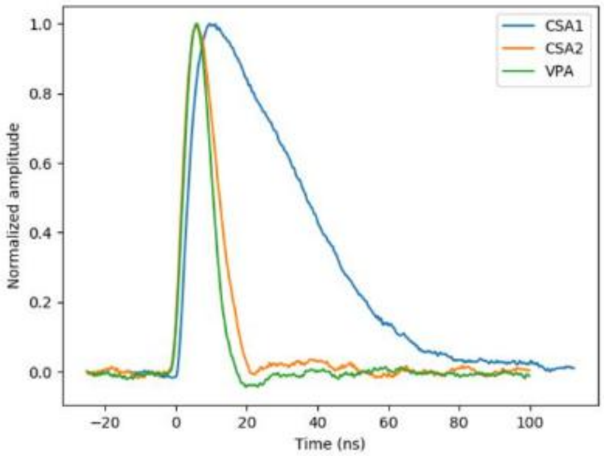
- Slow control, DACs and bias on-chip
- Pixel sizes: 1x1 mm^2, 1x0.5 mm^2, 0.5x0.5 mm^2
- Post-processed samples to 150, 175 and 200 µm
- CEA-IRFU and IFAE collaboration
- No gain on sensor
- Featuring three pre-amplifiers:
  - Two CSA and one VPA
  - Different return-to-baseline times (< 25 ns for CSA2 and VPA)



Pixels overview



Sensor FE architechture

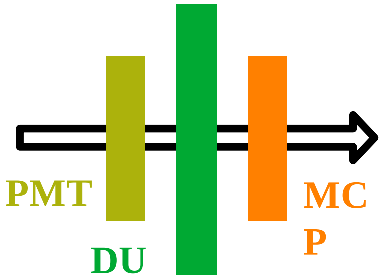


Return-to-baseline time

- Three testbeam campigns at CERN SPS:
  - July 2024 (parasitic DRD1, muons)
  - July 2025 (parasitic DRD1, muons + pions)
  - October 2025 (DRD3, pions)

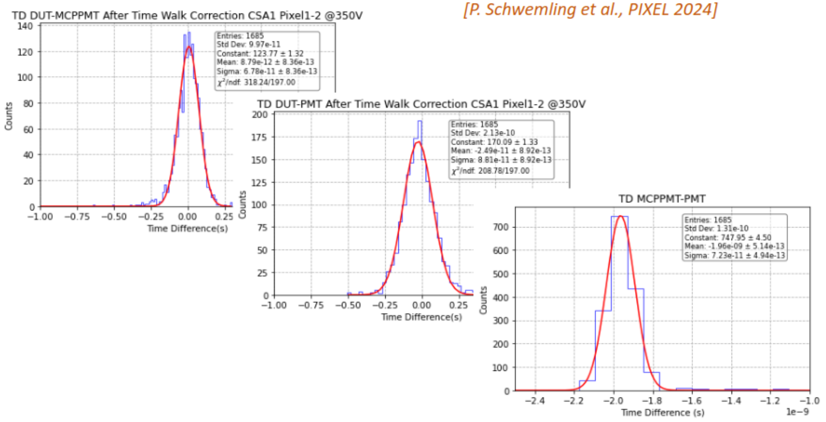
Testbeam July 2024

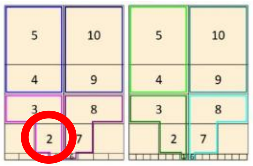
- First TB studying MiniCACTUS_v2
- 12 bit, 10 GS/s, 1 GHz bandwidth scope
- Issue with DUTs getting shorted on the sensor HV, causes understood later
- CERN SPS/H4 North Area with muons
- Best result of ~60 ps on 0.5x0.5 mm^2 pixel with 175 µm thickness @ 350V



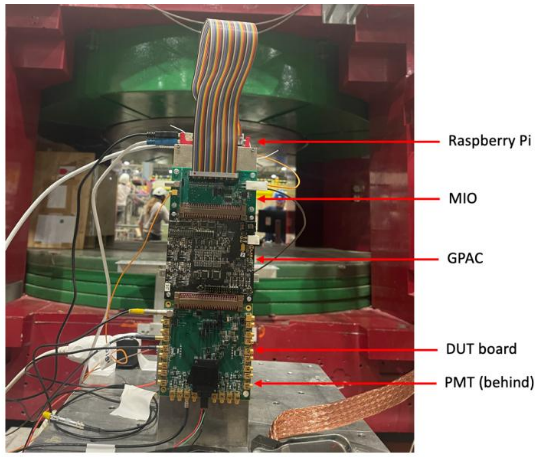
Detectors schematic

[P. Schwemling et al., PIXEL 2024]





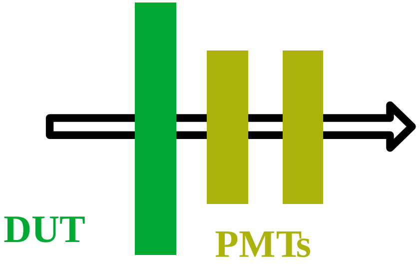
Sigma (DUT)	Sigma (PMT)	Sigma (MCP)
59.9 ps	64.4 ps	32.5 ps



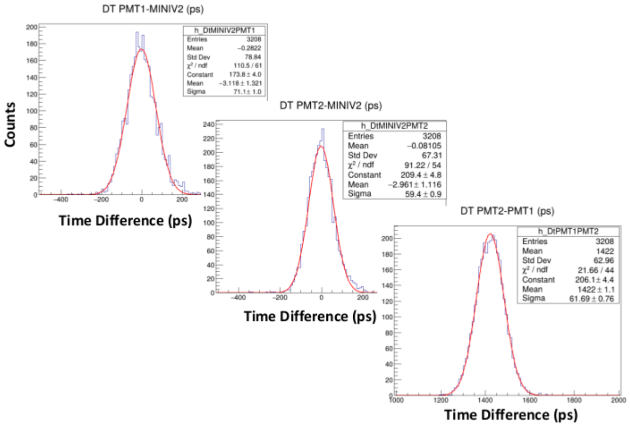
DUT setup

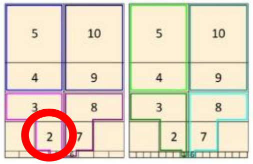
Testbeam July 2025

- 12 bit, 10 GS/s, 1 GHz bandwidth scope
- HV issue solved:
  - Increased HV lines isolation on PCB
  - Reducing amount of HV wire bonds over guard-rings
- CERN SPS/H4 North Area with muons and pions
- Best result of ~49 ps on 0.5x0.5 mm^2 pixel with 175 µm thickness @ 500V

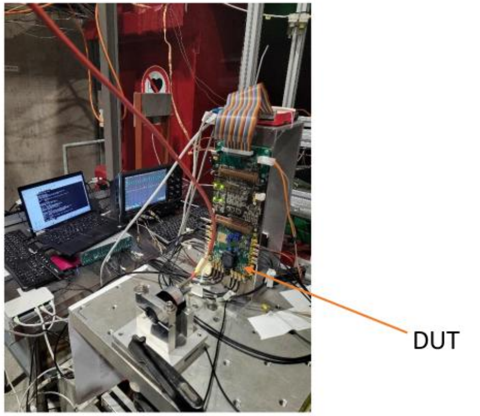


Detectors schematic





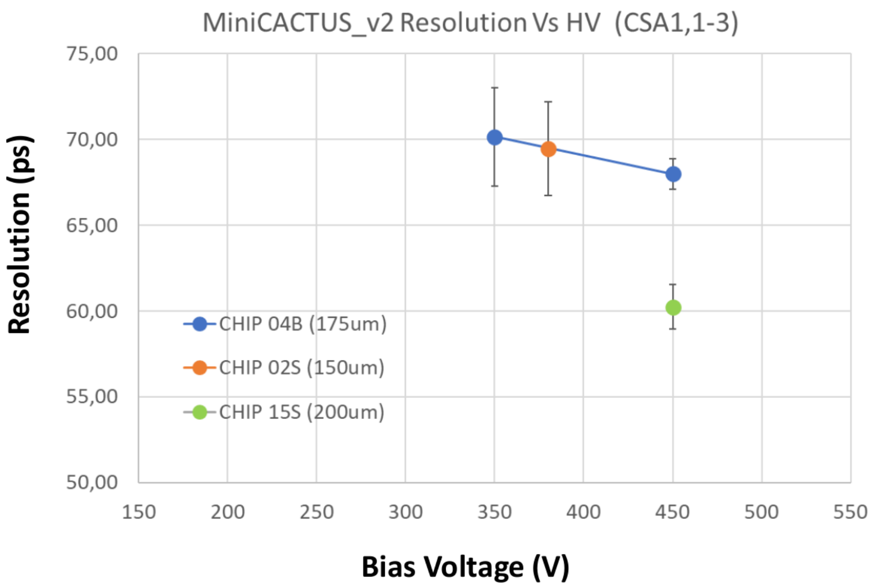
Sigma (DUT)	Sigma (PMT)	Sigma (MCP)
48.88 ps	51.64 ps	33.76 ps

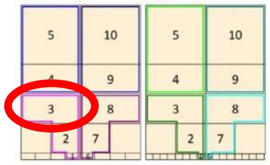


DUT setup

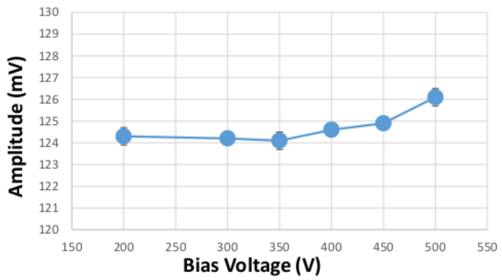
July 2025 – Timing on 1x0.5 mm² pixel

- Time resolution between 60 and 70 ps

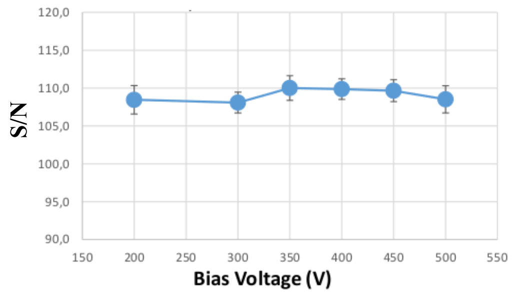




Sensor output amplitude MPV vs HV

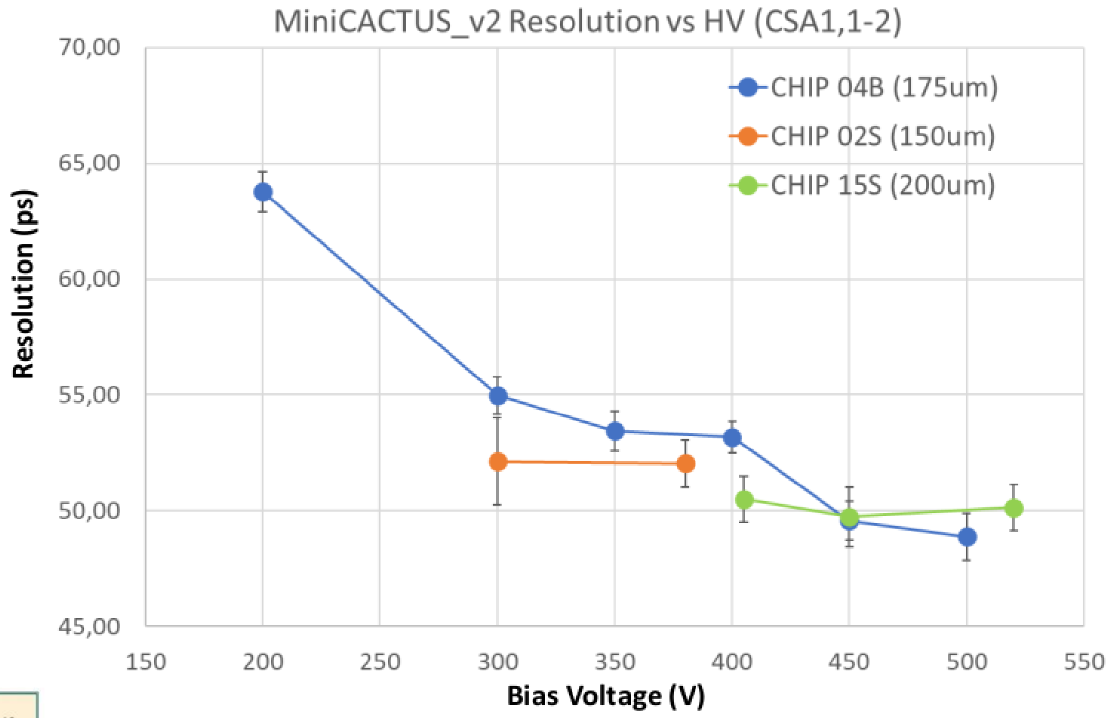


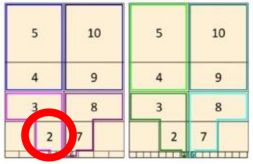
Sensor output Signal to Noise vs HV



July 2025 – Timing on 0.5x0.5 mm^2 pixel

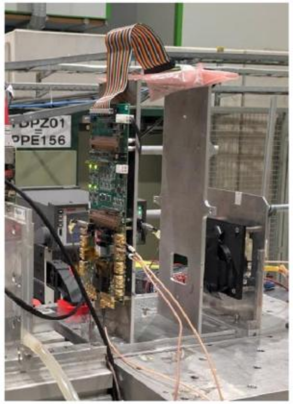
- Time resolution better than 55 ps above 300 V, down to 48.9 ps at 500 V



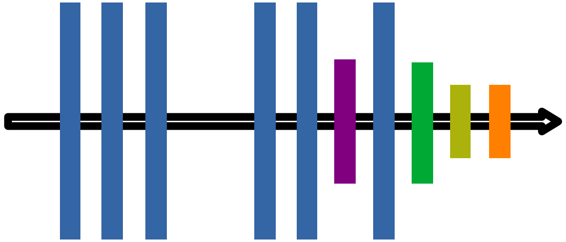


Testbeam October 2025 - DRD3

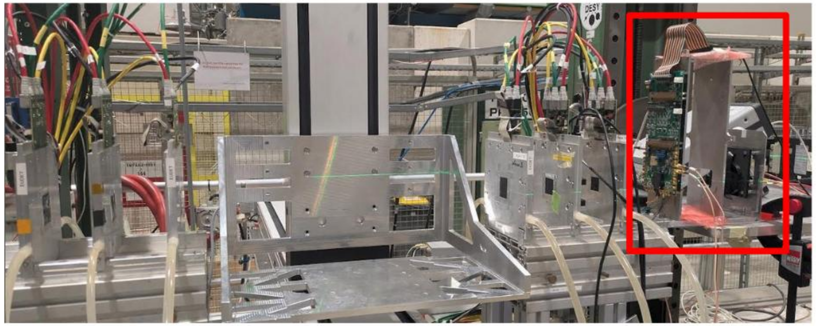
- 12 bit, 50 GS/s, 5 GHz bandwidth scope
- Using EUDAQ framework
  - Adapted producer from HGTD for the scope
  - Allowing to run Corryvreckan
- CERN SPS/H6 North Area with pions
- Detectors setup:
  - **EUDET Telescope**: tracking
  - **CROC**: For triggering ROI
  - **DUT**: MiniCactus_v2
  - **PMT**: Auxiliar timing reference
  - **MCP**: Timing reference



Zoom on DUT setup



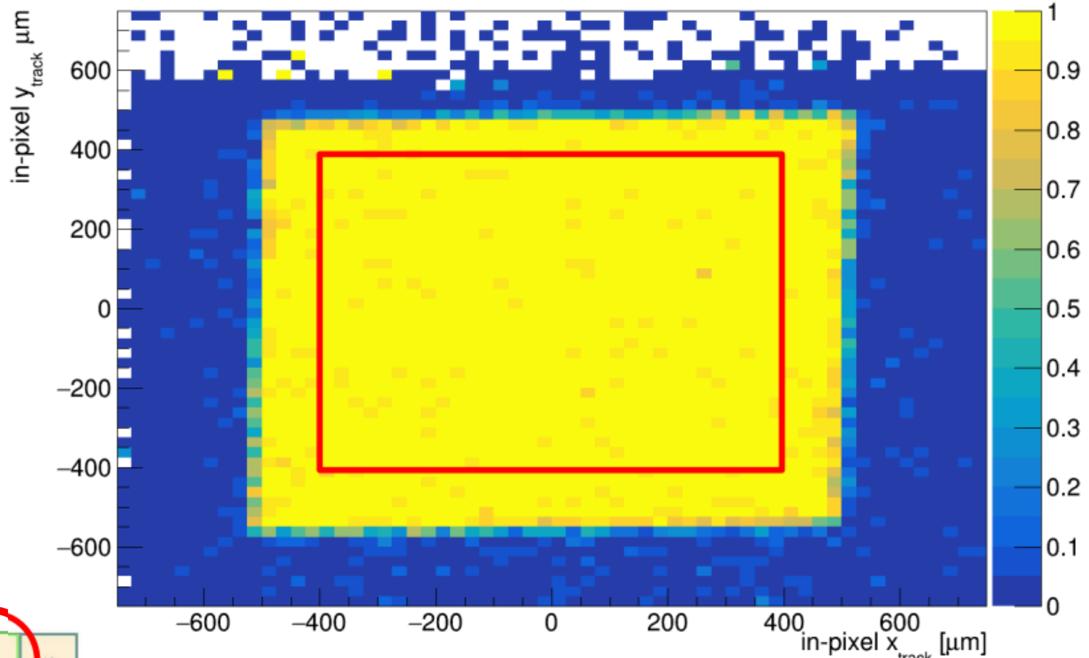
Detectors schematic

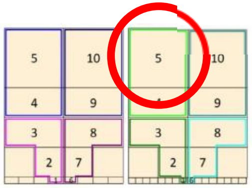


DUT setup

October 2025 – Tracking efficiency 1x1 mm^2

- Tracking efficiency of 99.0 ± 0.1 % on the central part on the pixel (in red, 0.8 x 0.8 mm) @350 V and 17 nA



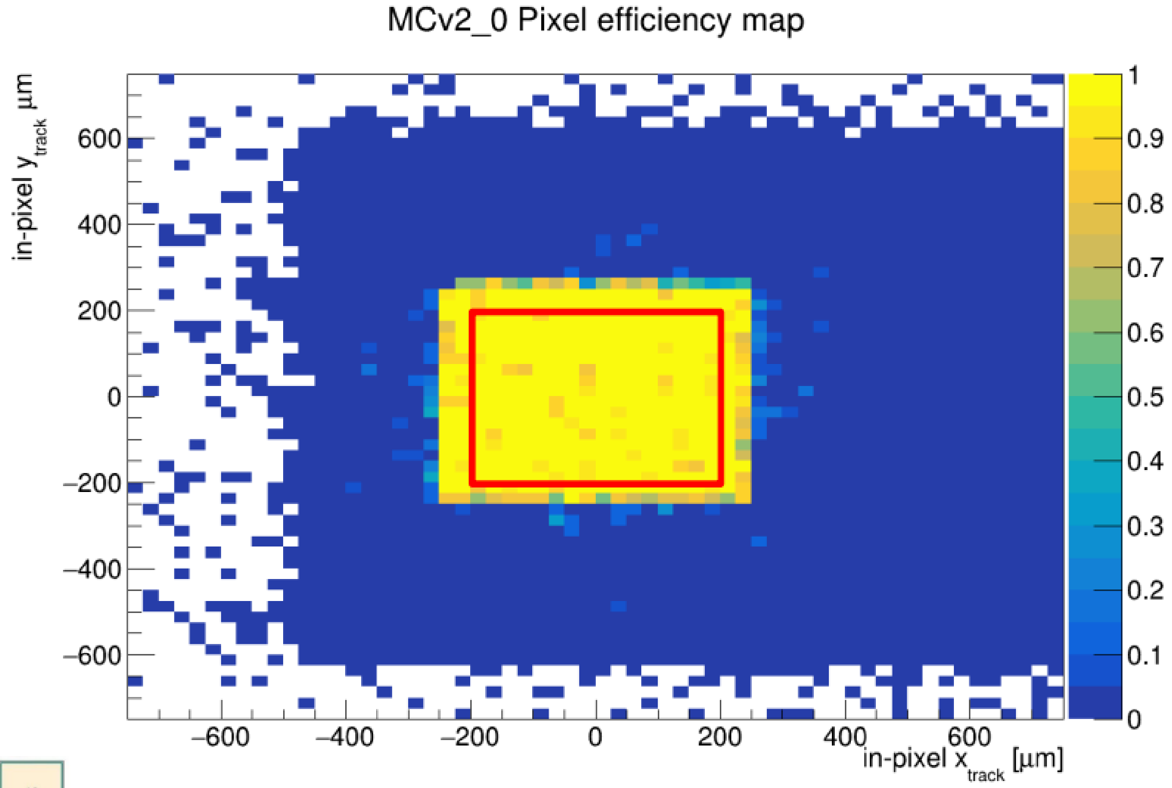


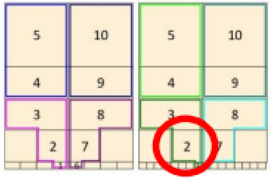
Efficiency defined as #tracks intercepting detector over detected tracks on single track events

Preliminary – Ongoing analysis

October 2025 – Tracking efficiency 0.5x0.5 mm^2

Tracking efficiency of 98.6 ± 0.3 % on the central part on the pixel (in red, 0.4x0.4mm^2) @400 V



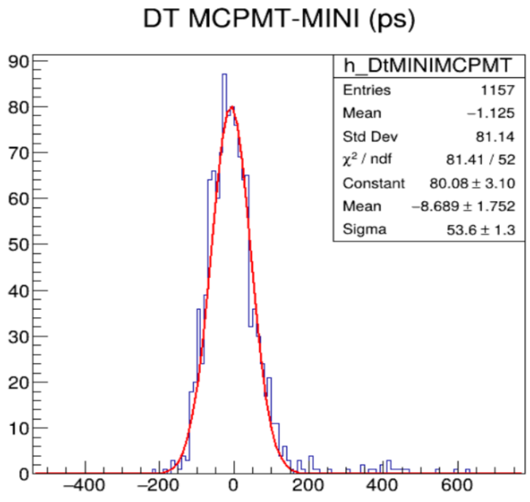


Efficiency calculated by tracks intercepting our detector over detected tracks on single track events

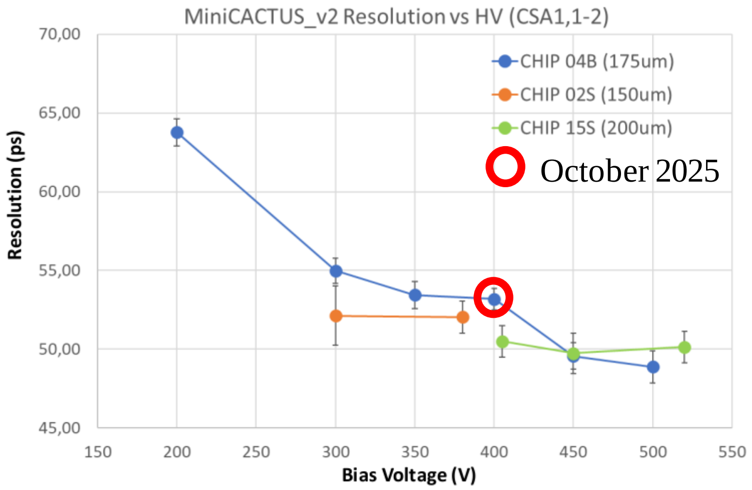
Preliminary – Ongoing analysis

October 2025 – Timing results

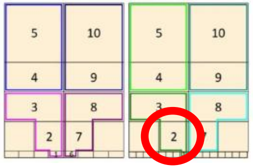
- Result of ~53.6 ps on 0.5x0.5 mm^2 pixel with 175 μm thickness @ 400V
- Compatible with previously (July 2025) obtained resolution on CSA 1 of 54 ps:



CSA2 0.5x0.5 mm^2 @400V



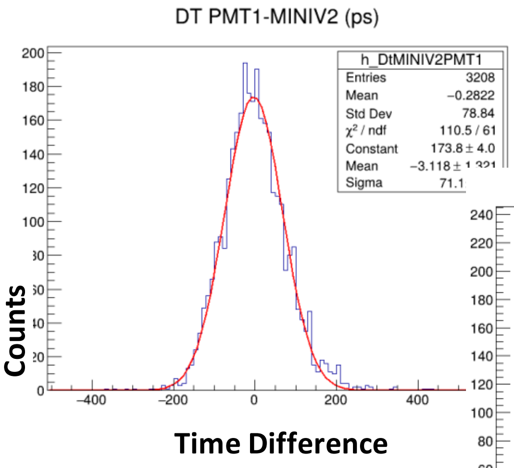
July 2025 Summary plot on 0.5x0.5 mm^2

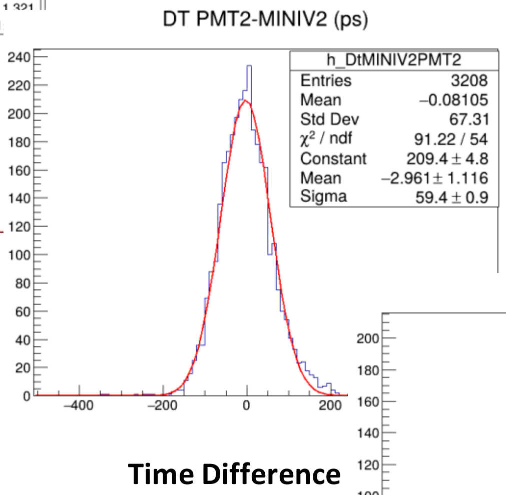


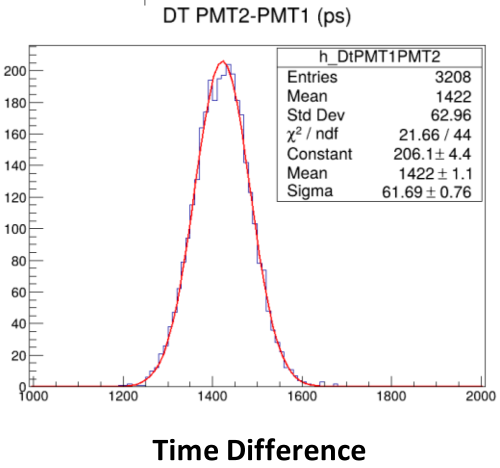
Preliminary – Ongoing analysis

Test-beam of MiniCACTUS_v2 in July 2025

Chip#04B, pixel 1-2**, 0.5 x 0.5 mm², 175 µm**, **-500V** (Back-side pol.)







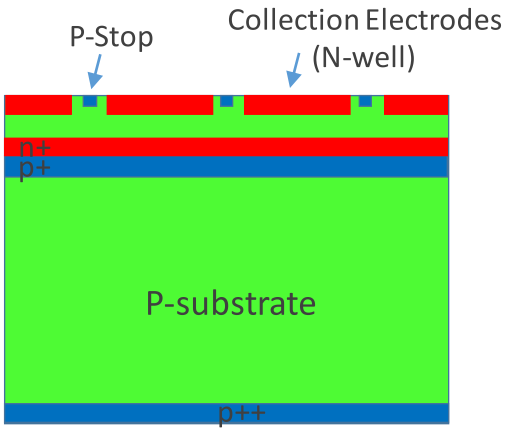
Measured Sigma Matrix after TW correction (ps)		
Sig(CACTUS-PMT1)	71.1	1
Sig(CACTUS-PMT2)	59.4	0.9
Sig(PMT2-PMT1)	61.69	0.76
Reverse of the matrix to get the sigma of each devices		
	Resolution (ps)	Errors (ps)
Sig(CACTUS)	**48.88**	1.03
Sig(PMT1)	51.64	0.97
Sig(PMT2)	33.76	1.49

Power consumption in this configuration : 0.6 W/cm²

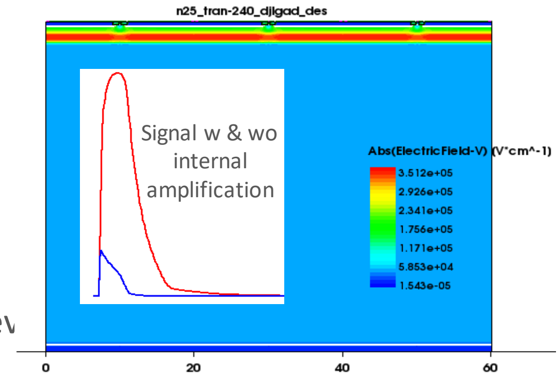
How to improve further the performances: CACTUS-GL

- Add intrinsic gain to:
  - Improve S/N → Potential improvement on time resolution
  - Reduce sensor thickness → Reduce Landau fluctuations
  - Reduce FE power consumption
  - Reduce pixel pitch
- Ultimate goal is to reach <50 ps resolution
- CACTUS-GL prototype submitted to fabrication in May 2024 (MPW run)
  - Deep junction LGAD concept with buried PN-junction
  - Better radiation hardness expected with this concept
  - TCAD simulations done with Sentaurus
  - Charge multiplication factor of ~10 expected form these simulations
  - PN junction implemented by the foundry (2 different P-dose versions)
  - Production implied only minimal modifications to LF15A standard process
    - change of implant energy of 1 layer (DNW)
    - addition of 1 customer layer
  - 6 diode structures with different guard-rings , 1 without gain layer
  - 2 epi (28 µm) and 2 HR wafers asked, HR wafers thinned & post processed similar to prev MiniCACTUS prototypes with 150 µm thickness

Cross section of the active area of CACTUS-GL (not to scale)



Typical Sentaurus TCAD simulation of a diode with buried PN junction

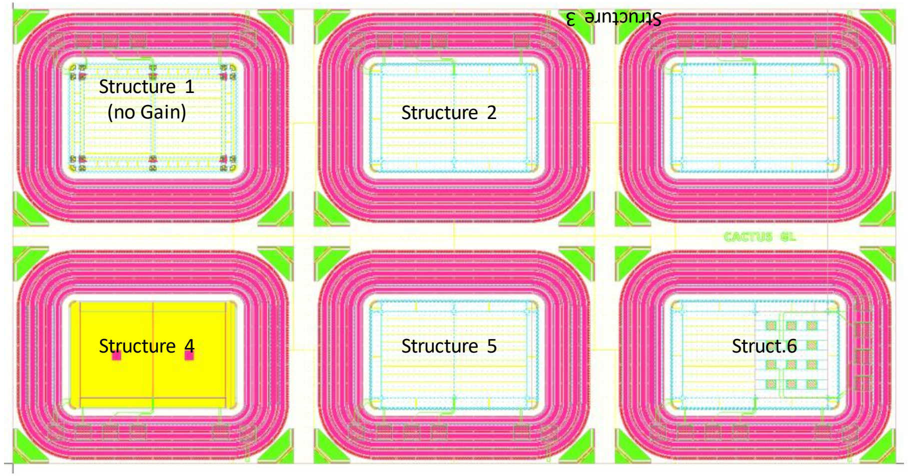


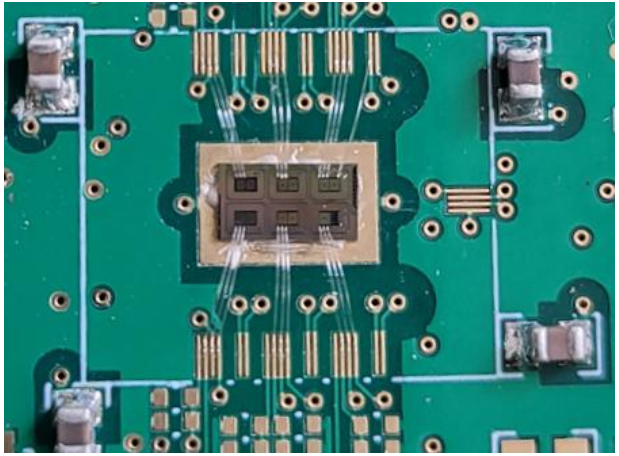
Chip layout

- 6 different diode layouts
- Each diode is split in two,
- and each half can be read out independantly

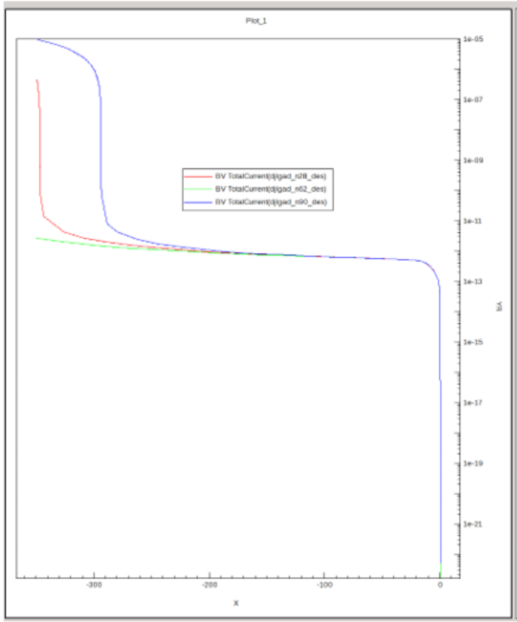
- One diode (structure 1) has no gain
- layer, for reference measurements
- Main difference from structure to structure
- is the guard rings

Layout of CACTUS-GL chip (2.3 mm x 4.3 mm)

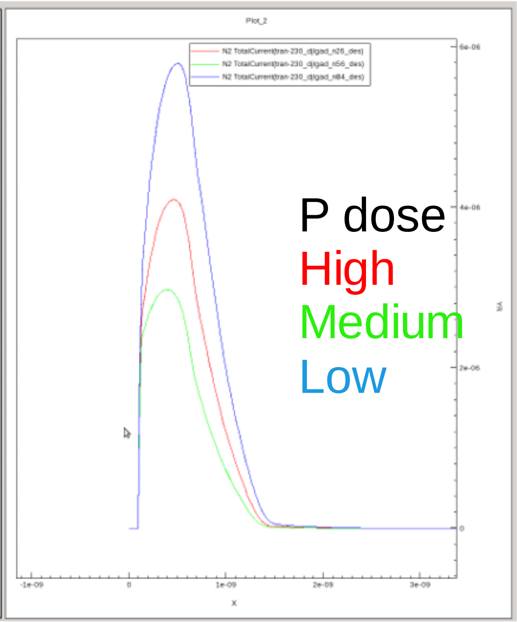




TCAD simulation of MiniCactus-GL

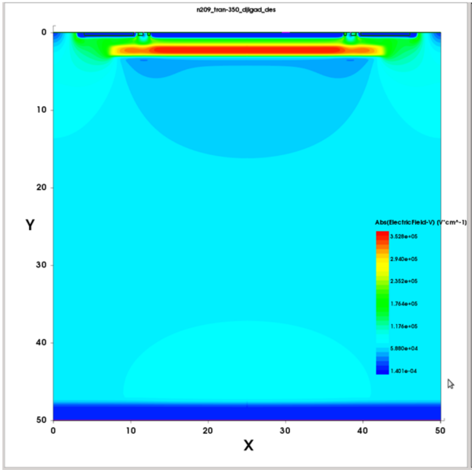


I-V curves

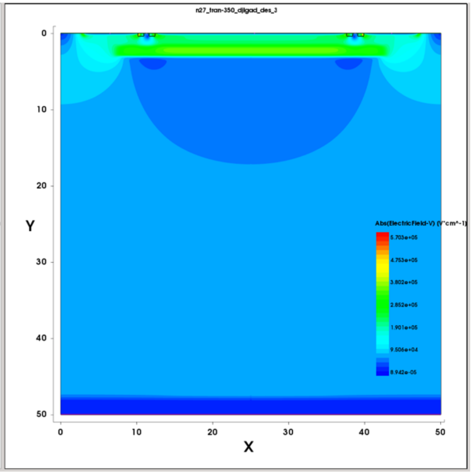


Transient signal

Electric field for one diode with external rings



NW diode



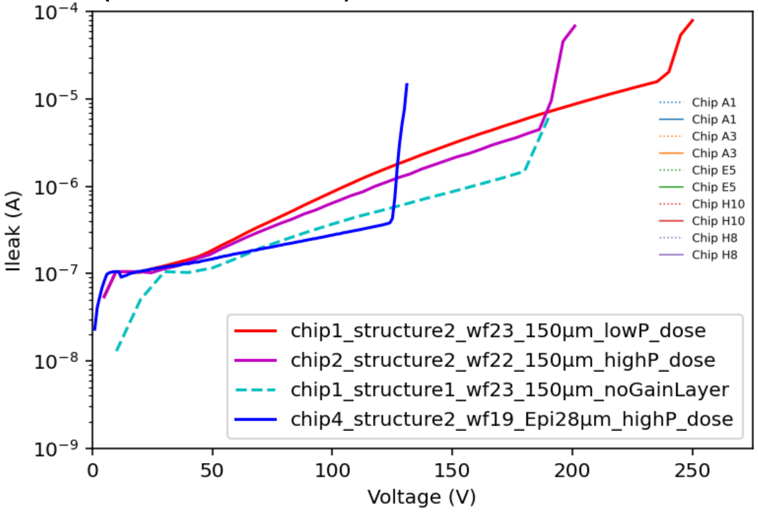
N+ diode

- Charge multiplication factor of about 10 looks possible
- Strong dependance of charge multiplication factor to P dose of gain layer structure → asked
- LF to produce wafers with two different P-dose settings
- Four wafers produced :
  - Two HR (two P-doses), thinned to 150 μ, post-processed at IBS (backside boron implant, metallization)
  - Two epi (two P-doses), 28 μ, diced at ALTER UK

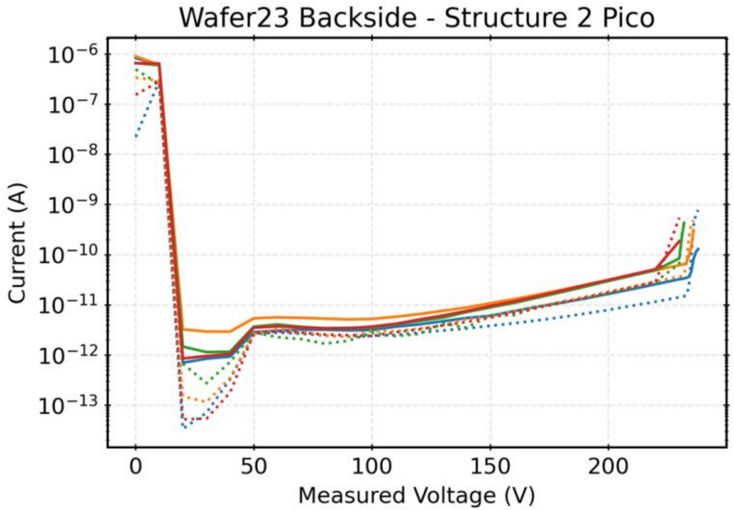
Test Results from MiniCACTUS-GL : IV curves

- Fabricated and post-processed sensors received at the beginning of 2025
- Preliminary I-V measurements done at **Liverpool** using a probe-station and later at IRFU on sensors bonded on PCB.
- Conclusions :
  - All N-well diodes with gain layer have similar behavior. **Reproducible** curves from one chip to others
  - Difference on current measurements at low bias between probe station and PCB induced by test setup (intercurrent between two half diodes)

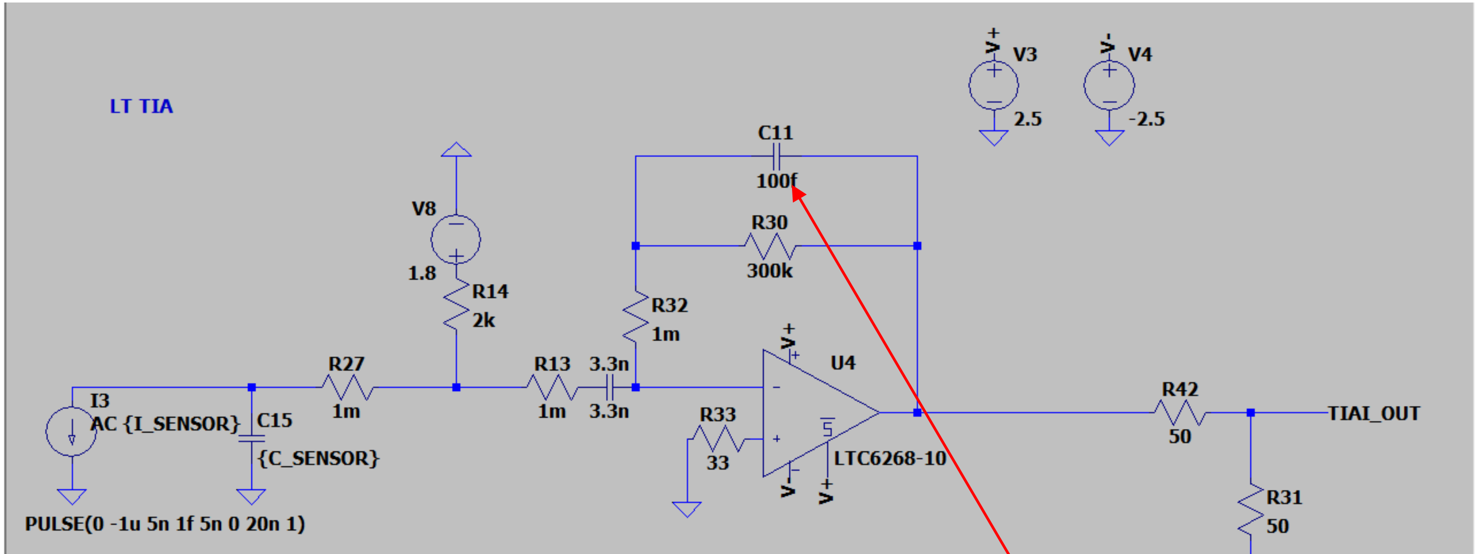
I-V curves measured on different samples (bonded on PCB)



I-V curves measured on different samples (Liverpool probe station)



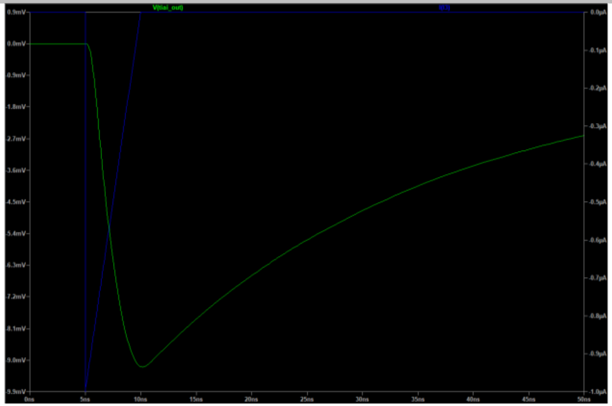
Discrete front-end : opamp TIA



LTC6268-10 : GBWP 4 GHz, slew rate 1.5 kV/us, uncompensated (stable for gains > 10)

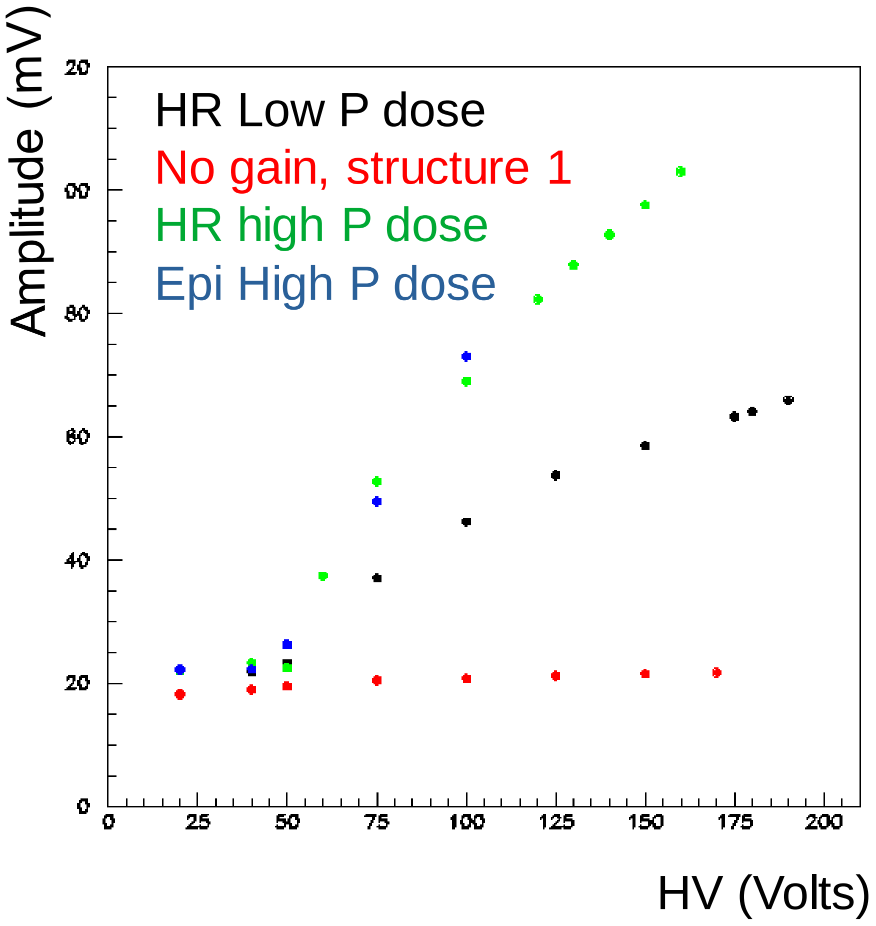
Front-end performance limited by parasitic caps

S/N with this discrete front-end does not allow good timing measurement (and this design was not intended for timing)



TIA architecture, AC coupled.
Relatively long risetime (7 ns), noise about 2 mV rms
Parasitic capacitance (C11) in feedback loop is critical. Value given here is a guesstimate deduced from pactical observations.
Output amplitude for a MIP (no gain) about 8 mV, no need for external amplification

IR LED amplitude measurements



- The clear amplitude vs HV behaviour difference between no gain and gain structure unambiguously proves there is charge multiplication occurring
- Signal amplitude high for high P dose chips than for low P dose, as anticipated from TCAD
- Charge multiplication starts earlier than predicted by TCAD, around 50 V instead of 100 V
- Epi high P dose gives interestingly high signals, given the low thickness (28 μ) of collecting diode
- Very large voltage range over which gain is present

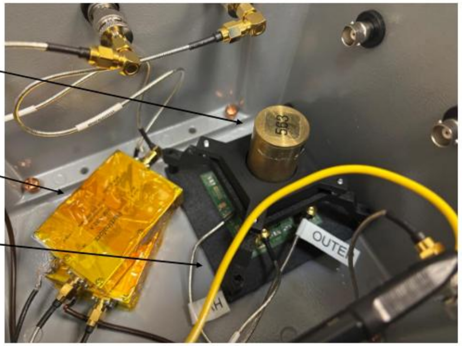
90Sr signals are visible even without FE

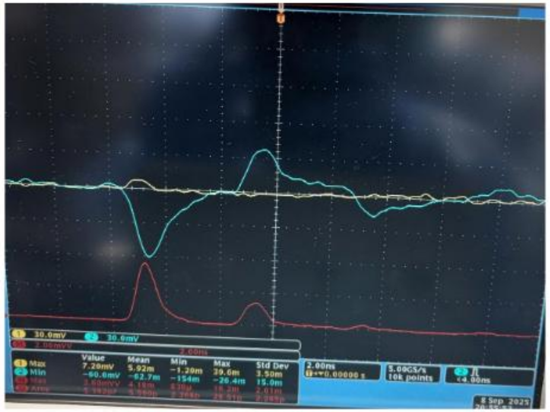
SR 90 Beta Source

Amplifiers connected to Left and Right Diodes, the to scope.

HV supply – connected to TopBias

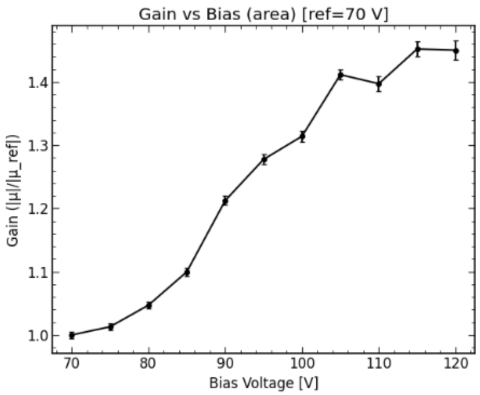
DummyDiodes grounded, all other connections floating





- Diode under test
- Diode signal squared

Epitaxial Wafer: Structure 2

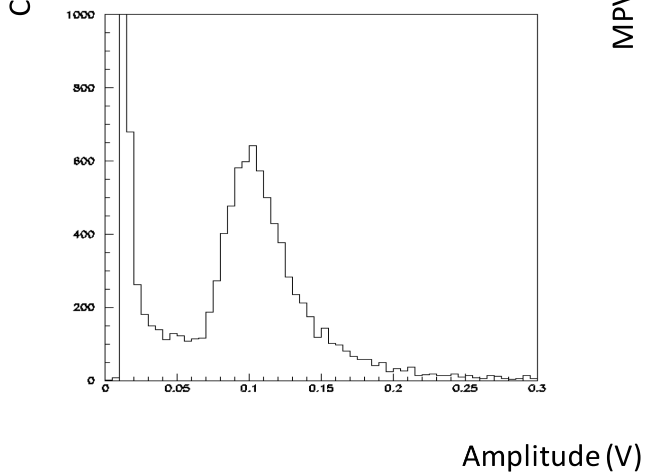


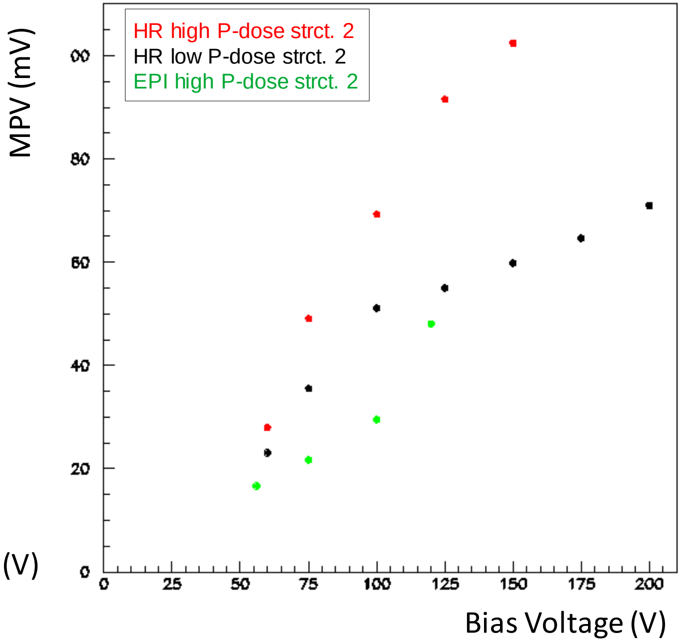
- Not true 'gain' plotted, since no signal detected on structure 1 (reference)
- factor of 1.4 gain at 120V, compared to 70V
- Expected to be ≈ 1.3 if only caused by increase in depletion region.

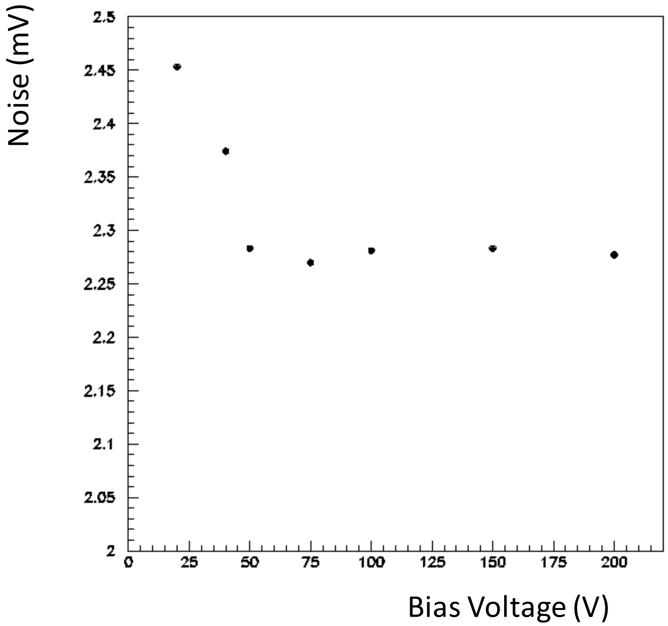
90Sr measurements

- ^{90}*Sr* spectra (*in coincidence with PMT below DUT*) obtained on gain layer diodes from HR high P dose, HR low P dose, and epi high P dose. Epi low P dose still to be tested.
- Peak not measurable on the version **wo gain** (due to S/N of external FE); only the **tail** of Landau visible
- High P-dose gives higher gain and lower BV as expected from TCAD simulations
- Very preliminary estimated gains using ^{90}*Sr* source is about ≈ 6 for the low P-dose and ≈ 10 for the high P-dose
- Capacitance variation visible (through noise measurement) below multiplication threshold

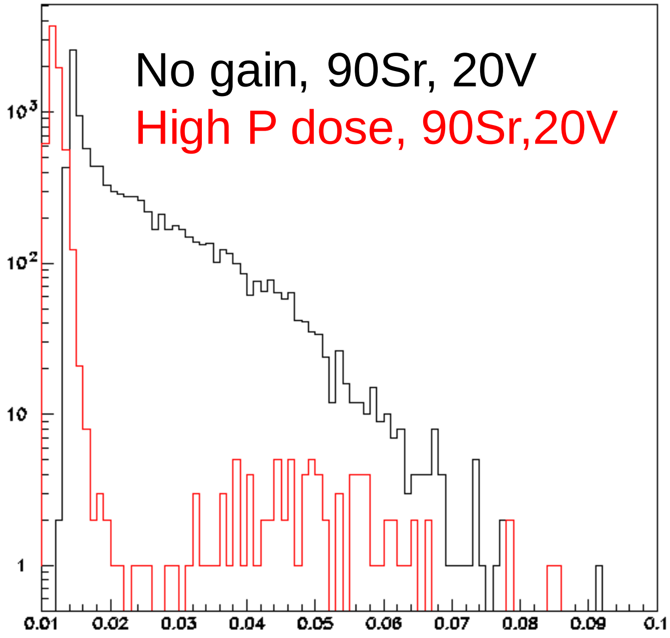
Typical Landau distribution obtained with 90Sr. HR High P dose, 150 V





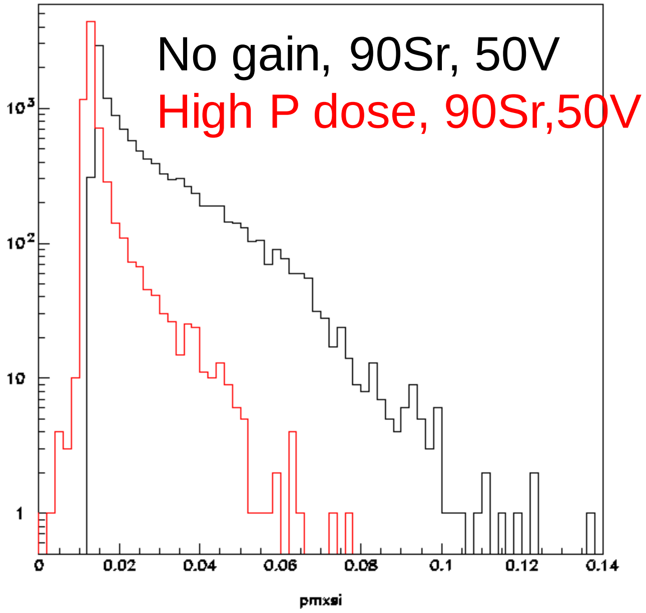


Comparison of 90Sr signals for amplified and non amplified structures below 50 V



Amplitude (V)

Response of a non amplified diode and an amplified diode are very different. Threshold effect due to gain layer ?



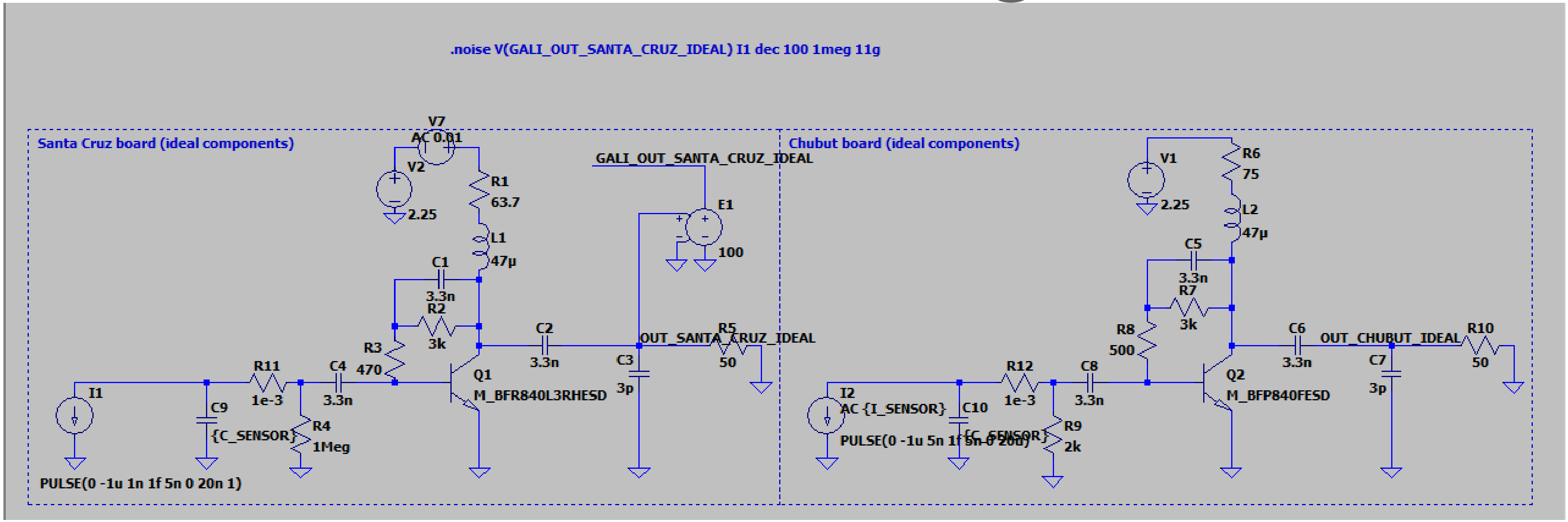
Amplitude (V)

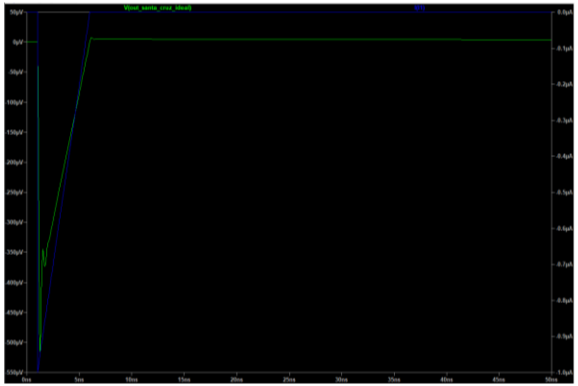
Conclusions and prospects

- Test structures produced with LF15A process clearly show charge multiplication above 50 V
- Epi wafer gives particularly interesting results
- Measurements just started, have still to test structures 3,4,5,6. Structure 5 has systematically BV higher than others → particularly interesting
- Need to revisit TCAD simulation to optimize further gain layer
- Plan to submit a MiniCactus V2 with GL chip (with integrated FE, suitable for timing) and improved test structures (higher BV) together with Radpix for LHCb

Backup

RF FE design

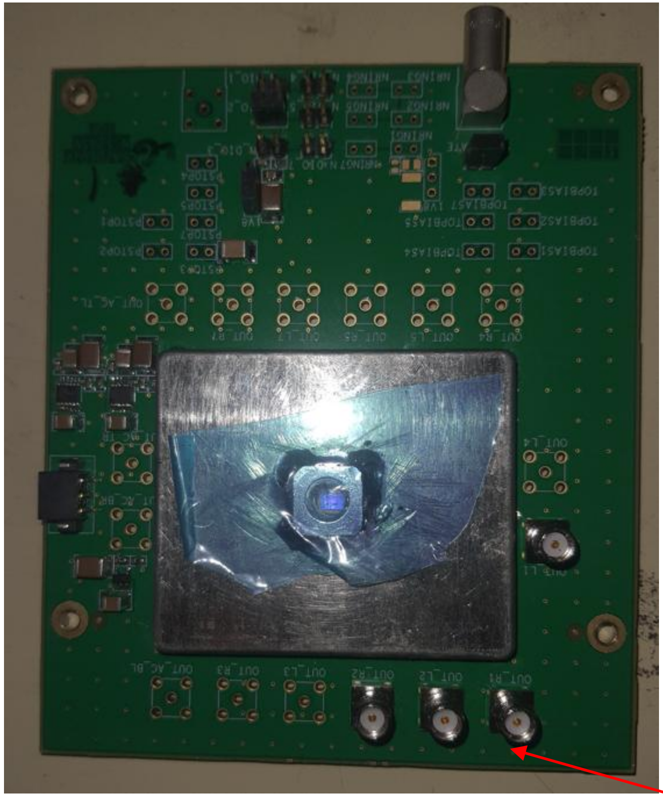


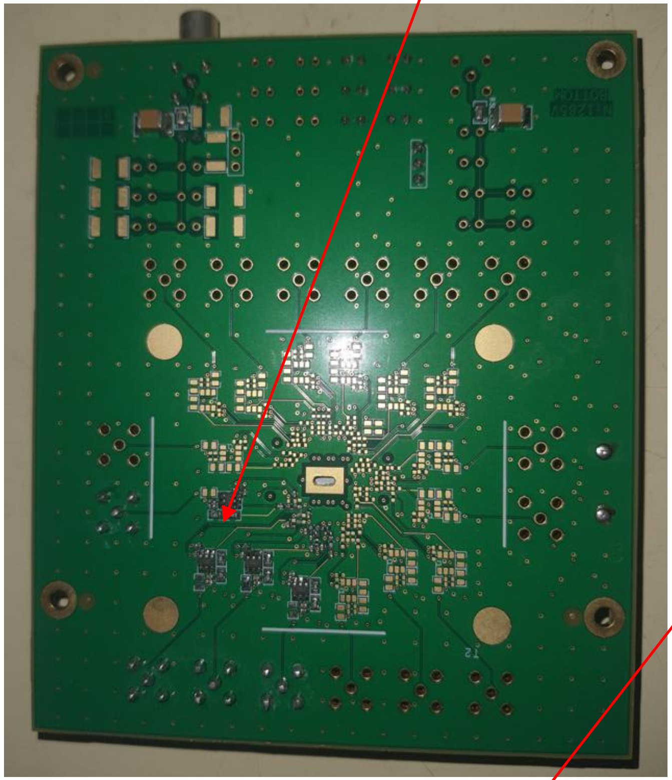


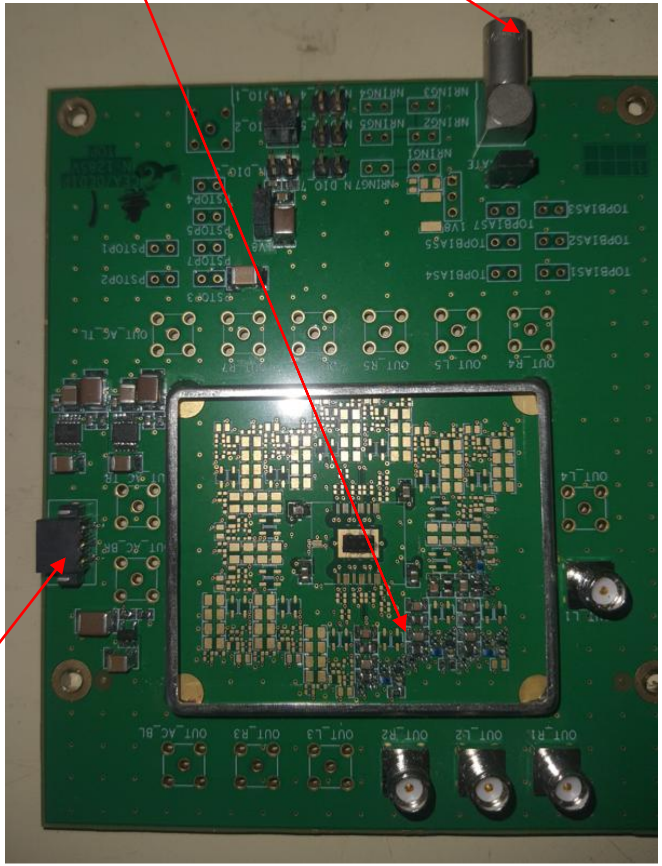
- CE BJT architecture, with SiGe heterojunction NPN RF transistor
- Copy/paste from Santa Cruz LGAD/Chubut test board (M. Senger, Zürich)
- Elaborate power rail filtering (not visible here)
- Very short risetime (800 ps), low noise (few hundreds of uV)
- Output amplitude very small (500 uV for a MIP), needs external voltage
- amplifier (Gali 52, x10)

Test board design

LT TIA (bottom) RF FE (top) HV (LEMO)







SMA Analog outputs

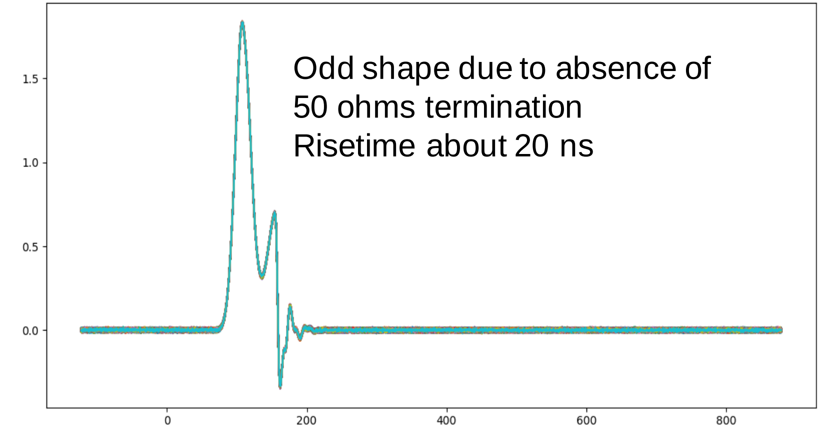
LV (+5/-5), same connector as MiniCactus

120 mm x 100 mm. Mounting compatible with MiniCactusV2 test frame,

Same chip position and same mounting holes positions → can potentially be used in testbeam

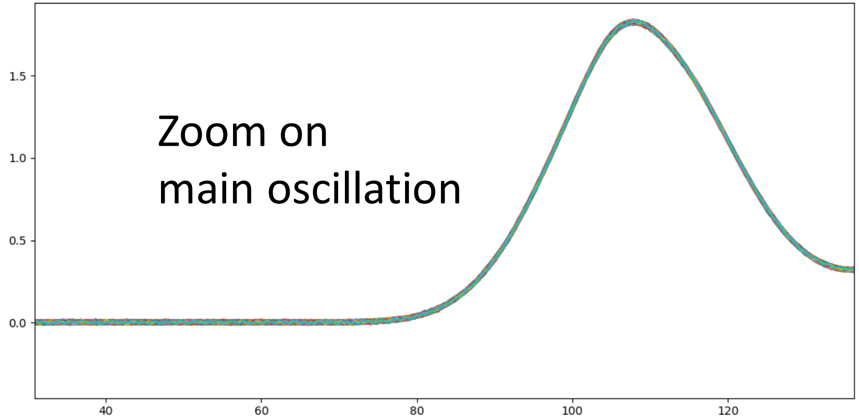
LED signals : injection with 940 nm IR diode

Vgene (V)



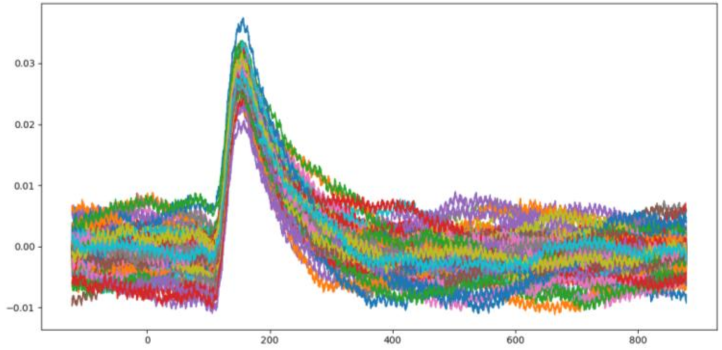
t(ns)

Vgene (V)



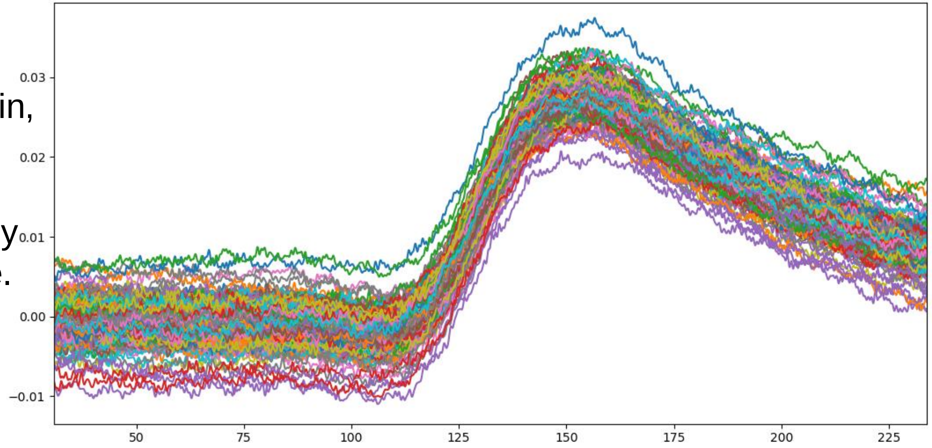
t(ns)

V out (V)



t(ns)

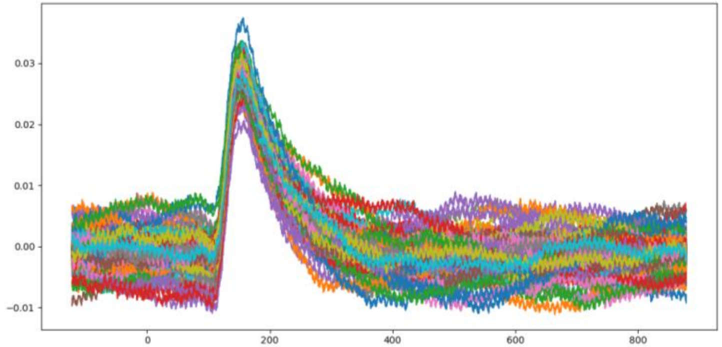
Structure 1, no gain,
100V, HR wafer
RT about 20 ns,
likely dominated by
AWG/Led risetime.



t(ns)

LED signals : structure 1 (no gain) vs structure 2

V out (V)

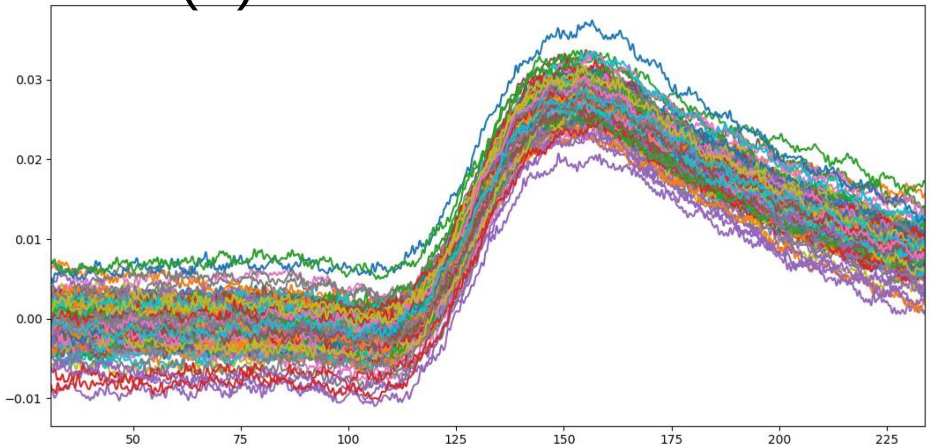


t(ns)

Structure 1, no gain, 100V, HR wafer
RT about 20 ns, likely dominated by AWG/Led risetime.

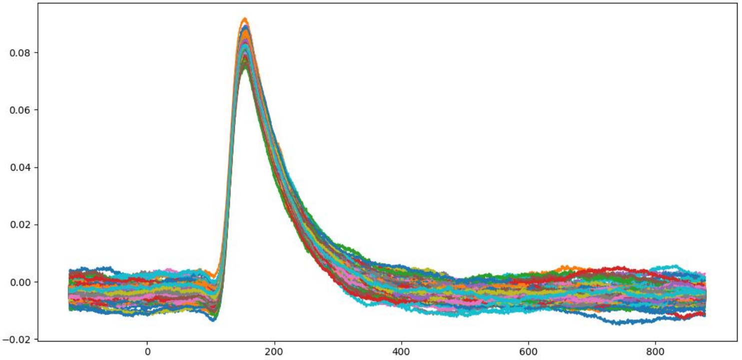
TIA LT FE

V out (V)



t(ns)

V out (V)



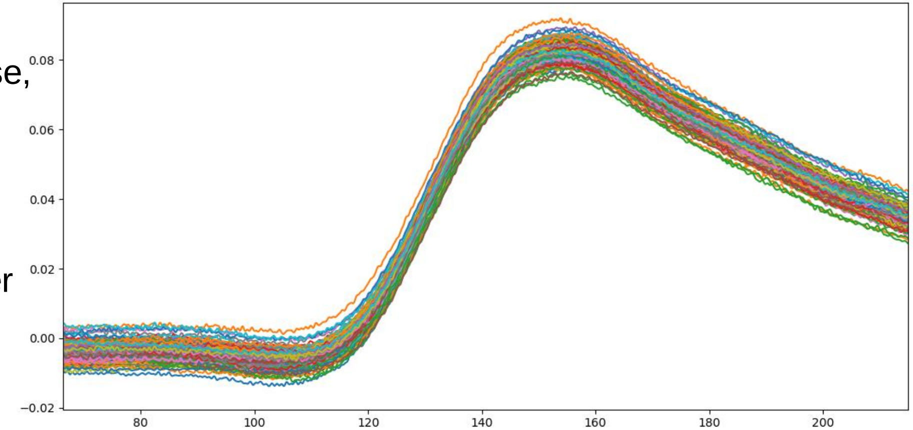
t(ns)

Structure 2, with gain layer, 100V, low P dose, HR wafer

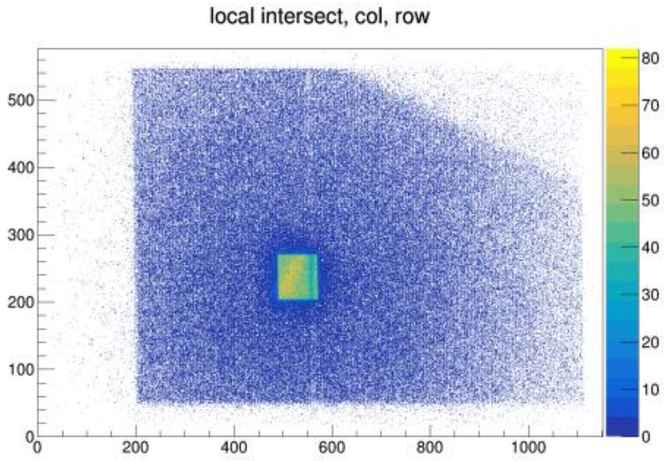
Signal shape similar to no gain signals, amplitude much higher (80 mV vs 30 mV). Risetime about 20 ns

TIA LT FE

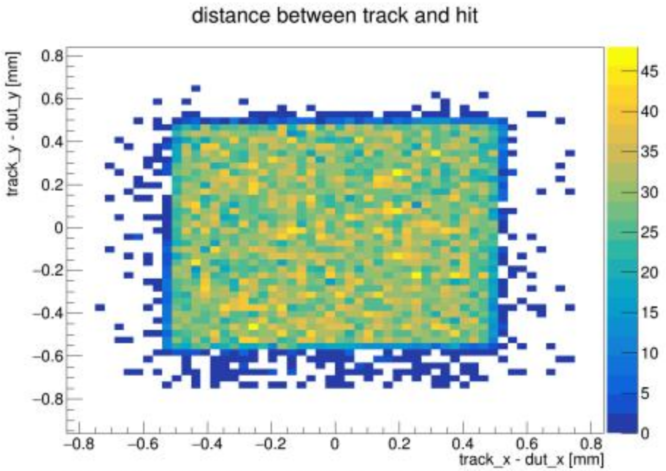
V out (V)



t(ns)

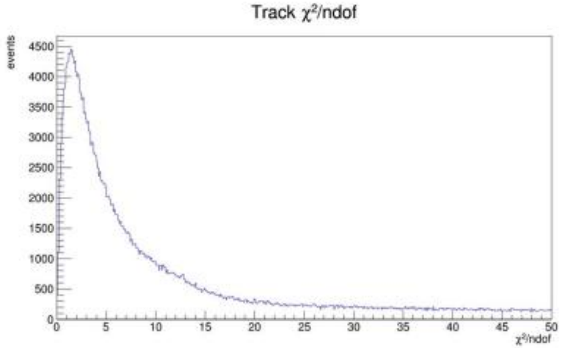


MIMOSA reference plane showing the ROI selected on the CROC, about 1.1x 1.2 mm^2



Distance from the tracks with hits on the DUT from the center of the DUT pad

- We assumed a hit if the analog output signal of the DUT was higher than 0.06 V
- Events for the efficiency calculated where selected for:
  - Single track/event
  - Event detected on at least 4 planes
  - Events intercepting the DUT



Track chi^2/n_{dof}

Preliminary – Ongoing analysis