The CALOROC family

Meeting FCC/DRD France PARIS

Ch. de LA TAILLE

Organization for Micro-Electronics desiGn and Applications

Trends for calorimeter readout (DRD6)

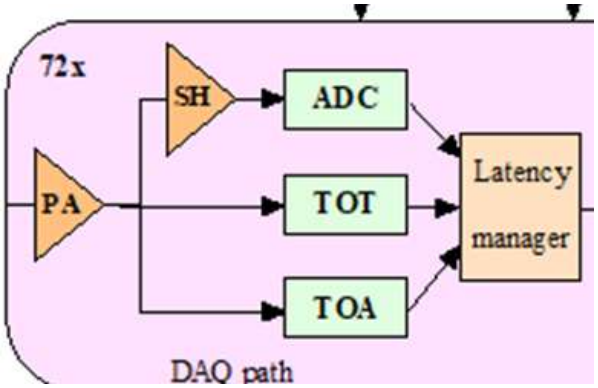
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

Embedded ASICs

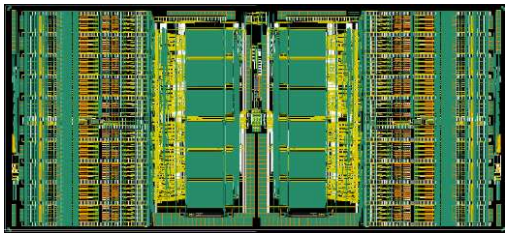
- Pioneered with CALICE R&D (SKIROC, SPIROC..)
  - Experienced with CMS HGCAL (HGCROC/H2GCROC)

- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch)

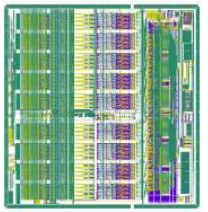
- Upcoming R&D
  - Power reduction,
  - Auto-trigger, Data-driven readout
  - Exercised with EIC CALOROCs



H2GCROC

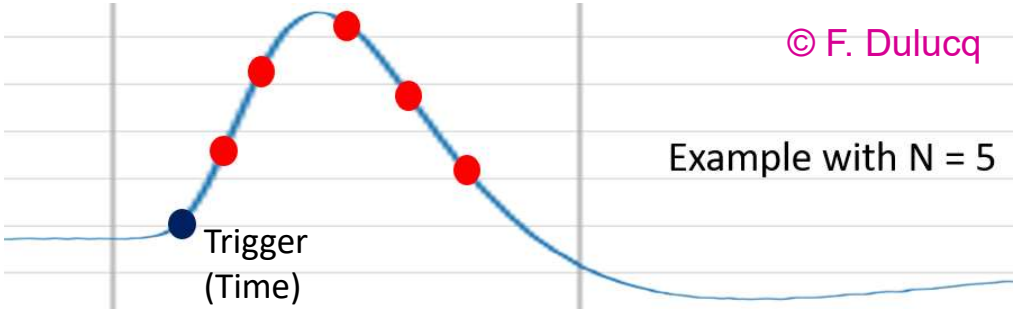


CALOROC



CALOROC: Waveform Digitizer with Auto-Trigger

- CALOROC is a waveform digitizer working @ 39.4 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm is outside (back-end or offline)



CALOROC can accept ~ 50 kHz rate per channel (worst case)

Internal HKROC memory writing is without dead time

Hit-rate is only limited by serial link bandwidth (average values above)

A zero-suppress feature can be activated

A fast command can trigger an ASIC snapshot
(monitoring, calibration, heartbeat)

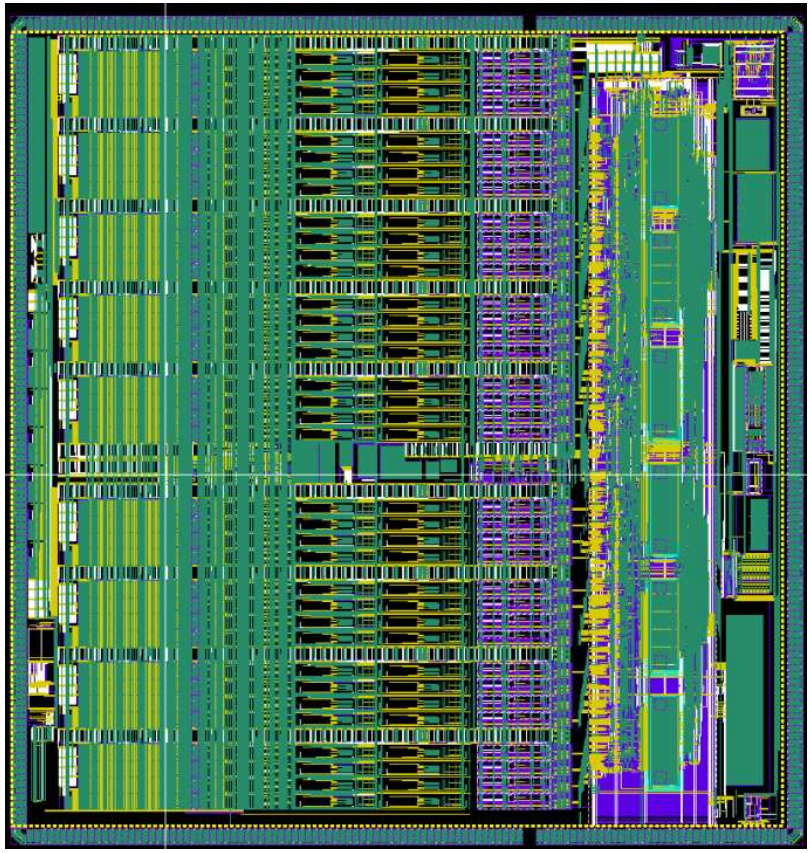
overview of CALOROC family : 1A/1B/1C

- **CALOROCs common features**
  - 36 channels ~10-15 mW/ch
  - Auto-trigger and Streaming readout : 2 links @ 1.28 Gb/s
  - Triplicated I2c configuration and fast commands inputs
  - TSMC 130n technology
  - BGA package : same pinout

- Conservative **CALOROC1A**: SiPM readout from H2GCROC

- New **CALOROC1B**: SiPM readout with gain switching
  - New analog front end : higher dynamic range and input capacitance
  - Lower noise, better jitter

- **CALOROC1C** for Si/LAr detectors: Si readout from HGCROC
  - Slower shaping
  - Cryogenic temperature adjustment

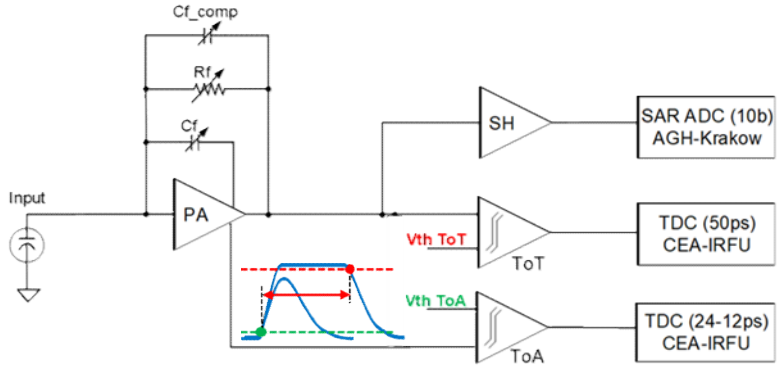


CALOROC1A/B/C overview

	CALOROC 1A	CALOROC 1B	CALOROC 1C
Detector	SiPM	SiPM	Si / LAr
Detector capacitance	0 – 1000 pF	0 – 10 nF	0 – 300 pF
Noise	20 fC @500 pF	2.6 fC @500 pF	0.2 fC @50 pF
Dynamic range	20 fC – 320 pC	2.6 fC – 200 pC (@500 pF)	0.2 fC – 10 pC
Shaping time	20 ns	25 ns	200 ns
Jitter @MIP=300 fC	400 ps (@500 pF)	35 ps (@500 pF)	-

CALOROC1A (based on H2GCROC)

- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / SiPM range 100-600 pF



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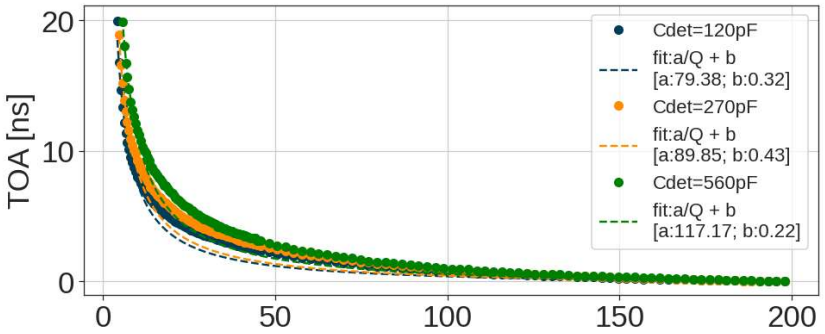
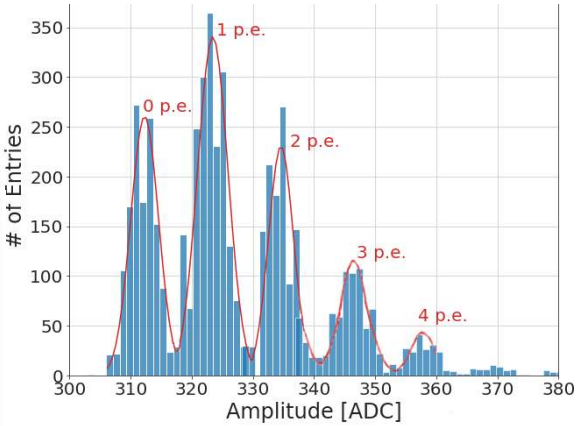
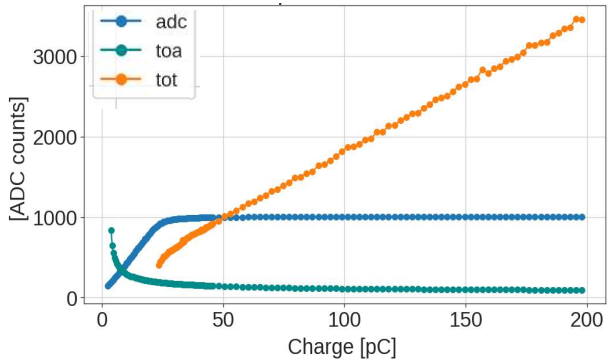
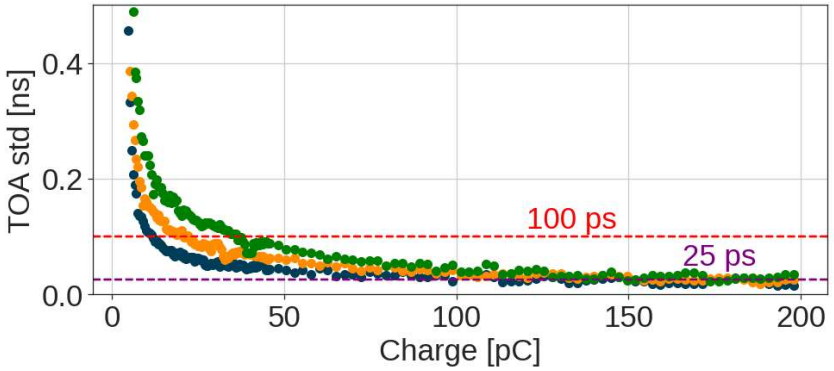
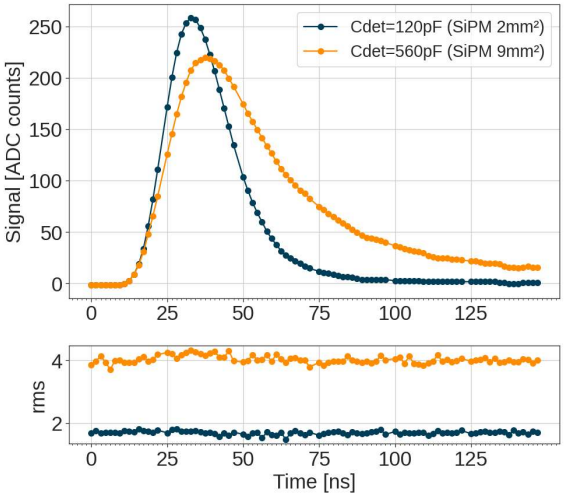








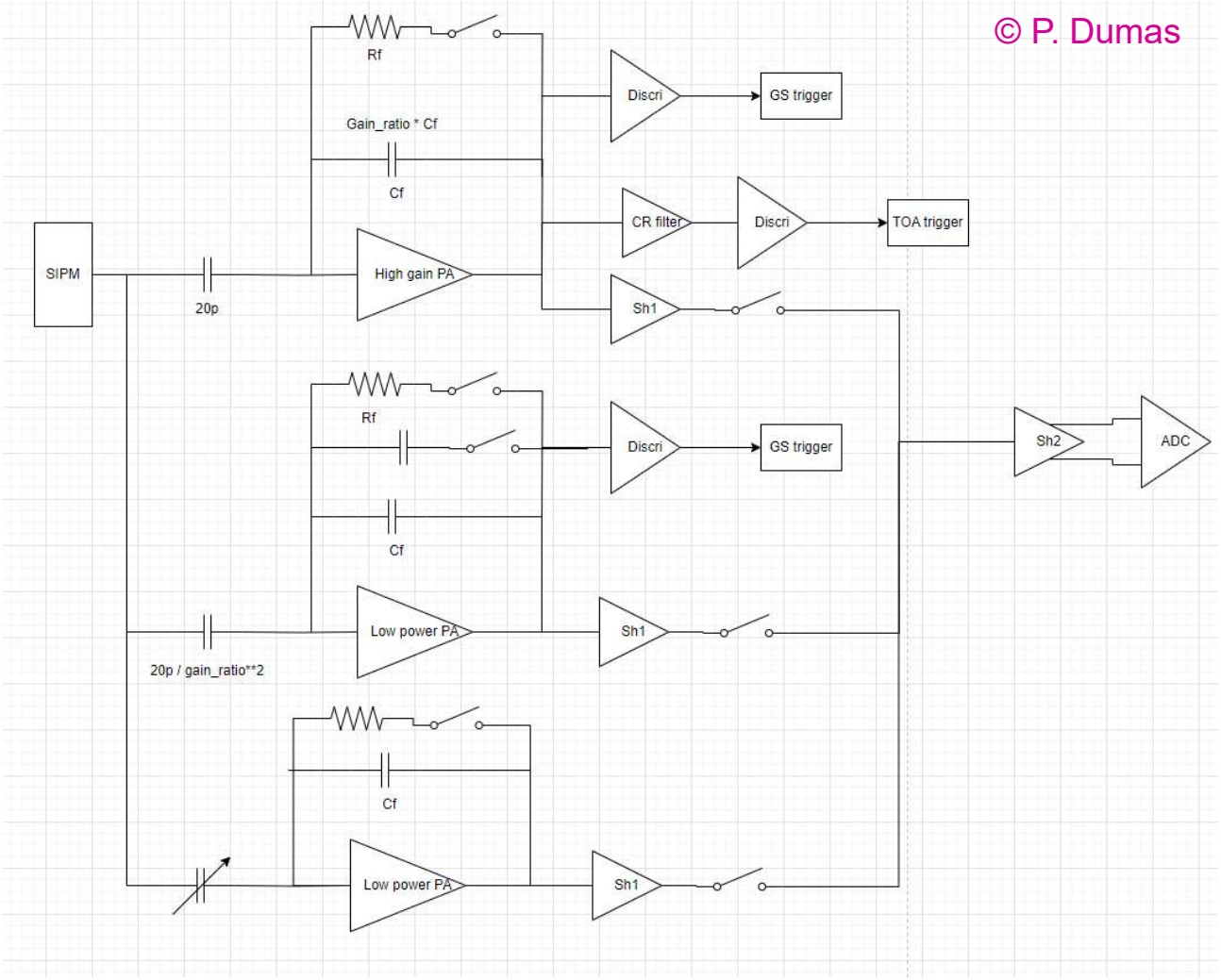


- CALOROC1A will only update its back-end to be EIC compatible

* TWEPP 2023 ➔ https://doi.org/10.1088/1748-0221/19/04/C04005

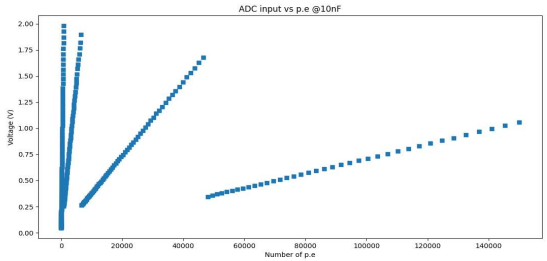
CALOROC1B: gain switching architecture

- New dynamic frontend with switched gain:
  - High gain
  - 2x medium gain
  - Low Gain
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 500 pF to 2.5 - 10 nF
  - ~ 10 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



CALOROC1B: simulated linearity

- Less than 1% linearity error



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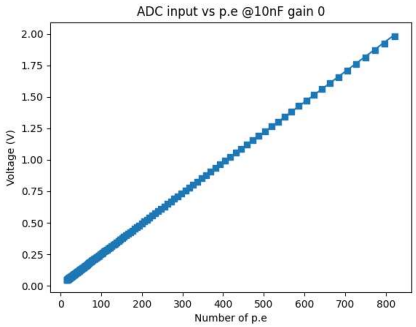

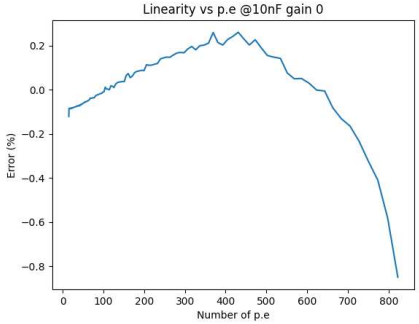

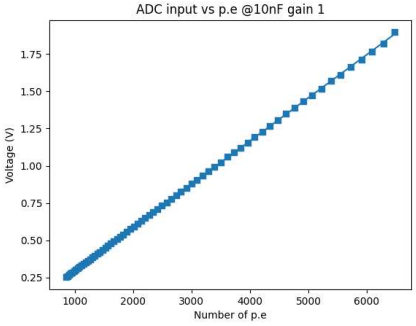

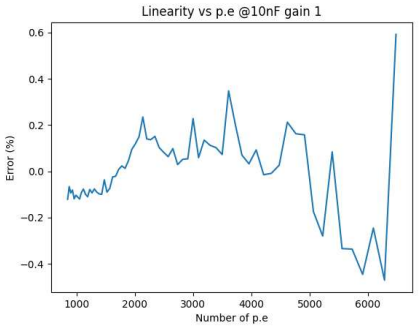

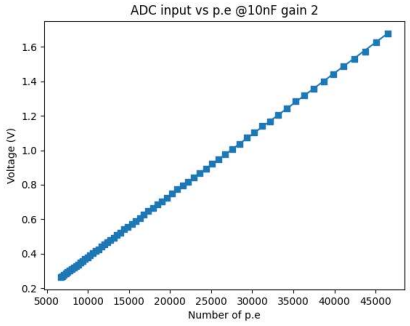

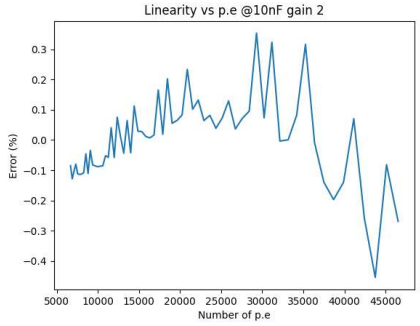

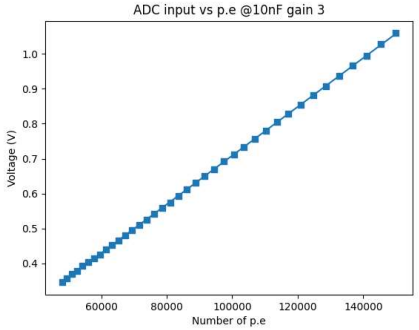

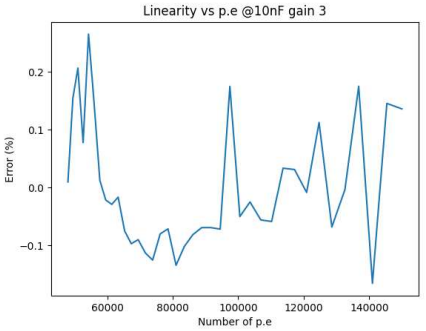

CALOROC1B: simulated timing accuracy

- Simulated time jitter goes down to 20 ps with < 500 ps for a MIP of 432fC @Cin=10nF
- Time walk is below ~2,5 ns

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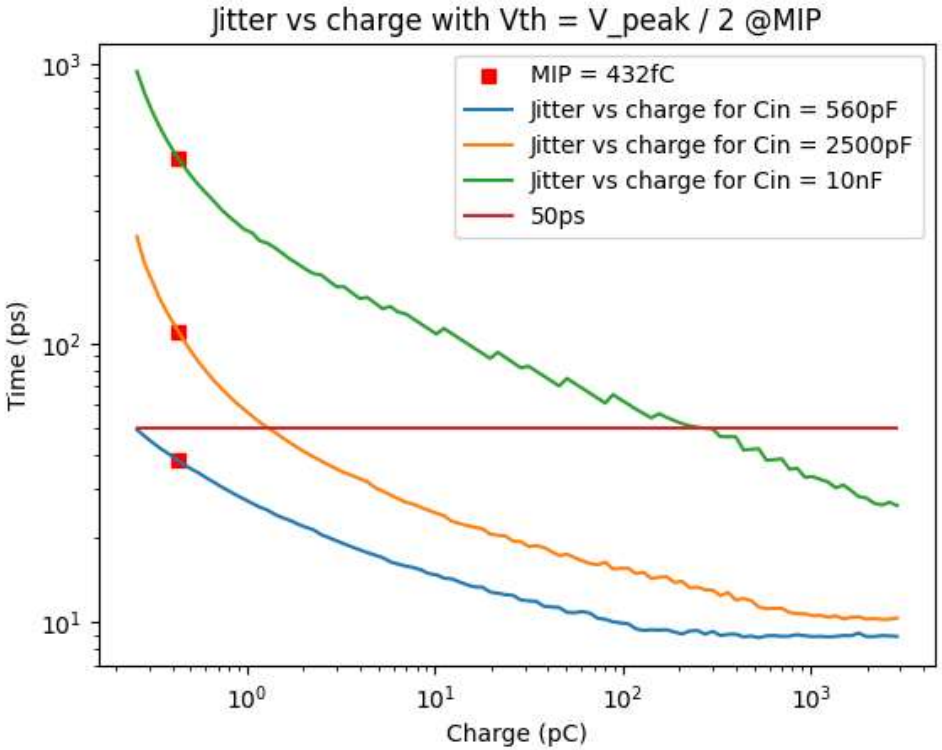

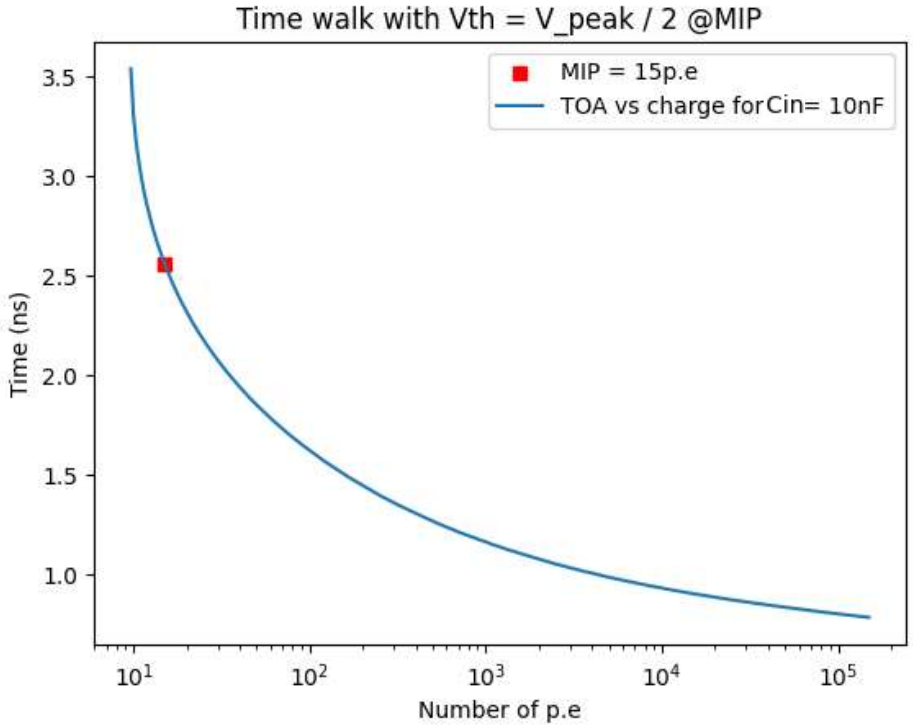

CALOROC1B: simulated SNR vs SiPM size

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- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

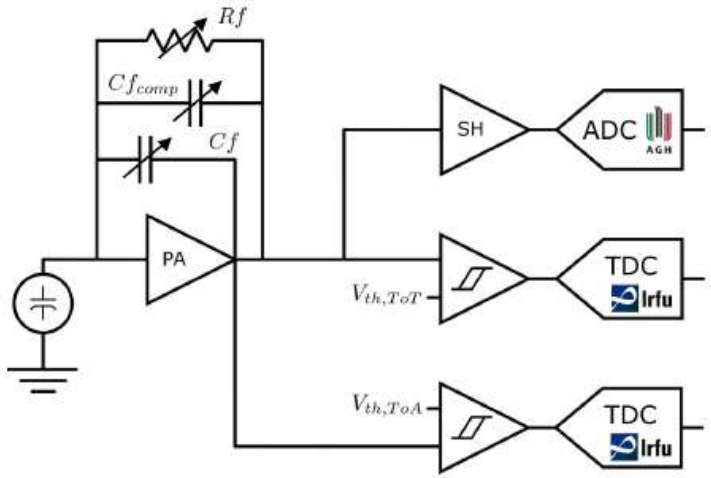
- CALOROC1b will be able to readout SiPM in the range ~ 500 pF to 10 nF
  - Timing measurements will focus on the MIP (~15pe)

Operation modes	1 SiPM of 530pF Caloroc1B	1 SiPM of 2.5nF Caloroc1B	4 SiPM of 2.5nF Caloroc1B	1 SiPM of 530pF Caloroc1A
Cin	530pF	2.5nF	10nF	560pF
Dynamic range in charge (Noise - Max)	2.6fC-190pC	12fC-770pC	48fC-3.1nC	20fC-320pC
Input time constant (occupancy related)	100ns	500ns	500ns	10ns
Jitter @ MIP (≈400fC)	35ps	110ps	470ps	400ps
SNR @ 1p.e (≈30fC@gain=1.8e5)	10	2.4	0.6	1.44

SiPM: S14160-3010PS 3x3mm (530pF) / S14160-6010PS 6x6mm (2.5nF)

CALOROC1C for Si and LAr

	LAr (FCC)	Si
Function	Charge Measurement	**Charge and Time Measurements**
MIP	**2.25fC** (750keV)	4fC
Dynamic Range	**0.2fC** - 4.5pC (70keV - 1.5GeV)	0.4fC - **10pC**
Temperature	**87K**	**Ambient T**
Cdet	50 - **220pF**	**20** - 50pF
Crosstalk	<**0.1%**	<1%



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	HGCROC
Function	Charge and Time Measurements
MIP	3.5fC
Dynamic Range	0.2fC - 10pC
Temperature	-30°C
Cdet	5 - 100pF
Crosstalk	<2%

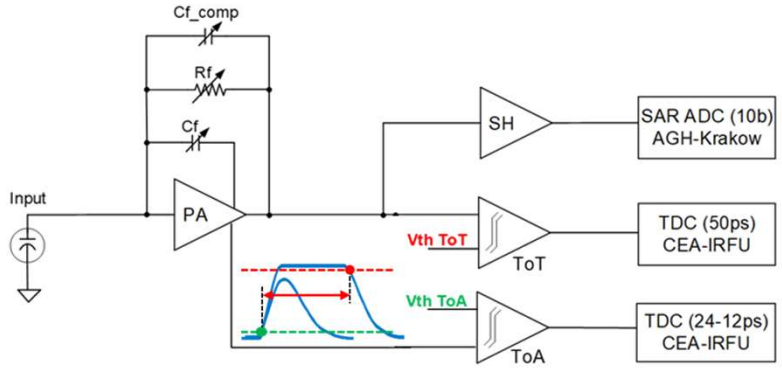
The specification fits nicely with HGCROC (chip for HL-LHC CMS HGCAL)

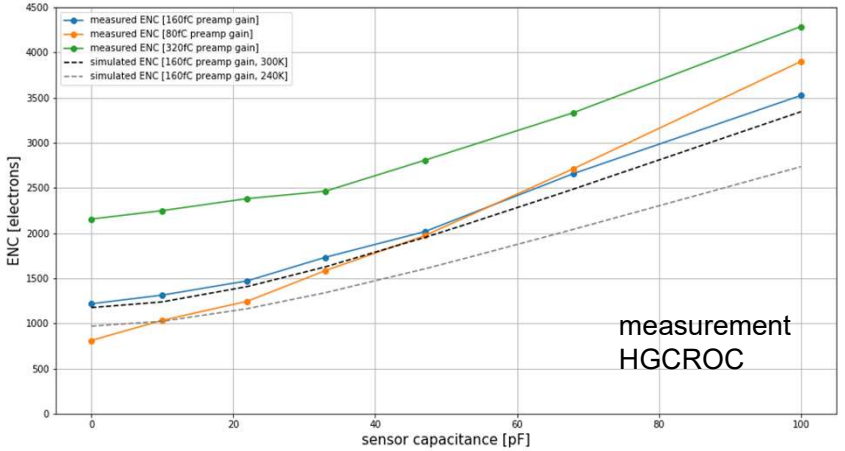
- except temperature (measured down to -30°C)
- and some 'minor' modifications

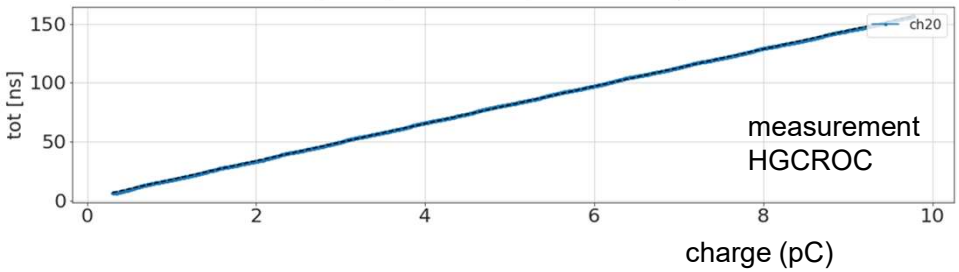
CALOROC1C (based on HGCROC)

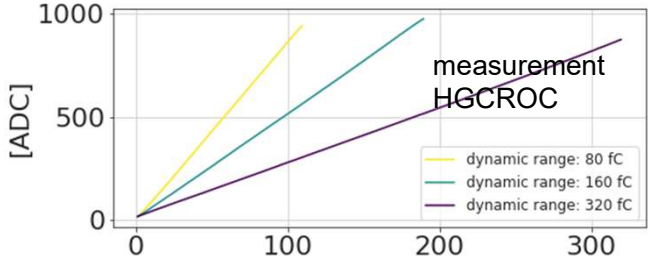
© D. Thienpont

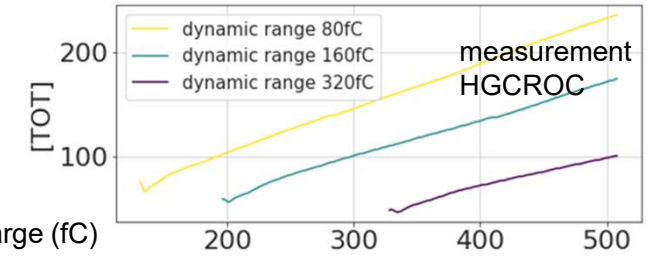
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / Radiation performance / Si up to 100 pF

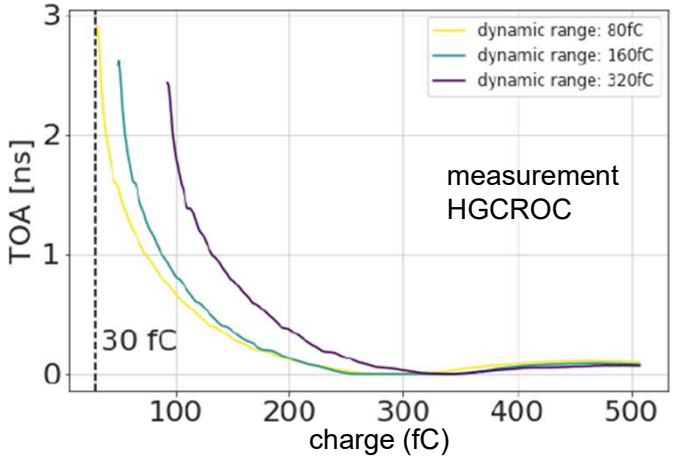












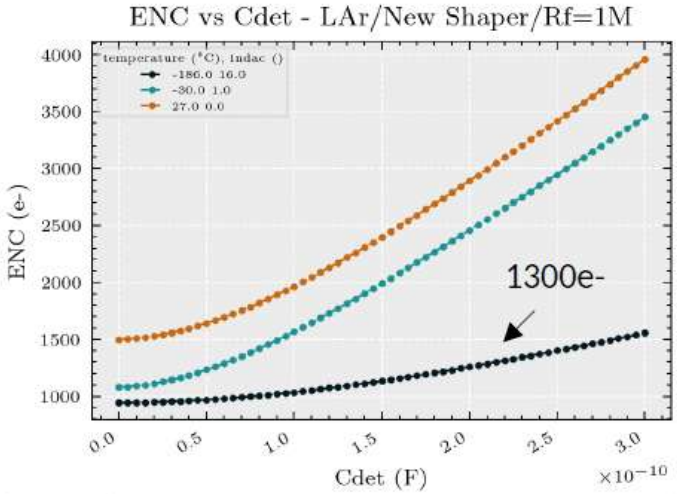
* TWEPP 2023 ➔https://doi.org/10.1088/1748-0221/19/04/C04005

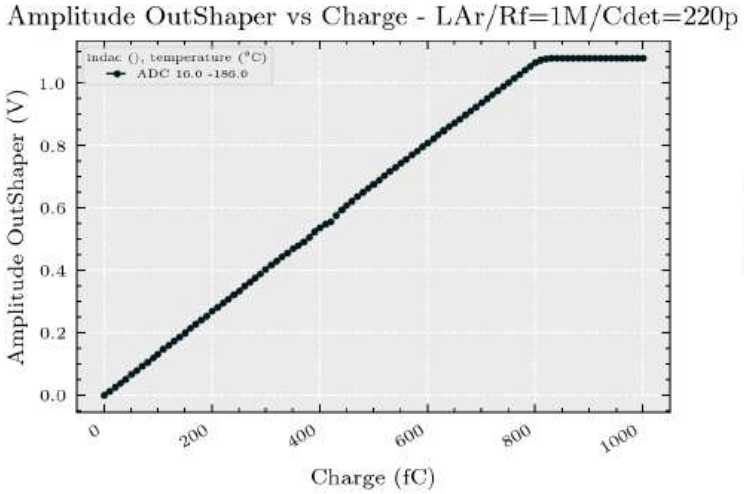
CALOROC1C : simulations for LAr application

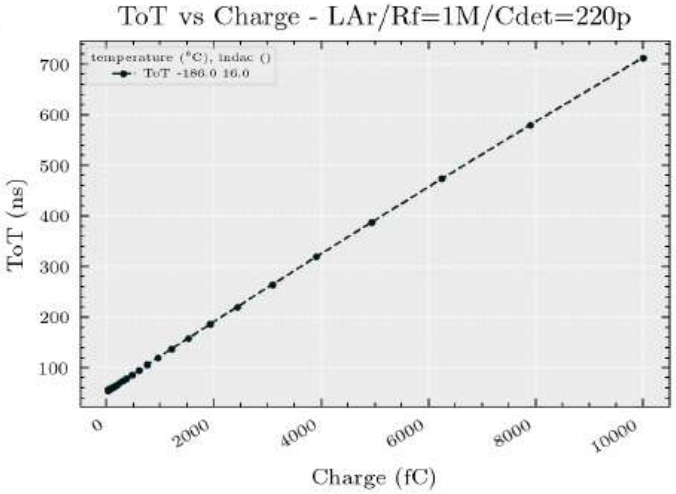
- Slower shaping time to reduce the noise from 7000 e- to 1300 e- (Cd=220 pF T=87K)

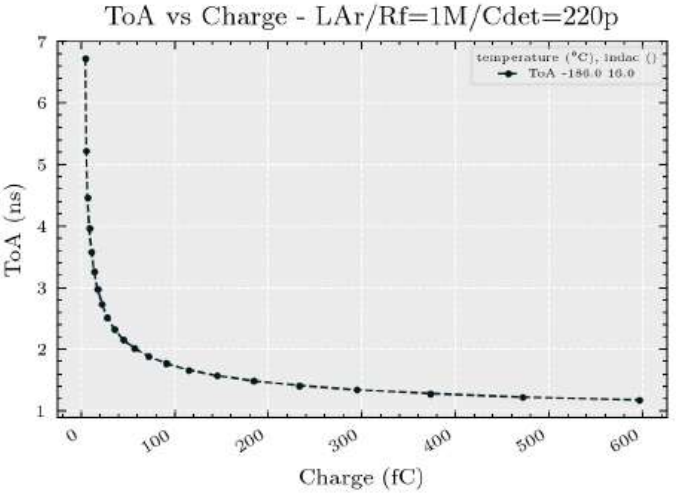
© A. Laffitte

- **Power:** ~10mW/channel
- **ADC Dynamic Range/Resolution:** 10bits
- MIP 2.25fC -> Noise < 0.45fC -> ENC < 2800e
  - **ENC:** (LAr/87K/220pF) ~1300e-
- **ADC Dynamic Range:** ~800fC
- **TDC Dynamic Range:** ~10pC



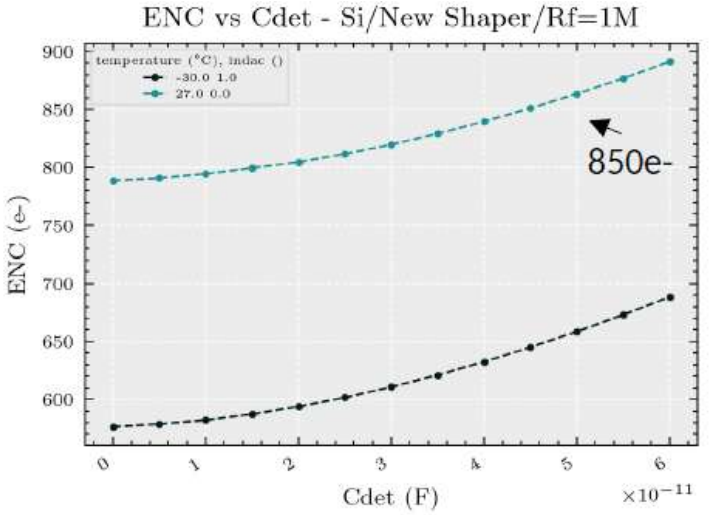






CALOROC1C : simulations for Si application

- **Power:** ~10mW/channel
- **ADC Dynamic Range/Resolution:** 10bits
- MIP 4fC -> Noise < 0.8fC -> ENC < 5000e-
  - **ENC:** (Si/27°C/50pF) ~850e-
- **ADC Dynamic Range:** ~350fC
- **TDC Dynamic Range:** ~10pC



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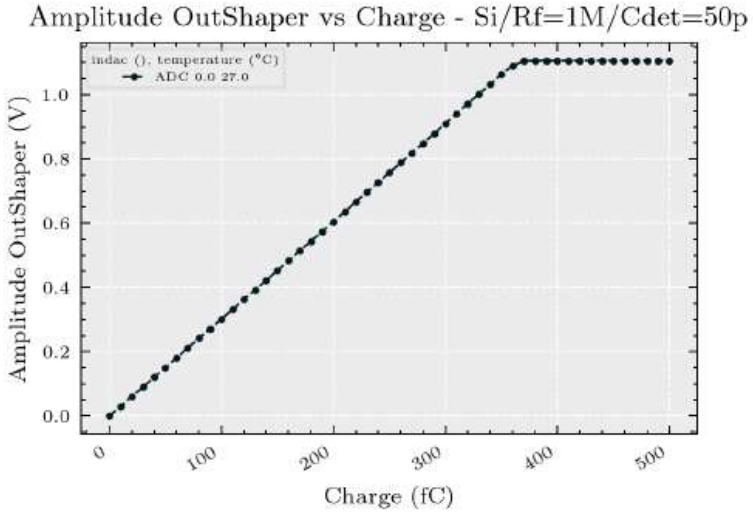
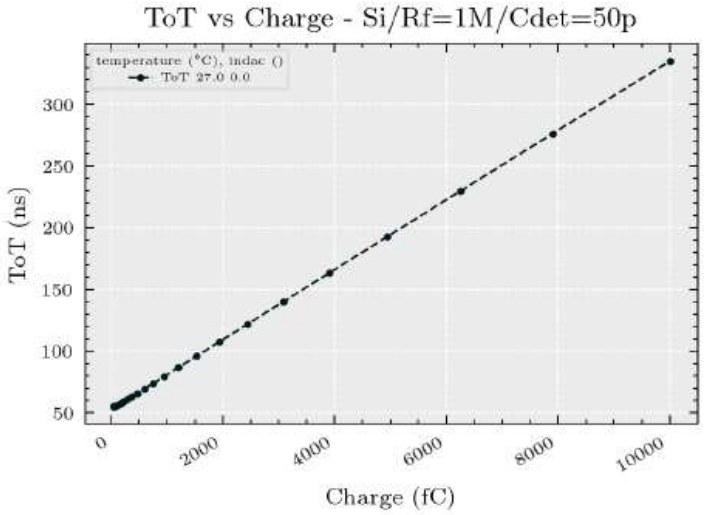
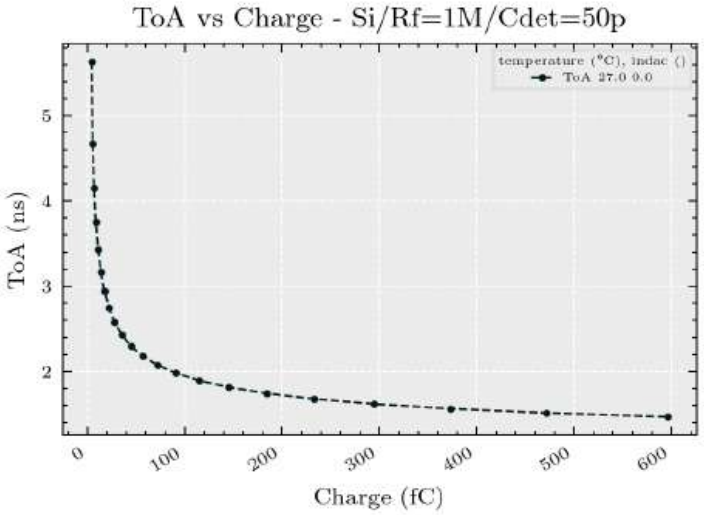
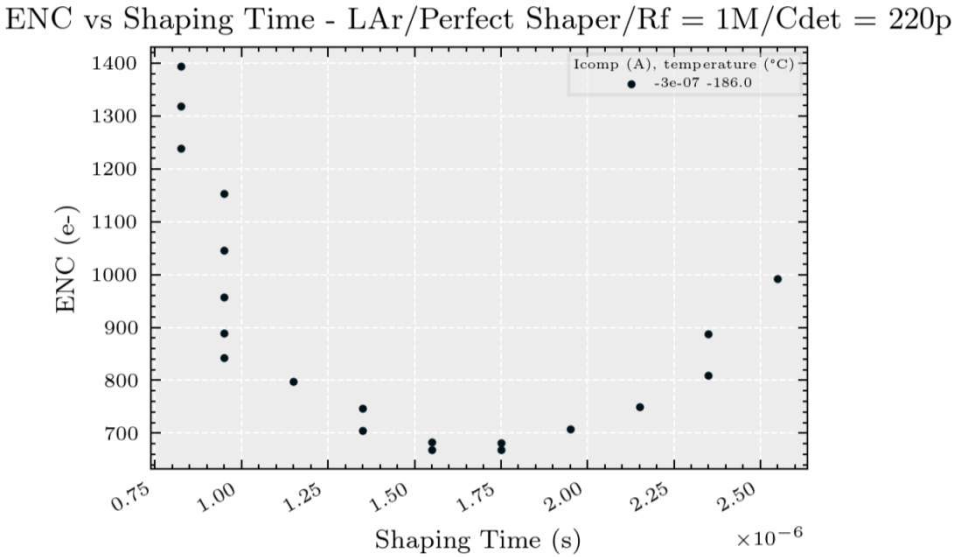






Future work on CALOROC1C : lower power

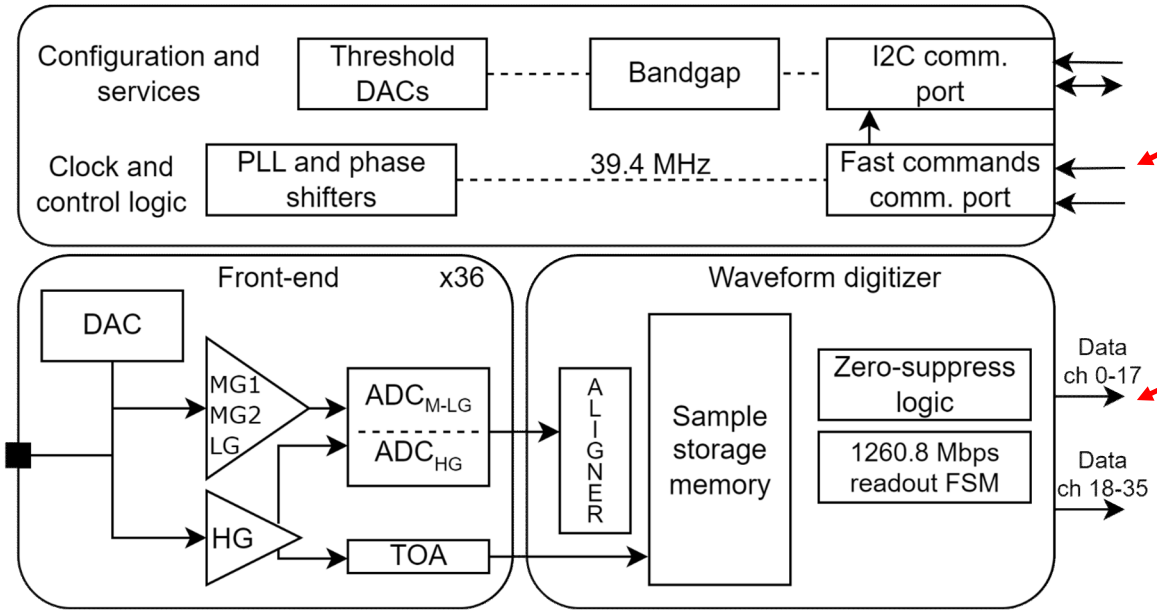
- MIP/noise = 10 good enough
  - Increase preamp noise to reduce power
  - ENC ~ Power$^{0.5}$
  - Use dynamic gain switching
- Reduce ADC speed : 20 MHz good enough
  - ADC power directly proportionnal to speed
  - Could also use Wilkisons -> more bits
- Remove TDCs ?
  - Probably not needed for Lar
  - To be studied for Si
- Lower data output speed (320M)



CALOROCs: block diagram and interfaces

- CALOROCs will have the same interfaces (comparable to CMS H2GCROC *):
  - Fast command to dynamically control the ASIC
  - I2C to set the parameters
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)

© F. Dulucq



Fast commands	Value
Idle	00011
External trigger	01101
ChipSync	01110
BCR	10101
EBR	11001
Link-sync-ROC or Link-reset-ROC	10110
Calibration int or ext	11010

CALOROC1A or 1B

4b-data Header	2b Mode	Dh	24b Timestamp	1
4b-data Header	8b 0	Dh -d	Dh -h	18 channels Hit map
2b Gain	10b ADC$_{-1}$ - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
2b Gain	10b ADC$_{-1}$ - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
⋮				
2b Gain	10b ADC$_{-1}$ - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
CRC				
Idle/Sync Header	28b default IDLE Pattern			

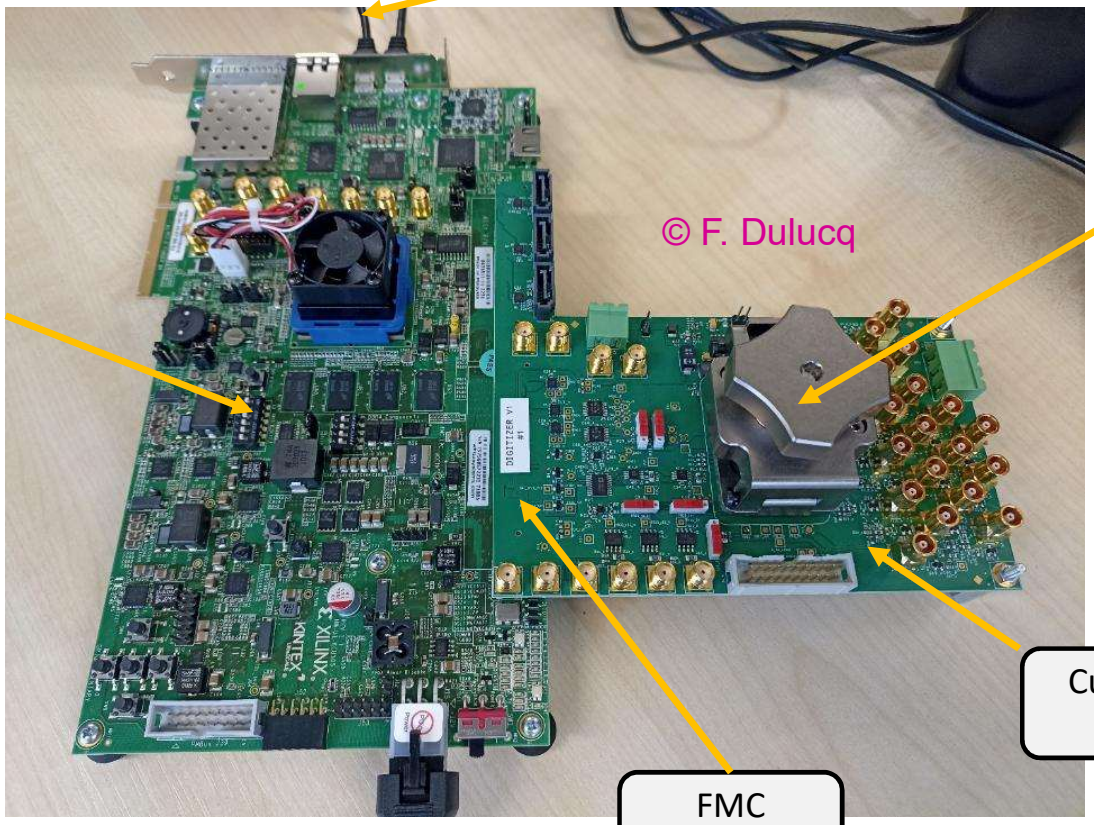
* CERN EDMS ➔ https://edms.cern.ch/document/2954073/1

Test System for Characterization

- CALOROC characterization motherboard under design at OMEGA:
  - Originally developed for HGCROC and the HKROC
  - Well-known at OMEGA and LLR (firmware based only)
  - Compatible with KRIA motherboard (CERN) but software + firmware needed

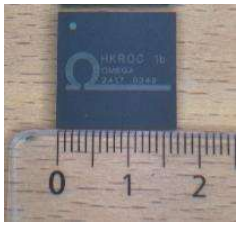
Python scripts

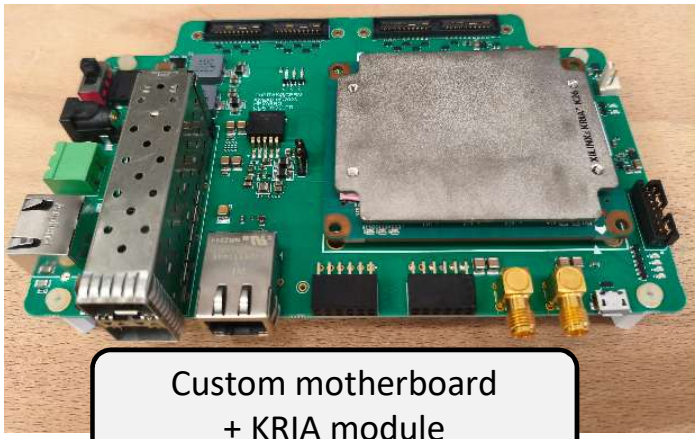
Monitor
Program
Test



Commercial
KCU105 board

CALOROC
BGA socket





Custom motherboard
+ KRIA module

Custom CALOROC
motherboard

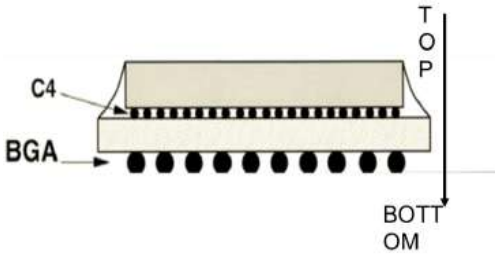
FMC
connector

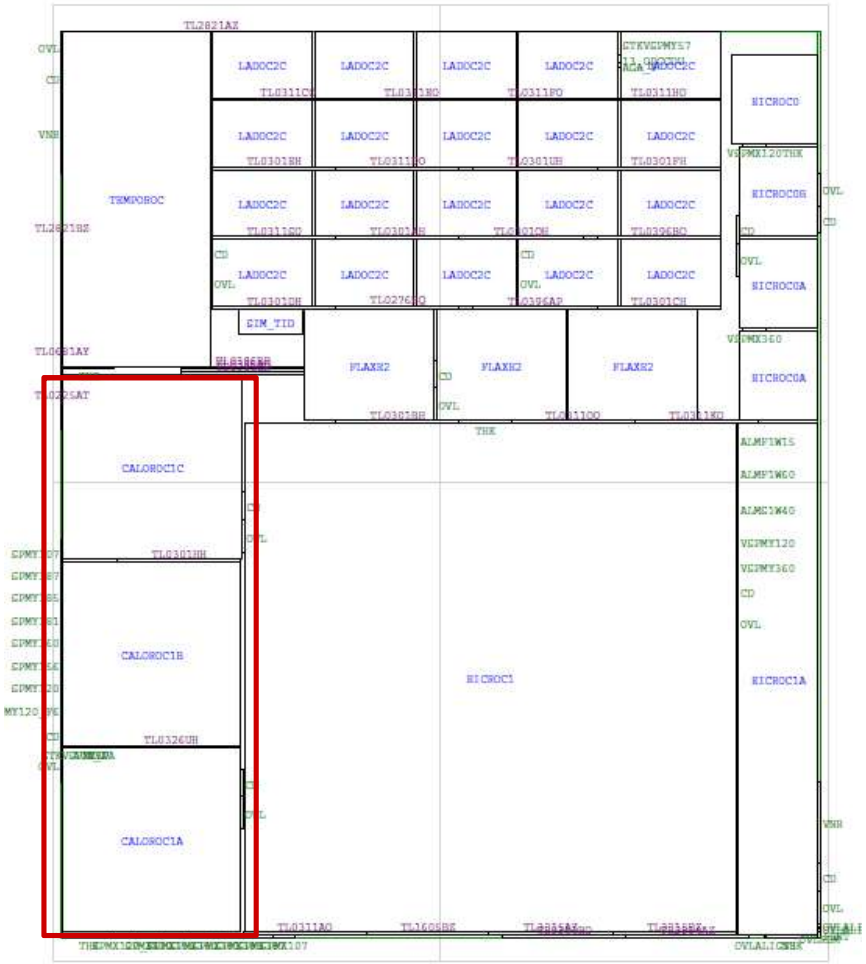
Conclusion

- Importance of joint optimization detector/readout electronics

- Trend to reduce power and data volume
  - Pileup will be less of an issue
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)

- CALOROCs first prototypes for DRD6/EIC next calorimeters
  - 1A/1B for SiPM readout
  - 1C for Si and LAr calorimeters
  - Engineering run submitted in september, expected for Xmas
  - BGA packaging in february 2026

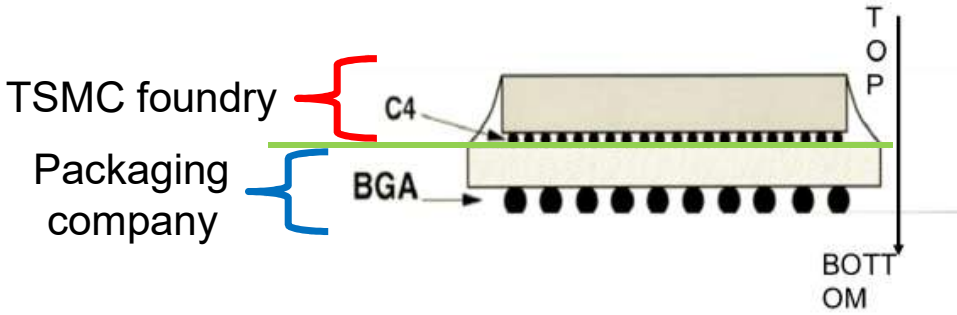




backup

CALOROC Packaging

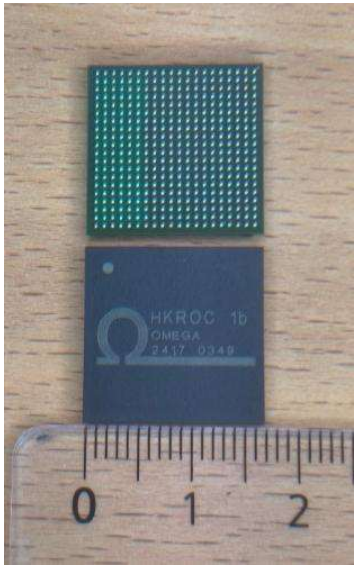
- CALOROC will have the same package as the existing HKROC:
  - JEDEC MO-216 – 17 x 17 mm BGA version
  - 400 balls with 0.8 mm pitch
  - Specific substrate (interposer) designed at OMEGA
  - **QR code** like HGCROC3



JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES	ISSUE: E	DATE: AUG 2003	MO-216

TABLE 3: SQUARE VARIATIONS – 0.80 PITCH

D / E	e = 0.80							
	MD/ME	N	SD/SE	VARIATION	MD-1/ME-1	N	SD/SE	VARIATION
14.00	17	289	0.00	BAJ-1	16	256	0.40	BAJ-2
15.00	18	324	0.40	BAK-1	17	289	0.00	BAK-2
16.00	19	361	0.00	BAL-1	18	324	0.40	BAL-2
17.00	20	400	0.40	BAM-1	19	361	0.00	BAM-2

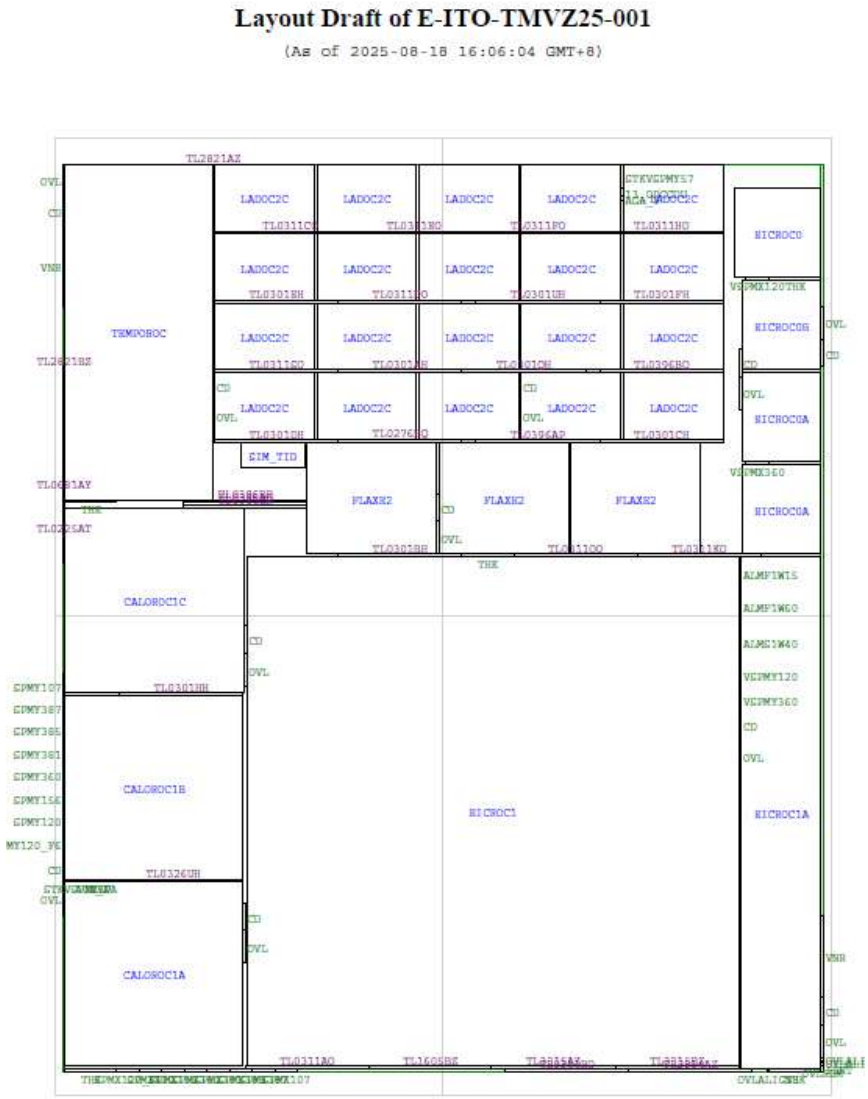


EICROC reticle 2025

- TSMC now requires to fully populate the reticle of 24x32
  - Cost ~300 k€

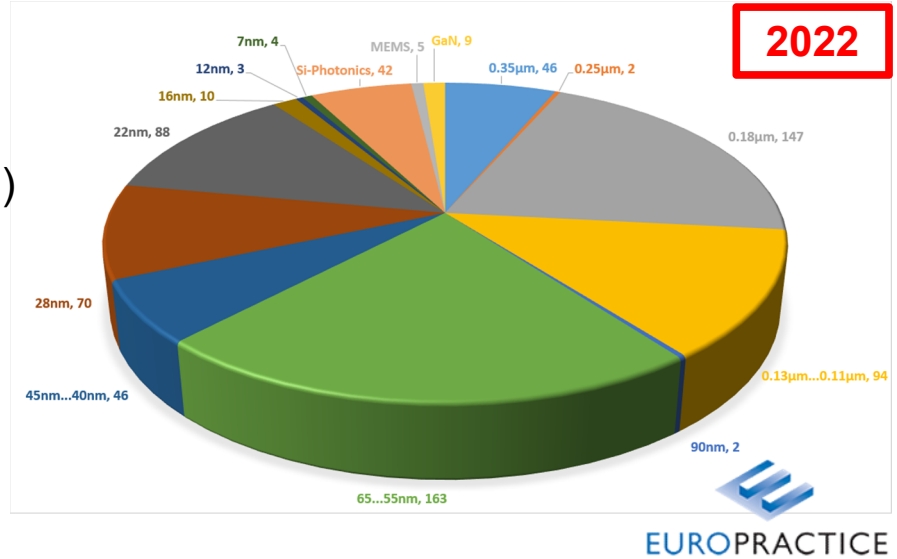
- For EIC we have
  - 1 EICROC1 32x32
  - 1 EICROC1A 4x32
  - 3 EICROC0/A/B 4x4
  - 3 CALOROC1A/B/C
  - ~70% of reticle area
  - EICROC1 is 40% of reticle area
  - gds files loaded end of may

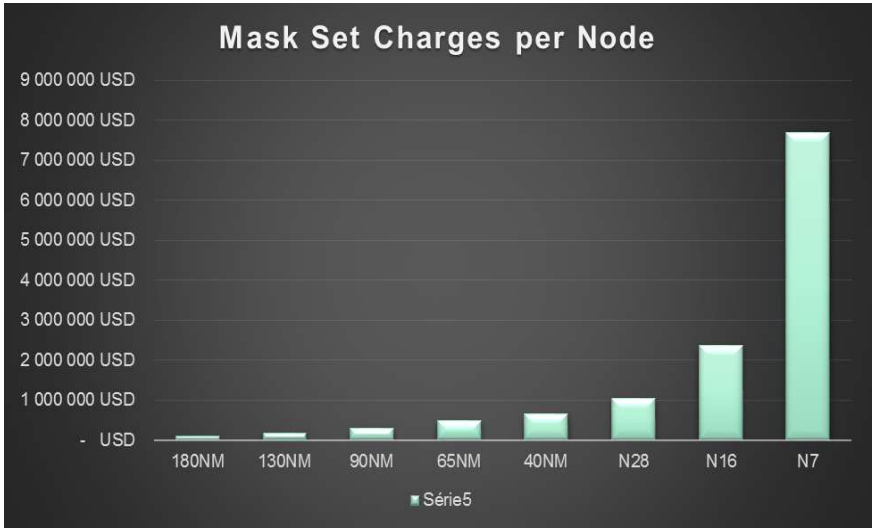
- Still administrative issues delaying the start of fabrication



Technology choice for mixed signal ASICs

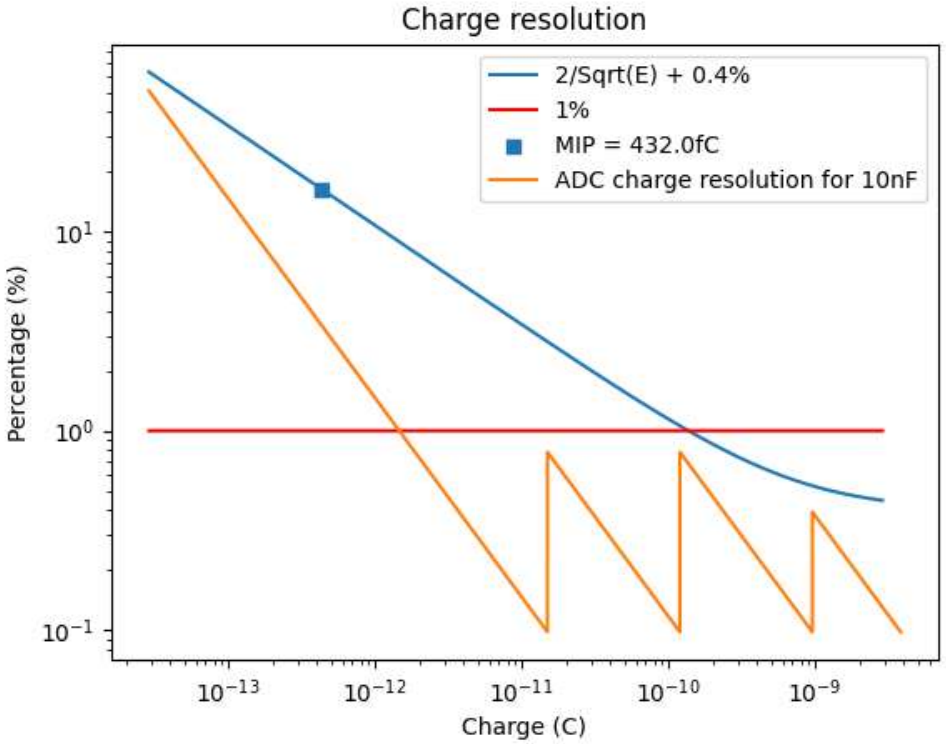
- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?
- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run





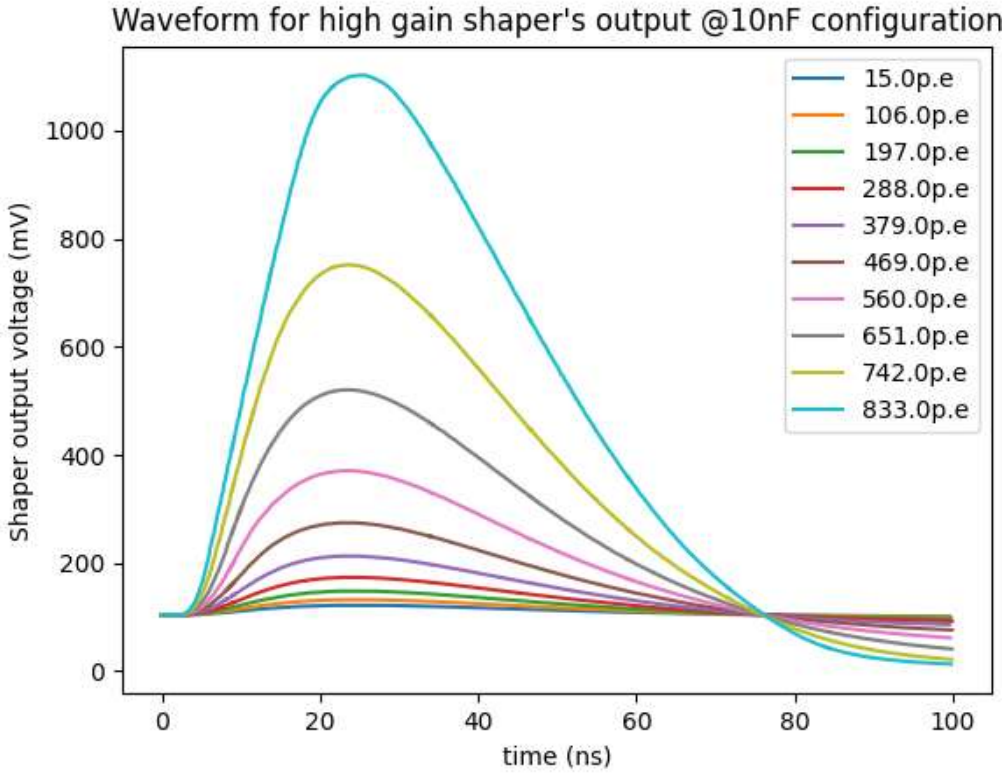
CALOROC1B: Dynamic range and resolution

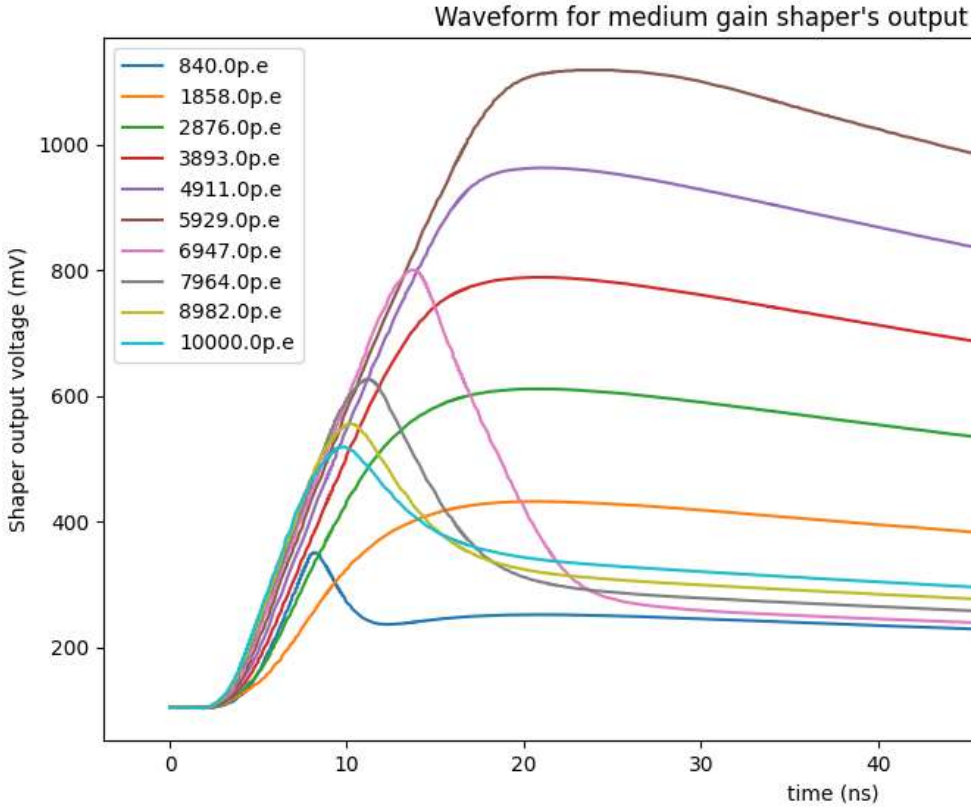
- The SiPM configuration has a direct impact on the dynamic range
  - The highest measurable charge is determined by the SiPM input capacitance.
  - The ratio between the highest and the lowest measurable charge is constant.
- 10b resolution and 16b dynamic range
  - With a 10b ADC and 4 gains (2b) we have a resolution of 16b
  - The measured charge is in the format of $10b * GainRatio^{2b}$
  - The gain ratio can be adjusted to increase the dynamic range in exchange for a lower resolution.
  - Using the highest resolution the dynamic range is 70k
  - Supposing 1MeV = 1p.e for the 4 SiPM setup this should give us a dynamic range of 1.5MeV (noise floor) to 100GeV



CALOROC1B: Charge and time simulations

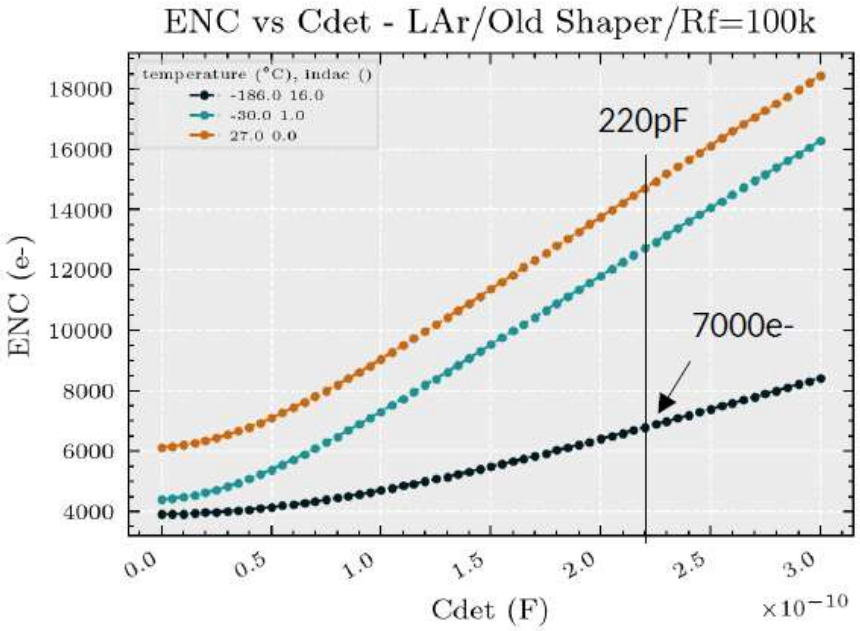
- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 10 nF

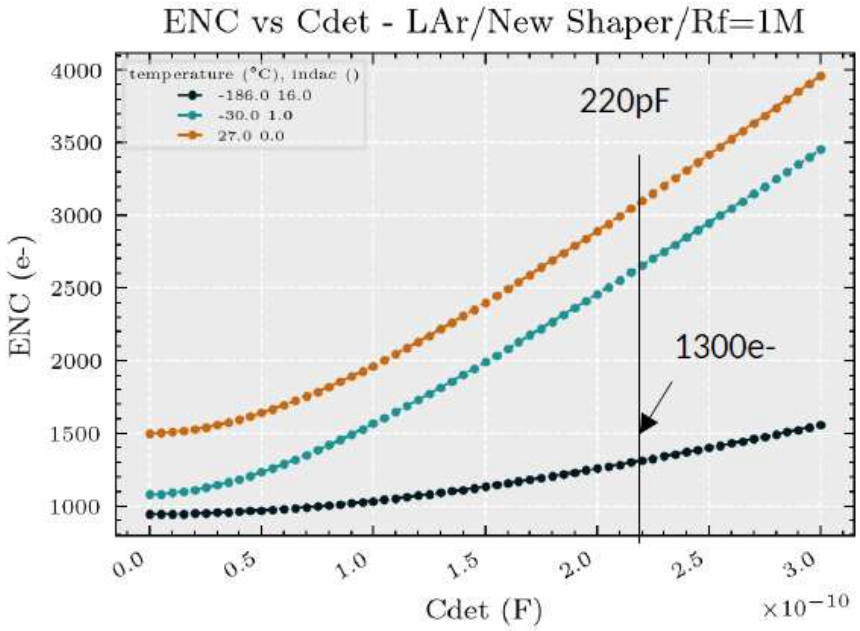




Slower Shaping

Higher Feedback R





HGCROC (CMS HGCAL)

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

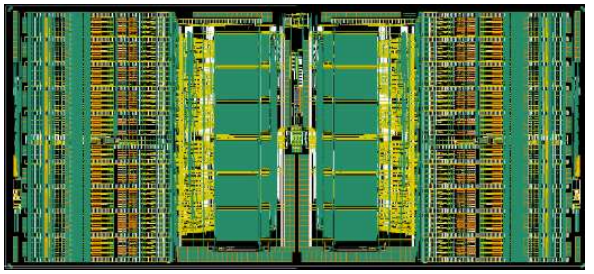
Control

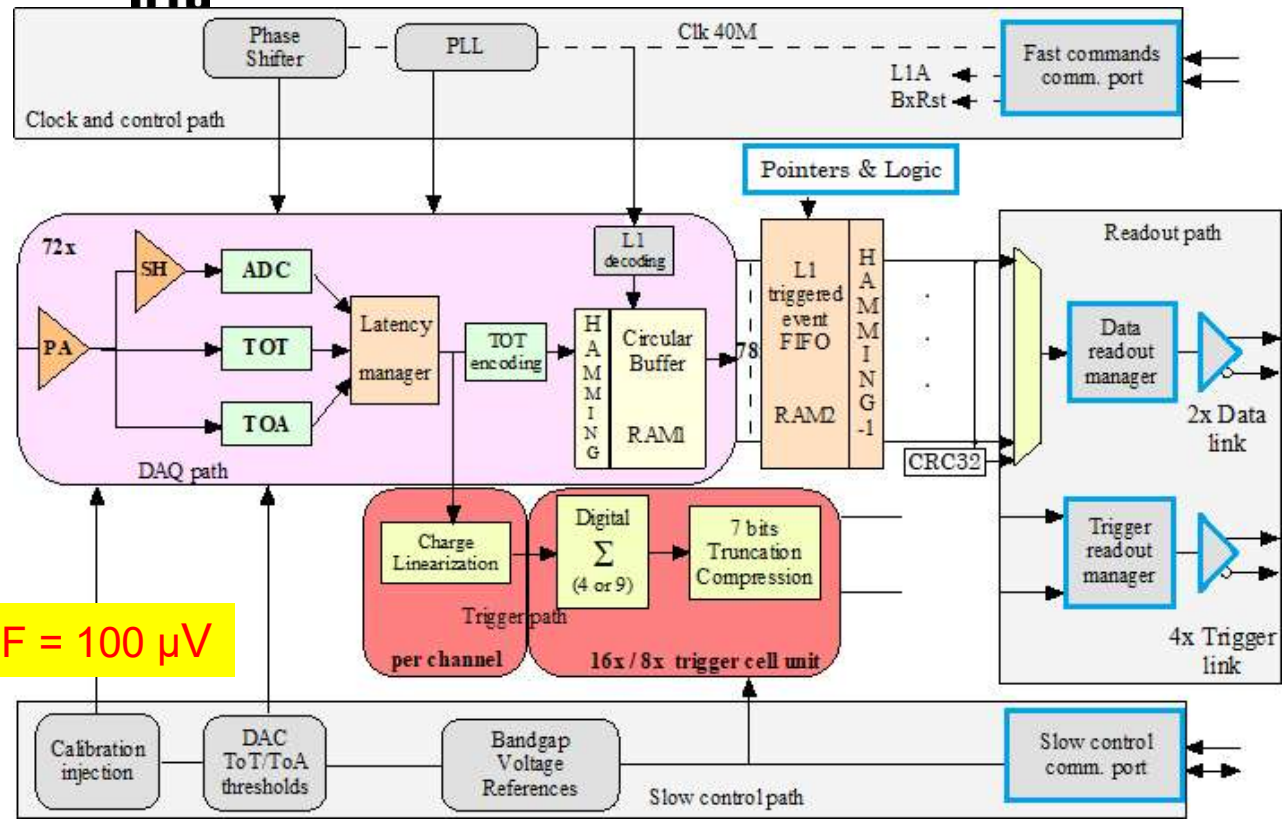
- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks

- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

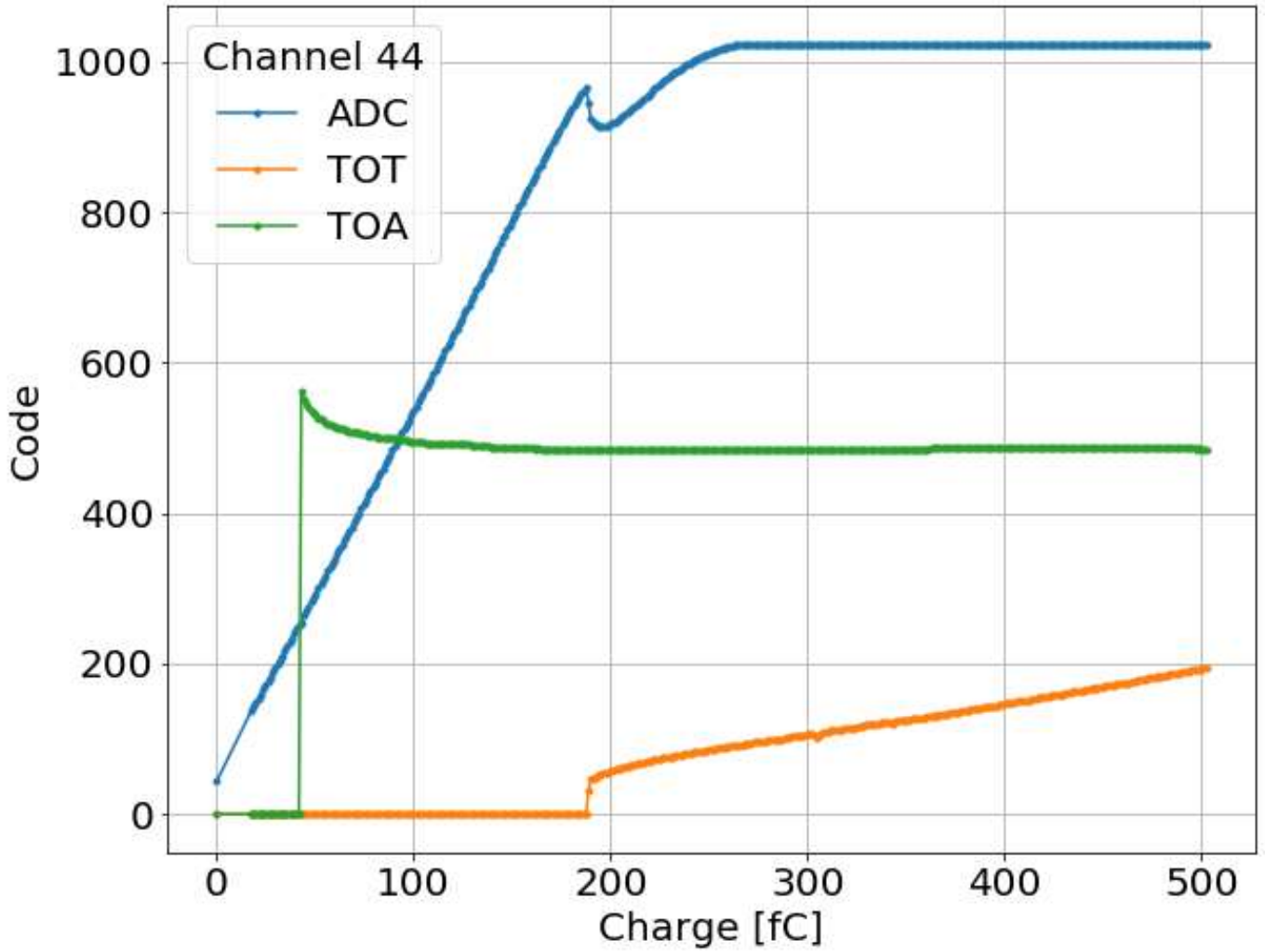
$Q_{MIP}/Cd \sim 3\ fC/30\ pF = 100\ \mu V$



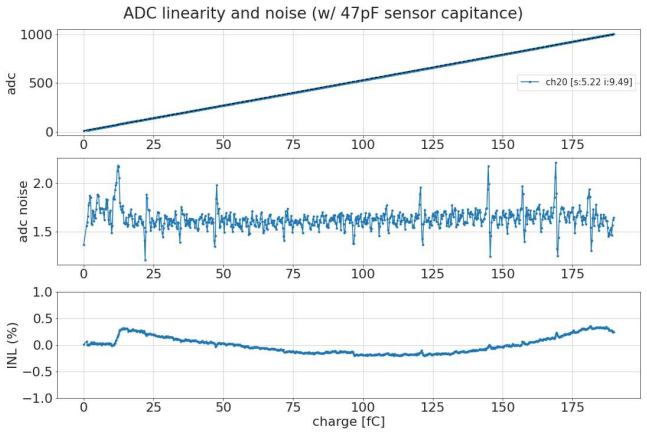


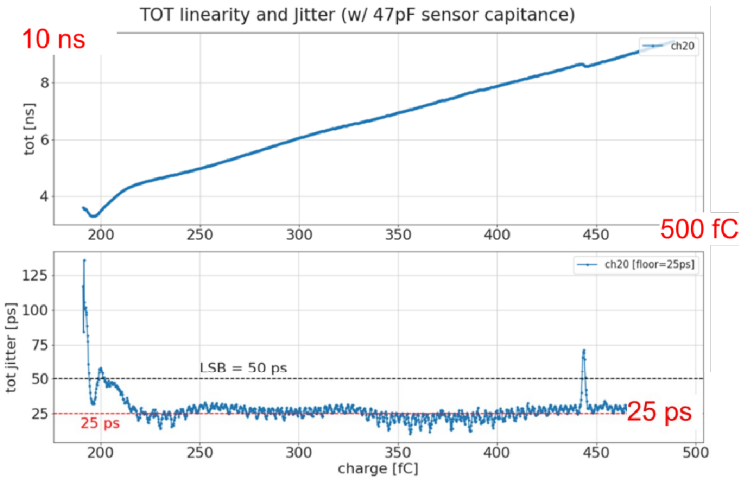
Handling the dynamic range : ADC and TOT

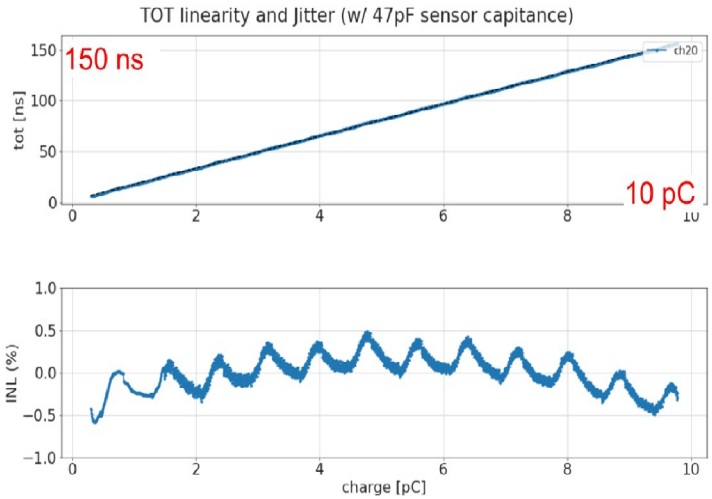
- ADC range 0 - 200 fC
- TOT range 200 fC - 10 pC
- Non-linear inter-region
- But 200 ns dead time

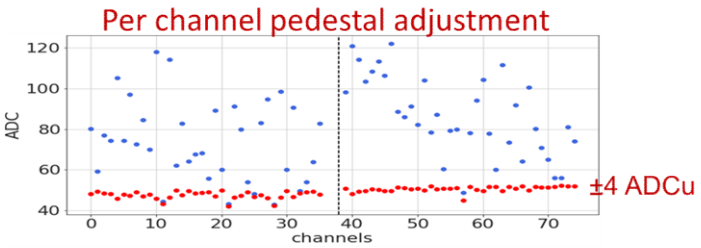


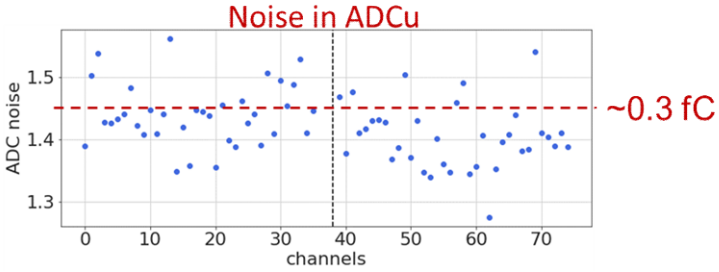
Performance

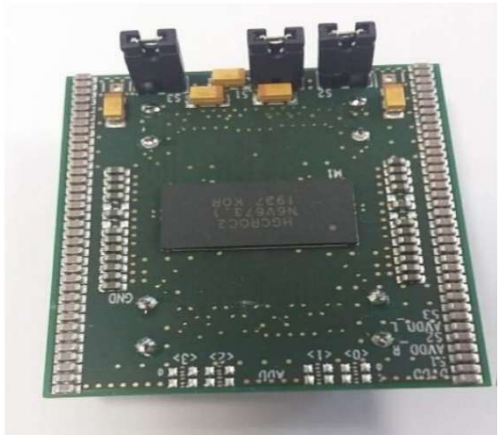


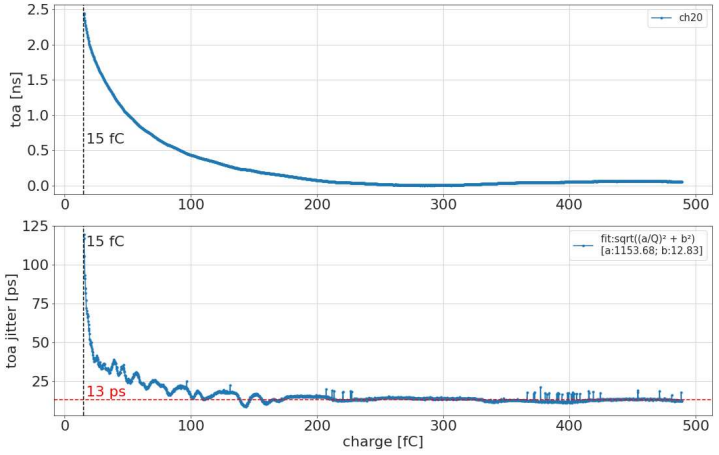












Zoom on timing

- ~2.5 ns time walk, 13 ps jitter for Q>100fC at Cd = 47 pF
- Fits also well MCPs for PID @EIC (HRPPD)