

The IDROGEN System

A high data rate acquisition system synchronized by an enhanced White Rabbit node

- IJCLab : Scientific themes : Astroparticles, Astrophysics & Cosmology, Nuclear physics, High Energy Physics, Accelerator Physics, Theory, Health, Energy
 - [Daniel Charlet](#), Antoine Back, Cédric Esnault, Christelle Soulet, Monique Taurigna, Chafik Cheikali, *Gaetan Seuillot, *Mathias Vecchio, *Sid Ali Cherrati
- Paris Observatory : Scientific themes : Time and frequency metrology, time and frequency transfer, inertial sensors, space-time reference frames, theory, epistemology
 - LTE : Paul-Eric Pottie, Michel Iours
 - Obs Nançay : Cédric Viou



Observatoire
de Paris

PSL



Station de
Radioastronomie
de Nançay

LTE

- The IDROGEN System
 - Master board
 - Additional functionalities
- Last results on different setup

IDROGEN mother board



IDROGEN Key concepts

- A new architecture where all signals generated by the board are synchronous with the master clock.
- In addition, the master clock can be synchronized by the WR protocol.
- In a network, all the boards are therefore synchronized to the grand master.
- High data rate acquisition system using standard protocols.
- Frequency generator.
- Fully re-configurable.



IDROGEN board v3

High speed data acquisition & Low phase noise WR node

- White Rabbit Design & development done by IJCLab (based on CERN schematic): Component upgrade and EMC design rules compliant → High stability timing distribution
- xTCA4.0 form factor board → Modularity

- Base on ARRIA 10 FPGA → High data rate transfer
- Standalone capability
- RTM extension boards
- FMC carrier board

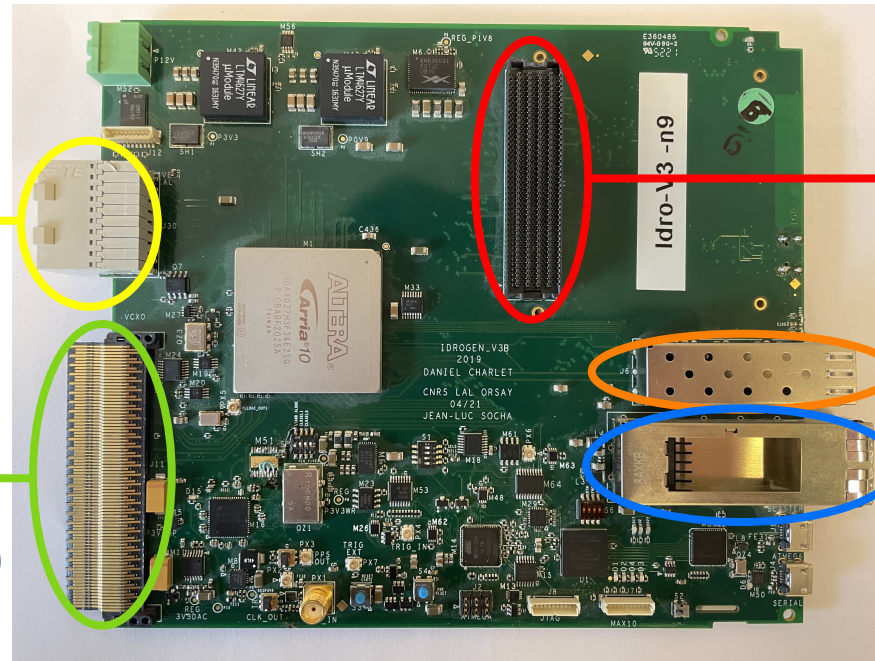
IDROGEN Enhancements

- System frequency
- PLL selection
- VCXO Frequency
- Input frequency for DDMTD
- Tx/Rx routing equalisation

RTM Connector

μTCA connector

- Ethernet 1Gb/s
- **PCIe Gen3x4 (8Gb/s)**



FMC Slot (ADC, DAC, clock synthesis, ...)

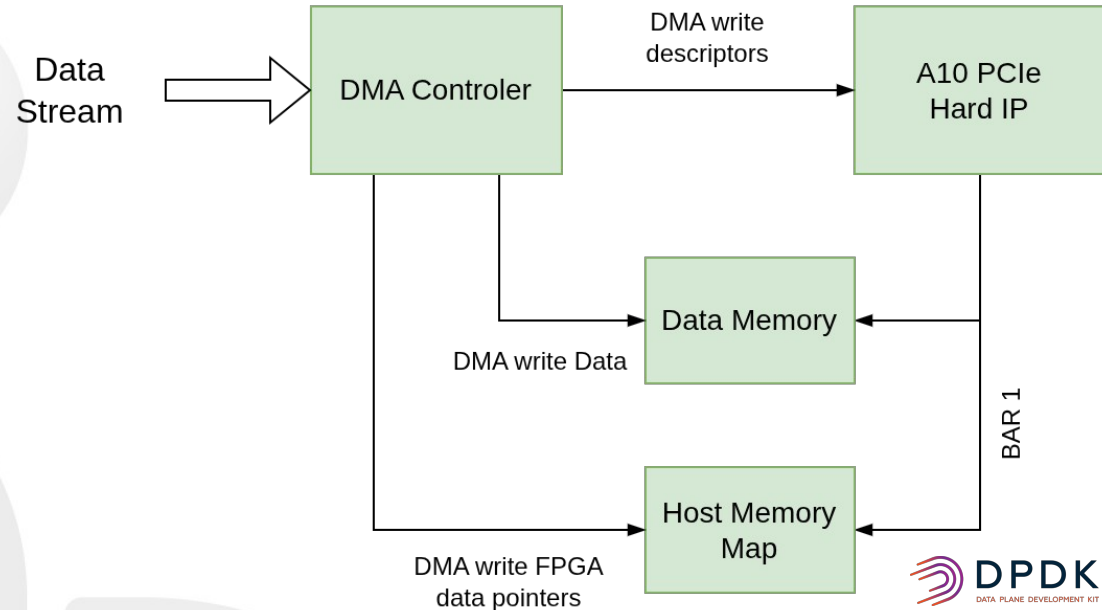
SFP+ connector for WR

QSFP connector for data transfer (Ethernet 1Gb/10Gb/40Gb, GBT, ...)



IDROGEN: Firmwares

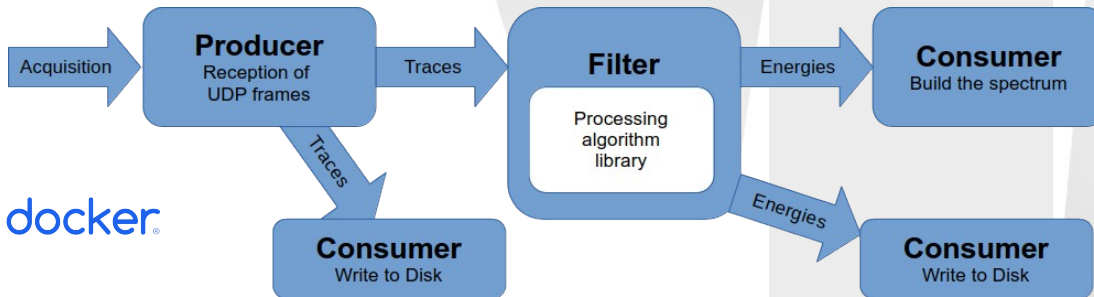
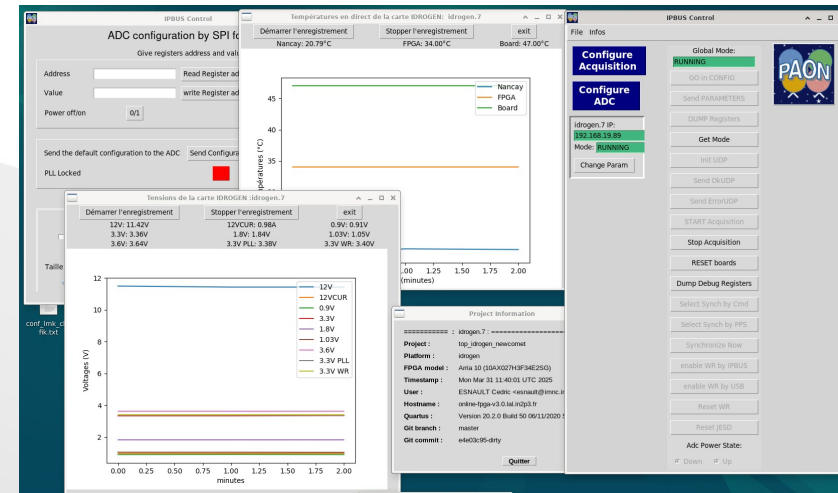
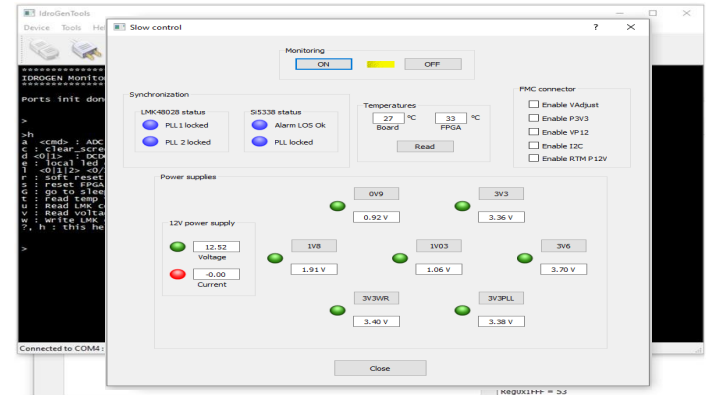
- Data transfer firmware
 - PCI-Express with DMA Gen3x4 (~25Gb/s)
 - GBT protocol (CPPM development for PCIe40)
 - IpBus 1G & 10G portage on Arria 10, from LPSC laboratory developments
 - UDP streamer 1G & 10G
 - Software C, Multi Jumbo frame by event
 - 2 x 10 Gb available, 40 Gb future development
- High speed ADC acquisition
 - JESD204B for (1G/500M/250M)
- Parallel 64 data acquisition
- White Rabbit core v4 & v5 porting on Arria 10
 - Master & Switch (on development)





IDROGEN: softwares

- Configuration GUI tools over USB and Ethernet (IPBus protocol)
 - Power, PLL, FMC and ADC configuration
- Monitoring GUI for power supplies and temperature monitoring
- Slow control library and tools (I2C, SPI, WR diagnostic, ...)
- Frame viewer
- Acquisition software
 - Based on DCOD framework
 - Implement a generic processing algorithm interface (loading a dynamic library)
 - Based on widely used technologies (Docker, DPDK)



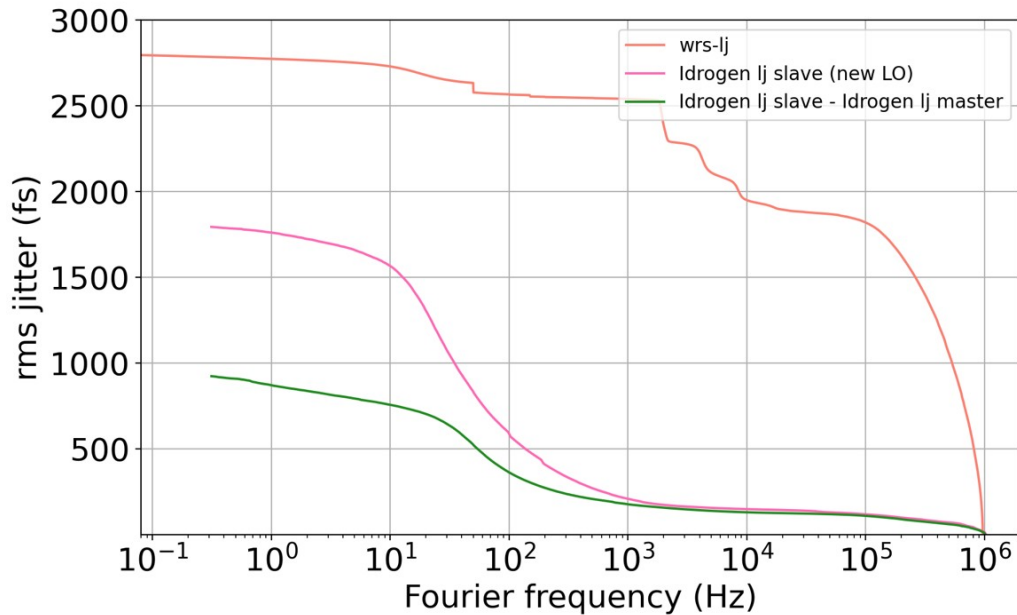
IDROGEN board: Timing performance



IDROGEN board performance

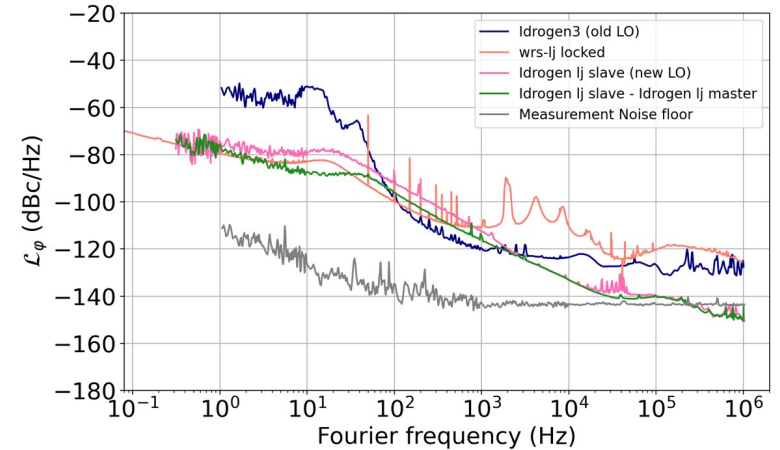
Phase noise measurement

Integrated jitter according to integration range



Variation of lower bound of integration range.
Upper bound fixed at 1 MHz

Phase noise measurement



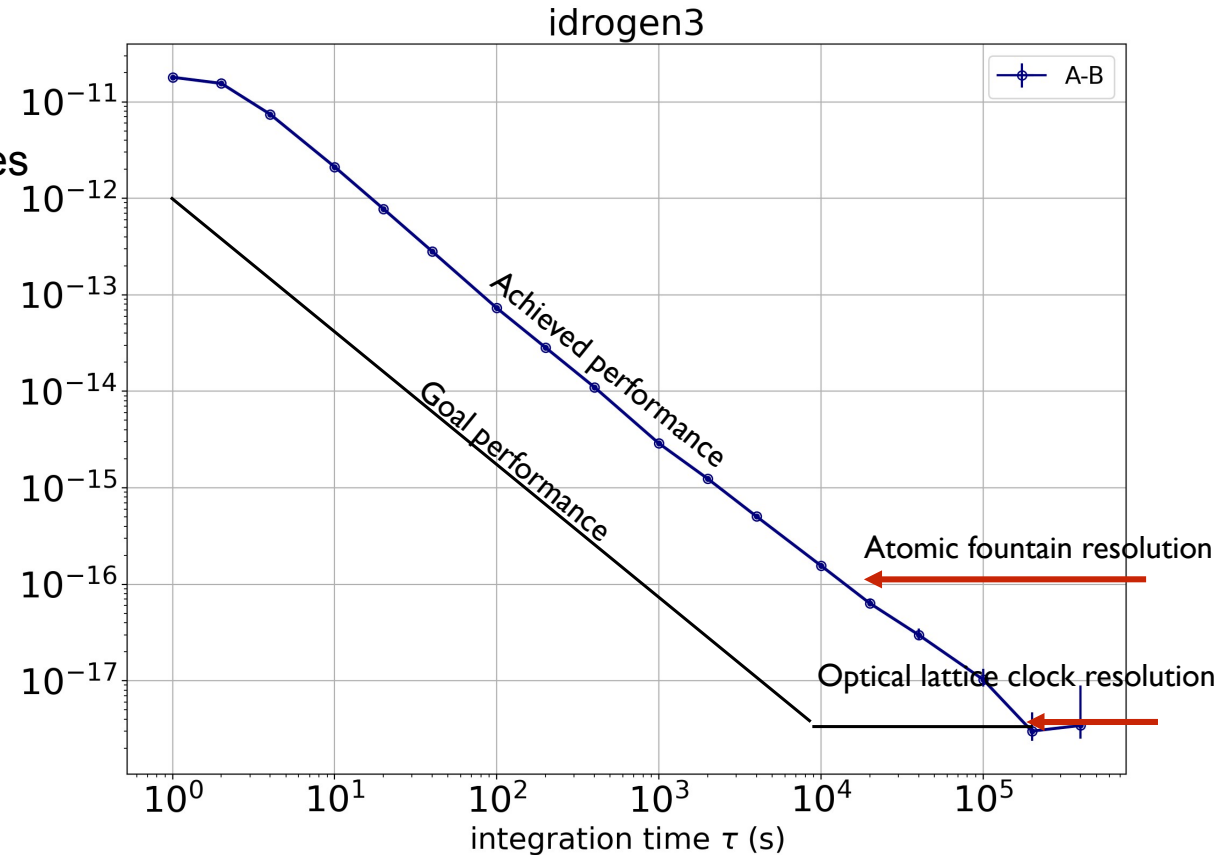
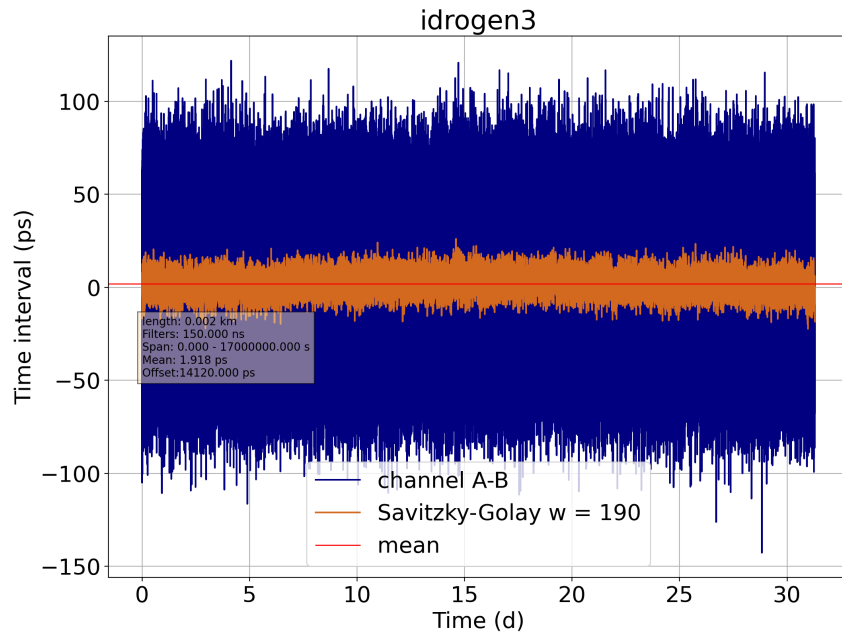
	1	10	100	1,000	10,000
wrs-lj	2 246	2 191	1 984	1 075	1 075
S	1 757	1 557	563	110	110
S-M	866	751	351	94	94
GM	445	439	432	129	129

Table 1: Integrated rms jitter expressed in fs for Idrogen and a wrs-lj, for integration bandwidth up to 100 kHz

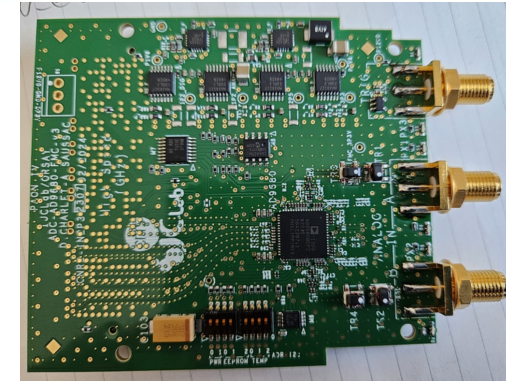
IDROGEN BOARD: 4x better than Switch Low Jitter from Safran/Seven Solution



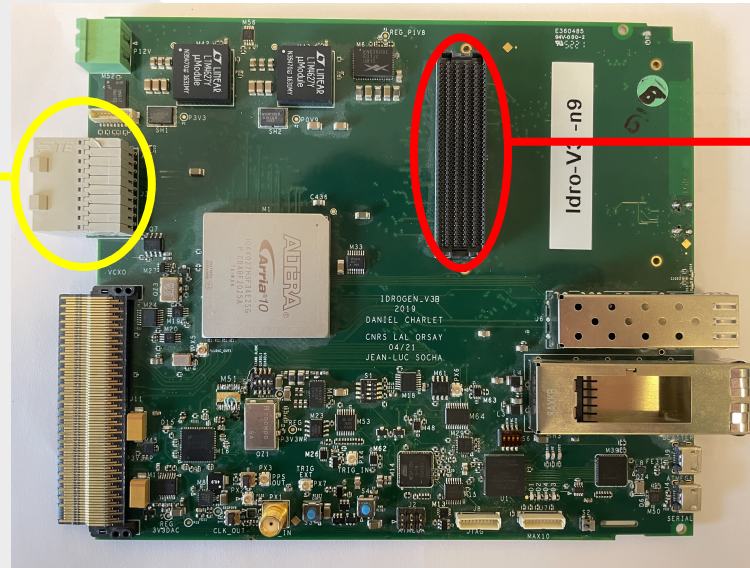
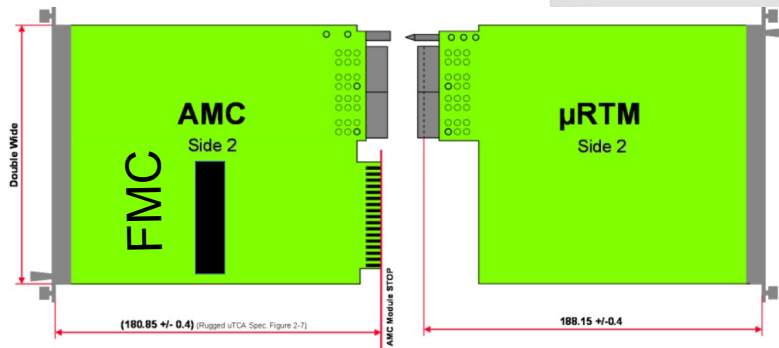
- PPS time difference between two independent IDROGEN3 boards
- Excellent long term stability : $\sim 3E-18$
- On-going work: improve short term performances
-



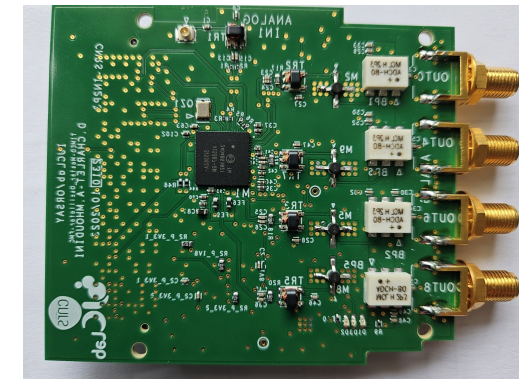
IDROGEN extension boards



RTM Connector



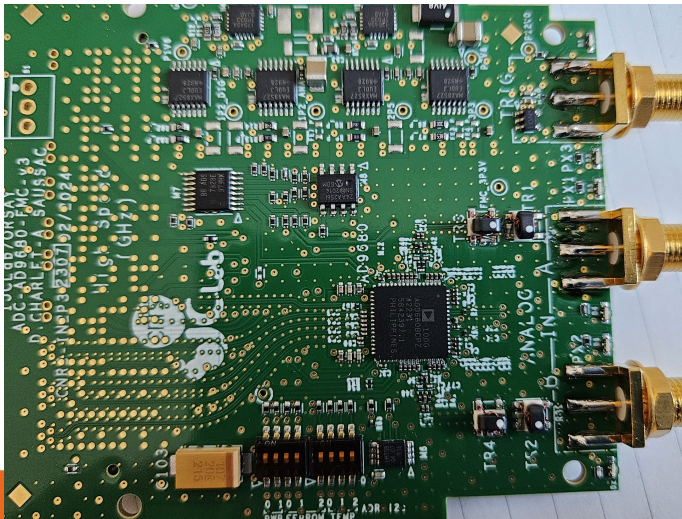
FMC Slot (ADC, DAC,
 clock synthesis, ...)





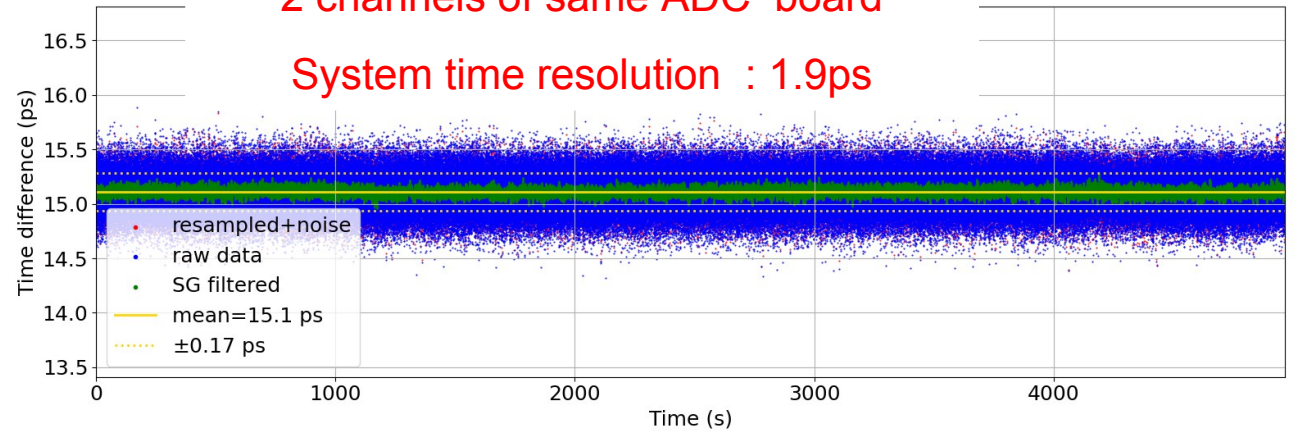
1GSPS ADC board: Synchronization performance

- Bandwidth (single board):
~500MHz (1GHz → 1.5GHz)
- 2 IDROGEN boards synchronized by WR
- 2 channels 1GSPS 14b ADC
- Same RF signal (312.5MHz) split on boards
- FFT 8k point
- Cross correlation



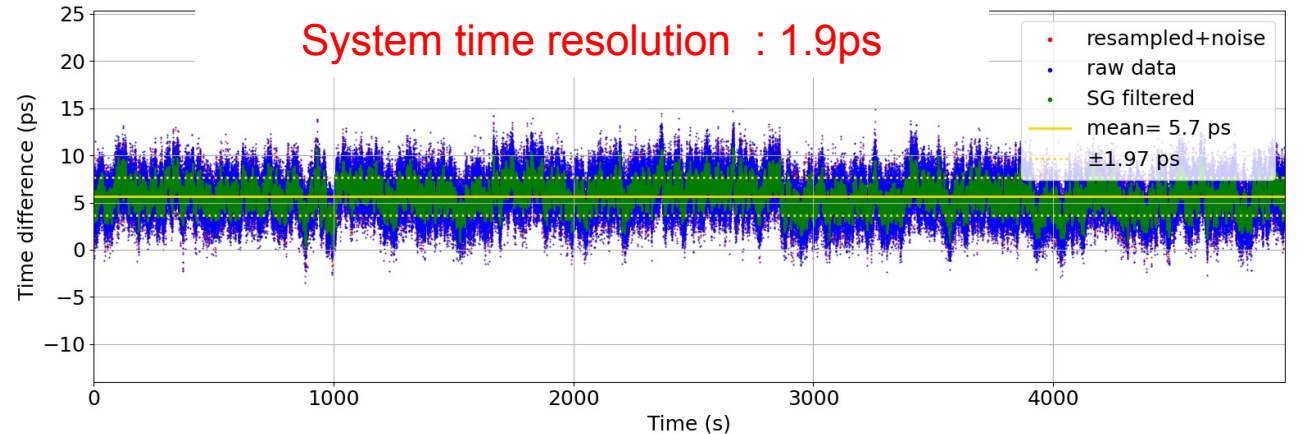
2 channels of same ADC board

System time resolution : 1.9ps



Two IDROGEN board

System time resolution : 1.9ps

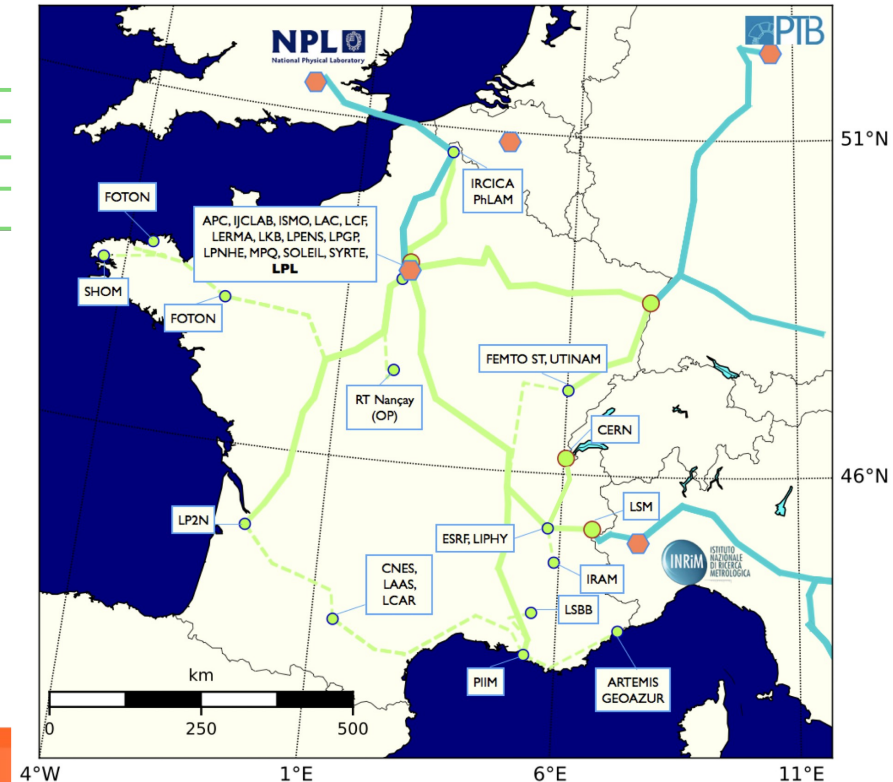
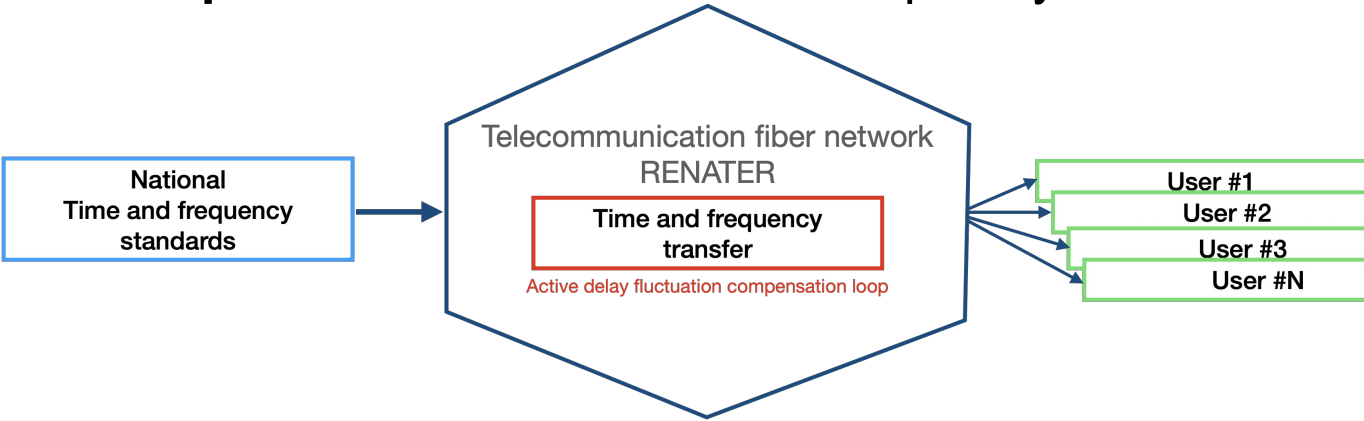




T+REFIMEVE

a new research infrastructure to disseminate time and frequency standards on active telecommunication network of RENATER (scientific data network)

Concept : Dissemination of time-frequency references by optical fiber



Signal to be provided by T-REFIMEVE

		Stability or relative stab. @1s	Stability or relative stab. @1day	Uncertainty	
				routine	dedicated
Radiofrequency	1 st pillar - 10 MHz (White Rabbit)*	1,00E-12	1,00E-15	1,00E-14	1,00E-15
	2 nd pillar - 1 GHz	1,00E-13	3,00E-16	1,00E-14	2,00E-16
Time	1 st pillar (White Rabbit)*	1 ns	1 ns	10 ns	10 ns
	2 nd pillar	20-50 ps	500 ps	10 ns	2ns to 100ps [§]
Optical frequency (194,5 THz/1542 nm)	Today	1,00E-15	3,00E-16	1,00E-14	2,00E-17
	Expected progress in 5 years	1,00E-16	2,00E-17	1,00E-14	1,00E-18

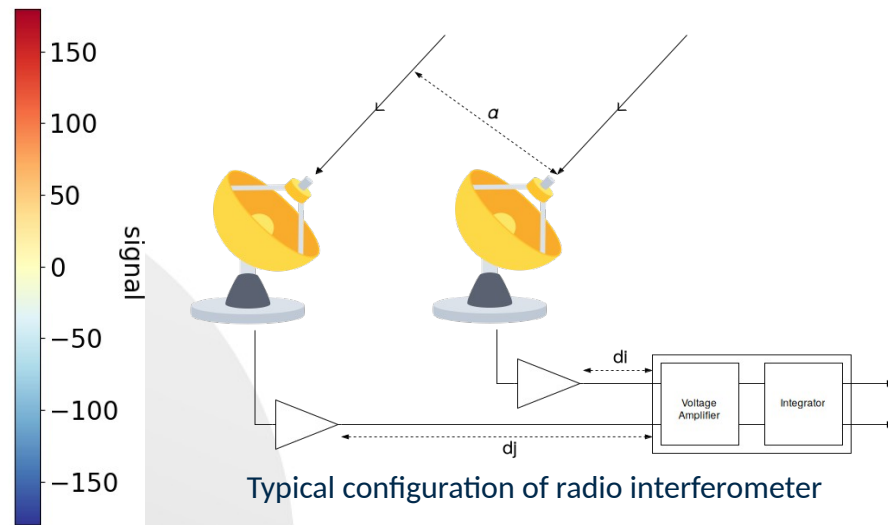
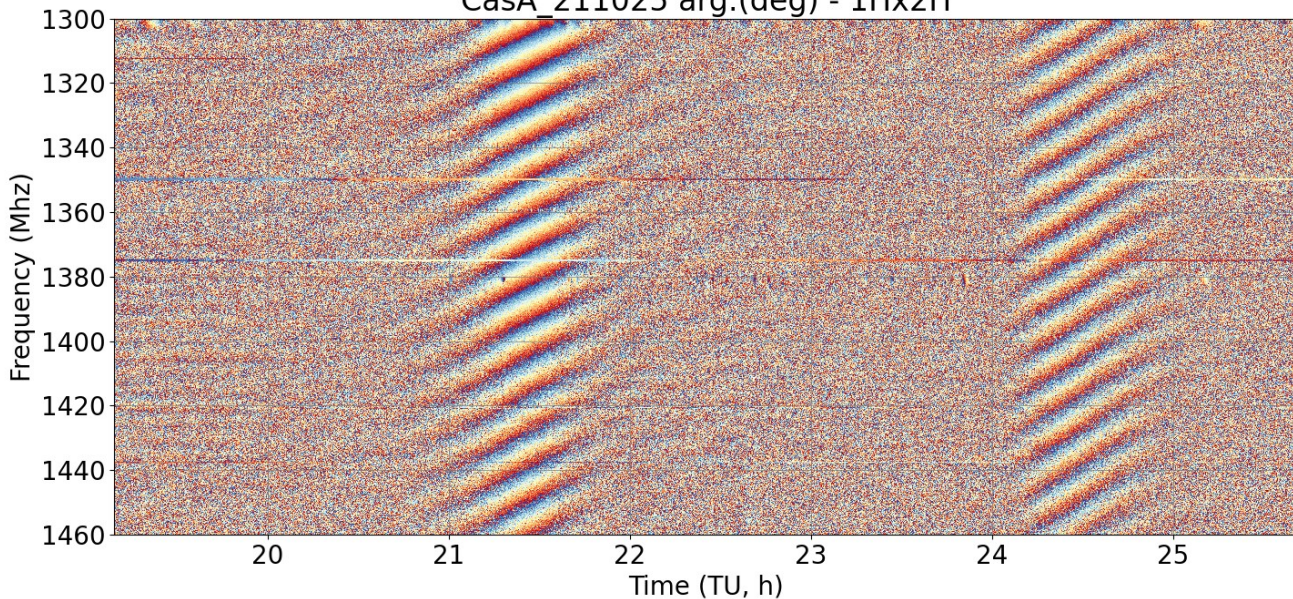


PAON IV Radio Interferometer

- Acquisition by IDROGEN board and ADC 1GSPS
- Phase difference between 2 antennas
- Synchronization by REFIMEVE network
- Paris observatory UTC(OP) connection
- Fiber link length $\sim 300\text{km}$
-
-



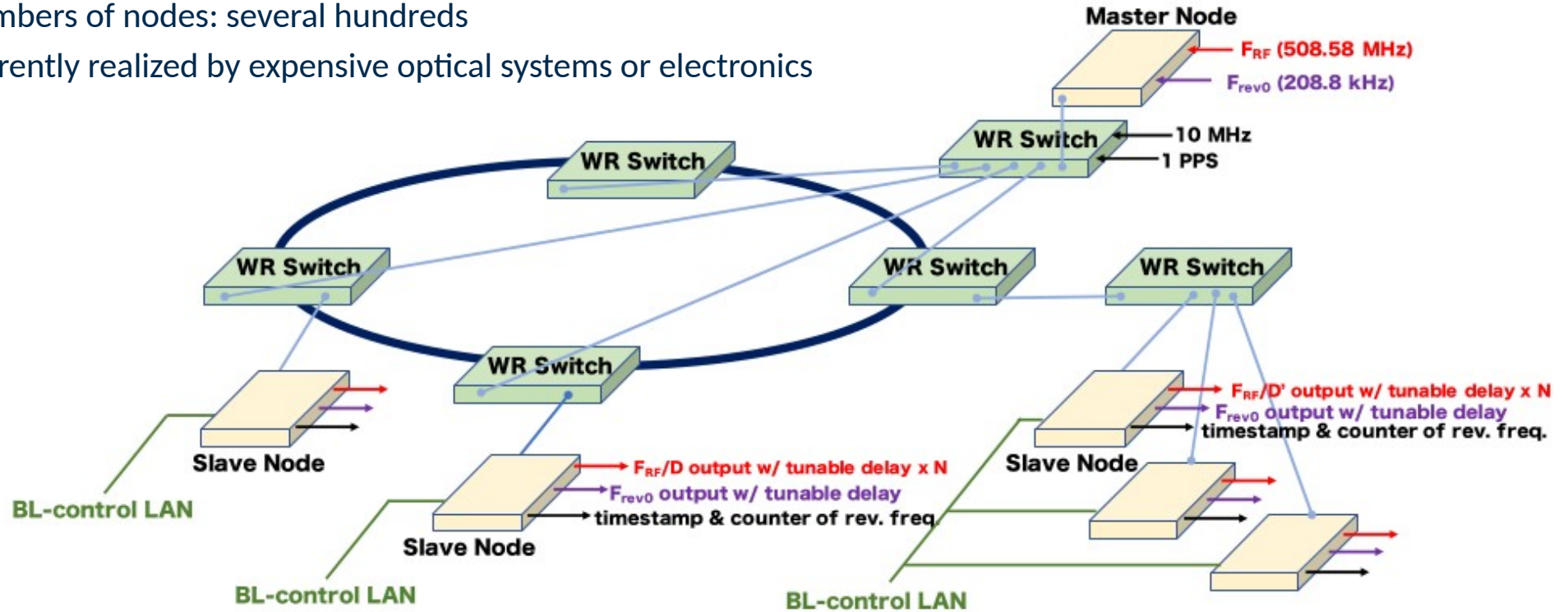
CasA_211025 arg.(deg) - 1Hx2H





Accelerator : Master oscillator distribution

- Real-time communication system: tight time constraints
- Jitter stability ($< 1\text{ps}$)
- Monitoring synchronization
- Long distances between nodes ($> 1\text{km}$): long transmission delays
- Numbers of nodes: several hundreds
- Currently realized by expensive optical systems or electronics





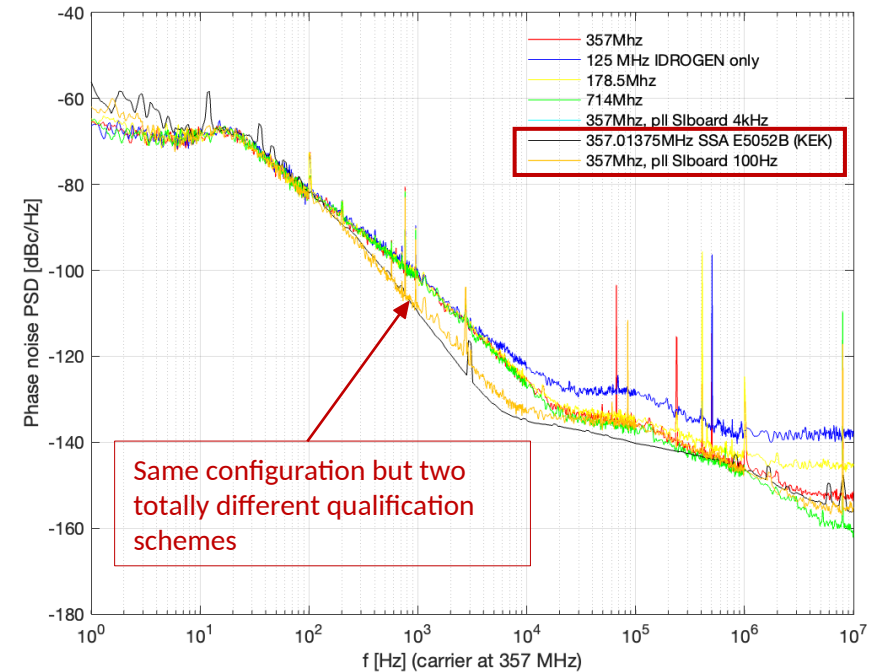
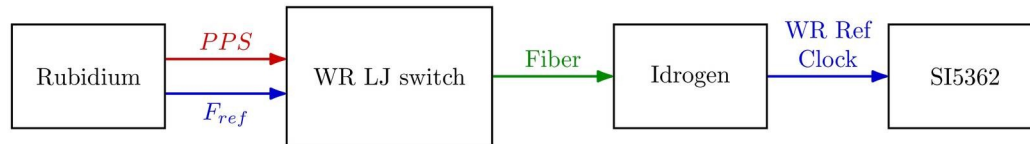
Clock synthesis for accelerators

Fractional PLL (FPLL) for accelerator synchronization (SI5362)

- Generate frequencies, disciplined by WR clock, from 10kHz to 2.75GHz, with 1 Hz resolution.

SI5362: Phase noise measurement

- Tests performed at IJCLab and KEK (SuperKEKB and ATF);
- Phase noise measured for various different output frequencies and input filters, re-scaled at 357 MHz: 1.7ps RMS jitter;
- Consistency of KEK and IJCLab measurements.



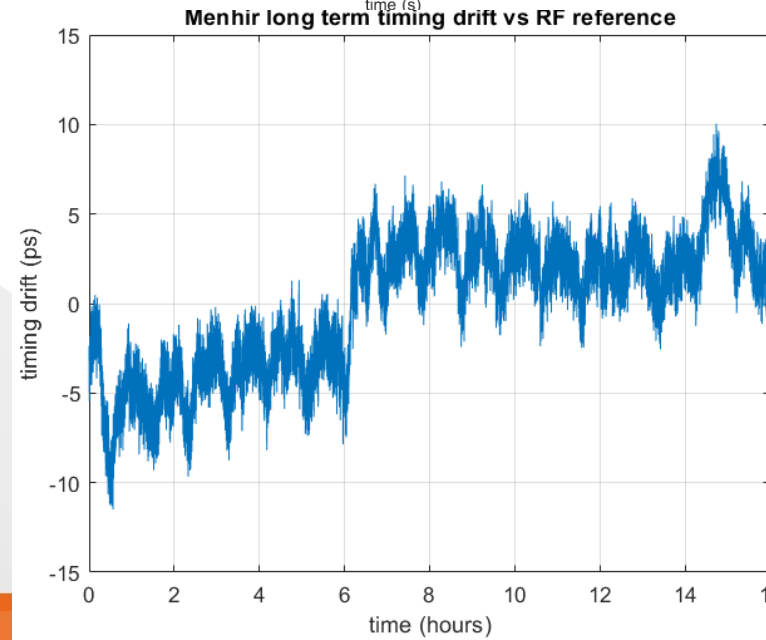
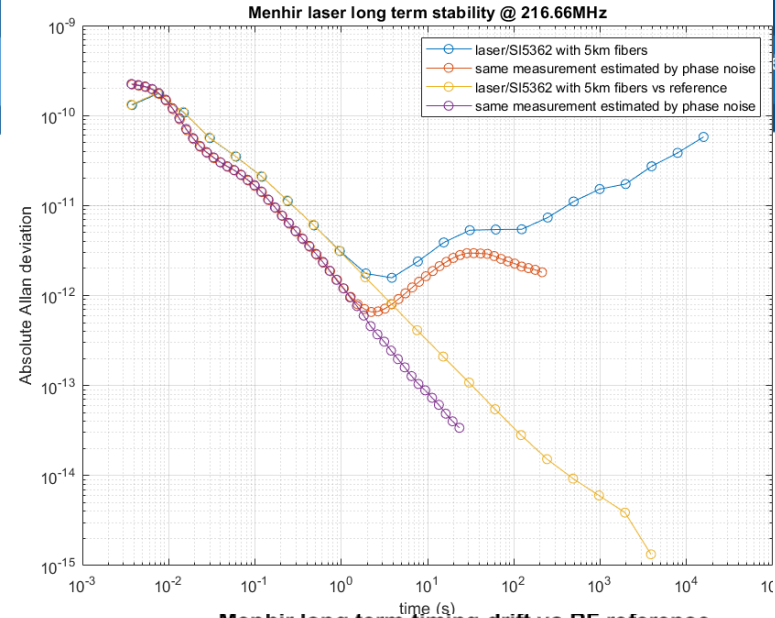
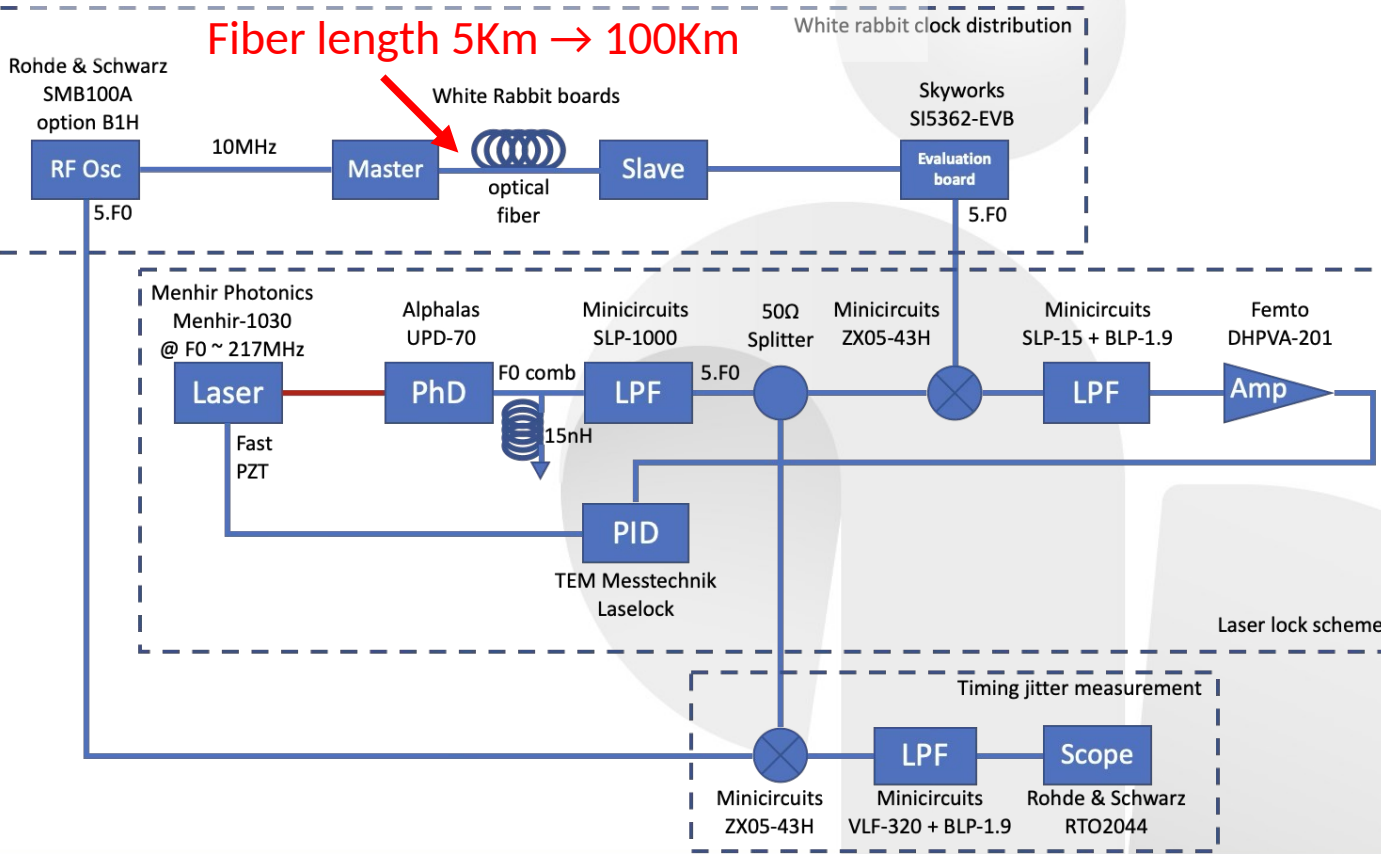
Funded by
the European Union

The research leading to these results has received funding from the European Union's Horizon Europe MSCA under grant agreement no. 101086276

Lazer synchronisation

IDROGEN 1 : GM → IDROGEN 2 slave

Fiber length 5Km → 100Km





IDROGEN: roadmap and future directions

- IDROGEN_V4
 - Development for Q4 2025, mass production end 2026
 - Replacement of obsolete components
 - Versatility Improvement
- FMC-AD42JB69 (in development)
 - 4 channels 250MSPS 16bits
- FMC-ADC 3GSPS
- White Fox (Highly improved White Rabbit)
 - Development with LTE
 - Sub 100-fs performance (prototype in development)
- Improve short term performance (ongoing development)
- 10Gb/s White Rabbit firmware
- IDROGEN_v5
 - New FPGA family AGILEX



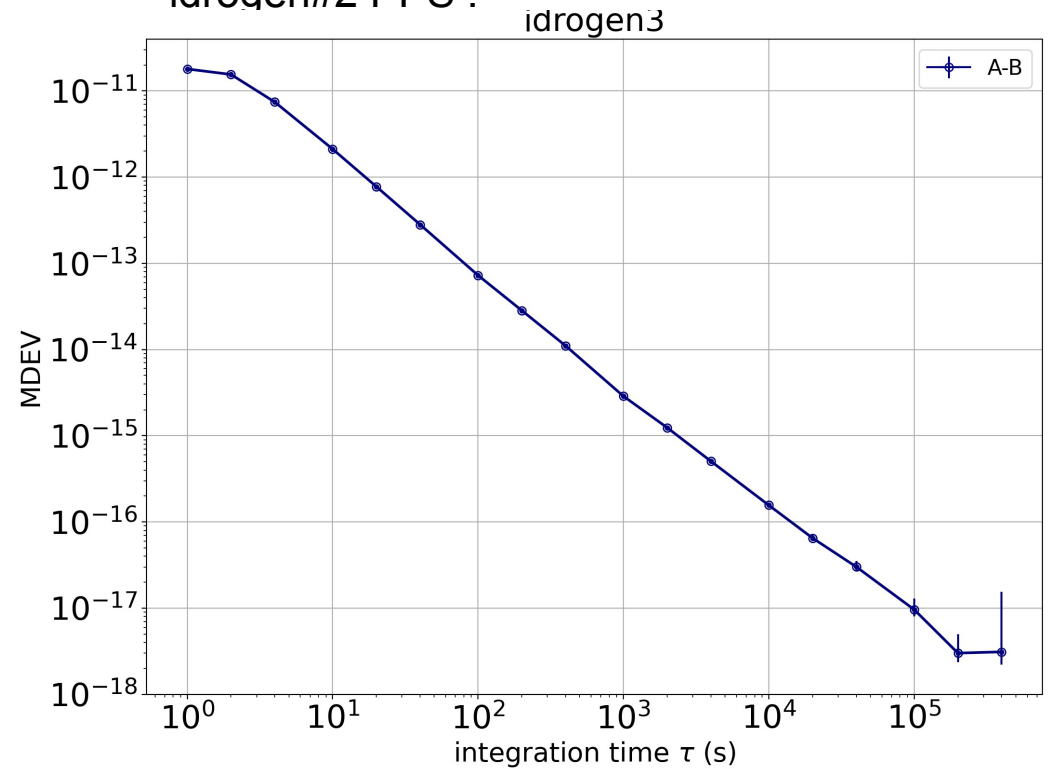
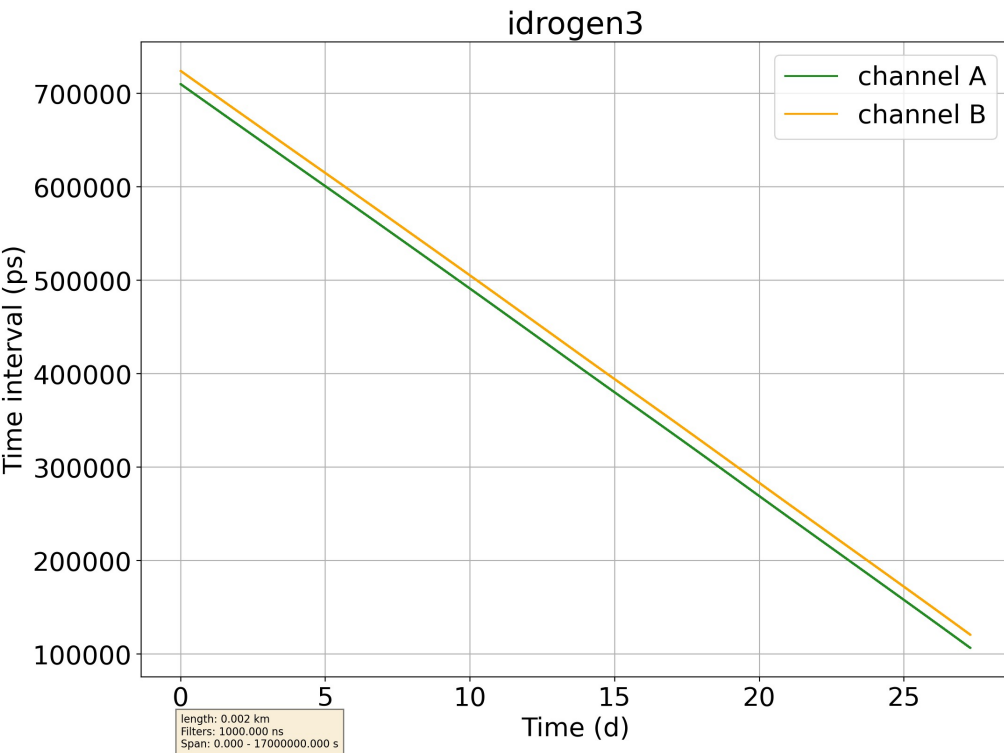
Conclusion

- Very promising results with IDROGEN board (sub-picosecond RMS jitter)
- New board version (v4) to address component obsolescence
- New projects: CTAO-MST, NENUFAR (Nançay observatory), ATF LLREF, KEK accelerators, New Comet (Nuclear physics @ IJClab),....
- Focus on essential hardware development
- Development:
 - low-frequency phase noise (low frequency)
 - White Fox project (jitter < 100fs) for future applications (FCC, Einstein Telescope,...)



IDROGEN board performances

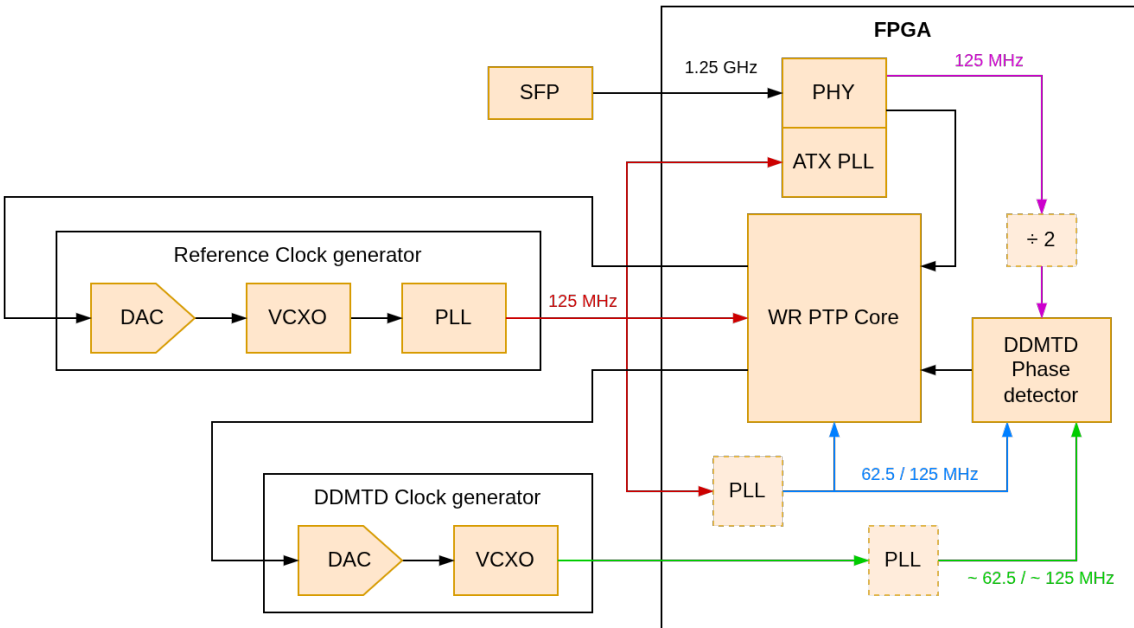
- the measurements were made by SYRTE (P.-E.Pottie)
- Measure the time interval between idrogen#1 and idrogen#2 PPS :





IDROGEN board : WhiteRabbit implementation

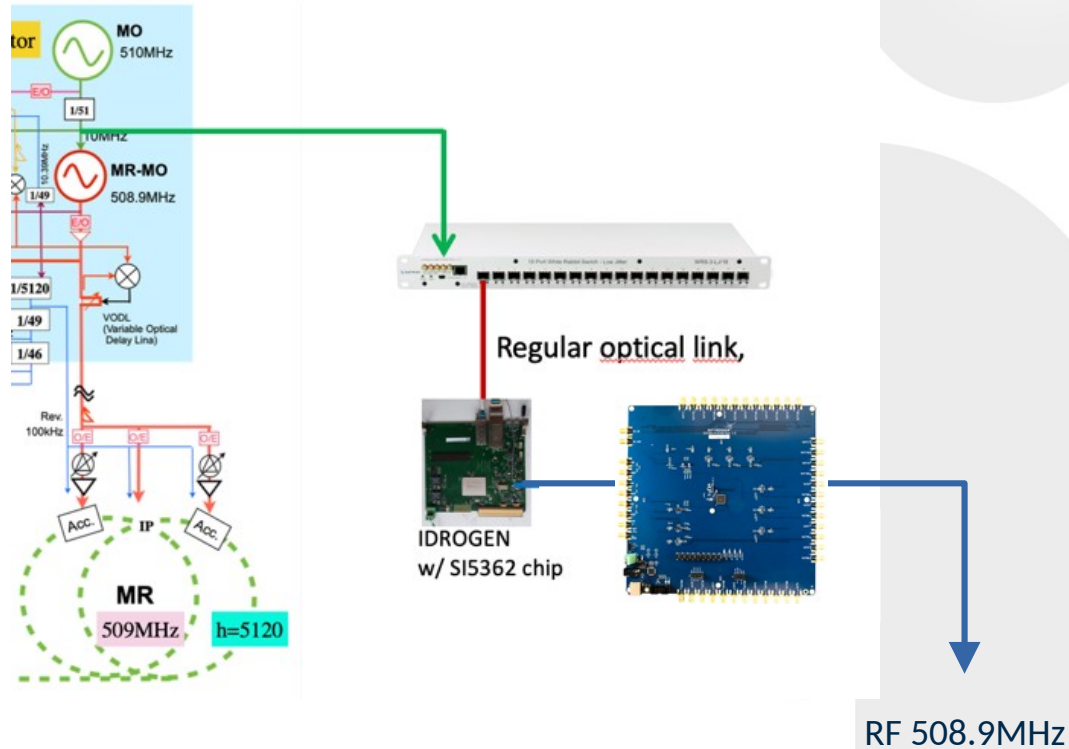
- Based on CERN open hardware with Enhancements
- Based on LMK4828 synthesiser
 - Ultra low noise clock jitter Cleaner with Dual Loop PLL
 - 90fs RMS jitter
- DDMTD internal of FPGA (placement with constraint)
- Two generated local clocks :
 - DDMTD source (comparison between WR master clock from SFP)
 - PLL source with phase adjustment
- IDROGEN Enhancements**
 - PLL selection
 - VCXO Frequency
 - Input frequency for DDMTD
 - Tx/Rx routing equalisation



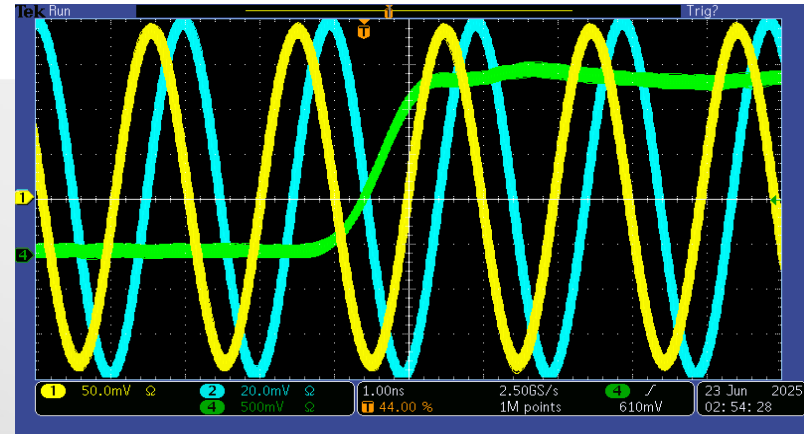


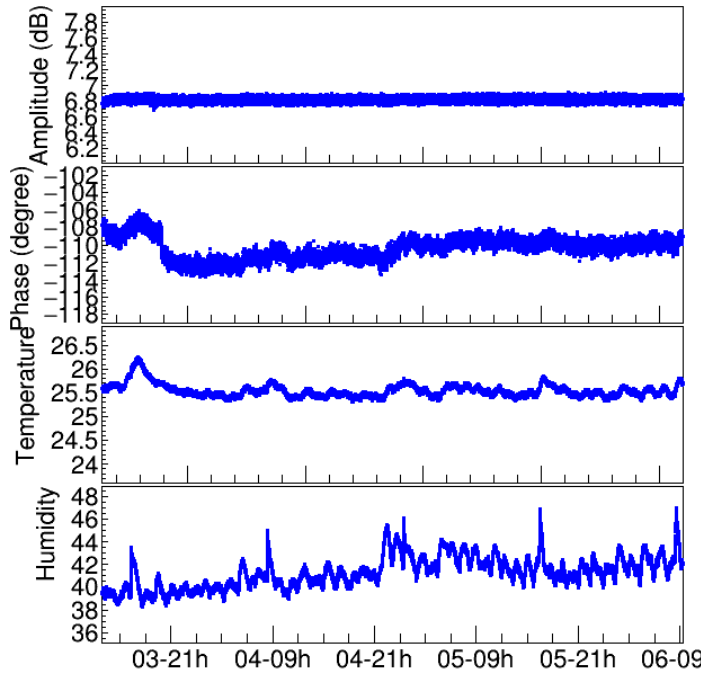
Clock synthesis for accelerators

Last result of Super KEK B clock synchronization with IJCLab IDROGEN board.



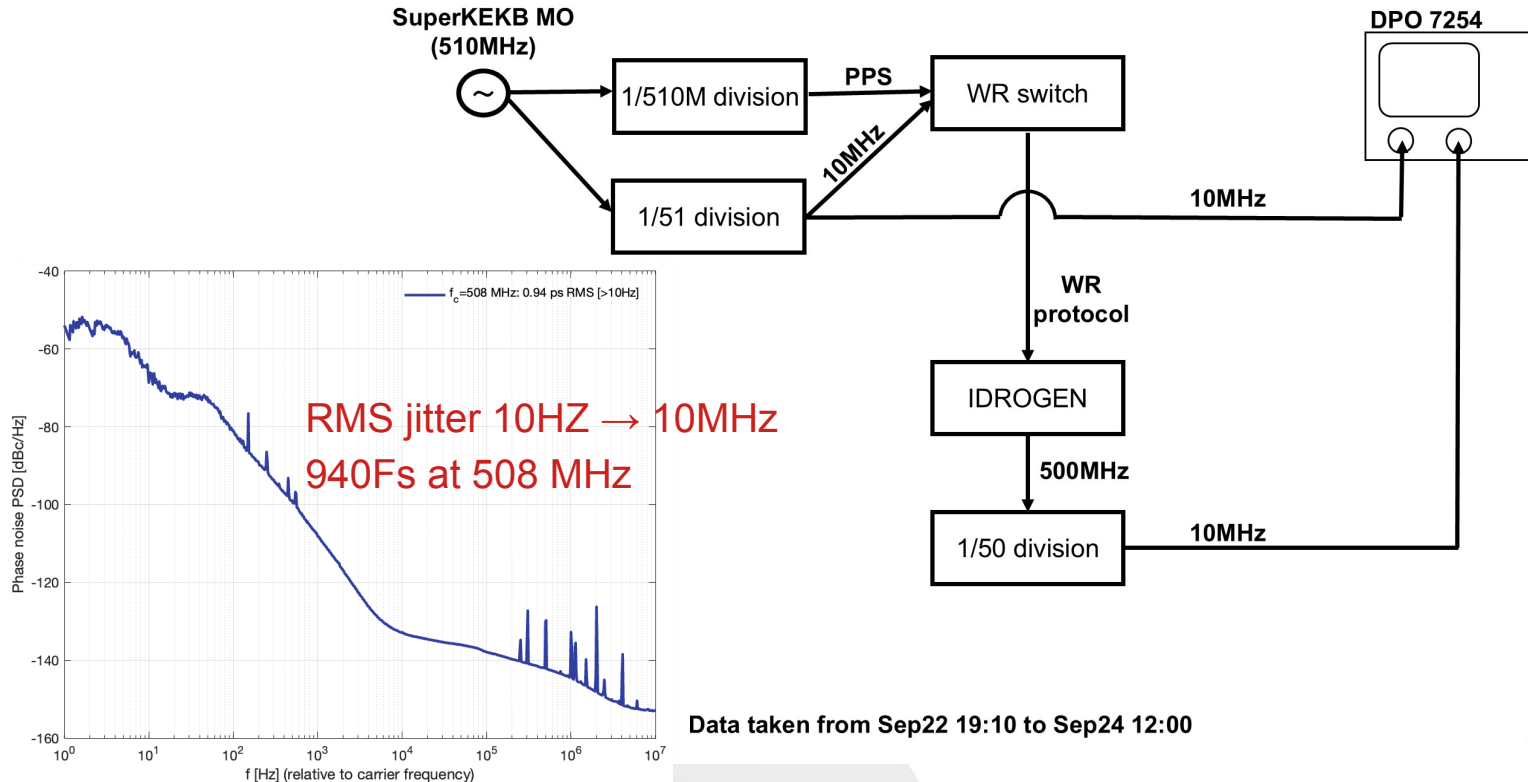
Comparison of SKB and Idrogen clocks
10h persistency, at scope resolution limit





509Mhz

IDROGEN synchronization setup

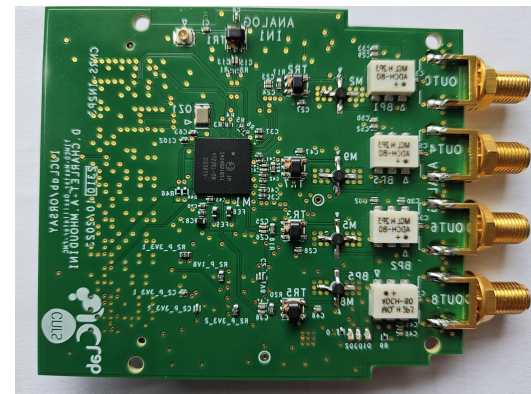




Accelerator synchronization: Arbitrary clock signal synthesizer

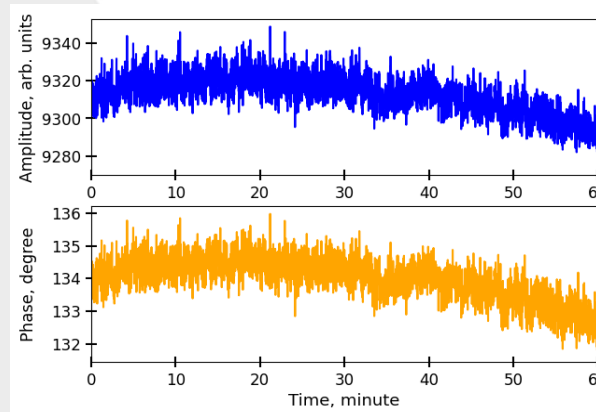
Fractional PLL (FPLL) FMC (on test)

- Replace very expensive system with recent, 30€ component
- Generate arbitrary frequency disciplined by WR clock
 - Frequency resolution 1 Hz
 - Phase noise system: 1.7ps (1 Hz, 10 MHz)
 - $\sim 0.3^\circ$ RMS phase jitter at 375MHz below 1Hz
 - 4 outputs 10KHz to 1.3GHz (2.75GHz: SI5361H chip)

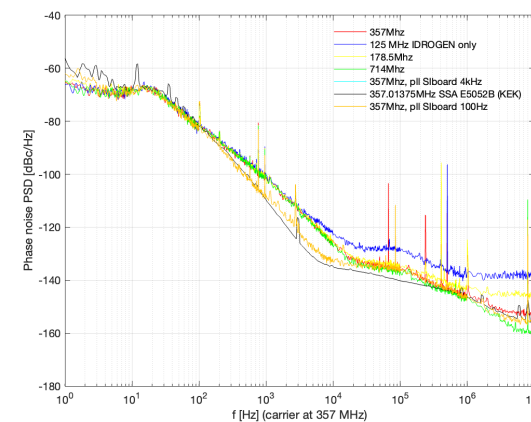


RTM board extension (under test)

- Arbitrary synthesizer
- High performance extension for optical time transfer (White Fox)



Long term drift

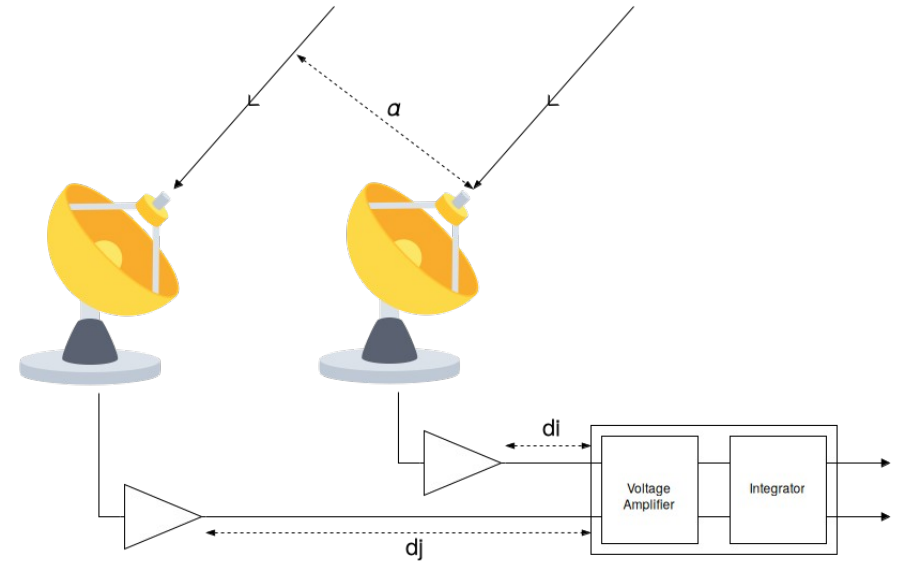


Phase noise for various different output frequencies



Radio Interferometer challenges

- Increasing of:
 - Deployment area
 - Receptor numbers
 - Receptor bandwidth
- Key issues:
 - Limitation: Length, node number, clock stability
 - Signal adaptation
 - Calibration
- Our solution: code directly at the receptor level
 - Requirements of this architecture:
 - High accuracy and stability of the timing distributed system
 - Example: PAON IV project requires ~1ns of stability
 - LOFAR, EVN in general,... LHAASO
 - Multi-messenger astronomy



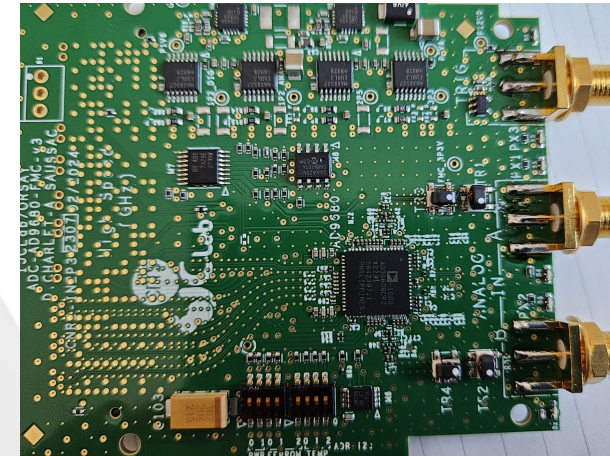
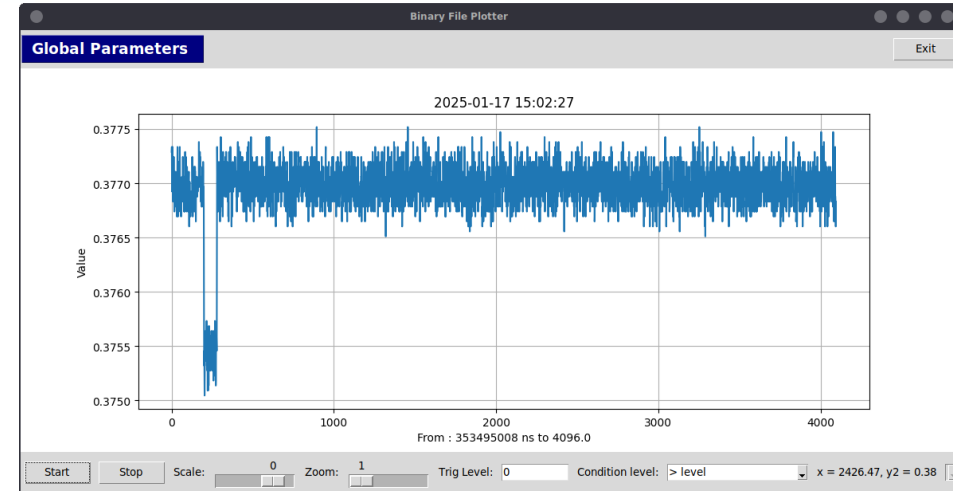
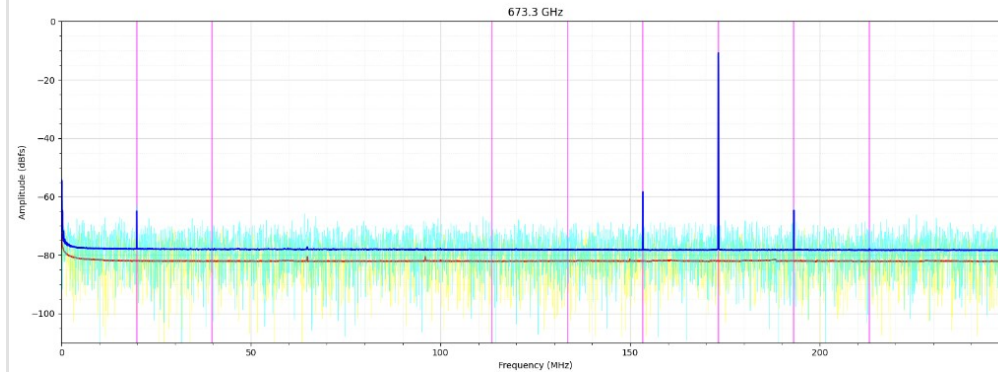
Typical configuration of radio interferometer



ADC acquisition board

Development of custom ADC board: Using the IDROGEN on board low jitter WhiteRabbit clock

- **FMC ADC9680_V1 (2022)**
 - 2 channels, 500 MSPS, 14 bits
 - 2GHz analog bandwidth
 - Clock provided by Idrogen board
- **FMC ADC9680_V3 (2024)**
 - 2 channels, 1 GSPS, 14 bits
- **FMC ADS42JB69 (2025)**
 - 4 channels, 250 MSPS, 16bits
 - One external trigger
 - Analog input 900MHz
 - 2.5V inputs voltage





Pulse Per Second : IDROGEN

- PPS 2 IDROGEN board
- 25m & 125m of optic fiber
 - ~50ps of dispersion of the PPS with calibration

