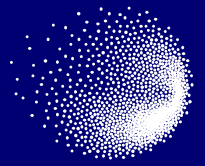


PSI Center for Accelerator Science and Engineering

Non-intrusive Observability and Load Isolation for Critical EPICS Timing Systems at PSI

EPICS collaboration meeting - April 2026

Romain Vallotton
Paris-Saclay, 22 April 2026

Agenda

1 **Context**

2 **SLS2 (Swiss Light Source) storage ring injection**

A. Event sequence observability issue

B. Solution – custom asynchronous logging system

3 **SwissFEL timing external network load**

A. Network overload issue

B. Solution – EPICS CA gateway

Context

Timing and Events systems at Paul Scherrer Institute, Switzerland

Hardware

PSI timing systems are based on Micro-Research Finland (MRF) HW:

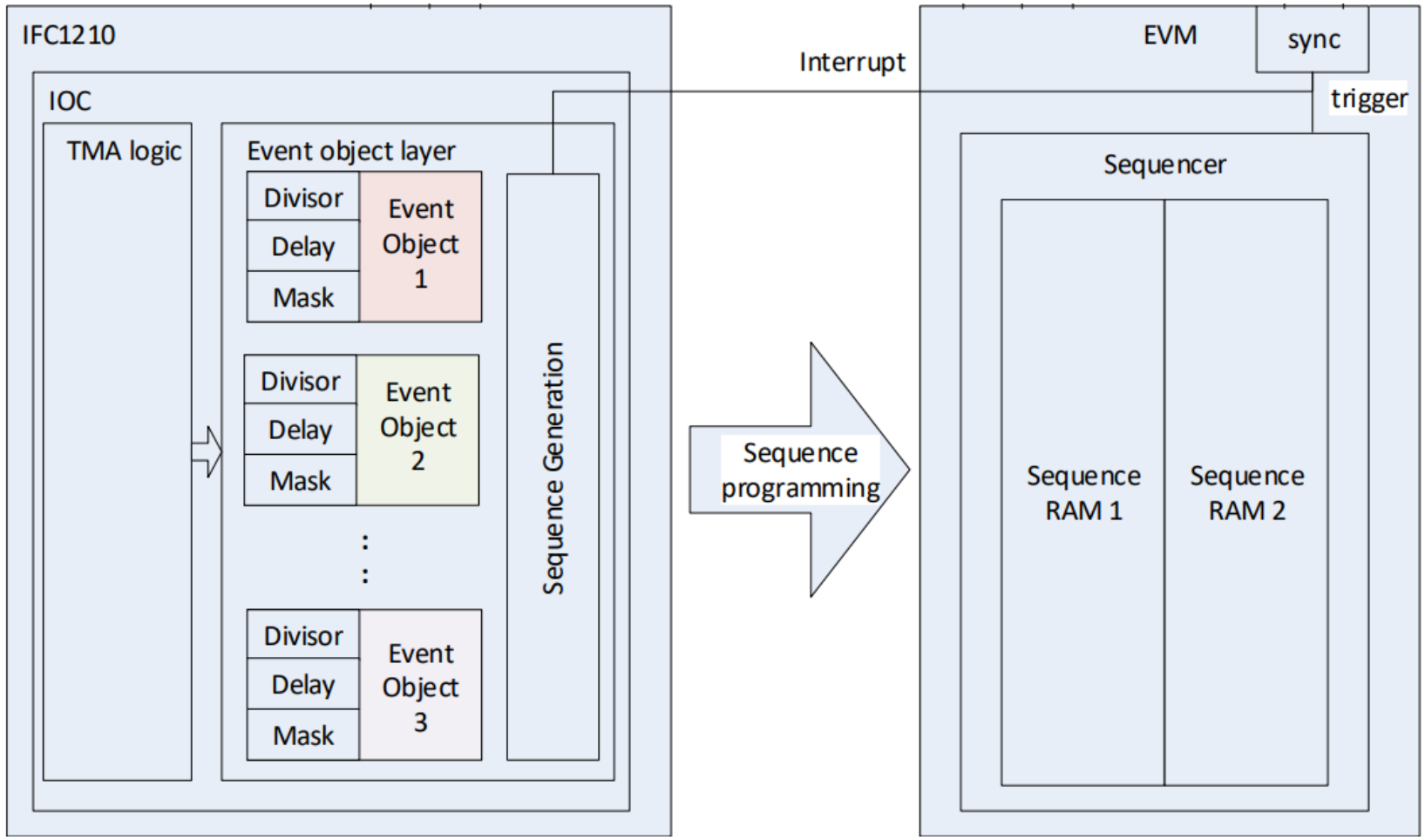
- **SwissFEL**: VME-300 series
- **SLS**: New in-house board based on cPCI-Serial. EVM Firmware ported by Jukka Pietarinen and Till Straumann

Context

Software

The main timing application is fully based on EPICS. It takes care of generating and configuring each event sequence executed by the HW, synchronised to the machine repetition rate.

Therefore, the EPICS-based application is critical.



SLS2 Storage Ring injection

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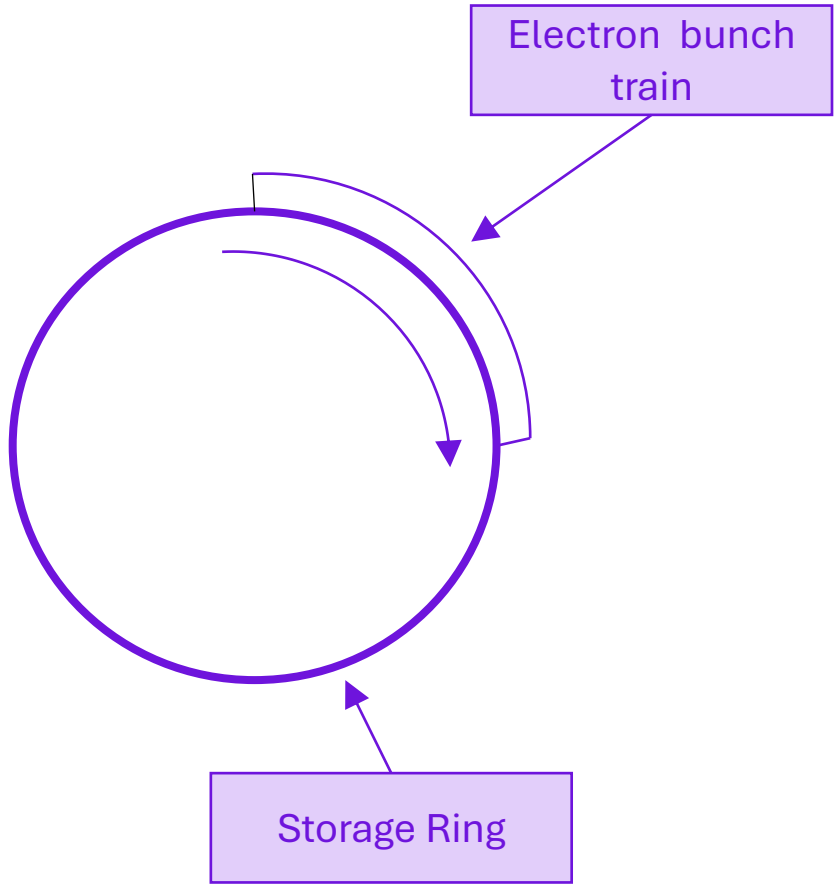
SLS2 Storage Ring injection

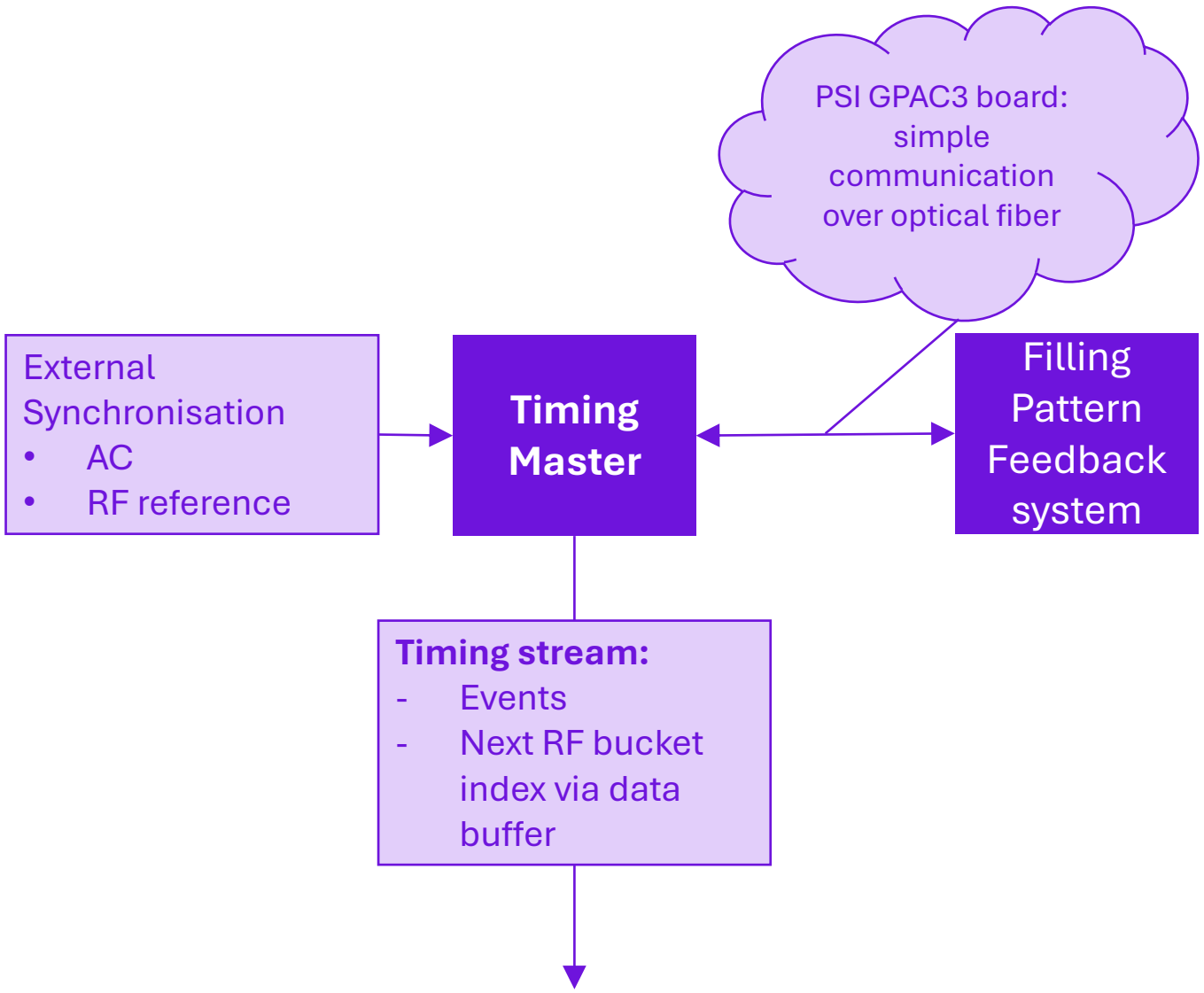
- In the synchrotron's storage ring, electrons circulate in fixed slots (called RF buckets).
- Over time, some slots become empty and must be refilled. This is detected by the filling pattern feedback system, which determines where injection is needed.
- The timing master is responsible for refilling the correct RF bucket by precisely timing the injection chain (Linac, Booster Ring, Storage Ring).
- To do so, it sends the identifiers of the slots to be refilled to the EVR downstream via the data buffer.



SLS2 Storage Ring injection

EPICS based timing master application

- Control sequence loop communicates with Filling Pattern feedback.
- Set local timing to next RF bucket.
- Send the next RF bucket via data buffer.
- Emit the EVR synchronisation event, telling all EVR to set their timing to the next RF bucket



SLS2 Storage Ring injection

Issue

- The timing master is critical: wrong bucket injection directly impacts machine operation. Debugging is critical, especially for filling pattern feedback mode.
- Standard logging (errlogPrintf) introduces latency and non-deterministic behavior.
- Need non-intrusive, local observability without disturbing the real-time process, in order to verify that the correct RF bucket is applied.
- Must integrate with EPICS to provide an expert diagnostic tool usable during operation.

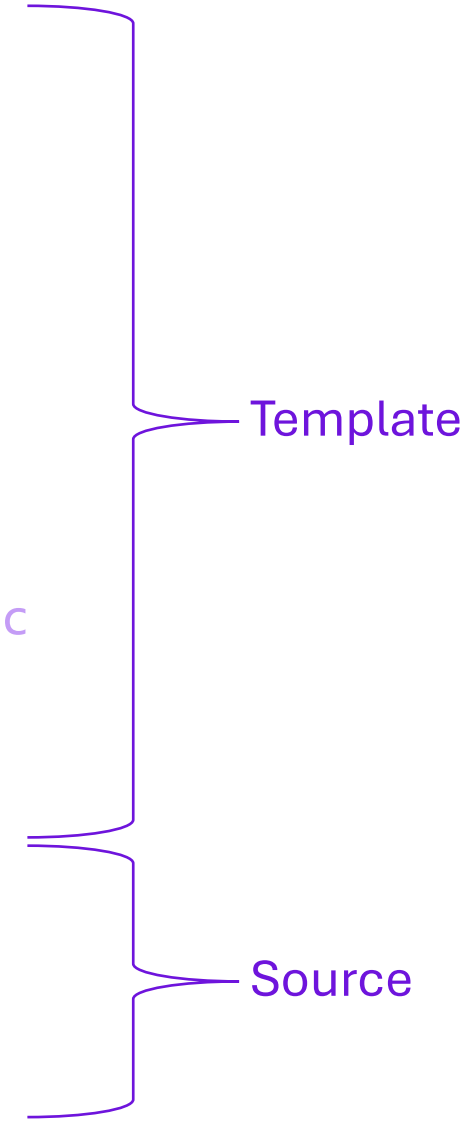
Solution – custom asynchronous logging system

For the development of filling pattern feedback, an EPICS asynchronous logging system was designed:

1. Message creation called from aSub record: evtSeqLogPrintMsg().
2. Allocate a slot from a fixed-size message pool, drop if empty (non-blocking, locked by mutex).
3. Message added to FIFO queue, signal EPICS event to notify consumer thread.
4. Asynchronous low-priority consumer thread: wait on event, dequeue messages one by one.
5. EPICS waveform record update: messages are copied to the record via BPTR field.
6. Message is recycled.

SLS2 Storage Ring injection

```
# SR Injection log waveform
record(waveform, "$(P)SR-Inj-Debug-I") {
    field(DTYP, "EVT SEQ LOG")
}

record(aSub, "$(P)FP-Local-Update_") {
    field(SNAM, "fp_local_update")  # in src/fp_local.c
[…]
}

In src/fp_local.c
if(sts_debug) evtSeqLogPrintMsg(“…%d”,var);
```



SwissFEL timing external network load

Context

- SwissFEL timing master generates the timing event sequence at a repetition rate of 100 Hz.
- It is based on IOxOS IFC1210 (VME).
- Originally, it was protected from high network load using a Soft IOC, acting as a gateway.

SwissFEL timing external network load

Issue – Disproportionate impact

- Over the years, the soft IOC was bypassed, and clients started using directly the local master PVs.
- The timing master became overloaded and often missed FEL pulses (more than 500 CA clients, and up to 9000 connections).
- This triggered an RF interlock, and caused an RF phase loss, interrupting the machine for 30 minutes.
- This is a known risk as the timing master is a single point of failure. However, the problem escalated significantly and cannot be justified to operations.

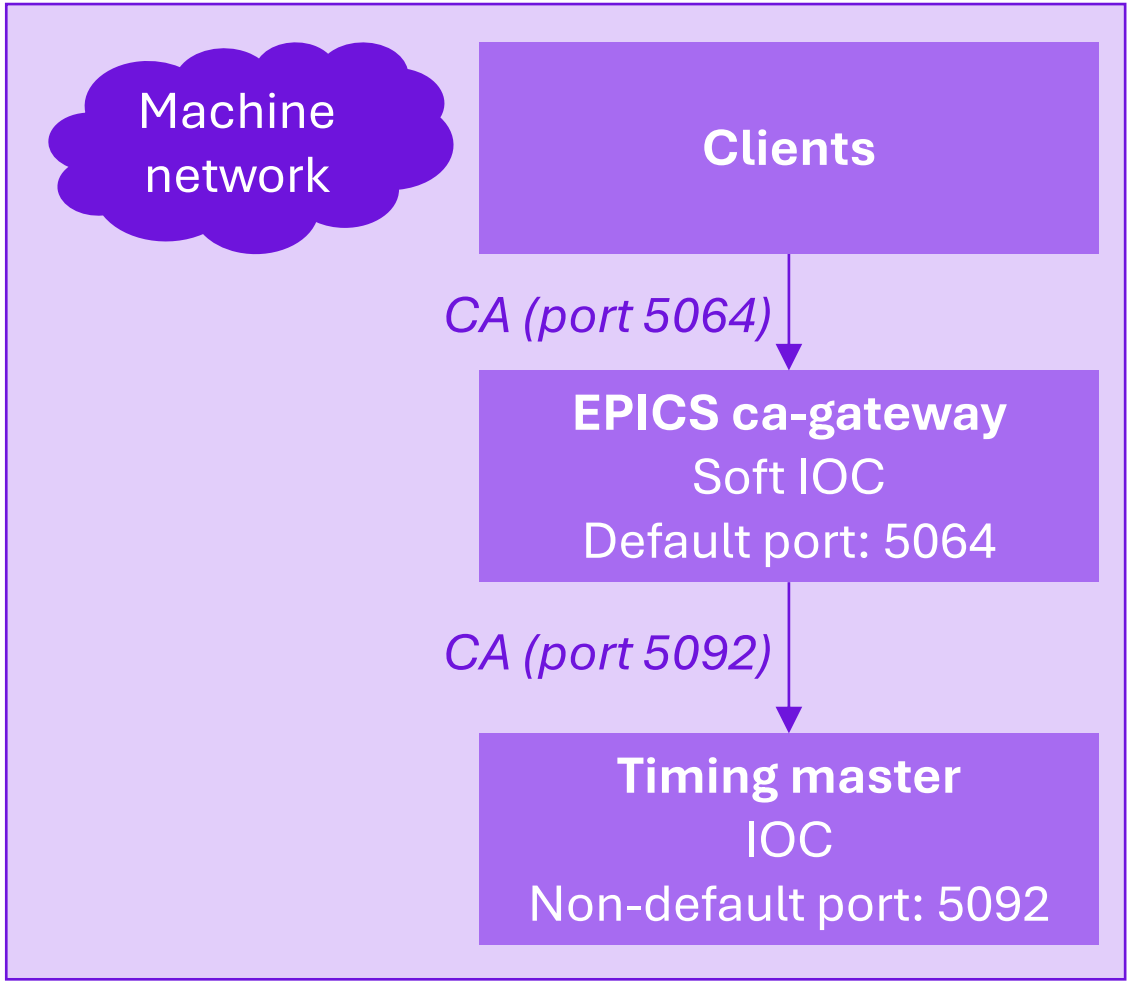
SwissFEL timing external network load

Solution - EPICS CA gateway

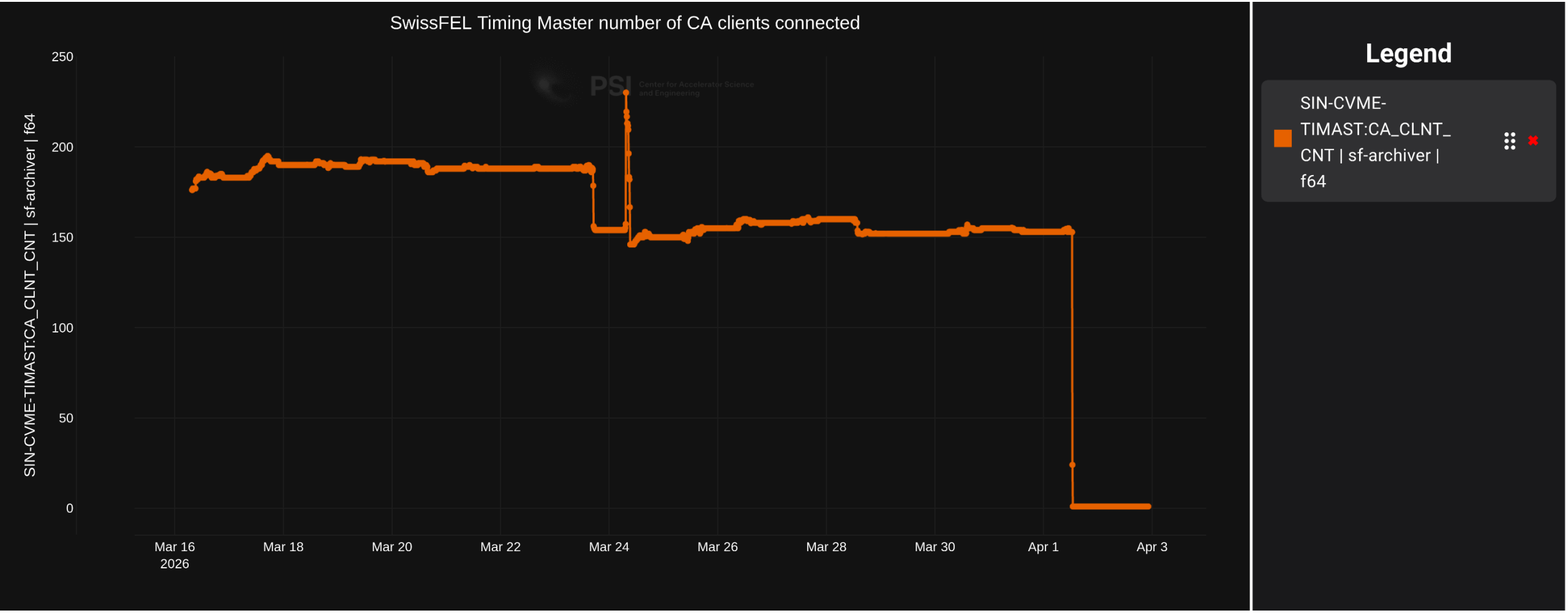
- Traditional CA gateway deployment, with IOC in another subnet is not convenient: We cannot justify creating a subnet for a single IOC.
- From the original documentation, we noticed that the gateway can be used to isolate an IOC.
- It is not necessary to use it to access PVs across subnets.
- This is the basic application of this EPICS extension, which is sometimes forgotten.
- The timing master can then be hidden by changing its default port.

SwissFEL timing external network load

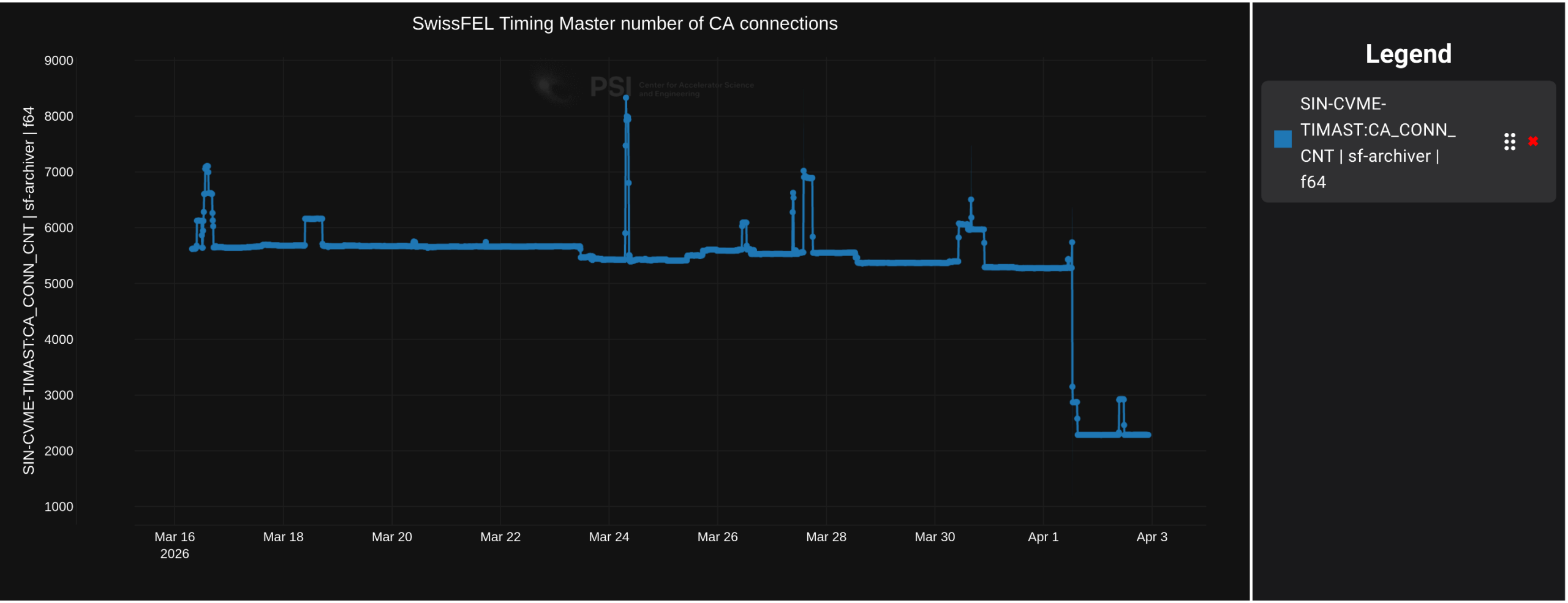
```
epicsEnvSet SYS "SIN-TIMAST"

### Hide IOC behind gateway

# Change IOC default server and beacon ports
epicsEnvSet("EPICS_CAS_SERVER_PORT","5992")
epicsEnvSet("EPICS_CAS_BEACON_PORT","5993")

# Setting CA port is not mandatory, but is done for consistency, and to
# prevent accidental exposure on default port (5064)
epicsEnvSet("EPICS_CA_SERVER_PORT","5992")
epicsEnvSet("EPICS_CA_BEACON_PORT","5993")
```



SwissFEL timing external network load



SwissFEL timing external network load



Thank you for your attention.

Any questions?

If you are interested by the sources of the asynchronous logging system, or want to discuss timing systems or other topics: romain.vallotton@psi.ch