uTCA White Rabbit Timing and Trigger System for Distributed Deterministic Control

EPICS CM 2026
20.04.2026

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Agenda

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What is a timing system?

02
Safran Solution: Timing System

03
Safran Solution: MPS Application

04
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05
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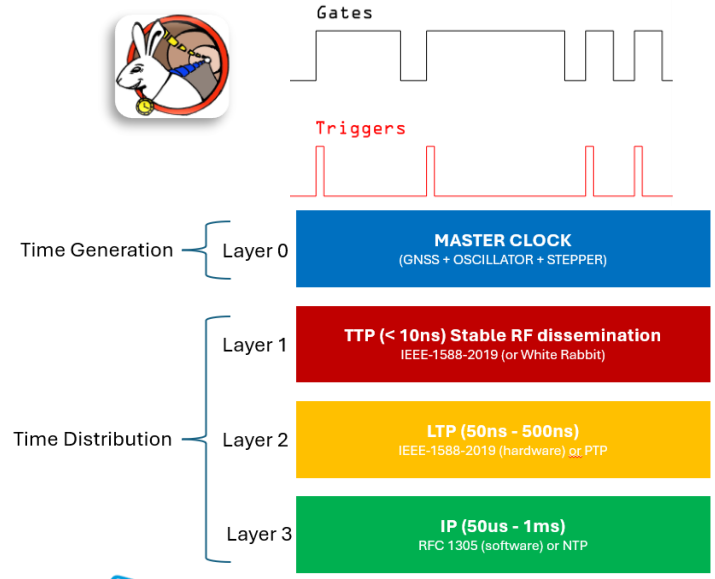
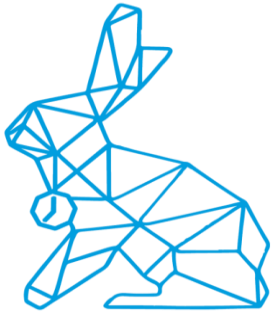
01 What is a timing system?

- **Applications: every installation requires timing and synchronization**
  - Crucial component used to synchronize and control the operations and events that occur during experiments or beam delivery in a particle accelerator
  - Main functions are:
    - **Timing/Synchronization**: ensuring that all the components operate at the correct time relative to each other.
    - **Trigger and gate generation**: generation of deterministic signals to initiate and coordinate subsystem actions, including precise pulses that define the timing of operations such as particle bunch generation.
    - **Deterministic Distribution**: Timing and trigger signals need to be distributed throughout the accelerator facility with minimal delay and jitter (this is especially critical in lasers).
    - **Control and supervision**: configuration and monitoring through the control system.
  - Other possible functions:
    - **RF distribution:** allows the reconstruction of the RF signal in the end-nodes (synchrotrons)
    - **Interlocks distribution**: enables the stop of the complete installation in case of failure.

01 Why White Rabbit for facility timing?

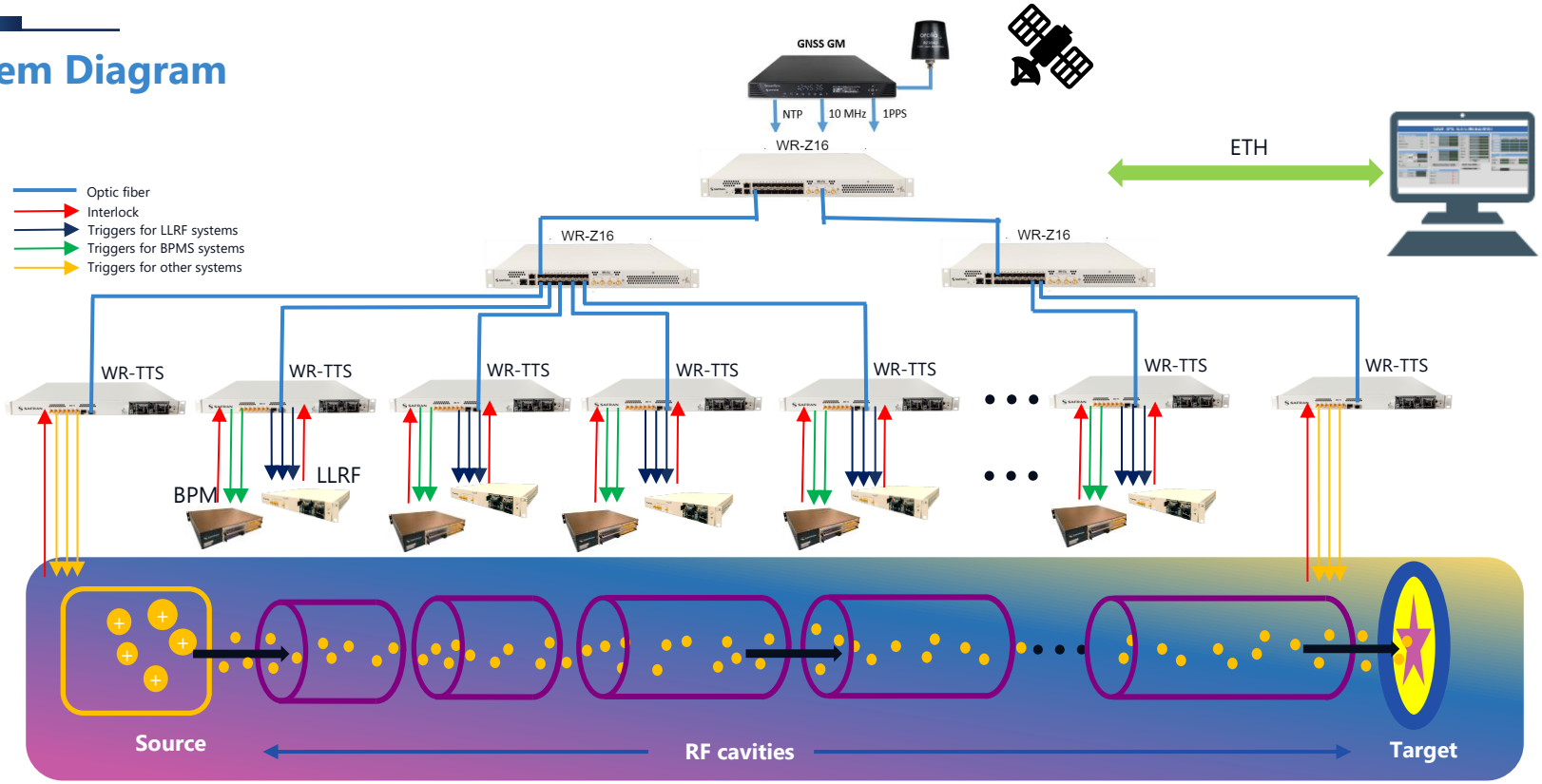
- **Main Advantages**
  - **Sub-nanosecond synchronization:** provides a common and highly accurate time base across distributed nodes.
  - **Deterministic timing over fiber:** enables precise trigger distribution and coherent operation of time-critical subsystems.
  - **Scalable and low-maintenance infrastructure:** new nodes can be added easily thanks to plug-and-play optical links and automatic link calibration.
  - **Unified timing base:** the same infrastructure supports synchronization, timestamping, and trigger generation for systems such as LLRF, BPM, MPS and diagnostics.





01 Why White Rabbit for facility timing?

System Diagram



02 Safran Solution

WR-TTS: Platform

FIRST VERSION based on HATI IP CORE

White Rabbit Commercial Products

WR-Z16

WR-SWITCH-LJ

WR-ZEN TP-32BNC

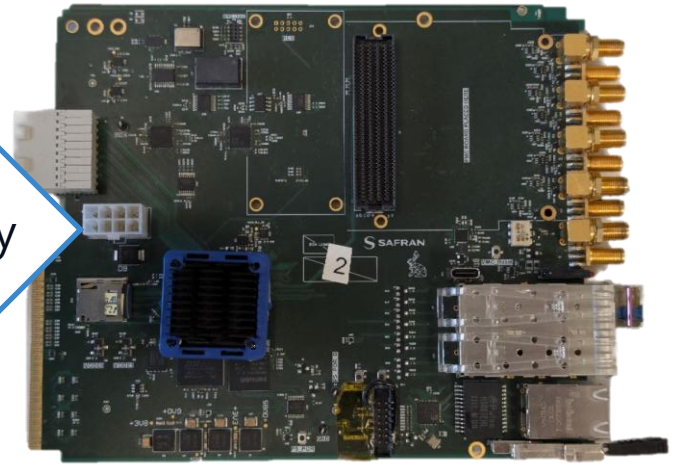
WR-WROX

WR-ZEN TP-FL

WR-LEN

WR circuitry

White Rabbit Timing & Triggering system



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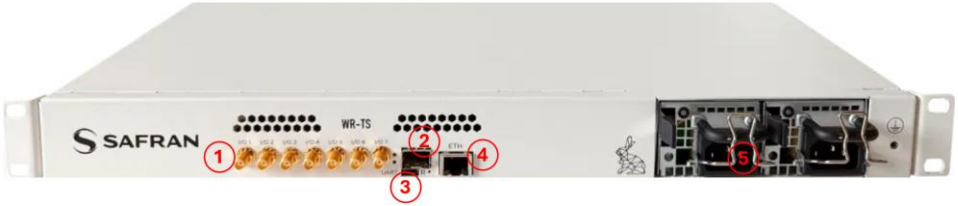
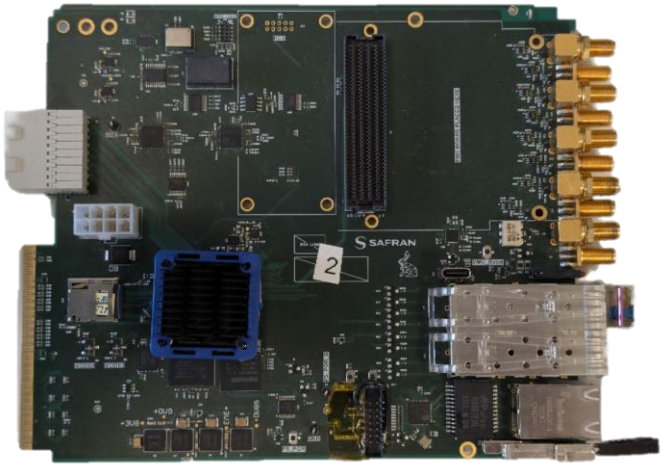
WR-TTS: Platform





Platform:

- Ultrascale + SoC FPGA-based architecture enabling deterministic real-time processing
- White Rabbit technology
  - Sub-nanosecond time accuracy
  - Very high scalability and large distance links support
  - Nanosecond timestamping
  - **10MHz and PPS outputs**
  - **Master/Slave Mode**

- uTCA form factor.
- Up to 9 configurable in/out ports
- 2 x SFP ports (WR and fast communications)
- 1 x ETH port (control, monitoring and management)
- 1 x USB port (management)
- Event Generation and Detection (nanosecond resolution)
- **FMC and RTM expansion connector for custom I/O and subsystem interfacing**
- EPICS/TANGO Controls integrated

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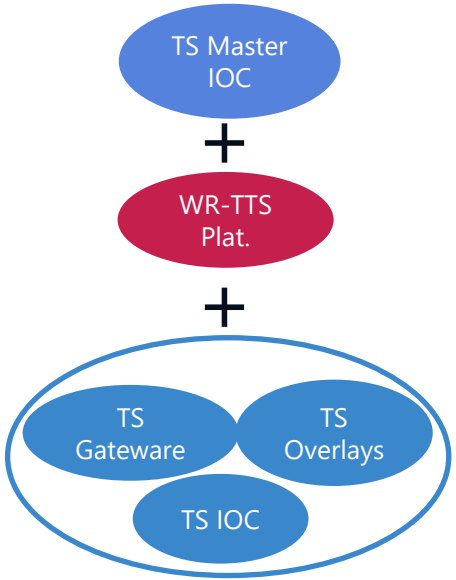
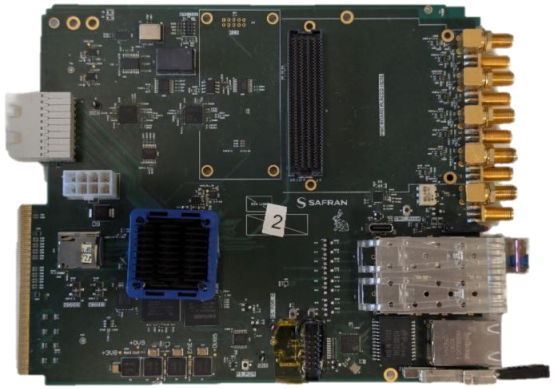
WR-TTS: Same Platform, Different purposes

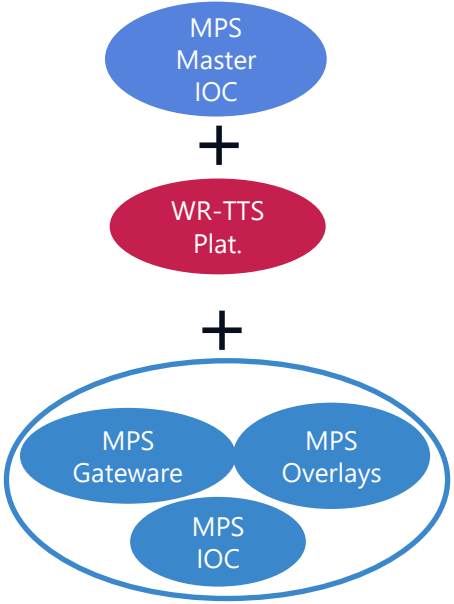
Timing & Triggering System





Hybrid Approach??

Machine Protection System



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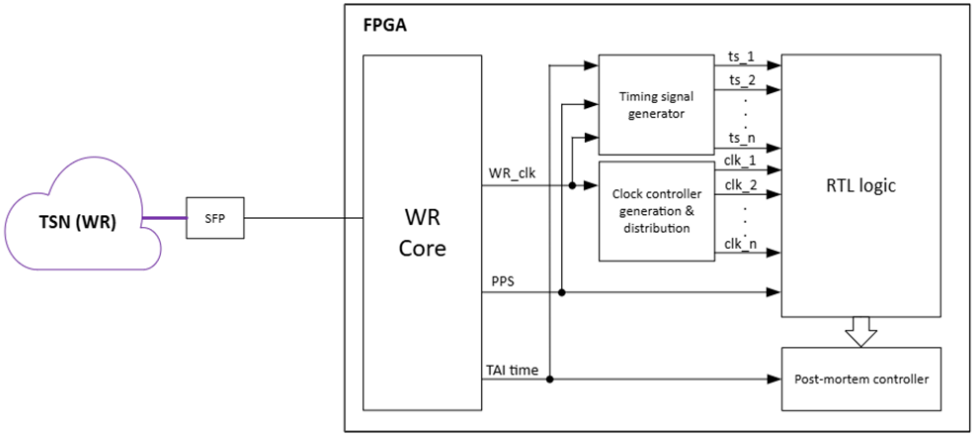
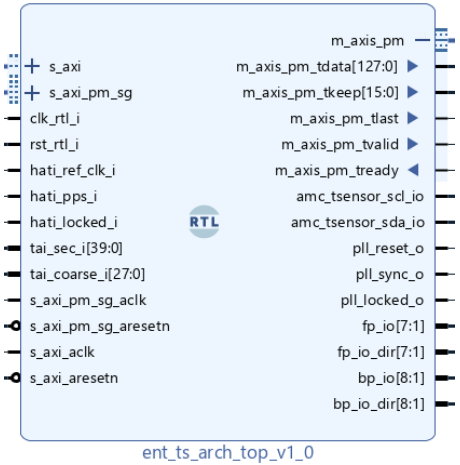
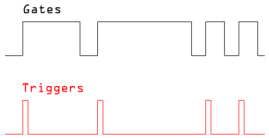
WR-TTS: Timing + Triggering







- Sub-nanosecond time accuracy
- Picosecond level precision
- Distance range: over 80 km using fiber
- DWDM compatible
- Dynamic compensation of asymmetries caused by weather conditions

- Programmable single shot or sequence triggers
- Resolution of 4ns.
- Programmable rate, delay and duty cycle.

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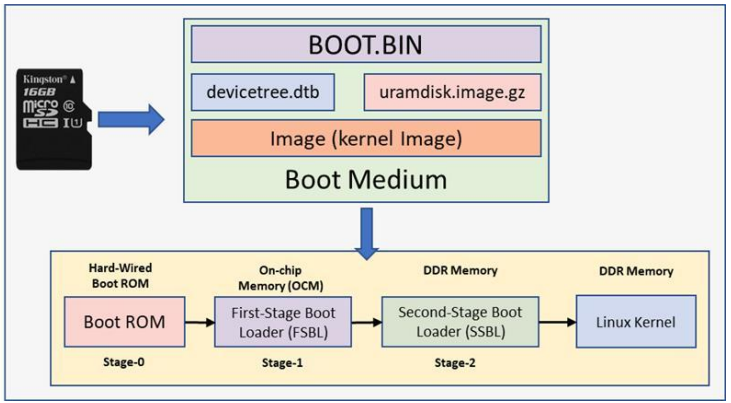
WR-TTS: Embedded Software



Buildroot-based OS – WR-ZYNQ-OS

- BOOT.bin: FPGA image
- Uboot: instructions to boot the devices
- Devicetree: mapping of devices of the system/hw plattform.
- Image: Custom Linux kernel image
- Root filesystem:
    - Linux services for configuring all the components on the platform (PLL, DMA, ADC, I2C devices…)
- Builds a CC Toolchain for:
    - SoC Communication Drivers (AXI)
    - Specific configuration tools (PLL, ADC, DAC, Sensors…)
    - **EPICS base and EPICS components (asyn, seq, autosave..)**
    - **EPICS IOC**

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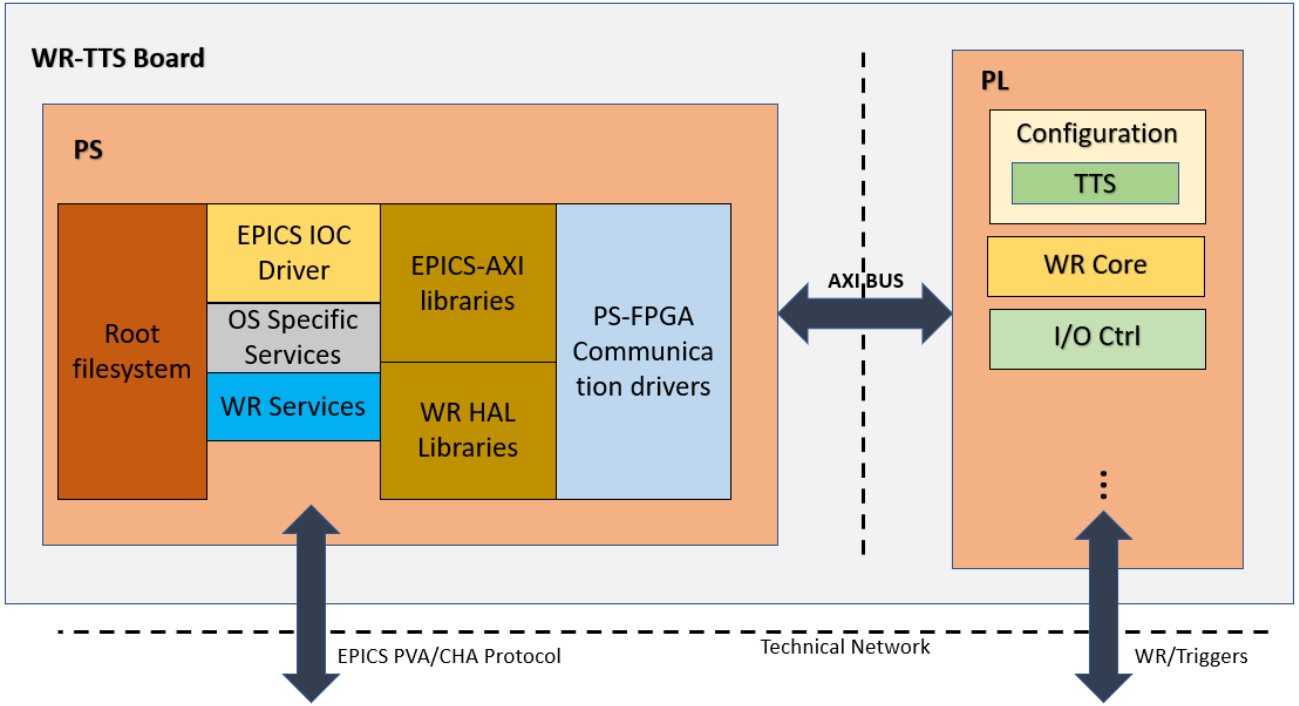
WR-TTS: Embedded Software



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WR-TTS: Embedded Software

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WR-TTS: Embedded Software

EPICS IOC

- **EPICS 7**
- **Asyn** 4.44-based driver using AXI bus for FPGA-Processor communications
- WBGen to define FPGA addressing and EPICS Asyn connectors
- AXI Register MAP matched with EPICS DB (trough asyn)
- Specific functionalities integrated on the EPICS driver (Postmortem, Device components control…)

```
lastreg = new EWBReg( pPrhGen, WB2_REG_ARGS( GEN, PL_FREQ ));
createParam( new EWBField( lastreg, WB2_FIELD_ARGS( GEN, PL_FREQ, VAL )));
```

```
##---------------- 'ext_pll_sync' in 'timing_system status & control registers'

record(bo, "$(user):ExtPllSyncCmd")
{
    field(DTYP ,"asynInt32")
    field(OUT  ,"@asyn($(PORT),$(ADDR),$(TIMEOUT))ctl_ext_pll_sync")
    field(DESC ,"ext_pll_sync")
}

record(bi, "$(user):ExtPllSyncStat")
{
    field(DTYP ,"asynInt32")
    field(INP  ,"@asyn($(PORT),$(ADDR),$(TIMEOUT))ctl_ext_pll_sync")
    field(SCAN ,"I/O Intr")
    field(DESC ,"ext_pll_sync")
}


##================ PL_Freq

##---------------- 'val' in 'PL_Freq'

record(ao, "$(user):PLFreqValSet")
{
    field(DTYP ,"asynInt32")
    field(OUT  ,"@asyn($(PORT),$(ADDR),$(TIMEOUT))PL_Freq_val")
    field(DESC ,"val")
}

record(ai, "$(user):PLFreqValRb")
{
    field(DTYP ,"asynInt32")
    field(INP  ,"@asyn($(PORT),$(ADDR),$(TIMEOUT))PL_Freq_val")
    field(SCAN ,"I/O Intr")
    field(DESC ,"val")
}
```

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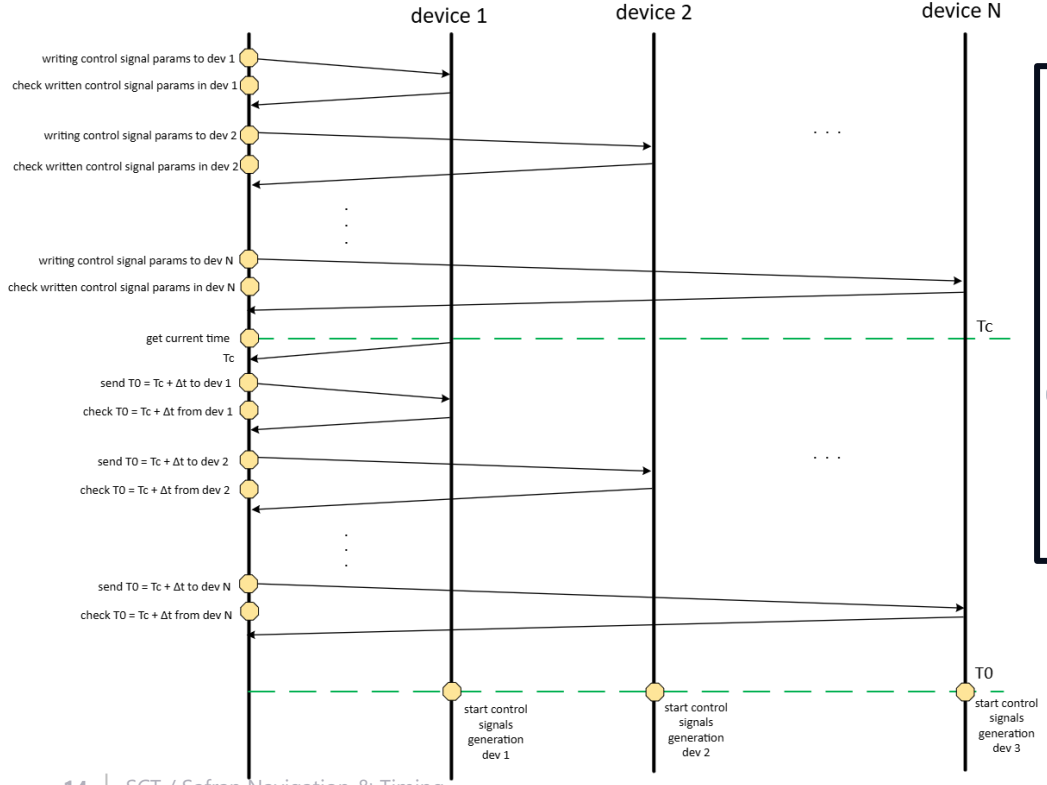
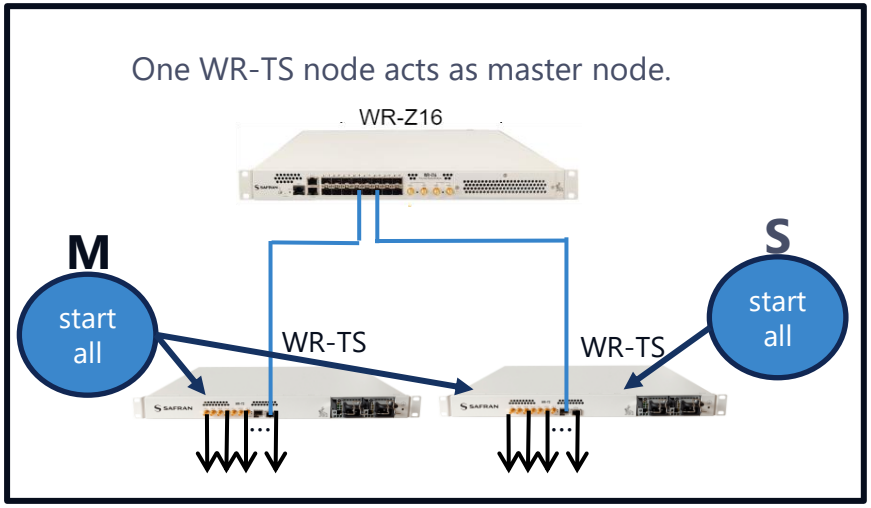
WR-TTS: Master-Slave





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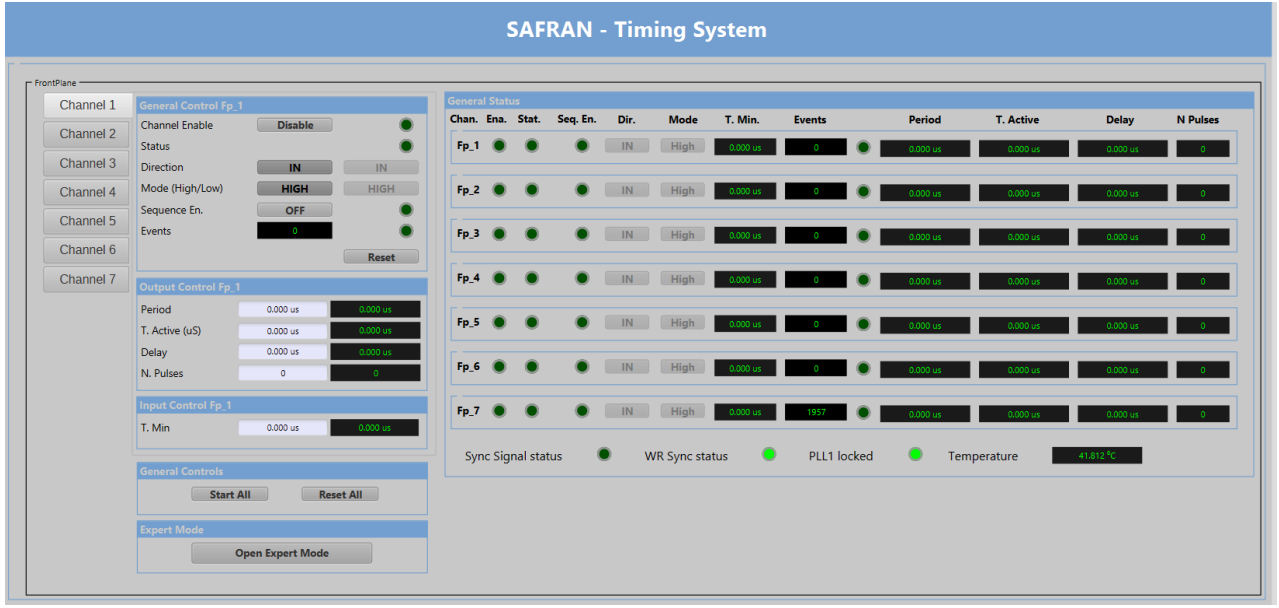
WR-TS: Graphic User Interface



Input configuration:

- **T.Min**: Minimum time to consider a pulse valid.

Output configuration:

- **Period**: Time between pulses.
- **T. Active**: Time that the signal will be High/Low.
- **Delay**: Time between the starting trigger and the generation of the pulse
- **N. Pulses**: Number of pulses to generate (∞ if 0).

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WR-TTS: Sequences of events

- Sequences of events can be defined in .csv files.
- The system loads these sequences in a double buffer in the WR-TS nodes. The WR-TS node executes one sequence of events during the current frame while receiving the sequence data for the following frame.
- /home/epics-user/data/sequencer/

	A	B	C	D
1	period	width	delay	n_pulses
2	20000	10	0	1
3	20000	10	0	1
4	20000	10	0	1
5	20000	10	0	1
6	20000	10	0	1
7	20000	10	0	1
8	20000	10	0	1
9	20000	10	0	1
10	20000	10	0	1
11	20000	10	0	1
12	20000	10	0	1

Event 1
Event 2
Event 3
.....
.....
Event 640

Frame N

Event 1
Event 2
Event 3
.....
.....
Event 640

Frame N+1

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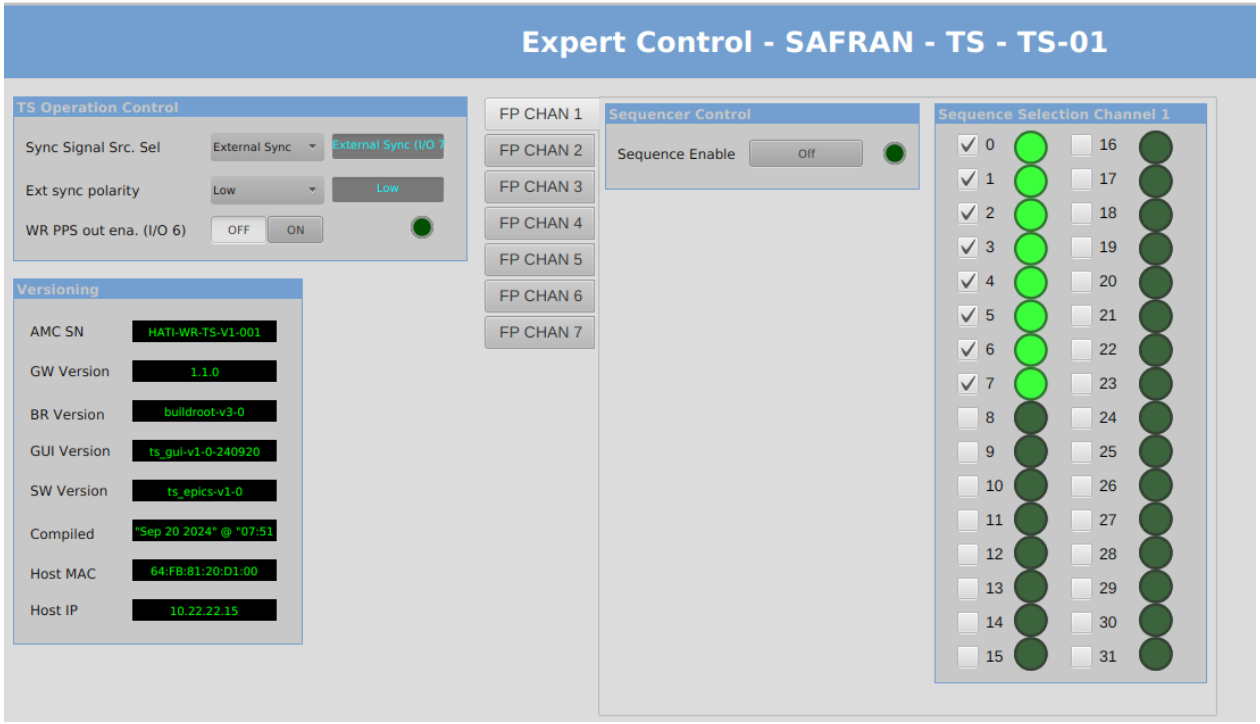
WR-TS: Graphic User Interface



Sequences of events mode

- Up to 32 selectable sequences of events.
- Internal PPS or external synchronization signal.

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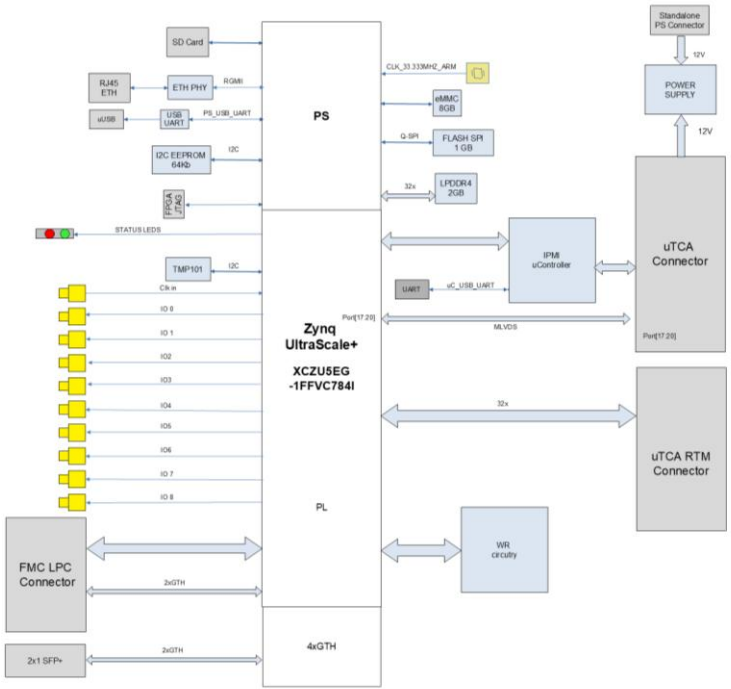
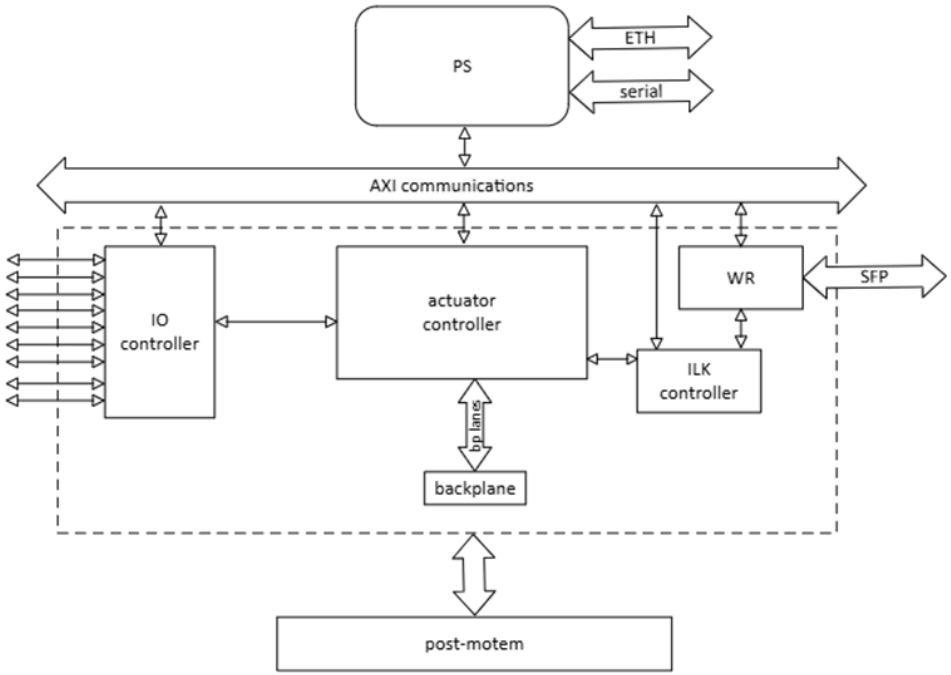
WR-TTS: Machine protection System





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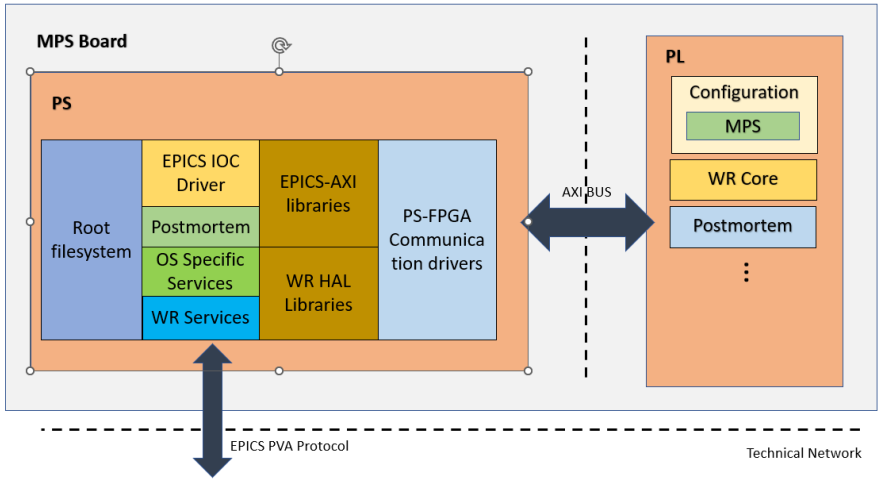
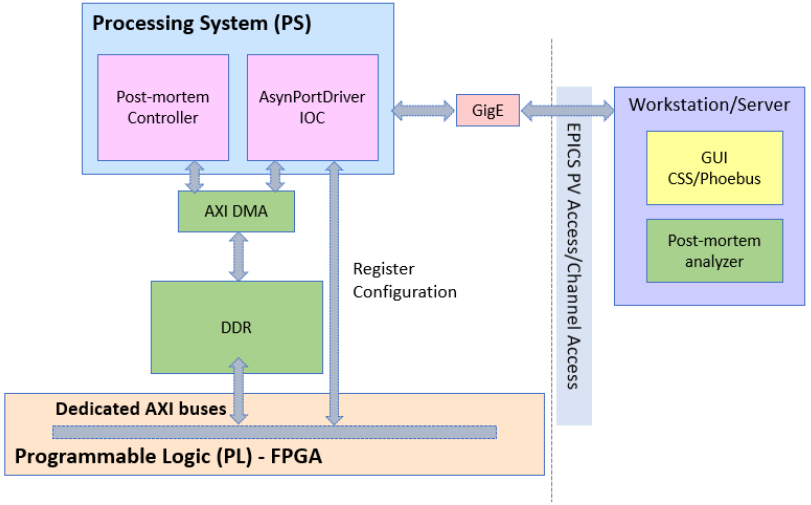
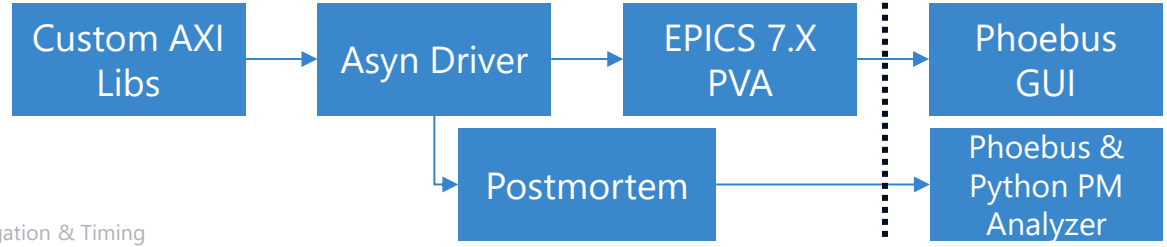
WR-TTS: Embedded Software







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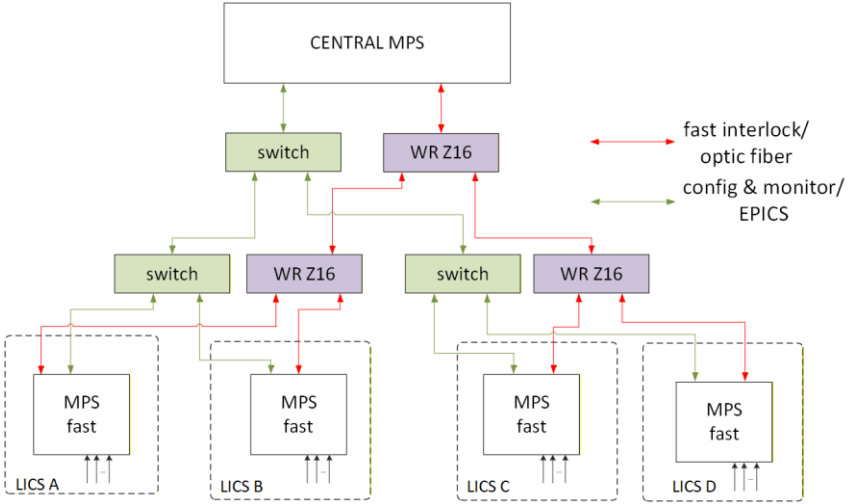
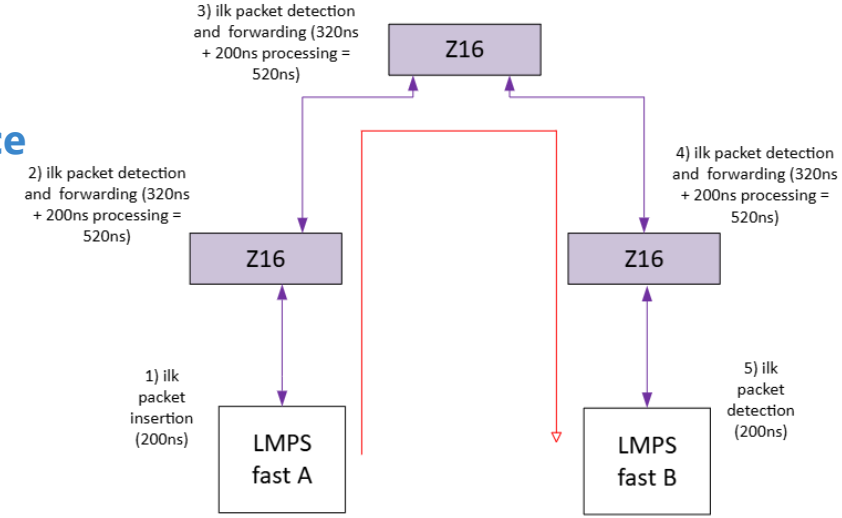
WR-TTS: Machine protection System; performance



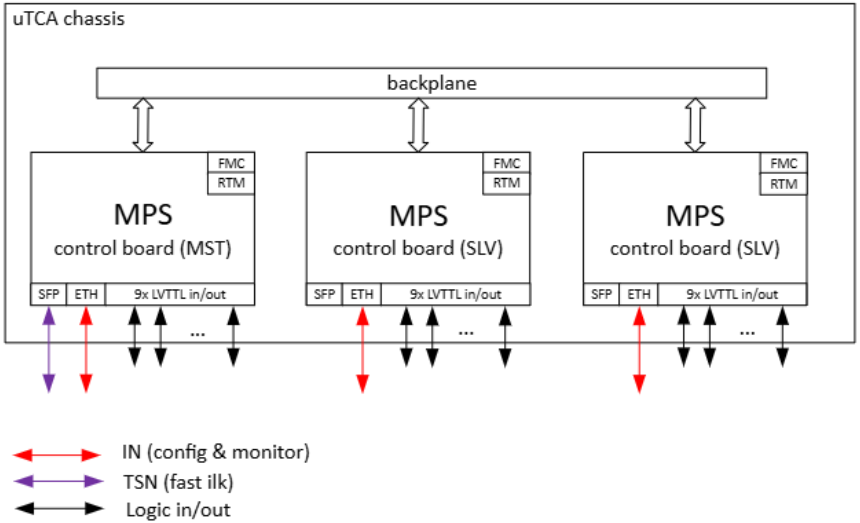


- **Ultra-fast response**: Optical fibers enable near-light-speed signal transmission with nanosecond reaction times (~500ns per hop) (**commas insertion on WR flow**)
- **EMI immunity and galvanic isolation**: Fiber optics are unaffected by electromagnetic interference and ensure complete electrical isolation between systems
- **Long-distance communication**: Signals can travel hundreds of meters with minimal attenuation
- **Scalability and flexibility**: Fiber systems can be easily expanded and reconfigured

03 Safran Solution

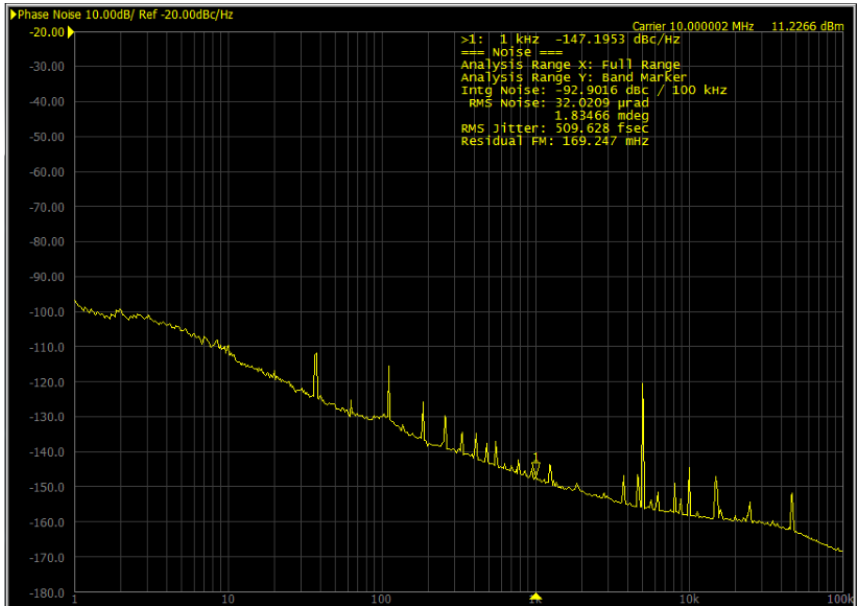
WR-TTS: Machine protection System

Master-Slave Mode in uTCA Crate



04 Tests & Results

WR-TTS: Jitter Measurements

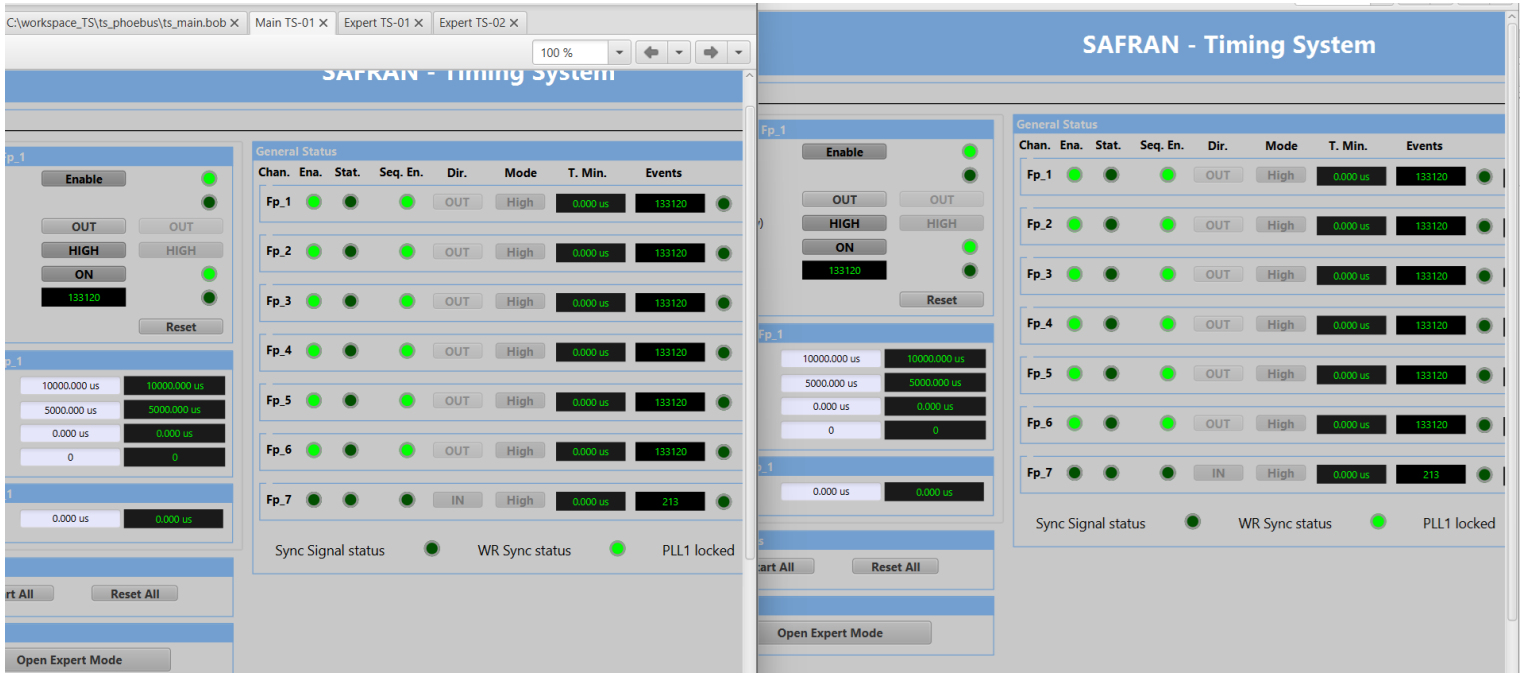


RMS jitter 10MHz output

~500 fs of RMS jitter measured at the 10MHz output

04 Tests & Results

WR-TS: Sequence of events generation

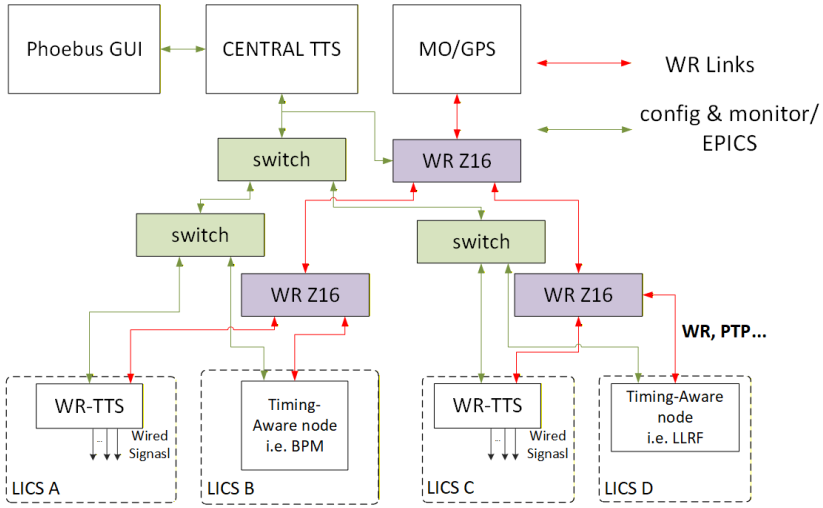


Long term test

05 Next Steps

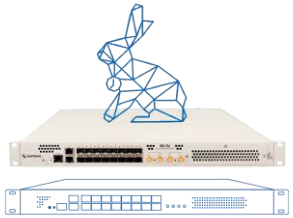
Work in Progress… Phoebus & EPICS-based Central Timing & Synchronization Entity

- **Auto-Discover Timing-aware nodes**: Using EPICS discover tools to get the PVa nodes and their timing-related PVs and **LLDP** for WR nodes.
- **Visual Trigger Programming**: Setup all the gates and triggers and check their shapes and organization in a chart before executing them.
- **Centralized Monitoring**: Monitor the health of the WR-TTS and timing-aware nodes.
- **Alarms Management**: Full TTS ecosystem integrated into the Phoebus Alarm System.
- **MPS Integration**: Fast interlock in case of a timing issue to avoid damages.



Recommendations and advice are Welcome!

Feel free to stop by our booth in the exhibition hall!



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