

# IRT-ICS – Thermal and Mechanical Design

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on behalf of the IAAT IRT Team



## 1. MCR RIDs:

Prove that EEE components stay inside their qualified temperature limits with ECSS derating margins; Board design temperature must be below 85°C

## 2. Redesign of the electronic box goal:

- Determine housing thickness, as it is the primary heat conductive path from the PCBs to the S/C interface
- Define relevant EEE components and their dissipated power and allowable temperature limits (from datasheets)

## 3. Boundary conditions:

S/C interface temperatures (as in EID-A 1.0), only conductive heat transfer

- ✓ Operational hot case (OP HC) +50 °C → likely ok (see following slides)
- ✓ Operational cold case (OP CC) -40 °C → likely ok
- ! Non-operational cold case: -55 °C → implies qualification to -65 °C per ECSS margin  
→ for EID-A 1.2 we propose T\_NOP\_min of the DHU = -45°C
- ! Switch on: -40°C, may be critical for the DBP baseline CPU, the GR740: its min. junction temp. is -40°C, leaving no room for margins → TBD

- Worst-case analysis:
  - Power: maximum power in datasheet/benchmark of manufacturer
  - Cooling area: assume only conduction heat flow path through min. area of ball/land grid array (BGA/LGA) at bottom
  - No heat sink bonded to the package, e.g., only metal-frame (see Fig. 2-1)

## Examples of critical EEE components

- GR740 CPU on DPB worst-case assumptions:
  - Power: max. 1804 mW (Doc. No GR740-VALT-0010). With component safety (factor 2), design safety (factor 1.2): **4.3 W**
  - Area LGA: min.  $(23.90 \text{ mm})^2$  (GR740 Datasheet, page 487f)
  - Storage temp: - 55 – 150°C, Operating junction temp: **-40°C – 125°C** (GR740 Datasheet, page 491)
- SAMRH707 MCU on FW/CUCB and MTCB:
  - Max. power in benchmark: 461 mW, 1.95V, with component and design safety: **2.2 W** (SAMRH707 Datasheet page 1392; 2 W max. defined on page 1388 (TBD with Jörg))
  - Area BGA:  $(21.00 \text{ mm})^2$  (SAMRH707 Datasheet page 1411)
  - Storage temp.: -65°C to +150°C, operating temp. **-55°C – 125°C**
- Detailed analysis of SXI DHU BEE-boards as worst-case for DC/DC converter temperatures

Figure 2-1. Mounting Technique with Metal Frames and Cold Plate

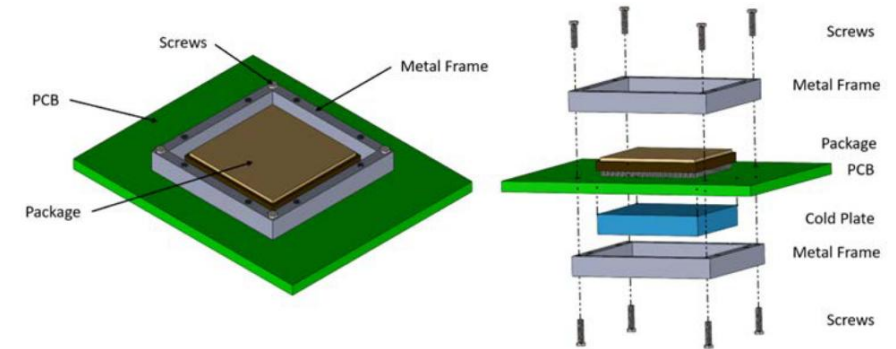


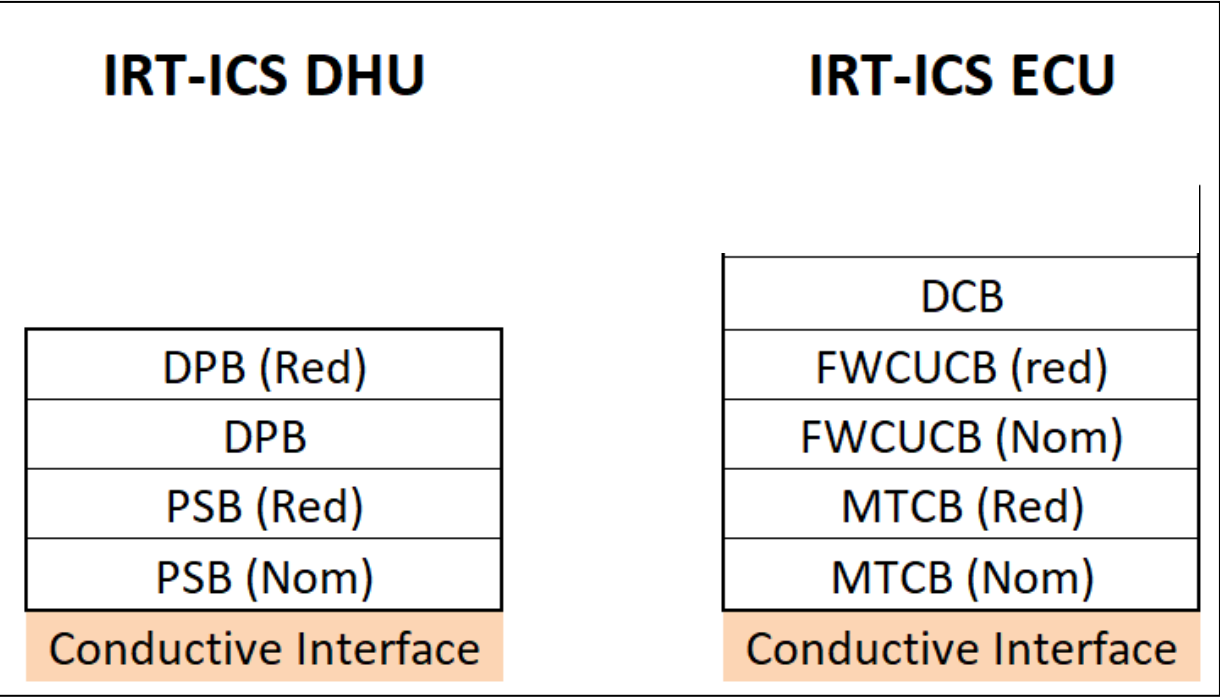
Fig 2-1: mounting support using a metal frame to prevent warping (no heat sink)



1. Define limits and loads of critical EEE components
2. Build a steady-state FEM in Siemens Simcenter3D
  1. Conduction-only heat transfer (per EID-A: box should be designed to conduct its heat to the S/C interface)
  2. Size the required thermal conductance from component → PCB → housing → baseplate (e.g. housing thickness, contact assumptions) to keep components within limits.
3. Based on this data determine the required thickness of the Al-frame material → **Provides preliminary FEM**
4. From step 2 & design assumptions → finish detailed model (lightweighting, connectors, bolts) in the next two weeks.
5. Thermal (Lauro)/mechanical (Roisin) simulations: identify model details for optimization in Simcenter3D
6. Iterate step 5 until FEM solution meets all temperature and structural requirements
7. Reduced thermal mathematical model (RTMM) in ESATAN-TMS model:
 

one node for the box, derive GL in Simcenter 3D, show correlation of models as defined in ESA-THESEUS-PLD-RS-001.
8. Additionally: transient model? (TBC)

Board	Critical components*	Datasheets
PSB	Heritage design from CBK, no detailed analysis for MSR	
DPB	GR740	<a href="#">User's Manual</a>
DCB	(pending)	<a href="#">Benchmark &amp; Power</a>
DFW/CUCB	SAMRH707 (see also Pauls slides)	<a href="#">User manual</a>
MTCB	SAMRH707	<a href="#">User manual</a>



Case			Total PCB Power [W]
IRT-DHU	Hot	Operational	36.5
IRT-DHU	Cold	Operational	29.38

\*Critical in terms of rated EEE components temperature ranges, ICs and FPGAs





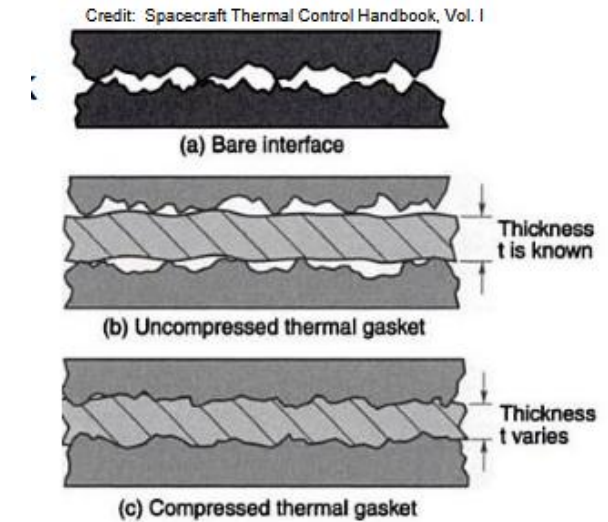
Material & Temper	Density $\rho$ (g/cm <sup>3</sup> )	Thermal conductivity $\kappa$ (W/m·K)	Specific thermal conductivity $\kappa/\rho$	Young's Mod. $E$ (GPa)	0.2% Yield Strength (MPa)	Specific stiffness $E/\rho$	Notes (Temper & General)	Datasheet Link
Al 6082-T6	2.70	180	66.7	69	260	25.6	<b>T6:</b> solution-treated & artificially aged for peak strength and machinability. Good balance of stiffness, thermal conductivity and machinability	BIKAR EN AW-6082 T6
Al 6061-T6	2.70	167	61.9	69	276	25.6	Higher tensile yield strength for the cost of lower thermal conductivity. <b>Will be used as baseline material for worst-case thermal simulations.</b>	MatWeb 6061-T6
Al 7075-T6	2.81	130	46.3	71	503	25.3	Further reduced thermal conductivity; much higher yield strength	MatWeb 7075-T6
Al-SiC MMC (AyontEX 13)	2.90 (2.54)	150 (134)	51.7 (52.8)	<b>140</b> (103)	350 (340)	48.3 (40.6)	+ Additional stiffness, lower coefficient of thermal expansion, conventional Al-coating techniques can be applied – Reduced machinability; procurement lead time and cost can be significantly higher than for conventional Al alloys	Materion AlSiC (Materion AISi)
Cu-OFE C10100	8.93	394	44.1	130	140/320 (temper R220/R360)	14.6	Highest $\kappa$ ; can be used for heat spreaders; strength depends strongly on temper	KME Cu-OFE (C10100)
CuCrZr CW106C	8.92	320	35.9	130	80/540 (temper s/aw)	14.6	Hardened copper: good $\kappa$ with higher yield	Müller GmbH CuCr1Zr
A286 steel UNS S66286	7.92	15.1	1.9	201	275	25.4	Fe-Ni-Cr hardened steel; high <b>fastener</b> strength	ATI A286

## Relevance of parameters:

- Higher specific thermal conductivity  $\frac{\kappa}{\rho} \rightarrow$  better (mass-normalized) heat transfer performance
- Higher Young's modulus  $\rightarrow$  reduced elastic deformation and improved vibration resistance
- Higher 0.2% yield strength  $\rightarrow$  greater margin of safety against plastic deformation (smaller than 0.2%) during mechanical loads

Optimize the thermal conductivity of the contact area between two stacked frames:

1. Specify flatness and roughness on the drawing on the surfaces that are in thermal contact (e.g. flatness over length and Ra; CMM and roughness report)
2. Aluminum 6061-T6 is the baseline material. Chromate-convert surfaces needed to be conductive (metal-to-metal thermal conductivity increases with better cleanliness, flatness and with electrically conductive surfaces)
3. Insert a compressible thermal interface material (**TIM**) between the surfaces. Chose thickness from measured flatness (Typical TIM thickness 0.1 – 0.3 mm, should include a margin (factor > 2) of measured flatness)
4. Ensure sufficient (see table below) and sustained clamping pressure (use Belleville washers) to compress the thermal gasket (see Fig. on the right)



TIM type (example)	Thermal Cond. (W/m·K)	@Compression	Notes (Material & General)	Datasheet Link
Indium Corp. Indium Heat-Spring	86	> 0.2 MPa < 0.7 MPa	99.99% Indium, 90In10Ag for thinner heat springs, avoid creep by overtightening	<a href="https://www.mateck.com">mateck.com</a> -> <a href="#">Indium</a> (DE Origin)
Panasonic GraphiteTIM; SGL Carbon Sigratherm	160 - 250	0.2 MPa	Graphite pad, thickness 200 – 350 µm, flight heritage to be evaluated. High in-plane k, lower through plane; fragile.	<a href="https://www.panasonic.com">panasonic.com</a> --> <a href="#">GraphiteTIM</a> (Japan origin) <a href="https://www.sglcarbon.com">sglcarbon.com</a> --> <a href="#">sigratherm</a> (DE origin)
Parker CHO-THERM; Saint-Gobain – ThermaCool	2.1	3 MPa	Electrically insulating, more interesting for cooling of EEE components	<a href="https://www.parker.com/">https://www.parker.com/</a> (US-based) <a href="https://www.saint-gobain.com">saint-gobain.com</a> -> <a href="#">tc3008</a> (FR origin)
Parker THERM-A-GAP Kerafol Gap Pad	8.3	0.3 MPa	For thick gaps (0.5 – 2 mm), be careful to select low-volatility grade	<a href="https://www.parker.com">parker.com</a> --> <a href="#">therm-a-gap-pad</a> (US-based) <a href="https://www.kerafol.com">kerafol.com</a> -> <a href="#">g ap-pads</a> (DE origin)



Details of assumptions in the thermal mathematical model (TMM):

- Stiffeners touch bottom and top board and create additional heat path through the box.
  - Interface between PCBs and the upper stiffener with thermal glue ([Henkel STYCAST 2850 FT](#) as example), 0.2 mm thickness ( $\kappa = 1.25 \text{ W/m}\cdot\text{K}$ ). PCB to lower frame: Cu to chromated frame, bolted,  $600 \text{ W/m}^2\cdot\text{K}$ .
- 2D simplification with associated 2D mesh thickness delivers more realistic results for thin objects while saving nodes.
- PCBs are orthotropic material with thermal conductivity of  $64.3 \text{ W/m}\cdot\text{K}$  in-plane and  $0.379 \text{ W/m}\cdot\text{K}$  through-plane.
- Housing material is Al6061., no copper rods
- TIM between housing of stacks lead to high heat transfer coefficient.

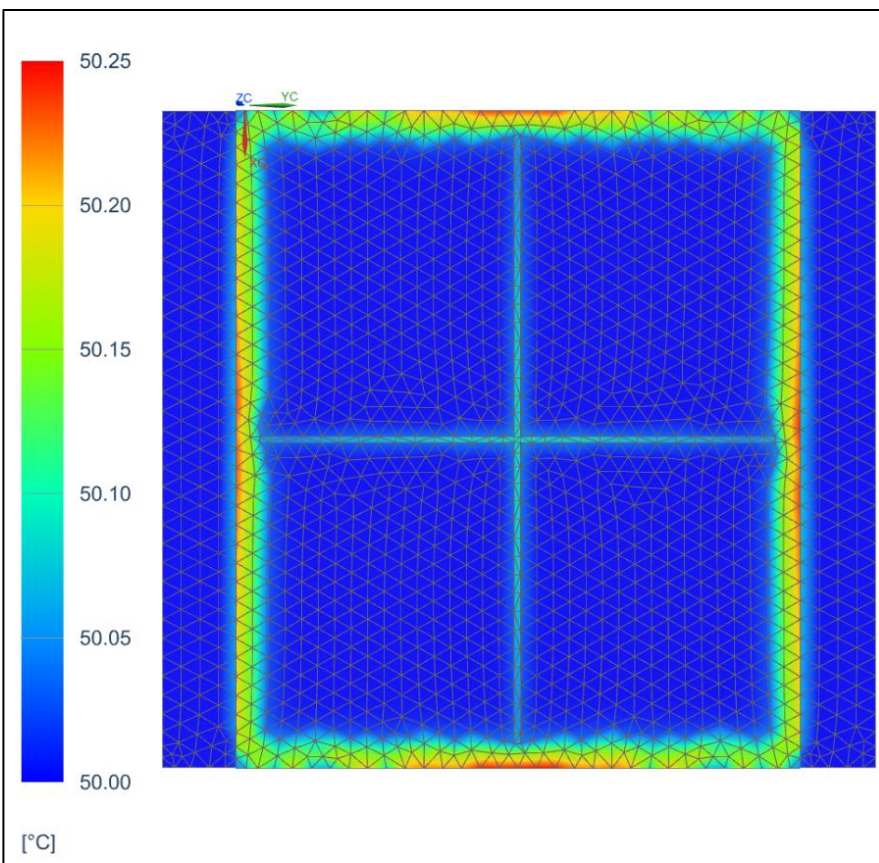


## R-INST-IF-THM-0580

*For all instrument units mounted in the SC, the absolute maximum temperature gradient difference Peak to Valley within the baseplate interface plane shall be  $< 3\text{ K}$  (TBC).*

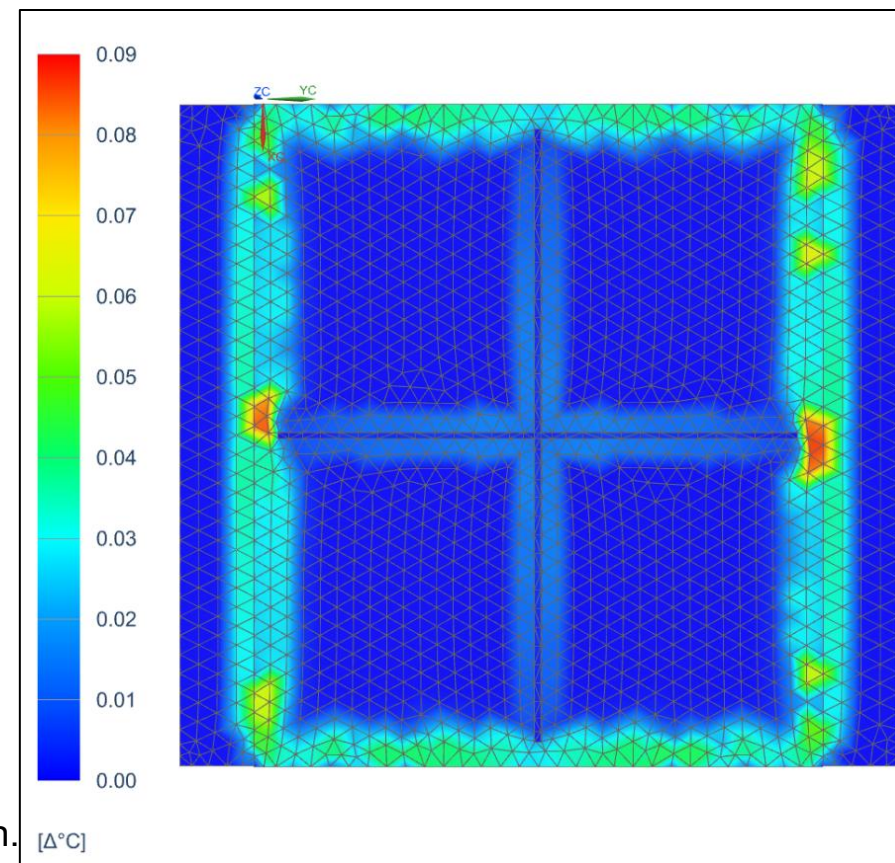
→ Simcenter 3D (Solver: Thermal/Flow v.2506.3), housing material (Al6061-T6), housing thickness 6mm

→ conductance between the box and the platform is assumed to be  $500\text{ W/m}\cdot\text{K}$



✓ Well below 3K

Right: Corresponding node error estimates in the solution.



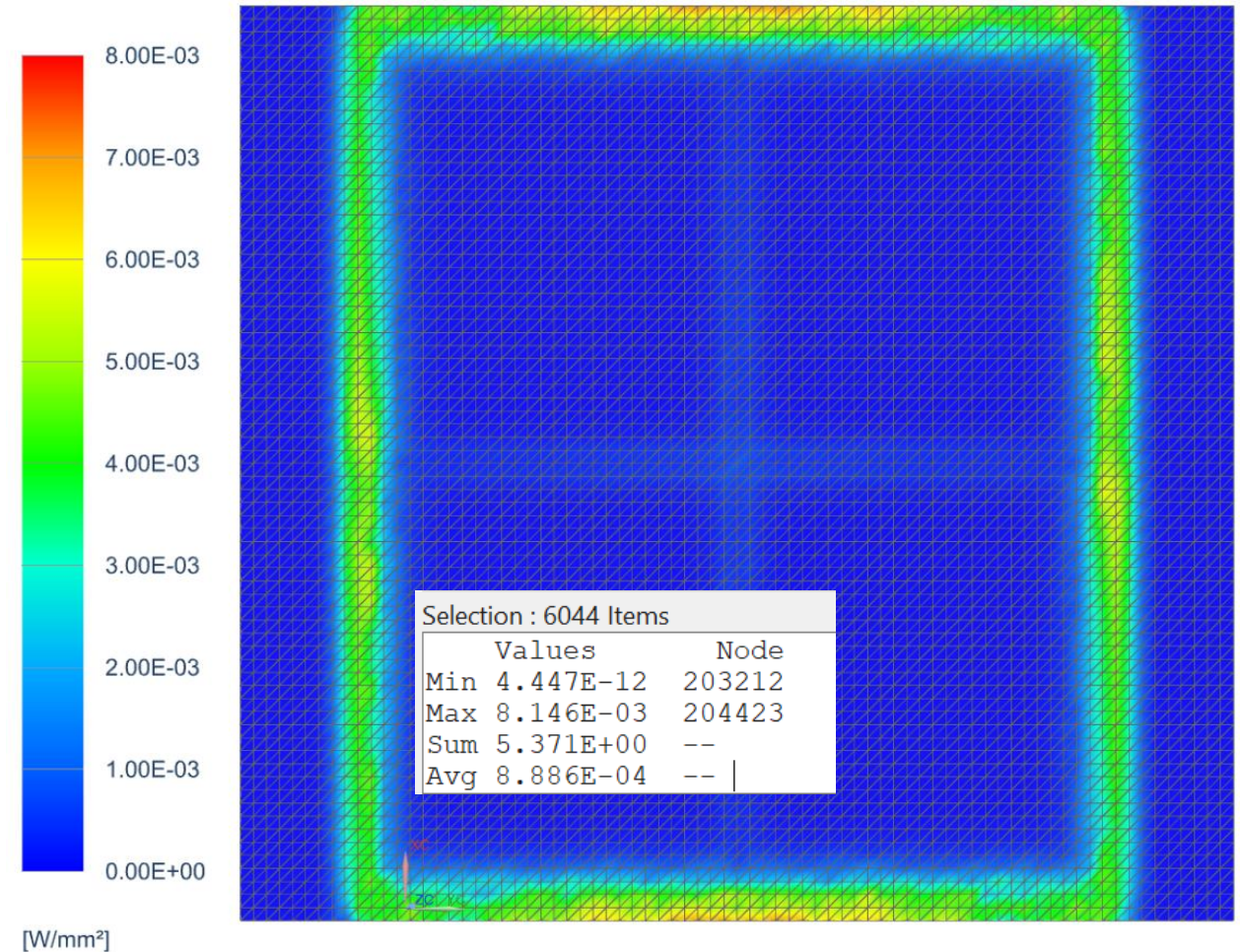


## R-INST-IF-THM-0590

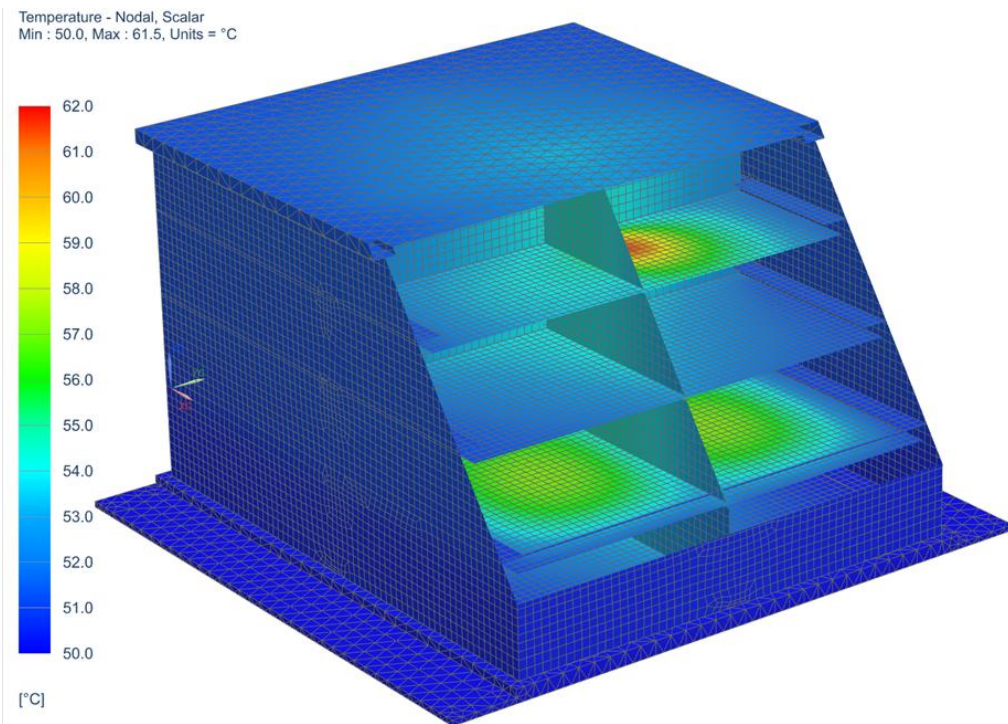
For all instrument units mounted on the SC, the maximum local **baseplate conductive heat flux density** shall not exceed 1.5x the average heat flux density. The average heat flux density shall not exceed:

- for  $A \leq 100 \text{ cm}^2$ : **2100 W/m<sup>2</sup>**
- for  $100 \text{ cm}^2 \leq A \leq 300 \text{ cm}^2$ : **1100 W/m<sup>2</sup>**
- for  $300 \text{ cm}^2 \leq A \leq 1000 \text{ cm}^2$ : **540 W/m<sup>2</sup>**
- for  $1000 \text{ cm}^2 \leq A \leq 2000 \text{ cm}^2$ : **850 W/m<sup>2</sup>**

Figure 10-1: Conductive flux of the baseplate per node (preliminary). Average is  $8.9 \cdot 10^{-4} \text{ W/mm}^2 = 890 \text{ W/m}^2$ . As the node size is very small this is probably below the requirement. The maximum is though larger than 1.5 times the average.



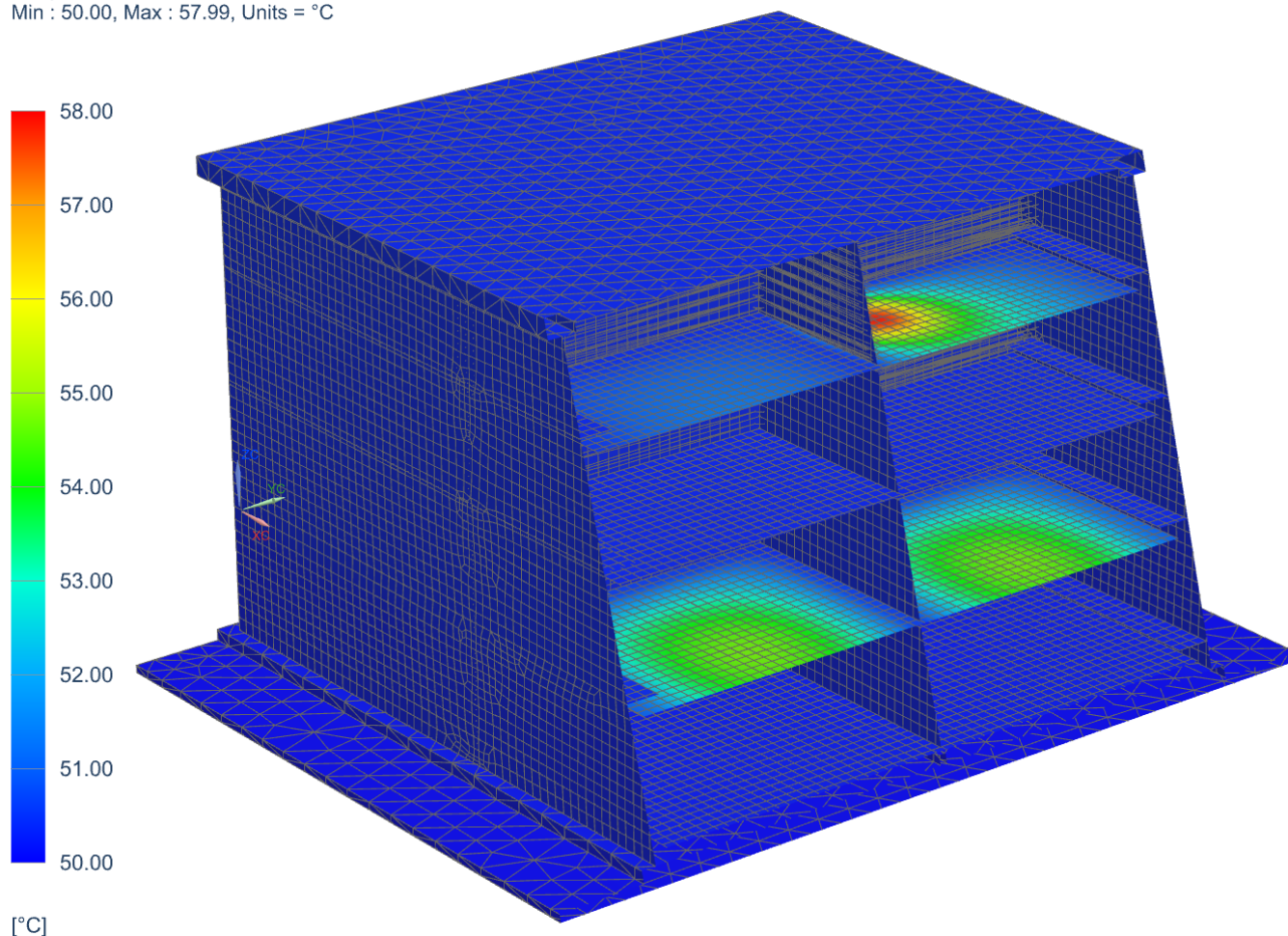
1. Board design temperature must be below 85°C
  2. S/C interface temperature in the hot case is +50°C, -40°C in the cold case
  3. Critical EEE-components are identified, goal is to verify their rated temperature limits
- Determine the thermal conductivity of the DHU box required to keep the components within their limits
  - **Vary thickness of housing** in the thermal mathematical model (TMM)
  - Simulations in Simcenter 3D include more details than MCR simulations in SolidWorks (e.g. thermal/mechanical couplings specified)



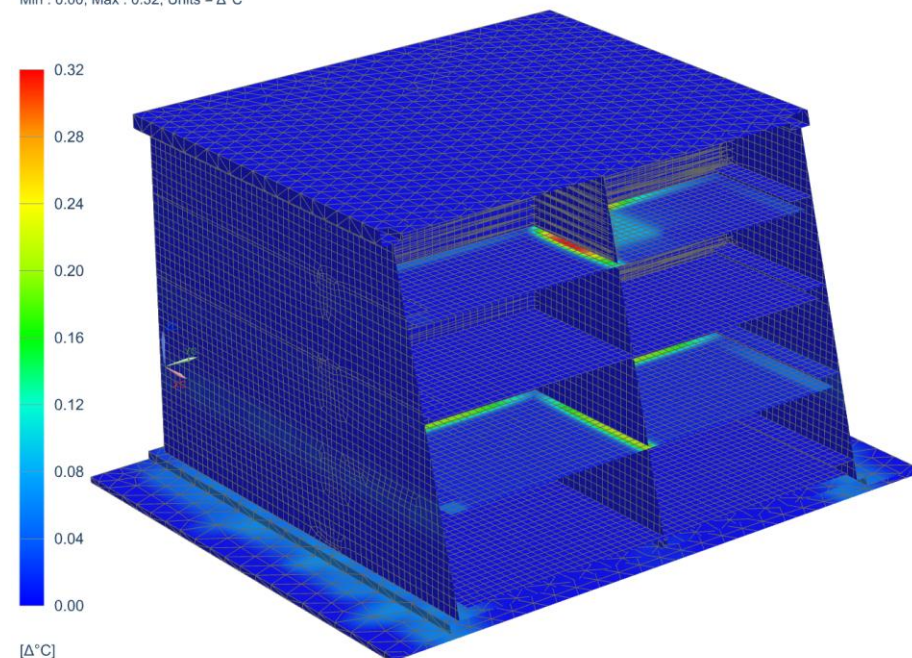
Left: RTMM of IRT-ICS DHU with four stacked boards. Second board from bottom is the PSB with average power across the board, as components are not yet fixed. Topmost board includes the GR740 CPU.



Temperature - Nodal, Scalar  
 Min : 50.00, Max : 57.99, Units = °C



Temperature Error Estimates - Nodal, Scalar  
 Min : 0.00, Max : 0.32, Units = Δ°C

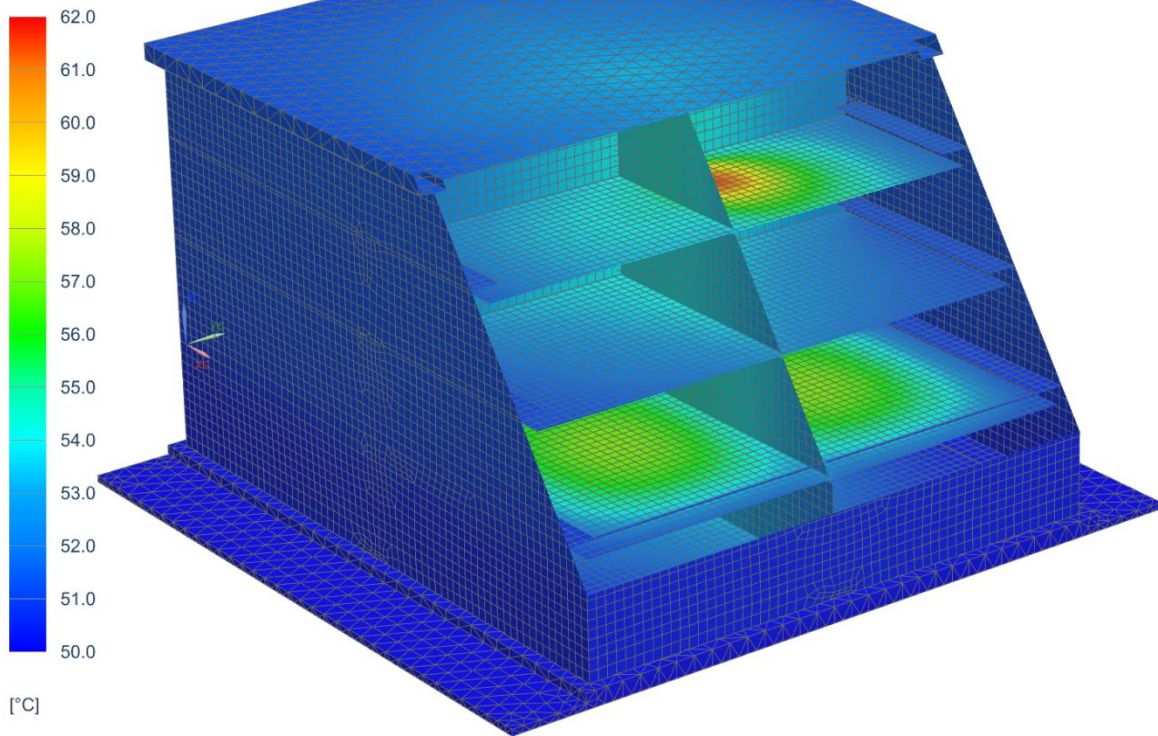


Error estimates of the model due to coarse node density and correspondingly unaligned nodes at interfaces (final model could use mapped nodes)

Board temperatures (OP HC) with 8 mm effective housing thickness (very thick). The corresponding junction temperature of the GR740 are about 6°C higher with CLGA package (thermal resistance 1.4°C/W, max. power 4.3 W). Number of nodes is about 43k, maximum number of nodes as defined in ESA-THESEUS-PLD-RS-001 is 100k.

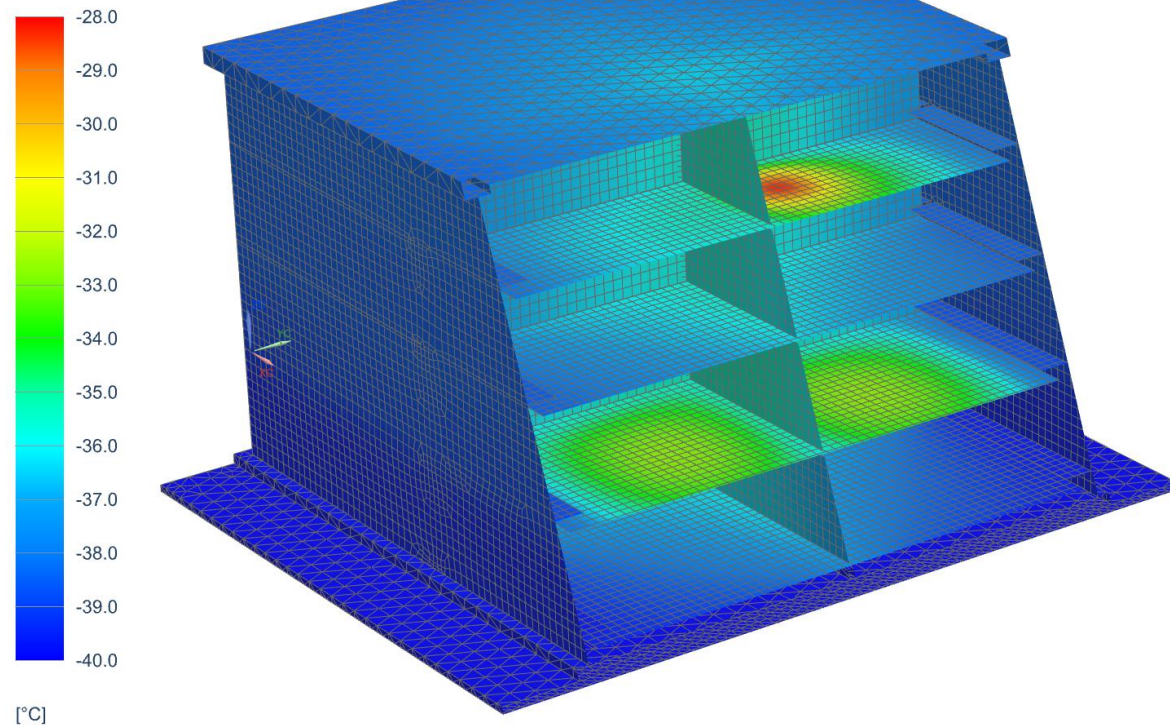


Temperature - Nodal, Scalar  
Min : 50.0, Max : 61.5, Units = °C



Board temperatures (OP HC) with 6 mm effective housing thickness (reasonable for 8 mm base thickness with lightweighting and steel screws). Maximum board temperatures is about 4K higher than with 8 mm effective housing thickness, junction temperature of the GR740 would be about 67°C to **82°C**, depending on package used.  
→ Op Tmax. +50°C is likely ok

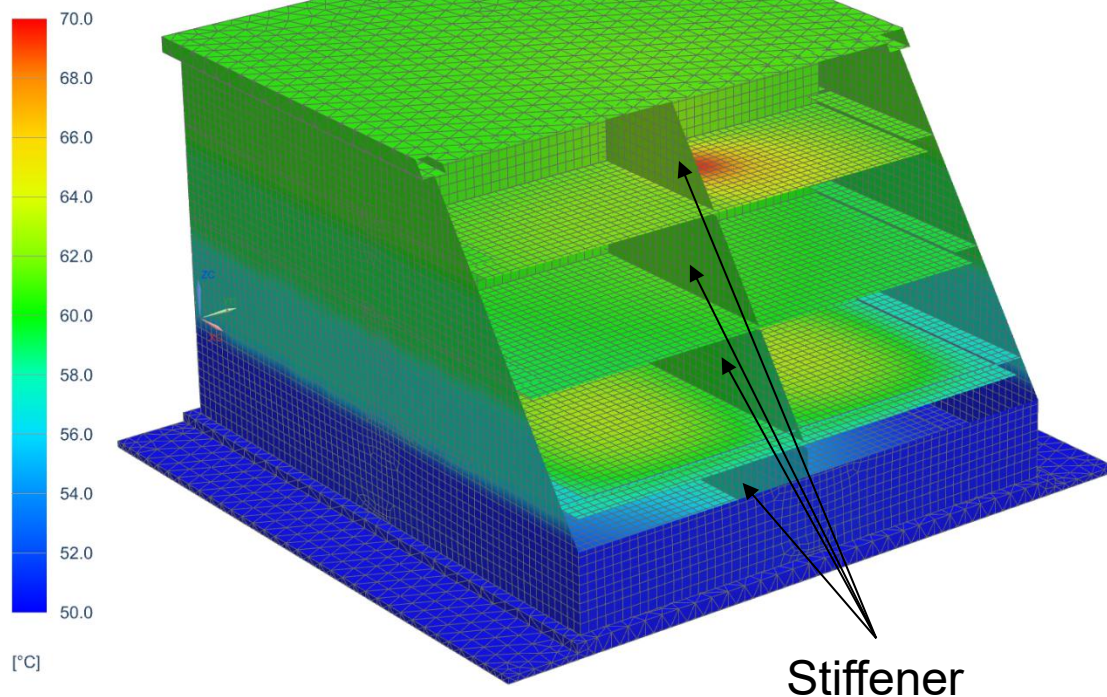
Temperature - Nodal, Scalar  
Min : -40.0, Max : -28.2, Units = °C



Operating cold case board temperature below GR740 is at -28°C. Junction temperature should be at least -15°C to include all margins (5 K qualification and 5 K acceptance margins, plus 15 K uncertainty), as the min. operating junction temperature of the GR740 is at -40°C, which is realistic with CCGA package. → Op Tmin. -40°C is likely ok



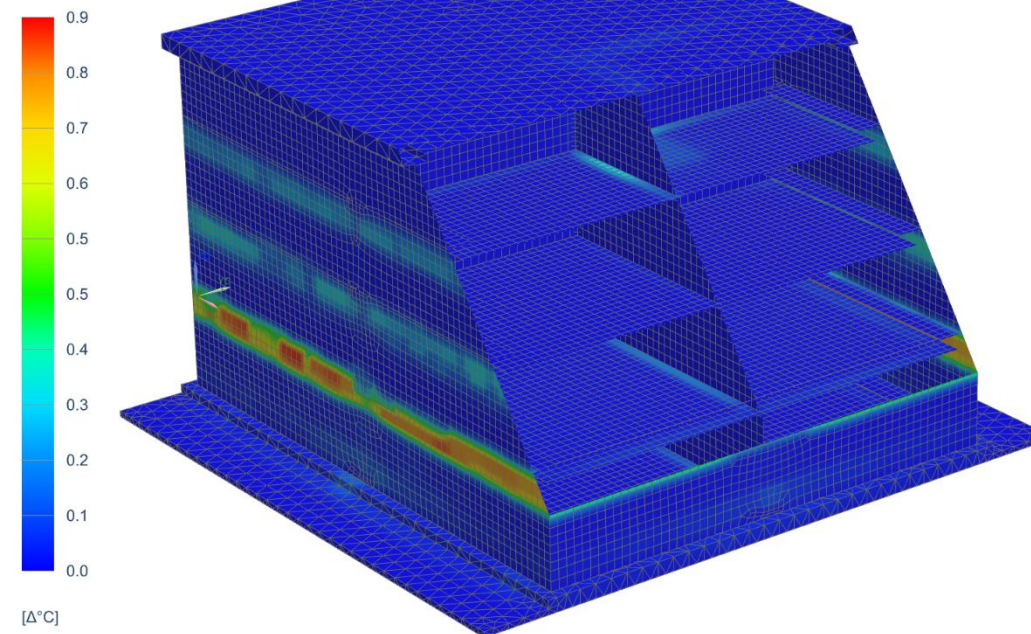
Temperature - Nodal, Scalar  
Min : 50.0, Max : 69.5, Units = °C



Board temperatures with only thin side walls to show the heat conduction path through the 2 mm thick stiffeners. → Compared to MCR DTMM, stiffeners provide an additional heat path to the S/C interface

Model details (rehearsal): Interface between PCBs and the upper stiffener with thermal glue (Henkel STYCAST 2850 FT), 0.2 mm thickness ( $\kappa = 1.25$  W/m·K). PCB to lower frame: Cu to chromated frame, bolted, 600 W/m<sup>2</sup>·K.

Temperature Error Estimates - Nodal, Scalar  
Min : 0.0, Max : 0.9, Units = Δ°C



Only error estimates in unimportant thin side walls are high, but board temperatures are well-estimated.

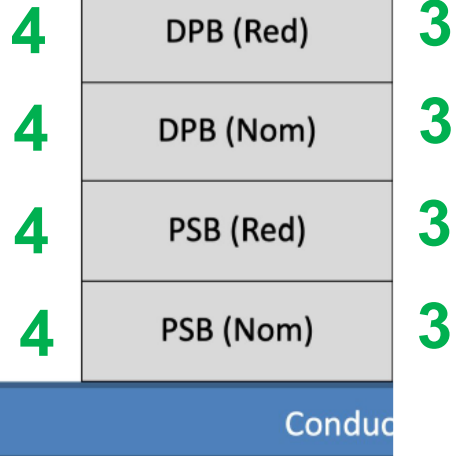




- Simcenter 3D simulations with more detailed thermal/mechanical interfaces than MCR SolidWorks model.
- 2D-simplifications of thin elements (PCBs, stiffeners) saves nodes and is more realistic
- Effective housing thickness of 6 mm seems optimal, fine adjustments in preparation (1 mm steps)
- Simulation with board temperatures below EEE-components in IRT-ICS ECU is in preparation
- Min. junction temperature of the GR740 is only -40°C (storage -55°C)
  - But: Op min and switch on are also at -40°C (no buffer for margins)
  - Also, non-op Tmin should be updated to -45°C. (already commented in EID-A v1.2 draft).



# Connector overview IRT-ICS DHU



Board	To	Purpose	F / B <sup>(3)</sup>	Connector Type	Connector ID
PSB(M/R) SVM	SVM	Voltage monitoring (new)	Front	MDM-15 (TBC)	J11 (J21)
PSB(M/R) SVM	SVM	Primary power	Front	DEMA9S <sup>(2)</sup>	J12 (J22)
PSB(M/R) DPB	DPB	Secondary power	Front	DEMA9S <sup>(2)</sup>	J13 (J23)
PSB(M/R) DPB	DPB	HK/TM/TC	Front	MDM-9 <sup>(1)</sup>	J14 (J24)
PSB(M/R) FW/CUCB	FW/CUCB	Secondary power	Back	<b>DEMA15S</b>	J15 (J25)
PSB(M/R) DCB	DCB	Secondary power	Back	DEMA9S <sup>(2)</sup>	J16 (J26)
PSB(M/R) MTCB	MTCB	Secondary power	Back	DEMA9S <sup>(2)</sup>	J17 (J27)
DPB(M/R) SVM	SVM	SpaceWire to SVM	Front	MDM-9 <sup>(1)</sup>	J31 (J41)
DPB(M/R) SVM	SVM	Synchronization line to SVM	Front	MDM-9 <sup>(1)</sup>	J32 (J42)
DPB(M/R) PSB	PSB	Secondary power	Front	DEMA9S <sup>(2)</sup>	J33 (J43)
DPB(M/R) PSB	PSB	HK/TM/TC	Front	MDM-9 <sup>(1)</sup>	J34 (J44)
DPB(M/R) FW/CUCB	FW/CUCB	CAN: HK/TM/TC	Back	MDM-9 <sup>(1)</sup>	J35 (J45)
DPB(M/R) MTCB	MTCB	CAN: HK/TM/TC	Back	MDM-9 <sup>(1)</sup>	J36 (J46)
DPB(M/R) DCB	DCB	SpaceWire: HK/TM/TC	Back	MDM-9 <sup>(1)</sup>	J37 (J47)

Figure: IRT-ICS DHU boards and (“Nom” are Main/M) and the total connectors as defined in Table

Table: Boards and connectors for Main (M) and Redundant (R) boards of the IRT DHU according to IRT ICS 7.1.0. Entries in black as defined during MCR, blue entries are TBC and derived from the updated EID-A 1.2 and IRT\_PSB\_definition\_V0 document. Note: SQ version of SUBD9 is DEMA9P

(1) Per connector with EMI backshell (ESCC 3402/078 lightweight, top circular) and 2x screw assembly (ESCC 3401/032 var. 18)

(2) Per connector (variant 01) with grommet

(3) Optimal side in terms of harness length/mass. Front (F): SVM; Back: IRT-ICS DHU connections. Internal connectors are then placed on side with most space left



4

2

2

2

2

DCB	2
FW/CUCB (Red)	2
FW/CUCB (Nom)	2
MTCB (Red)	2
MTCB (Nom)	2
Active I/F	

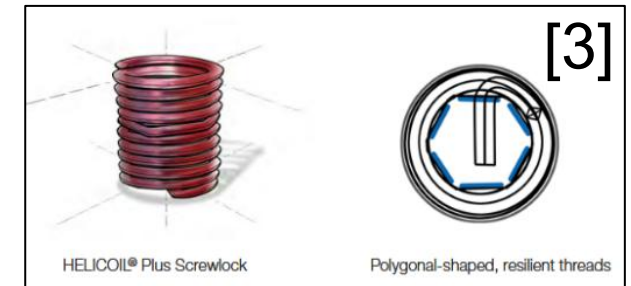
From	To	F/B <sup>(1)</sup>	Function / Purpose	Connector Type	ESCC Spec
DCB	DHU/PSB	Front	Secondary power - M	DEMA9S <sup>(2)</sup>	3401/002
DCB	DHU/DPB	Front	SpaceWire: HK/TM/TC - M	MDM-9	3401/029
DCB	DHU/PSB	Front	Secondary power - R	DEMA9S <sup>(2)</sup>	3401/002
DCB	DHU/DPB	Front	SpaceWire: HK/TM/TC - R	MDM-9	3401/029
DCB	IRT/SIDECARD	Back	SIDECARD interfaces	<b>MDM-51</b>	3401/029
DCB	IRT/FPA	Back	Thermal sensors & heater regulation	MDM-15	3401/029
FW/CUCB(M/R)	IRT/CU	Back	Calibration Unit interfaces	<b>MDM-37</b>	3401/029
FW/CUCB(M/R)	IRT/FW	Back	Filter Wheel assembly interfaces	<b>DBMA25S</b>	3401/002
FW/CUCB(M/R)	DHU/PSB	Front	Secondary power	<b>DAMA15S</b>	3401/002
FW/CUCB(M/R)	DHU/DPB	Front	CAN to DHU	MDM-9	3401/029
MTCB(M/R)	IRT/CAM	Back	Thermal sensors on CAMERA	<b>MDM-25</b>	3401/029
MTCB(M/R)	IRT/TEL	Back	Thermal sensor & heater (telescope mirror)	<b>DCMA37S</b>	3401/002
MTCB(M/R)	DHU/PSB	Front	Secondary power	DEMA9S <sup>(2)</sup>	3401/002
MTCB(M/R)	DHU/DPB	Front	CAN to DHU	MDM-9	3401/029

(1): Placement to reduce harness mass. Connectors with cables connected to the **IRT-ICS DHU** are placed on the “front”, correspondingly for **IRT/-CAM/-TEL etc. on the “back”**. **There are no internal connectors on IRT-ICS ECU**



# DHU box – Concept of the thermal design

Function	Part used	Image illustration
Alignment of two stacks, stability in y-, x-direction	Dowel pins	[1]
Tension between lid and bottom for TIMs	M6 tie rods	[2]
Main tie-points of M6 rods	Threaded inserts	[3]



## Most important changes:

1. Copper rods are not used as thermal path, as their specific thermal conductivity is lower (could still save space to use).
2. Still M6 tie rods run through the units, but to provide tension between the stacked frames and compress the TIM between the housing.
3. Stiffeners do have contact with the PCBs on both sides (one side glued, other side bolted)



# Thanks for listening!

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