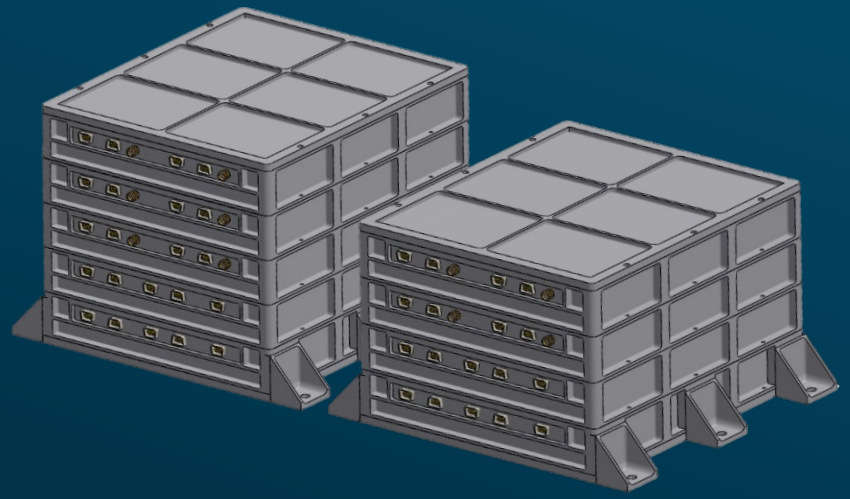
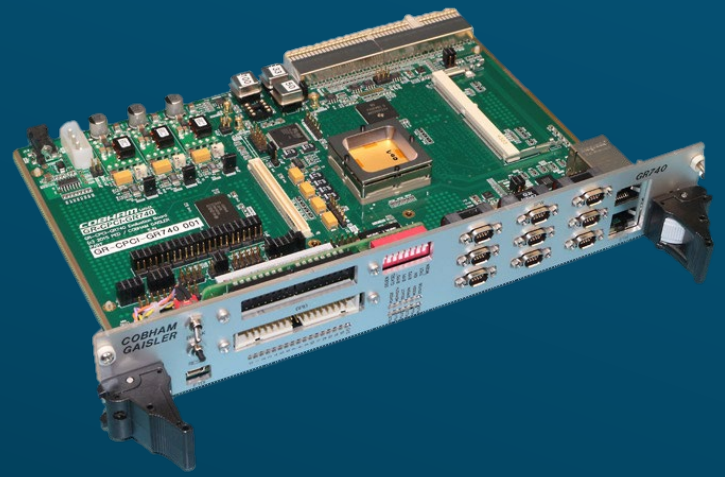




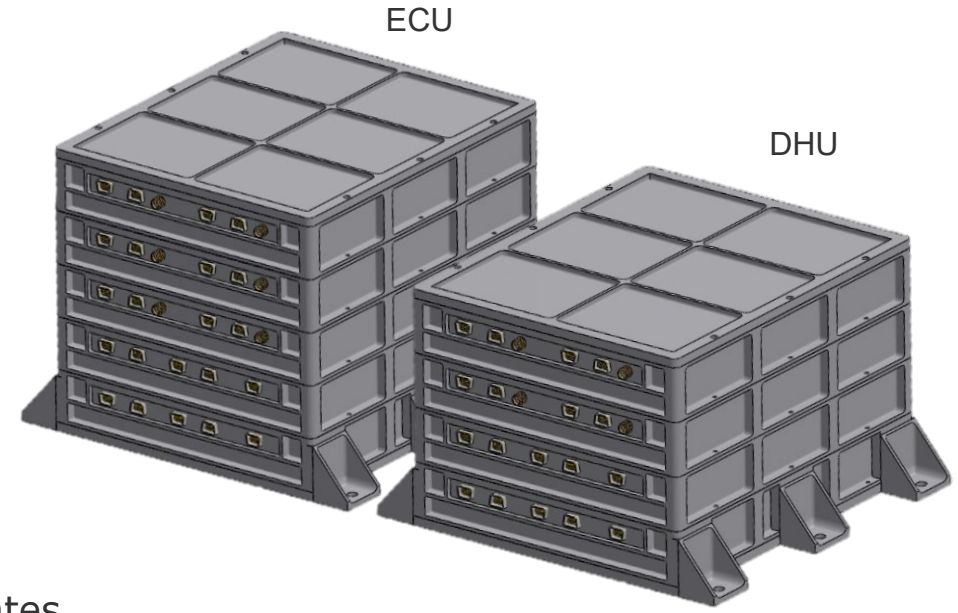
IRT ICS Baseline & Trade-offs

Mariachiara Celato

on behalf of the IAAT IRT Team

IRT-ICS Baseline Configuration

- **IRT Instrument Control System**
  - **1x Data Handling Unit**
    - Data Processing Board (N+R)
    - Power Supply Board (N+R)
  - **1x Electronics Control Unit**
    - Detector Control Unit (N)
    - Filter Wheel & Calibration Unit Control Board (N+R)
    - M2 Thermal Control Board (N+R)



- **Two aluminium boxes comprising stacked PCB frames**
  - See Lauro Conti's presentation for latest design/analysis updates
  - M5 box design still baseline, but redesign study ongoing
  - Mass budget will be updated accordingly

- **Data Processing Baseline:**
  - Frontgrade-Gaisler GR740
  - Software written in C using RTEMS
  - Alternative baselines remain as open or future trade-off studies

Trade-off Study Status

KOSMOS

Baseline: C code built on RTEMS
Trade-off: KOSMOS Flight Software + Xtratum Hypervisor

Latest Updates:

- 3 month KOSMOS evaluation study was scheduled to kick-off in September
- Evaluation plan was drafted in collaboration with DTU Space (for XGIS)
- Due to administrative complications both groups have agreed to postpone the evaluation period until after MSR (March/April 2026)
  - Purchase of Xtratum license from Fentiss has been put on hold
- Meeting scheduled for end of November to discuss roadmap for KOSMOS porting/qualification for next-generation processors

Trade-off study is postponed, but will be documented for MSR and completed on Phase A funding

DHU Processor

Baseline: GR740
Trade-off: GR765

Advantages:

- GR765 provides significant increases in all specifications
- Confirmed backwards compatibility with GR740
  - Smooth transition of SW development
- Flash controller simplifies DPB mass memory design

Disadvantages:

- GR765 is unqualified, with reduced TRL
- Release date unknown (as of 17/10/2025)
  - Target release was October 2025
  - Recently delayed by up to a year
  - "No guarantee of product launch"

Trade-off study is therefore postponed to Phase B

GR740

- **250** MHz Quadcore LEON 4FT with dedicated FPU and MMU
- **459** DMIPS per core
- **4** GB SDRAM
- **8**x SpaceWire Ports (up to 200 Mbps full-duplex)
- Integrated SpaceWire Routing Switch
- CCSDS/ECSS 5-channel Telecommand encoder/decoder
- MIL-STD-1553, CAN, High-speed Ethernet, SPI, PCI

GR765

- **800** MHz Octacore LEON 5FT with dedicated FPU and MMU
- **2600** DMIPS per core
- **16** GB DDR2/3/4 RAM
- **12**x SpaceWire Ports (up to 200 Mbps full-duplex)
- Integrated SpaceWire Routing Switch
- ONFI 4.0 NAND Flash interface
- And more…

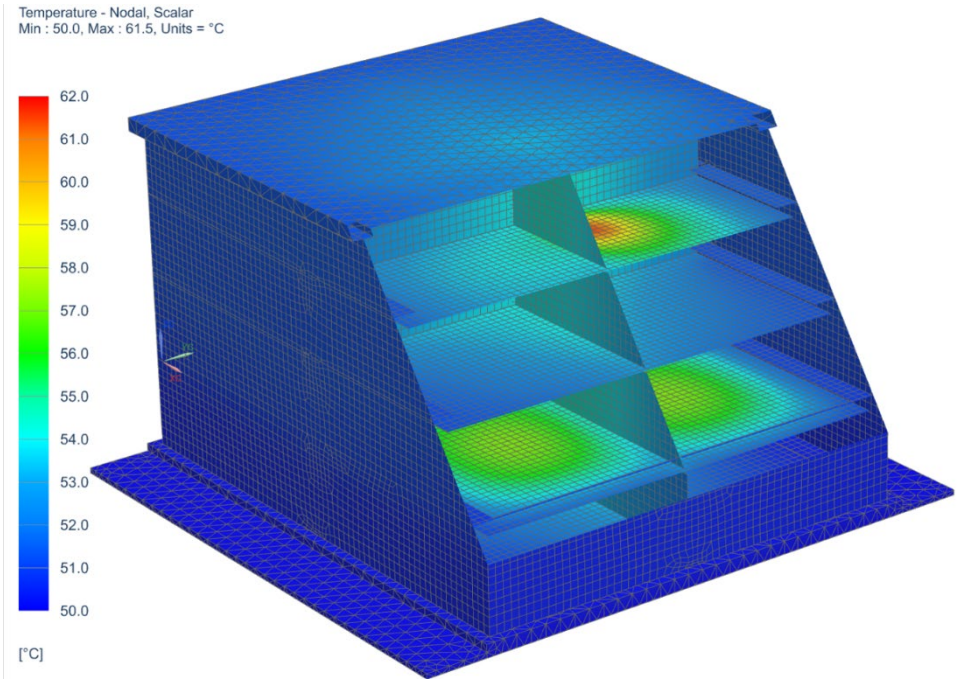
ICS Mechanical Redesign

Mechanical redesign trade-off study is ongoing

- Latest designs will be presented in ICS Mechanical presentation later today
- Design decisions will be implemented in the next two weeks

Impact on MSR datapack (w.r.t MCR):

- Updated CAD models for IRT-DHU & IRT-ECU
- Corresponding FEA models & reports
- Updated Mass Budget



Trade-off study will be closed pre-MSR

Additional Updates

- **Filter Wheel Control Unit**
  - IAAT now has a functional block diagram of Top-turn sensor & encoder ring readout electronics
  - Design is based on EUCLID, so we need to clarify with Geneva what can be shown in MSR documentation/presentations without going to jail

- **Calibration Control Unit**
  - Full feasibility study determined to be outside scope of Phase A for IAAT
  - Compatibility of CUA control requirements with chosen microcontroller (SAMRH707) is being assessed

Thanks for listening!

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