NUCLÉAIRE & PARTICULES

Omega

ÉCOLE POLYTECHNIQUE

IP PARIS

CALOROC for SiPM readout
EIC calorimetry

EAP 2025

September 26 - 2025

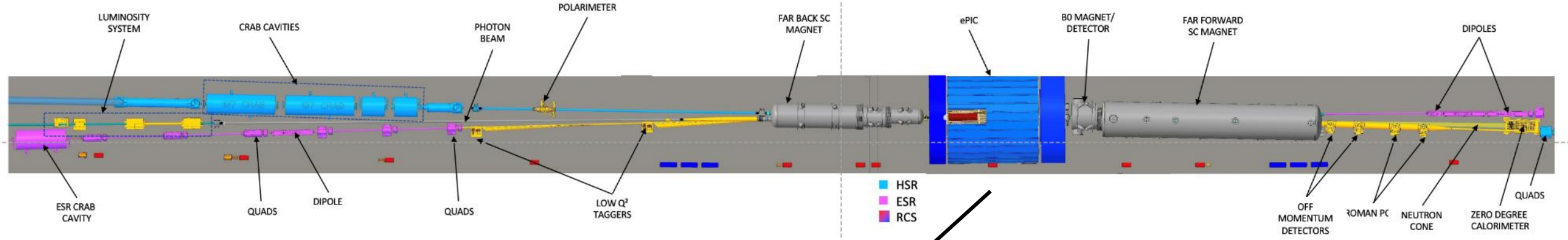
F. Dulucq

AGH

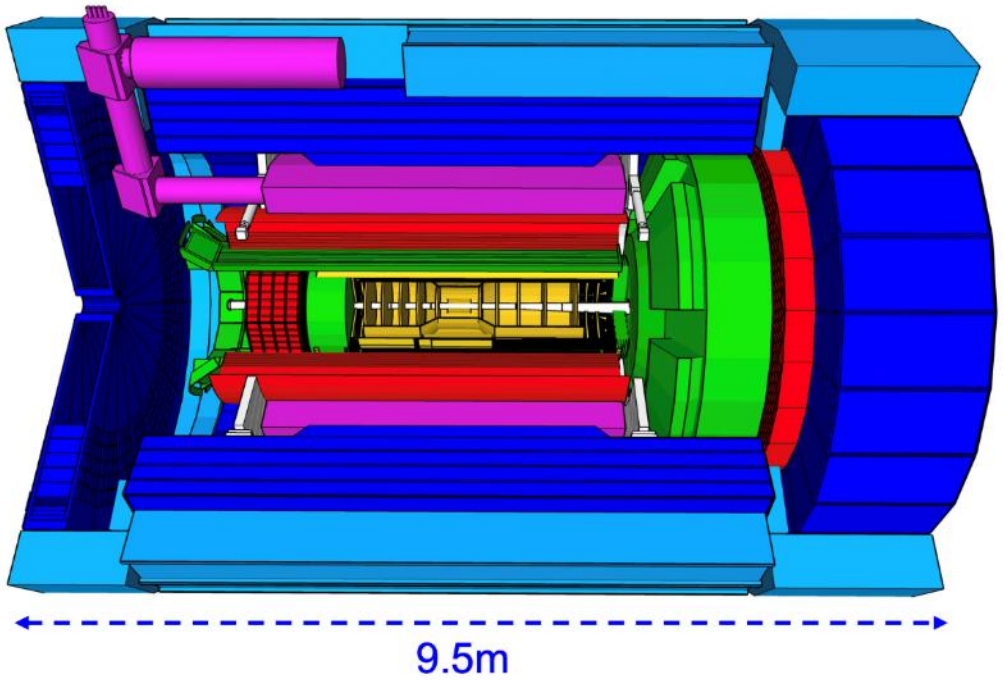
Irfu

Organization for Micro-Electronics desiGn and Applications

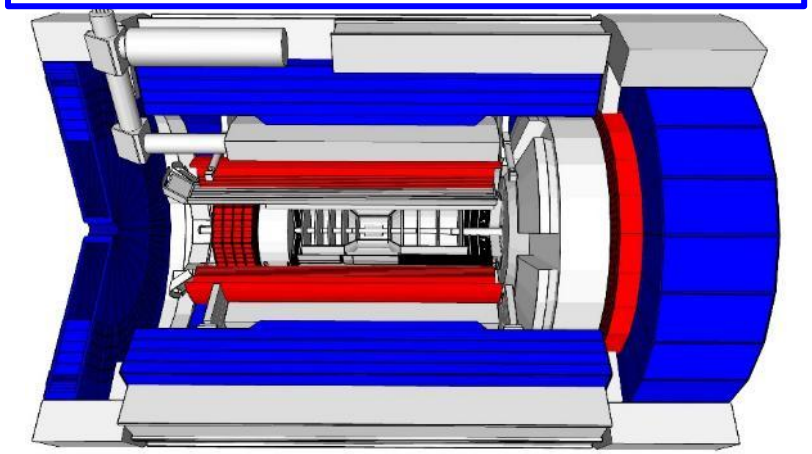
ePIC calorimetry SiPM-based



- hadronic calorimeters
- Solenoidal Magnet
- e/m calorimeters (ECal)
- Time.of.Flight, DIRC, RICH detectors
- MPGD trackers
- MAPS tracker



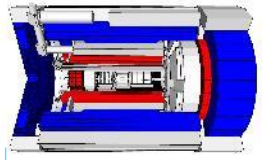
Backward HCAL
Barrel HCAL
Forward HCAL

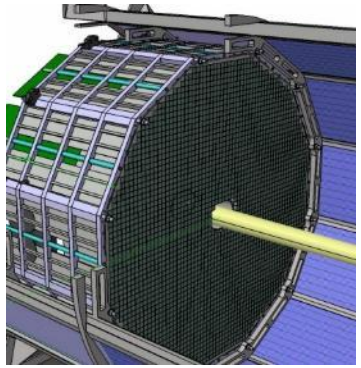
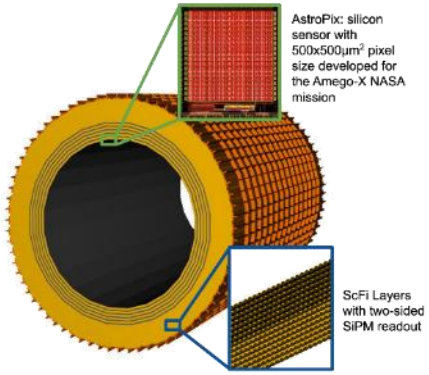
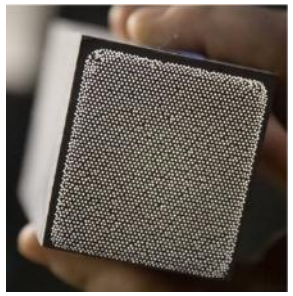
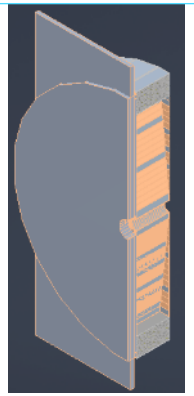
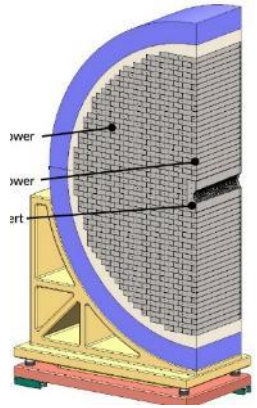


~ 10 ns bunch structure with stream readout

Backward ECAL
Barrel ECAL
Forward ECAL

ePIC Calorimetry



Backward ECal	Barrel ECal	Forward ECal	Backward HCal	Barrel HCal	Forward HCal
					
Main Function					
scattered lepton detection → very high-precision	scattered lepton and γ detection, hadronic final state characterization	lepton and γ detection, hadronic final state characterization → π^0, γ separation	muon and neutral detection → improved jet Energy reconstruction	muon and neutral detection → improved jet Energy reconstruction	particle-flow measurements
Proven Technology					
PbWO4 – crystals → long lead procurement	Pb/SciFi sampling part using SiPMs combined with imaging section (6 layers) interleaving Pb/SciFi with ASTROPIX	Tungsten-powder + SciFi SPACAL design Developed through EIC R&D and applied successfully in sPHENIX	Steel + Scintillator SiPM-on-tile	Steel + Scintillator design re-used from sPHENIX	longitudinal segmented Steel + Scintillator SiPM-on-tile Pioneered by CALICE analog HCal High resolution insert next to beam-pipe
IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis; OMEGA Microelectronics	Use of ASTROPIX in Calorimetry	world's first at ePIC			first-time full-size CALICE like calorimeter in collider experiment

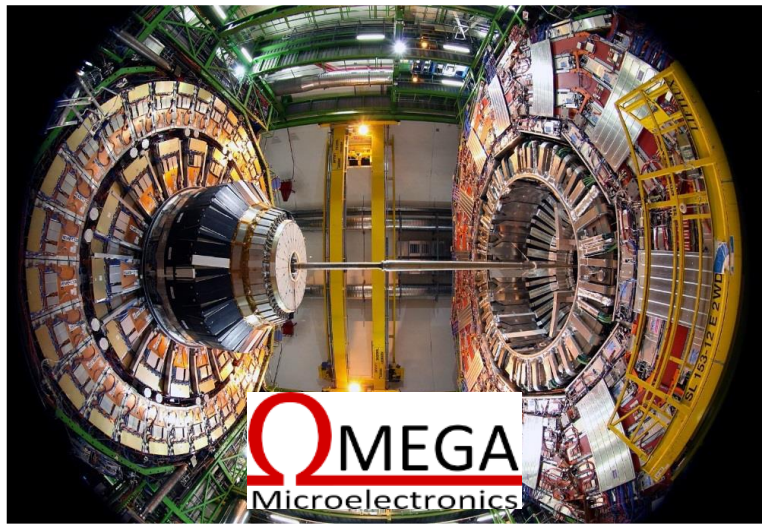
From CMS SiPM readout to CALOROC

H2GCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year



CALOROC for EIC

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

Common interfaces

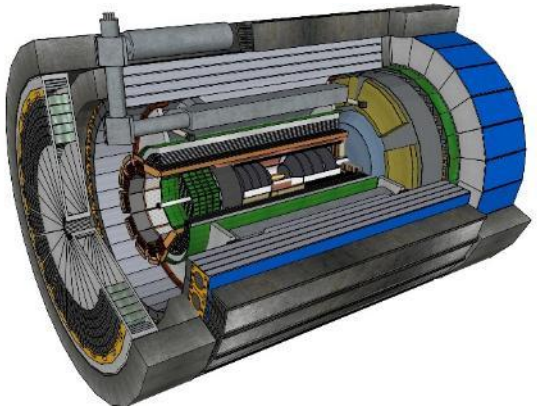
HEP trend => imaging calorimetry

- ❑ High number of channels
- ❑ Charge and precise timing (<100 ps)
- ❑ Low power + System-On-Chip

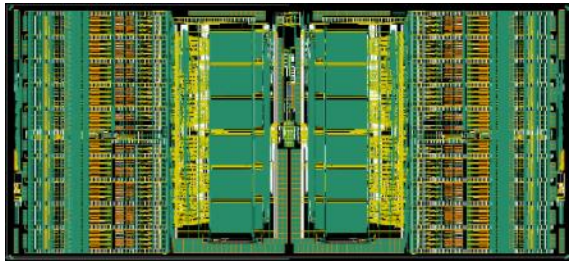
CALOROC will minimize the risk by reusing H2GCROC verification framework and reusing the 130 nm node (IN2P3 CS recommendations)

What is CALOROC ?

- CALOROC will be available in 2 versions for SiPM readout:
  - SiPM range capacitance from 500 pF to 10 nF
  - ~ 10-15 mW / channel
  - Radiation hardening (HL-LHC levels)
    - 200 Mrad and 10^{16} n_{eq} / cm^2 (1 MeV equivalent neutrons)
    - SEE hardening on control logic
  - Charge and time measurement



HGCROC



HKROC

- Streaming readout (no external trigger required)
- Conservative CALOROC1A based on CMS H2GCROC:
  - H2GCROC (ADC, TOT) analog/mixed reuse
  - Back-end compatible with EIC + zero-suppress
- New CALOROC1B based on gain switching:
  - New analog part without TOT (dynamic gain switching)
  - Backend « à la HKROC »: auto-trigger, zero-suppress – EIC compatible

CALOROC 1A
CMS front end
EIC readout

CALOROC 1B
New front end
EIC readout

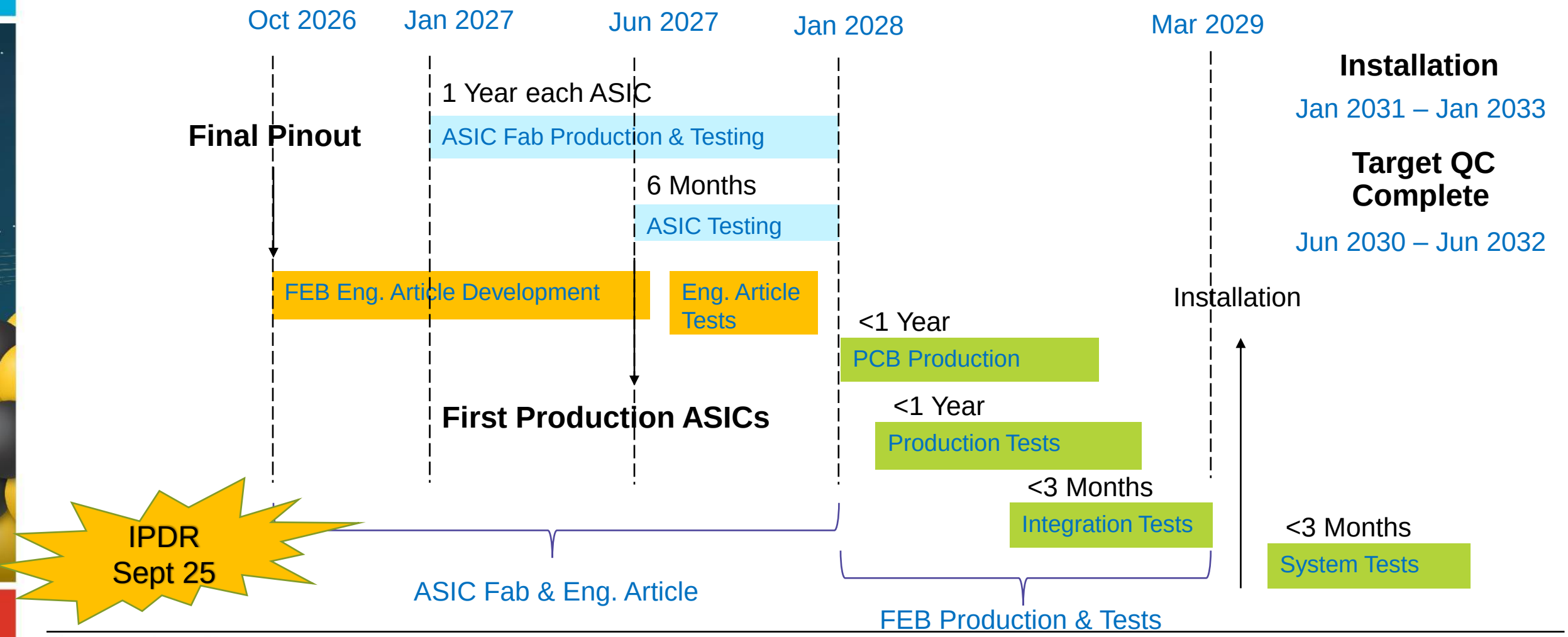
CALOROCs will share a common backend
+ pin-pin compatibility

Timeline cont. - Development

NOTE: FEB designs are contingent upon final ASIC pinout/package design.

Charge 3, 4

Example: Final Design FY27 ASIC Submission



➢ *Also refer to backup materials*

CALOROC Project at OMEGA in 2025

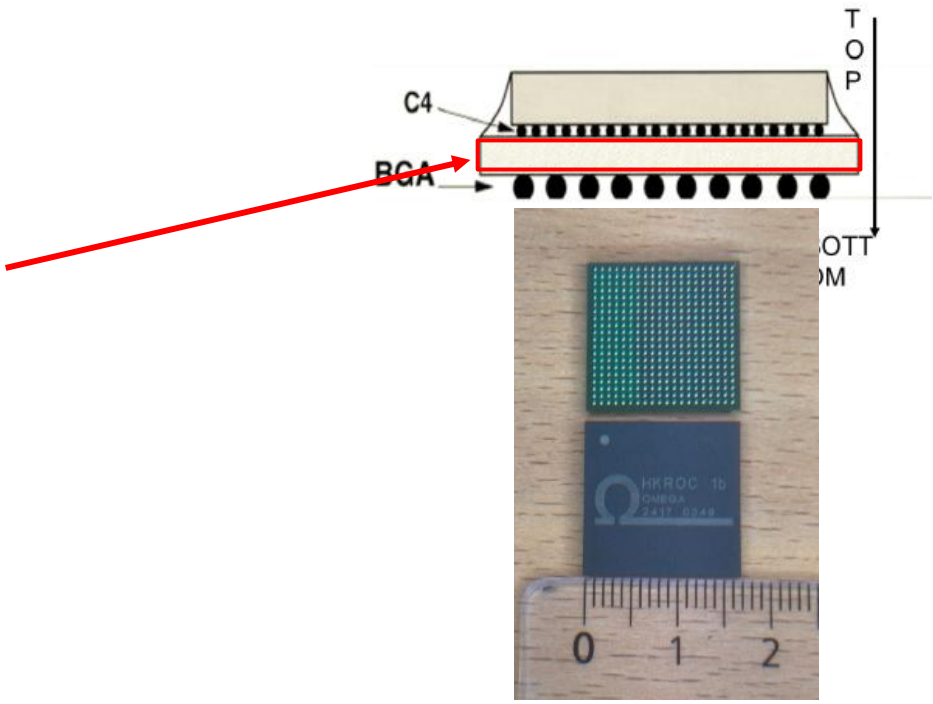
- ~3,7 FTE involved with one Thesis (Pedro – ending in Jan 27)

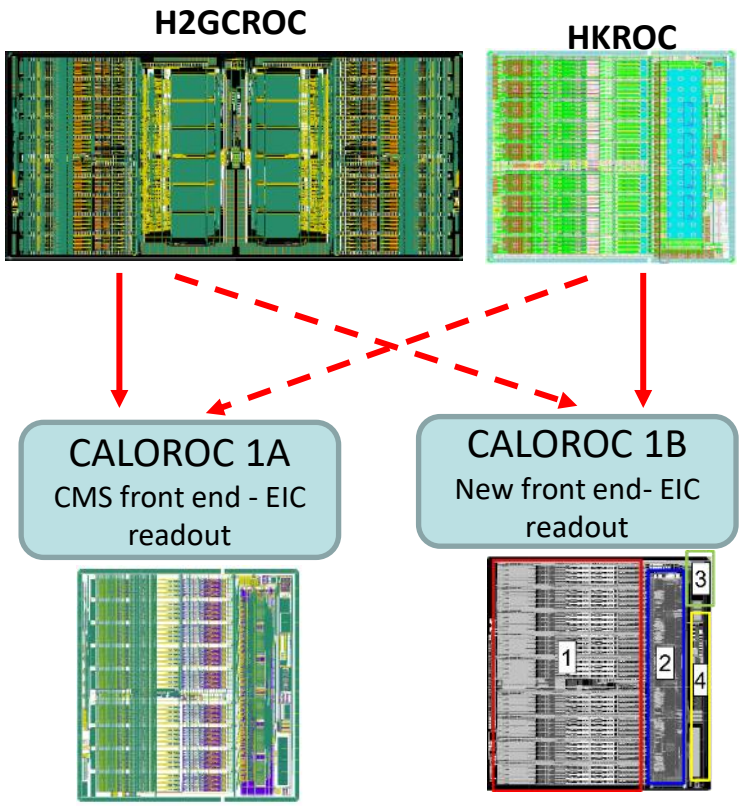
- CALOROC submission in September 2025 (ready in May)
  - All features inside – radiation hard
  - Expected Jan-Feb 2026 (after packaging)

~ 45 k from 2024 IN2P3 EIC-CALO

- CALOROC substrate designed
  - Needed to package the chip
  - Based on CMS substrate
  - Ordered in June 2025

JLAB-OMEGA contract 25 k





CALOROC Project at OMEGA in 2025

- CALOROC testboard (motherboard) design started in June
  - Prototypes v1 will be ordered by the end of 2025

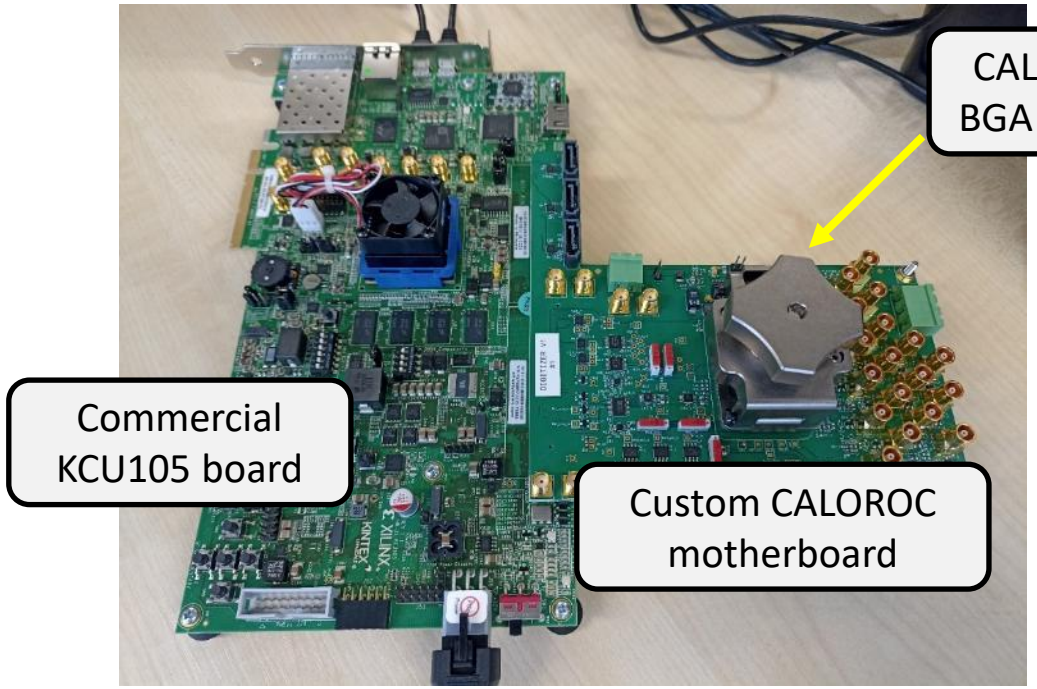
~ 5 k from 2025 IN2P3
EIC-CALO

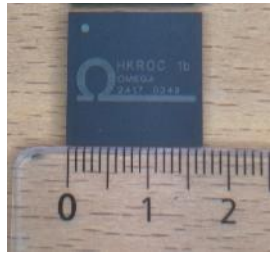
- 1x CALOROC socket ordered and received (Sept)
  - 1 will be reused from another project

~ 2 k from 2025 IN2P3
EIC-CALO

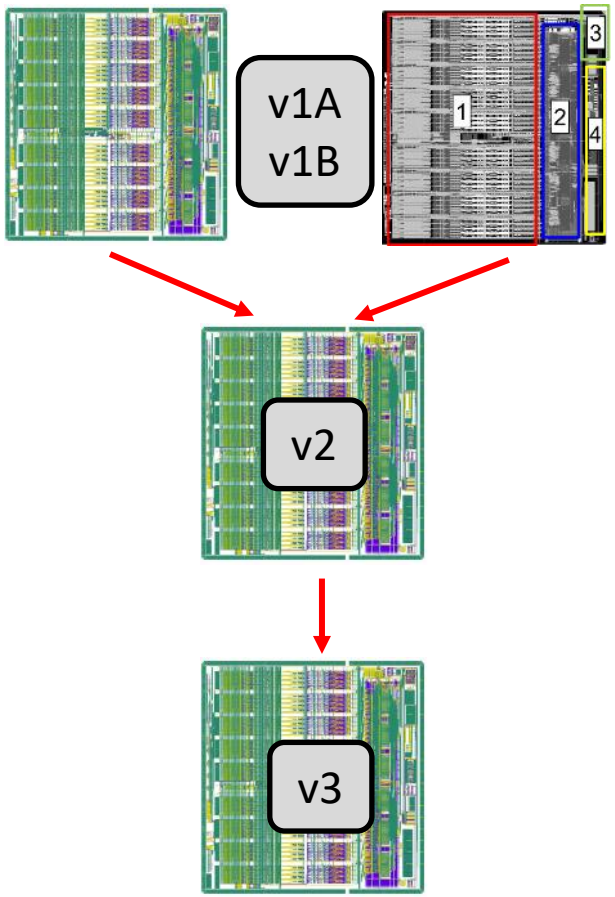
- KCU available (now at IJCLAB)

From HK project





CALOROC Project at OMEGA in 2026 and after



- ❑ Jan 2026: produce and distribute testboards
  - ❑ Characterization (with socket to be ordered)
- ❑ 2026 - Extensive tests and comparison of CALOROCs
  - ❑ End of 2026: selection on performances and system needs
  - ❑ Substrate validation
  - ❑ Channel count selection (baseline = no change)

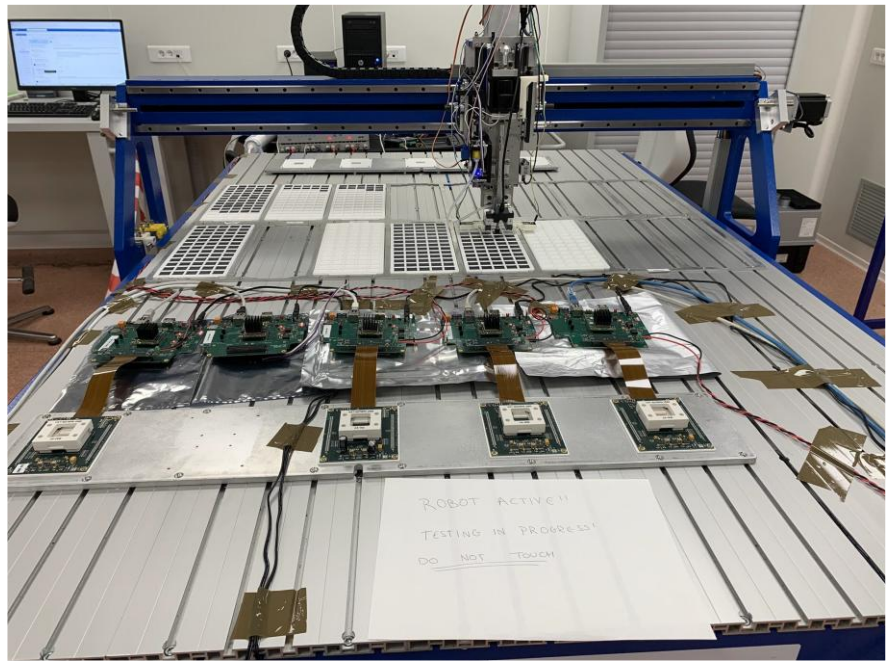
Requested **10 k€** for 26
- Test PCB x6 (3 with socket)
- Active components
- Injection board (A and B)
- Wafer dicing

Travels **12 k€** for 26
- 2x 2ppl EIC meeting
- 2x conf with proceedings

- ❑ 2027: Submission of selected CALOROC2 (**50 k€**)
  - ❑ If needed new substrate (**25 k€**)
  - ❑ Substrate validation
  - ❑ Irradiation tests (**12+2 k€** order end 2026 to have a slot ?)
  - ❑ Robot testboards (**10k€** sockets + **5 k€** tb)
- ❑ Q2 2028: Submission of final CALOROC3 (full wafer **300 k€**)
  - ❑ To be adjusted with EICROC tech node (130 vs 65 nm)

Quality Assurance and Timeline

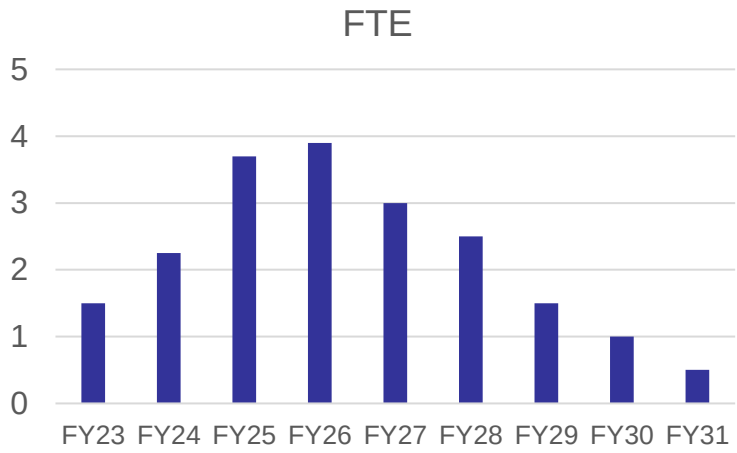
- Expertise in radiation-hardened front-end ASICs for HEP
  - HL-LHC ASICs: ATLAS HGTD and CMS HGCAL (10^5 ASICs)
- Expertise in irradiation testing (dose and displacement)
  - HL-LHC levels 200 Mrad and 10^{16} n_{eq} / cm² (1 MeV equivalent neutrons)
- Standard interfaces ensures a full compatibility with our robot
  - 2x 50 ASICs tested per hour (H2GCROC) with QR code scan
- CALOROC timeline – 2025 to 2028
  - Now: submission process start - CALOROCs submission (Eng. Run)
  - Dec 2025: first packaged ASICs back to the lab
    - 2 months to have an overall view of the performances
    - + 6 months for a deeper characterization
  - 2026: Decision for the final number of channels + version A and B
  - 2026-2027, irradiation campaigns + CALOROC2
  - Q2 2028: final submission CALOROC3 (same channel count) + production

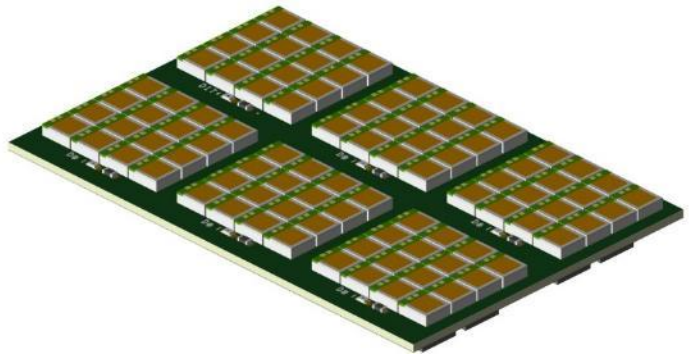


Presented at IPDR Sept 25

Summary and FTE

- Both **CALOROC1** includes everything
  - Based on CMS SiPM H2GCROC with EIC readout
- ASIC production foreseen in 2028
- Front-end boards work started at LLR and ORNL
- System tests are crucial for the ASIC validation/characterization
  - ASIC mounted on the “final” board



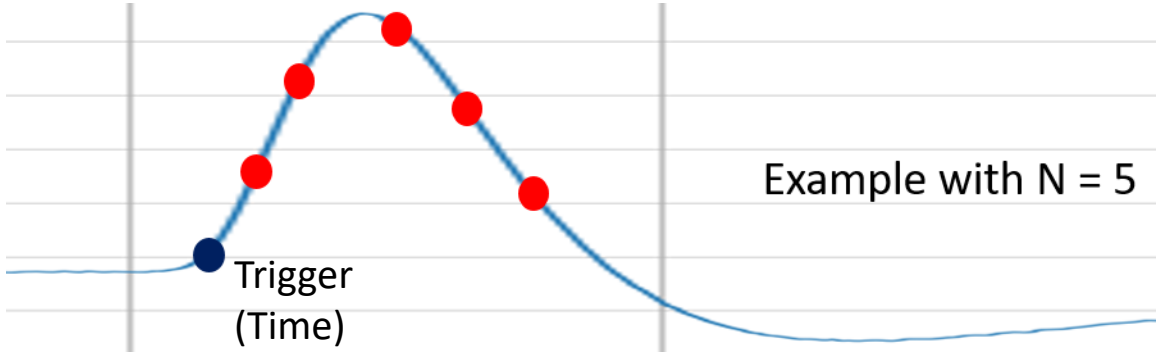


CALOROCs include all features + radiation hardness on the first submission

backup

CALOROC: Waveform Digitizer with Auto-Trigger

- CALOROC is a waveform digitizer working @ 39.4 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm is outside (back-end or offline)



CALOROC can accept ~ 50 kHz rate per channel (worst case)

Internal HKROC memory writing is without dead time
Hit-rate is only limited by serial link bandwidth (average values above)

A zero-suppress feature can be activated

A fast command can trigger an ASIC snapshot
(monitoring, calibration, heartbeat)

Readout Chains

Charge 2, 3, 4

Detector System	Sensor	ASIC / Digitization	Digitization Clock	FEB	FEB-RDO Protocol	RDO Type	RDO Location	Notes
Si Tracking --- (ITS3 / LAS): (IB, OB, EE, HE)	ITS3/LAS	Integrated /w sensor	39.4 MHz (2-8 us time)	Integrated (Schambach)	GBT	Fiber Aggregator GenericRDO	South Platform	• J. Schambach Presentation
MPGD tracking: (SAMPA): (IB, OB, EE, HE)	urWELL / uMegas	SALSA	39.4 MHz	lpGBT / VTRX+	GBT	4 → 1 GenericRDO	South Platform	• RDO – N. Novitzki Presentation • FEB – F. Barbosa Presentation
Calorimeters (CALOROC): BarrelHCAL, Backward HCAL, Barrel ECAL, Backward ECAL, Backward HCAL	SiPM	CALOROC	39.4 MHz	lpGBT / SFP+	GBT	4 → 1 GenericRDO	South Platform	• N. Novitzki Presentation
Calorimeters (CALOROC): LFHCAL, HCAL Insert	SiPM	CALOROC	39.4 MHz	lpGBT / SFP+	GPT	4 → 1 GenericRDO	East HCAL Platform	• N. Novitzki Presentation
Calorimeters (Discrete): FwdEcal	SiPM	Discrete	98.5 MHz	FPGA / SFP+ / Cu	Internal	16 → 1 GenericRDO	South Platform	• G. Visser Presentation • Planned RDO similar to existing designs
Far Forward (AC-LGAD / EICROC): B0 tracking, Roman Pots, Off Momentum	AC-LGAD	EICROC	39.4 MHz	lpGBT / VTRX+	GBT	Direct to FELIX	N/A	• Same as per Endcap TOF
Far Backward: (AC-LGAD / FCFD): Lumi photon spectrometer tracker	AC-LGAD	FCFD	39.4 MHz	lpGBT / VTRX+	GBT	Direct to FELIX	N/A	• Same as per Barrel TOF
Central Detector (AC-LGAD / EICROC): Endcap TOF	AC-LGAD	EICROC	39.4 MHz	lpGBT / VTRX+	GBT	Direct to FELIX	N/A	• F. Barbosa Presentation
Central Detector (FCFD): Barrel TOF, pfRICH, DIRC	HRPPD / MCPMT	FCFD	39.4 MHz	lpGBT / VTRX+	GBT	Direct to FELIX	N/A	• F. Barbosa Presentation
Far Forward/Backward (CALOROC / Discrete): B0 Crystal Calorimeter, ZDC Crystal Calorimeter, ZDC HCAL, Lumi Photon Spectrometer Calorimeter	SiPM	Discrete	39.4 MHz (or) 98.5 MHz	FPGA / SFP+ / Cu (or) lpGBT / SFP+	Internal GBT	16 → gRDO (or) 4 → 1 gRDO	East/West Tunnel Near Detectors	• Small channel count detectors • Expect to copy either CALOROC or Discrete
Far Backward: (Discrete): Direct Photon Lumi Calorimeter*	SiPM	Flash-250	197 MHz	FADC 250	Streaming ADCs	(N/A)	West Tunnel	• Special FELIX processing to histogram / Sum bunch by bunch luminosity data
Far Backward: (TimePix): Low Q Tagger	TimePix	Integrated / w sensor	98.5 MHz	Integrated / w sensor	Internal	SPIDR4 Variant (NIKEF)	West Tunnel Under Detector	• K. Livingston Presentation • Planned RDO similar to existing designs
Imaging Calorimeter (Astropix):	AstroPix	Integrated / w sensor	98.5 MHz	Integrated / w Sensor	Astropix Internal	End of Stave Card (NASA)	On Detector	• J. Metcalfe Presentation • Planned RDO similar to existing designs
Central Detector (ALCOR): dRICH	SiPM	ALCOR	39.4 MHz	FPGA / Cu	Internal	FPGA / VTRX+	On Detector in PDU	• Pietro Antonioli Presentation

Electron-Ion Collider

Electronics design pending
Planned variants of GenericRDO
Scope of outside Electronics/DAQ

ASICs – Path to Completion

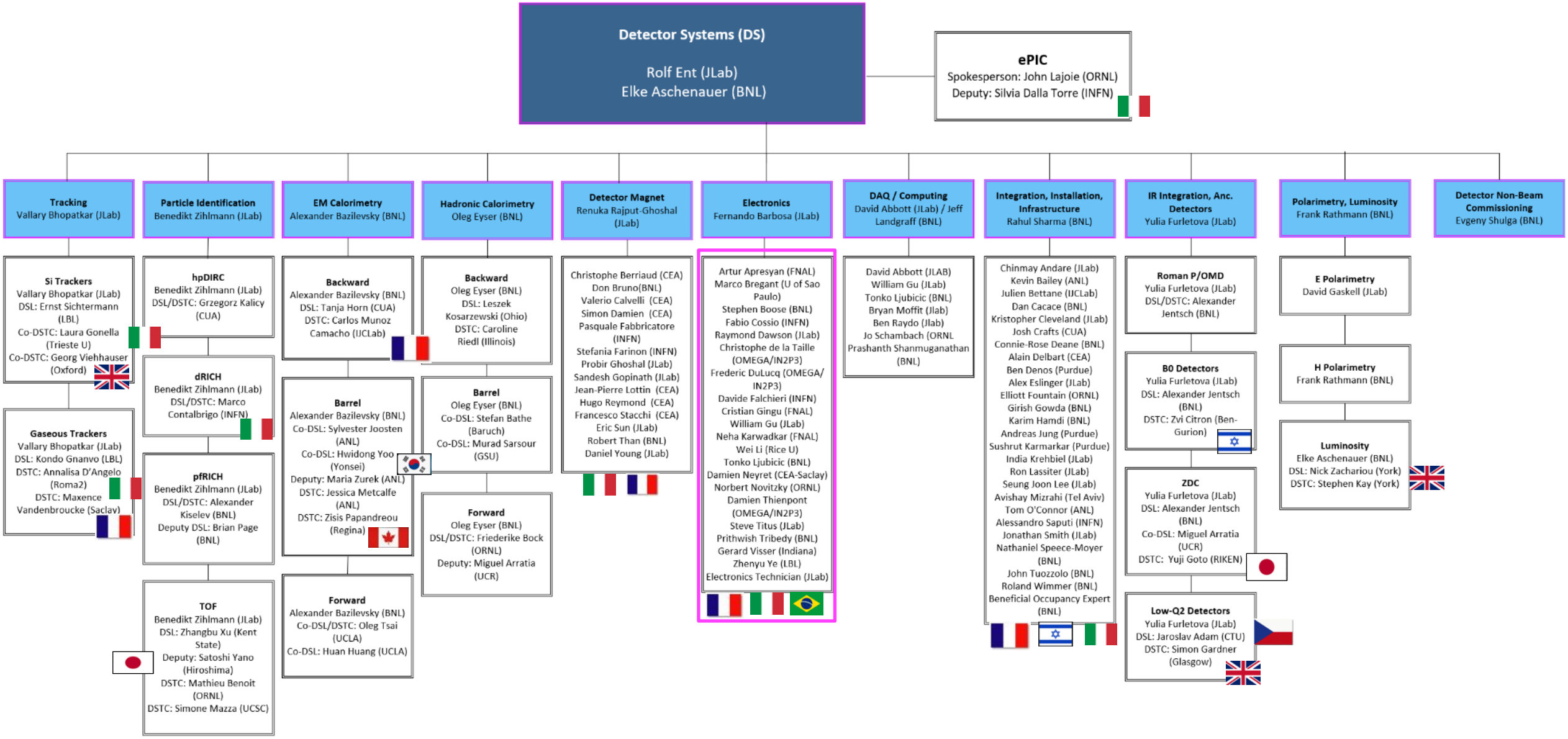
Charge 1, 2, 3, 5

	Status & Development Summary	Next Steps	Production	Institution
CALOROC	Interface design FY23- FY24, CALOROC1A/B designed FY24-FY25 *CALOROC1A: ADC/TOT + TOA, full SRO interface* *CALOROC1B: Switched gain (4) + ADC + TDC, full SRO interface* *Tests: Oct 2025*	CALOROC2 (64 ch) – FY25-FY26 *Select version and increase (?) channels from 32 ch to 64 ch.*	FY28	OMEGA/IN2P3/IJCL, ORNL
EICROC (32x32)	EICROC0A (4x4) designed FY24-FY25, EICROC1 (32x32) FY25 *EICROC0A: ADC + TOA, improved testability* *EICROC0B: Replaced ADC with peak sensing, Wilkinson ADC, lower power* *EICROC1: added full SRO interface*	EICROC2 (32x32) FY26 *Add Derandomizer and ZS. Digital on Top design for lower power (~1 mW/ch).*	FY27 – FY28	OMEGA/IN2P3/IJCL/CEA-Saclay, AGH
FCFD (128)	Front end characterized, FCFDv1 (6 ch) FY23-FY24 characterized, FCFDv1.1 FY25 *Optimized for HPK sensor characteristics*	FCFDv2 (32 ch) FY25-FY26 *Add ADC, TDC, interfaces from ETROC, ECON CERN.* FCFDv3 (128 ch) FY26	FY27	FNAL
FCFD Variant (64)	FCFDv1.1 FY25 *Preliminary tests with sensors*	Harmonize sensor/ASIC specifications, adapt FCFD for 64 ch.	TBD	FNAL
ALCOR	ALCORv2.1 (32 ch) beam tests FY24, ALCOR v3 (64 ch) FY24-FY26 *Full specification, SRO interface, BGA*	ALCOR-64 – FY26 *Final iteration for production*	FY26 – FY27	INFN
SALSA	SALSA0/1 FY24, SALSA2 (32 ch) designed FY23-FY25 *Full SRO interface, most DSP features, Submission October 2025*	SALSA3 (64 ch) FY25-FY27 *full DSP, 64 ch*	FY28	CEA-Saclay, U Sao Paulo

- ASIC production is ~1 Year: Fab, Packaging, Test. Additional information in the following slides. PED is expected to be completed in FY26.

Complete. Fab is imminent – at TSMC now.

Integrating ePIC Collaboration in Detector Subproject Organization



ASICs & Electronics - Scope of the Effort

Charge 1, 2, 3

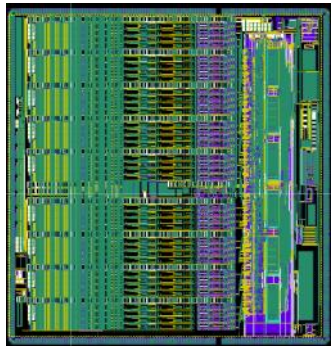
- Approximate quantities and costs.
- Costs include mask sets, fabrication and packaging, wrt quantities needed.

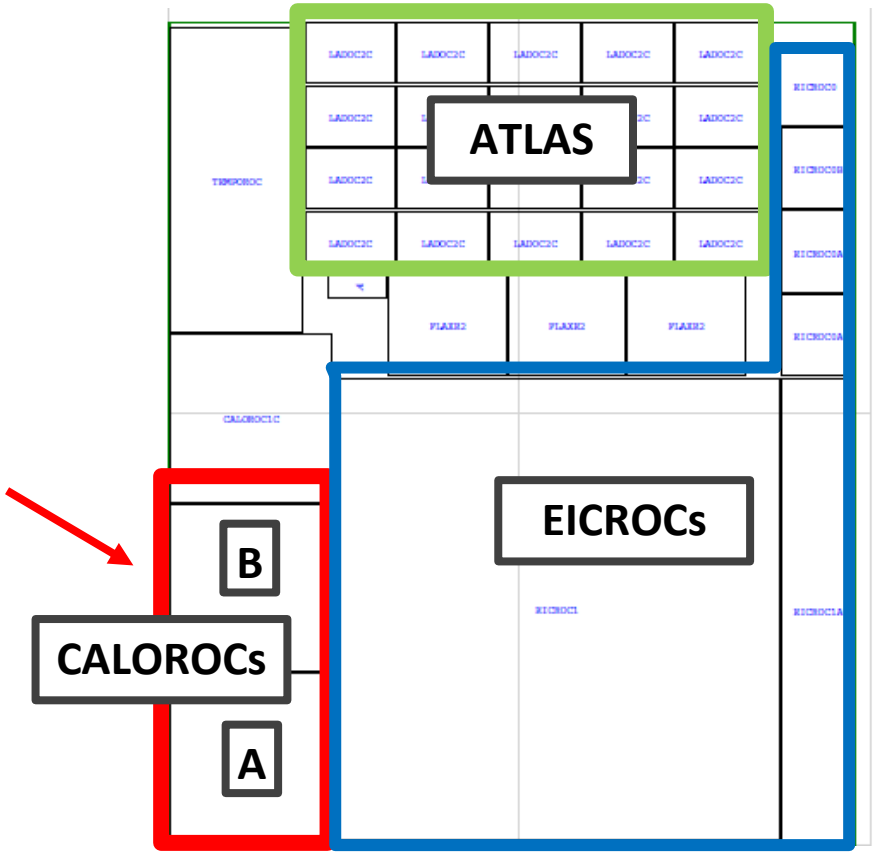
	#Ch	#Ch/Unit	#ASICs /Wafer	#Wafers	Node (nm)	Packaging	Cost/ch ($)	Institution
Discrete/COTS	24 k	32	NA	740 Digitizers	COTS	NA	91 (Includes FE Adapter)	Indiana University
CALOROC	97 k	64	480	5	130	BGA	3.2	OMEGA/IN2P3/IJCL, ORNL
EICROC	5.2 M	1,024	160	42	130	Wafer Bump	0.1	OMEGA/IN2P3/IJCL/CEA-Saclay, AGH
FCFD strip FCFD Variant	2.6 M 144 k	128 64	180	149 13	65	Wire Bond BGA	0.5	FNAL
ALCOR	318 k	64	800	8	110	BGA	0.9	INFN
SALSA	167 k	64	500	7	65	BGA	4.1	CEA-Saclay, U Sao Paulo

- Production
  - 65 nm: $750 k masks + $3.5 k per wafer
  - 110 nm: $190 k masks + $4 k per wafer
  - 130 nm: $250 k masks + $4 k per wafer
- Packaging BGA: $3-$7.5 per chip.
- ASIC Costs Total: ~$3.3 M
  - Masks: ~$2.2 M; Chips: ~$1.1 M

Summary and FTE

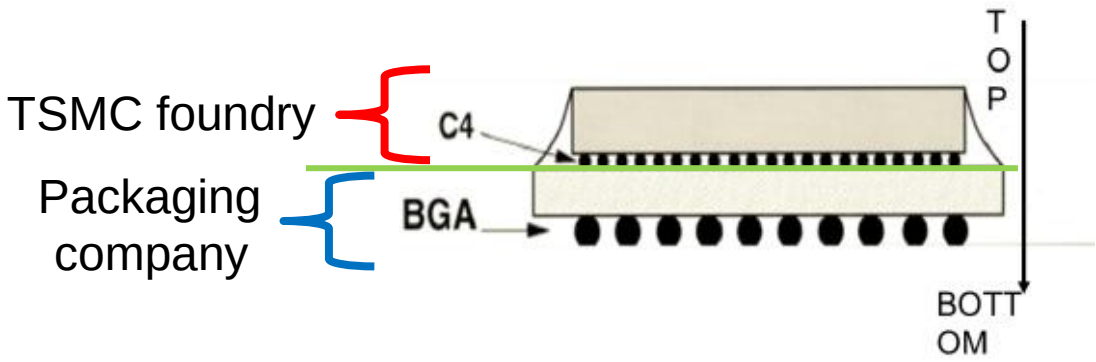
- Conservative **CALOROC-1A**:
  - Based on CMS SiPM H2GCROC with EIC readout
- New **CALOROC-1B**:
  - New analog front end
  - Higher dynamic range and input capacitance
  - Same backend (and pinout)
- All CALOROCs share the same backend + RadHard
  - We **~150 ASICs per each flavor**
  - GIT for back-end designers
  - Datasheet available now
- ASIC submitted with CERN/IMEC (May 2025)
  - Chips expected packaged in December





CALOROCs are targeted to include all features + radiation hardness on the first submission

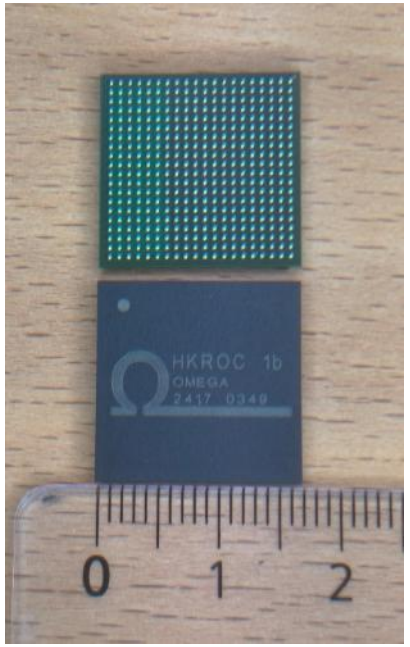
- CALOROC will have the same package as the existing HKROC:
  - JEDEC MO-216 – 17 x 17 mm BGA version
  - 400 balls with 0.8 mm pitch
  - Specific substrate (interposer) designed at OMEGA
  - **QR code** like HGCROC3



JEDEC SOLID STATE PRODUCT OUTLINE	TITLE: THIN PROFILE, SQUARE AND RECTANGULAR, BALL GRID ARRAY FAMILY, 1.00 & 0.80 mm PITCHES	ISSUE: E	DATE: AUG 2003	MO-216

TABLE 3: SQUARE VARIATIONS – 0.80 PITCH

D / E	e = 0.80							
	MD/ME	N	SD/SE	VARIATION	MD-1/ME-1	N	SD/SE	VARIATION
14.00	17	289	0.00	BAJ-1	16	256	0.40	BAJ-2
15.00	18	324	0.40	BAK-1	17	289	0.00	BAK-2
16.00	19	361	0.00	BAL-1	18	324	0.40	BAL-2
17.00	20	400	0.40	BAM-1	19	361	0.00	BAM-2

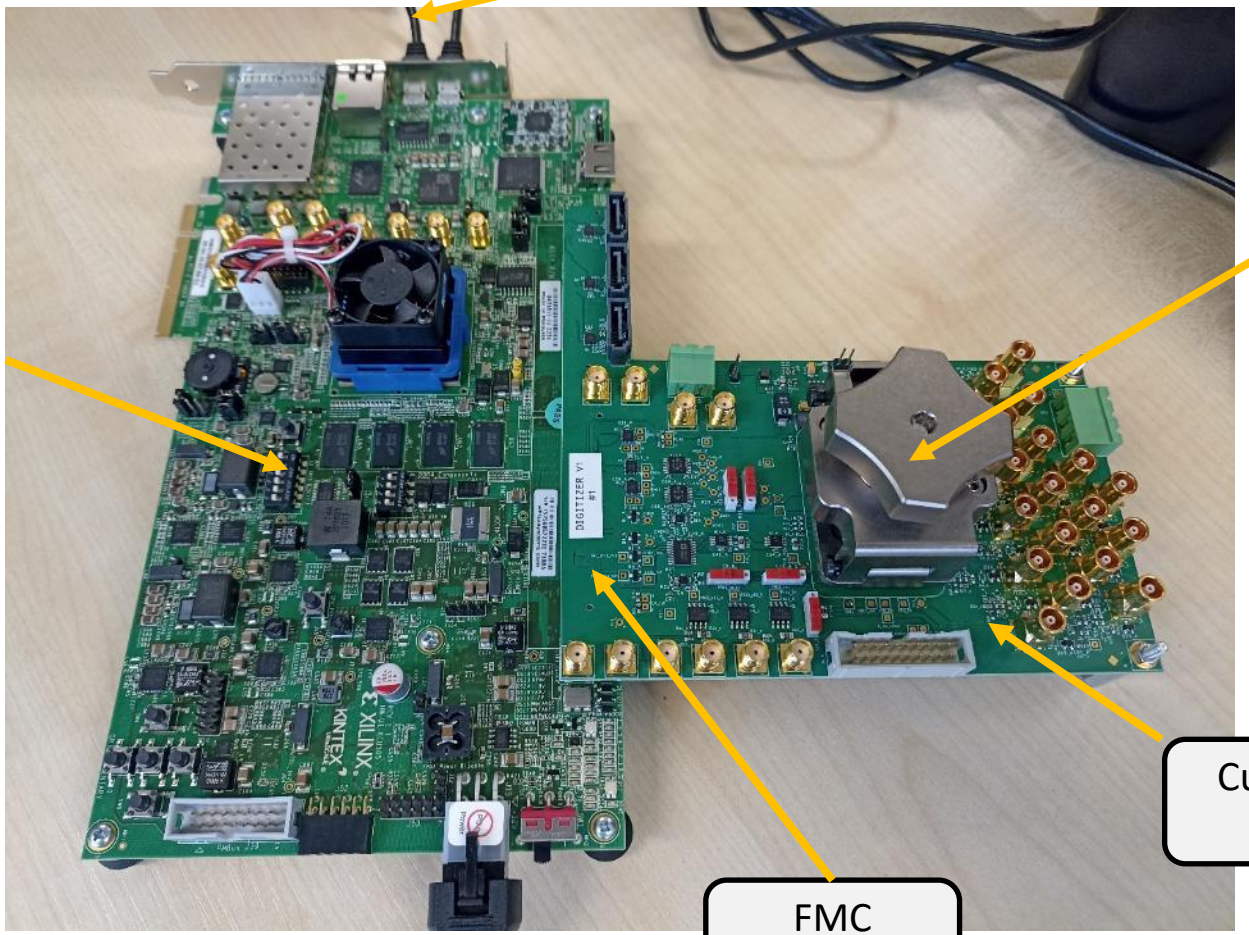


Test System for Characterization

- CALOROC characterization motherboard under design at OMEGA:
  - Originally developed for HGCROC and the HKROC
  - Well-known at OMEGA and LLR (firmware based only)
  - Compatible with KRIA motherboard (CERN) but software + firmware needed

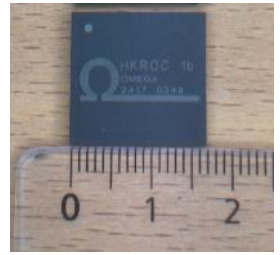
Python scripts

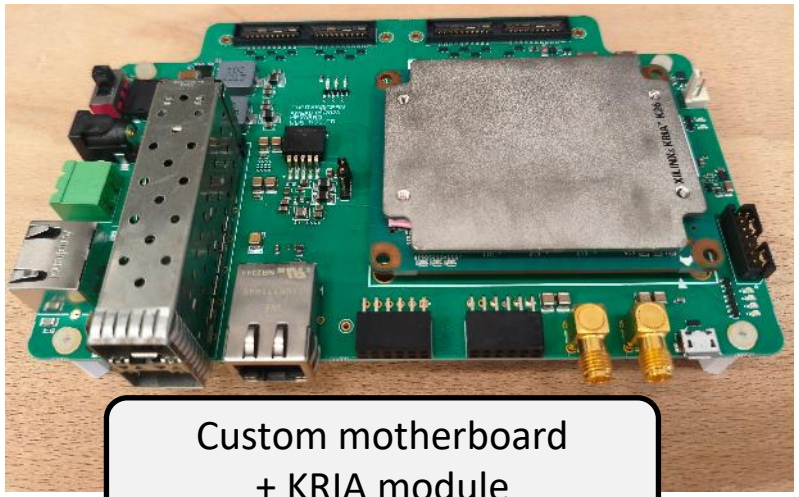
Monitor
Program
Test



Commercial
KCU105 board

CALOROC
BGA socket





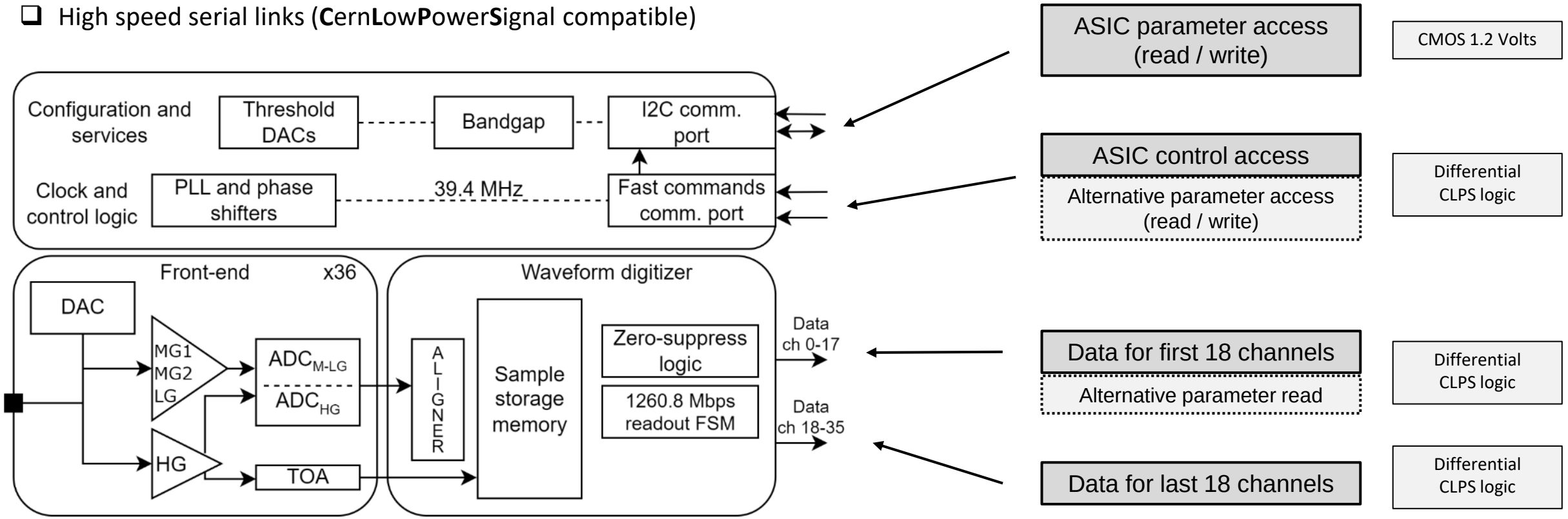
Custom motherboard
+ KRIA module

Custom CALOROC
motherboard

FMC
connector

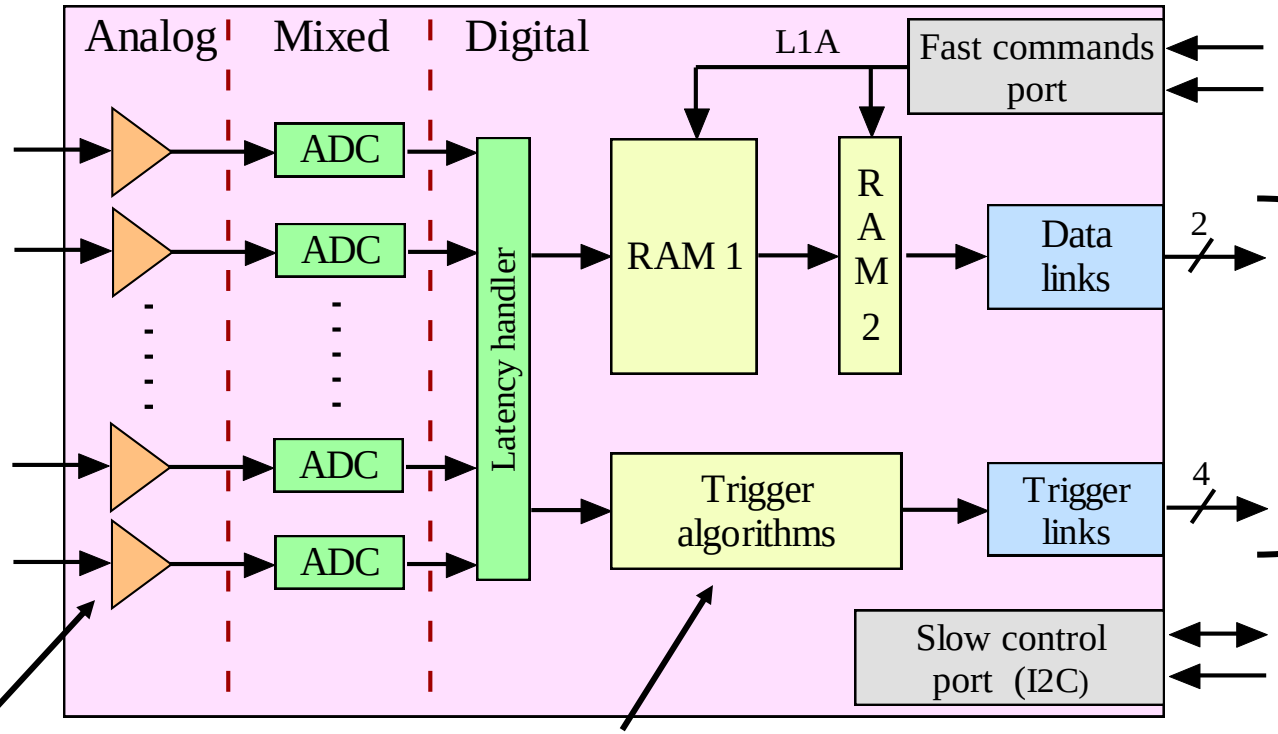
CALOROC: Block Diagram - Interfaces

- CALOROCs will have the same interfaces (comparable to CMS ones):
  - 1 clock @ 315.2 MHz + 2 resets (hard + soft)
  - Fast command to dynamically control the ASIC (differential)
  - I2C to set the parameters (tbc)
  - High speed serial links (**C**ern**L**ow**P**ower**S**ignal compatible)



ROC Chips Standard Structure

- H2GCROC (for SiPM readout) is an HL-LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (but interfaces for CALOROC will similar)



Dedicated fast command interface : calibration pulses, external L1 trigger

Data and trigger serial links with CLPS signaling (LpGBT @ 1.28 Gbps)

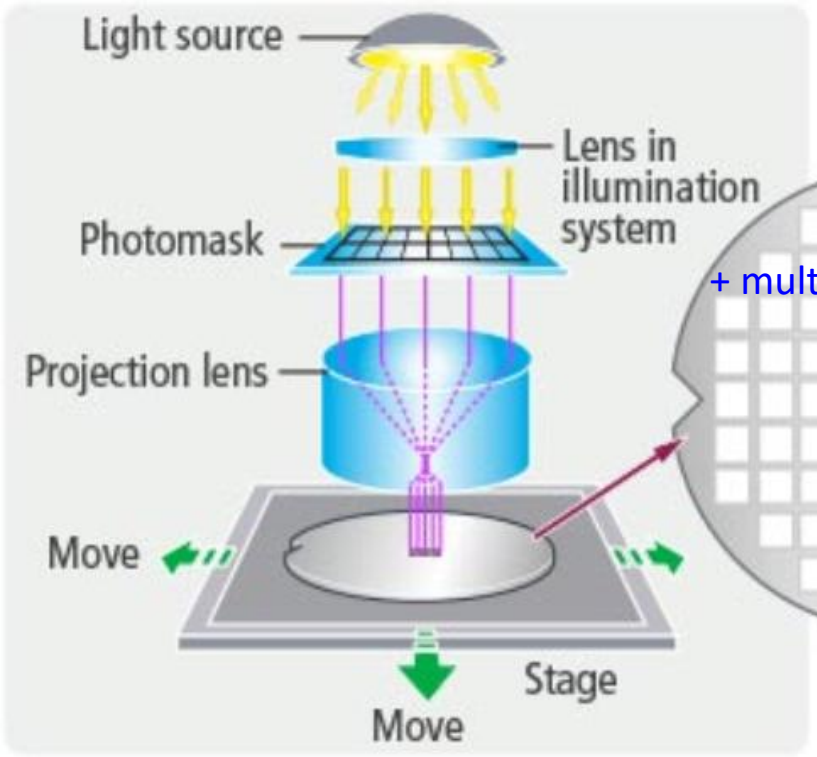
Analog front-end specific to sensor

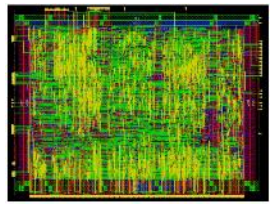
LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

I2C interface to load the ASIC parameters (slow control interface)

ASIC Fabrication Overview

Charge 1, 2, 3





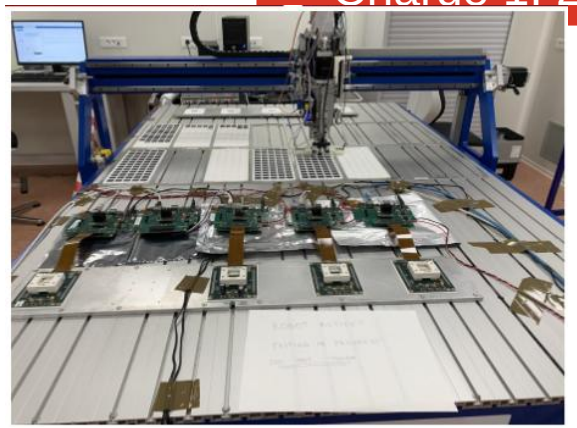
CALOROC

+ multiple chem. steps

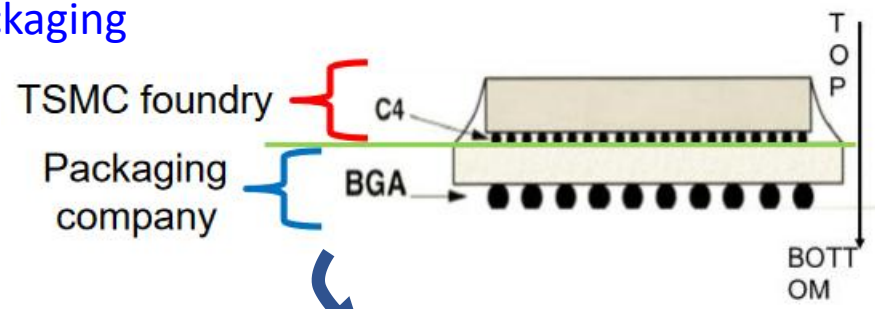
Area which can be exposed at once

Testing

Packaging



Testing @ Omega (~100/hour).



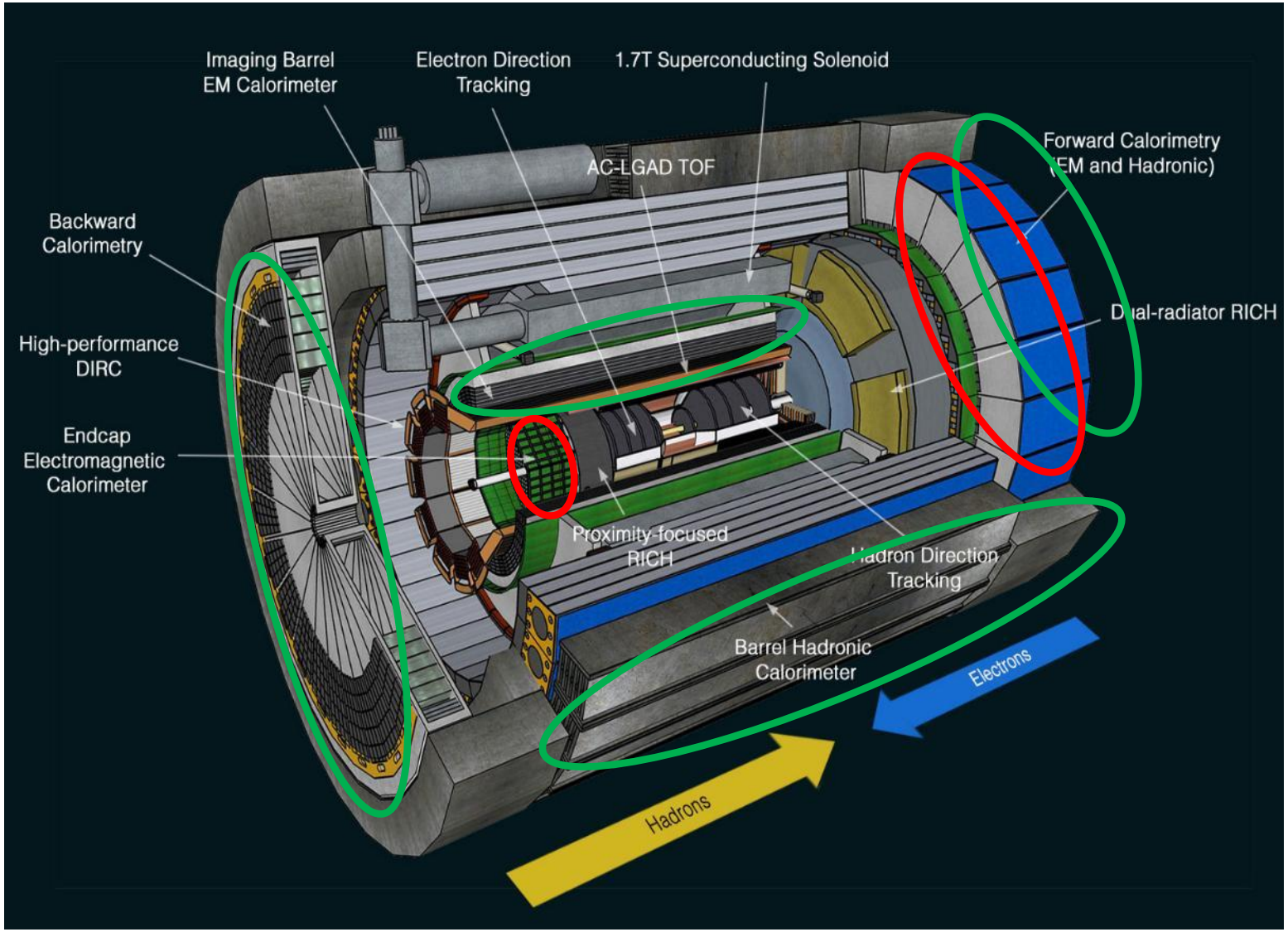
Functional Tests

Stepper – Very high precision

Reticle - may include multiple ASICs (e.g. set by TSMC)

- ASIC to fit within Reticle, or port design to a different technology node (e.g. 130 nm to 65 nm) - EICROC?
- A mask set may consist of 40 – 50 masks (to build layers of metal, oxide, implantation, etc.) to make an ASIC
- Wafer tests for process QA/QC

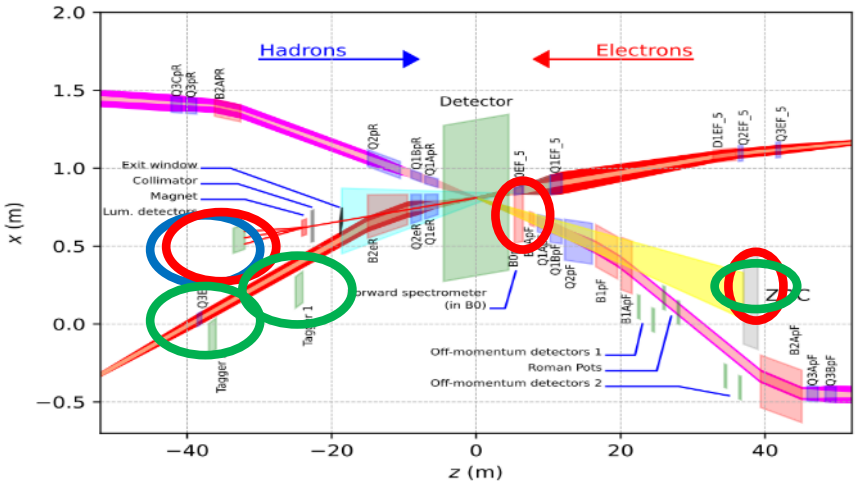
Calorimetry at ePIC



13 Calorimeters:

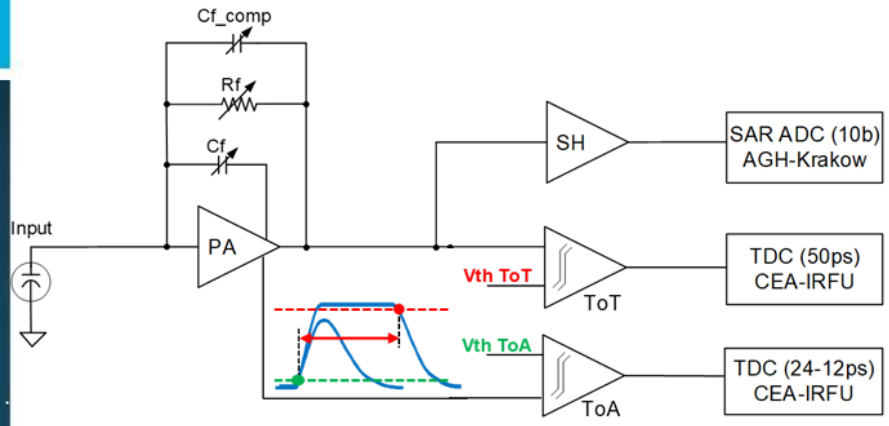
- 7 x SiPM – CALOROC
- 5 x SiPM – Discrete
- 1 x SiPM – Commercial fADC250

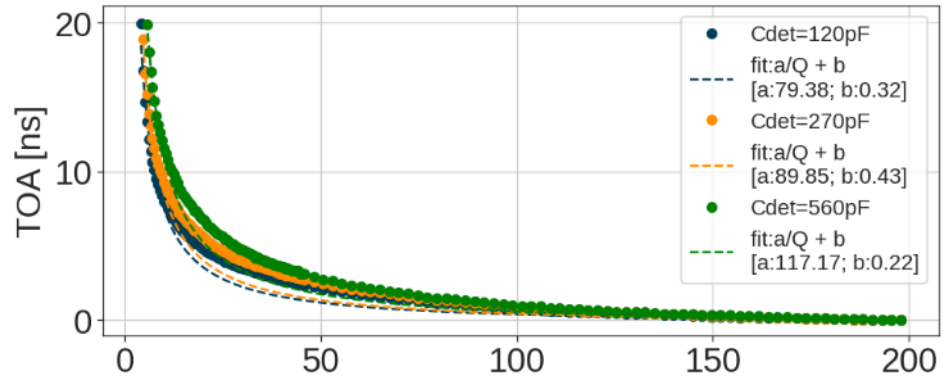
From J. Landgraf
(IDR review)

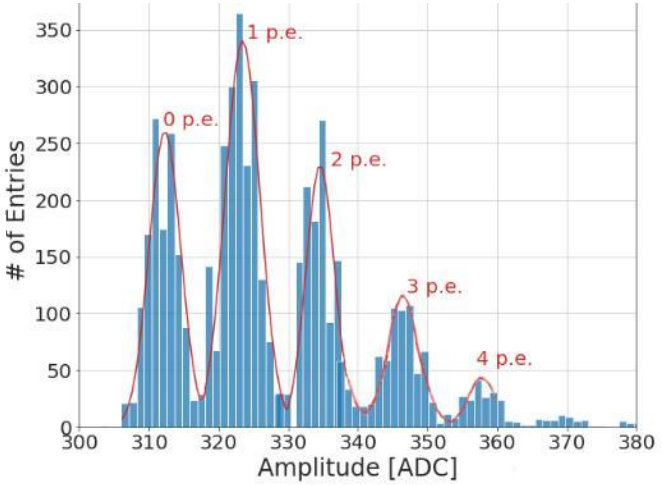


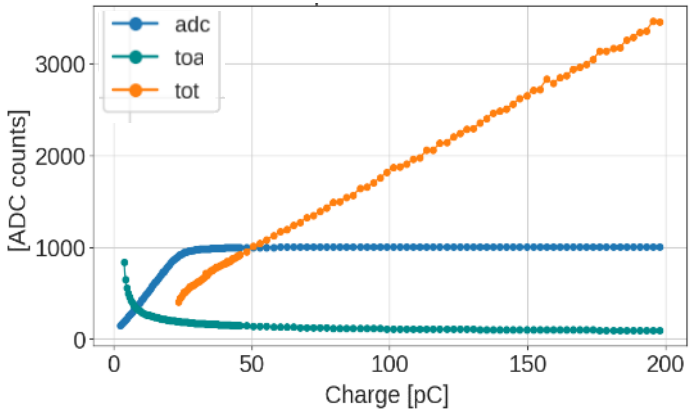
CALOROC1A (H2GCROC-Based)

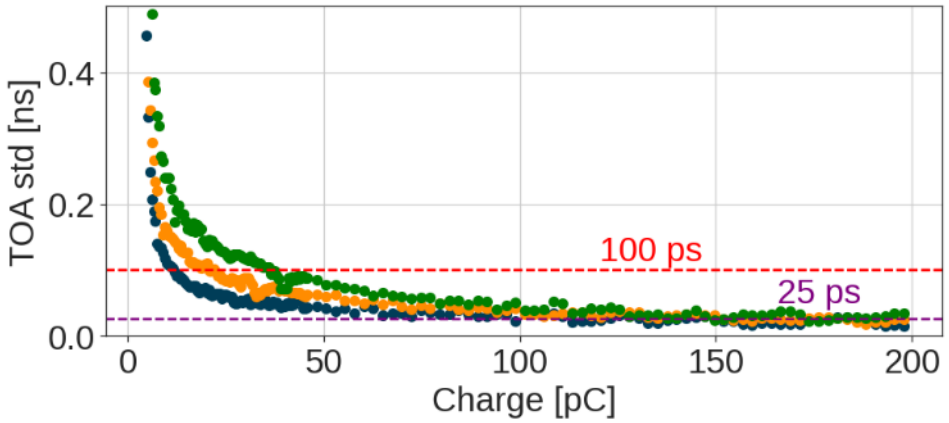
- Reuse of analog front-end based on ADC/TOT and TOA: fully characterized *
  - 15 mW per channel / R adiation performance / SiPM range 100-600 pF

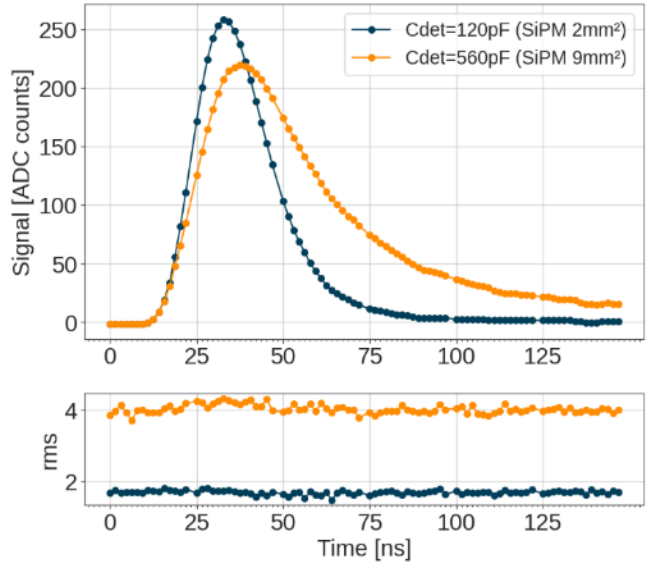










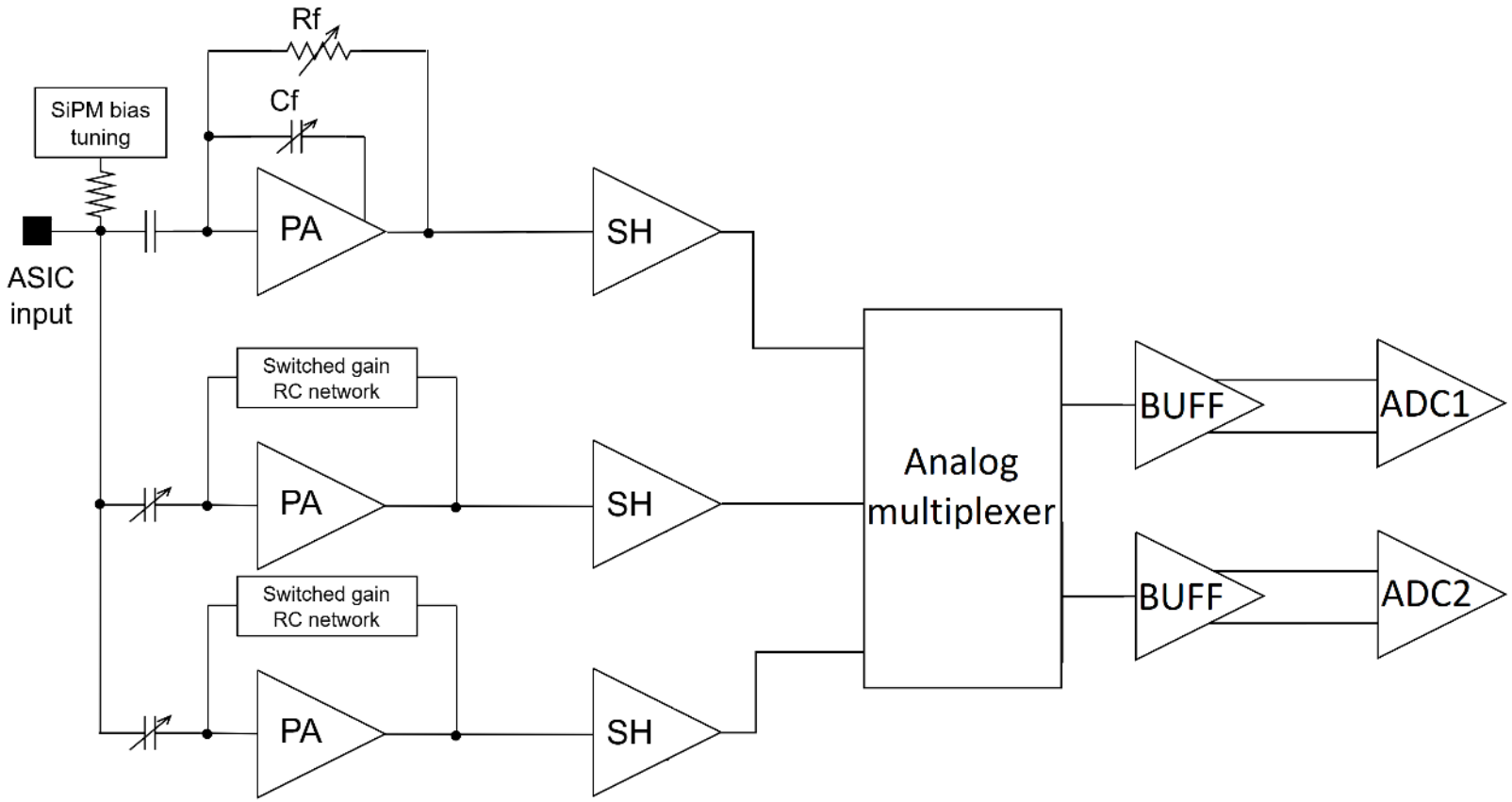


- CALOROC1A will only update its back-end to be EIC compatible

* TWEPP 2023 → https://doi.org/10.1088/1748-0221/19/04/C04005

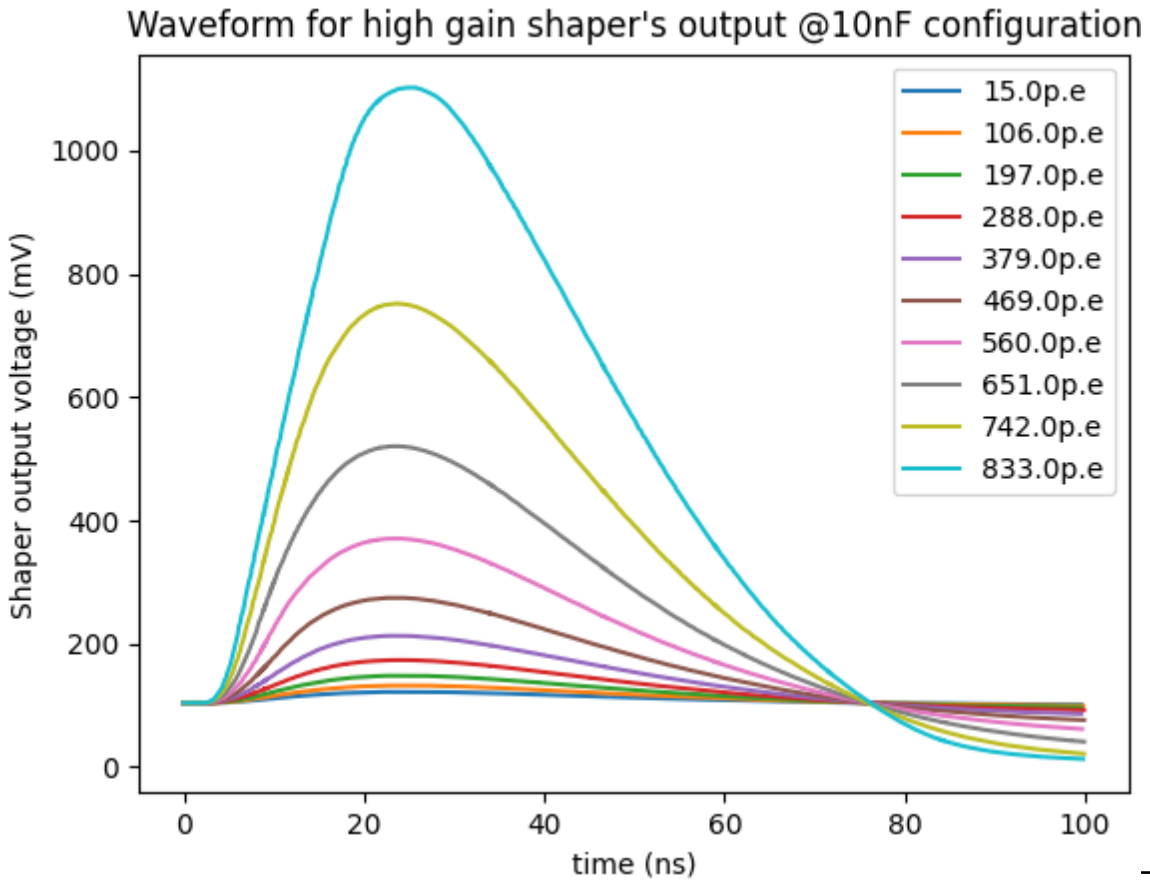
CALOROC1B: Channel Architecture [P. Dumas]

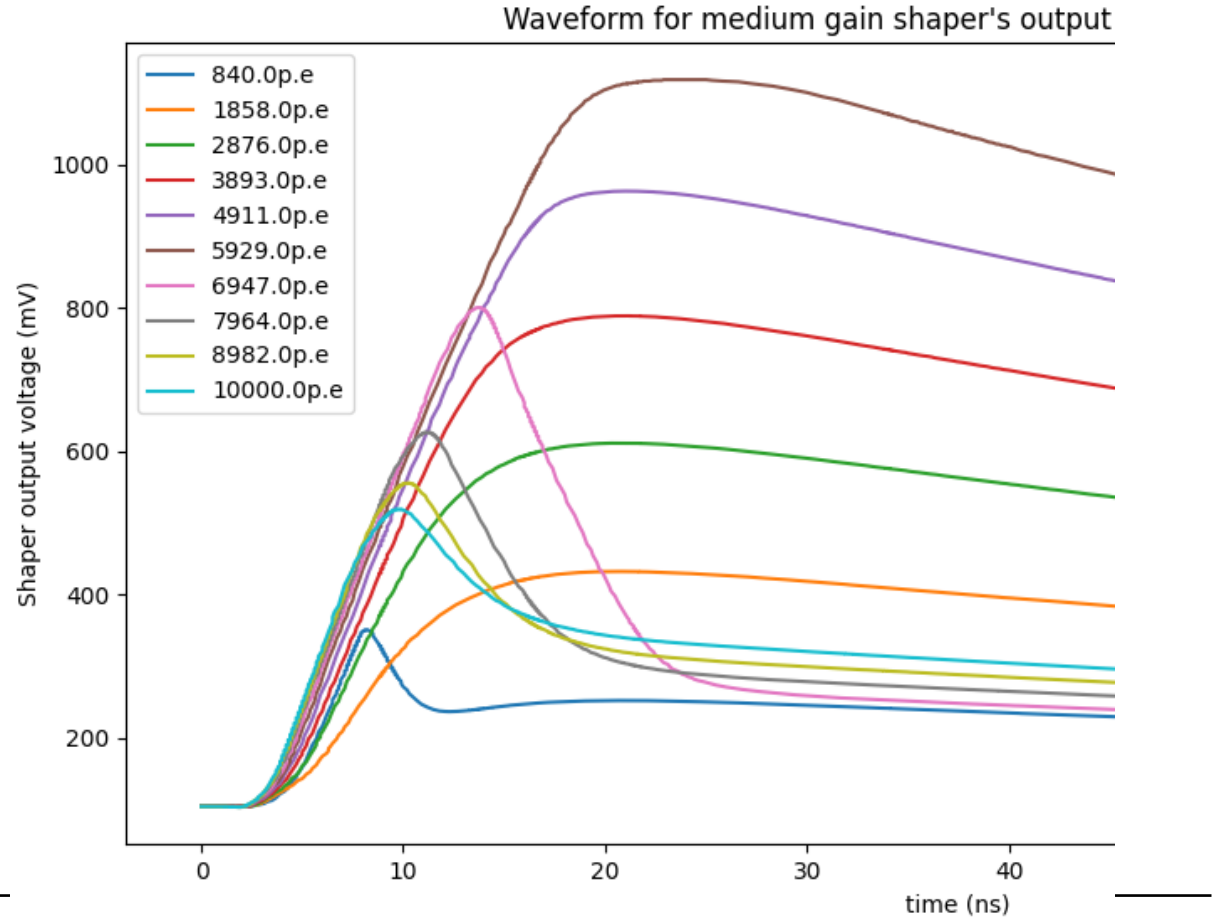
- New dynamic frontend with switched gain:
  - 1 high gain preamplifier
  - 2x low power preamplifier
  - 1 analog multiplexer
- Reuse CMS-H2GCROC ADCs and TDCs:
  - 10-bit 40 MHz ADC (Krakow)
  - 25 ps TDC (Saclay)
- Shared CALOROCs backend
- Common specifications:
  - SiPM from 500 pF to 2.5 - 10 nF
  - ~ 10-15 mW/channel
  - CMS HL-LHC Radiation level 200 Mrad



CALOROC1B: Charge and Time Simulations

- Waveform for HG on the left + gain switching on the right:
  - Example with Cd of 10 nF





CALOROC1B: SiPM vs SNR

- The SiPM configuration has a direct impact on the SNR
  - SNR for 1p.e is proportional to Q/C (larger SiPM cap decrease SNR)
  - Gain of 1.8e5 electrons per p.e (table below)

- CALOROC1b will be able to readout SiPM in the range ~ 500 pF to 10 nF
  - Timing measurements will focus on the MIP (~15pe)

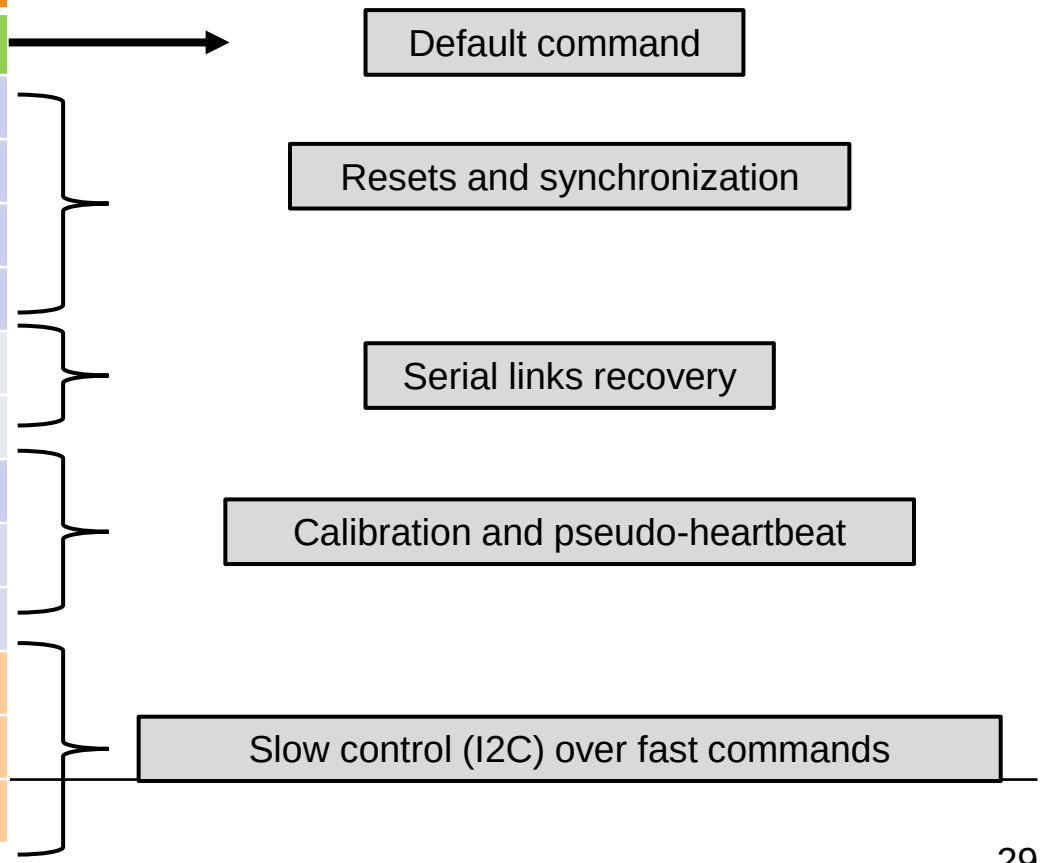
Operation modes	1 SiPM of 530pF Caloroc1B	1 SiPM of 2.5nF Caloroc1B	4 SiPM of 2.5nF Caloroc1B	1 SiPM of 530pF Caloroc1A
Cin	530pF	2.5nF	10nF	560pF
Dynamic range in charge (Noise - Max)	2.6fC-190pC	12fC-770pC	48fC-3.1nC	20fC-320pC
Input time constant (occupancy related)	100ns	500ns	500ns	10ns
Jitter @ MIP (≈400fC)	35ps	110ps	470ps	400ps
SNR @ 1p.e (≈30fC@gain=1.8e5)	10	2.4	0.6	1.44

SiPM: S14160-3010PS 3x3mm (530pF) / S14160-6010PS 6x6mm (2.5nF)

CALOROC: Fast Commands

- Commands to interact dynamically with the ASIC
  - 8 bits commands synchronized with incoming 315.2 MHz clock – MSB first
  - Only idle needed – others have a known latency
  - Detailed in the datasheet

Fast commands	Value	Description
Idle	00110110	Default command inside
ChipSync	11010010	Reset FSM, buffers and counters
BCR	00011101	Reset timestamp counter to a default value
EBR	11010001	Empty readout buffers
PING	10011001	Ping status and counters
LinkResetROCD	10011010	Transmission of synchronization patterns
ROC-Serializer-Reset	10011100	Reset serializer link module only
L1A	01001011	External trigger (all channels)
CalPulseInt	00101101	800 ns internal calibration pulse
CalPulseExt	01111000	100 ns external calibration pulse
SC_0	01011010	I2C over fast command - send ‘0’
SC_1	01011100	I2C over fast command - send ‘1’
SC_Valid_Reset	10001011	Valid or reset (2 consecutives) current transaction



CALOROC: Readout Frames

- For charge measurements, CALOROC-A based on ADC/TOT, CALOROC-B only ADCs

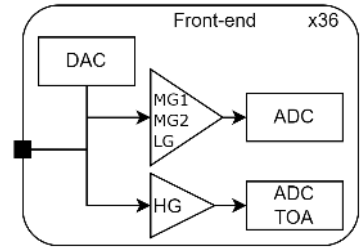
CALOROCA (CMS-like)

4b-data Header	2b Mode	Dh	24b Timestamp	1
4b-data Header	8b 0	Dh -d	Dh -h	18 channels Hit map
Tc	Tp	10b ADC-1	10b ADC or TOT (Tc = 1)	10b TOA
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
⋮				
Tc	Tp	10b ADC-1	10b ADC or TOT	10b TOA
CRC				
Idle/Sync Header	28b default IDLE Pattern			

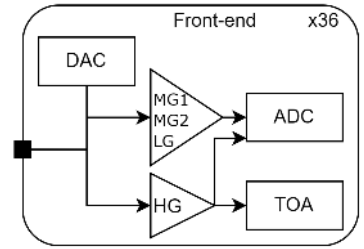
CALOROCB – 2 ADCs or 1 ADC (4 gains)

4b-data Header	2b Mode	Dh	24b Timestamp	1
4b-data Header	8b 0	Dh -d	Dh -h	18 channels Hit map
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
⋮				
2b Gain	10b ADC - HG or 0s	10b ADC 3-gain or 4-gain	10b TOA	
CRC				
Idle/Sync Header	28b default IDLE Pattern			

CALOROCB (2 ADCs)

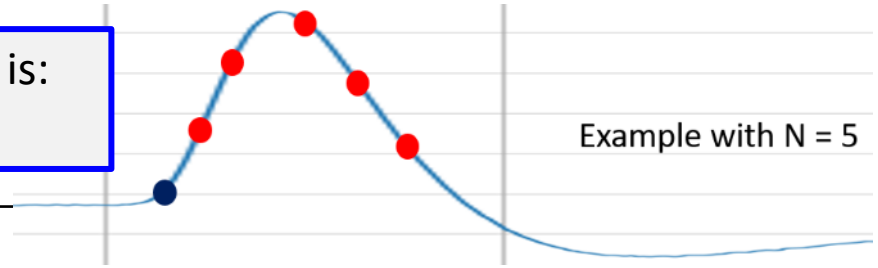


CALOROCB (1 ADCs)



In ZS mode, for X (1-18) hit channels and N samples, number of 32-bit words is:

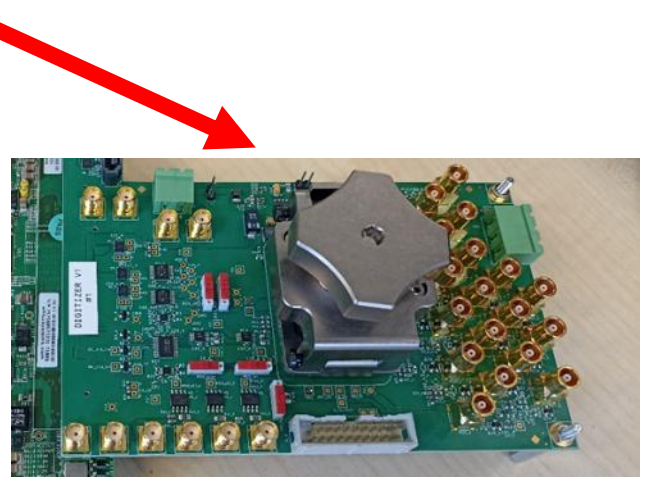
N x (2Headers + X + 2Trailers)

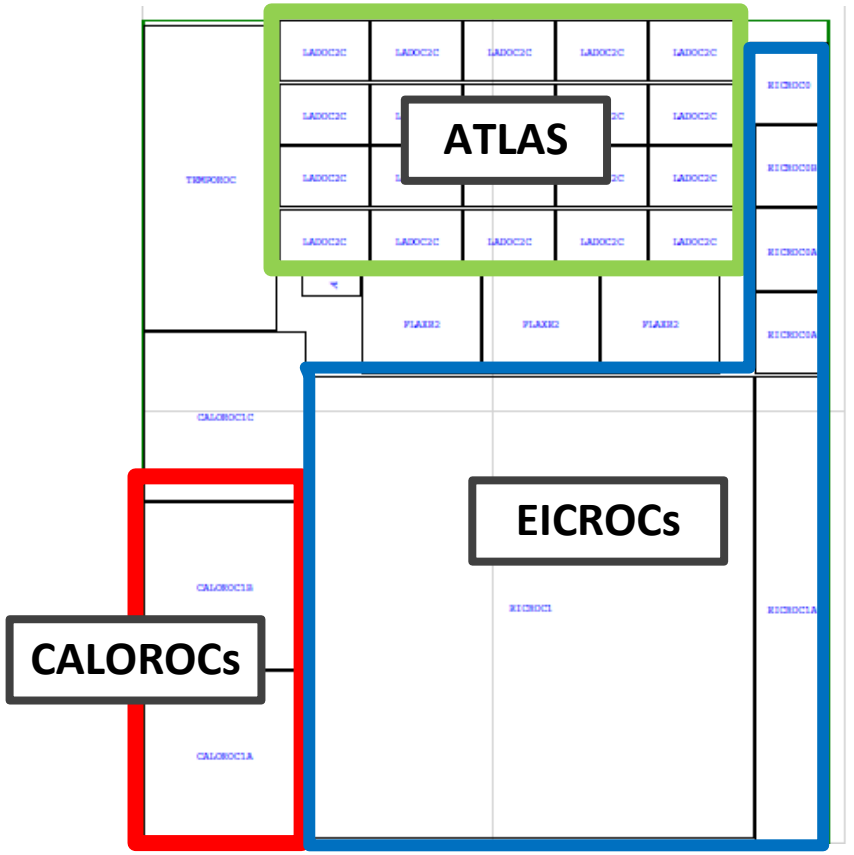


In characterization mode, forced TcTp, ADC, TOT, TOA for all channels

Summary 1/2

- Technical design work finished
  - Delays due to administrative issues
  - Moving to the preparation of datasheet / Packaging / testboards
- CALOROC substrate (x1000) ordered for the packaging
  - We expect 160 caloroc / version
- Characterization board design in progress (first schematic done)
  - Socket ordered





CALOROC integration and power supply consideration

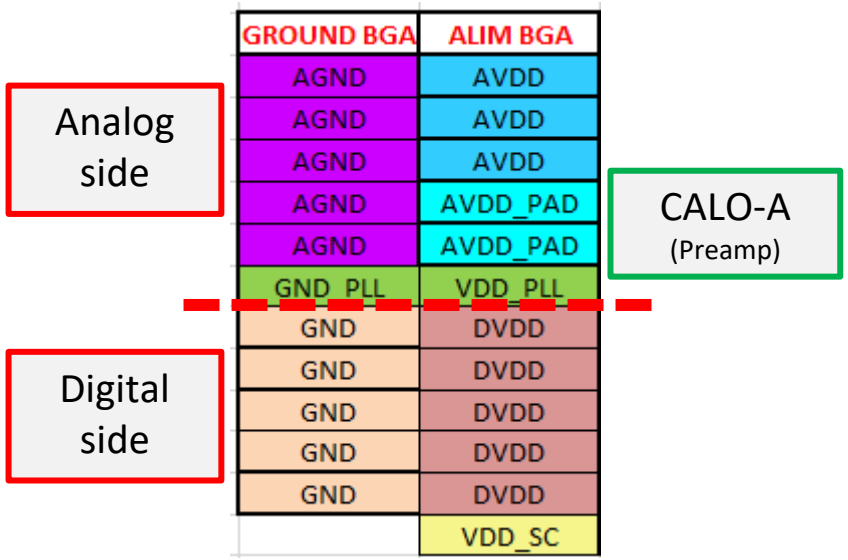
- On the board, CALOROC will need a maximum of 3 power supplies:
  - Analog / Digital + 1 dedicated for CALOROC-A (Preamp)
  - (Not shown here: LED power and HV)

Digital side

Analog side

MAPPING CALOROC_1 BGA 400 (TOP VIEW)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
SDA	RSTB_I2C	HARD_RSTB	SOFT_RSTB	ERROR	CK_320_N	CK_320_P	FCMD_P	FCMD_N	ADD<4>	CHIP_R	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND
SCL	GND	GND	GND	GND	GND	VHI10<0>	VHI10<1>	FLAG_AF	ADD<4>	VREF_ADC	AGND	AVDD	AGND	IN<0>	AGND	IN<1>	AGND	NC	VDDA_PAD
DAC_ALDO	GND	GND	GND	GND	GND	NC	NC	FLAG_AF		VCM_ADC	AGND	AVDD	AGND	IN<2>	AGND	IN<3>	AGND	NC	VDDA_PAD
NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<4>	AGND	IN<5>	AGND	NC	VDDA_PAD
NC	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<6>	AGND	IN<7>	AGND	NC	VDDA_PAD
OUT_TSPFF	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<8>	AGND	IN<9>	AGND	AGND	AGND
SIPM_CALIB	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<10>	AGND	IN<11>	AGND	NC	VREF_SK_LP
NC	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<12>	AGND	IN<13>	AGND	AGND	AGND
STROBE_EXT	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<14>	AGND	IN<15>	AGND	NC	VREF_NOINV_SK
EFUSE	NC	GND	DVDD	VDD_PLL	VDD_PLL	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<16>	AGND	IN<17>	AGND	NC	VREFINV_VBM3PA
TRIG_P	NC	GND	DVDD	VDD_SC	VDD_SC	AGND_PLL	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<18>	AGND	IN<19>	AGND	NC	VREFTOA_VBIPA
TRIG_N	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<20>	AGND	IN<21>	AGND	NC	VREFTOT_VBMPA
DAQ2_P	NC	GND	DVDD	DVDD	DVDD	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<22>	AGND	IN<23>	AGND	NC	VBG_1V
DAQ2_N	PLL_LOCK	GND	DVDD	VDD_SC	VDD_SC	GND	GND	GND	AGND	AGND	AGND	AGND	AGND	IN<24>	AGND	IN<25>	AGND	NC	PROBEPA_VBOPA
DAQ3_P	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<26>	AGND	IN<27>	AGND	NC	INCTEST
DAQ3_N	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<28>	AGND	IN<29>	AGND	NC	VDDA_PAD
ADD<3>	GND	GND	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	DVDD	AVDD	AVDD	AVDD	AGND	IN<30>	AGND	IN<31>	AGND	NC	VDDA_PAD
ADD<2>	GND	GND	GND	GND	GND	NC	NC	NC		VCM_ADC	AGND	AVDD	AGND	IN<32>	AGND	IN<33>	AGND	NC	VDDA_PAD
ADD<1>	GND	GND	GND	GND	GND	NC	VHI10<2>	NC	NC	VREF_ADC	AGND	AVDD	AGND	IN<34>	AGND	IN<35>	AGND	NC	VDDA_PAD
ADD<0>	PROBE_TOT_PA	PROBE_TOA	PROBE_DC2	PROBE_DC1	PROBE_INV	VNEG	VHI10<3>	PROBE_NOINV	TRIG_EXT	TRIG1_EXT	AGND	AVDD	AGND	AGND	AGND	AGND	AGND	AGND	AGND



Board power	Nominal value	ASIC power	Max ratings
Analog power	1.2 Volts	AVDD, VDD_PLL	8 mW / chn
Preamp power	2.5 or 1.2 Volts (CALO-A or CALO-B)	AVDD_PAD	2 mW / chn
Digital power	1.2 Volts	DVDD	5 mW / cnn

Values will be refined after first measurements

IPDR 2024 – CALOROC Related Comments

1) For the ASICs, we recommend a strong monitoring of the progress towards finalization of the designs and the decision making between options (e.g., CALOROC v1A or v1B)

=> Selection based on the characterization and on SiPM capacitance

- For the EICROC/CALOROC designs, there is a worry that human resources for digital design may be limited in the key institutes. This must be monitored closely. Can

=> Permanent position open at OMEGA in 2025 (possible to stabilize our fixed-term position)

3) For the CALOROC and SALSA, it was unclear how the 40/50 MHz sampling would translate into the 100MHz BX regime and the time-tagging of the hits. This should be clarified and documented.

=> CALOROC is working at 39.4 MHz to be compatible with LpGBT. Time reconstruction will be handle in the back-end. A new fast command has been added to keep the synchronization with the back-end.