EICROC status and plans
EAP 26 sep 2025

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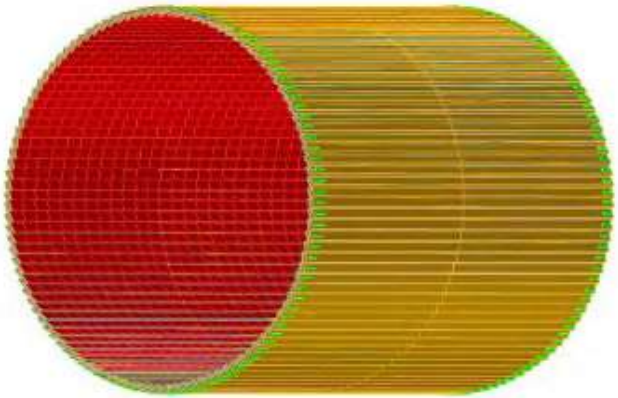
Organization for Micro-Electronics desiGn and Applications

ePIC AC-LGAD detectors

Specifications of ePIC AC-LGAD detectors:

BToF



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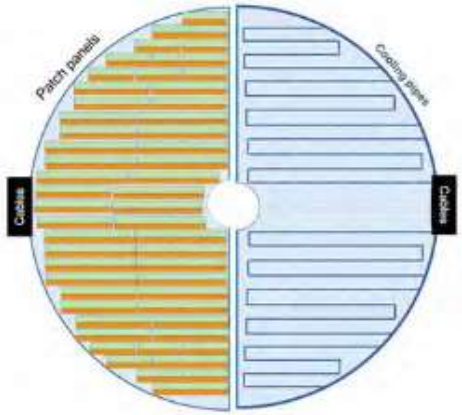
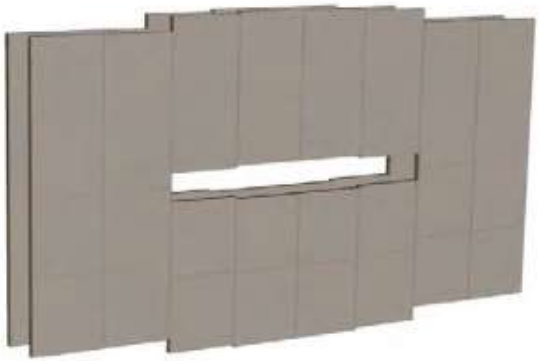


Roman Pots

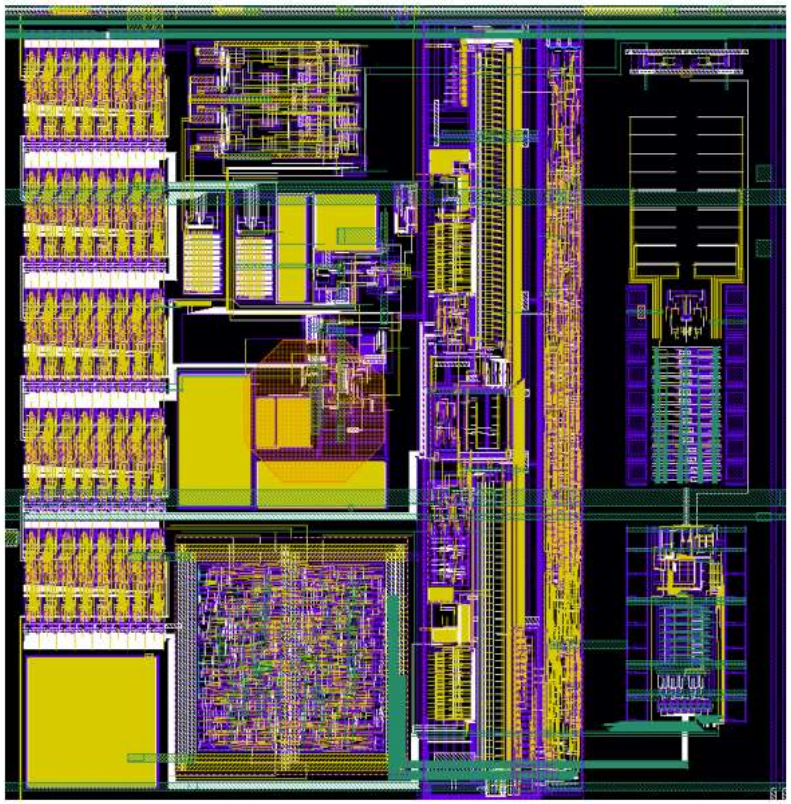


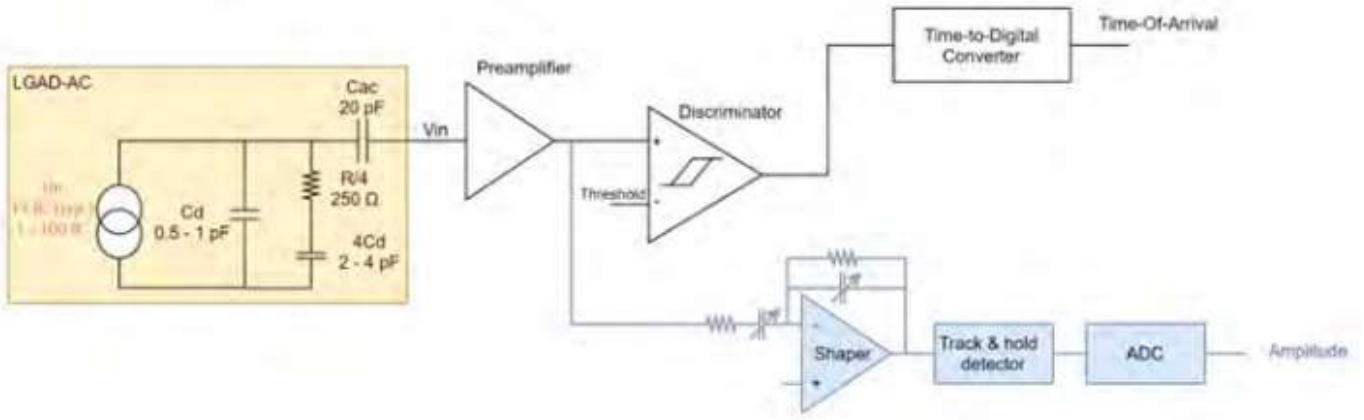
4D Trackers

	Area (m^2)	Channel size (mm^2)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10.9	0.5*10 (strips)	2.4M	30 ps	30 μm in φ	0.01 X0
Forward TOF	2.22	0.5*0.5 (pixels)	8.8M	25 ps	30 μm in x and y	0.08 X0
B0 tracker	0.07	0.5*0.5 (pixels)	0.28M	30 ps	20 μm in x and y	0.05 X0
RPs/OMD	0.14/0.08	0.5*0.5 (pixels)	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

EICROC0

- Analog frontend similar to ATLAS ALTIROC but 0.5x0.5 mm²
  - Cd = 1 pF (max 3 pF)
- ADC instead of ToT for charge measurement : 8bit 40 MHz from AGH Krakow
- TDC taken from HGCROC by CEA Saclay
- Simple digital readout but SEE-proof I²C slow control
- ~2 mW/pixel
- Fabricated in spring 2022 in TSMC 130nm

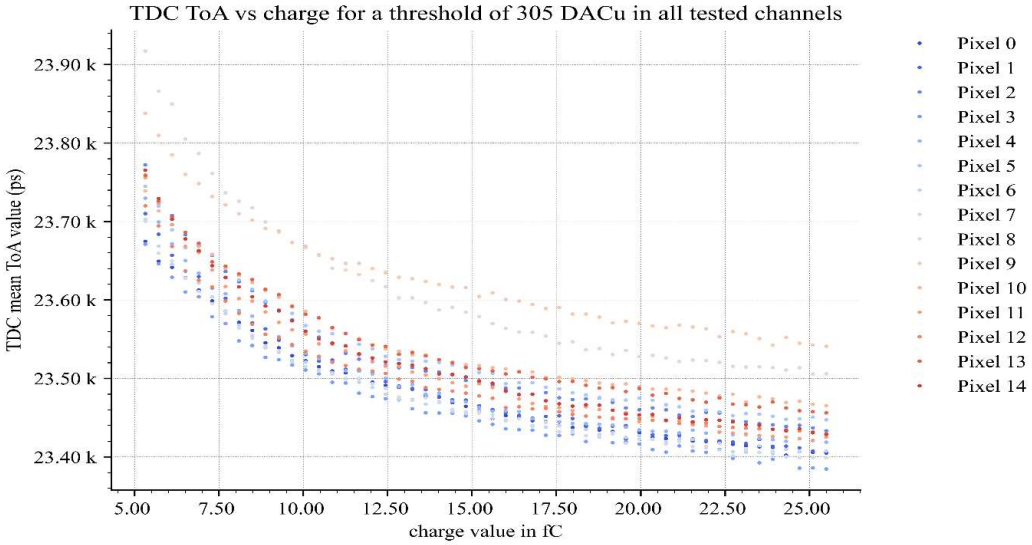


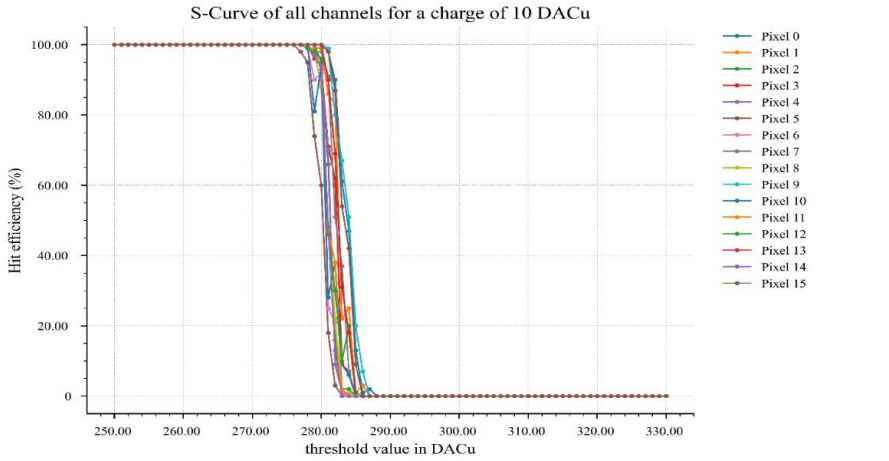


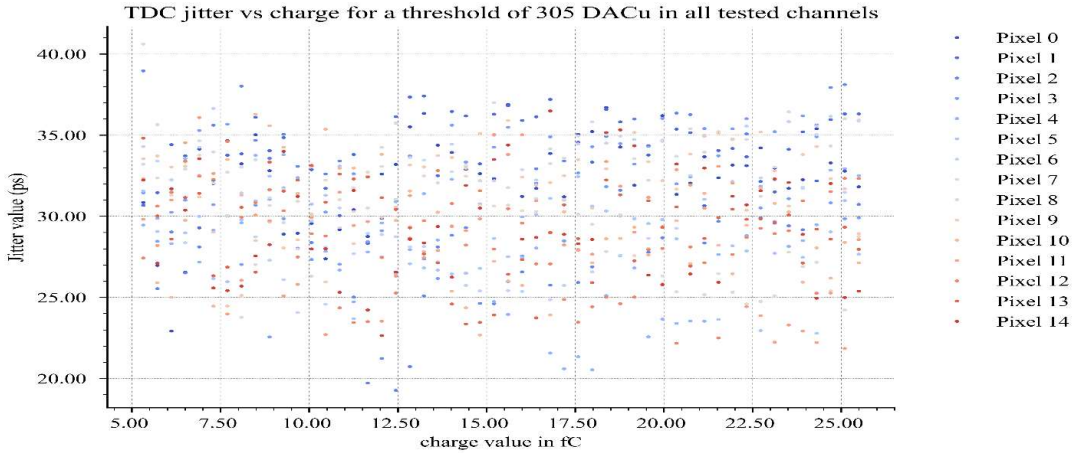
Slow control | PA +discri | TOA TDC | 8b 40M ADC

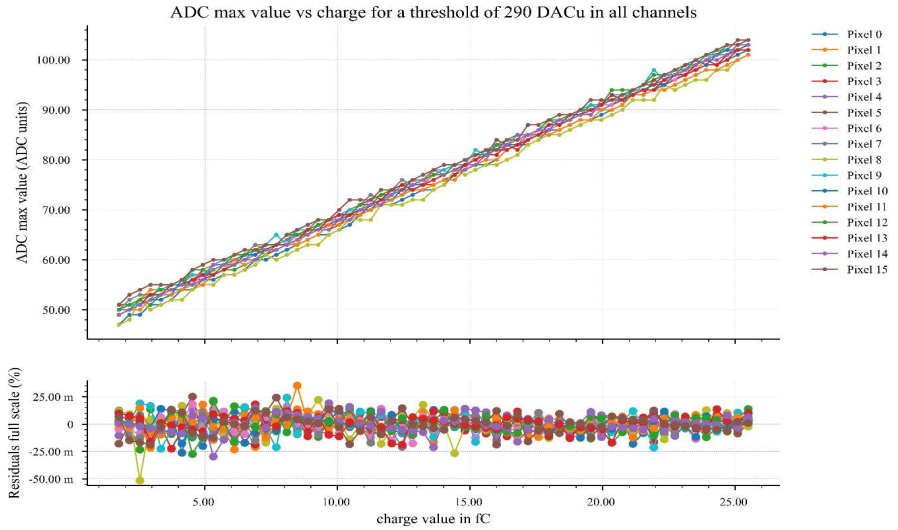
ΩMEGA Microelectronics | Irfu | AGH

EICROC0 performance (ASIC alone) [A. Verplancke]









2025 : EICROC0 variants

- EICROC0A : same as EICROC0 with more testability
  - Each pixel can be by-passed by SC (clock is then turned off)
  - Buffers in SC to allow extension to 4x32
  - Larger dynamic range in pulse injection

- EICROC0B (4x4)
  - Same preamp/discri/TDC/integrator
  - ADC and driver replaced by peak sensing and Wilkinson ADC
  - Currently ADC path ~1 mW/ch becomes 200 uW/ch

- EICROC1A : 4x32
  - Same I/Os than EICROC0, same testboard

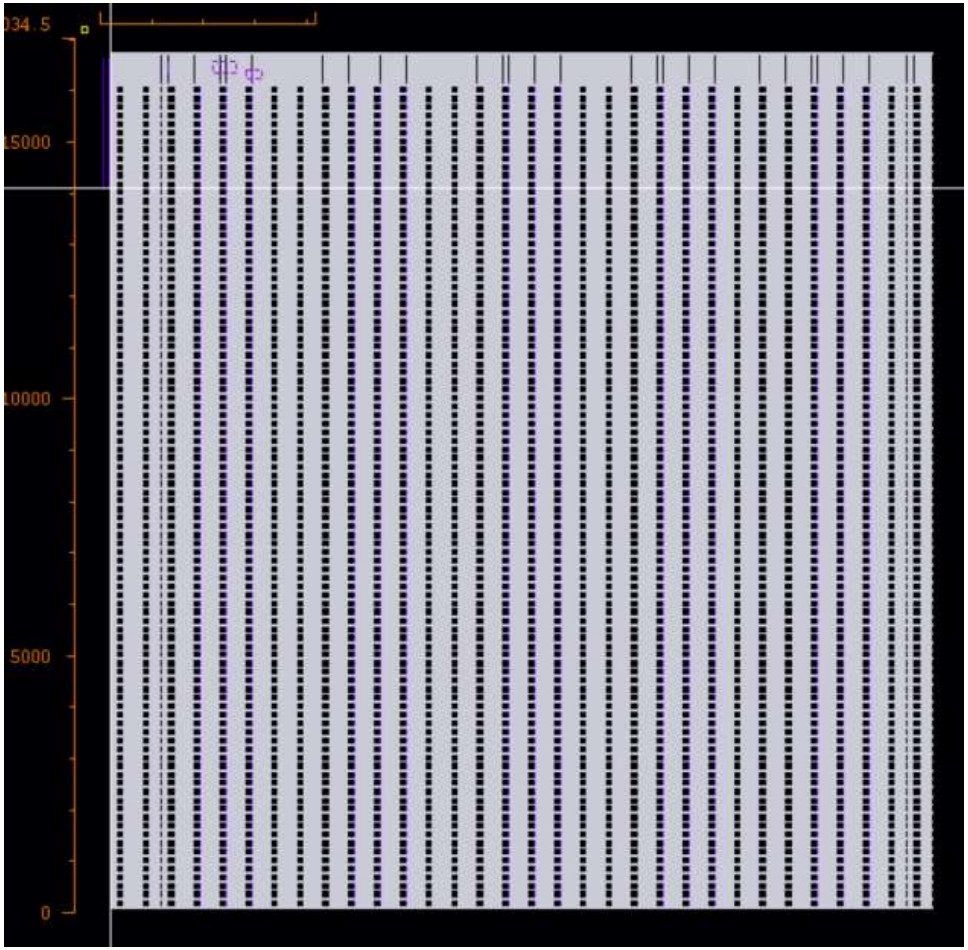
- Will be fabricated with EICROC1 below

2025 : EICROC1

- 32x32 chip : final dimensions

- Goal :
  - test full-scale chip analog performance (IR drops)
  - Allow final sensor characterization
  - Test interface with DAQ : fast commands and 320 Mb/s data output
  - Progress on module/front-end boards

- Caveats ;
  - Not (yet) zero-suppressed data
  - Still 2mW/ch
  - Still analog-on-top

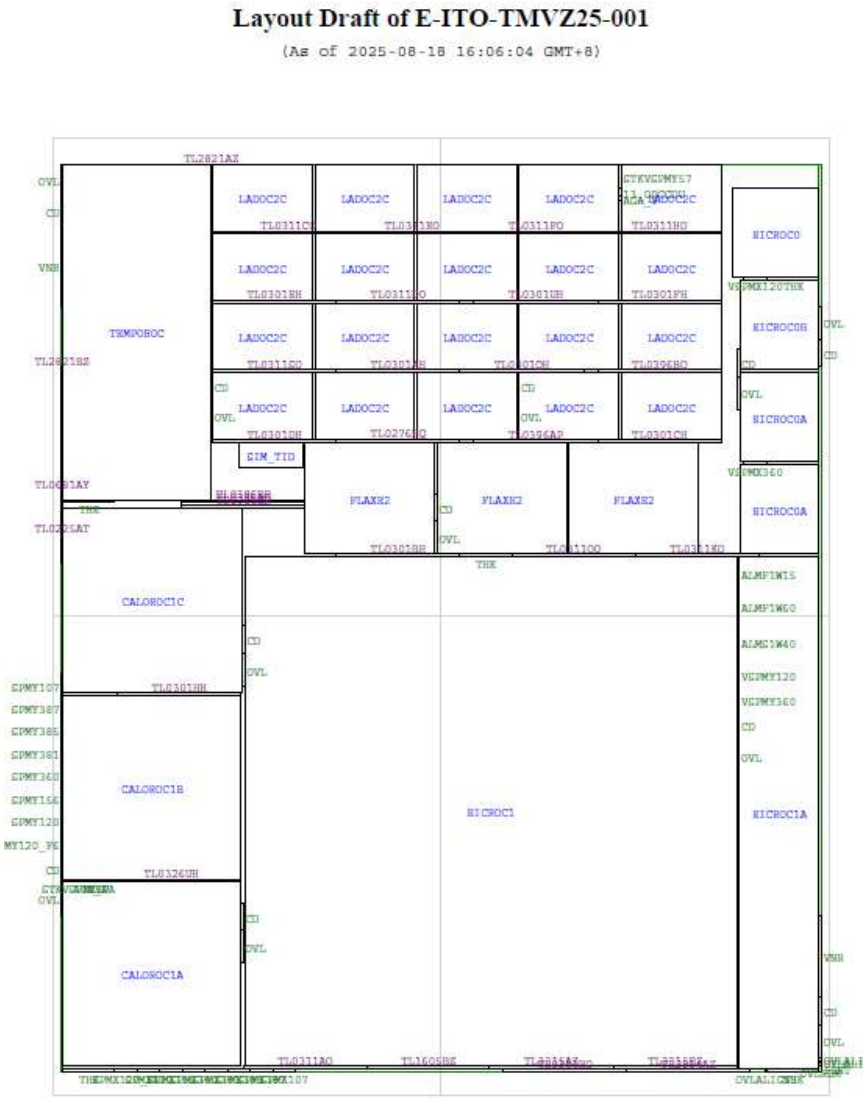


EICROC reticle 2025

- EIC/ATLAS engineering run (may 25)
  - Just started this week (long administrative issues)

- EIC chips 63% of wafer area
  - EICROCs 48% = 130 k€
  - 100 k€ of EICROC1 paid by ANR
  - Rest paid by 2024 money

chip	area	Fraction	#		cost
CALOROC1A/B/C	113,807	15,3%	3	C4	40 500 €
EICROC0/A/B	27,807	3,7%	3	WB	9 895 €
EICROC1	283,860	38,0%	1	WB	101 015 €
EICROC1A	47,810	6,4%	1	WB	17 014 €
LADOC2C	160,992	21,6%	20	WB	57 291 €
TEMPOROC3	56,927	7,6%	1	C4	20 258 €
FLAXE2	52,650	7,1%	3	WB	18 736 €
SM_TID	2,170	0,3%	1	WB	772 €
Total	746,022	100%	33	0	265 482 €

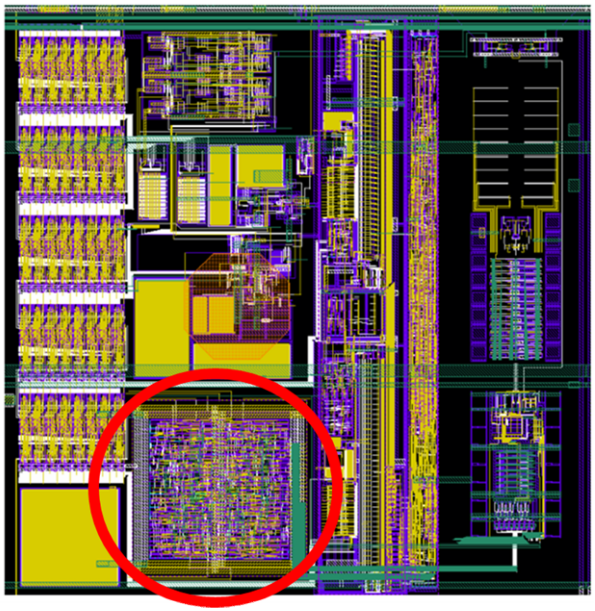


Future EICROC2 (2026)

- What is missing in EICROC1 ?
  - Larger rate compatibility ?
  - Derandomizer for successive events (how many ?)
  - Digital on Top (DoT) design for digital power reduction and timing verification on large area : more powerful tools available (UVM)
  - Auto-trigger and zero_suppressed data
  - Power reduction if possible down to ~1 mW/ch

- Our colleagues from Clermont Ferrand now joining to help on the DoT
  - Already participated in ATLAS ALTIROC
  - The design and verification should take ~1 year from now

- Technology choice ?
  - Depends mostly on rate estimates and complexity of digital



2026 : requests and plans

- Test of EICROCO/A/B/1/1A
  - Chips should arrive end 2025. Dicing and bonding to foresee
  - Testboards and test equipment (5 k @LPC)
  - Tests with sensors (Ijclab/BNL)

- Design of EICROC2 with Clermont
  - Simulations, choice of technology
  - Prototype analog blocks EICROC0 in 65 nm (MPW 3x3 mm² = 9*4190€ ~ 40 k€ via ANR)
  - Travel to/from Clermont

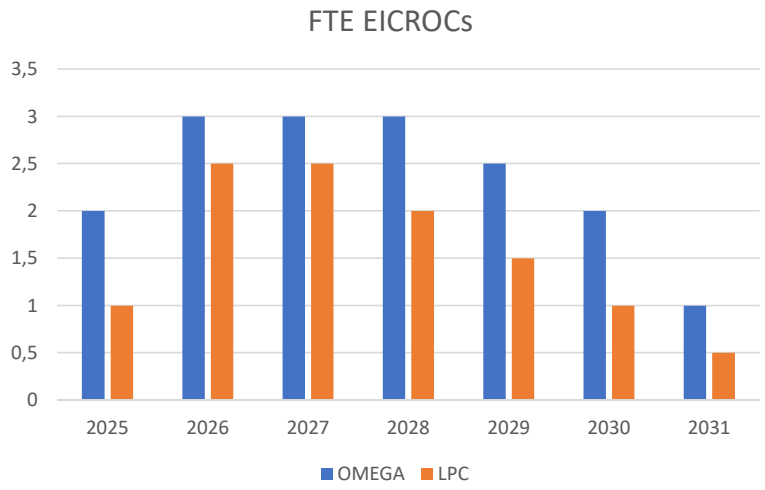
- Start to send the money to CERN for the next engineering run
  - 300 k€ in 130nm and/or 650 k€ in 65 nm

- Travels : (5+2) persons/2 and 2 meetings/yr = 12 k€ Ω + 3 k€ LPC

EICROC timeline & FTEs

- Sept 2025 : EICROC1 fabrication
- 2026 : test of EICROC1 and design of EICROC2 DOT + EICROC0/65n
- Beg 2027 : fabrication of EICROC2
- Mid 2027 : test of EICROC2
- 2028 : more system tests and possibility for an iteration EICROC3
- 2029-2030 : fabrication (6 wafers are enough for RPs)

- FTEs
  - Design : 2-3 OMEGA + 2-3 LPCF : 2026-2031 + 0.25 IRFU
  - Test : 1 OMEGA + 1 LPCF
  - Production test on wafer : to be subcontracted



summary

- EICROC now reached full scale 32x32 with EICROC1
  - Important for analog performance and sensor test
  - Also allows to progress on system design (1 yr of tests foreseen = 2026)

- Small scale EICROC0s 4x4 still under test to improve performance and reduce power
  - Foresee also version in 65n in case digital does not fit in 130n

- EICROC2 now needs its digital design : ~1 year design time from now
  - With the most welcome help from LPC Clermont Ferrand
  - Main driving specification is the hit rate : 50 Hz/pixel OK ?
  - Engineering run foreseen Q1 2027

- Administrative agreement to pay for the runs should be handled by IN2P3
  - We lost 6 months in 2025 due to administrative delays…

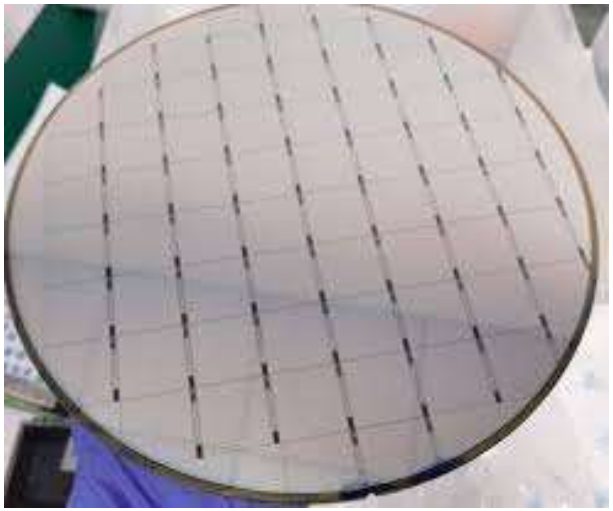
backup

Path towards production and QC

- For roman pots ~500 chips would be needed (500 k ch) = 6 wafers
  - Small quantity (200 wafers done for ATLAS or CMS)

- Final version would be an EICROC3 to fix possible bugs in EICROC2
  - ~1 year after EICROC2 tests and system tests complete

- Wafer probing station and test setup will be needed
  - Can be inspired from ALTIROC setup



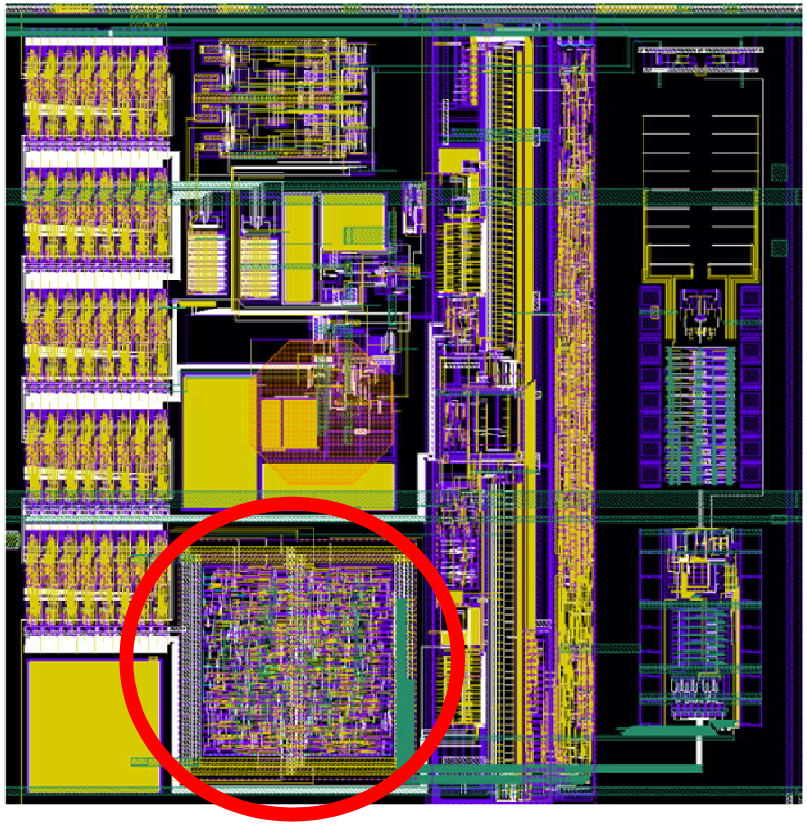
EICROC1 max rate

- Payload and readout speed
  - Each pixels provides 8 samples of 24 bits (12b TDC 12b ADC) at 40 MHz + header
  - 200 bits * 25 ns = 5 us/pixel
  - 128 pixels * 5 us = 640 us => ~1.5 kHz maximum rate per block of 4x32 ~10 Hz/pixel
  - Same rate for full chip with serialized 320 MHz output
  - Spec is 15 Hz/pixel (max 28 Hz)

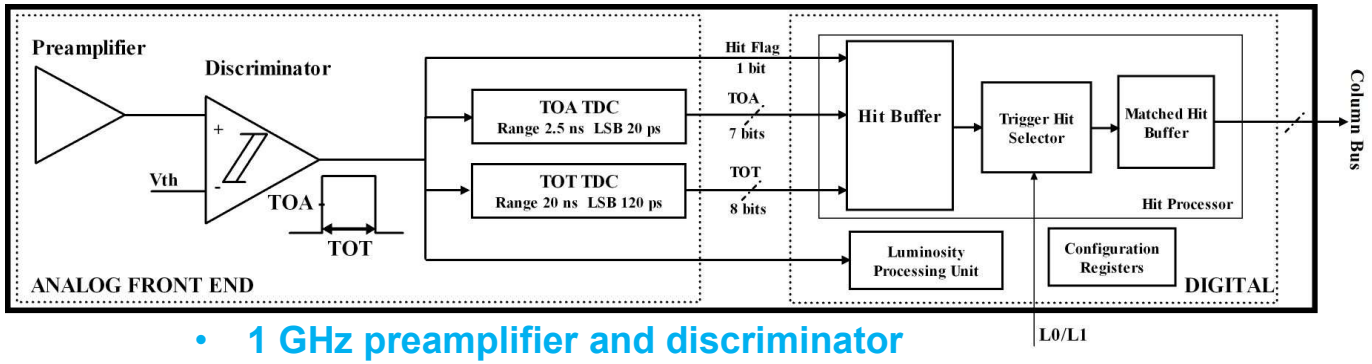
- Future improvements
  - Payload reduction to 12b TD C + 5 samples of 8b ADC = 64 bits => ~30 Hz/pixel max rate
  - Zero-suppression : read only channels with hits and their (4-8) neighbours (for barycenters)
  - With 1 hit/column gives ~10 improvement => ~300 Hz/pixel max rate
  - A derandomizer would also be needed

Technology choice 65/130n

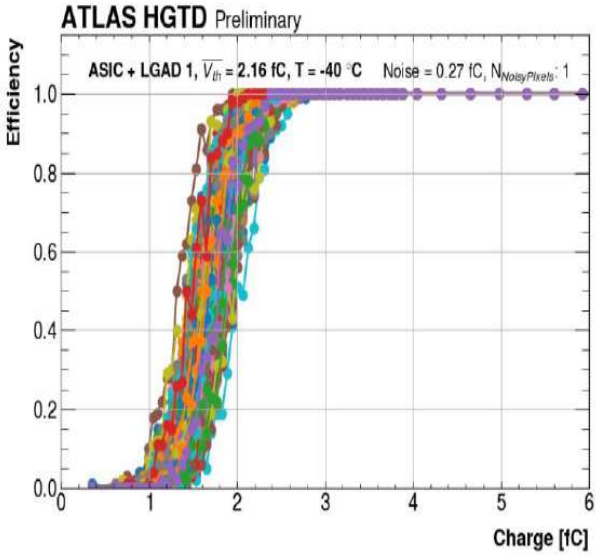
- Little impact on analog/digital performance
  - Analog similar in 65/130
  - Possibly more significant on TDC
  - Digital much simpler than LHC chips
- Update of digital part
  - Little space available => main reason for 65 !
- sizeable cost impact : ER 700 k$ vs 300 k$
  - But possibly more partners (but EICROC 50% of reticle)
- Prepare for design in 65 nm
  - Make an EICROC0/65n to test analog part and TDC

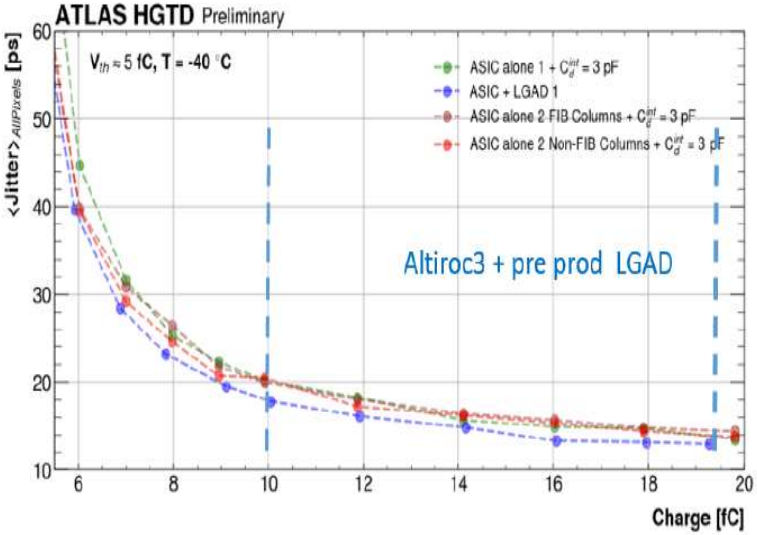


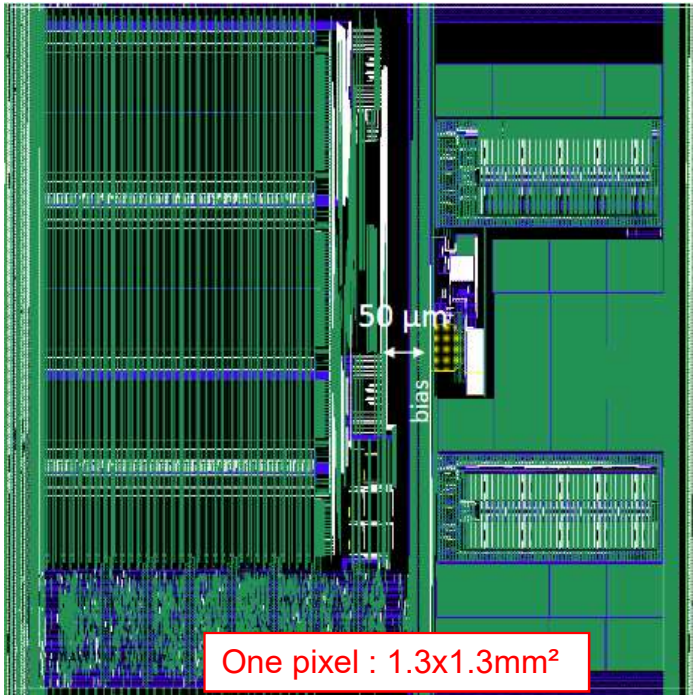
ALTIROC pixel scheme and layout



- **1 GHz preamplifier and discriminator**
- **2 vernier TDCs for ToA and ToT**
- **Hit buffer:** SRAM 1536 x 19 bit (38 µs latenccy)







Chips versions

Chip	date	Techno	size	Analog	Digital	goal
EICROC0	Jun 2023	130n	4x4	Conservative	Simple	Study sensor
EICROC0A/B	beg 2025	130n	4x4	Low power	same	Study analog
EICROC1	beg 2025	130n	32x32	Conservative	Same	Study power distribution
EICROC0_65n	end 2025	65n	4x4	final	Simple	Study analog in 65n
EICROC2	End 2026	?	32x32	Low power	Final	First final prototype

Chip	date	Techno	size	Analog	Digital	goal
CALOROC1A	beg 2025	130n	36ch	Conservative	Final	Study sensor
CALOROC1B	beg 2025	130n	36ch	Low noise	final	Study analog
CALOROC2	End 2026	130n	36/72	final	final	First final prototype