ATLAS Phase-II upgrades for the High-Luminosity LHC

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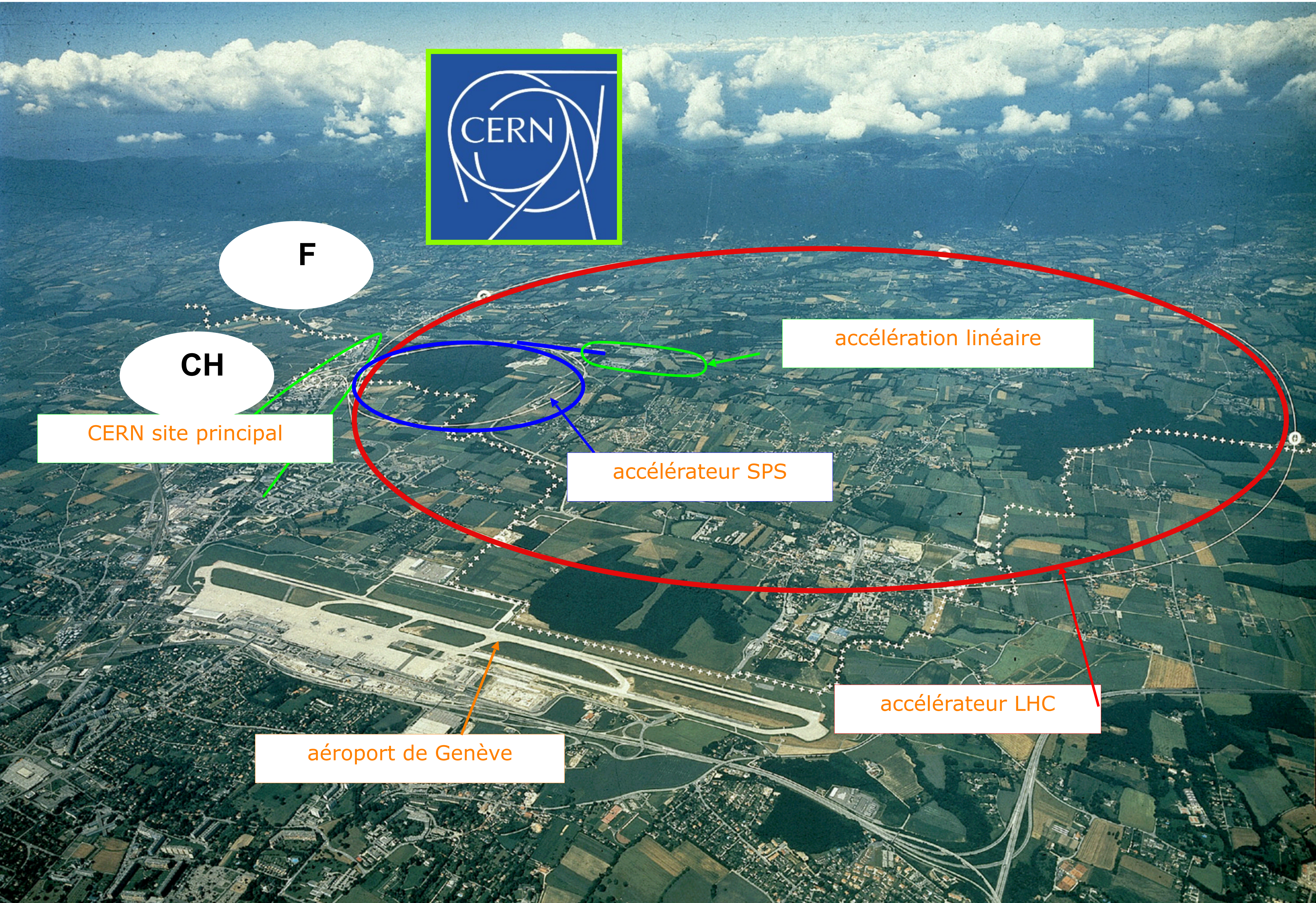
(based on the work of thousands of physicists, engineers, technicians,…)

1st of July 2025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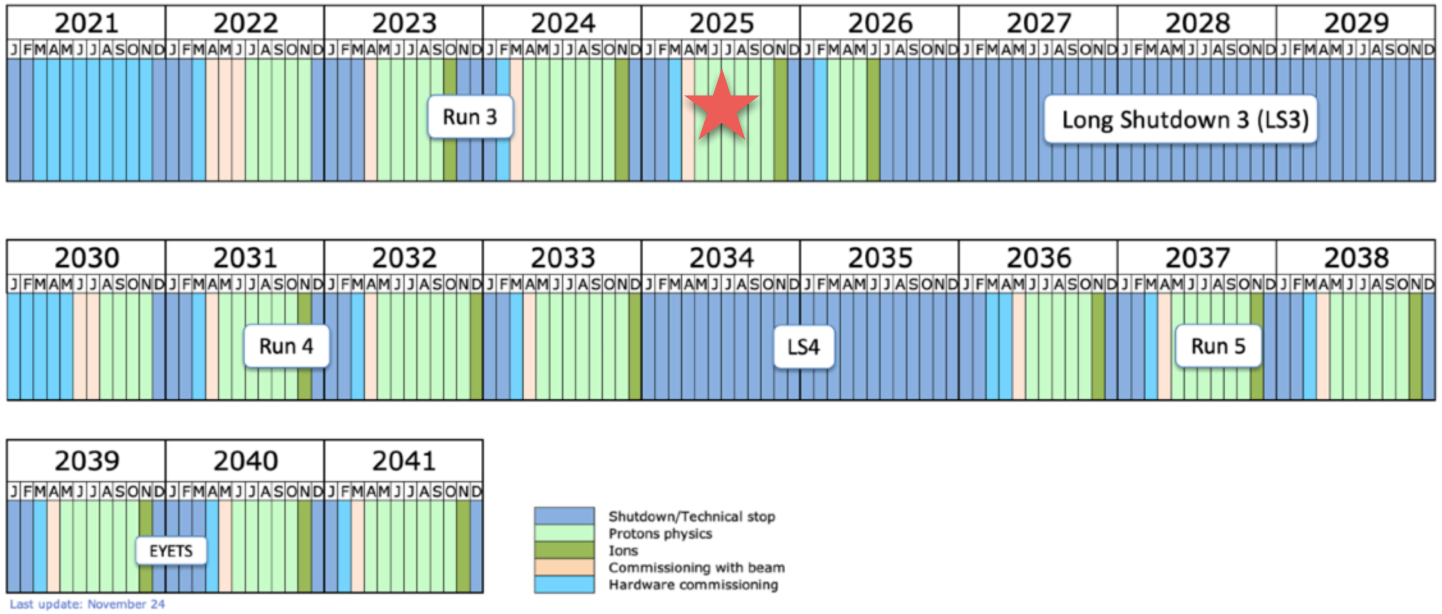
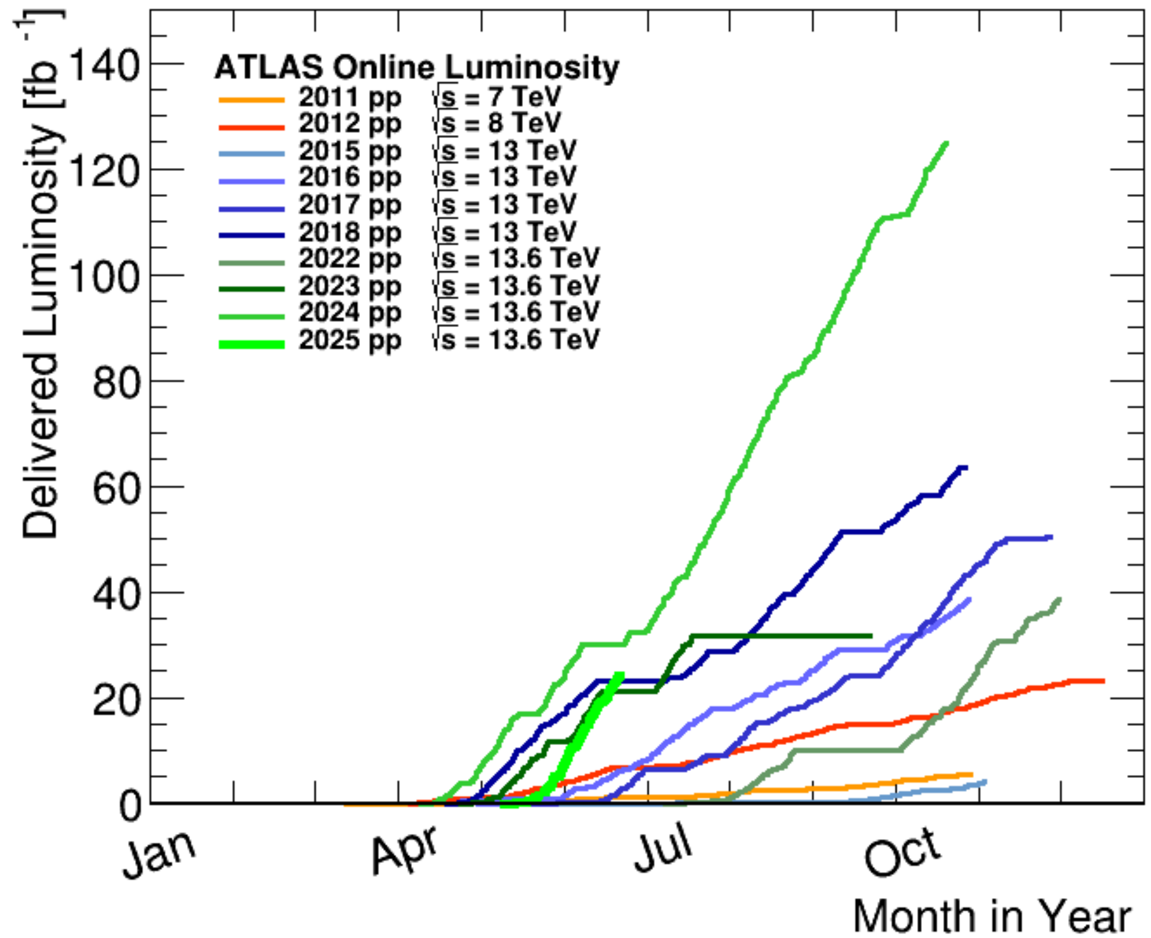
Introduction

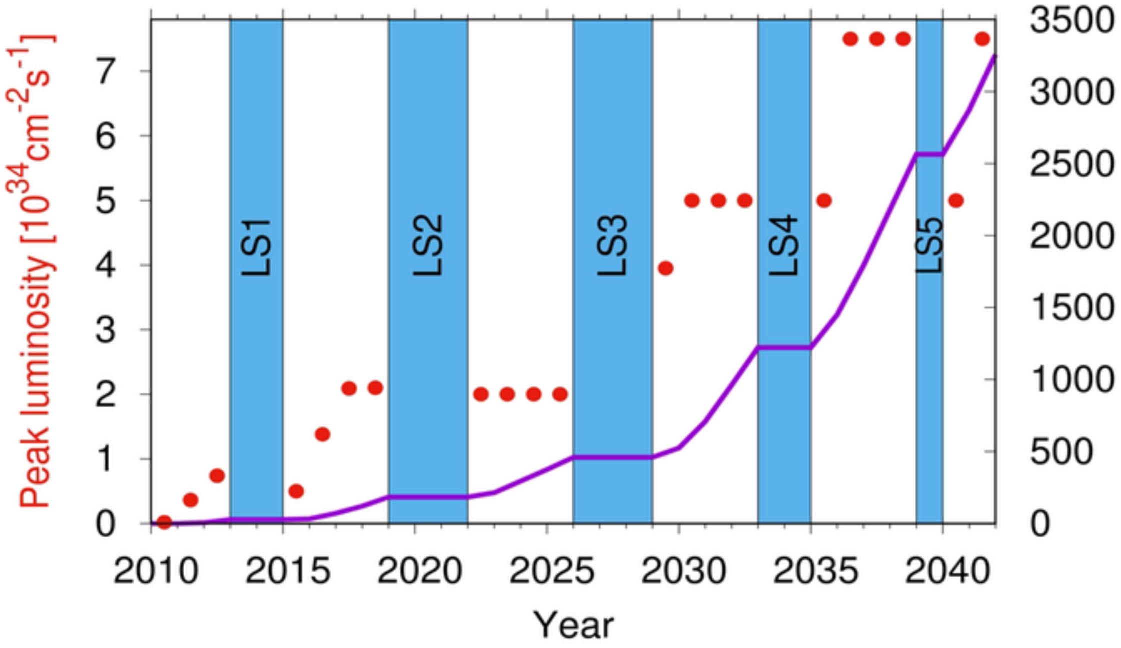




- The LHC is ageing well, providing lots of good data since 2010
- But it's only half of its lifetime as it will be continued with the HL-LHC program (2030-2041):
  - Higher levelled luminosity: 4x10^34 cm-2s-1 to 5x10^34 cm-2s-1.
  - —> Expecting ~250 fb-1 integrated luminosity for pp collisions / year
  - —> Should provide >~3000 fb-1 of integrated luminosity
  - Maximum levelled luminosity of 7.5x10^34 cm-2s-1
  - —> Higher increased radiation doses: up to an order of magnitude larger than nowadays
  - —> Higher pile-ups: <mu> = 55 (Run3) to <mu> ~ 200
- Will allow to probe the Standard Model even more precisely and especially rare processes

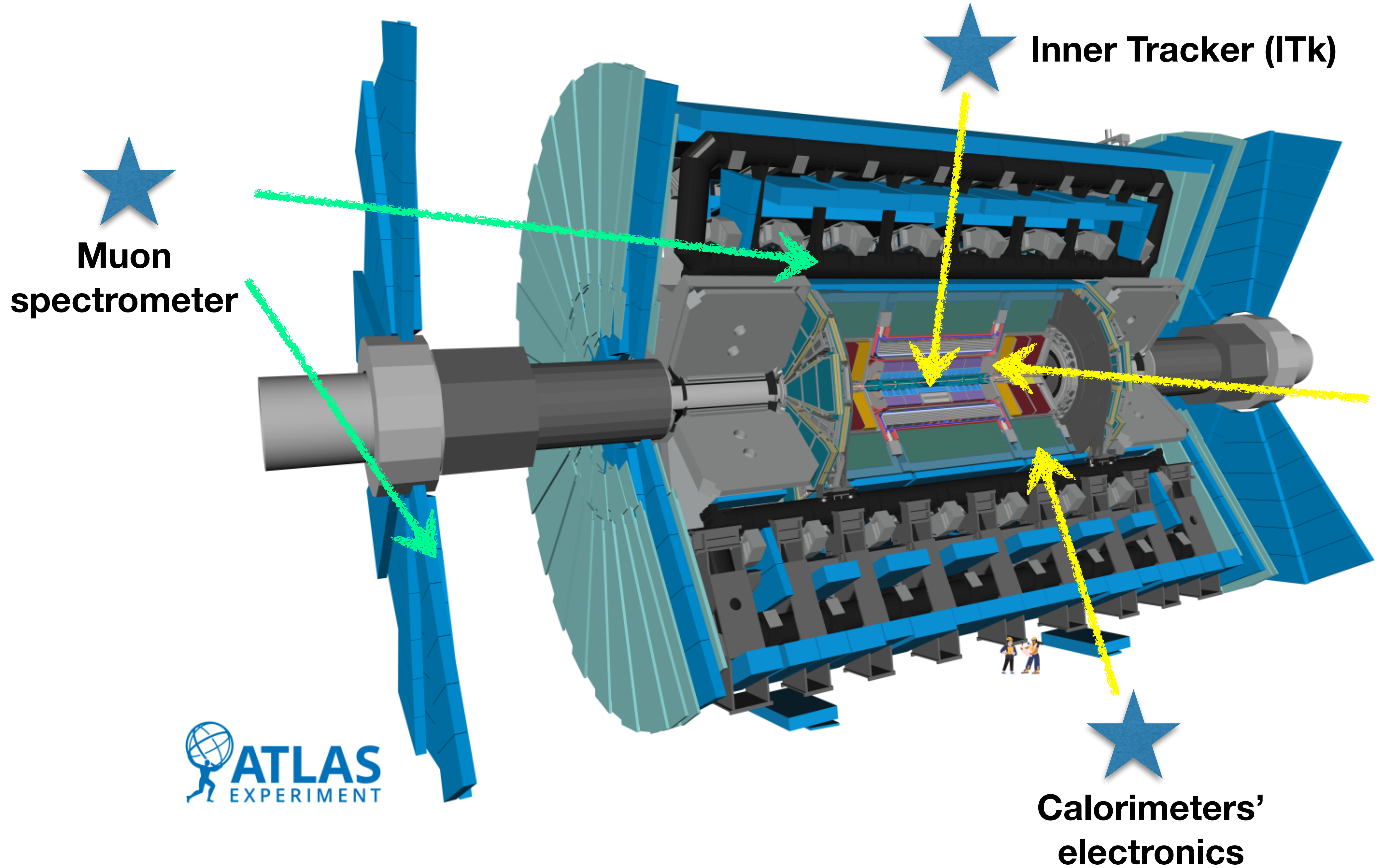
Necessity for ATLAS Phase-2 upgrades

- To benefit from the higher luminosity, the level-0 trigger rates need to increase from 100 kHz to about 1 MHz
  - This requires a new TDAQ (trigger & acquisition) system to maintain (or even decrease) the thresholds used to trigger the recording of specific (HL-)LHC bunch-crossings
  - New trigger and readout electronics need to be used by sub-systems (Tile & LAr calorimeters and the muon spectrometer)



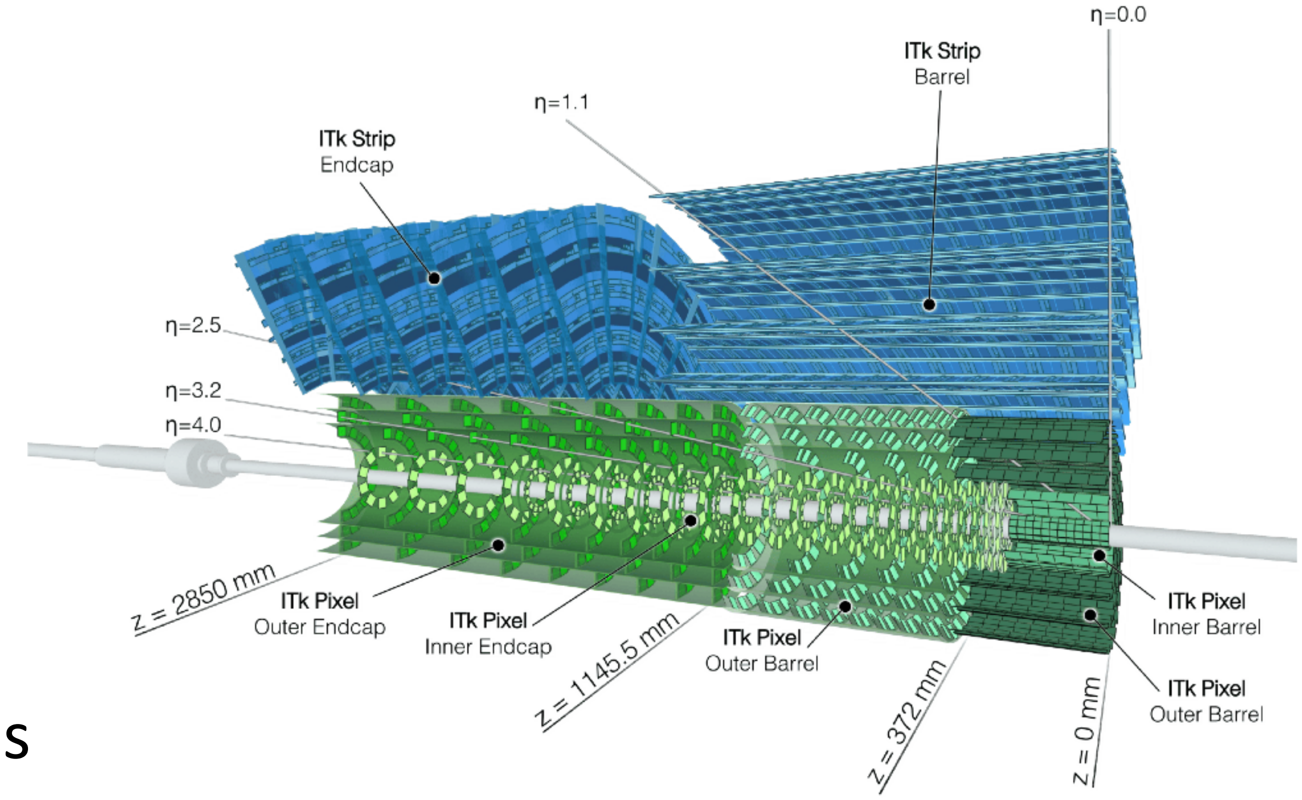
- To cope with the increases radiation doses (up to an order of magnitude), a new radiation-resistant inner detector (ITk) will replace the current Pixels + SCT + TRT one
- To better reject the increased pile-up, a new timing detector (HGTD) will be installed
- Summed up, ATLAS should have during the HL-LHC a larger cover with a better granularity and background rejection

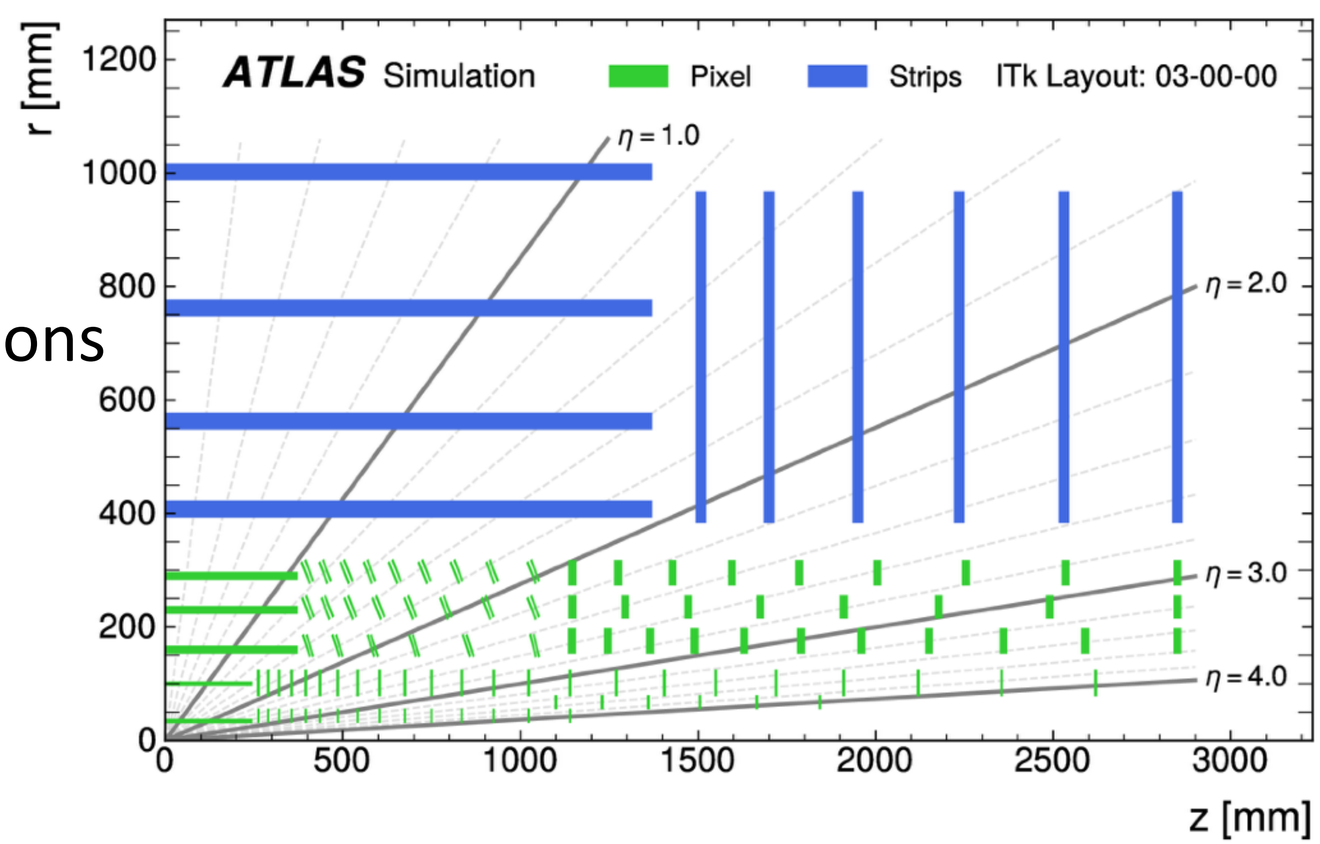
All ATLAS Phase-2 upgrades in one view



Trigger and Data acquisition

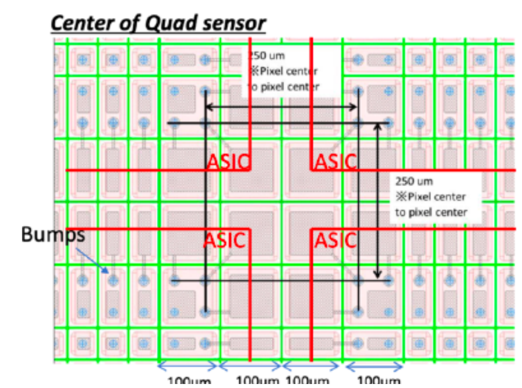
- Completely new silicon-based tracker
  - Inner part made of pixels
    - 5 billions channels in 5 layers (barrel) and rings (end-caps)
  - Outer part made of strips
    - 60 millions channels distributed in 4 layers of strips « staves » in the barrel and 6 layers of disks in end-caps
  - Coverage up to |η| = 4
  - Should provide at least 9 hits per track in the central region
  - Low material budget in the forward regions
  - Pile-up- and radiation-compliant

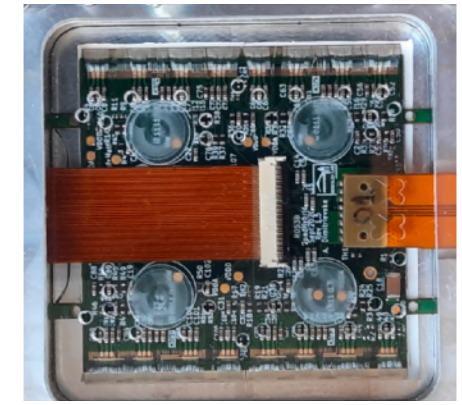


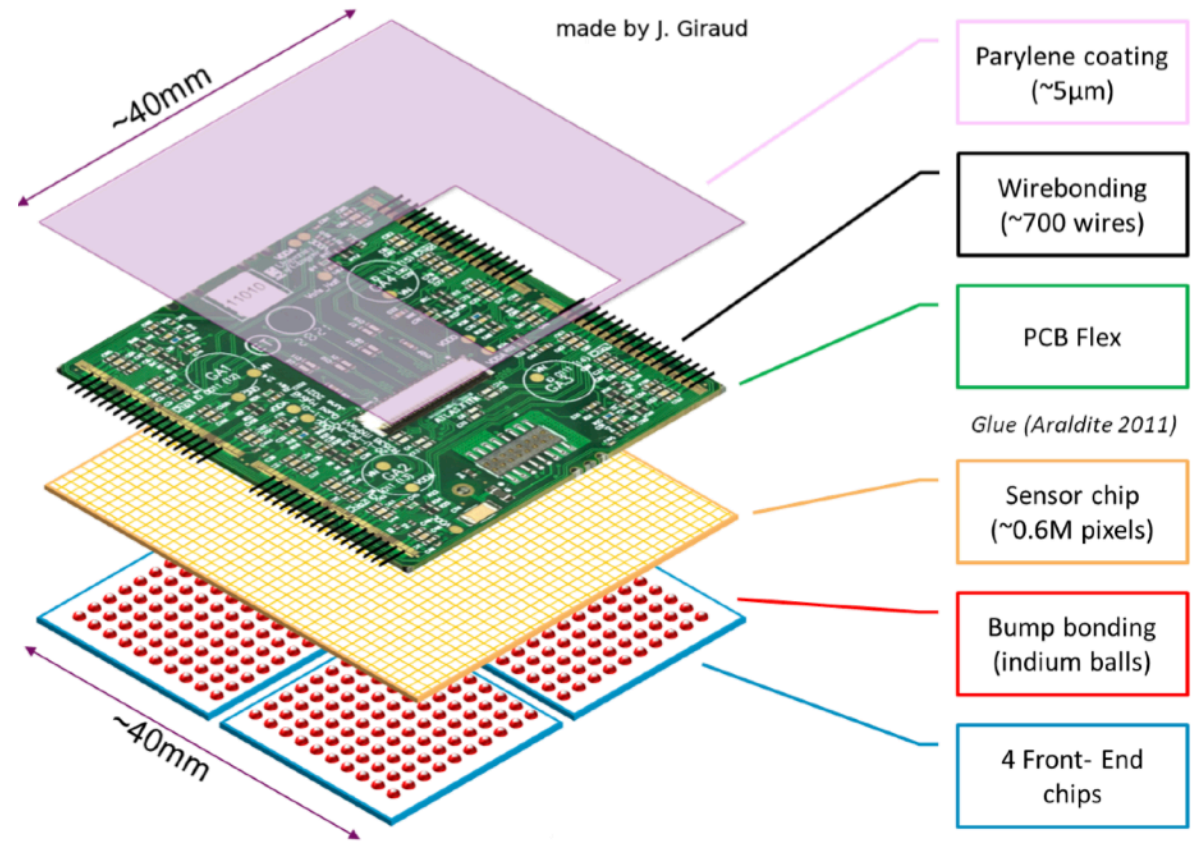


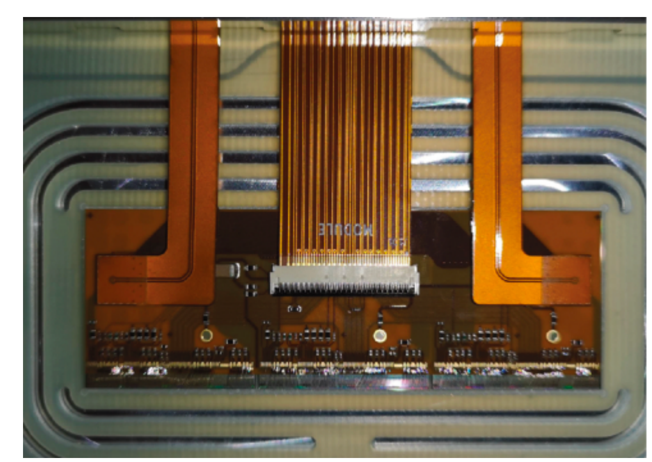
ITk Pixels

- Innermost layer of pixels
  - 3D sensors technology for the inner-most layers (more radiation tolerant / more expensive)
  - 2600 modules are needed organised in triplets
- Other layers use
  - n-in-p planar sensor
  - 7166 modules organised in quad (~13m^2)
- Sensor sandwiched between flex PCB and front-end chips inside the modules
  - chip is bump-bounded to the sensor
  - flex PCB wire bonded to the Front-End chips
- Production:
  - Very complex assembly process, distributed across 20 institutes
  - ~1/2 of production done for sensors and chips
  - started module assembly
  - module loading on structure has started

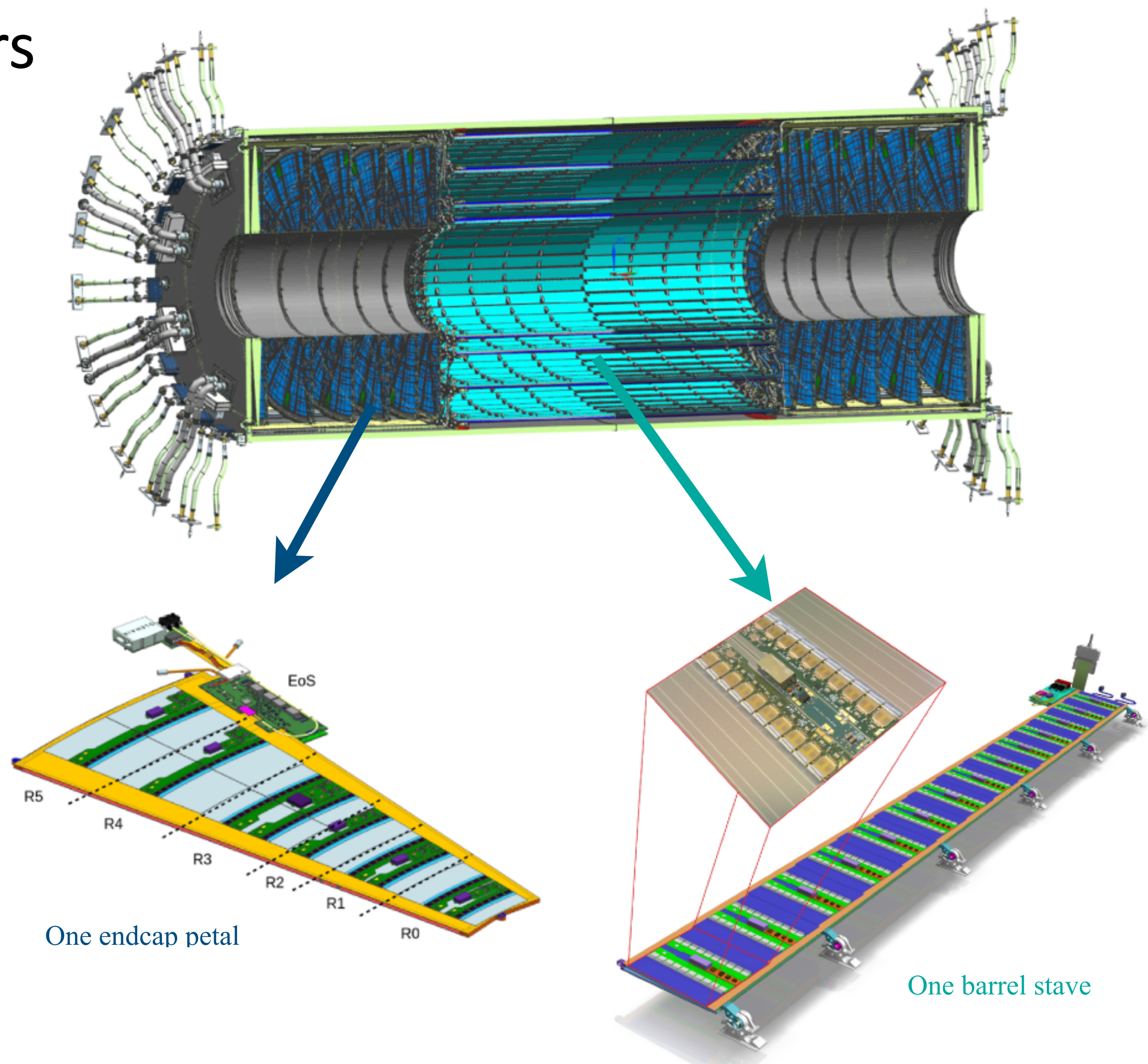


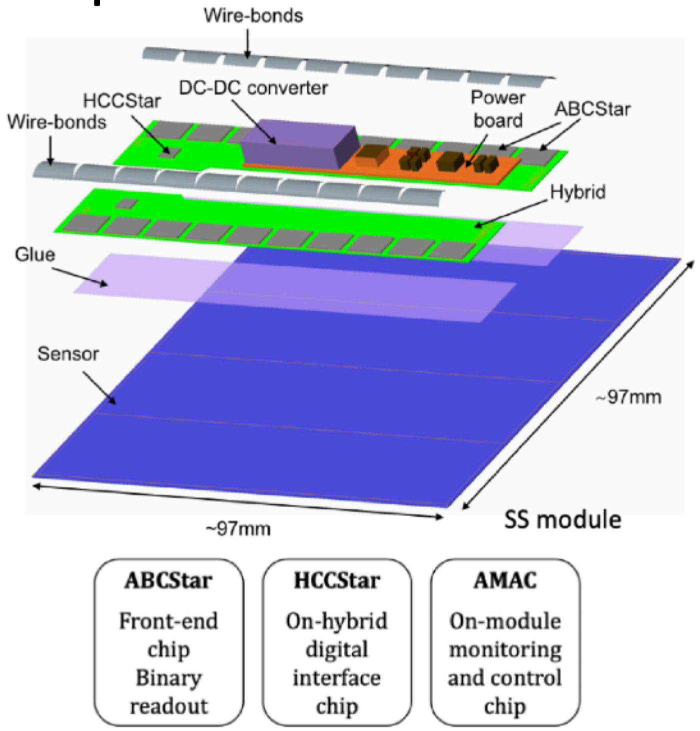






- Modules mounted on « staves » for barrel & « petals » for end-caps
  - 4 of (2 short- and 2 long-) strips modules layers in the barrel
  - 6 disks on each side
- Strip sensor typically is $10 \times 10\ \mathrm{cm}^2$
- Strip pitch is $75.5\ \mu\mathrm{m}$
- Hybrids hosting readout (ABCStar) ASICs + power modules are glued into the n-on-p sensor
- Strips wire-bonded to the ABCStar chips

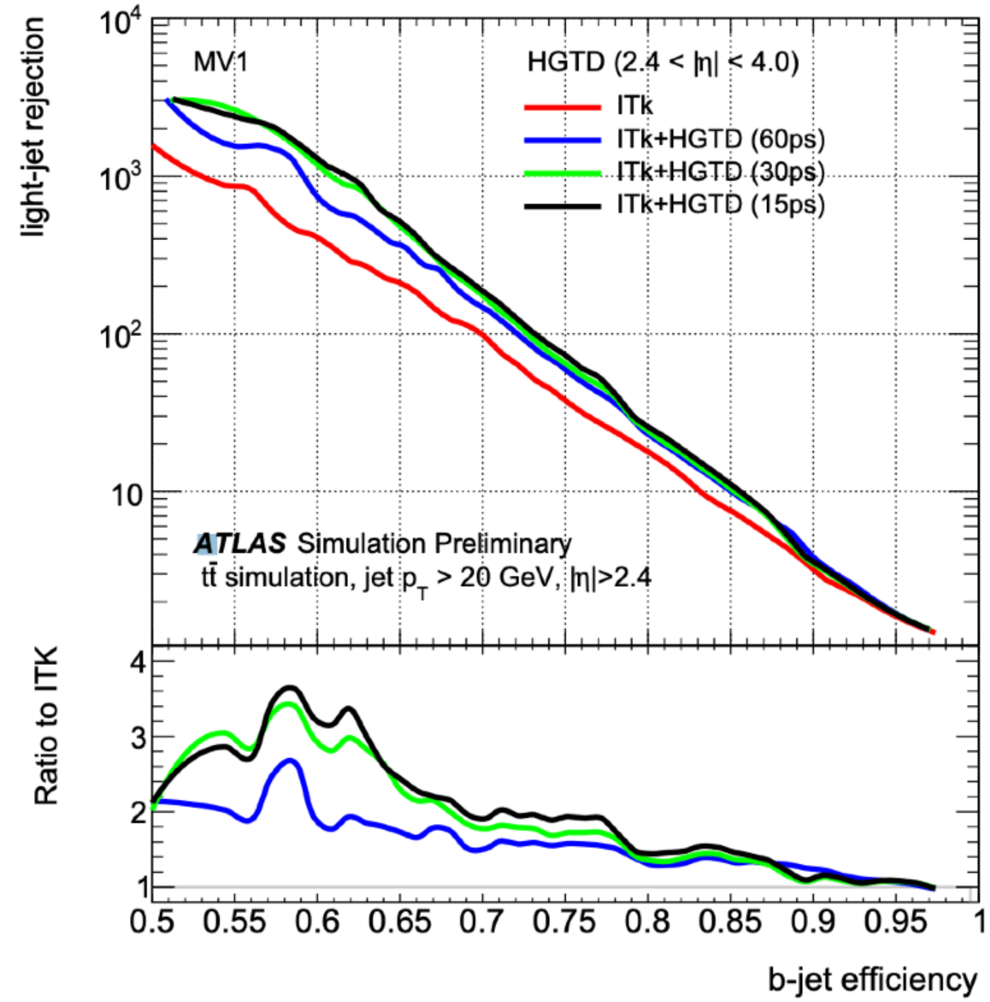


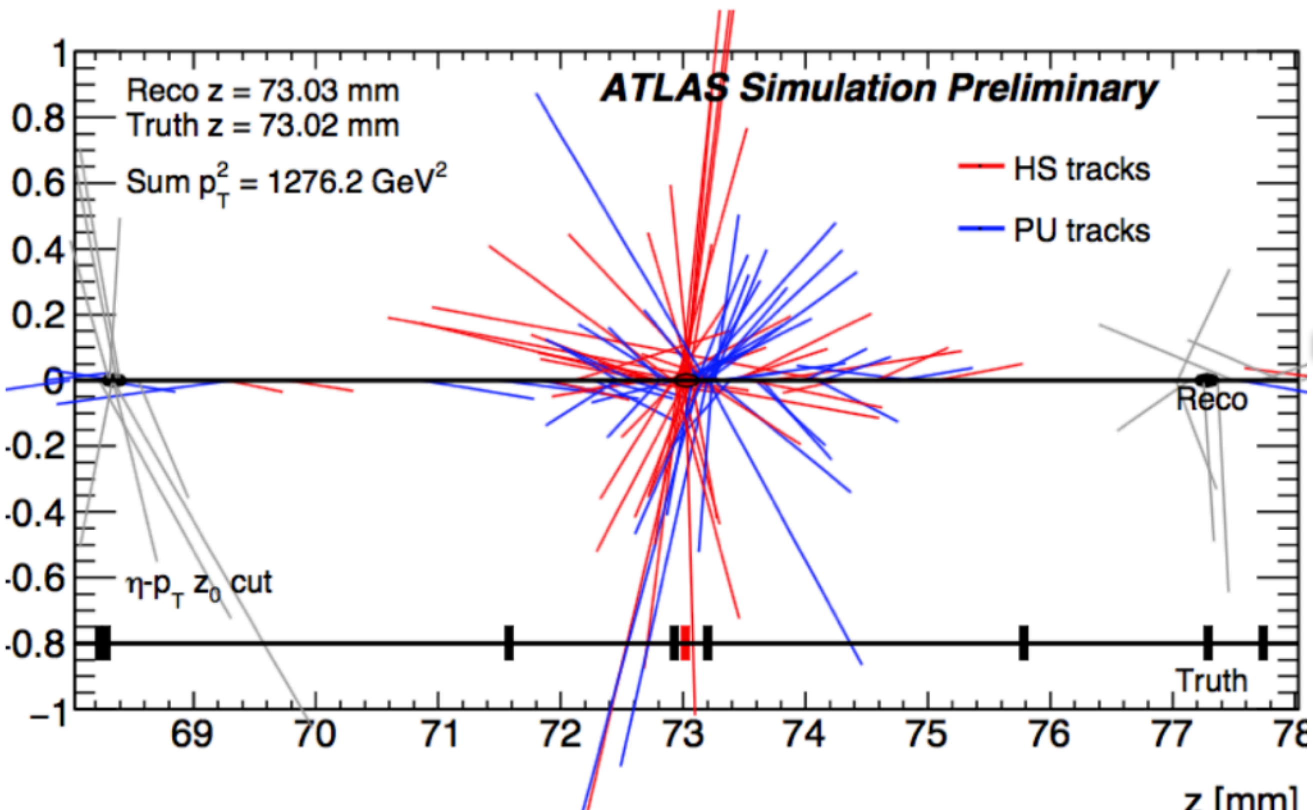


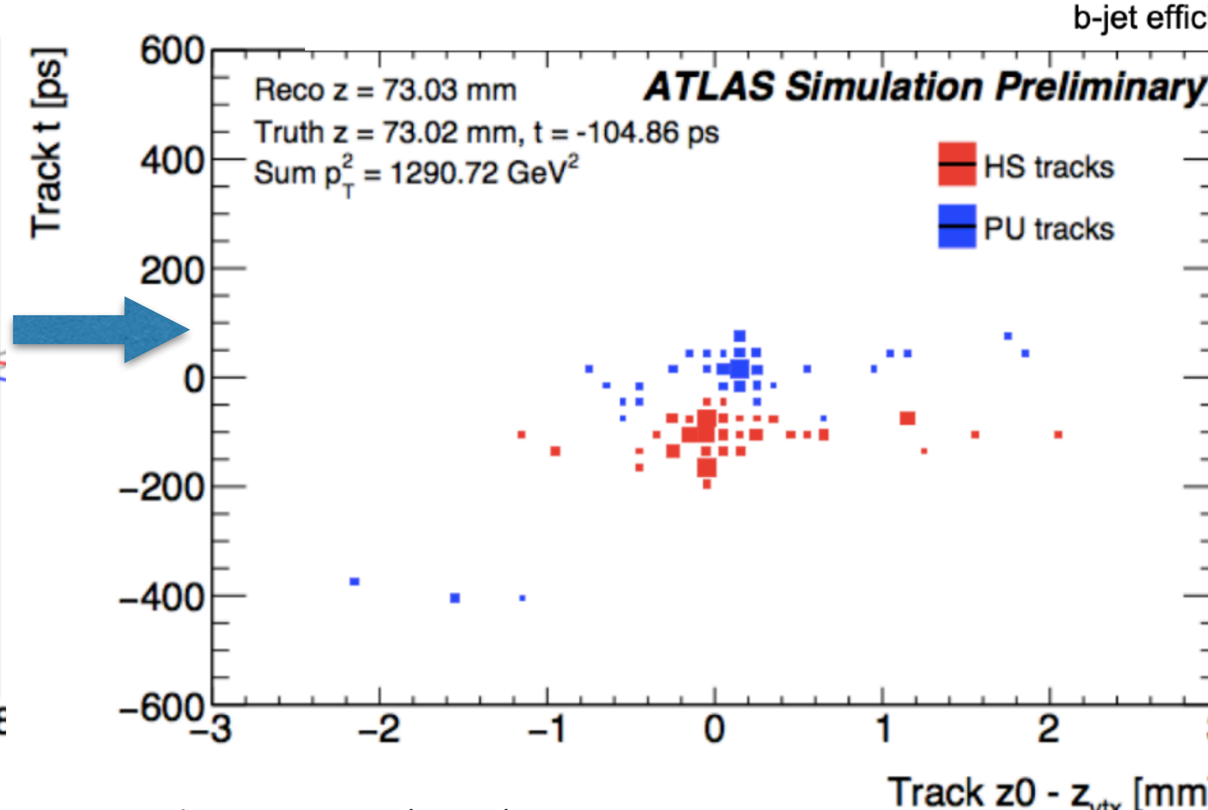
- Production of sensors and ASICs close to complete (pre-irradiation ongoing to limit TID effect on power consumption)
- Production of modules assembly started

High Granularity Timing Detector (HGTD)

- New silicon based timing detector placed between ITk and the end-cap calorimeters (|z|=3.5m)
- Provides timing resolution of O(40 ps) for tracks with $2.4 < |\eta| < 4$ (12 cm < r < 64 cm)
  - allowing better pileup rejections
  - should also provide bunch-by-bunch lump measurement down to 1% uncertainty
  - provides better physics performance, e.g. b-tagging

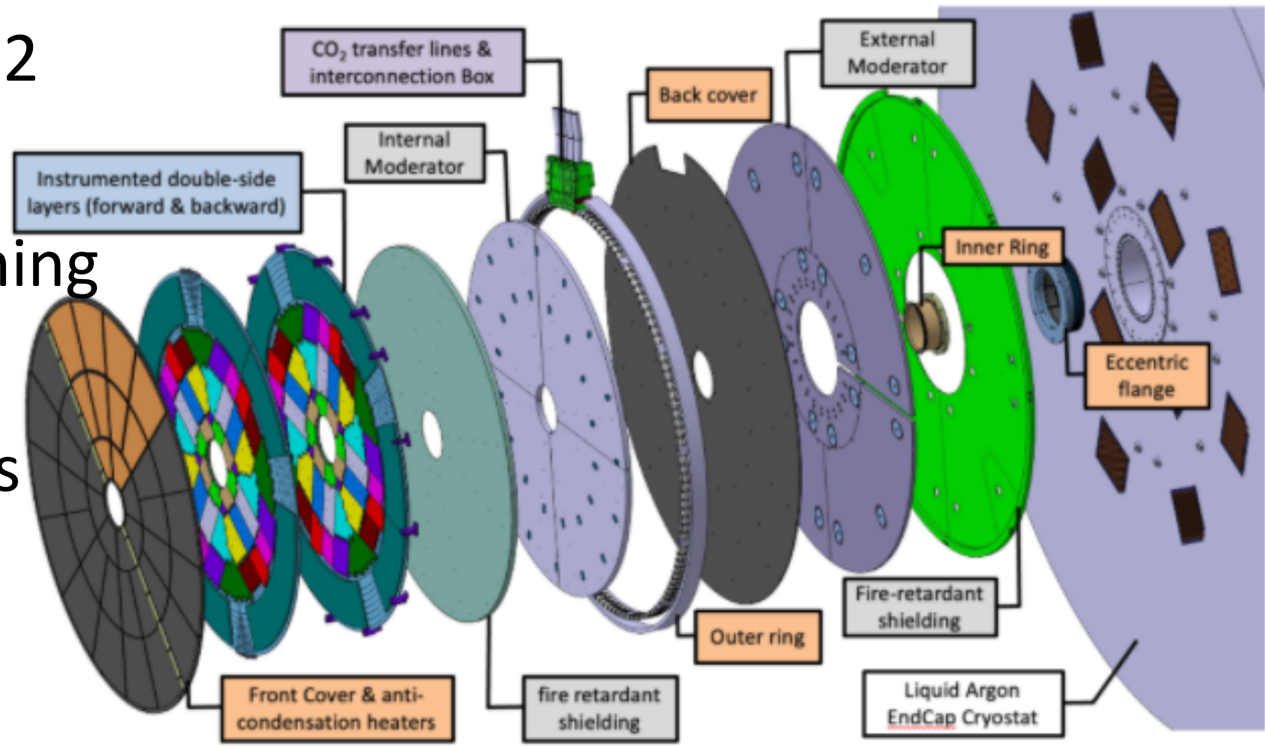




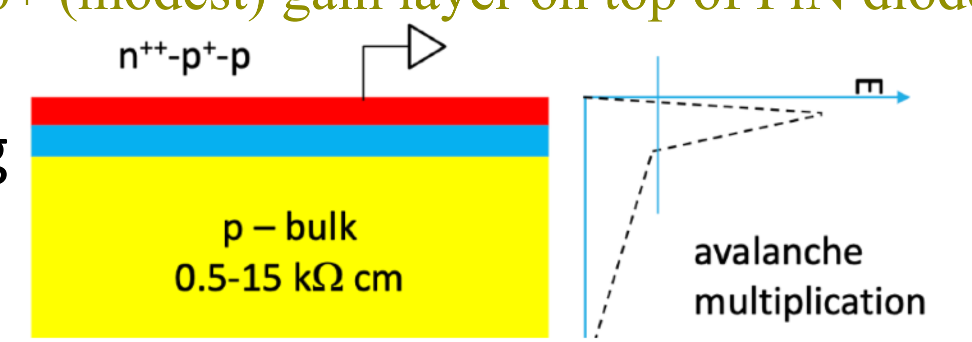


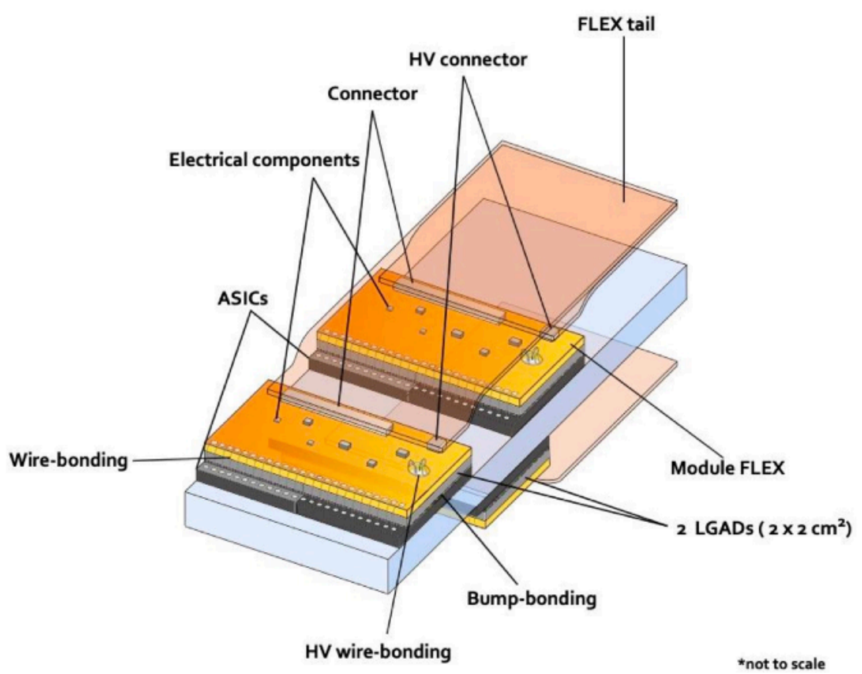
High Granularity Timing Detector (HGTD)

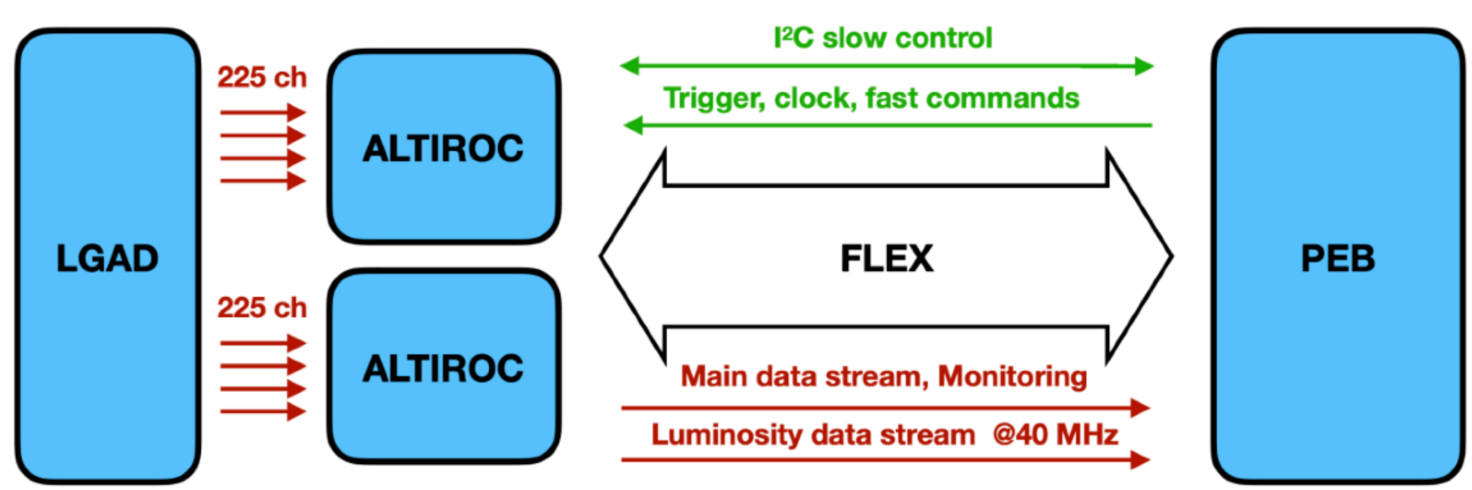
- Two double-sided disks (7.5cm thick) with 8032 modules —> 3.6M readout channels
  - High drift velocity, thin active layer, fast timing
  - 2x Low Gain Avalanche Detector LGADs bump-bonded into ASIC (ALTIROC) modules
    - High granularity: each LGAD = 15x15 pads of 1.3x1.3 mm^2
  - Connected by flex cables to Peripheral Electronics Board (DC/DC, lpGBT, VTRx)
    - strong radiation tolerance for the MUX64 ASIC
- Sensor production started, ALTIROC production starting



p+ (modest) gain layer on top of PiN diode

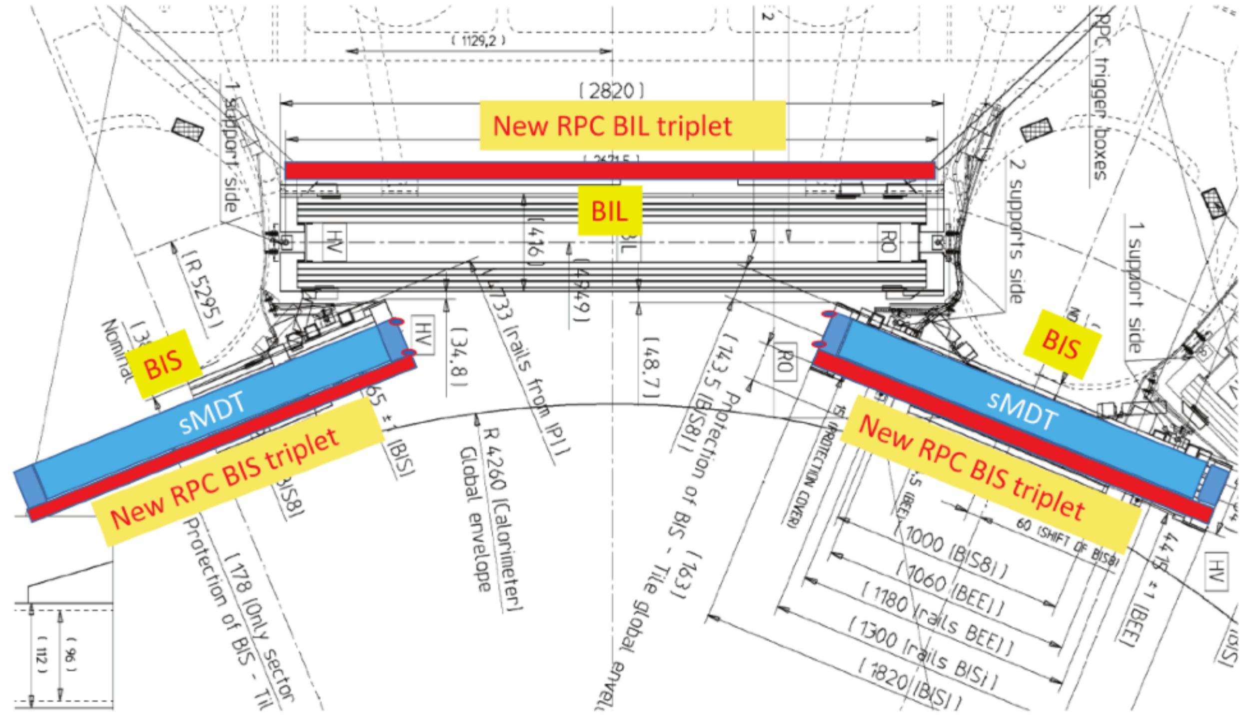






Muon spectrometer

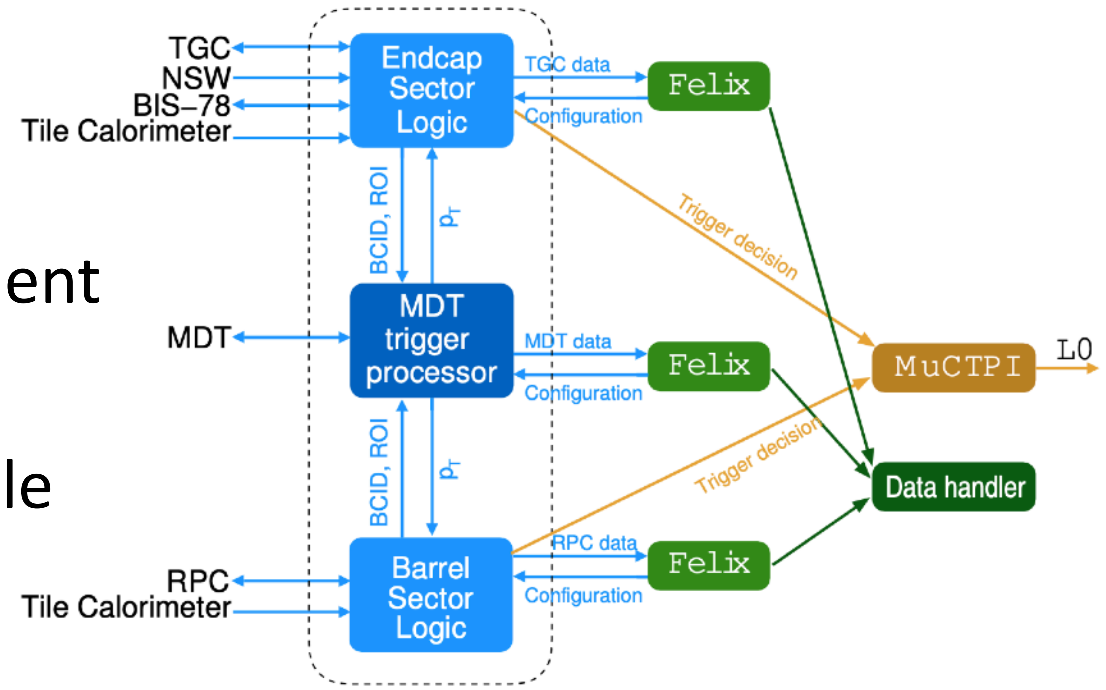
- Multiple upgrades to improve trigger efficiency
  - by increasing coverage for Barrel
  - by sending all data at 40 MHz off detector to perform trigger logic on FPGA
- In the barrel
  - Small Monitored Drift Tubes (sMDT) will replace MDTs in small sector
  - gain of space allow the insertion of additional Resistive Plate Chambers (RPC) —> chambers are produced, integration is ongoing
  - Add RPC triplet on long sectors

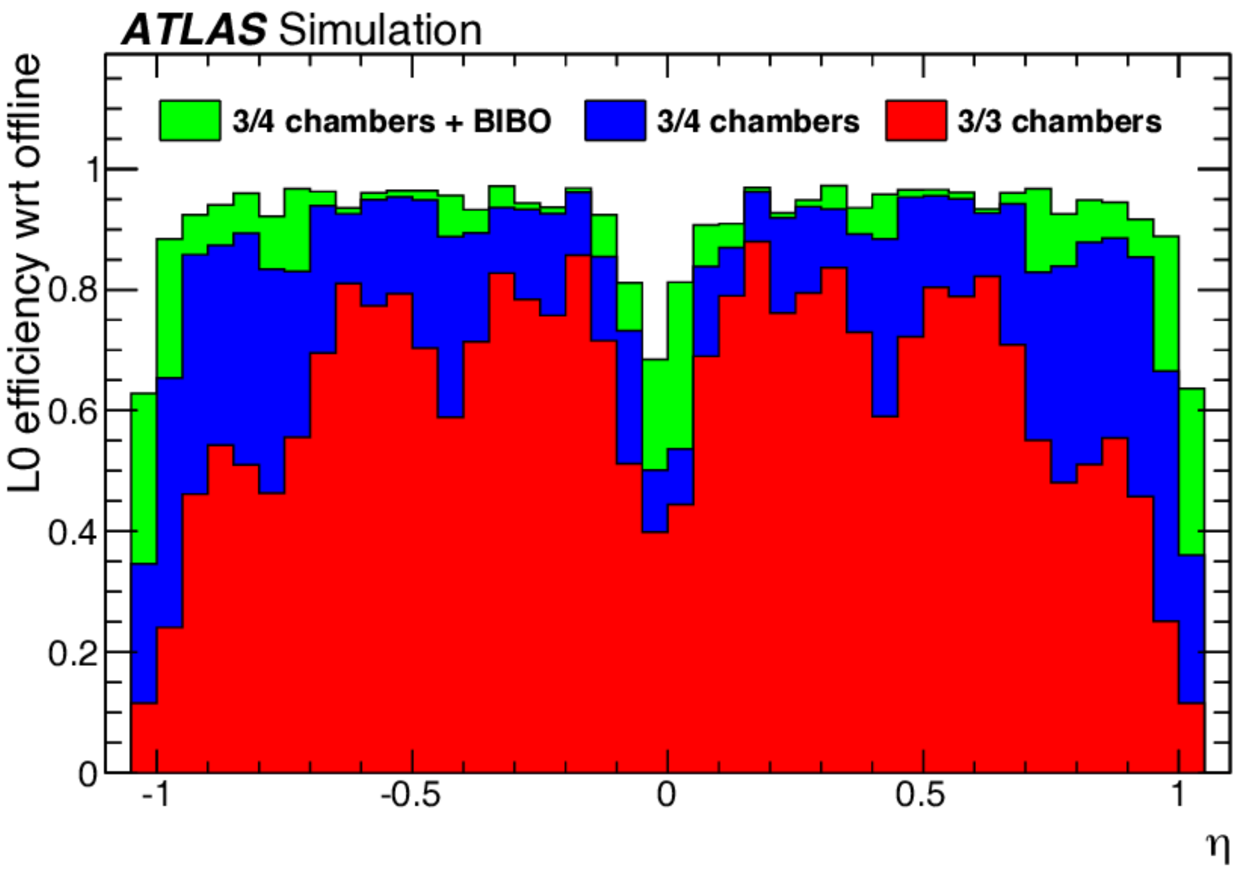


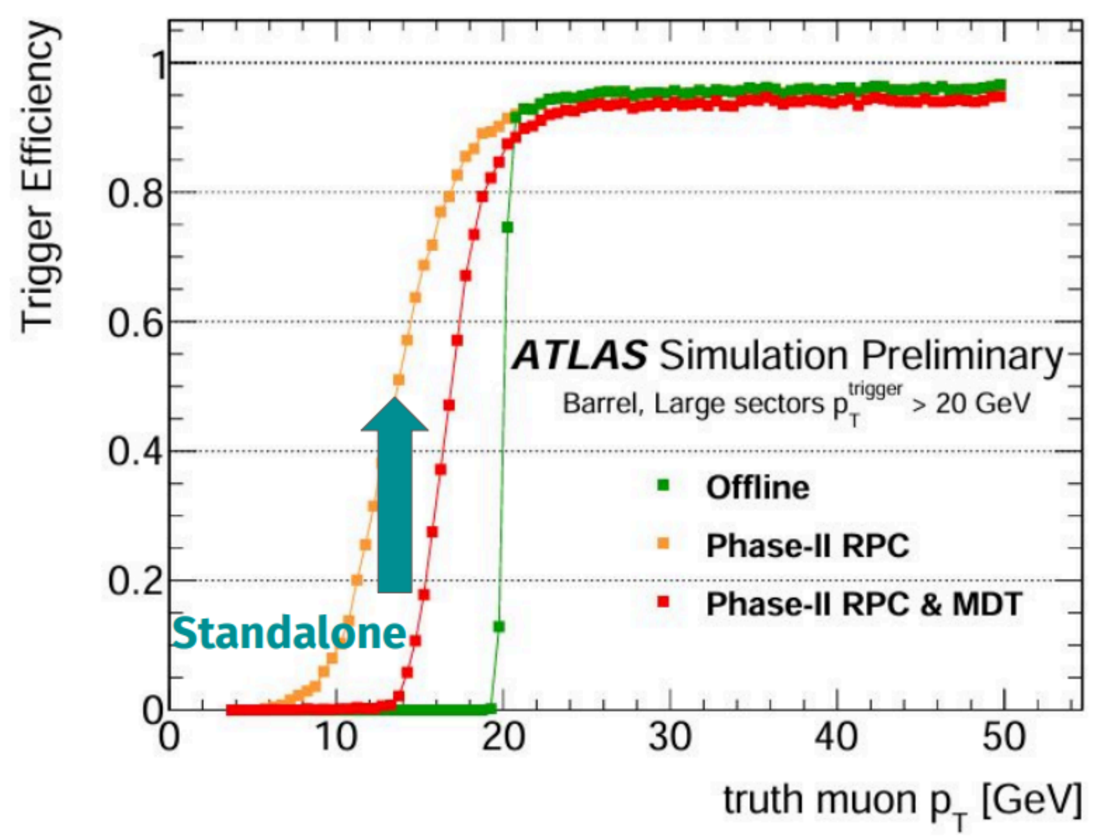
- In the end-caps
  - New Small Wheel (NSW) as part of the LS2 « Phase-1 » upgrade
  - Replace in the same end-cap Inner Layer 4 envelop doublets by triplets of TGCs —> production ongoing (pilot installed during last YETS)

Muon spectrometer

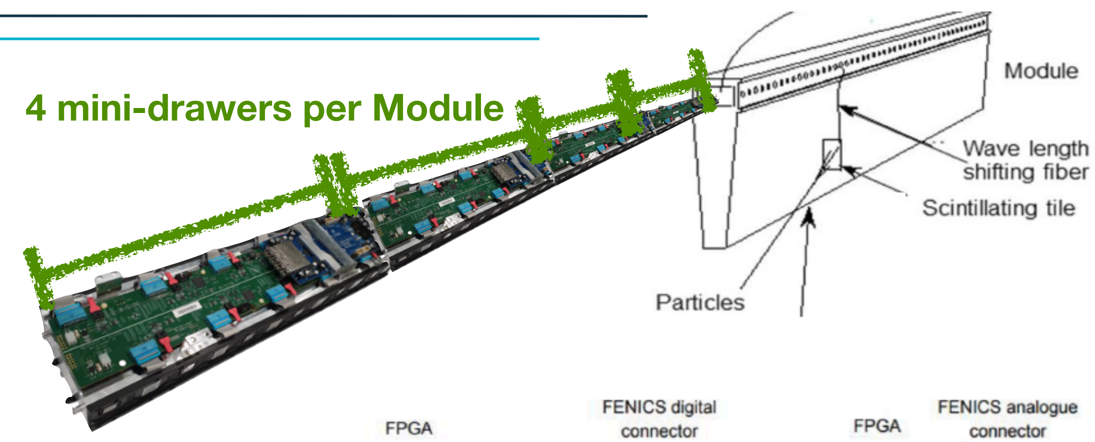
- New electronics
  - replacing both frontend and backend for TGC
  - introducing FPGA-based road finder and segment finder for MDTs
- Trigger decision using data from TGCs and RPC, Tile and MDT trigger processor collected by MuCTPi
- All muon hit data readout through FELIX and sent through the High Level Trigger and downstream readout system

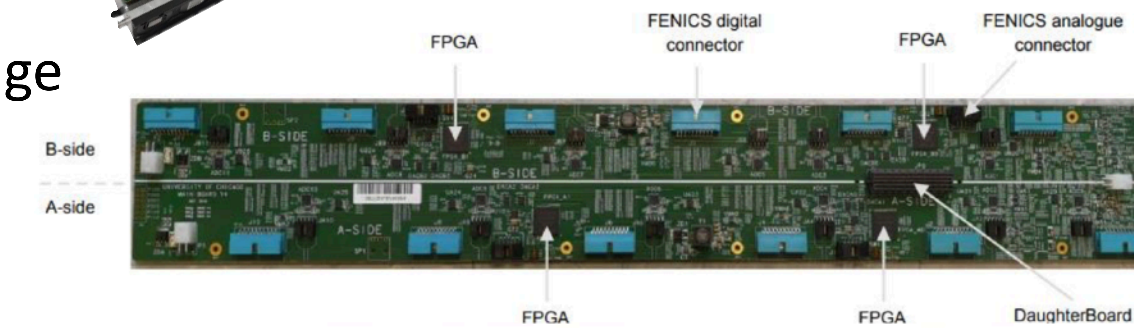


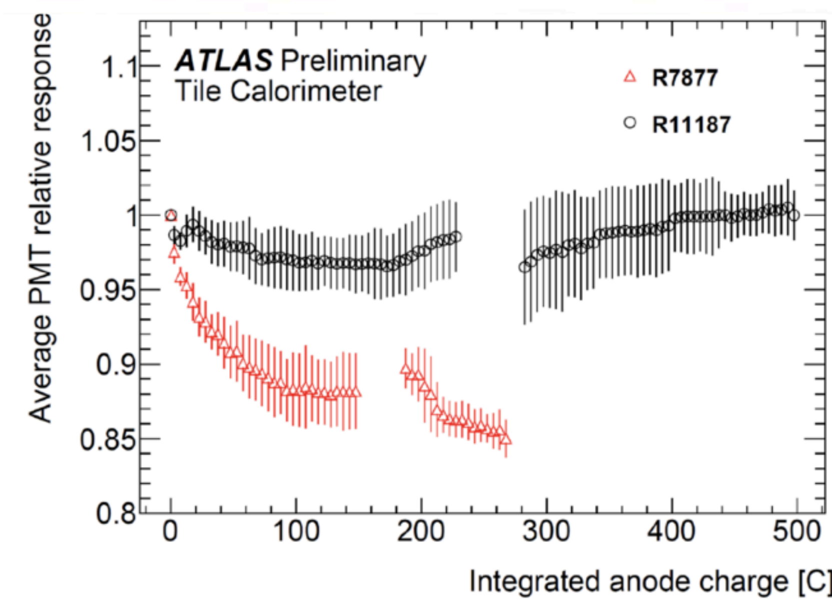




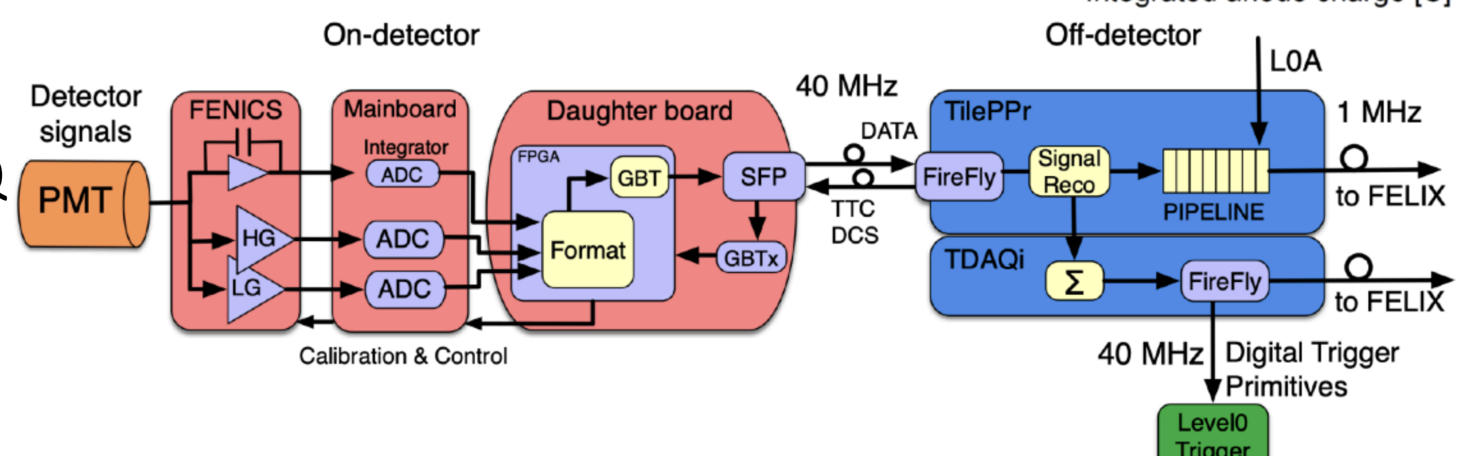
- Replacement of readout electronics to reach the full granularity at 40 MHz for the trigger
- On detector
  - New structure (Mini-Drawers) to ease maintenance
  - ~10% of PMTs will be replaced to avoid radiation damage and aging reducing the light yield and the uniformity
  - FENICs shape and amplify PMT signals (x2 gains)
    —> production ongoing
  - Main Boards digitize signal using 12b ADCs and control FENICs
    —> production done
  - Daughter Boards: serialise digital data and send them off-detector with 2 Kintex Ultrascale FPGAs / board
    —> Production soon to start





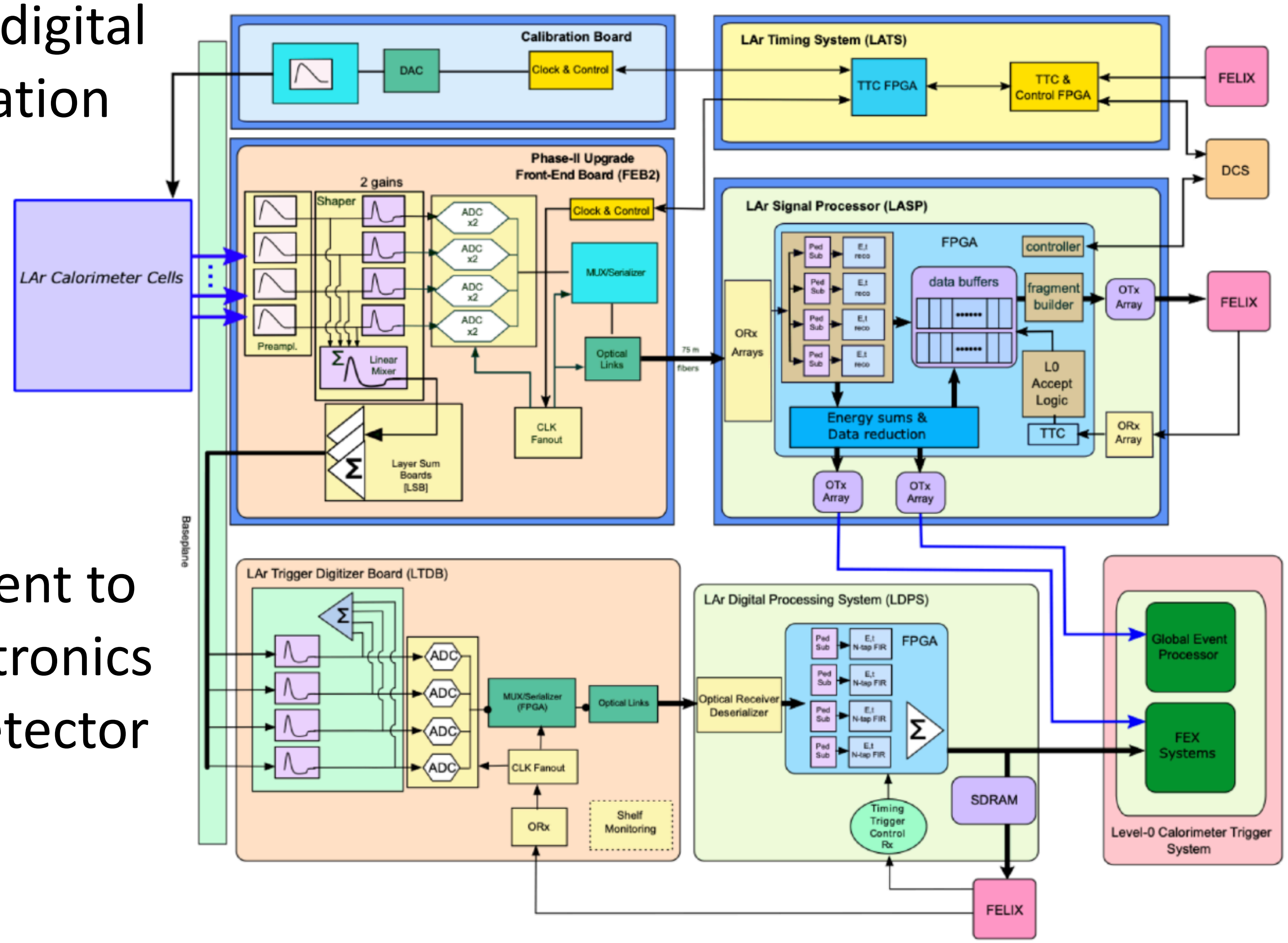


- Off detector
  - Pre-processor (PPr) compute energy deposits, provide data to Trigger and DAQ
  - TDAQi to sum up energies and send to L0
    —> Pre-production under tests

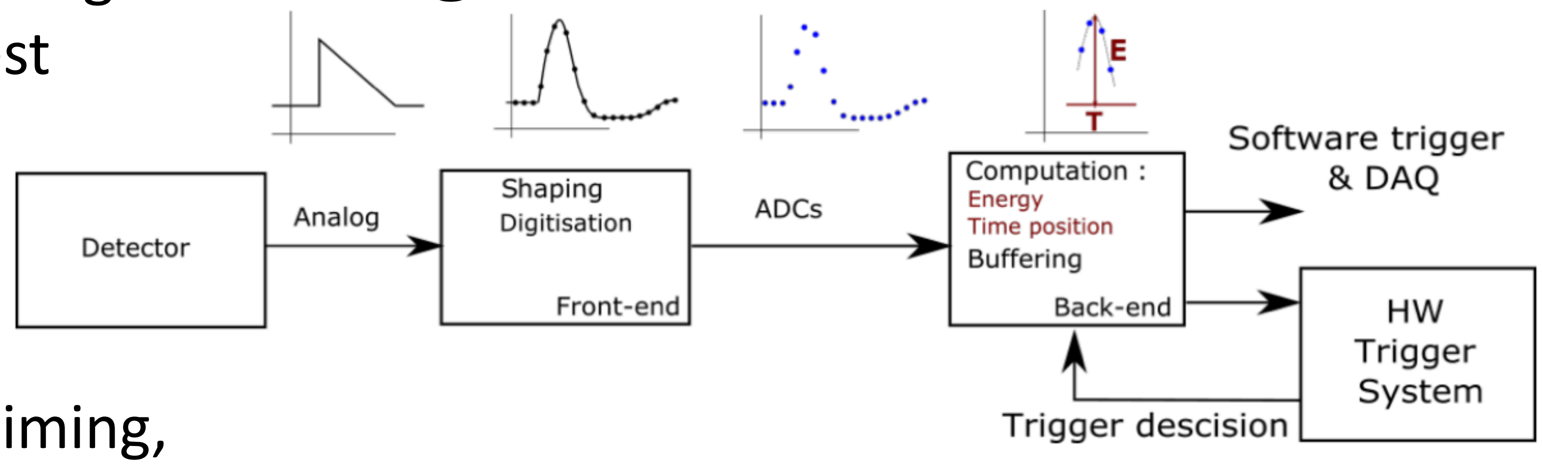


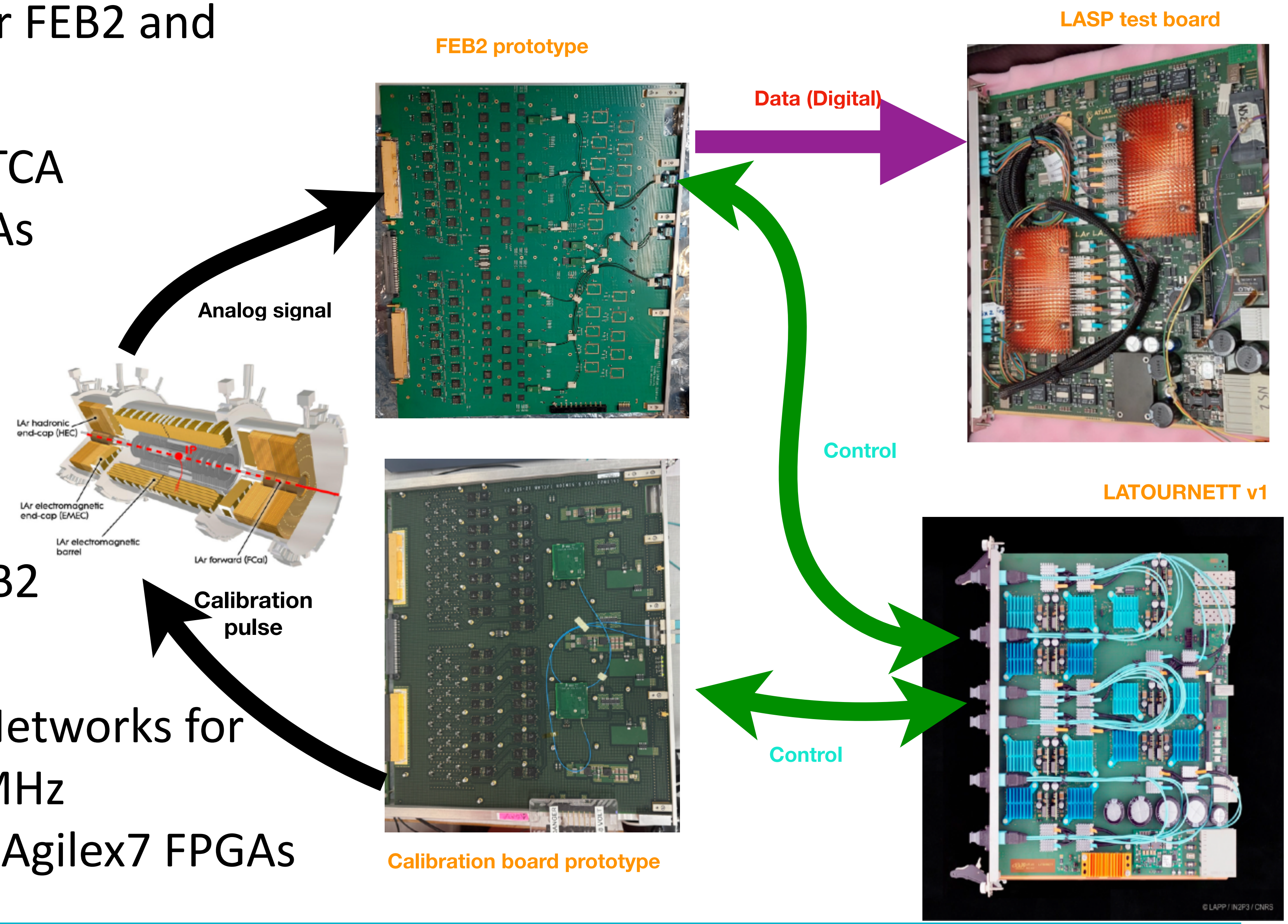
Liquid Argon calorimeter

- Detector itself remains unchanged (inside the cryostat)
- ~All the electronics will have been changed by the time we reach the HL-LHC
  - current frontend electronics digitize the signal of each detector cell at 100kHz max (sampling every collider bunch-crossing = 25 ns)
  - wish to reach 1MHz L0 accept rate for the higher luminosity runs
- Triggering system already became digital during last long shut-down (installation of LTDB and LDPB boards)
  - will be updated in order to be able to trigger with individual cell granularity (instead of supercells summing 4-6 cells)
- Long Shutdown 3 will be the moment to change the other parts of the electronics chain, both on-detector and off-detector boards and connectivity



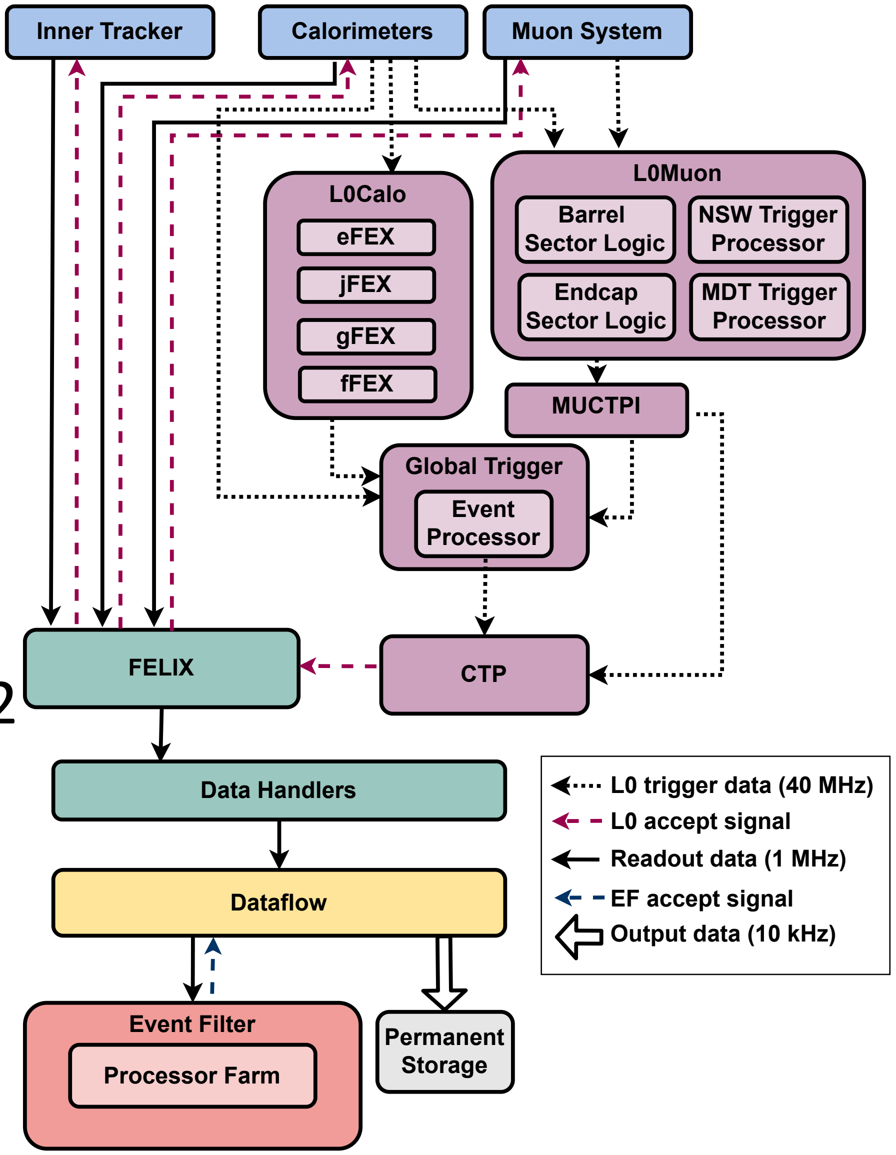
- 1524 Front-End boards (FEB2) digitise single-cell data @40 MHz
—> Design is almost finished (noise test needed in fully loaded crate)
- 122 calibration boards for pulsing
—> Board design almost done
- New timing system (LATS) to provide timing, trigger signals, and slow-control for FEB2 and calibration boards
  - 30 LATOURNETT high-fanout ATCA boards with 13 Cyclone10 FPGAs
  —> Test of 2nd (final?) prototype
- 278 LAr Signal processor (LASP)
  - 2xFPGAs boards to process the digitised ADCs coming from FEB2 into energy
  - Investigation on using Neural-Networks for energies in high PU env. @40 MHz
  —> redesign of the board with Agilex7 FPGAs

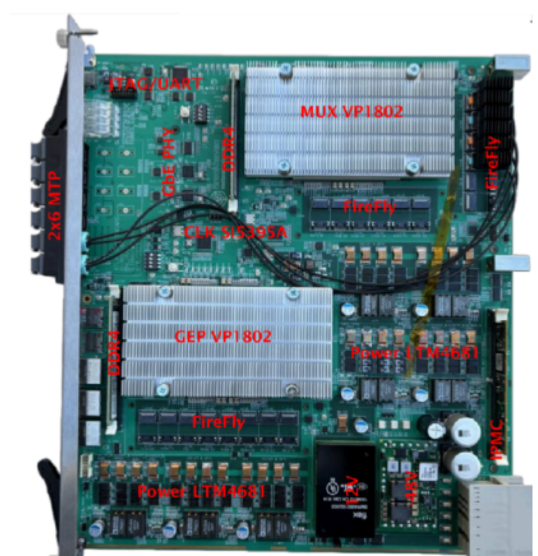




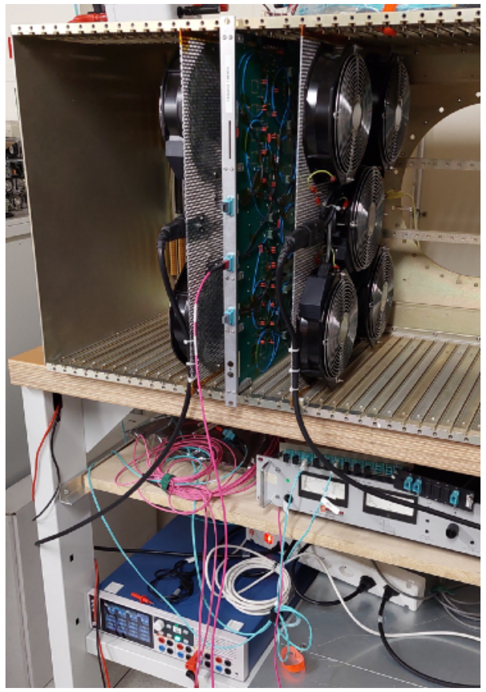
« Central » Trigger & Data Acquisition (TDAQ)

- Goal = to increase trigger rate but keep energy thresholds
  - Level-0 (L0) trigger reduce data from 40 MHz to 1MHz (x10 more w.r.t Run3)
  - Expected event size ~4.5 MB (x4 w.r.t Run3)
  - Event filter reduces data from 1MHz down to 10kHz (x 5 w.r.t Run3)
- Upgrade of the hardware trigger (L0) system :
  - « Global Trigger » aggregates event data into FPGA VP1802
  - receives trigger objects from Phase-1 electronics (FEXes + MuCTPI) with full calorimeters granularity
  - object level & event level (approx. 50 Tb/s) reconstruction
  - new timing distribution system (LTI)
- Upgrade of data acquisition
  - New readout card (FELIX) with higher bandwidth and processing capabilities
- Event Filter farm upgrade
  —> technology evaluation (FPGA/CPU/GPU) to be finalised in Q4 2025

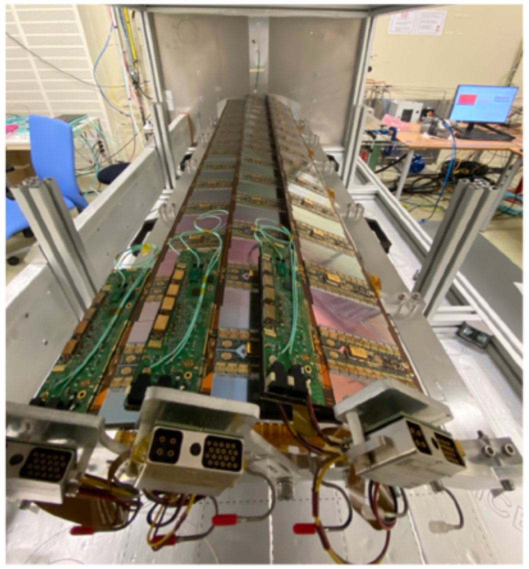




- With prototypes and/or pre-production of the different parts of the Phase-II upgraded ATLAS detector, much effort on all fronts to build « system tests » in order to integrate all new components in the full picture
  - Ongoing tests between TDAQ/DCS/Infrastructure and systems



FEB2 prototype in Front End crate

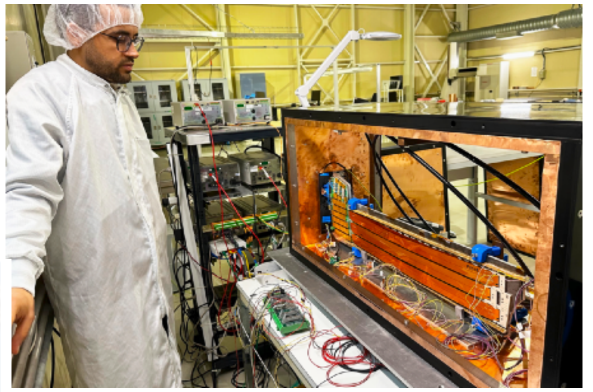


Assembly of 3 ITk strips staves

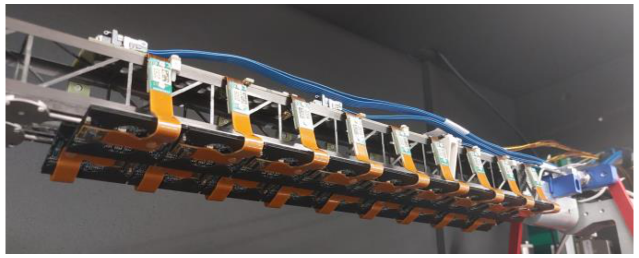
TDAQ Event Filtering Slice

Thermal tests of Tile PPr

HGTD prototype



Muon sMDT integration

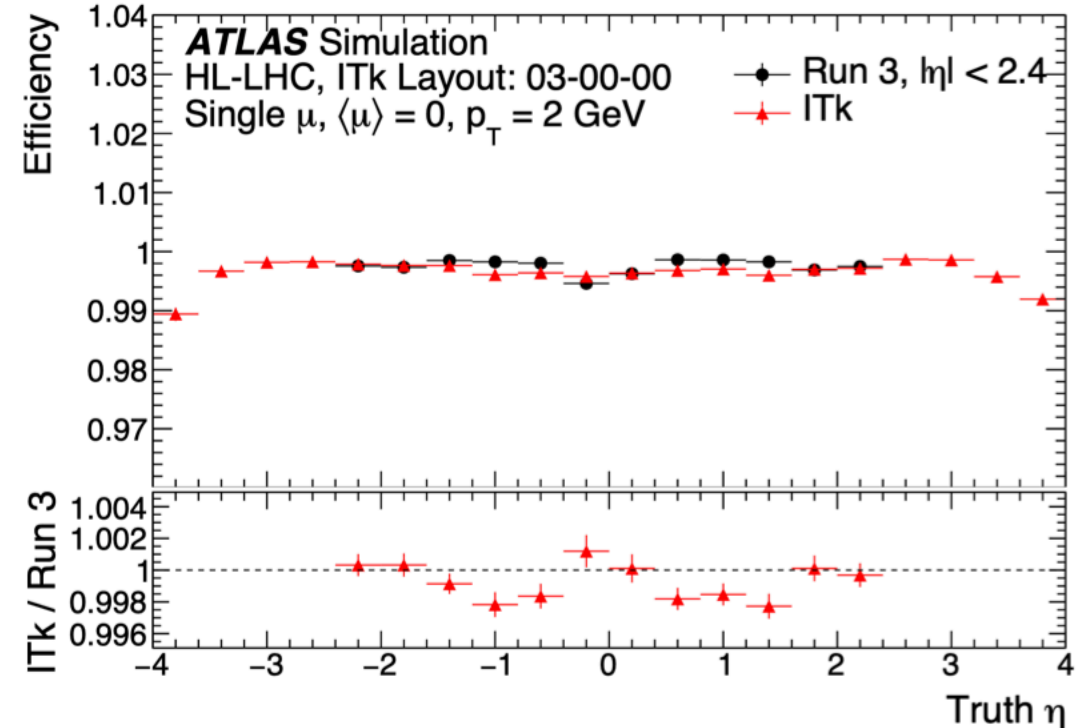


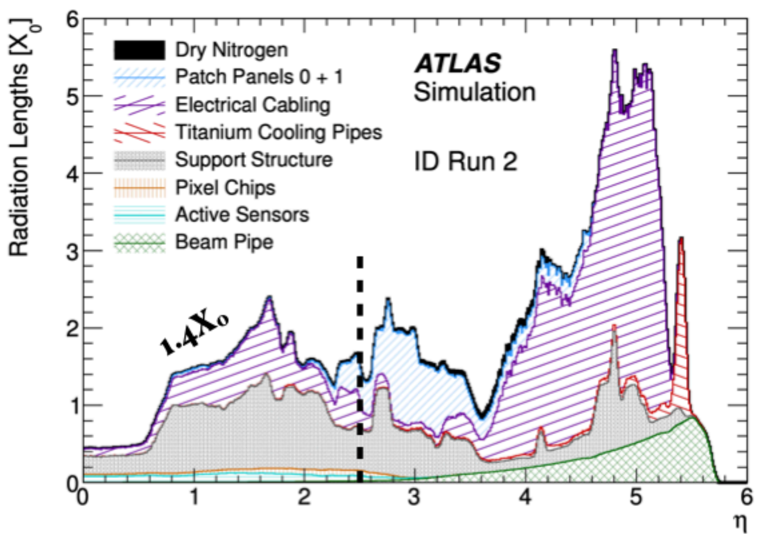
ITK pixel pre-production loaded longeron

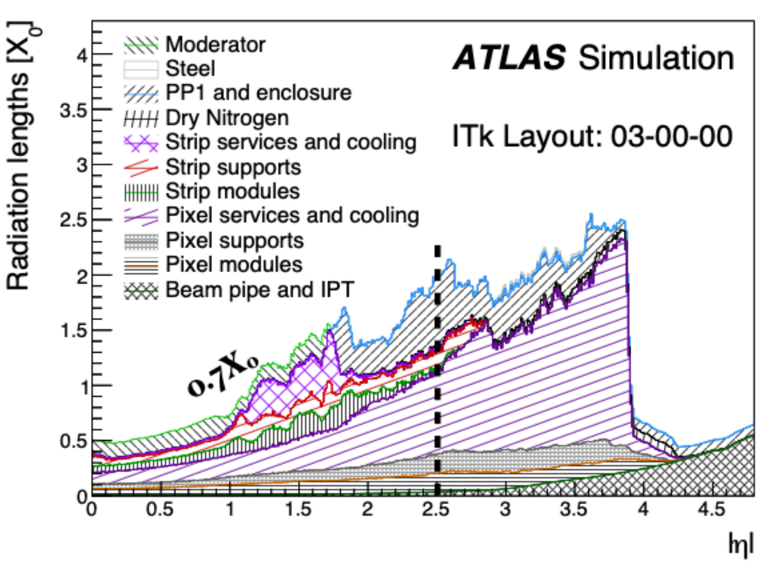
Integration between HGTD and new timing system (LTI) board

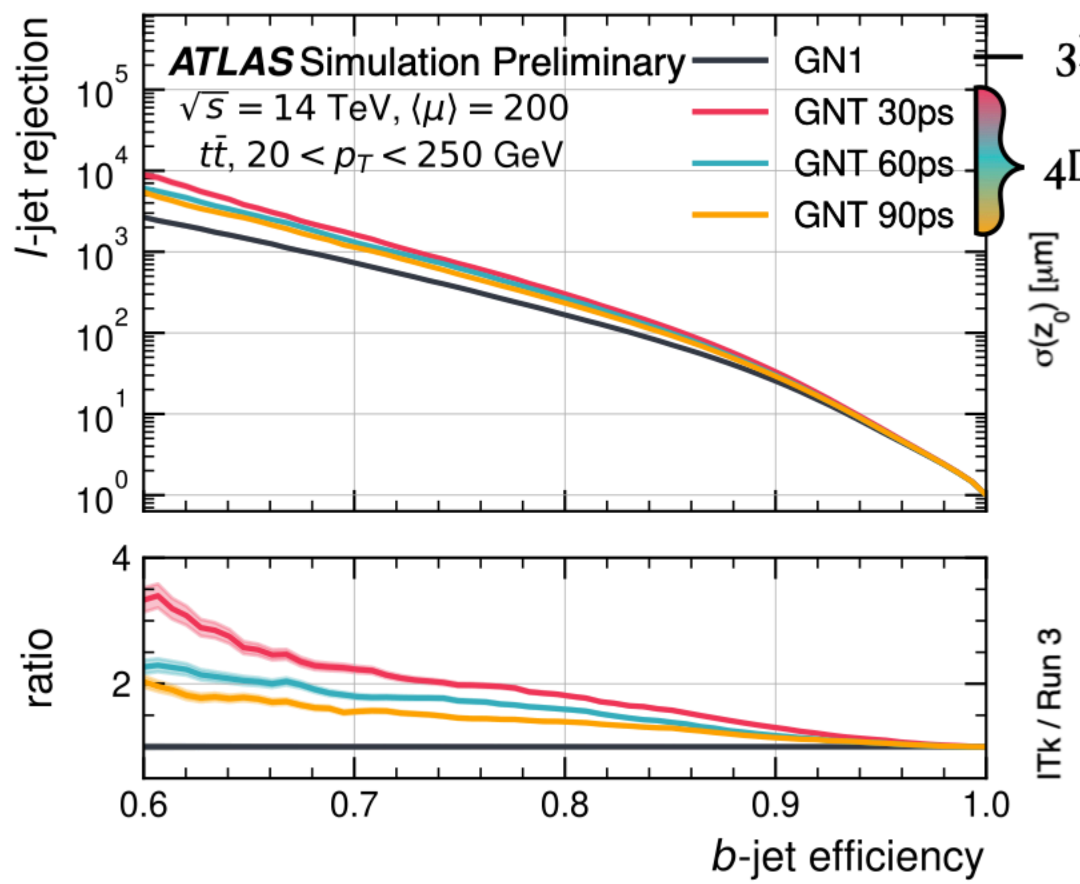
- Also time to test cooling, powering, insertion tools,…
- Entering the difficult times consisting in scheduling the person-power for the installation

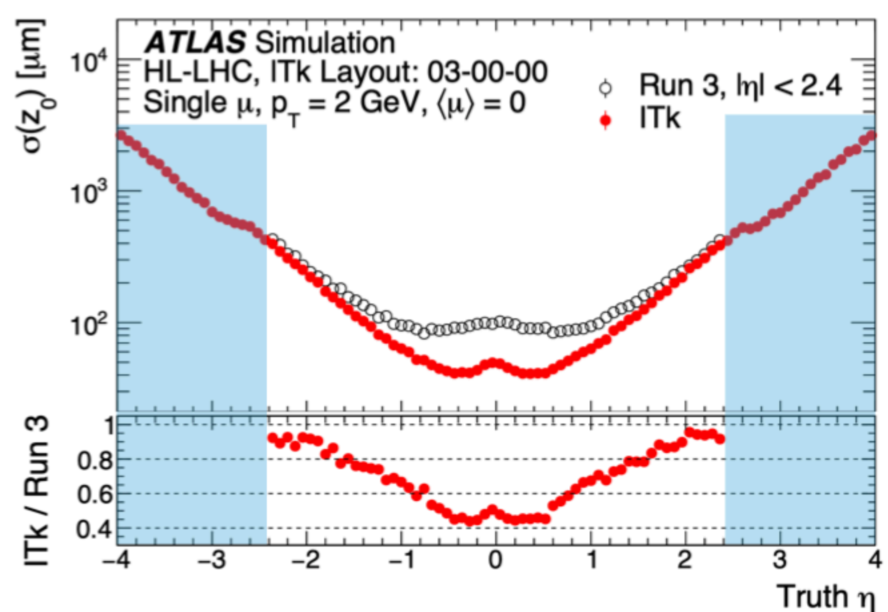
- The upgraded ATLAS will have
  - larger coverage
  - better granularity (online & offline)
  - different material budget
  - new precise timing information





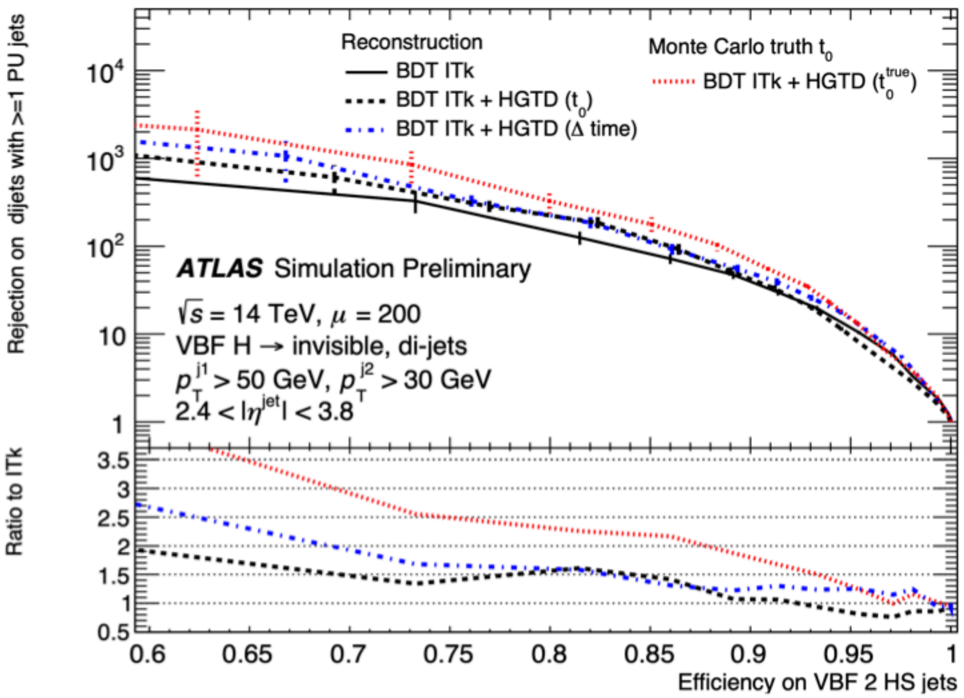




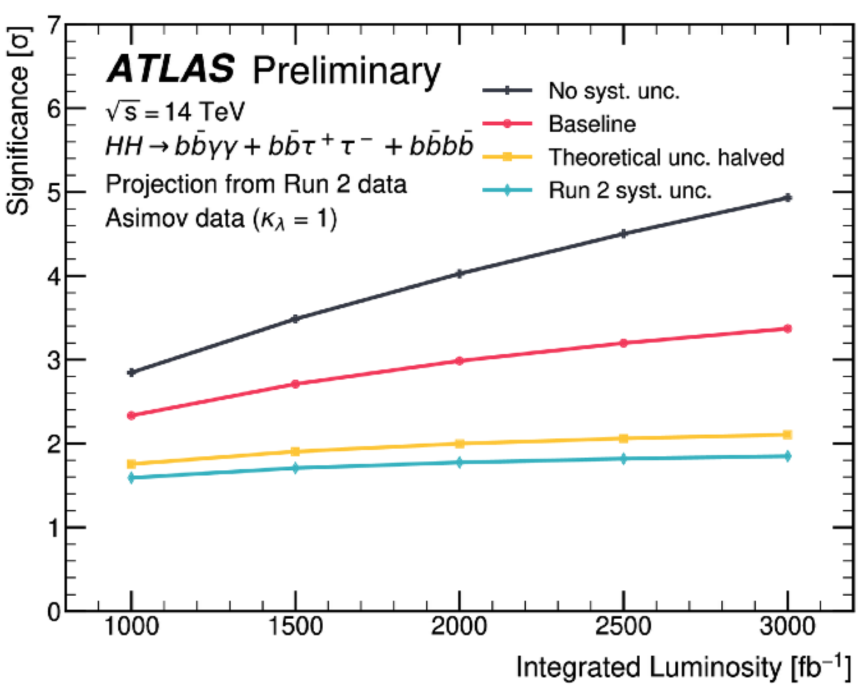


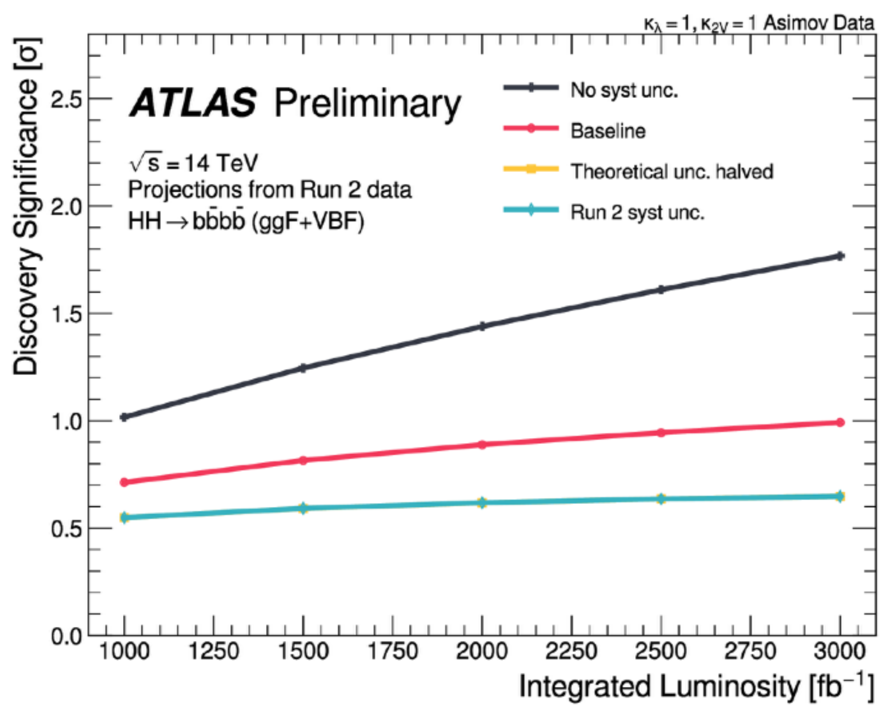
What for ? which physics at the end ?

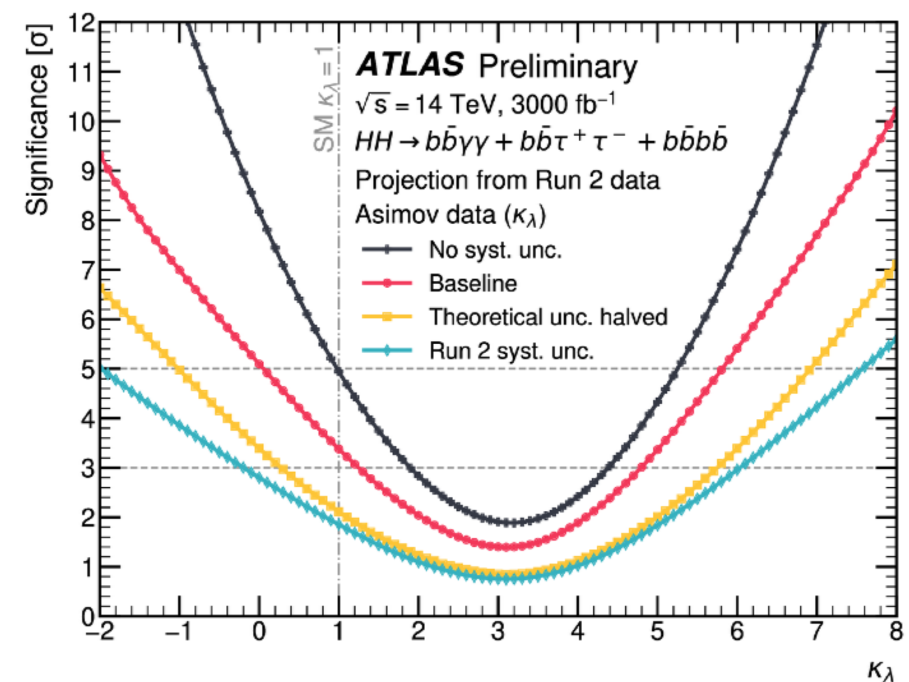
- Clear impact of the « objects » performance on existing analyses
- Better performance helps the statistics-limited analyses (e.g. di-Higgs studies)



- ATLAS Phase-II upgrades not only allow for recording data with high-luminosity LHC but even improve the instrumental performance !
- Still working on getting always better out of the CERN hadrons collisions







- Whatever is in the data, the HL-LHC and its upgraded detectors will provide insights on our new play-ground: the scalar Higgs-boson sector
- We'll learn about it and potentially about much more (scalar field shape, meta-stability of the Universe,…)
- The legacy of HL-LHC will be enormous and very complementary to the future precision machine: the FCC at CERN !