CMS pixel detector operations in LHC Run 3

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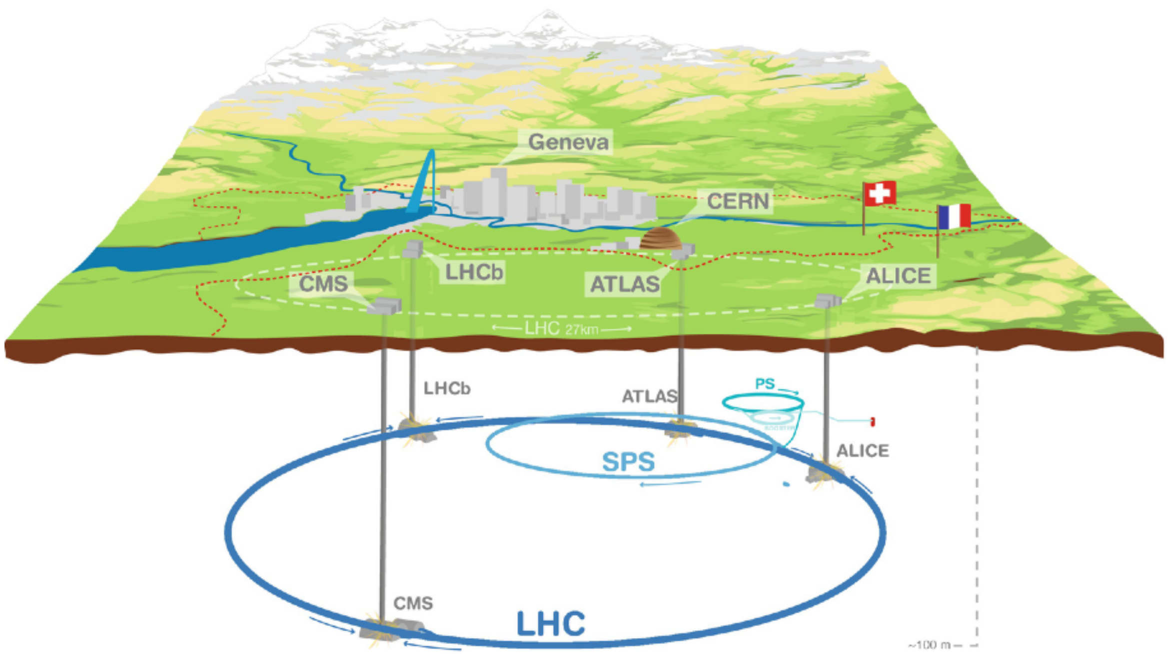
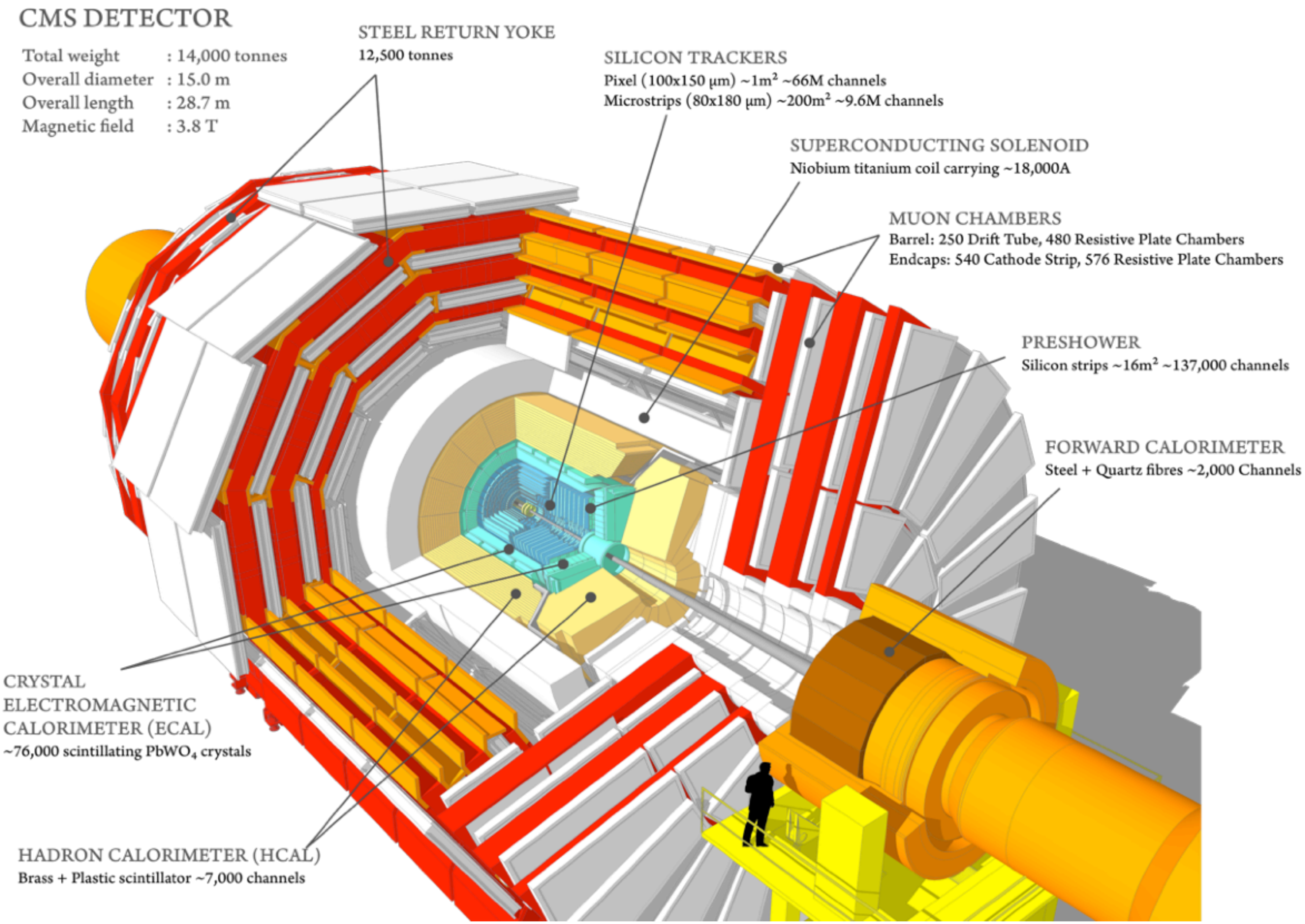
Large Hadron Collider



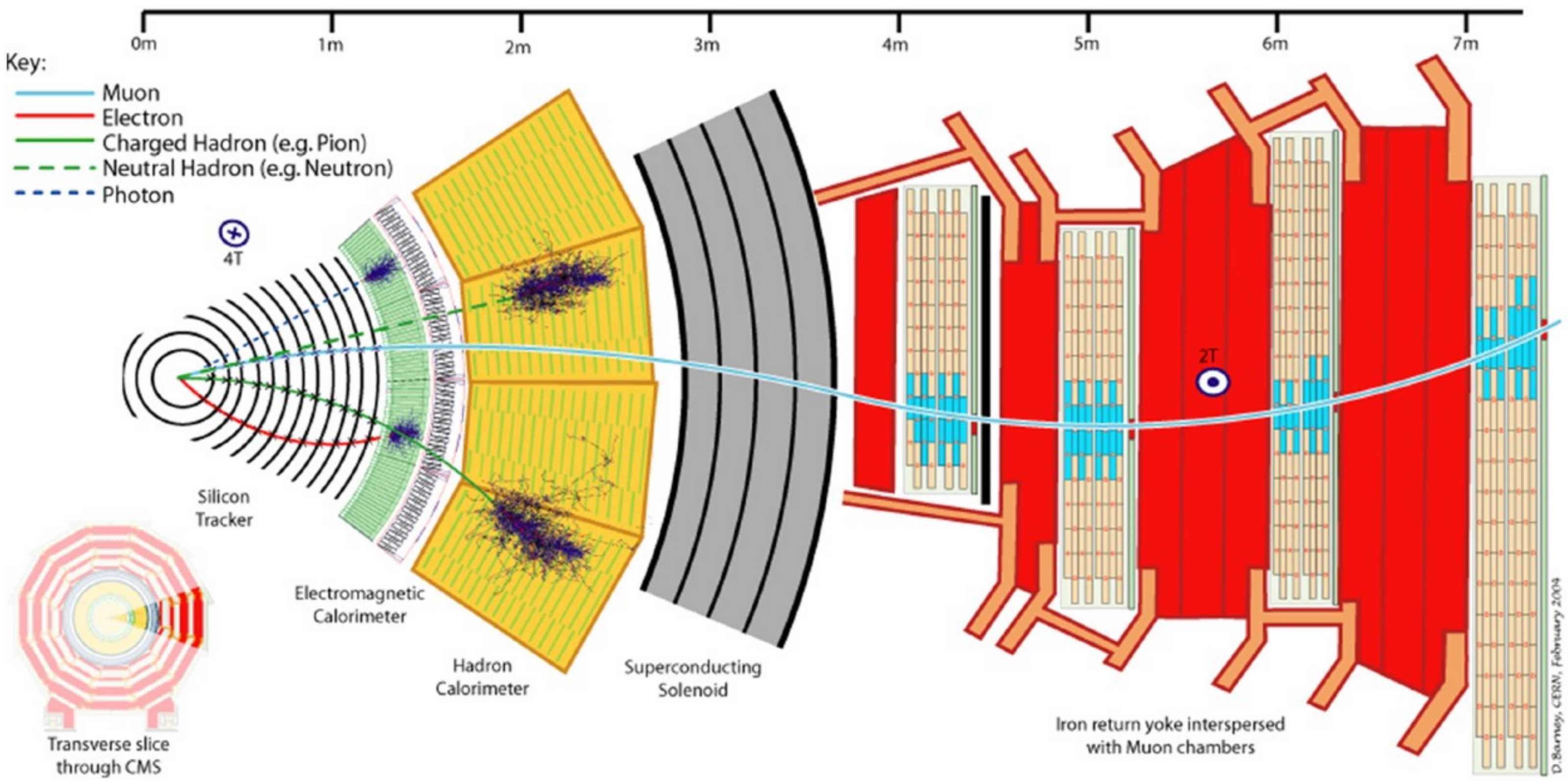
- Large Hadron Collider accelerates two beams of protons and collides them at four points around the ring with $\sqrt{s}$ = 13.6 TeV

- Compact Muon Solenoid is one of the large general purpose detectors

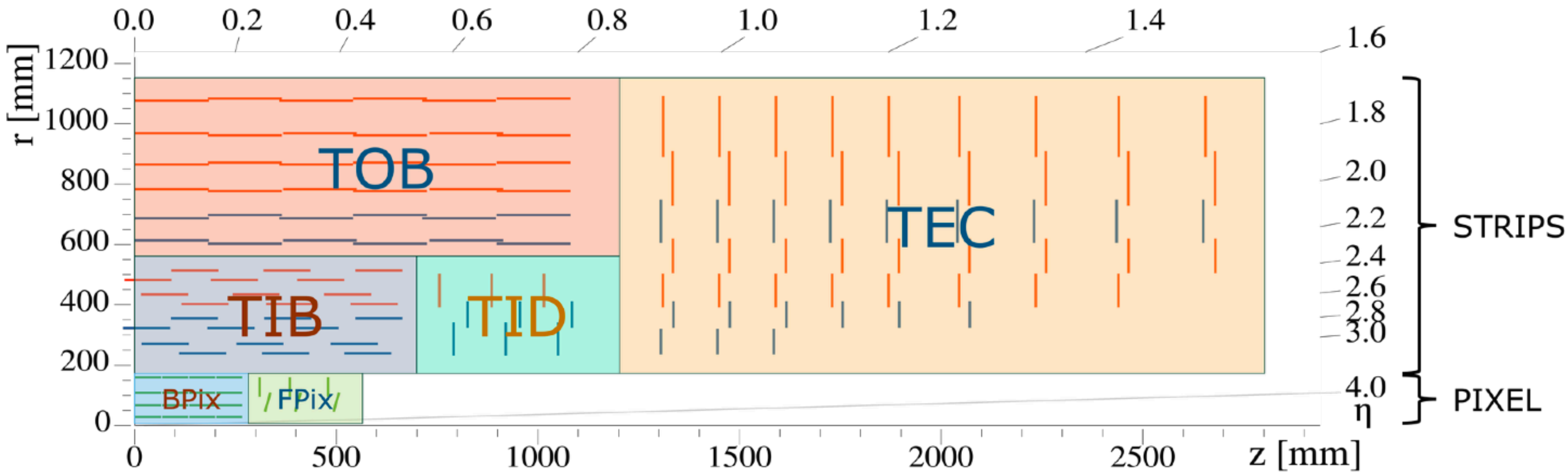
The CMS experiment



A particle's journey through CMS



Tracking detectors of CMS



Pixel tracker

➡ Barrel Pixels and Forward Pixels

Strip tracker

➡ Tracker Inner Barrel, Tracker Inner Disk, Tracker Outer Barrel, Tracker Endcap

Pixel detector

Barrel pixels (BPix)

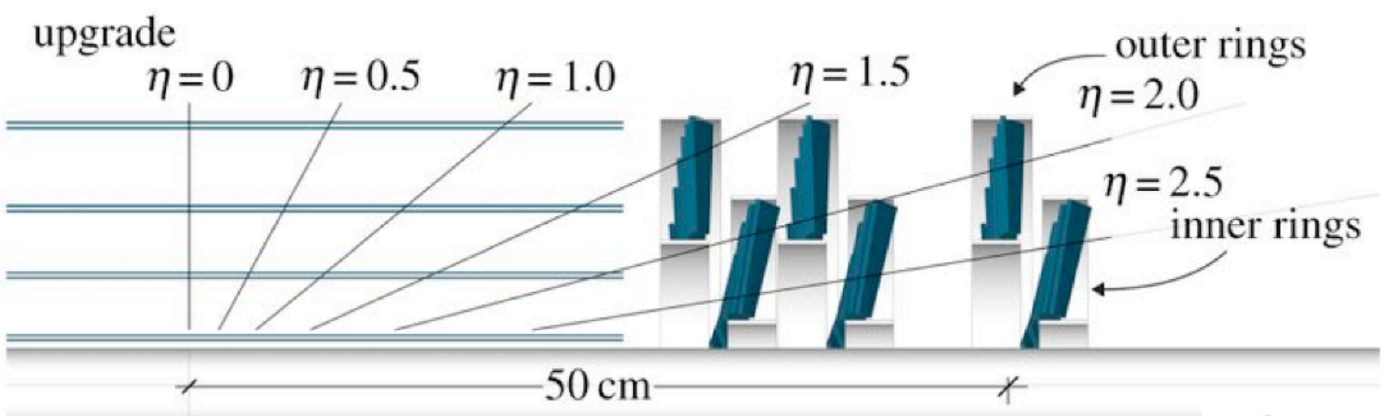
- 4 layers
- 1184 total modules

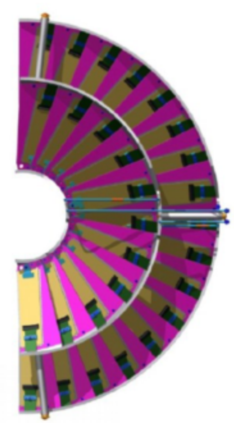
Forward pixels (FPix)

- 3 disks * 2 rings on each end
- 672 total modules

Layer 4
r = 160mm

Layer1
r = 29mm

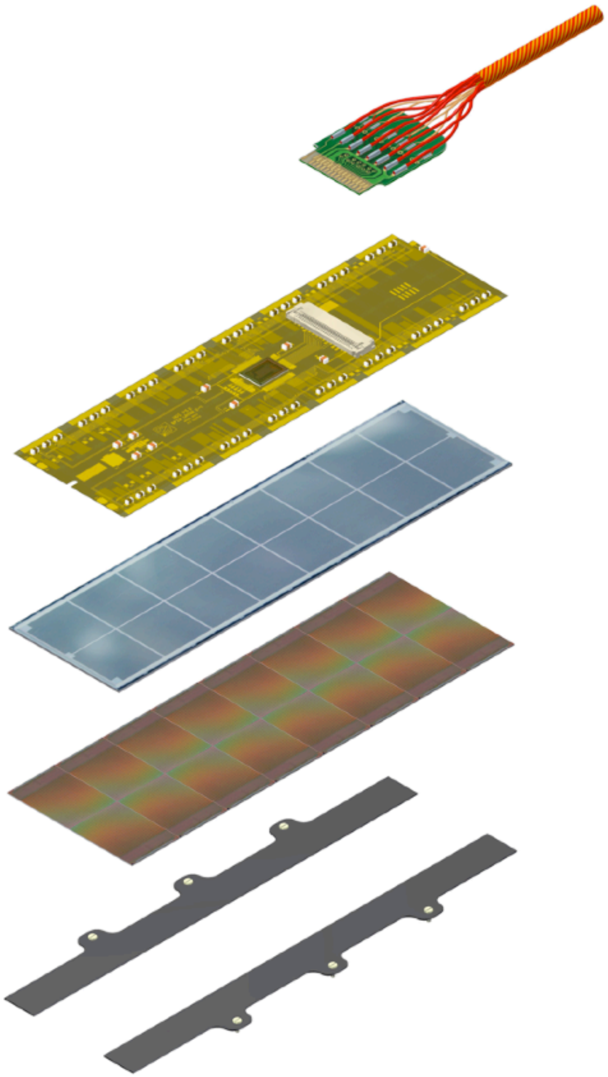




Ring 1

Ring 2

Module design



Signal and power cables

Token bit manager (TBM) chip

- Receives clock, level 1 trigger accept, configuration data
- Orchestrates readout
- 2 TBM/module in layer 1

Silicon sensor

- (150x100) μm^2
- 280 μm n-in-n

Read out chips

PSI46dig

- Digital readout
- Double column drain
- > 90% efficiency up to 200MHz/cm^2 hit rate

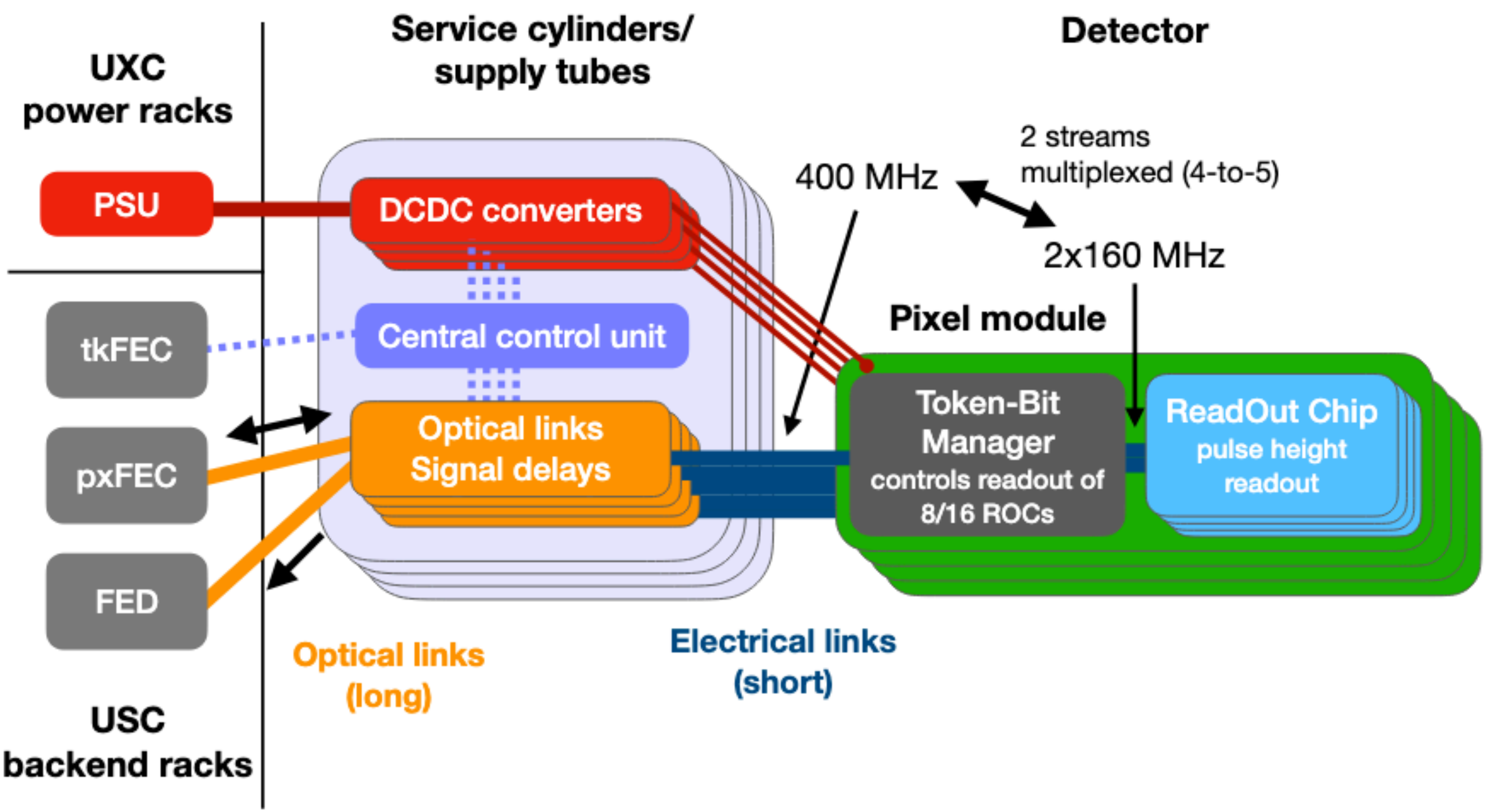
PROC600

- Specialized for layer 1
- > 90% efficiency up to 600MHz/cm^2 hit rate

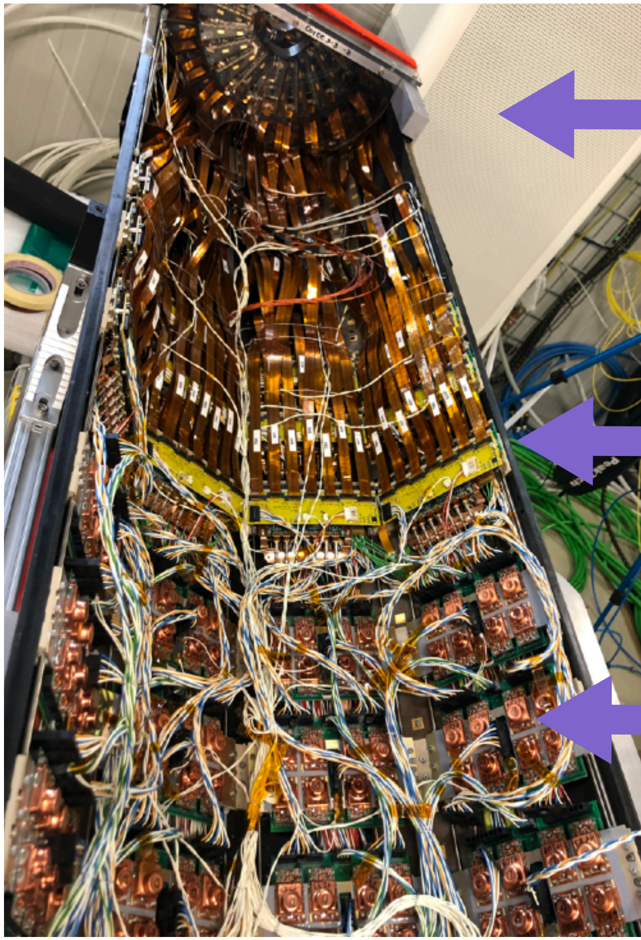
Base strip

Signal path

FEC = Front-end Controller
FED = Front-end Driver
USC = Underground Service Cavern
UXC = Underground Experimental Cavern



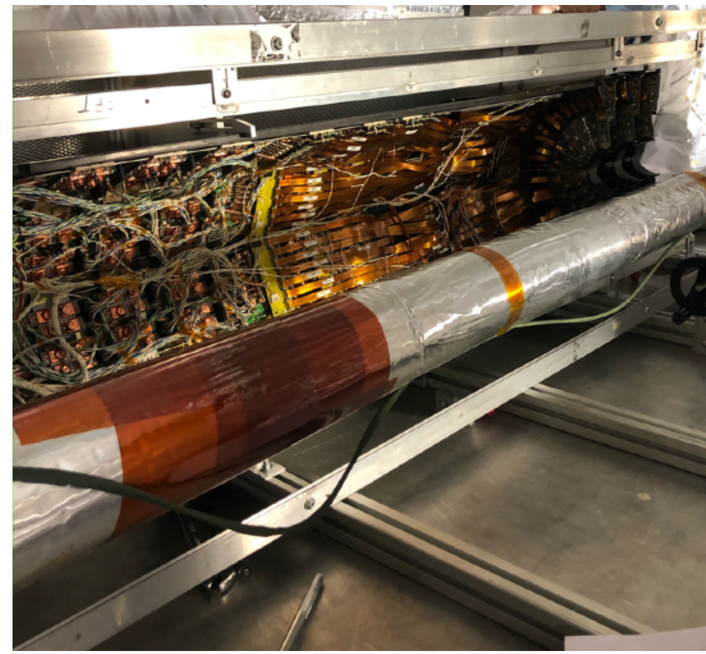
Detector with service cylinder



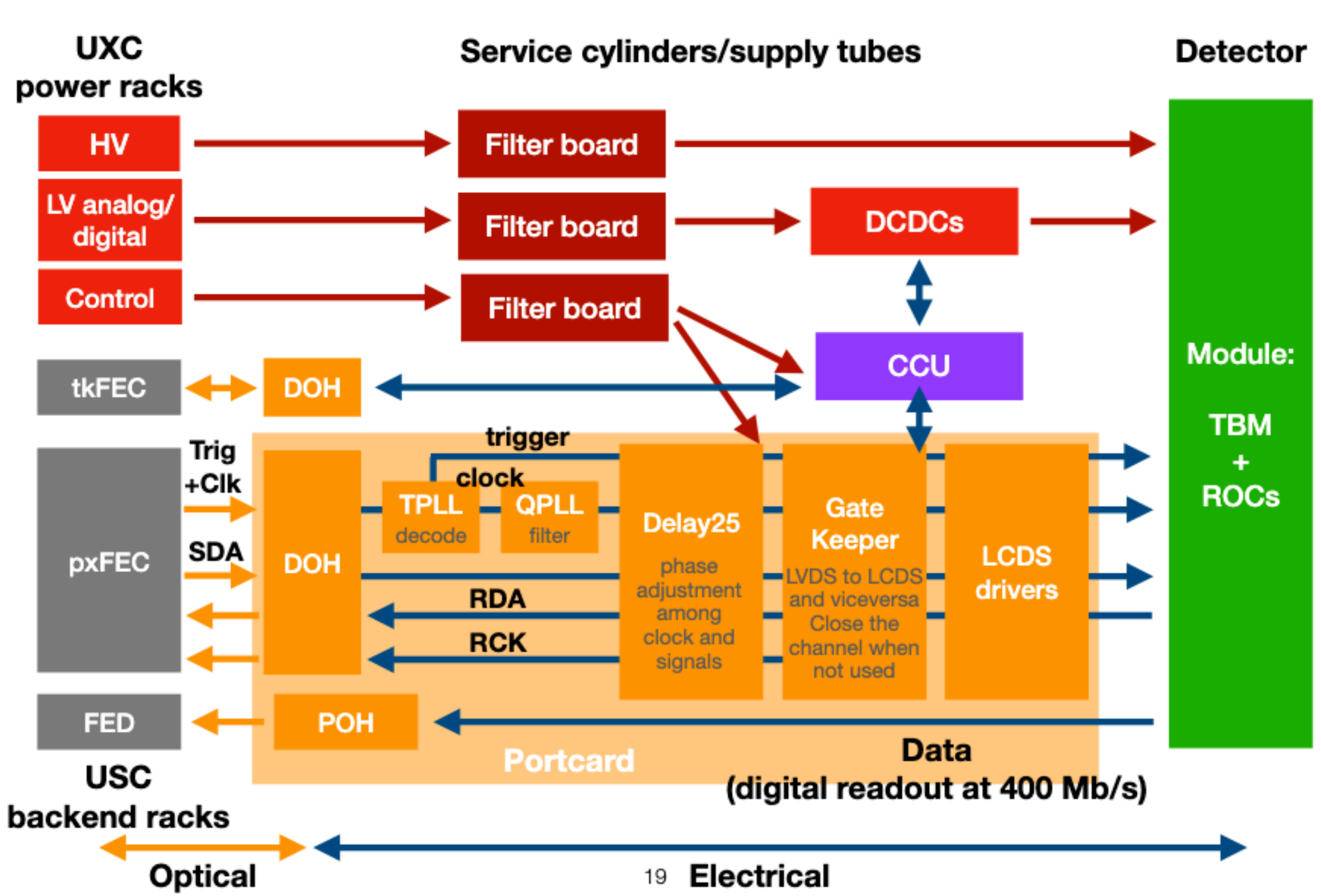
Modules

Portcards/
electronics with
delay chips

DCDC
converters

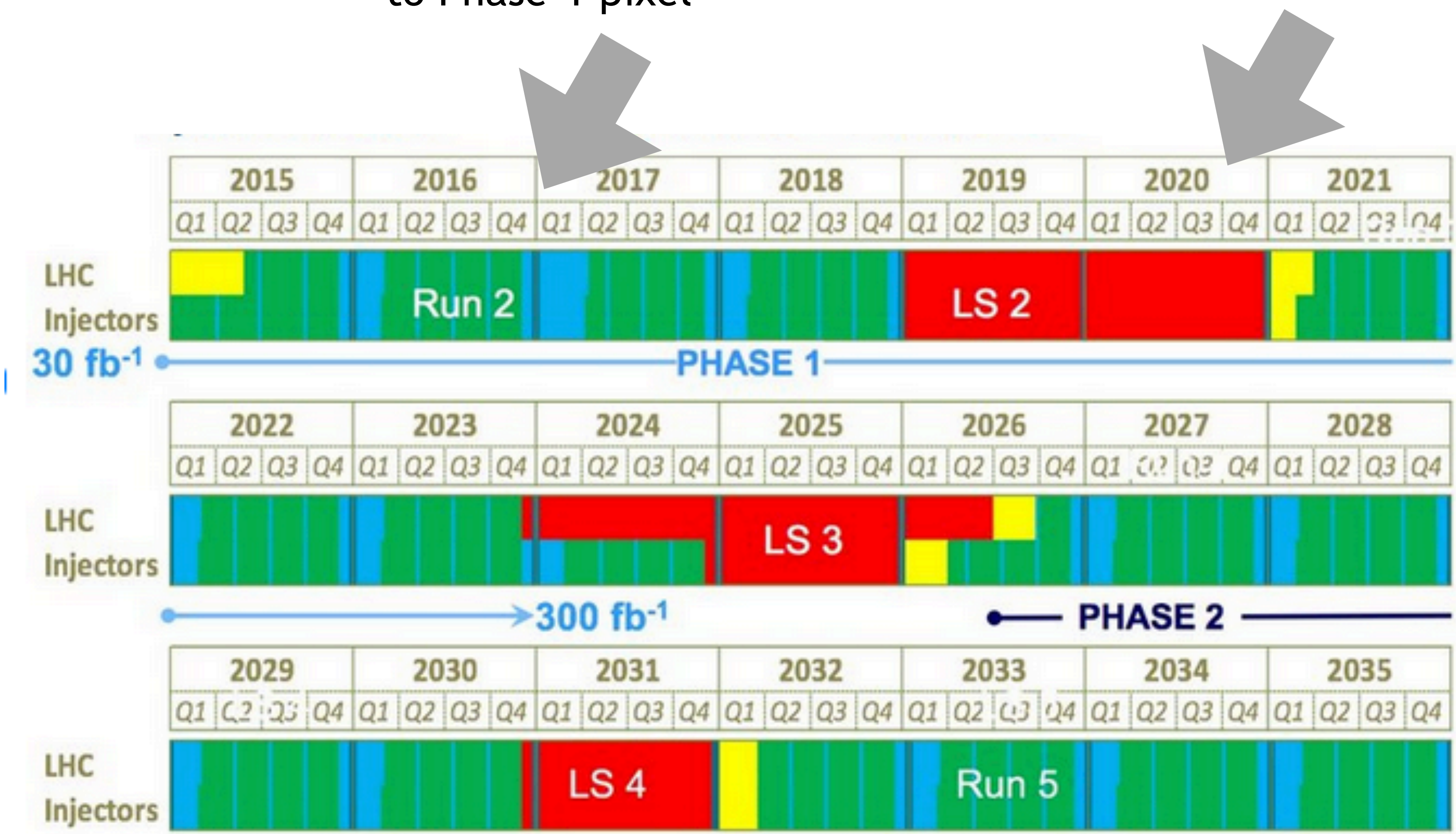


Hardware connections

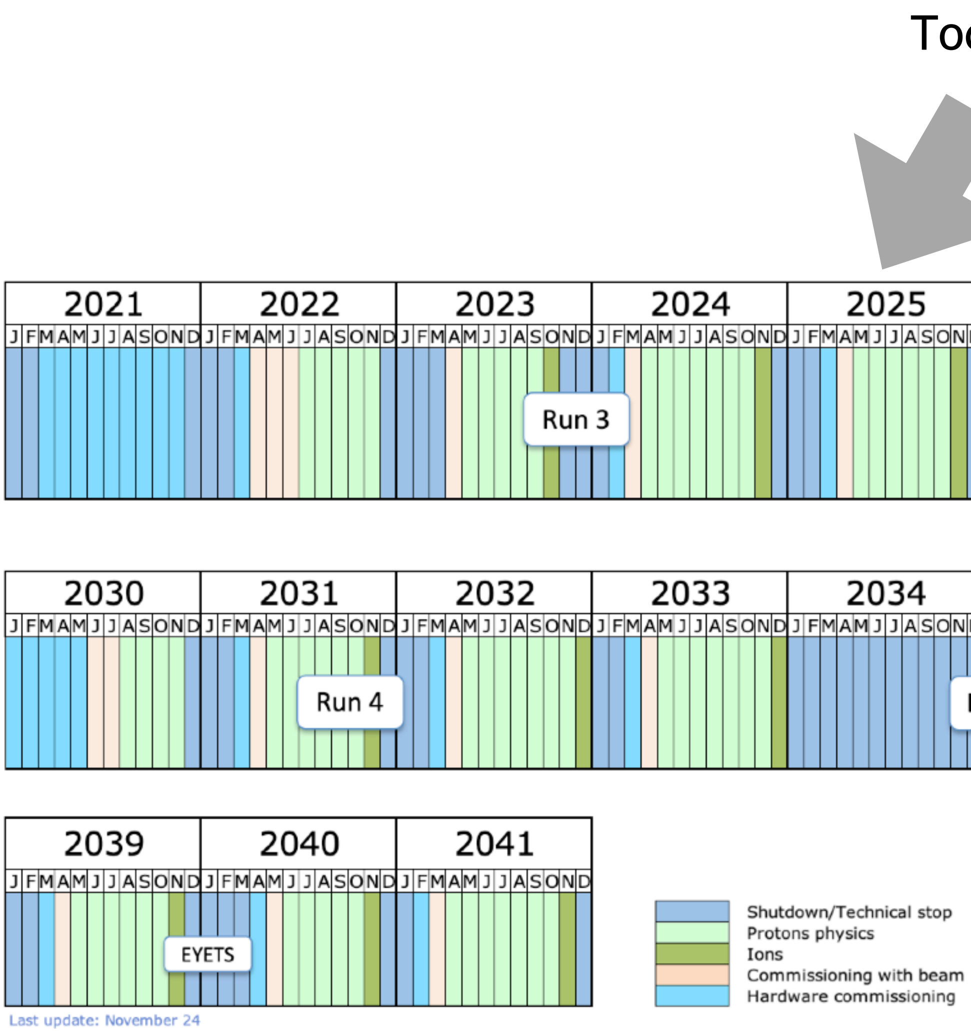


Change from Phase-0 pixel to Phase-1 pixel

Refurbishment of Phase-1 including new BPix Layer 1



an old version of the LHC schedule!

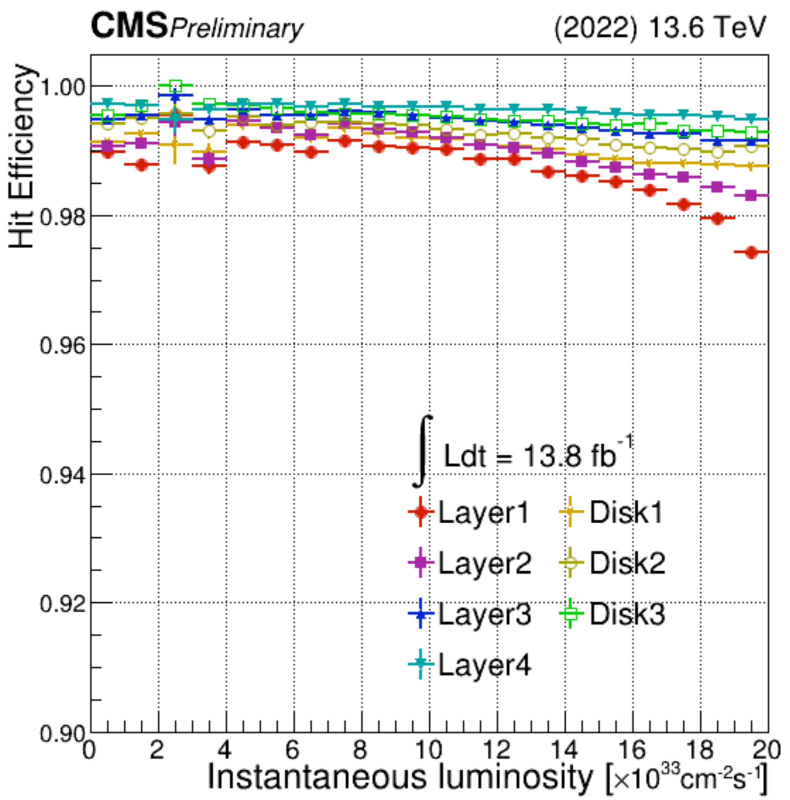


Today
2021
2022
2023
2024
2025
2026
2027
2028
2029
Run 3
Long Shutdown 3 (LS3)
2030
2031
2032
2033
2034
2035
2036
2037
2038
Run 4
LS4
Run 5
2039
2040
2041
EYETS
Last update: November 24
Shutdown/Technical stop
Protons physics
Ions
Commissioning with beam
Hardware commissioning

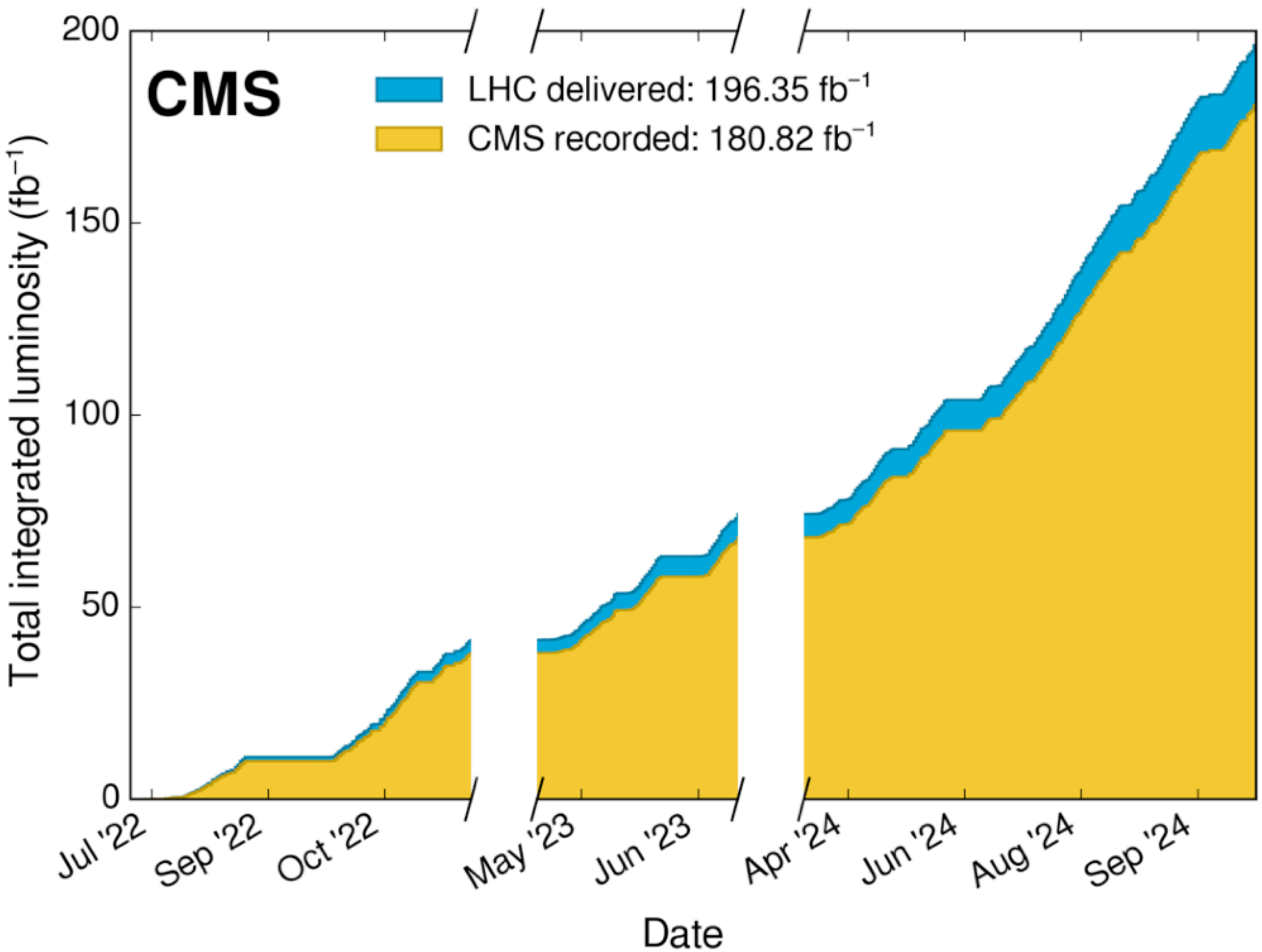
Beginning of Run 3

- Pixels refurbished and reinstalled in June 2021
- **Completely new layer 1** has significant improvements
    - ➡Readout chip decreased dynamic inefficiency and reduced crosstalk
    - ➡New TBM with additional delay option
    - ➡New high density interconnect for more robust HV operation
- Some layer 2 modules replaced
- New DCDC converters
- Improved FPix cooling connections

➡**Excellent performance in start of Run 3 in 2022**

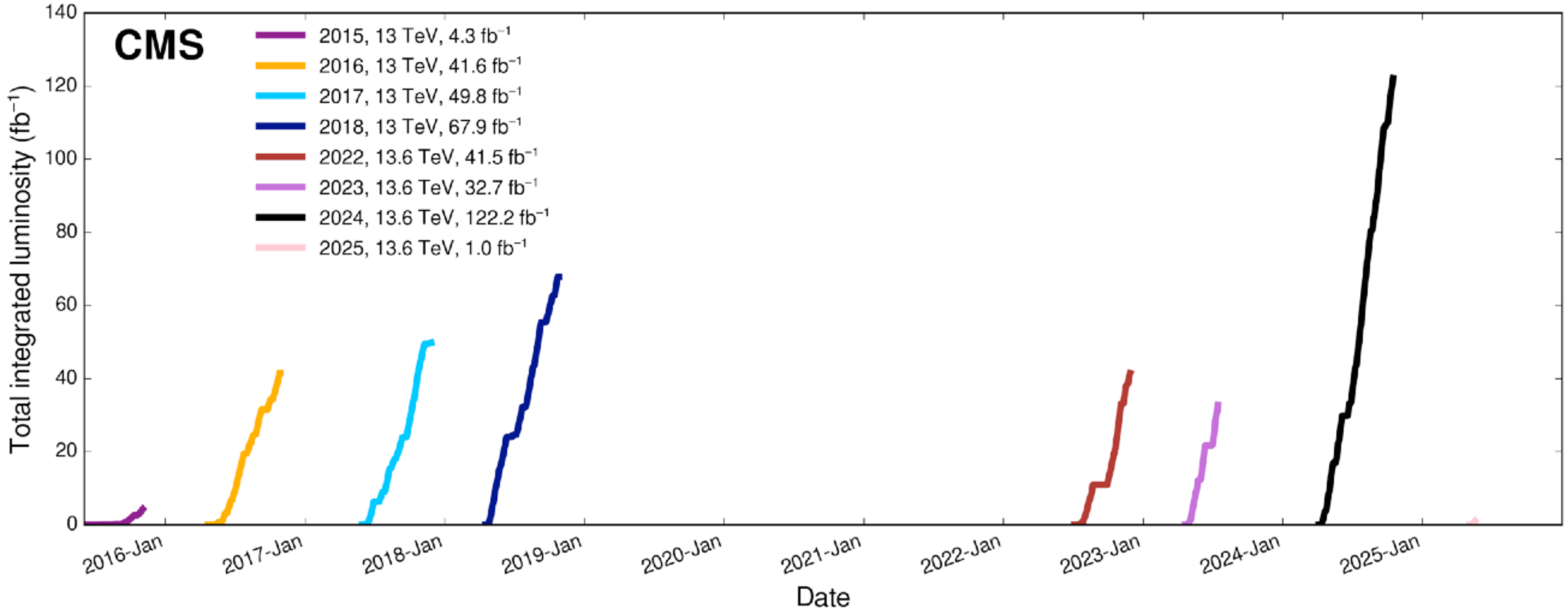


Run 3 luminosity

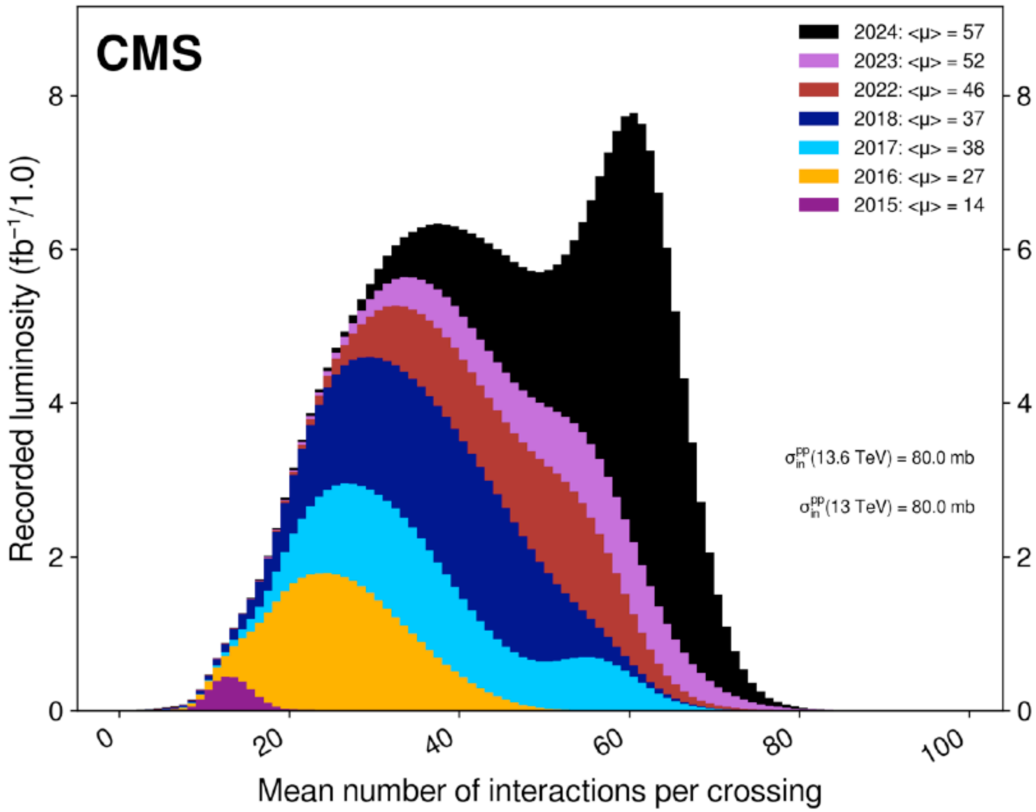


- 124 fb^{-1} delivered in 2024
- Projecting up to 120 fb^{-1} in 2025

Luminosity since 2016



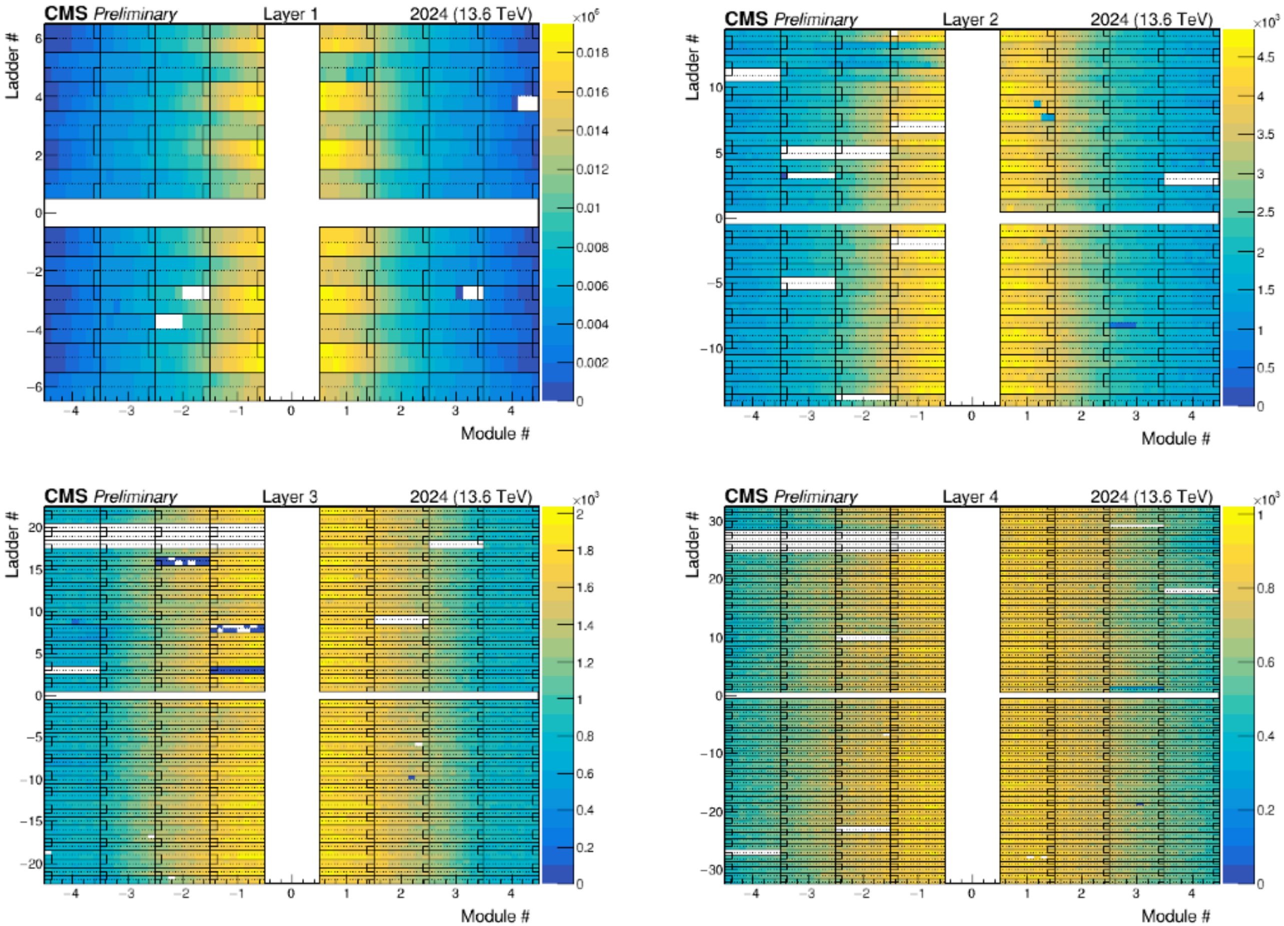
Pile up



- Number of interactions per crossing during pp collisions
- CMS is becoming more ambitious over the years

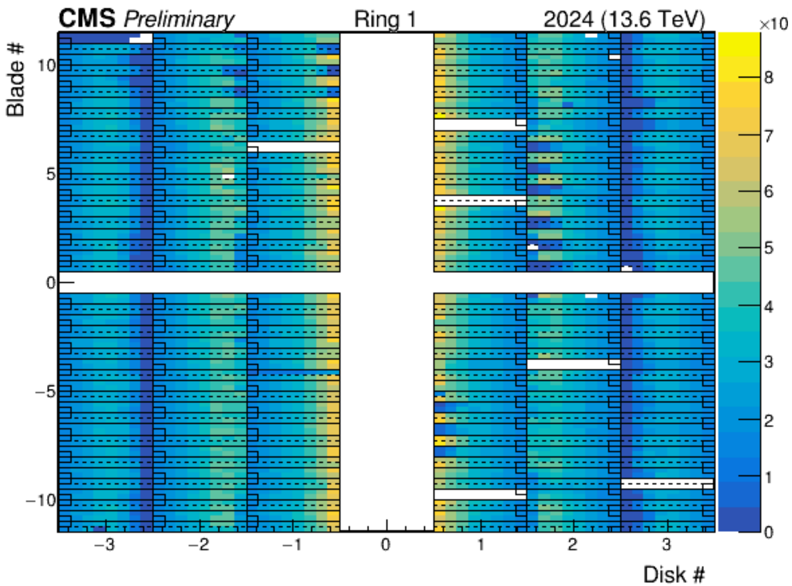
Performance

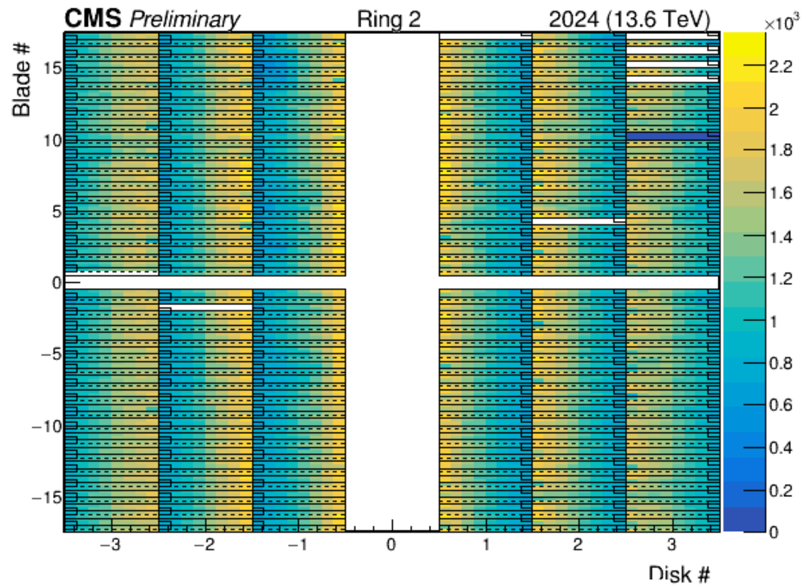
Active detector fraction: BPix



Total active fraction now: 96.0%

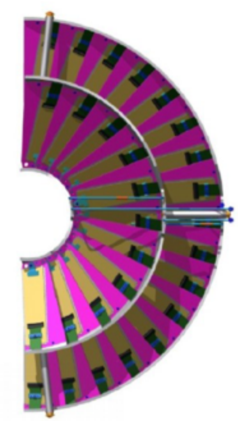
Active detector fraction: FPix





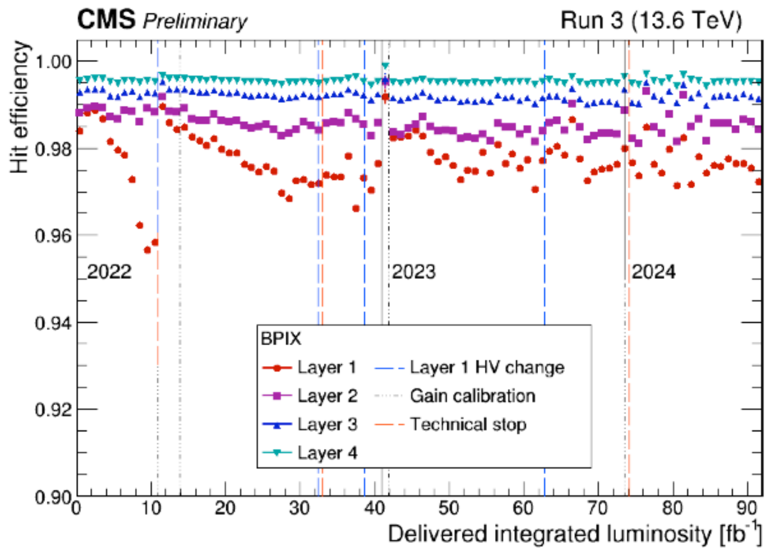
Ring 2

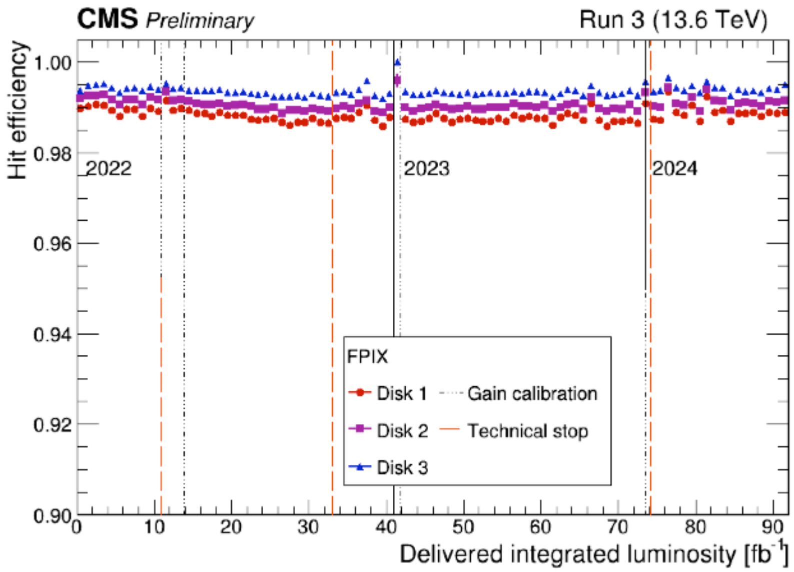
Ring 1



Total active fraction now: 95.8%

Hit efficiency

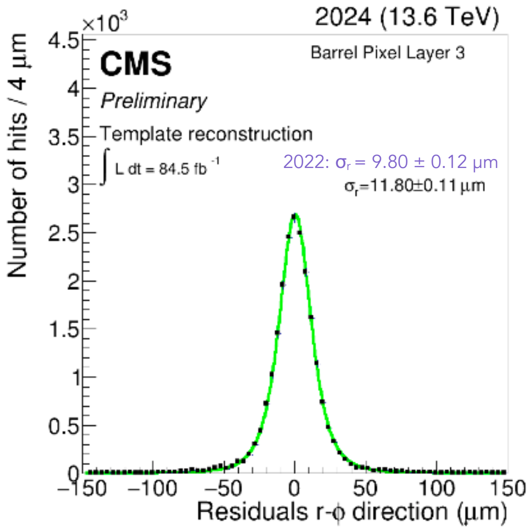


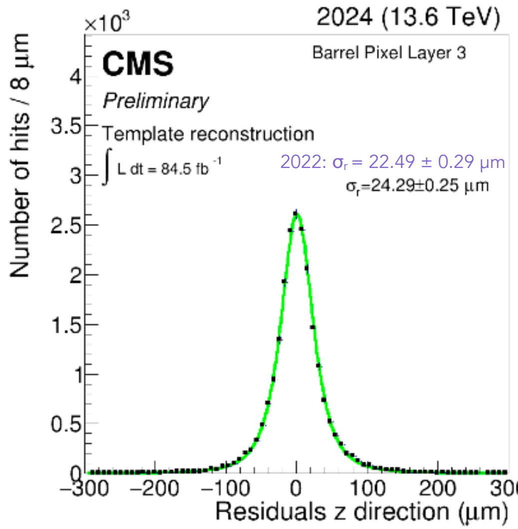


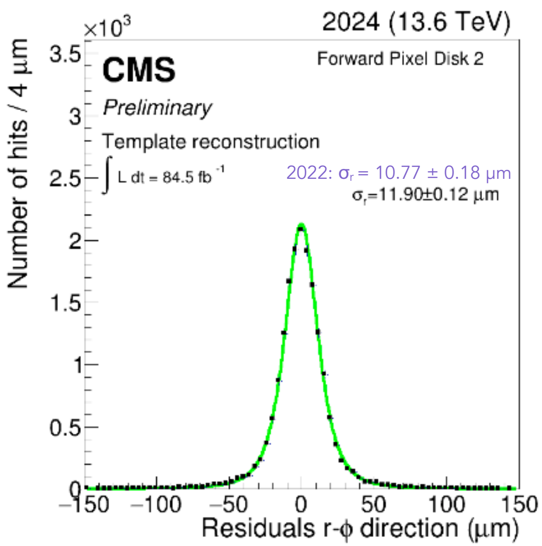
- Hit efficiency affected by gain calibration, HV setting, and annealing during technical stops

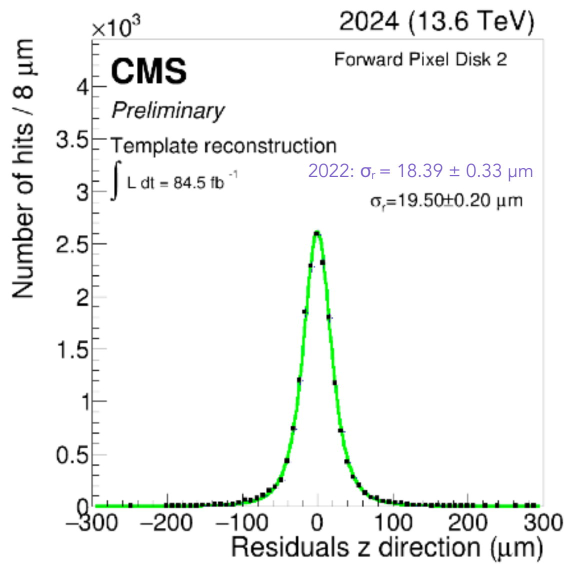
➡ High hit efficiencies for all layers and disks

Resolution









Great position resolution

➡ Performance consistent with expected evolution

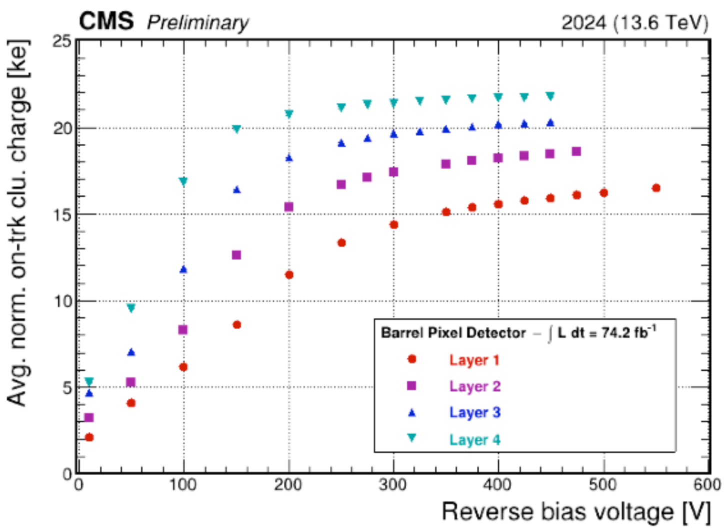
➡ Comparable to performance seen in previous years

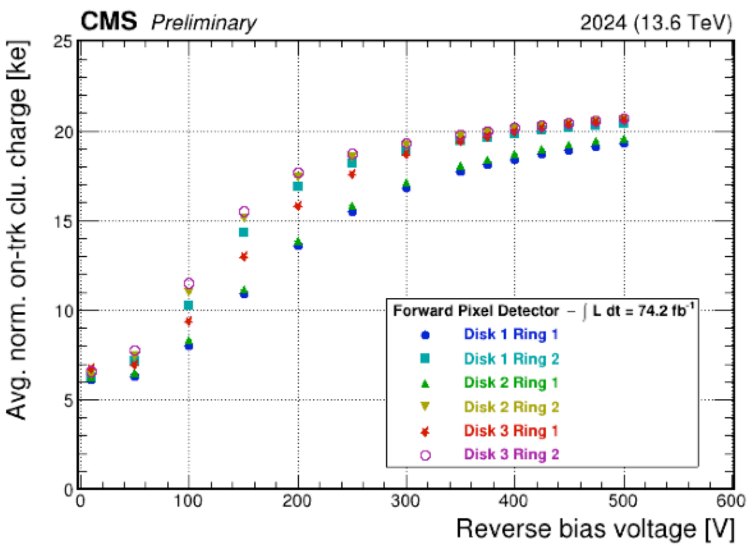
Cluster charge measurement

Cluster charge measured as function of bias voltage to determine when settings should be adjusted

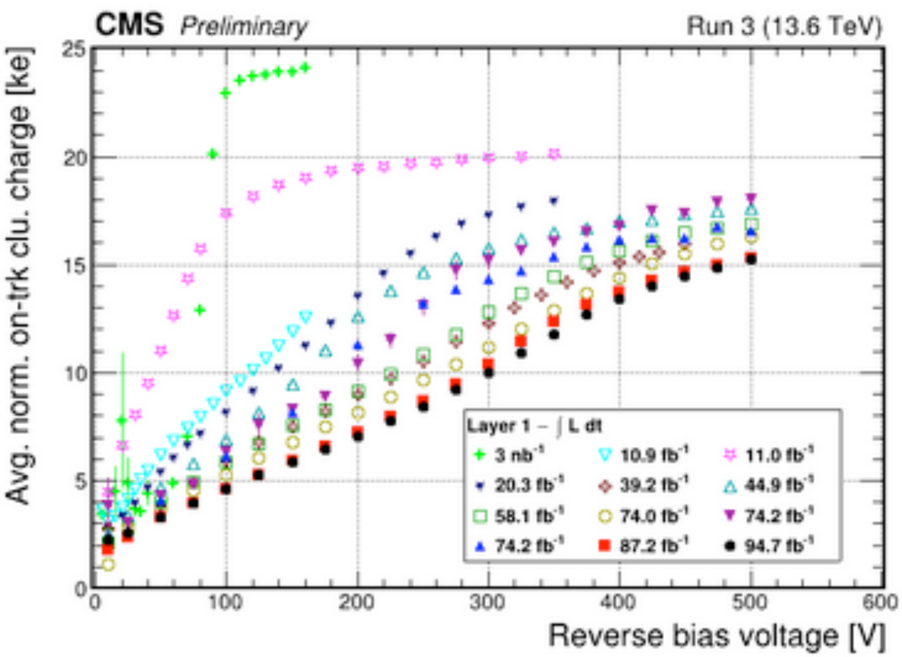
Current settings

- Layer 1: 600 V
- Layer 2: 450 V
- Layer 3: 350 V
- Layer 4: 300 V
- Ring 1: 450 V
- Ring 2: 350 V





BPix Layer 1 bias scans



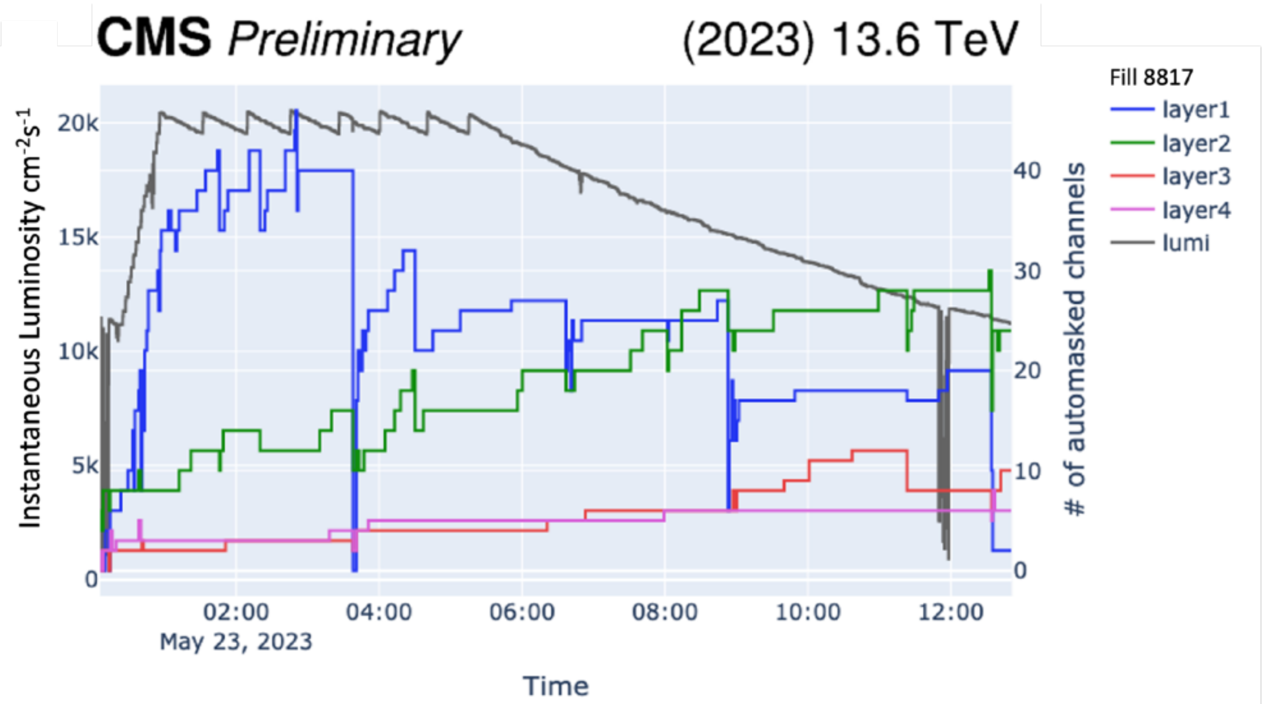
Layer 1 evolving rapidly

- ➡ HV bias scans performed regularly to monitor performance
- ➡ Layer 1 began Run 3 with HV bias of 150 V, now at 600 V
- ➡ Maximum setting of power supplies is 800 V

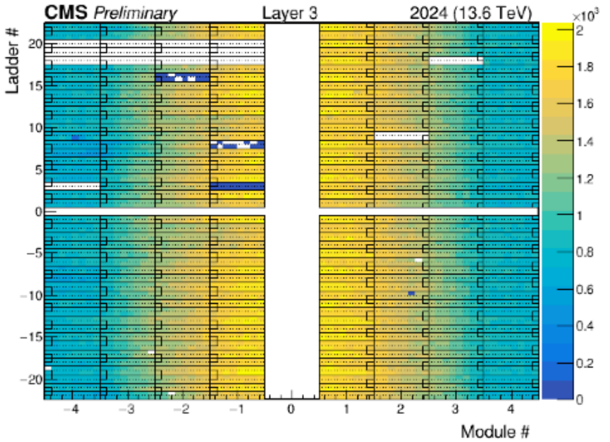
Operational challenges

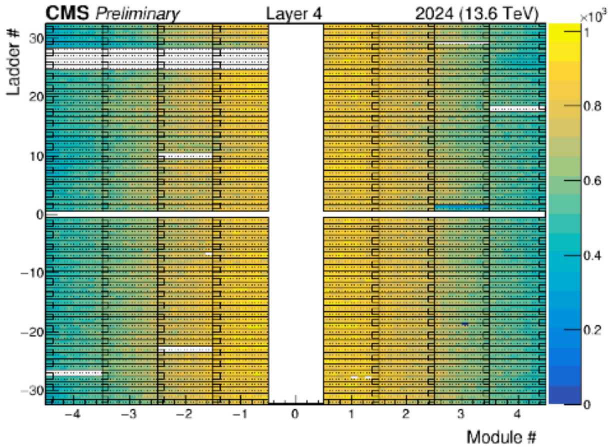
Automasked channels

- Channels masked during data-taking due to readout errors
  - ➡ **Layer 1:** operational problem sometimes mitigated by changing timing settings on TBM
  - ➡ **Layer 2-4:** unrecoverable SEUs accumulate over a fill, recovered by powercycling via DCDC between LHC fills
- Recovery action at certain pile up for Layer 1

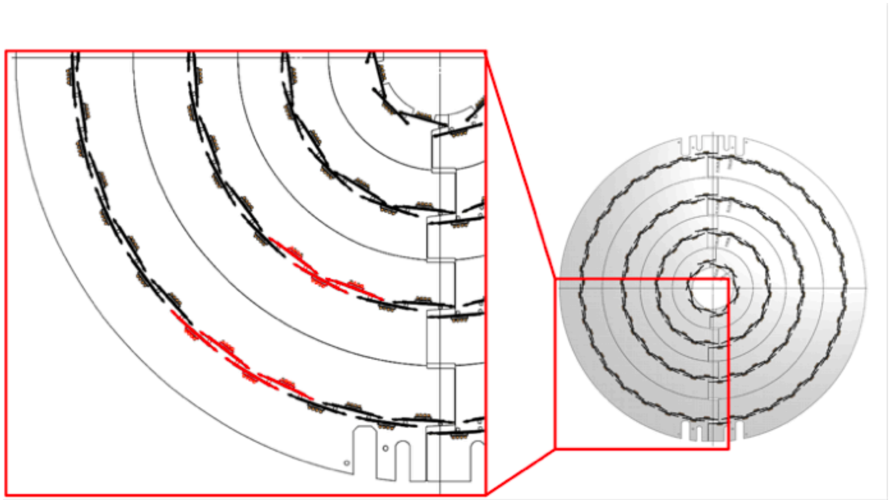


BPix QPLL issue

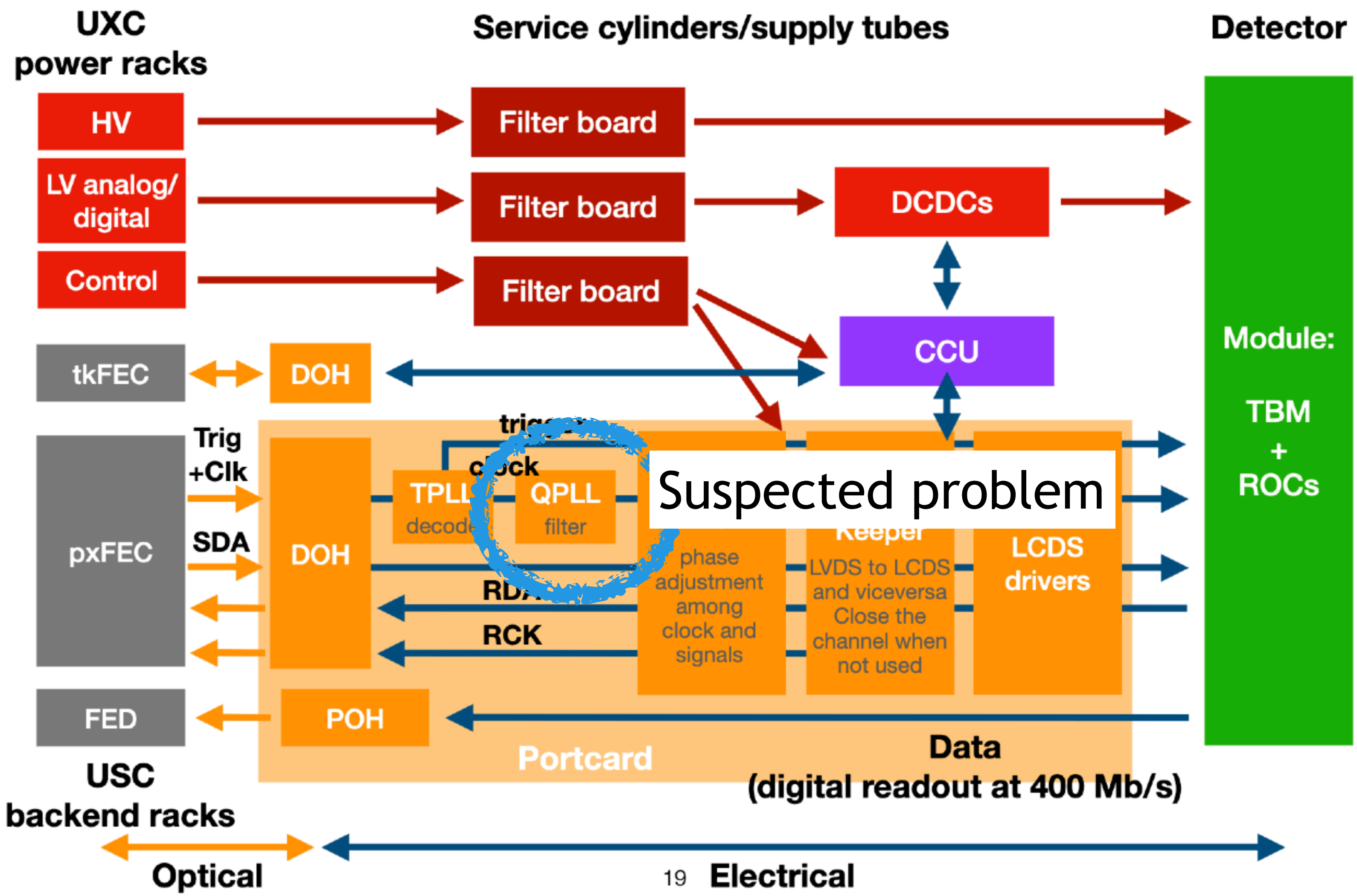




- Quartz controlled PLL circuit does not lock to LHC clock
- Layers 3 and 4 of one sector of barrel pixels affected
- Modules are not currently read out
  - ➡ Fixing the issue would require extracting and reinstalling pixel detector

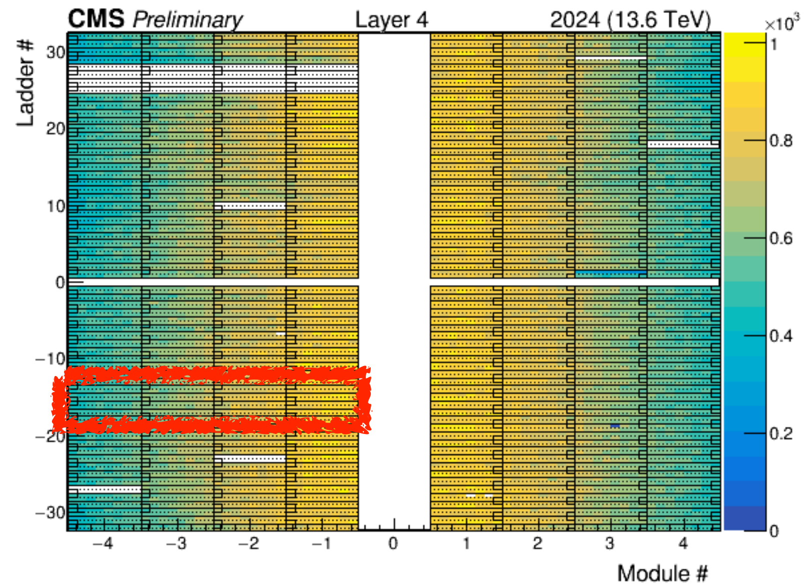


Pixel hardware connections



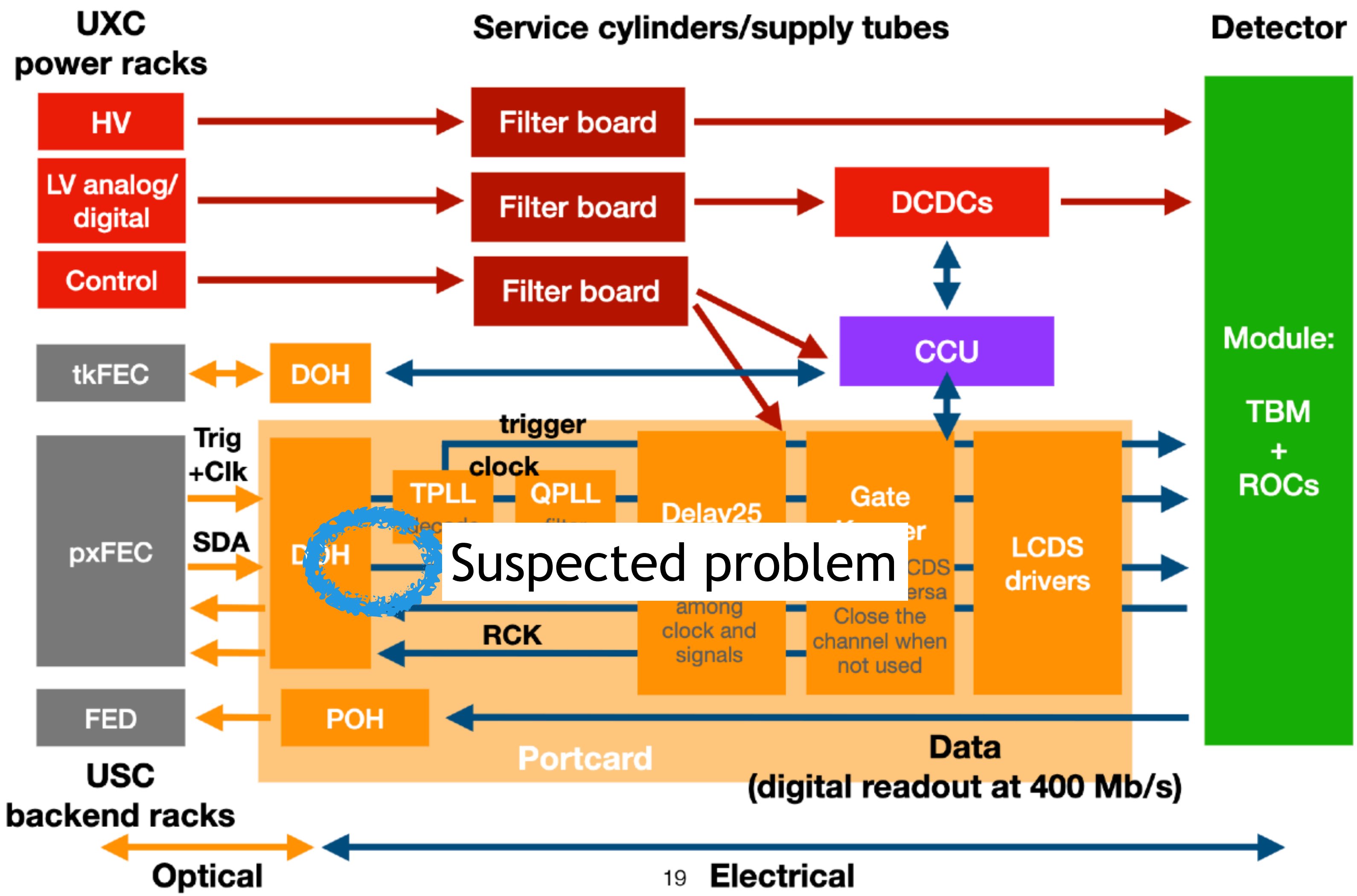
BPix issue on electronics line

- Group of 16 modules in BPix Layer 4 that are functional only sporadically
- Implemented software change to minimize the number of times the modules are reprogrammed



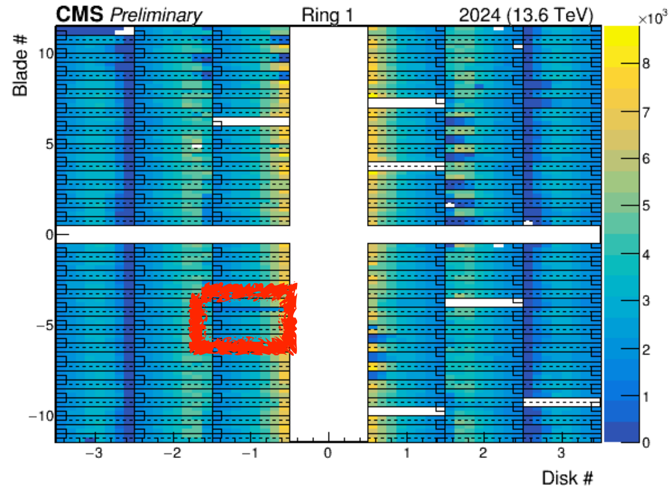
➡ Another issue that would require extracting and re-installing the detector

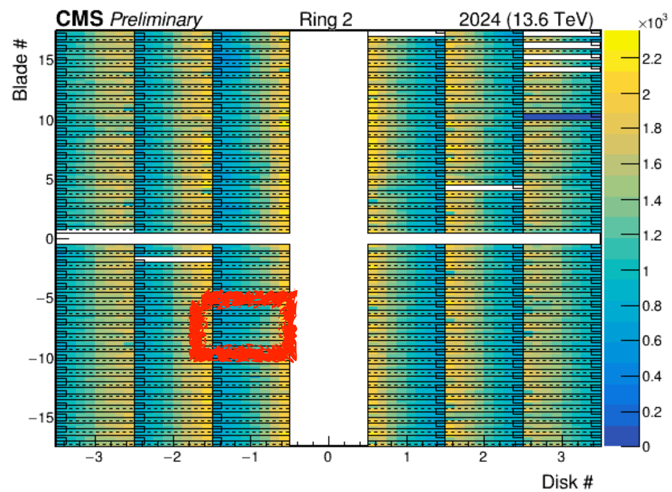
Pixel hardware connections

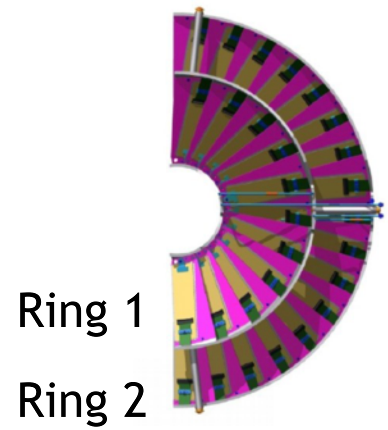


FPix portcard issue

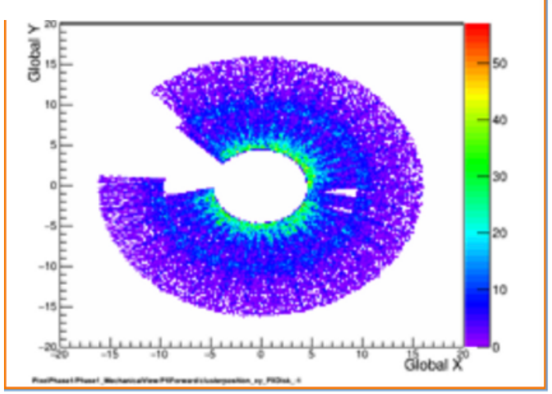
- FPix portcard stopped working in July 2024
- Corresponds to a group of 14 modules
- Receives clock but no triggers





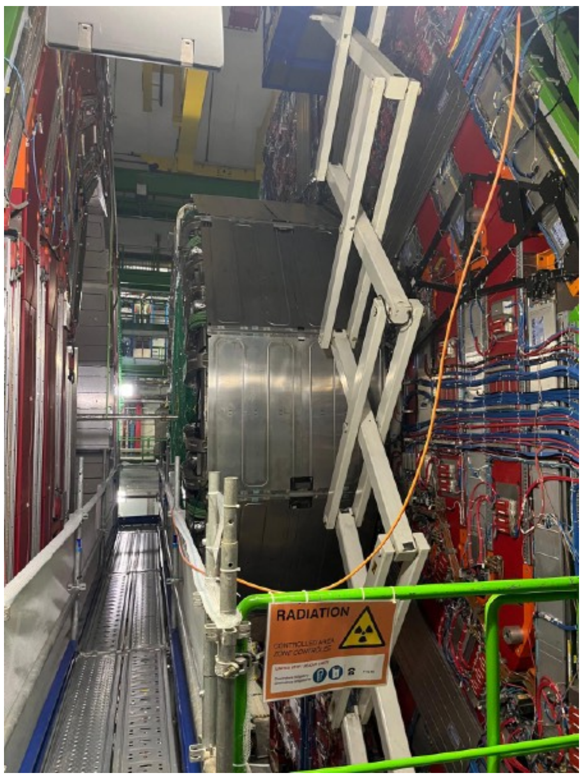


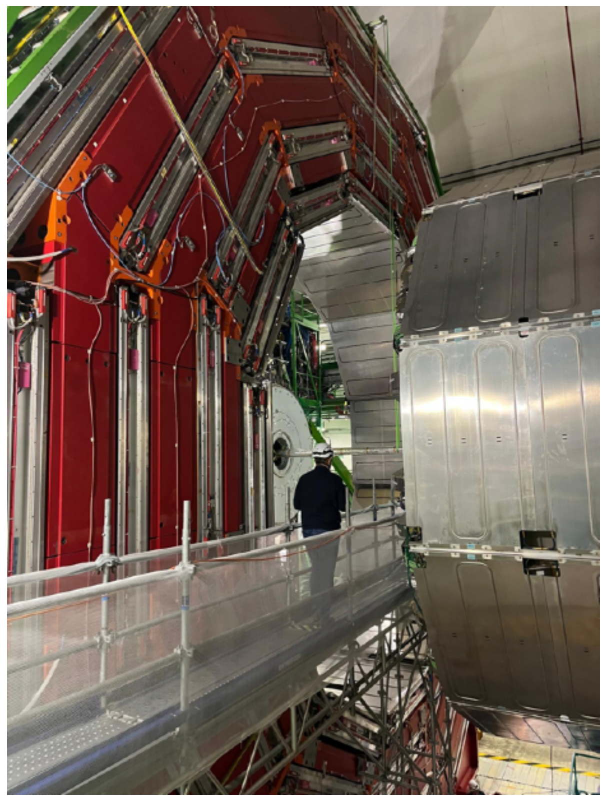
FPix Disk1 BmO



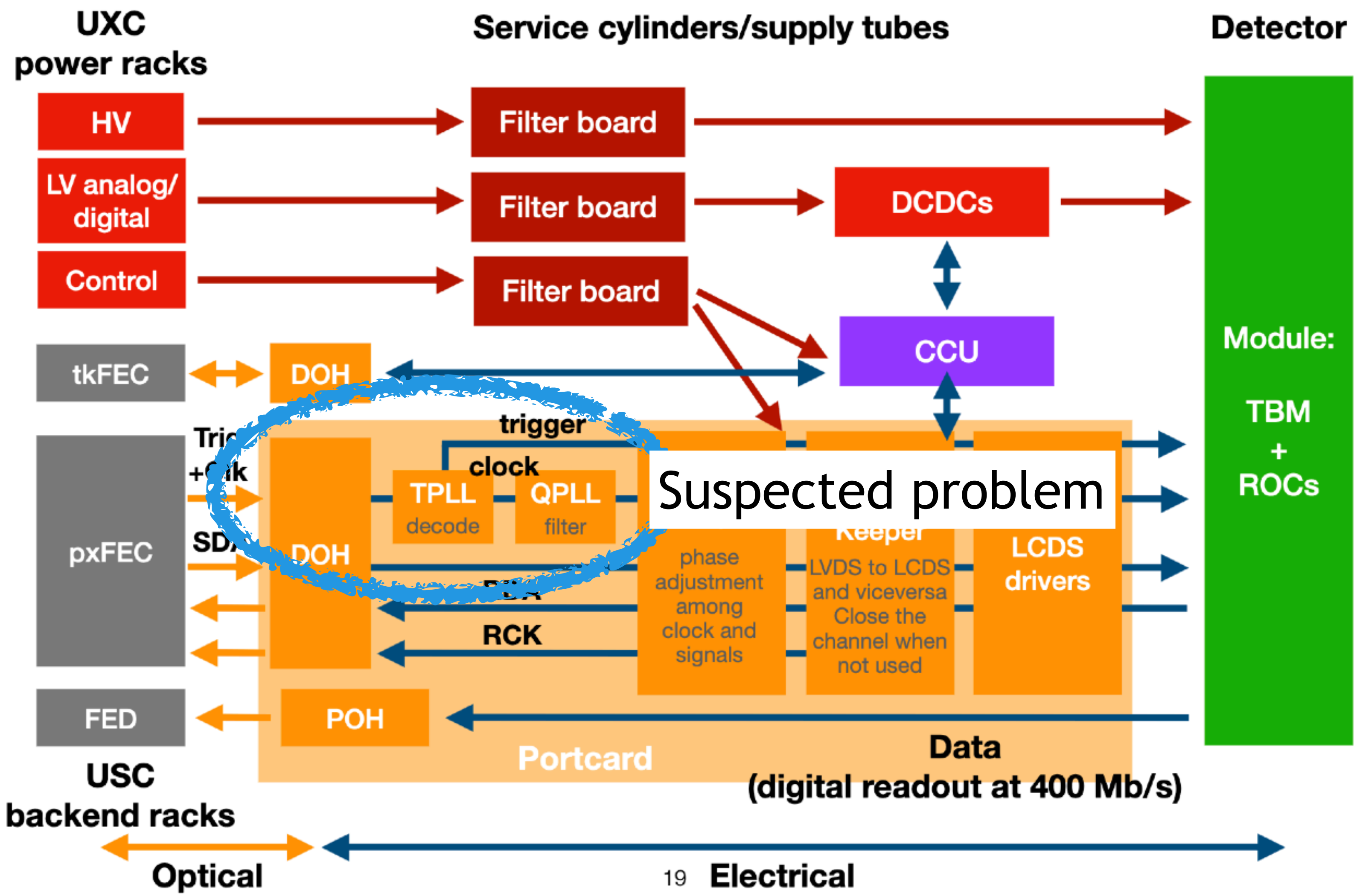
Intervention on FPix this year

- The CMS detector was opened during the 2024/2025 Technical Stop of the LHC
- We took the opportunity to try to clean our fiber connection of the malfunctioning portcard!

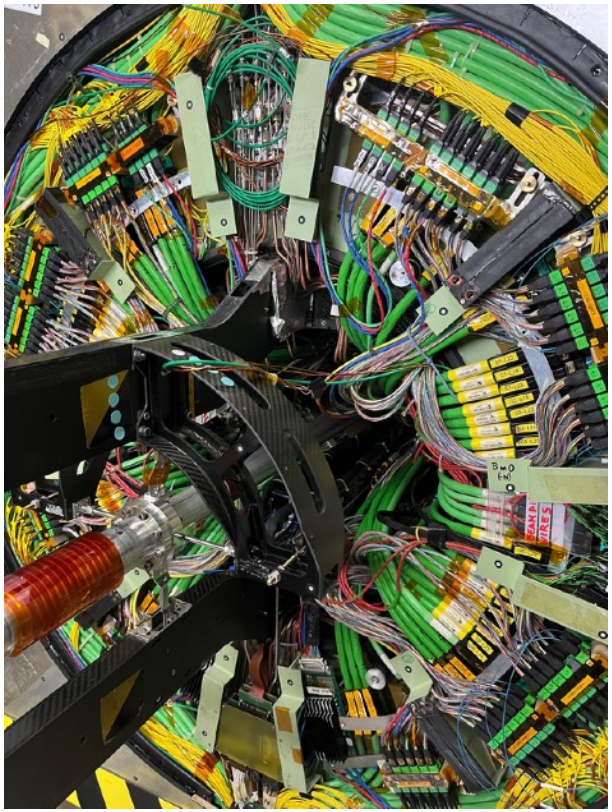





Pixel hardware connections

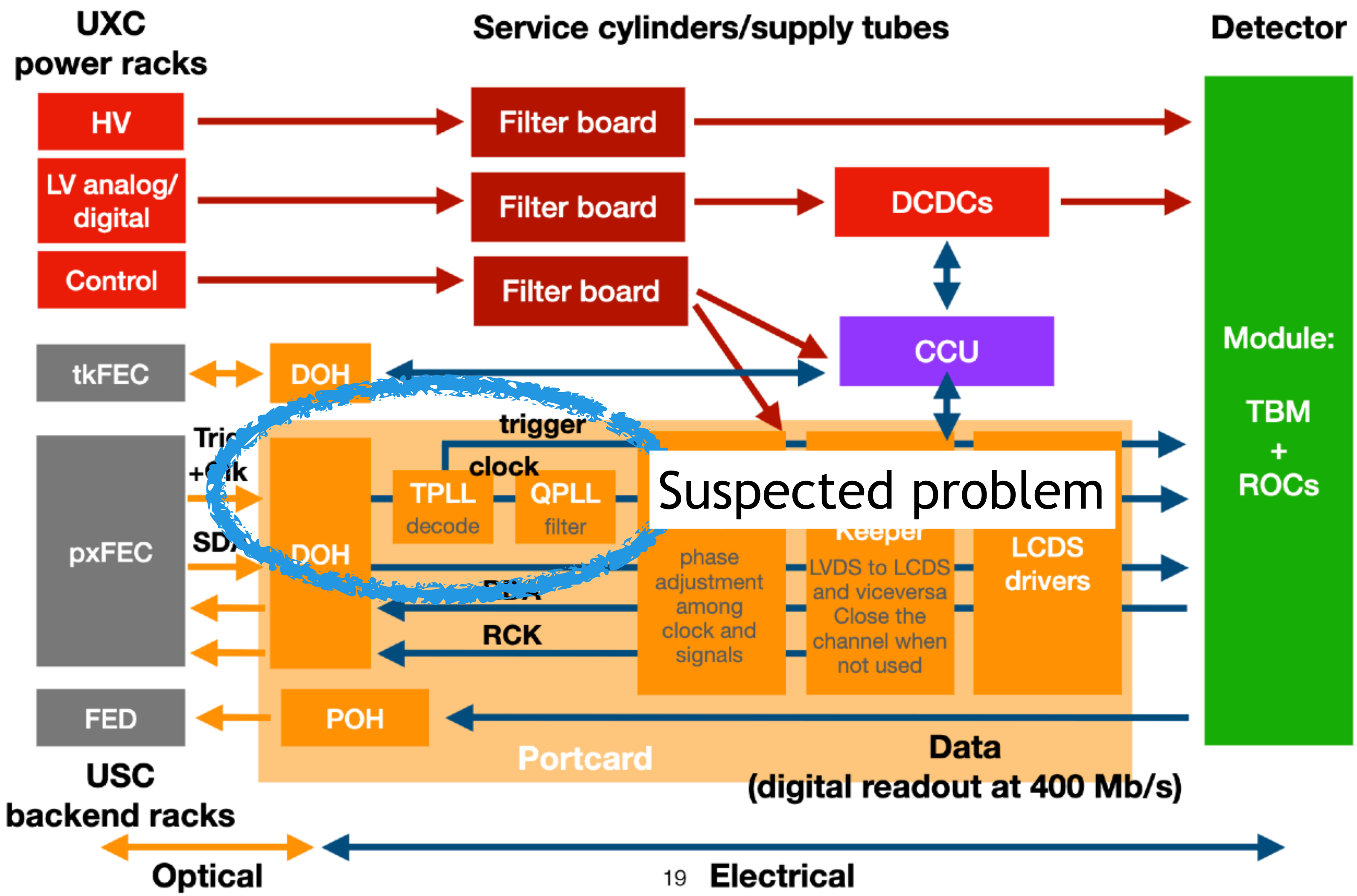


Cleaning pixel fiber assoc. with problematic FPix portcard

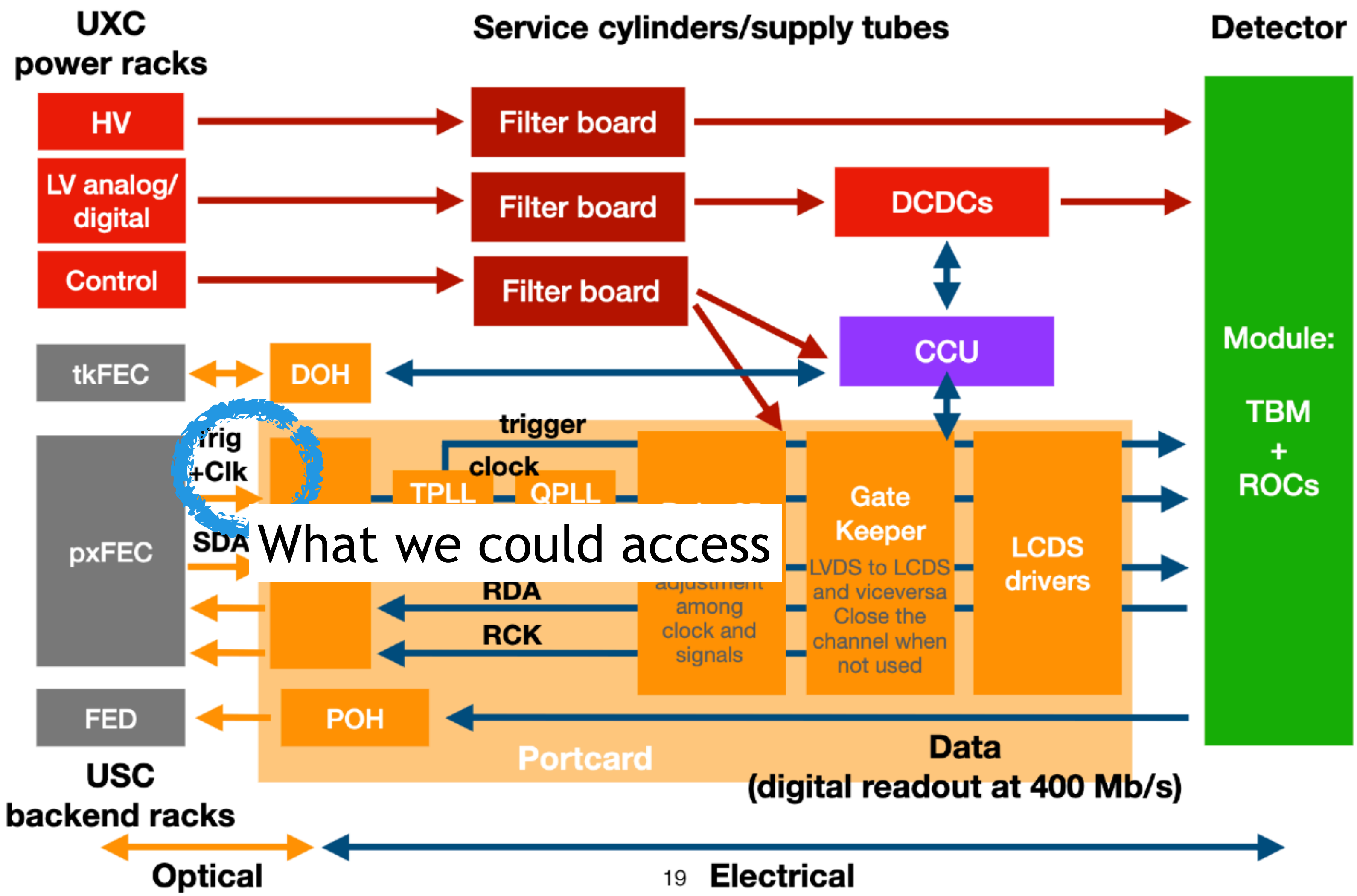


- ➡ Optical fiber connection inspected and cleaned
- ➡ Intervention did not recover these modules

Pixel hardware connections

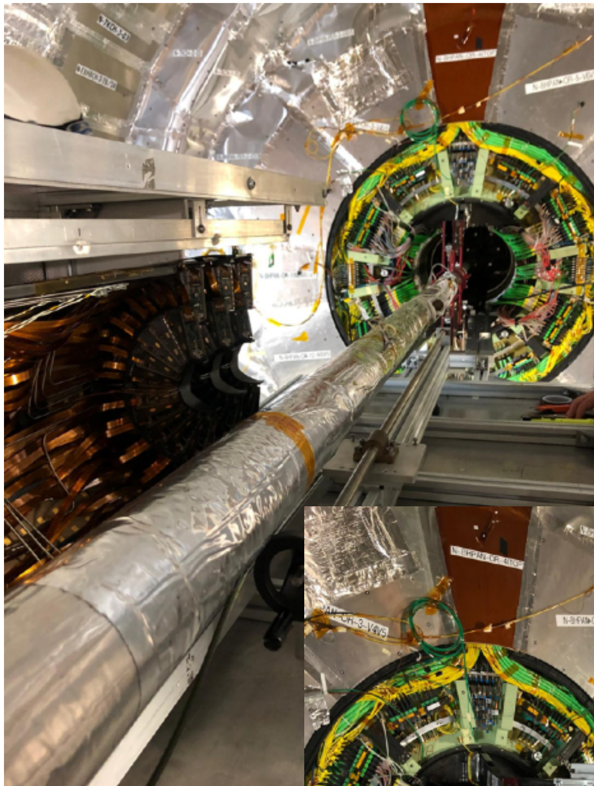


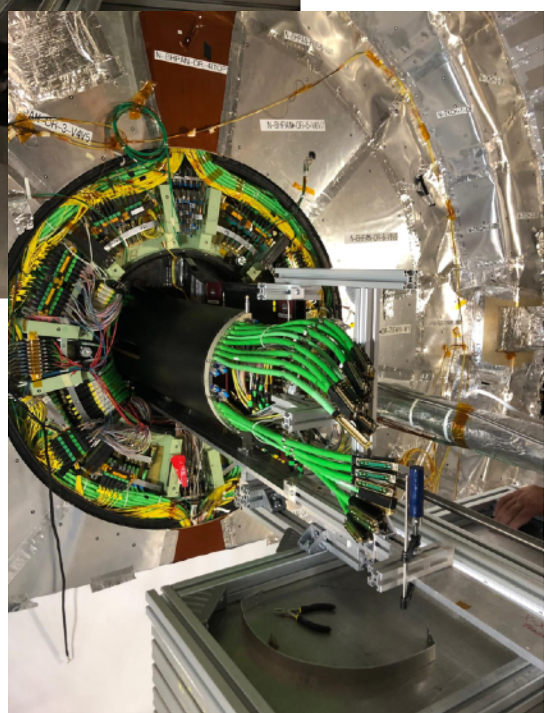
Pixel hardware connections



What’s next?

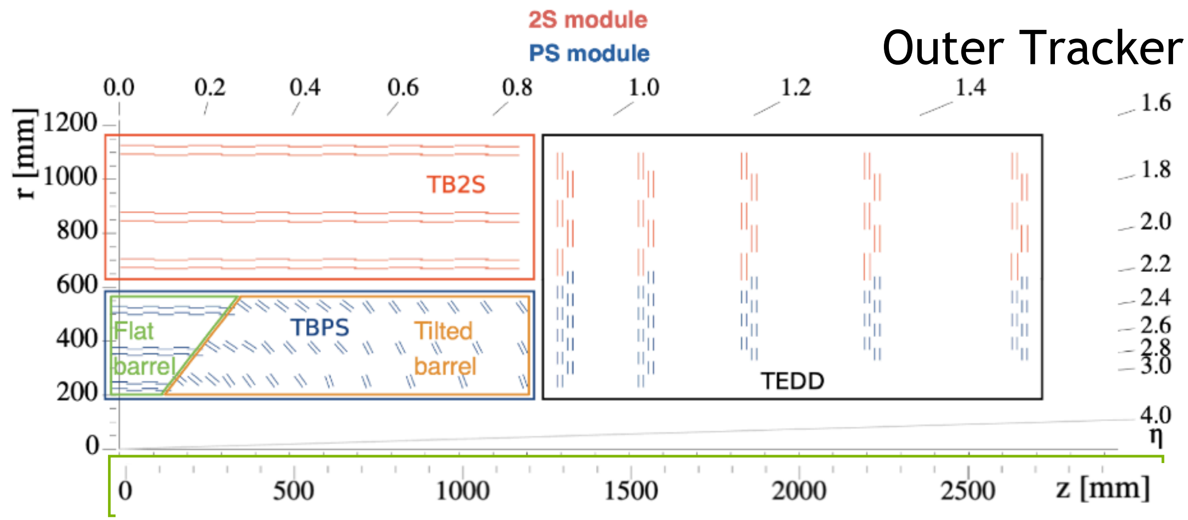
Decommissioning activities for 2026

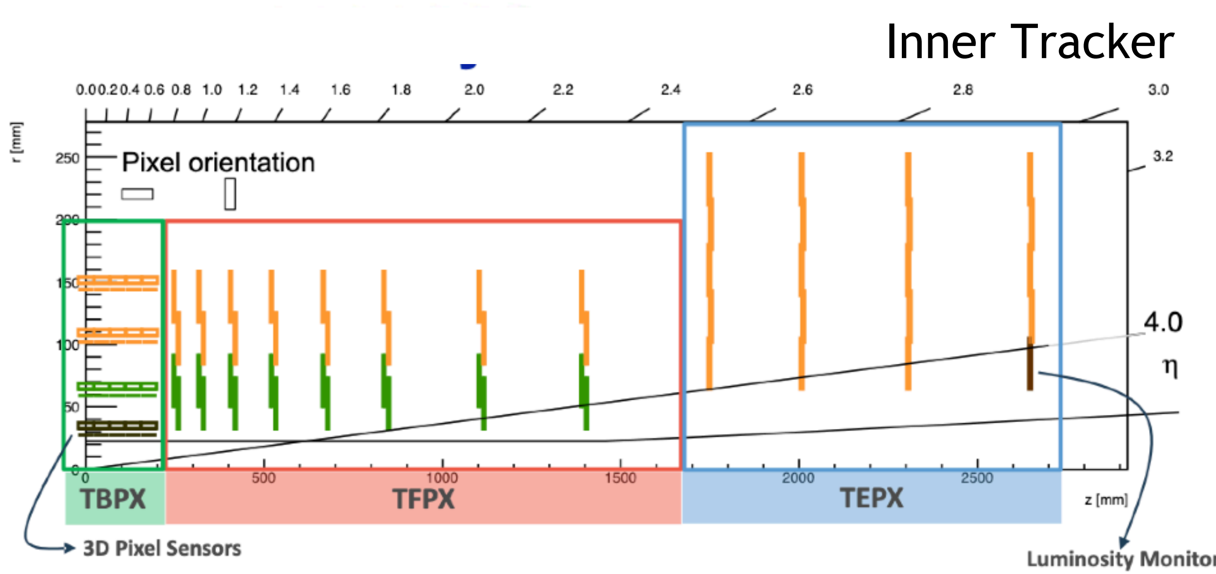




- **Run 3 ends 30 June 2026**
- UXC (experimental cavern)
    - Pixel detector and beampipe
    - Cooling and power systems
    - Strip tracker and its services
- USC (service cavern)
    - Services and DAQ racks

Transition to Phase 2





- CMS will be getting a brand new tracking system for HL-LHC (aka CMS Phase 2)
- **IPHC will play an extremely important role!**

Summary

- The CMS pixel detector is performing well with continuous monitoring and calibrations
- High amount of integrated luminosity during LHC Run 3 has presented challenges
  - ➡ Radiation damage degrades performance over time
  - ➡ A few problems with electronics located on the service cylinders have led to losses of small groups of modules
  - ➡ Readout errors at high pile up create a challenge for BPix Layer 1
- Run 3 will conclude next year and the tracking system of CMS will be upgraded

Thank you!

Backup

Radiation levels

BPix Layer 1

End Of	Luminosity[fb-1]	Dose[Mrad]	Fluence[10^14]	Voltage
2017	51	19.	4.0	350
2018	117	45	9.3	450
2022	41	16	3.2	400
2023	73	28	5.8	450
2024	197	75	16	550

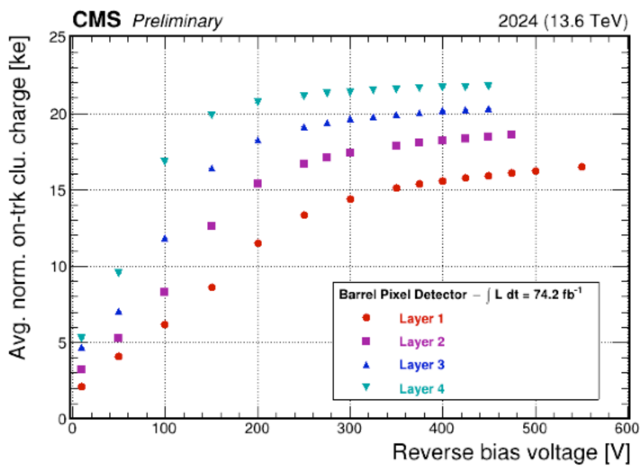
Comparison among BPix and FPix

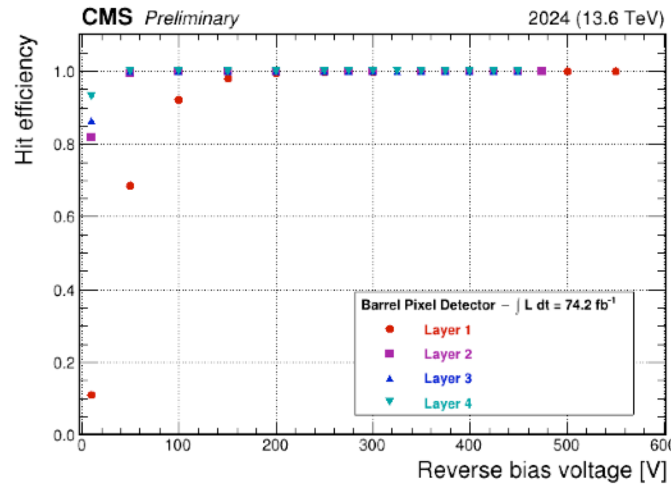
	Dose[Mrad]	Fluence[N-eq/cm2]		
Layer 1	75	16E14	121/25	143/30
Layer 2	31	6E14	42/8.3	48/9.4
Layer 3	15	3E14	20/4.1	23/4.7
Layer 4	8	1.8E14	11/2.5	12.5/2.9
FPix inner	83	17E14	115/23	131/26
FPix middle	17	3.2E14	23/4.4	26/5.0
FPix outer	9	1.8E14	12/2.4	14/2.8

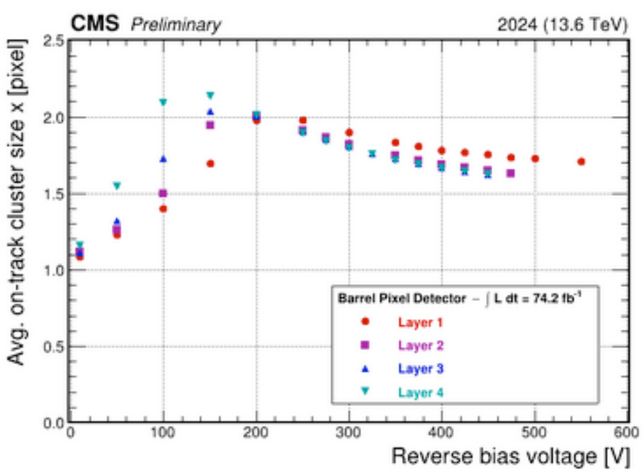
from Danek

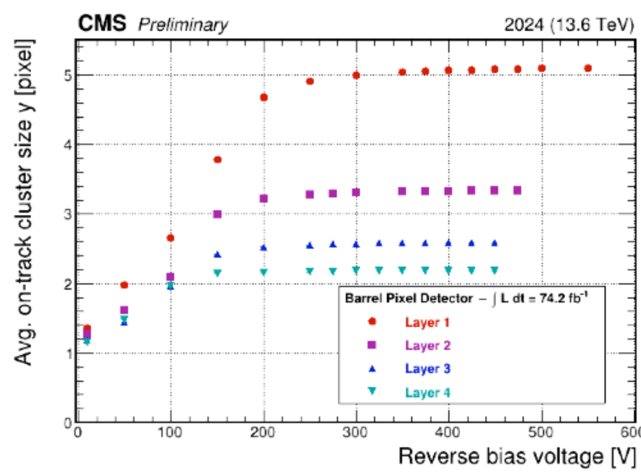
Cluster size and hit efficiency

Hit efficiency and cluster size in x and y also used to evaluate performance









UXC vs. USC

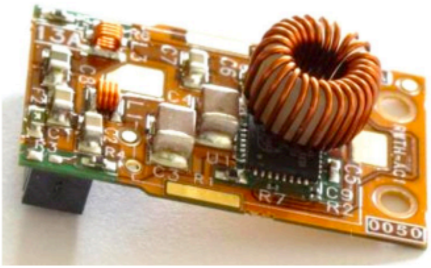
- Important distinction between activities in the experimental cavern (UXC) and service cavern (USC)
- Especially at the beginning of LS3, there will be restrictions in UXC based on the radiation zone classification
    - More trainings required
    - Active dosimeter to be worn
    - Limit time in this zone
    - Will be closely monitored by Radiation Protection team

UXC

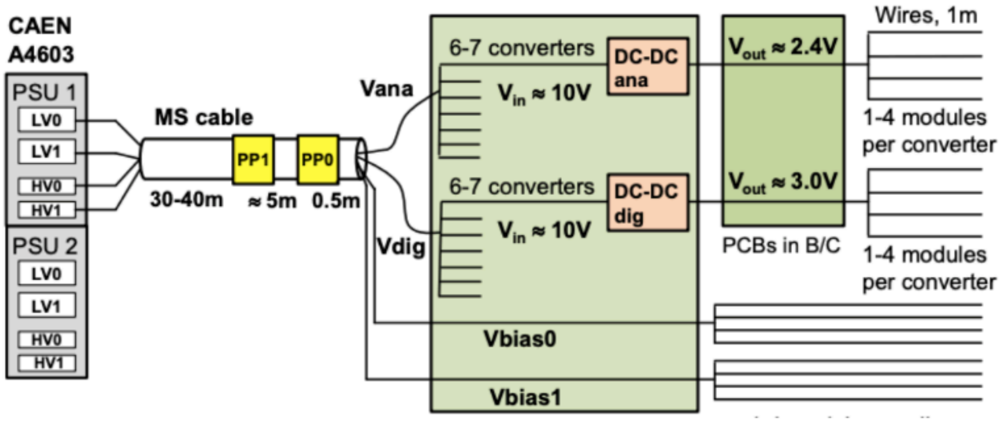
USC

Powering

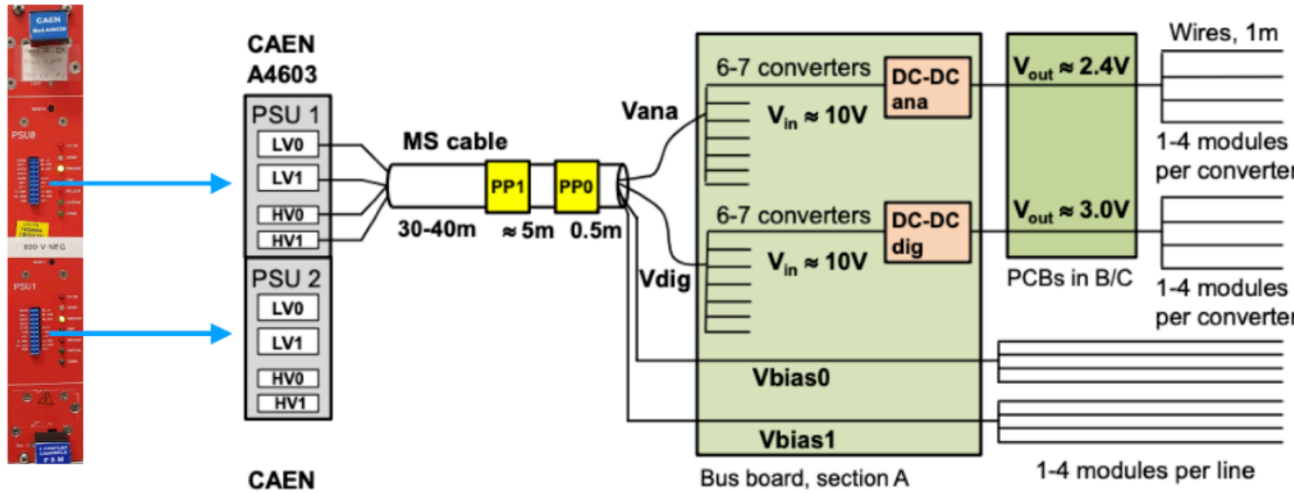
- DC-DC converters used in detector
- 1216 total DC-DC converters convert input of 10 V and converts this to 2.4 - 3.5 V for the ROC and TBM
- One pair of DC-DC converter delivers the analog and digital voltage
- Placed about 1 m away from detector modules
- Connected to power supply channel

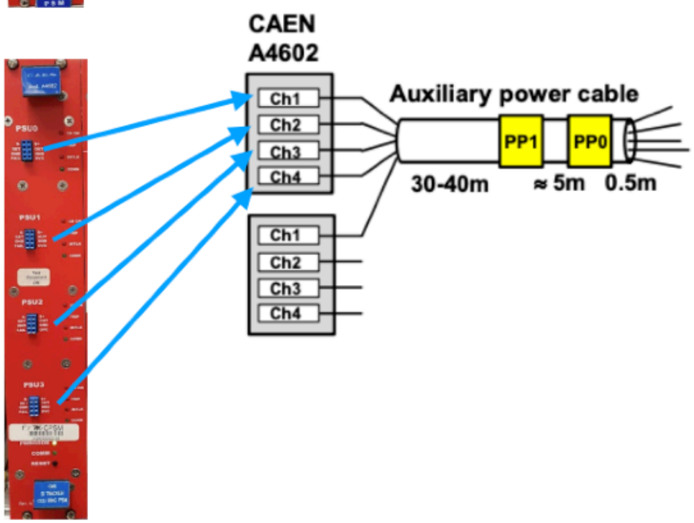


Type	Required
2.4 V (= Analog)	608
3.3 V (=Digital, BPix)	320
3.5 V (=Digital, FPix & BPix L2)	288



Powering system





5 x power to POHs etc.
of one readout slot,
or to CCUs of one control ring

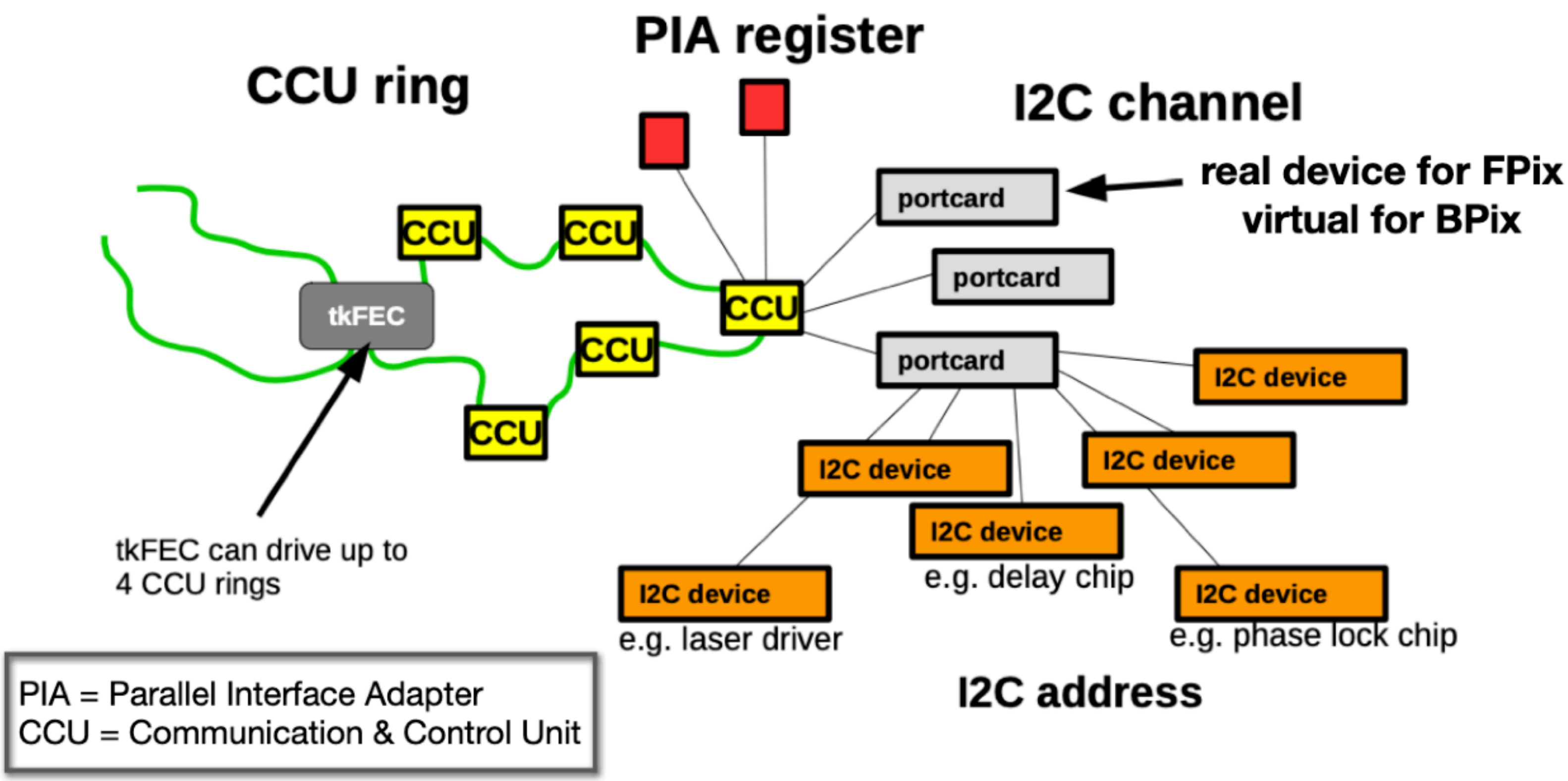
Different Power requirements

- Low Voltage: Analog and Digital module power
- High Voltage: Sensor power
- Control Voltage: Auxiliary electronics power

Auxiliary hardware

CCU uses

- 12C channels to program readout electronics on service half-cylinders
- PIA registers to enable/disable DCDC converters and generate reset signals



Hit efficiency and residuals measurement

Hit efficiency is the probability to find any cluster within 1mm around an expected hit independent of the cluster quality

- Measured using muon tracks with pT > 2 GeV
- Bad components of the pixel detector are excluded from the measurement

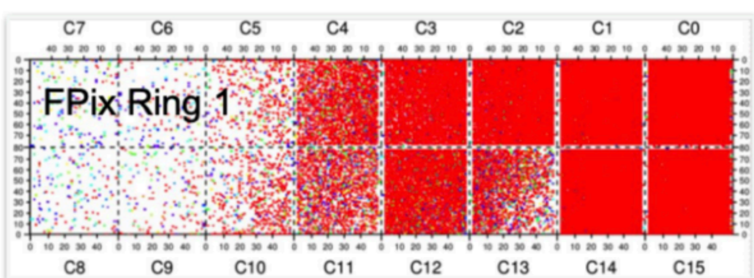
Hit residuals measurement:

- Triplet method
  - p_T > 12 (4) GeV tracks with hits in 3 layers (disks) are selected and refitted using hits in two of three layers (disks) for the BPIX (FPIX).
  - Trajectory is extrapolated to remaining layer (disk) and residuals with the actual hit are calculated for the BPIX (FPIX)
  - Residual distribution fitted with the Student-t function to obtain the mean offset (μ) and resolution (σ)
    - Residual offset (mean) and resolution are obtained from the fit
  - Triplets considered:
    - Layer 3: propagate from hits on Layer 2 and 4
    - Disk 2: propagate from hits on Disks 1 and 3
- Reconstruction:
  - Generic:
    - Simple algorithm based on track position and angle
    - Used in our High Level Triggers (HLT) and early track iterations offline
  - Template:
    - Algorithm based on detailed cluster shape simulations
    - Used in the final fit of each track in the offline reconstruction

DCDC damaged modules

DCDC damaged modules not correctly powered

- Sensor leakage current cannot be drained efficiently if the ROC is not powered
- Bias voltage (HV) ON and module power (LV) OFF leads to bad grounding
- Leakage current is drained through the pre-amplifier, damaging the pre-amplifier and the module
- Damage seems to accumulate with radiation and distance from beamline
- 6 (accessible) Layer 1 modules replaced during 2017-18 YETS out of total 8 damaged modules in Layer 1
- Accessible DCDC-damaged modules in Layer 2 were replaced during LS2



Damages due to HV on and LV off

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