Tests and validation of the HGCAL Front End electronics

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June 23, 2025

Who am I?

- Have been around LLR for the last 2–3 years
  - Probably, it is not the first time you see me :D
- Worked on several projects: but mostly on software or physics
- First time working on hardware thanks to this M1 internship
- To carry on Bastien's work from his winter internship

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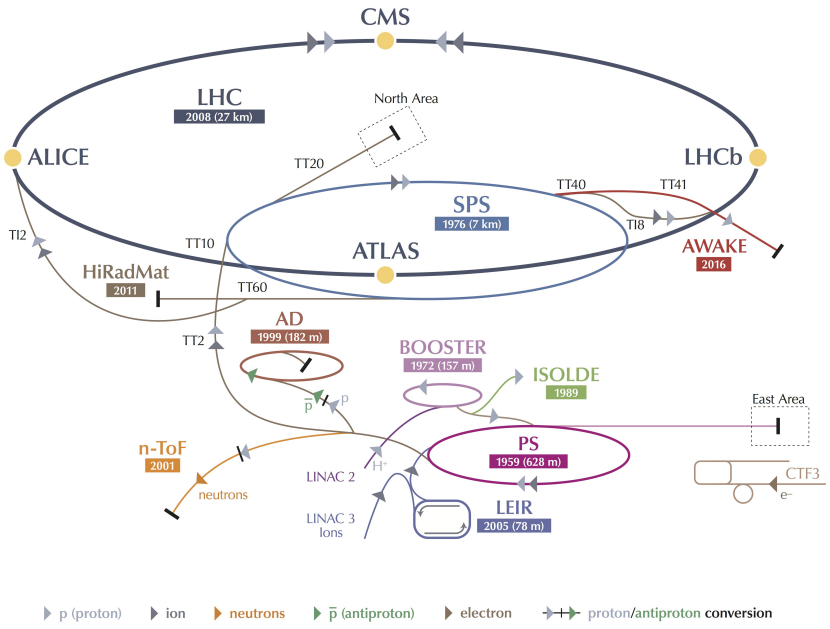
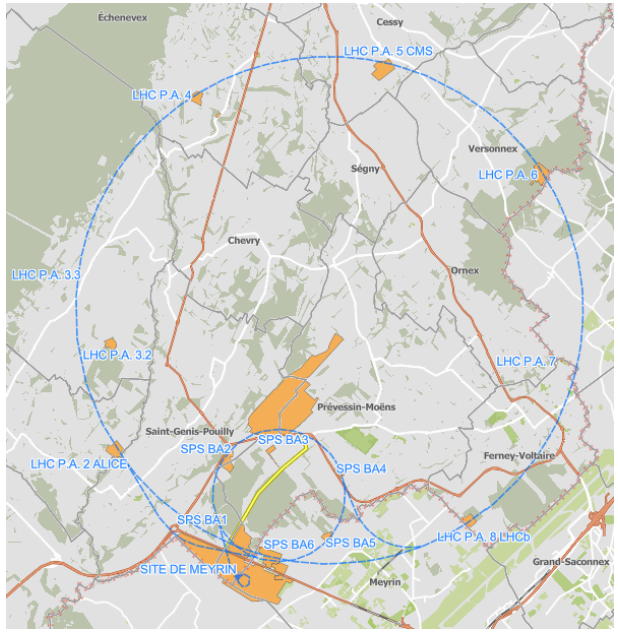
The Large Hadron Collider (LHC)

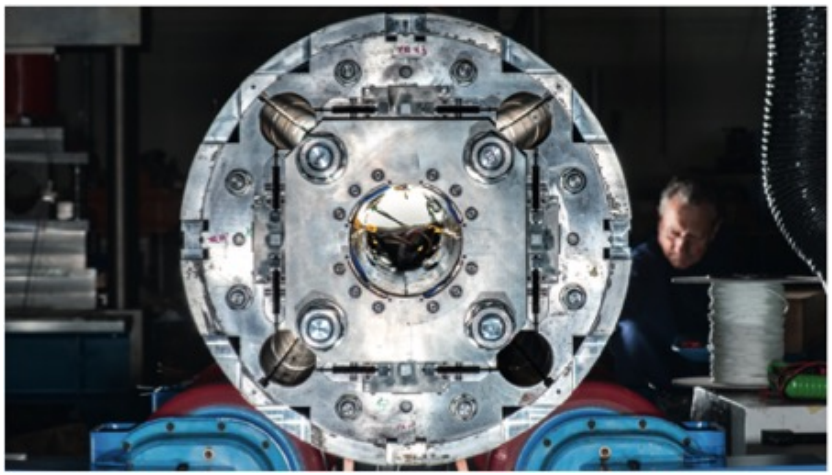
- Accelerator and collider of protons and ions. Built in the 27 km tunnel of LEP, buried ∼100 m underground.
- Counter-rotating two beams at 6.8 TeV in Run-3 (2022–2026)
- Bunch structure: 2808 bunches, 25 ns spacing.
- Four major detectors (ATLAS, CMS, LHCb, ALICE) at IPs.
- Physics reach covers from Higgs couplings to TeV-scale BSM searches.





The High Luminosity LHC (HL-LHC)

- Following Run-3, we will enter Long Shutdown 3 (LS3) period until 2029.
- Instantaneous luminosity[1] $\times$ 5-7.5
- Finally reaching to 7 TeV/beam ($\sqrt{s} = 14$ TeV).
- HL $\Longrightarrow$ higher radiation damage and more pile-up interactions
  - Detectors with better radiation hardness, timing resolution, and granularity.
- Accordingly, many upgrades to the detectors and electronics.

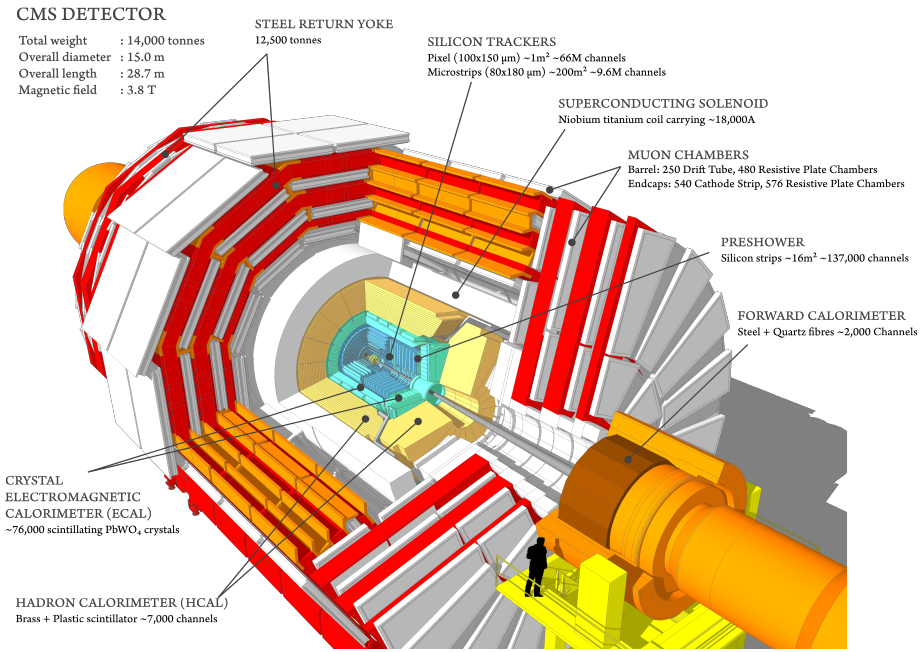


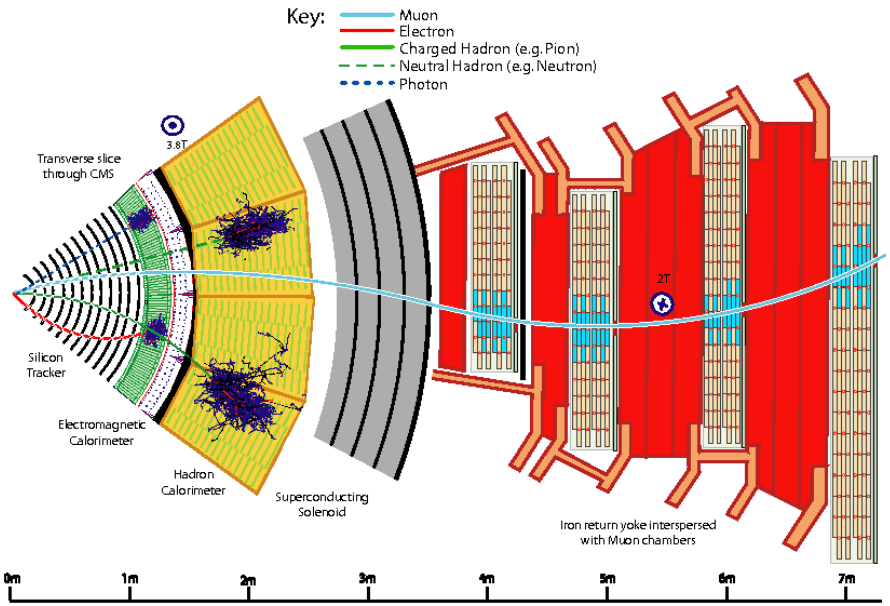
12 more powerful quadruple magnets to provide final focusing before collisions.

[1] rate of collisions per unit of cross section

The Compact Muon Solenoid (CMS)

- General-purpose detector. Discovery of the Higgs boson
- Superconducting solenoid of 6 m inner diameter, 3.8 T magnetic field.
- $|\eta| \leq 1.479$ barrel, $1.479 < |\eta| < 3.0$ endcaps.
- Gas-ionization detectors outside the solenoid.



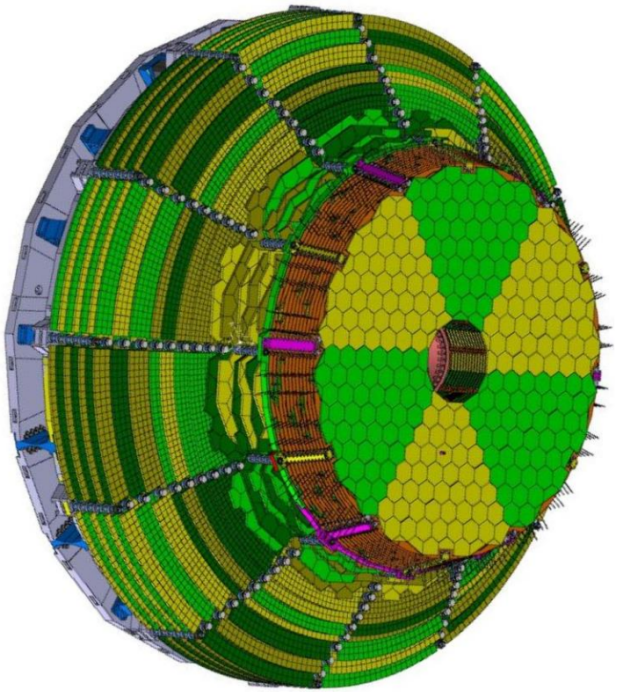


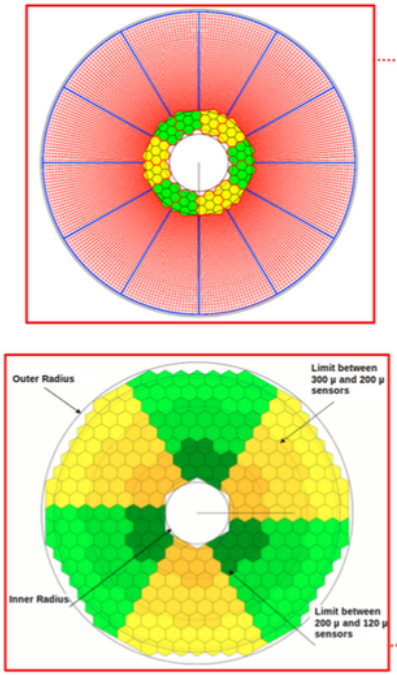
High Granularity Calorimeter (HGCAL)

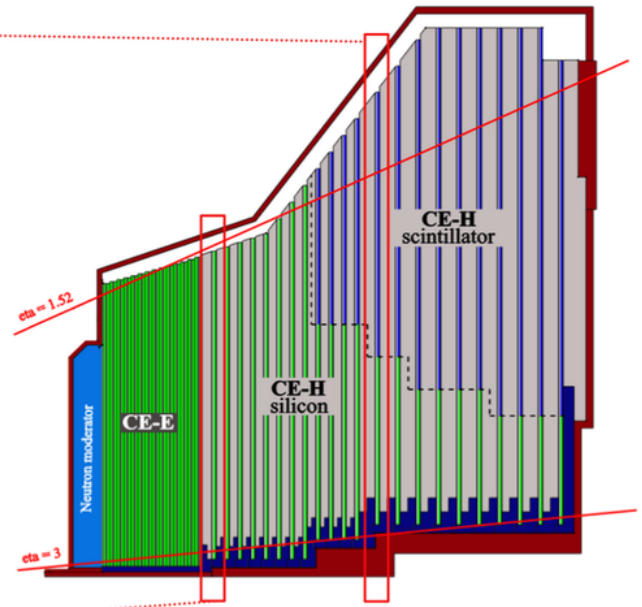
- Heavily irradiated calorimeter endcaps of CMS needs to be replaced.
- Higher radiation tolerance needed for HL-LHC and better resolution.

$\Longrightarrow$ Silicon sensors and Scintillator tiles + SiPM

- Absorber plates for interleaving: CE-E lead, CE-H steel.

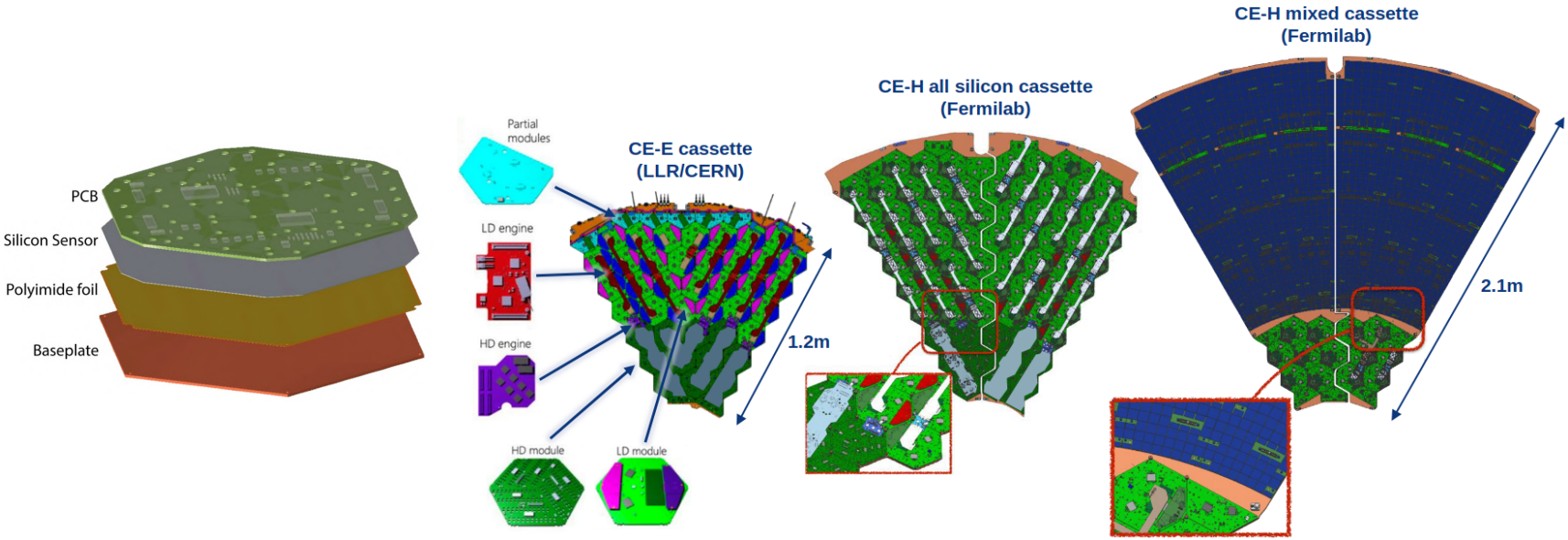






47 layers!!!

So... what do we do?



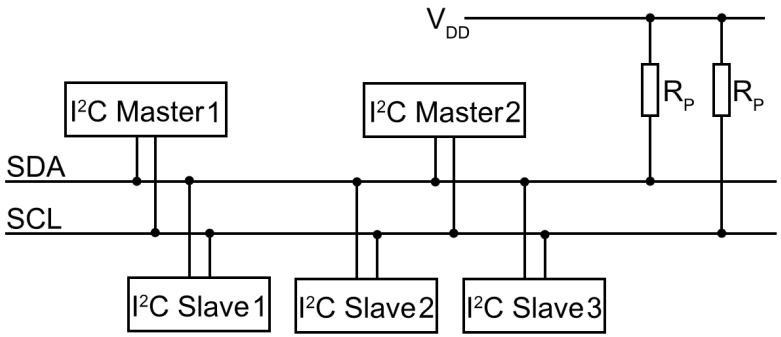
And... what do I do?

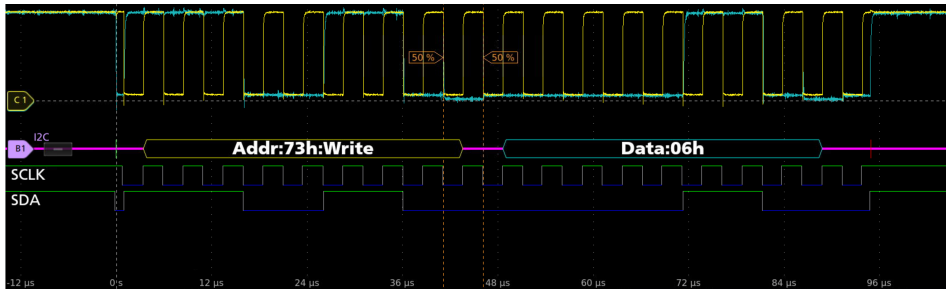
- HGCAL will be composed of many hexamodules (hence hexaboards).
- Clearly, they need to pass certain amount of tests:
  - visual inspection
  - electrical test
  - charge injection test
  - cold room tests
- Thus, we need to develop a test system!!!
  1. Single module test system
  2. Multimodule test system $\Longrightarrow$ multiplexer board

$\Longrightarrow$ This requires hardware, firmware, and software development.

Last piece of info: Inter-Integrated Circuits (I^2C)

- Communication bus/protocol
  - Serial[2] (*not parallel*)
  - Synchronous by a periodic "clock" signal
  - Multi-target / bidirectional
- SDA (serial data), SCL (serial clock), GND (ground), V_{DD} (positive supply voltage)





[2] bits are sent sequentially on a given wire

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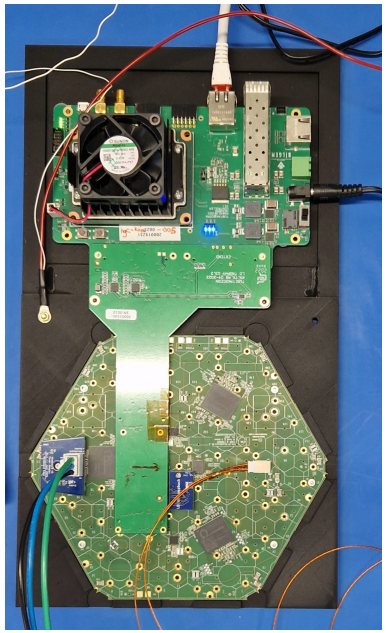
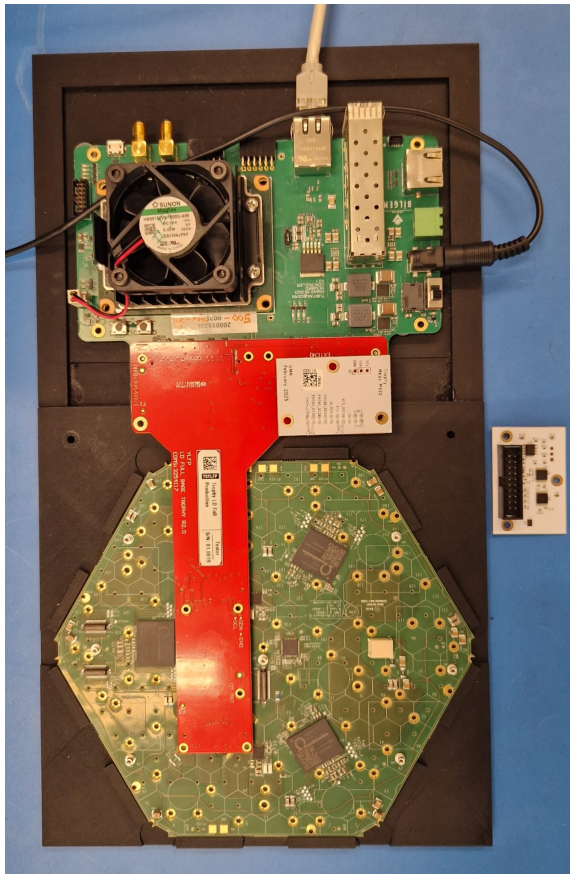
Electrical Tests at Point 5

- Single module testing shifts at P5 for two weeks
- Throughput dropped due to trophy-connector wear
- Hands-on with testing software & GUI, KRIA controllers, I^2C issues



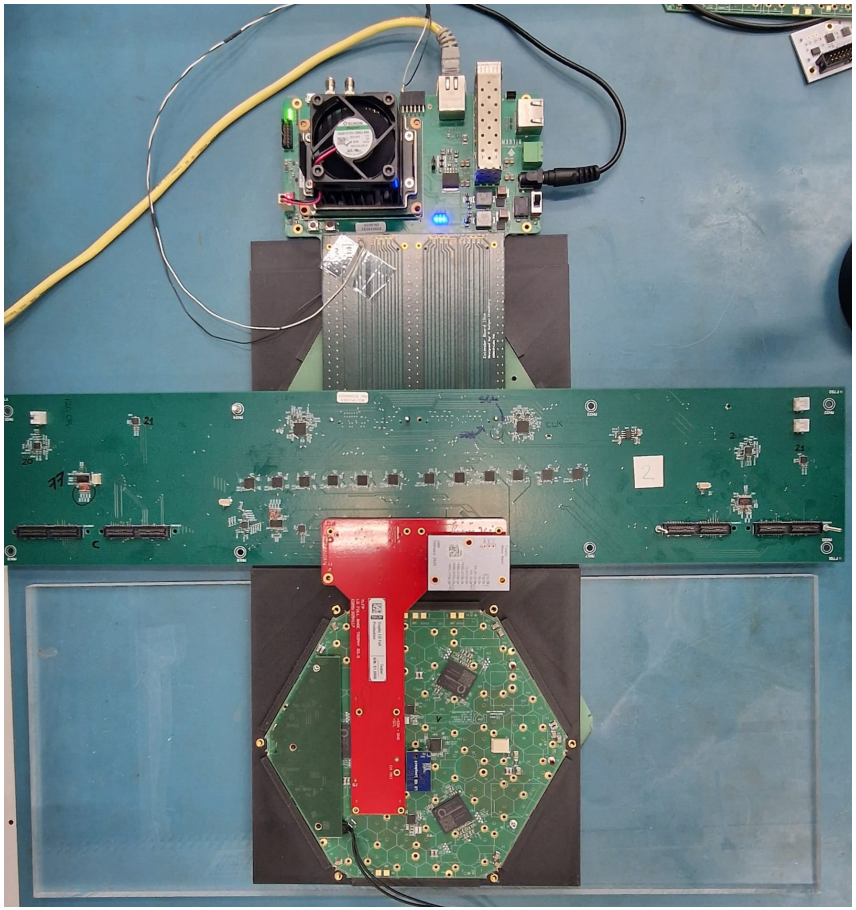
New LD Trophies

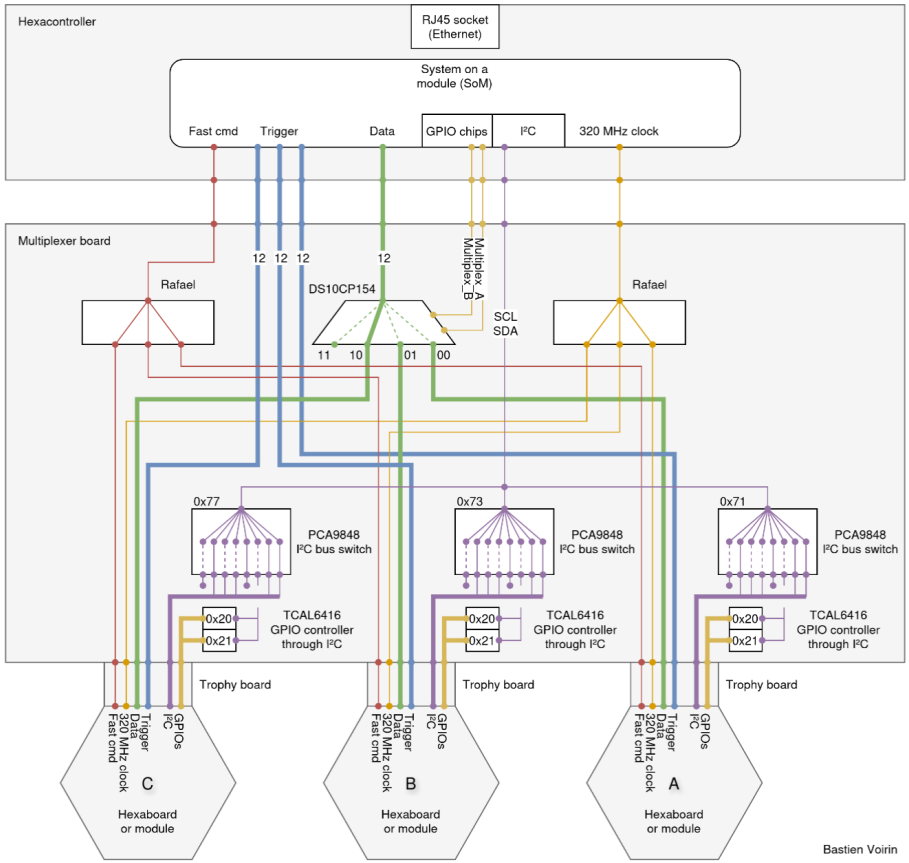
- Same pin-out as the HD trophies
  - $\Longrightarrow$ Chance to work with LD boards and v3c ROCs in the multiplexer.
  - $\Longrightarrow$ Better hw/fw compatibility
- Mezzanine added.
  - All the important components are on the mezzanine.
  - EEPROMs are added.
  - The trophy only has the connections/pins.
  - New control points added.
- Adapted the single module test system to the new trophies.
  - ! Urgent due to arrival of new boards and modules
  - Required multiple changes in the client and server scripts.



Multiplexer Board

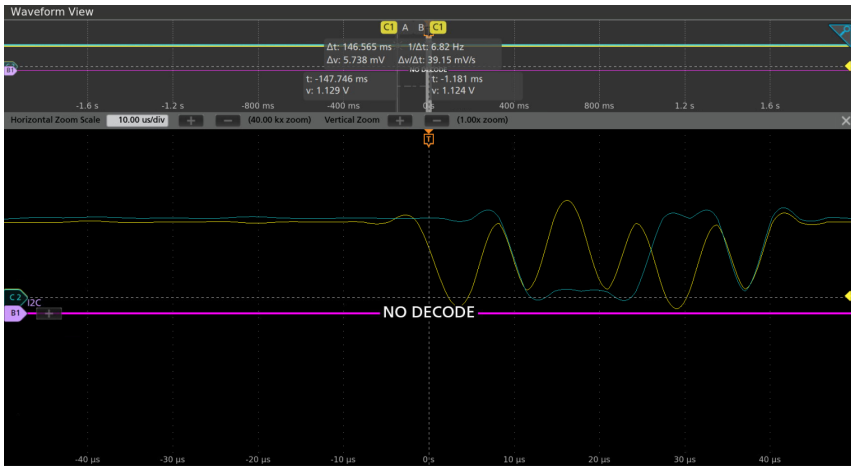
- 3 slots
- Development only with HD hexaboards

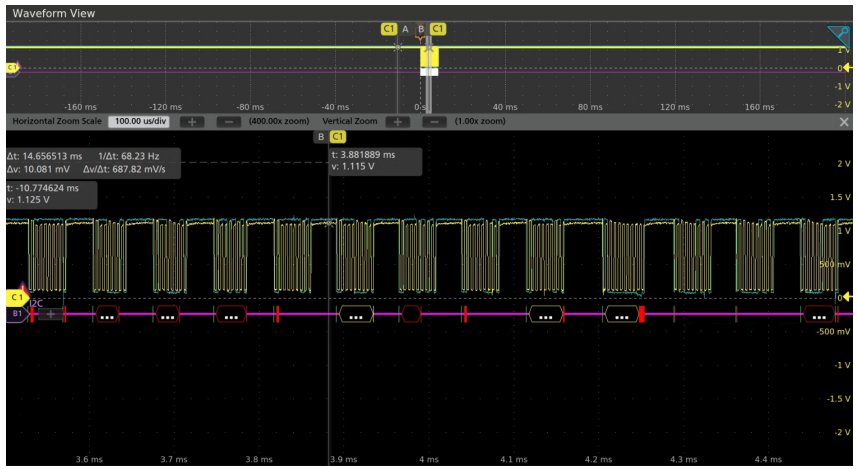




A first look into multiplexer

- I^2C were highly unstable.
- Pull-up resistors seemed fine. Problems expected to arise from firmware.
- Initially restricted to work on slot A.

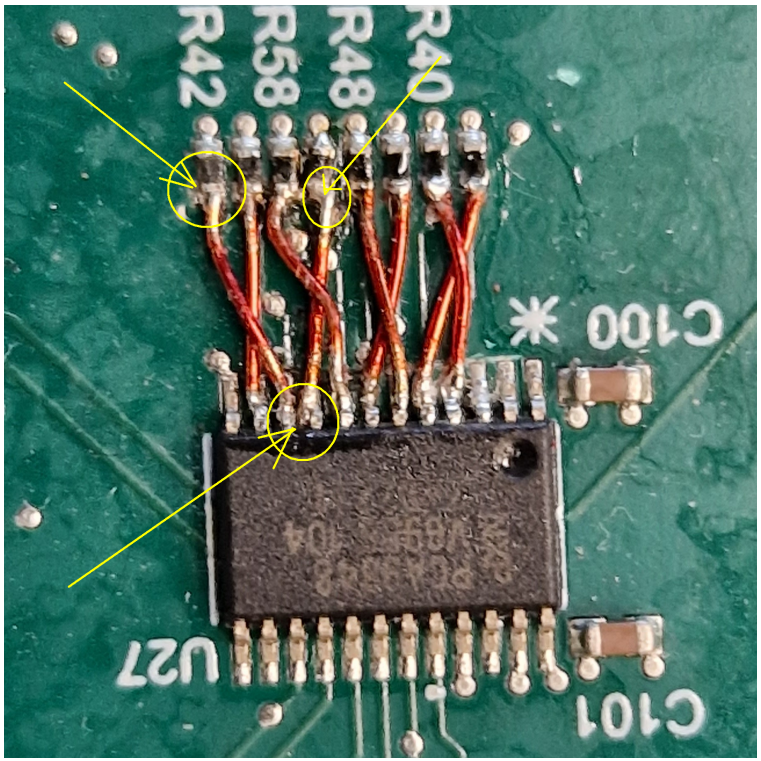


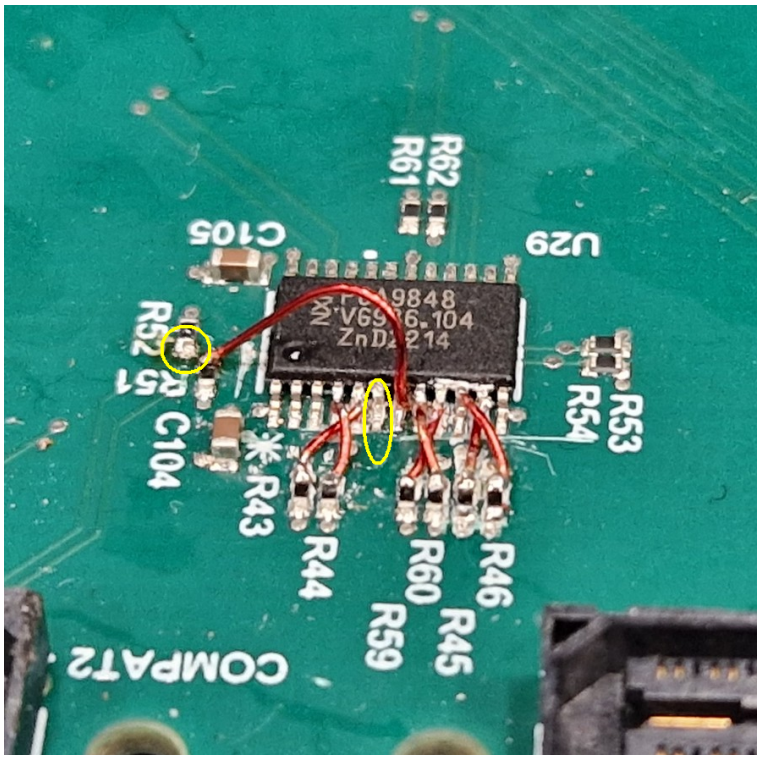


- Firmware updates (Feb $\rightarrow$ May 7) solved the I^2C issues.

Slot B/C

- Diagnosed some hardware issues on other slots. (Similarly on the sister board)

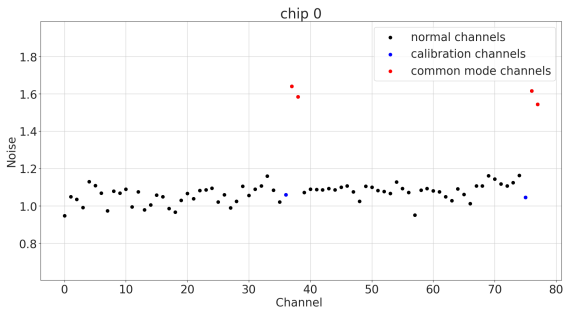


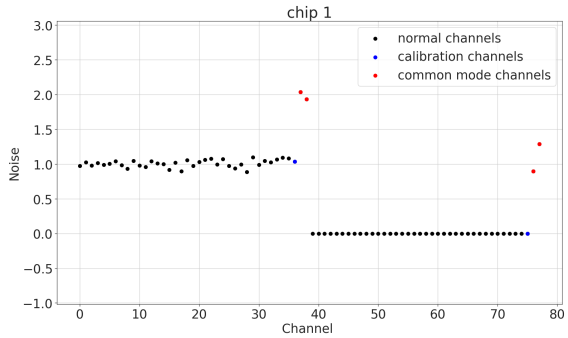


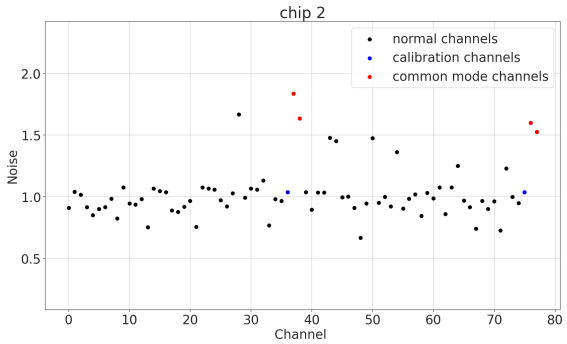
- After repairs, I^2C became VERY stable!!!
- For the first time, ADCs, EEPROMs, and ROCs are *co-visible*!!!

Configuring ROCs and aligning links (back to slot A)

- As I^2C ready, let's configure the ROCs!
- Initially seemed to work, but a closer look showed that FCMD signal is very unstable and noisy.
- Firmware update (May 7 $\rightarrow$ May 14).
- Corrected config yaml files (ROC Top modifications and polarity corrections).
- Finally, links are all aligned!!!
- So... let's take some data! Results from single module testing are retrieved for this board. ✓

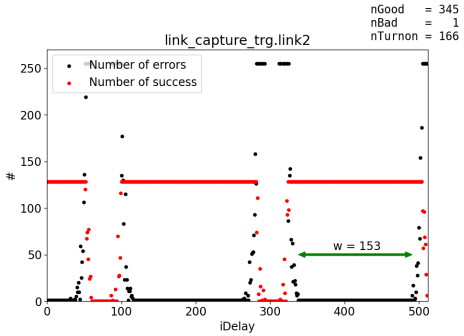




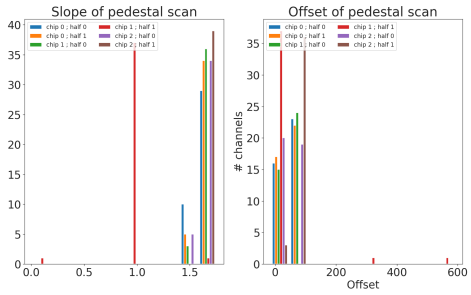


Attempt to make things plug-and-play

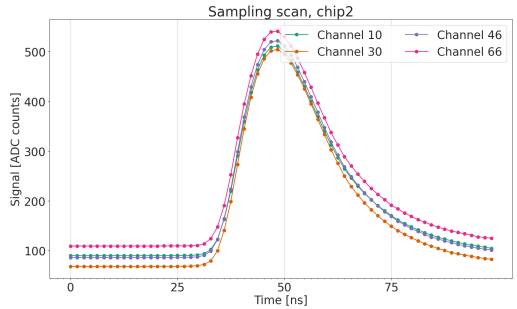
- Configuration/initialization remotely and automatically.
- Drastically reduced the print lines for future debug searches.
- Pedestal run and many others are available through the mux board.
- Not all...(e.g., probeDC) Hardcoded addresses and missing methods!



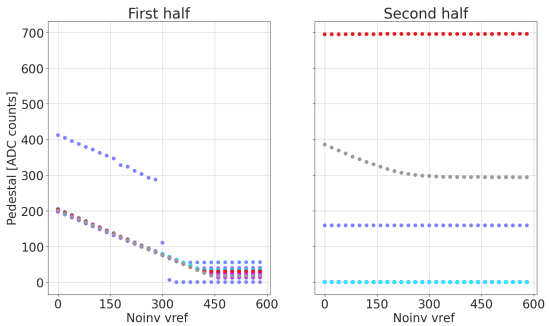
Delay scan example



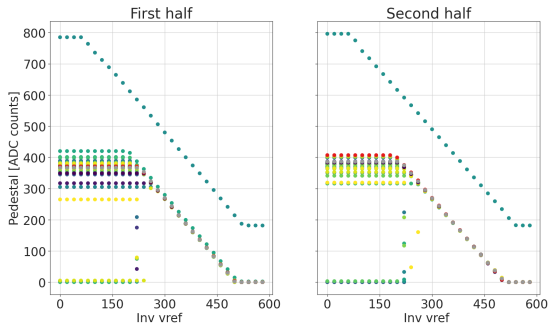
Pedestal scan example



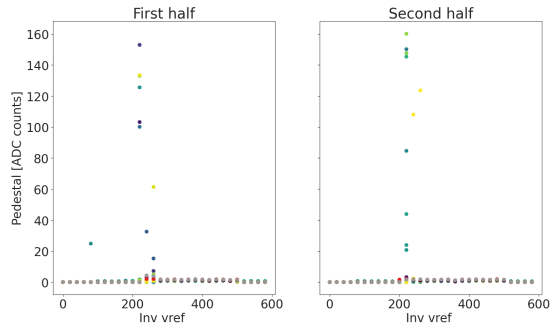
Sampling scan example



Pedestal vs. $V_{refnoinv}$



Pedestal vs. V_{refinv}

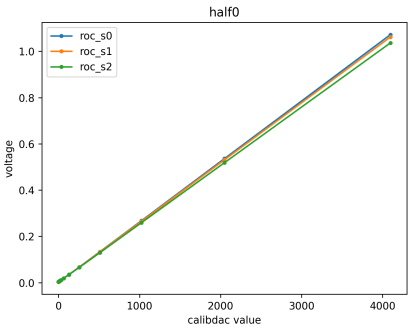


Noise vs. V_{refinv}

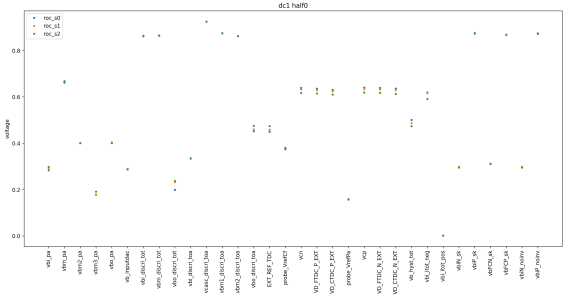
ProbeDC is ready!

- Trickshot: `i2cset -y 2 0x71 0x06`. Device tree is elegant but long.

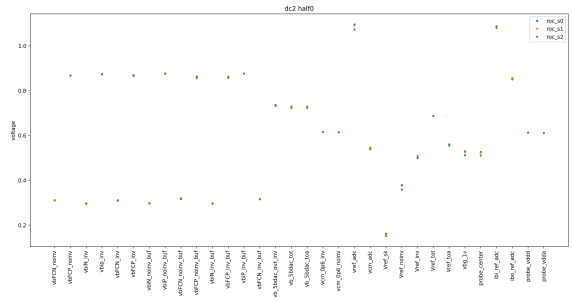
```
     0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
00: -- -- -- -- -- -- -- -- 08 09 0a 0b 0c 0d 0e 0f
10: -- -- -- -- -- -- -- -- 18 19 1a 1b 1c 1d 1e 1f
20: -- -- -- -- -- -- -- -- 28 29 2a 2b 2c 2d 2e 2f
30: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
40: 40 -- -- -- -- 45 -- -- -- -- -- -- -- -- -- --
50: -- -- -- -- -- -- 56 -- -- -- -- -- -- -- 5e --
60: -- -- -- -- -- -- -- -- -- -- -- -- -- -- -- --
70: -- 71 -- 73 -- -- -- 77 -- -- -- -- -- -- -- --
```



Calibdac half0



DC1 half0

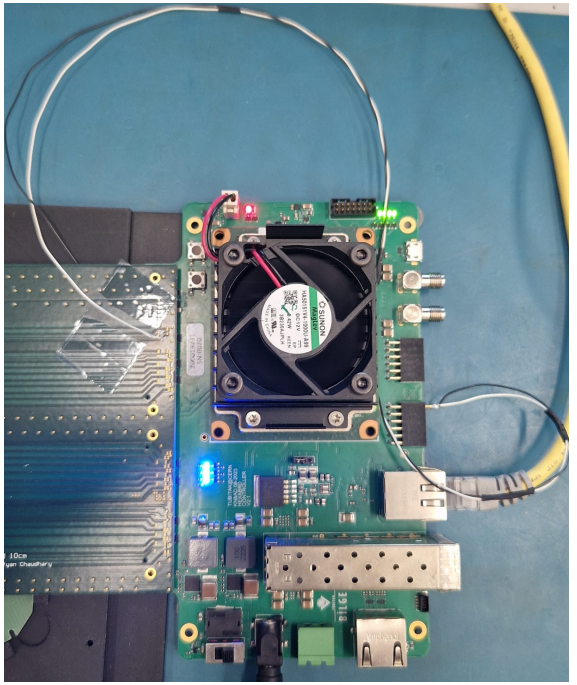


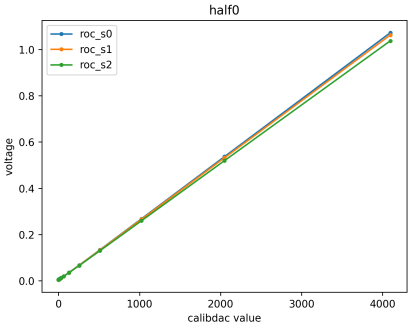
DC2 half0

A first look into multiplexing: slots B/C

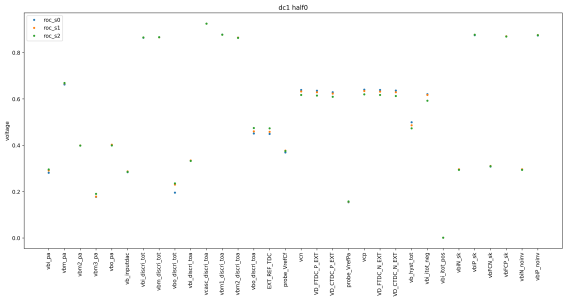
- A hardware and firmware hack.
- On slot B: ProbeDC ✓, Pedestal run ✗.
- Definetely a fast-sector problem.
  - Configuring & aligning links is not working.

21/06: Configuring is achieved. Alignment problems are diagnosed.

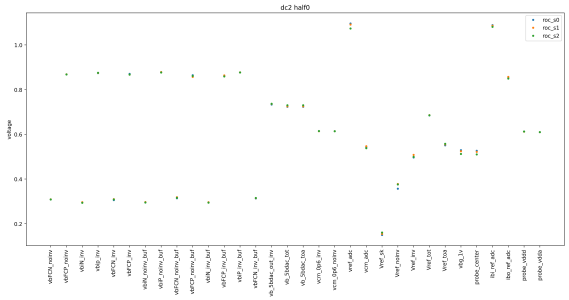




Calibdac half0



DC1 half0



DC2 half0

An optimistic picture of the future

- Solve the alignment problems!!!
- Perform all the tests for a single hexaboard through slots B/C of the multiplexer.
- Insert 2 (and 3) boards to the multiplexer and make sure that both the slow and fast sectors work correctly.
  - Powering these board may be cumbersome.
- Be able to run all the tests on the multiplexer board with mutliple hexaboards.
- Adapt/implement GUI for the era of multimodule testing.

End...

Thank you for listening! Any questions?