PBR Radio Instrument: DAQ

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Outline

1. Overview
2. Boards Procured
3. Initial Tests
4. Next Steps

Overview: Digram

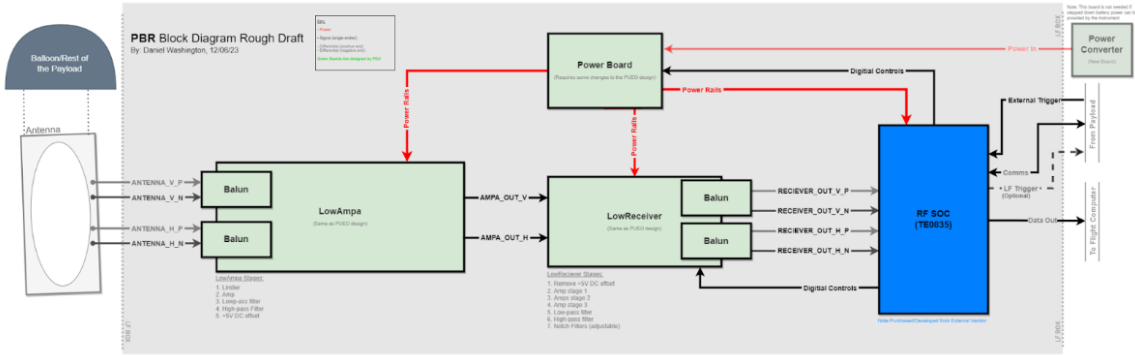


Diagram by D. Washington (PSU)

RFSoC General Idea: ADC+DAC, FPGA, PS in one chip

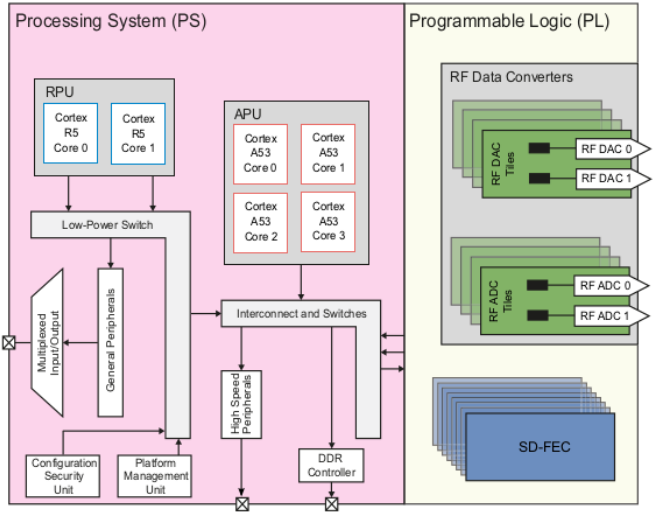


Figure from RFSoC Book

- RF Data Converters:
  - ADCs (up to 16): 12/14-bit up to 5.0 GSa/s;
  - DACs (up to 16): 14-bit up to 9.85 GSa/s;
- PL – FPGA;
- PS:
  - Quad-core Arm Cortex-A53 – Operating System (PetaLinux, PYNQ);
  - Dual-core Arm Cortex-R5 Real-Rime Processor – Low-Level Real Control.

Overview: RFSoC Board

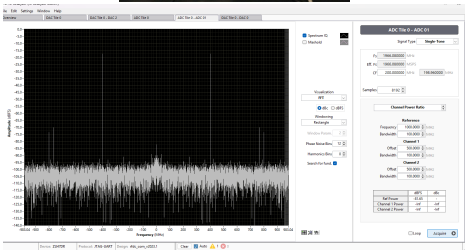
- Main board – KRM-4Zu47DR produced by Knowledge Resources;
- Chip: xczu47dr-fsvg1517-1-e;
- 8 x ADC + 8 x DAC
- RAM: 2 x 8GB PL + 8G PS;
- Trigger: External + Internal;
- Power: 6A at 12V Maximum; ∼4A at 12V Realistic;
- Communication with main instrument: Ethernet;

Boards Procured

2 kits are now at UD. One for PSU.

- Each kit consists of: K**KRM-4ZU47DR 3x 8GB RAM -1E** board and **KRC-4700 Kit 6GHz** carrier board;
- Simple assembly (installing heat sink and fan) was required;

Initial Tests



- Pre-built bit-stream with "RF Analyzer" project was used (specific version of Vivado is required);
- Boot from SD-card (PetaLinux image);
- Communications with the carrier board – over serial;
- Communication with RFSoC – over JTAG;
- All 8 DACs and ADCs were tested: DAC0-ADC0, DAC1-ADC1, ..., DAC7-ADC7;

Next Steps

Short Term

- Memory Tests;
- Clock Distribution;
- Interfaces;
- PYNQ functionality;
- Power Consumption;

Longer Term

- Carrier board design (PSU);
- Trigger;
- Data handling;
- Machine Learning (??): denoising, classification.