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37th international JEM-EUSO Collaboration meeting

MIZAR ASIC

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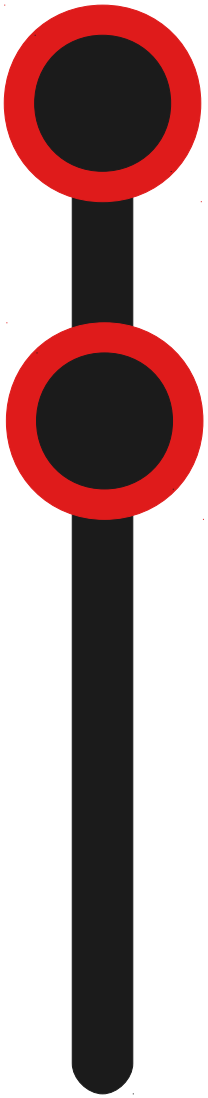
Production and ASIC test

The MIZAR chip has been delivered to INFN Torino

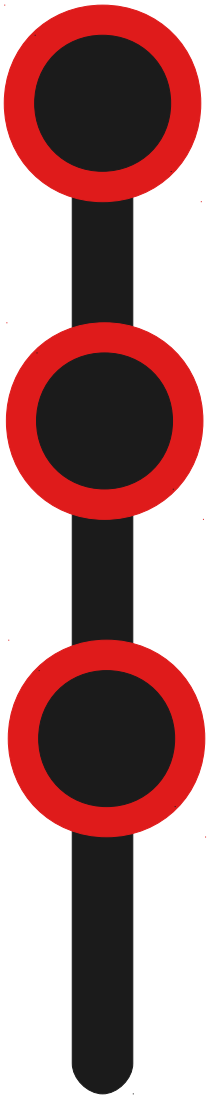
Production and ASIC test



The MIZAR chip has been delivered to INFN Torino

The test board has been delivered to INFN Torino

Production and ASIC test

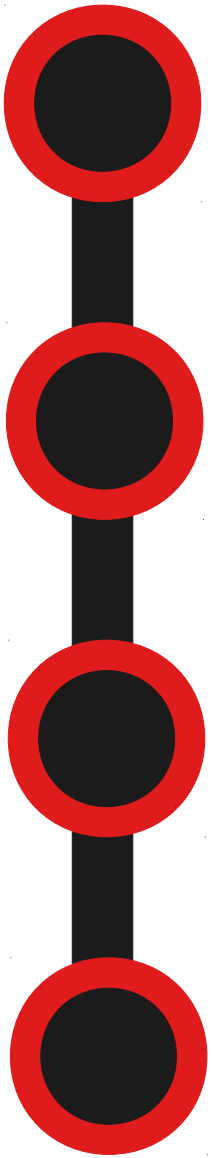


The MIZAR chip has been delivered to INFN Torino

The test board has been delivered to INFN Torino

The MIZAR chip has been bonded on the test board

Production and ASIC test



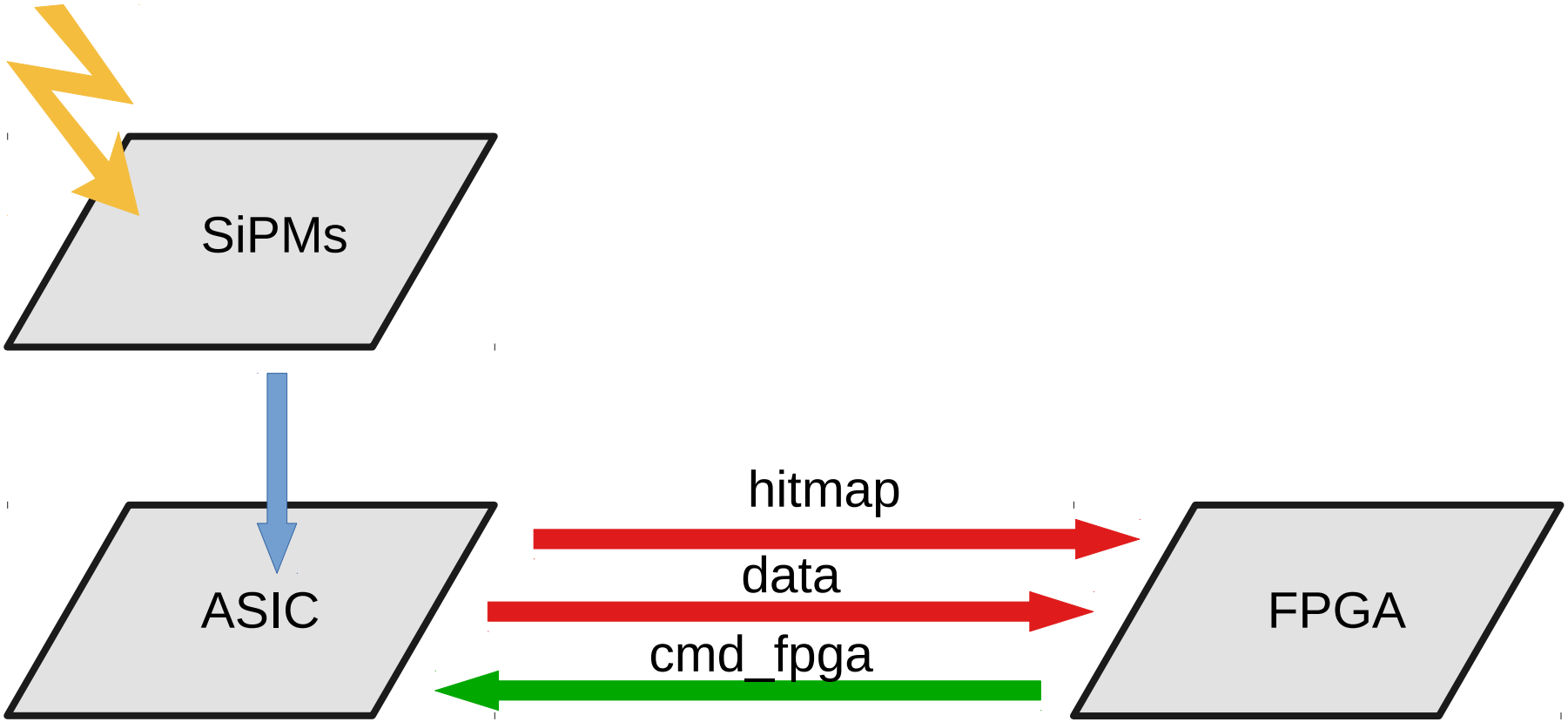
The MIZAR chip has been delivered to INFN Torino

The test board has been delivered to INFN Torino

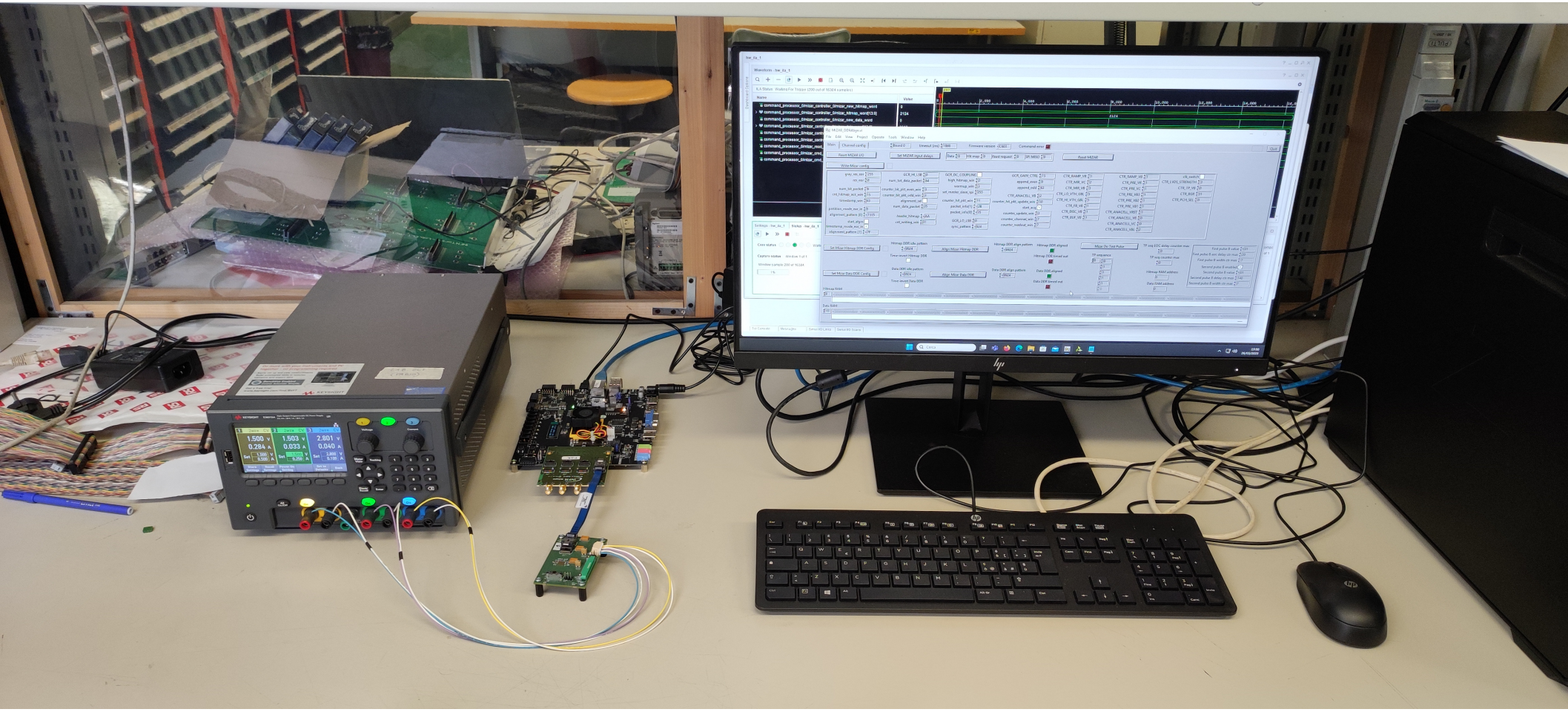
The MIZAR chip has been bonded on the test board

Preliminary tests: neither open nor short circuits

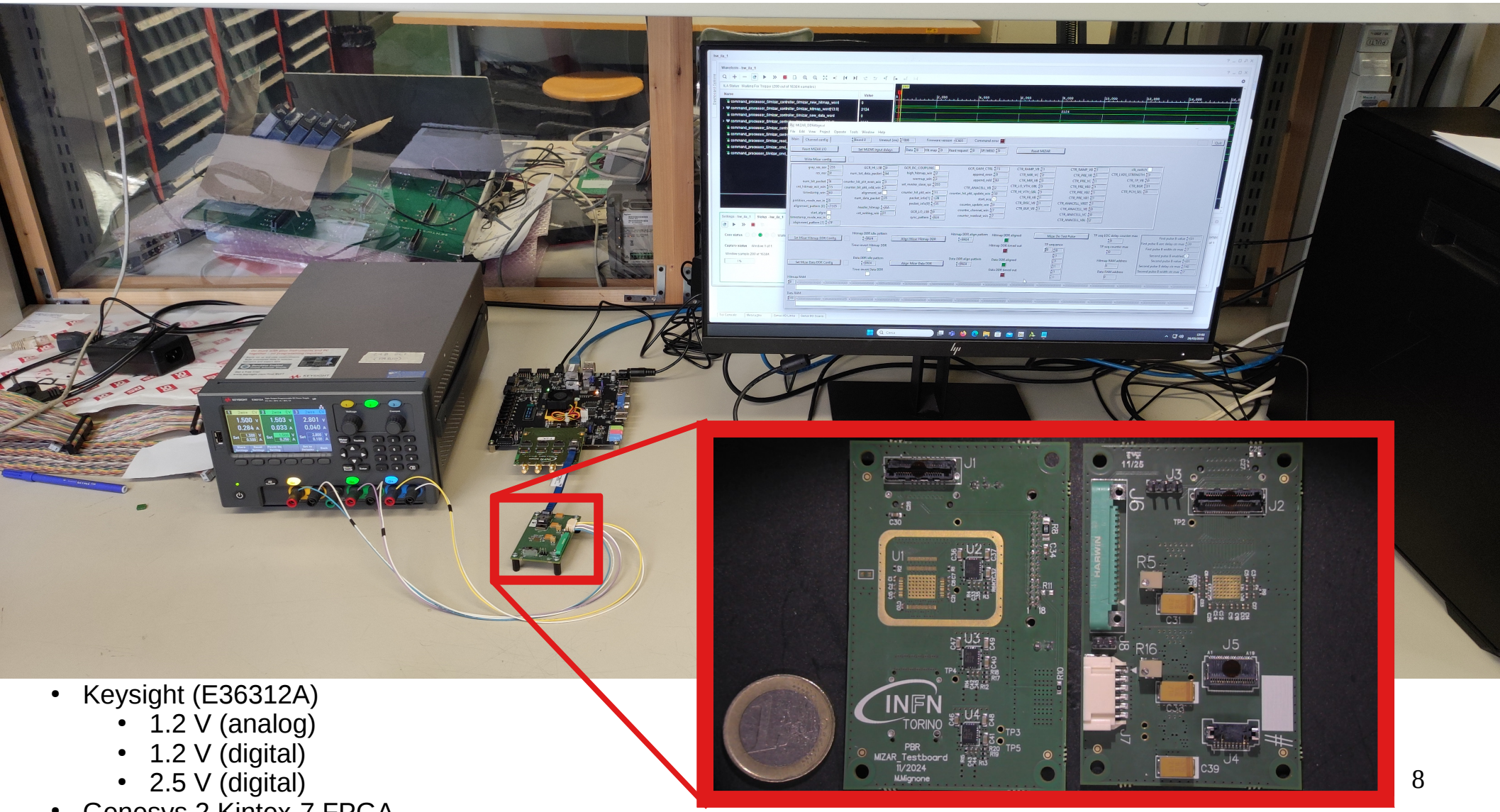
Data flow



Testing - setup



Testing - setup



- Keysight (E36312A)
  - 1.2 V (analog)
  - 1.2 V (digital)
  - 2.5 V (digital)
- Genesys 2 Kintex-7 FPGA

Testing


200
400
600
800
1,000
00100100100100
00100100100100
00100100100100
TP

Testing


200
400
600
800
1,000
00100100100100
00100100100100
00100100100100
Hitmap request
from FPGA

Testing

Hitmap transmission to the FPGA

Testing


200
400
600
800
1,000
00100100100100
00100100100100
00100100100100
Data request
from FPGA

Testing

Data conversion (8 bits resolution)

Testing

Data transmission to the FPGA

Summary of the preliminary results

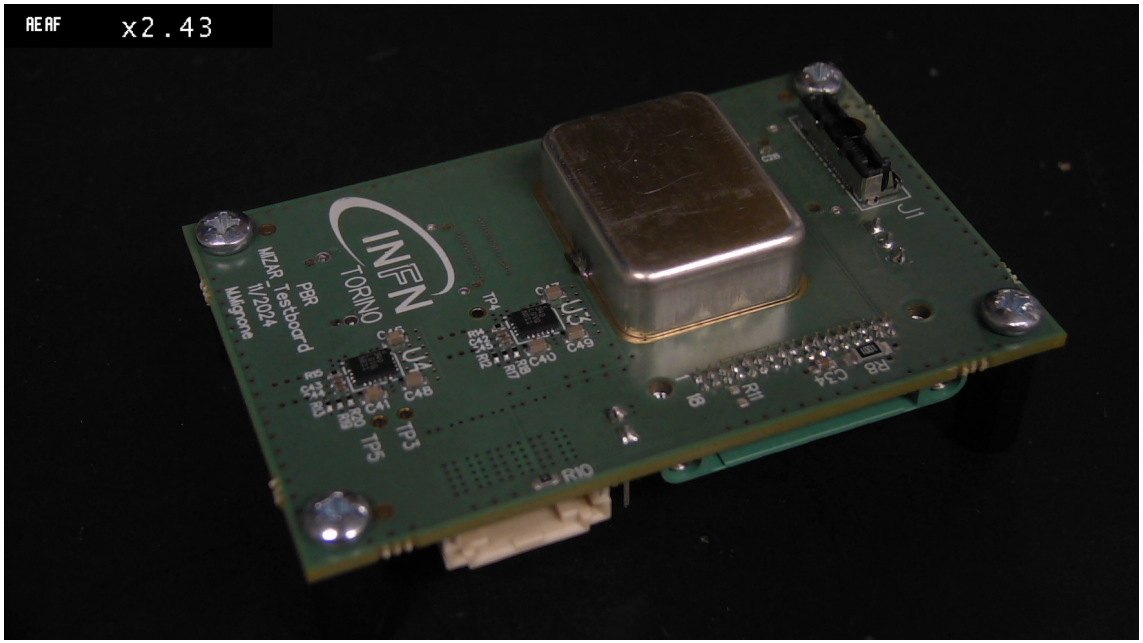
TEST	RESULT
Writing/reading of the registers by SPI	✓
Hitmap generation request by FPGA	✓
Hitmap structure validation	✓
Hitmap transmission to FPGA	✓
Pixel masking	✓
Data generation request by FPGA	✓
Data transmission to FPGA	✓
Data structure validation (64 channels, 32 cells partition, 8 bits resolution)	✓

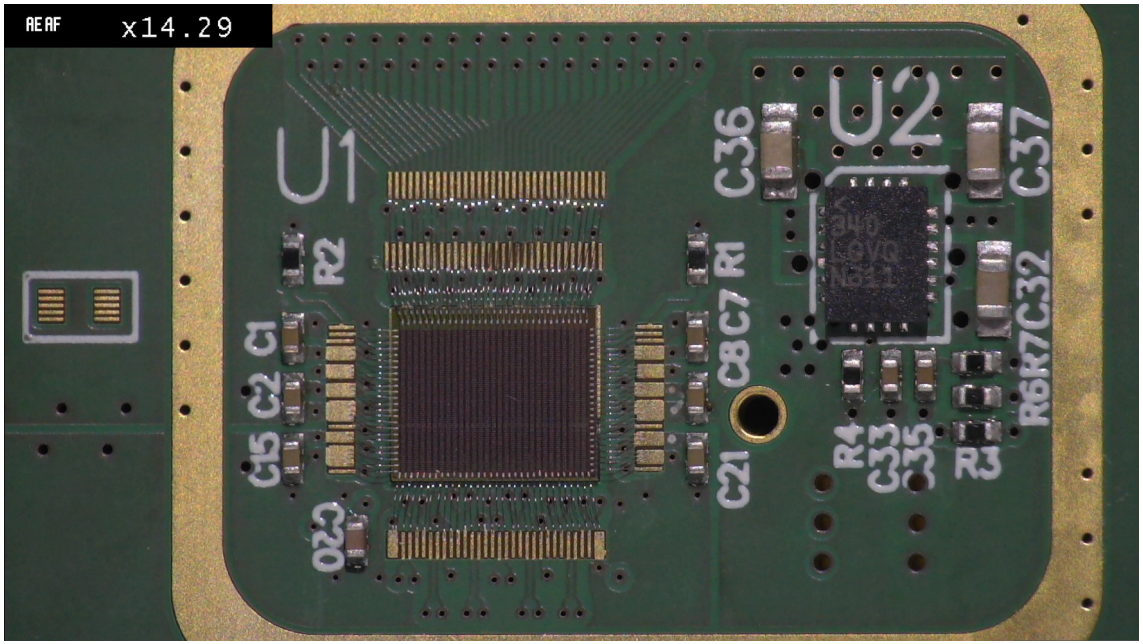
Next steps

Roadmap
Test pulse (TP) configuration
Data analysis with TP stimulus
Channel calibration
Exploring more configurations

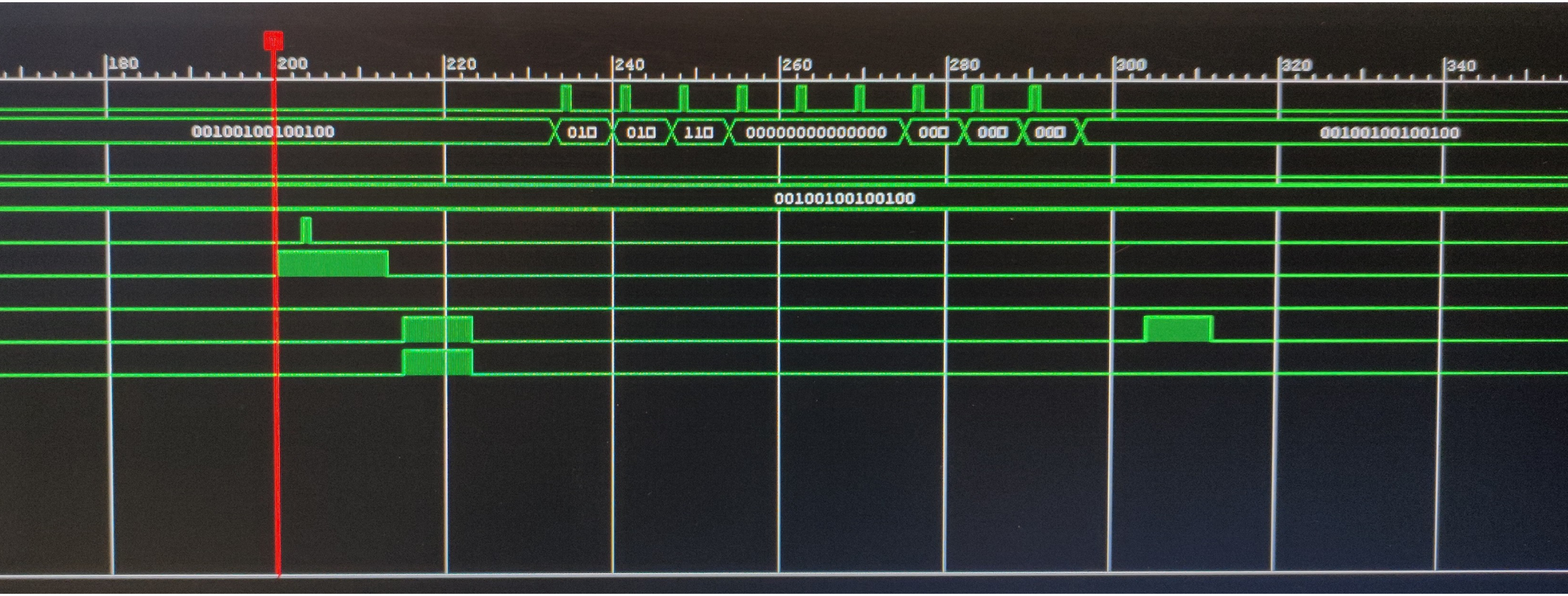
EOF

Testing - setup





Testing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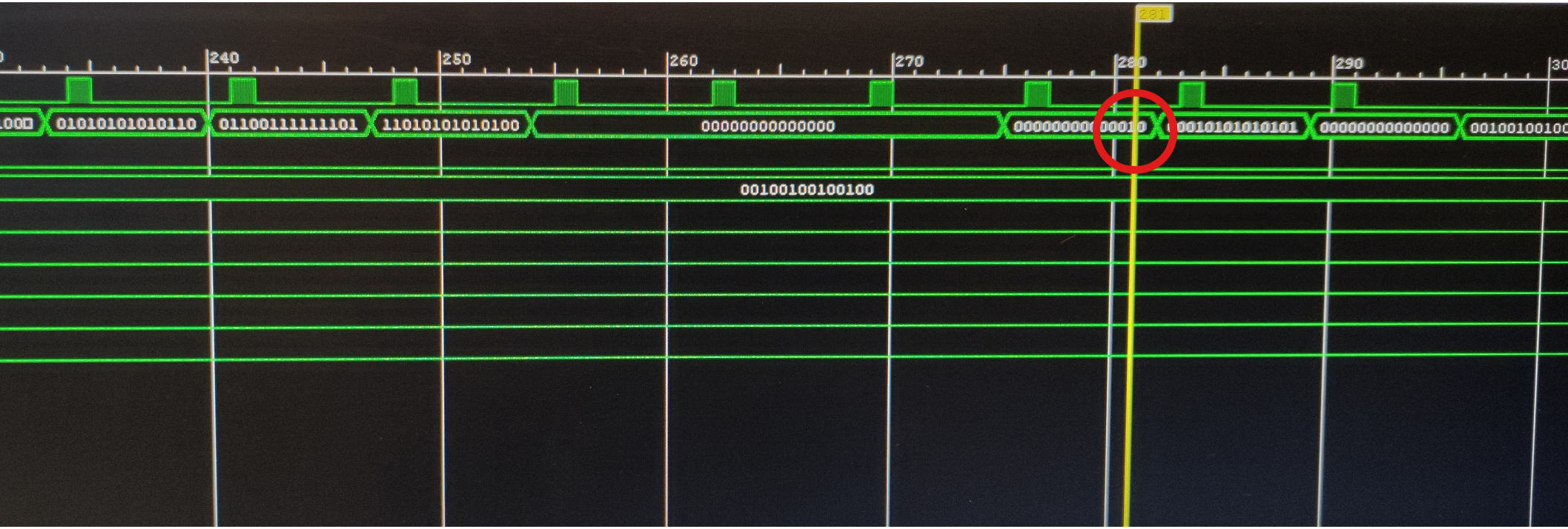
Testing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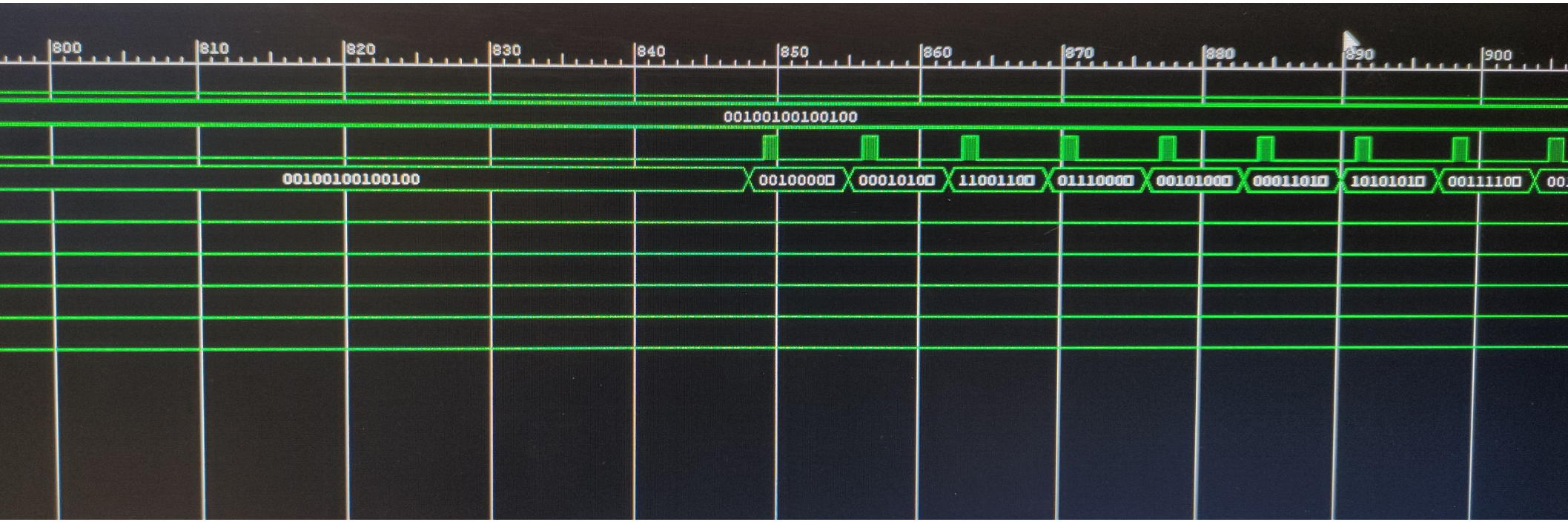
011001111111101
110101010100100
000000000000000
001001001001001

Testing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00011010
10101010
00111100