The Arcadia R&D project: CMOS Fully depleted MAPS for FCC

Binational conference on Detector R&D

18-20 November 2025, LPNHE, Paris

Davide Falchieri

INFN Bologna, Italy

on behalf of the **ARCADIA collaboration**

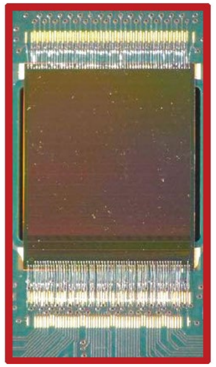
Arcadia FD-MAPS R&D at INFN

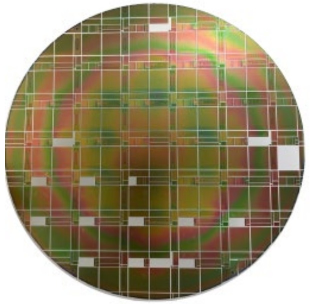
ARCADIA:

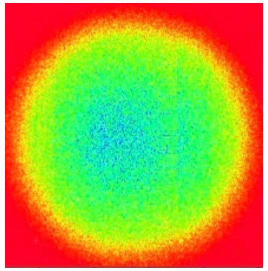
Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

CMOS sensor design and fabrication platform on LF11is technology:

- sensor R&D and technology, CMOS IP Design, Chip Integration and Data Acquisition
- main Demonstrator full-chip FDMAPS for Medical (CT), Future Leptonic Colliders and Space Instruments
- scalable FD-MAPS architecture with very low-power
- custom BSI process allow to develop fully-depleted thick sensors (400µm) for X-ray imaging
- fully-depleted monolithic active micro strips with fully-functional embedded readout electronics
- ongoing R&D for the implementation of monolithic CMOS sensors with gain layer for fast timing

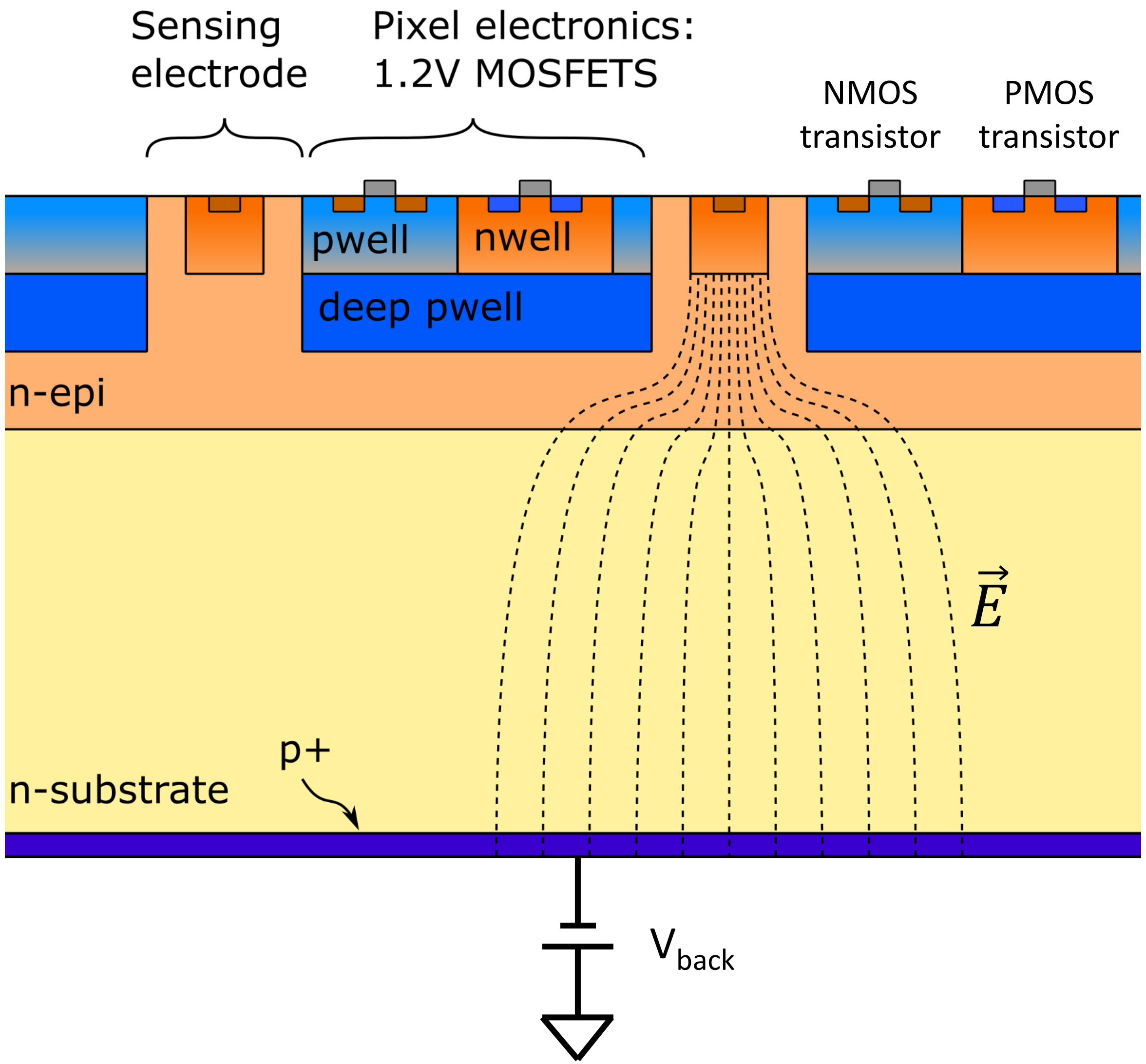






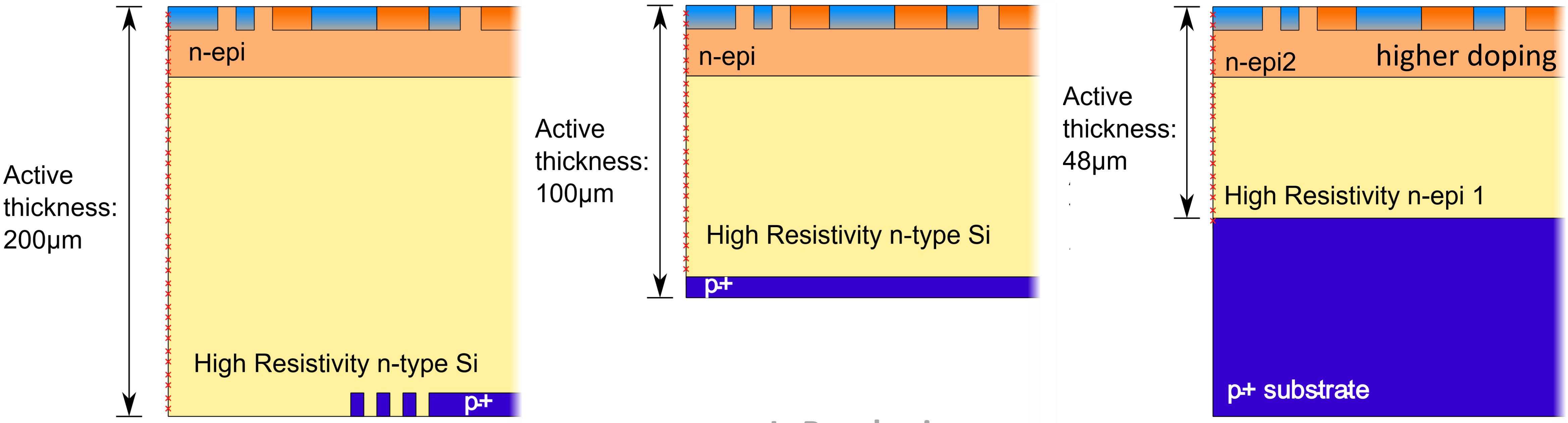
Sensor concept

- n-type **high resistivity** active region
- reverse-biased **junction at the bottom**: depletion grows from back to top
- **n-epi** layer: reduce **punch-through** current between p+ and deep pwells
- **sensing** electrodes can be biased at **low voltage** (< 1V)
- nwells and pwells with electronics shielded by **deep pwells**
- operation in **full depletion** with fast charge collection by **drift**
- **small collecting electrodes** for optimal SNR
- compatible with standard CMOS fabrication process
- technology: **LF11s 110 nm CMOS node** (quad-well both PMOS and NMOS), high resistivity bulk



Sensor concept and substrates

HR wafers – backside lithography | HR wafers - no backside lithography | p+ wafers - double epi



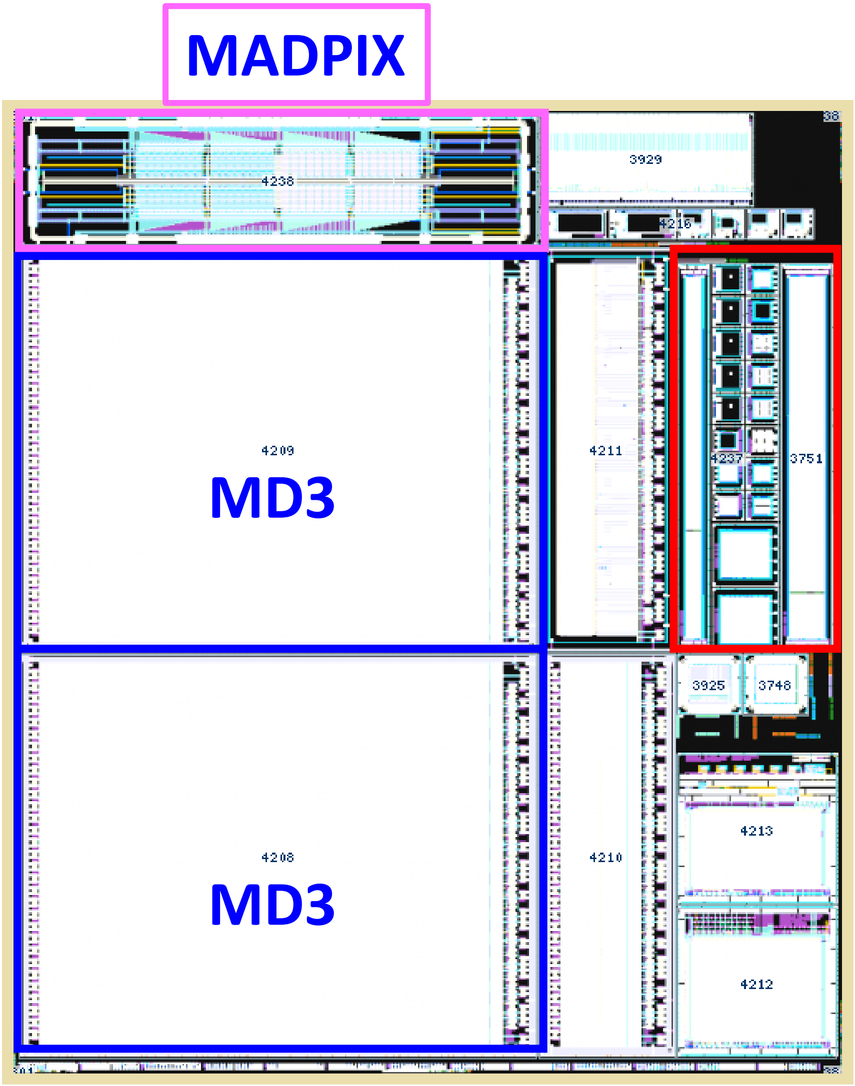
L. Pancheri

post-processing: thinning, then backside **p+ implantation** and laser annealing,
patterning on the backside to prevent junction breakdown

post-processing: thinning, then back-side **p+ implantation** and laser annealing,
no patterning on backside

p+ starting substrate:
thinning down to a 100 μm total thickness,
active thickness below 50 μm

Arcadia technology demonstrators

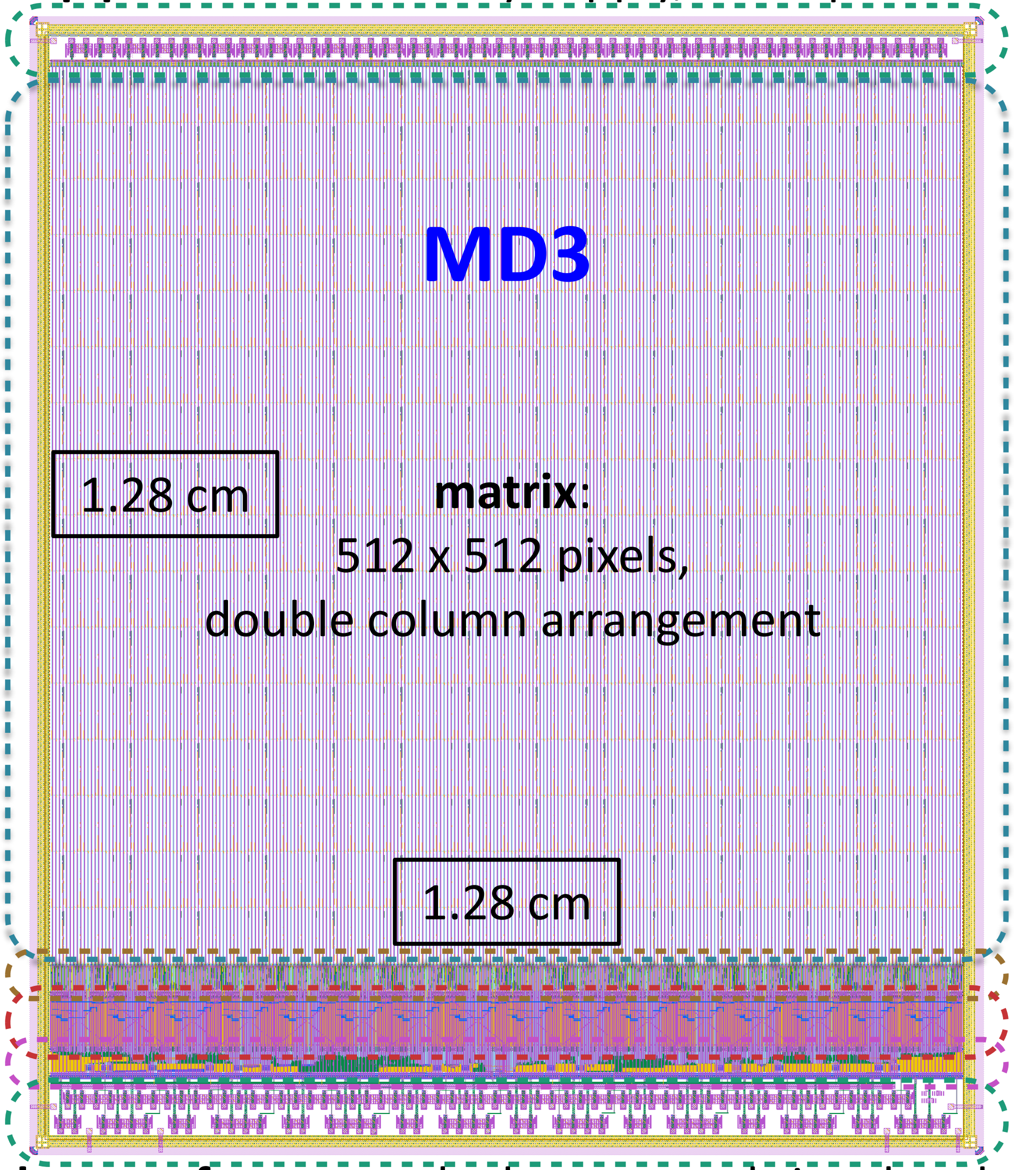


List of produced devices:

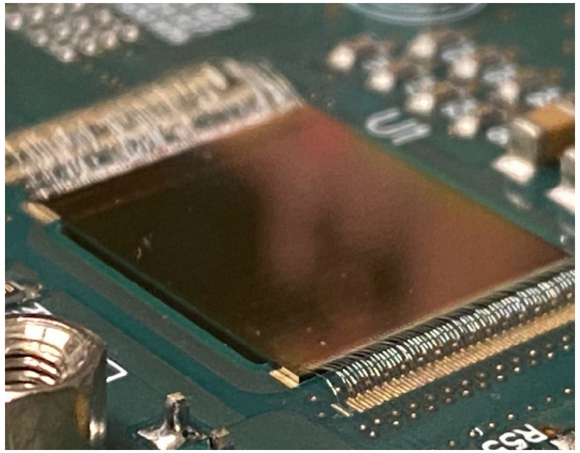
- **main demonstrator MD3**: pixel detector - **512 x 512** 25 µm by 25 µm pixels array
- small **pixel arrays** with different **pitch** (10 µm – 25 µm – 50 µm) with and without active readout
- **strip detectors** with and without active readout
- ASTRA 64-channel ASIC for Si-strip readout
- **test structures** for sensors characterization and process qualification
- **MATISSE** low power (ULP front-end for space instruments)
- **HERMES**: small-scale demonstrator for fast timing
- X-ray multi-photon counter
- **MADPIX**: CMOS LGAD multi-pixel active demonstrator chip for fast timing

Arcadia Main Demonstrator MD3: chip floorplan

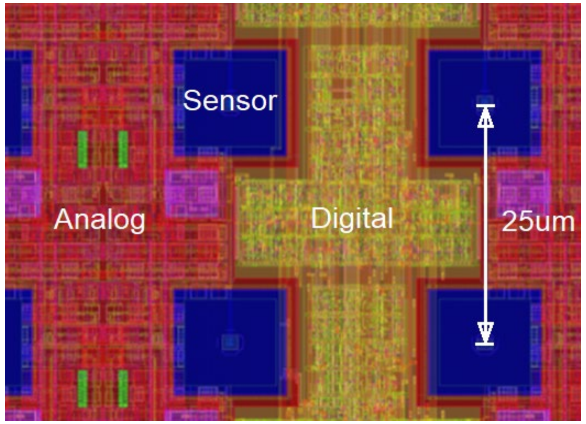
top padframe: auxiliary supply, IR drop measure



bottom frame: stacked power and signal pads



512 x 512 pixel sensor bonded on PCB



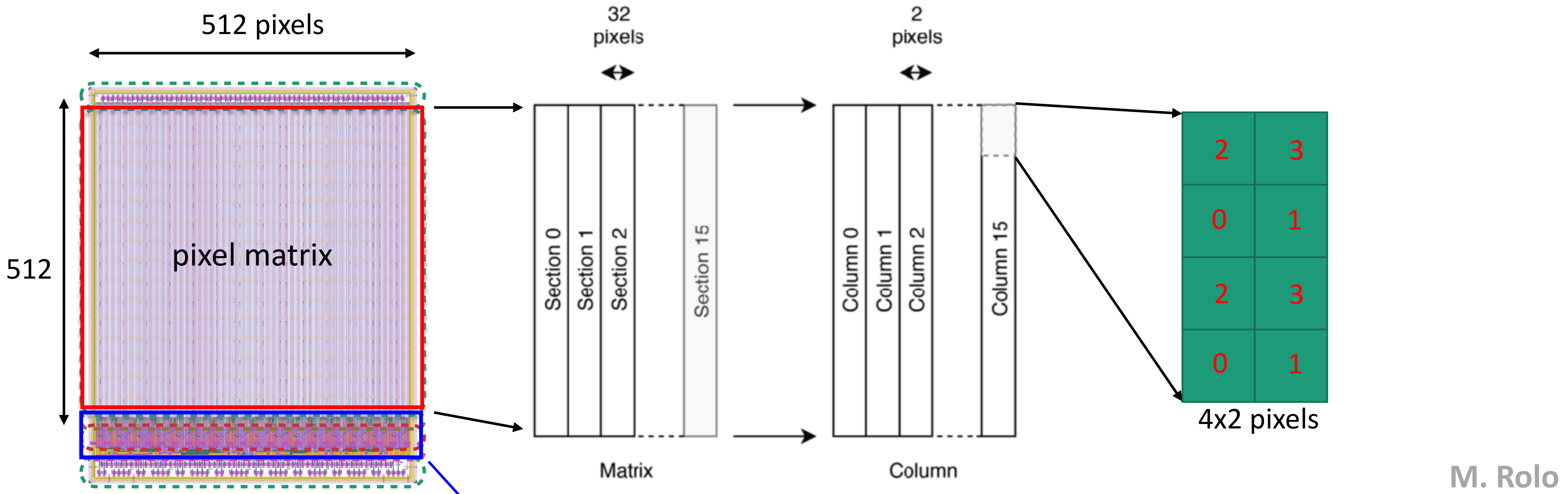
detail of pixel layout

M. Rolo

- pixel pitch: 25 μm
- electronics: **analog** and **digital**, with in-pixel **threshold** and **data storage**
- triggerless data-driven readout with low-power asynchronous architecture with **clockless pixel matrix** integrated on a power-oriented flow
- power: 10 – 30 mW /cm^2
- event rate: up to 100 MHz/ cm^2

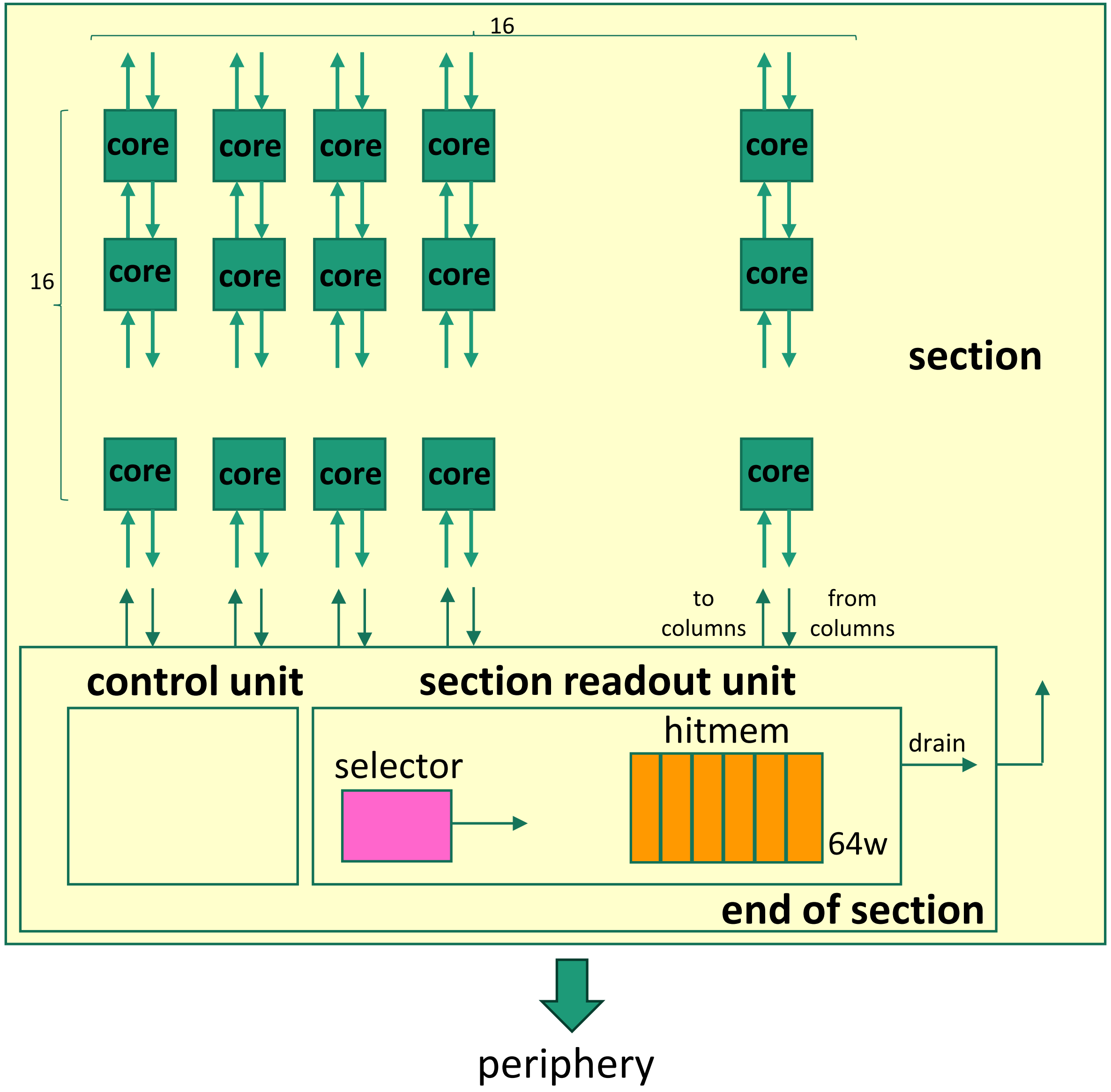
MD3: chip architecture

pixel matrix: 512×512 pixels arranged in 16 sections with independent bias and readout



periphery:
end of section: to configure and readout pixels
section biasing units for I/V biases
SPI for configuration, 8B10B, serializers

MD3: asynchronous architecture



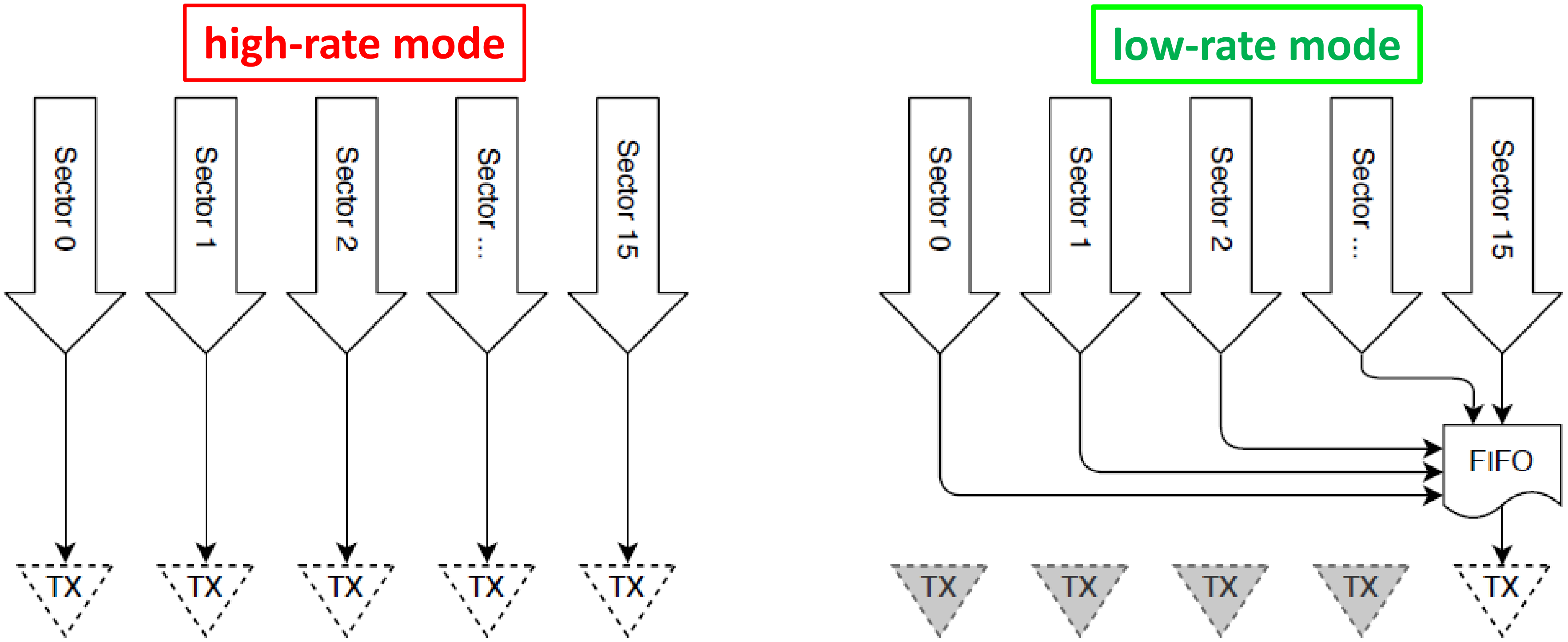
frameless asynchronous readout with clockless matrix:

- if any **pixel** is **hit**, the pixel status register is set to high and the **full flag of the pixel region** is set.
- a **token chain** is created by summing the pixel region full flags starting from the top.
- the token signal is propagated to the **section readout unit** and the timestamp is latched.
- the payload consisting of the column data, column address and timestamp is then sent to the **output FIFO** and will be sampled by the periphery circuits.

The 32-bit data words are 8B10B encoded in 40-bit packets and sent out via 320 MHz DDR serializers.

MD3: peripheral dataflow

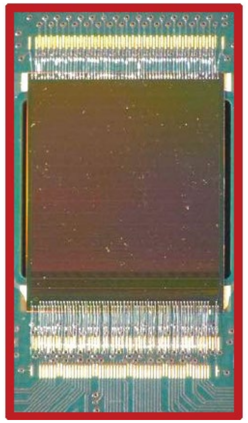
- each sector has an independent readout and output link when operating in **High-Rate Mode**
- sector data is sent out (8B10B encoded) via dedicated 320 MHz DDR serializers
- in **Low-Rate Mode**, one serializer processes data from all the sections. The other serializers and C-LVDS TXs are powered off to reduce power consumption

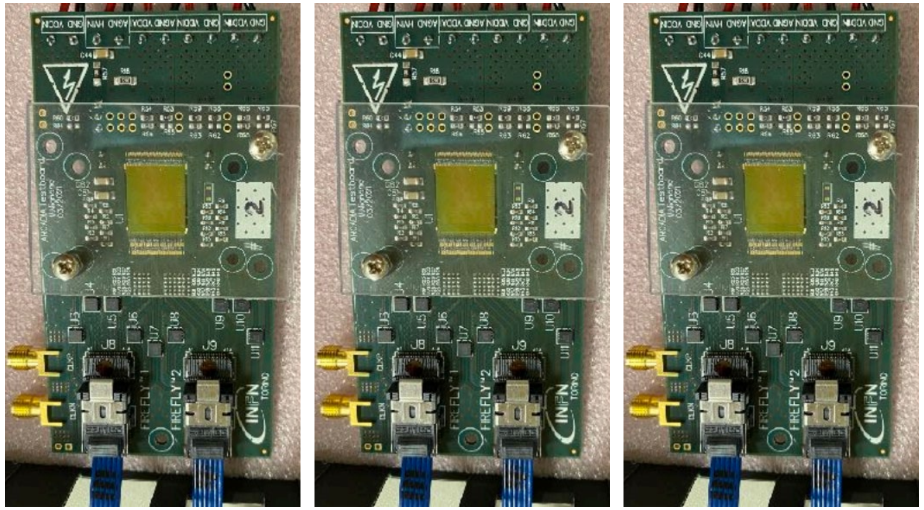


measured value: **17-30 mW/cm²** (to be verified at high rates up to 100 MHz/cm²)

measured value: **10 mW/cm²**

Front-end board and DAQ



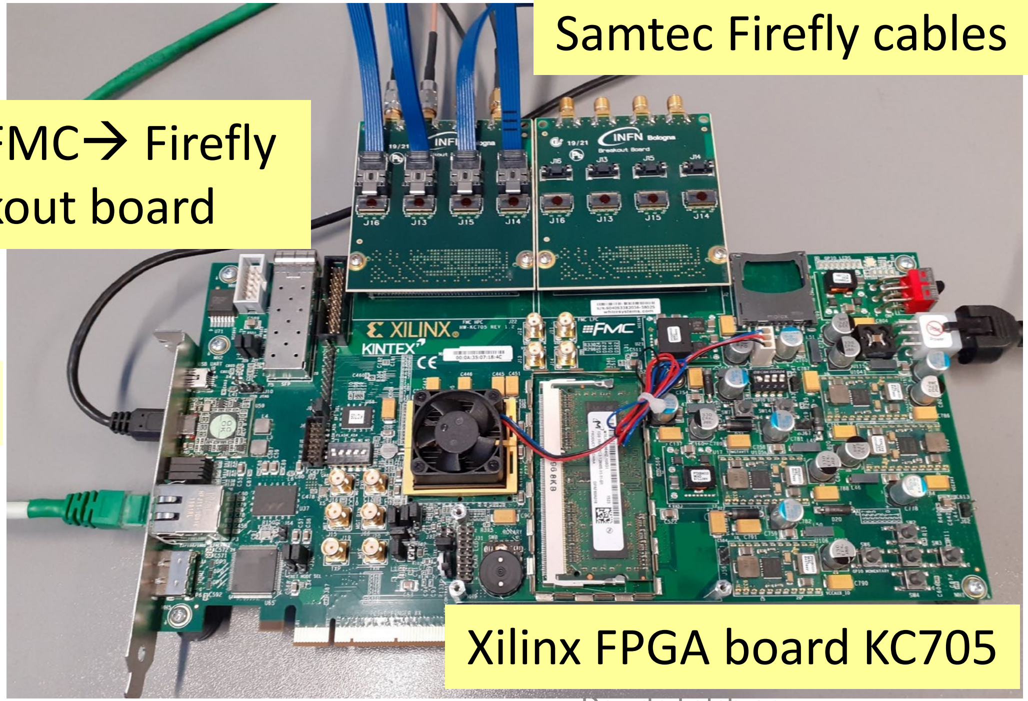


Arcadia front end board

PCB through-hole for matrix Back Side illumination

Samtec Firefly cables

custom FMC→ Firefly breakout board



Xilinx FPGA board KC705

1 Gb ETH

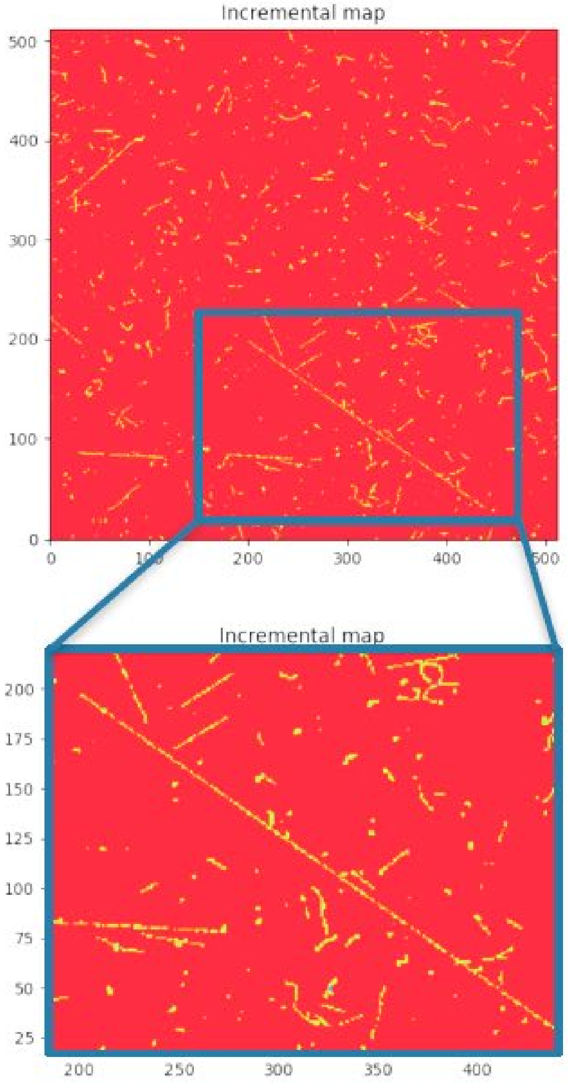
CERN IPbus

The **FPGA**:

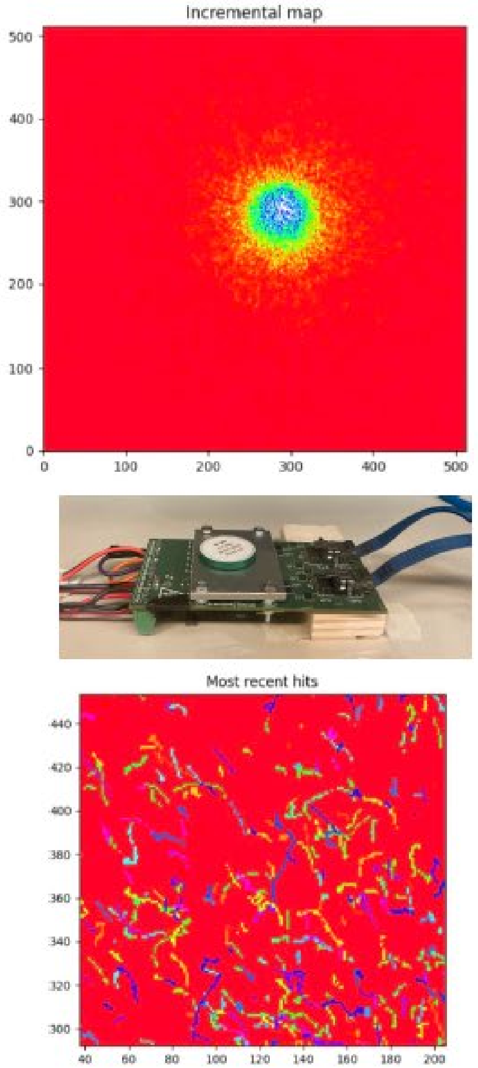
- drives the SPI interface
- extracts hits from the 16 input lanes and stores them locally, before they are sent to a PC using the CERN IPbus protocol
- can work both in data-push mode or in triggered mode

MD3: charged-particle detection

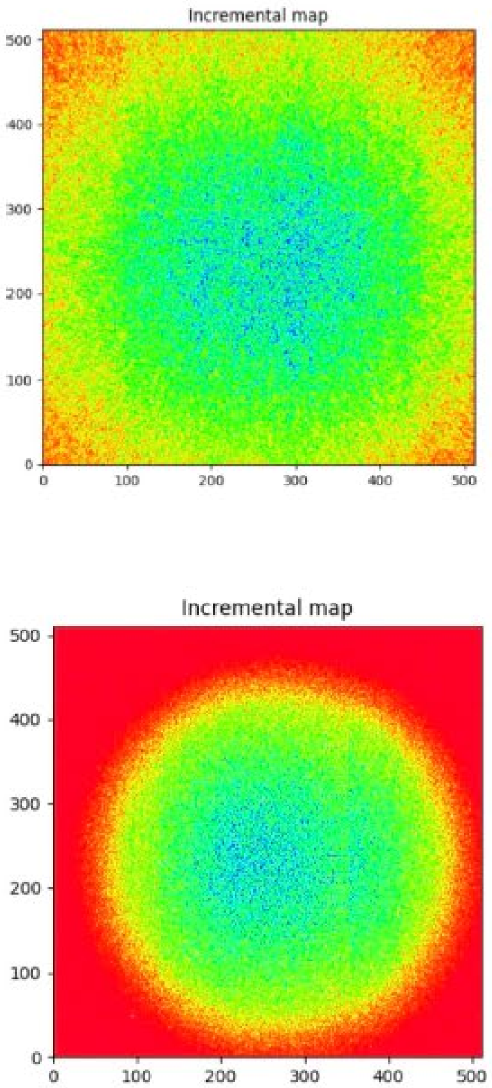
cosmic rays (tilted sensor)



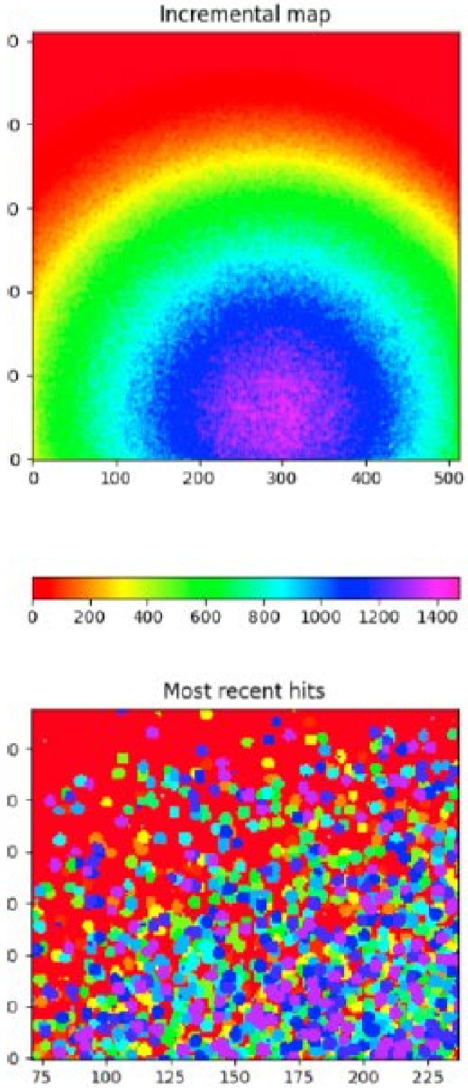
Sr90 (collimated 1 mm)



Sr90 (uncollimated)

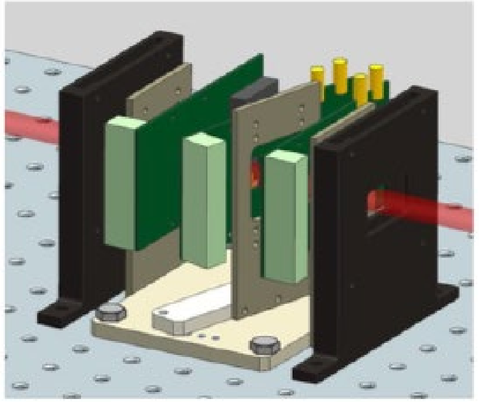


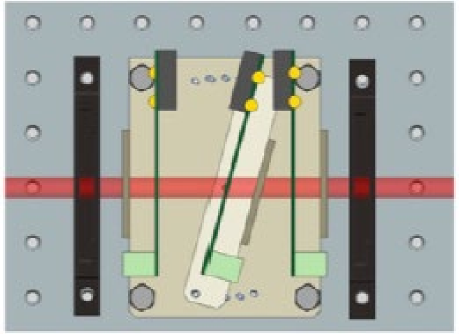
Am241

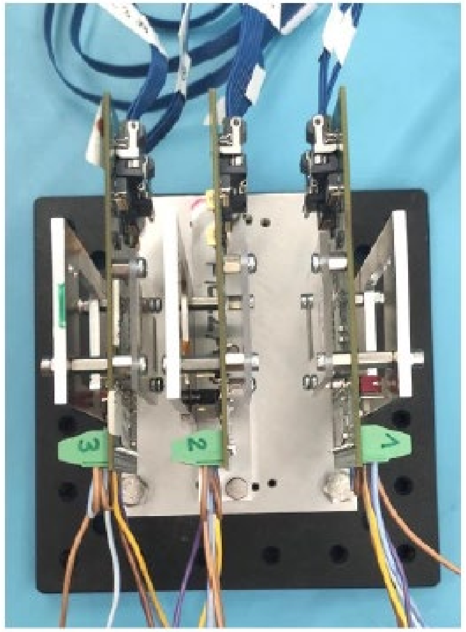


MD3 test beam at FNAL with 120 GeV protons

- mini-telescope with 3 200-µm-thick ARCADIA-MD3 sensors
- threshold, sensor HV and incidence angle parametrization:
  - study of cluster size, collection efficiency and spatial resolution



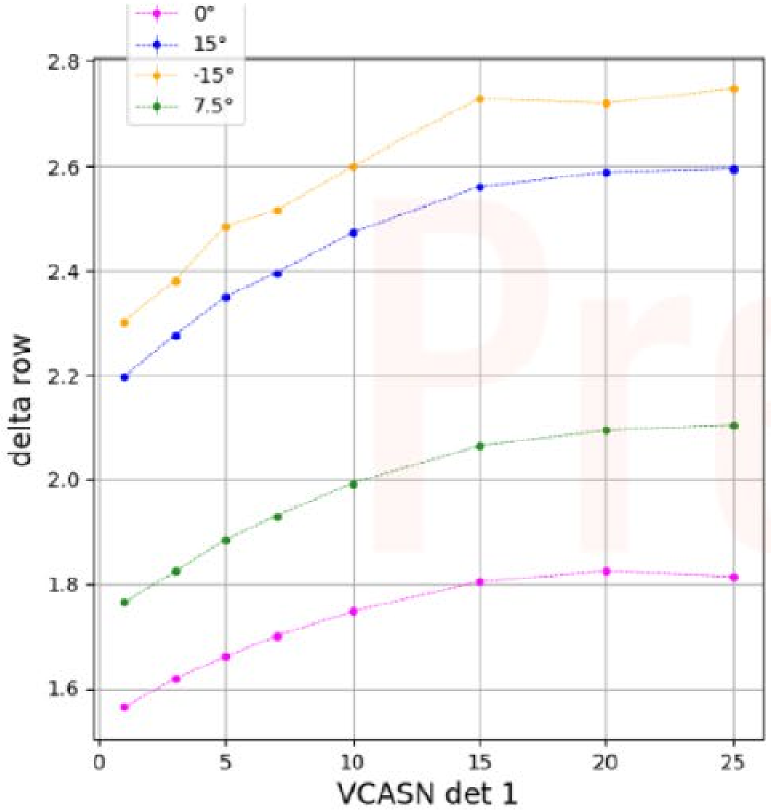


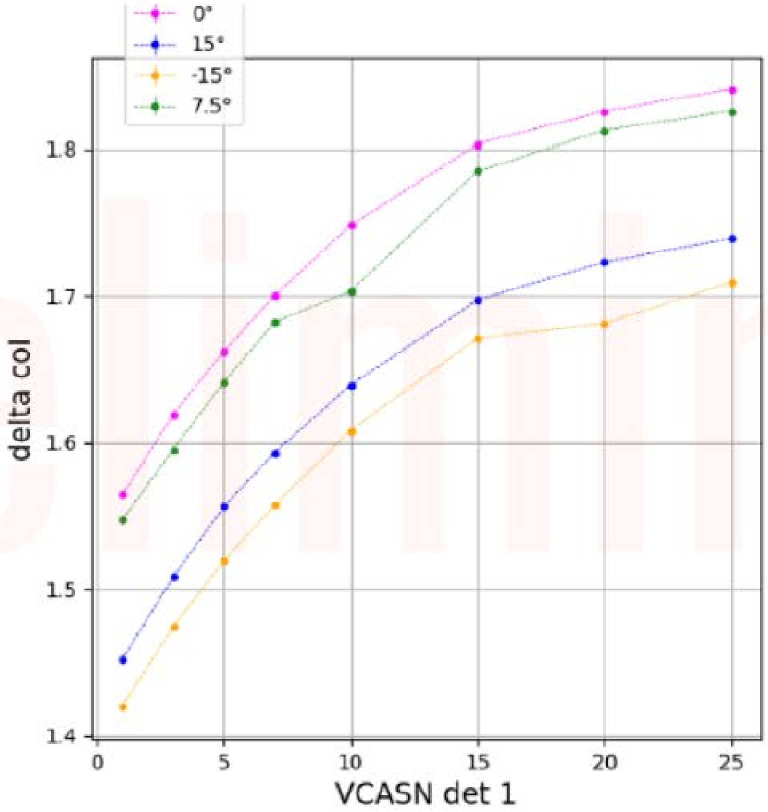


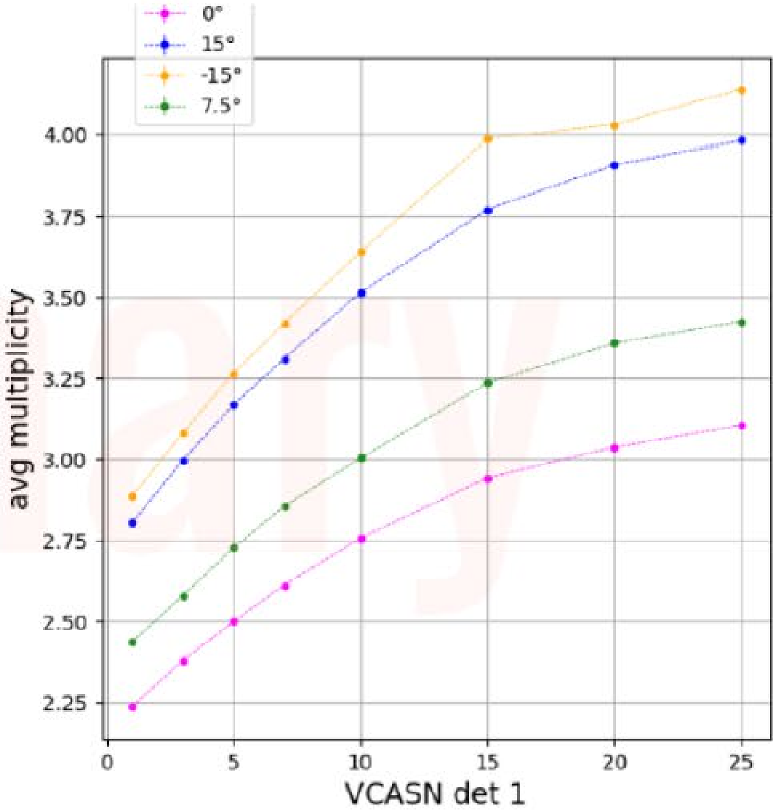
The INFN-PD test beam Team:
Sabrina Ciarlantini, Caterina Pantouvakis, Michele Rignanese, Alessandra Zingaretti, Piero Giubilato, Jeffery Wyss, Serena Mattiazzo, Chiara Bonini, Davide Chiappara, Devis Pantano, Patrizia Azzi e Rosario Turrisi
At FNAL:
Irene Zoi, Nicola Bacchetta, Artur Apresyan, Aram Hayrapetyan, Pierce Affleck

MD3 test beam at FNAL with 120 GeV protons

Cluster dimensions on the middle MD3 (DUT) as a function of the discriminator threshold (835 to 290 e-) and incidence angle (0°, ±15°, 7.5°)

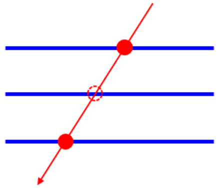




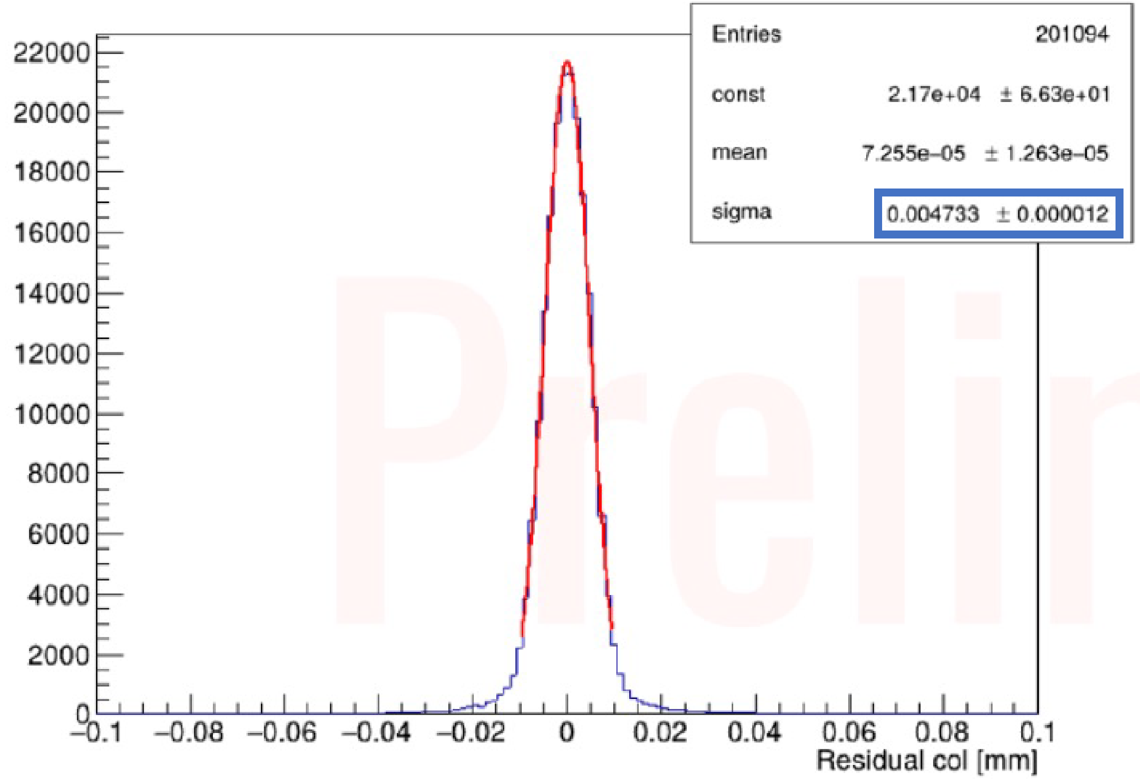


835 e- 290 e- 835 e- 290 e- 835 e- 290 e-

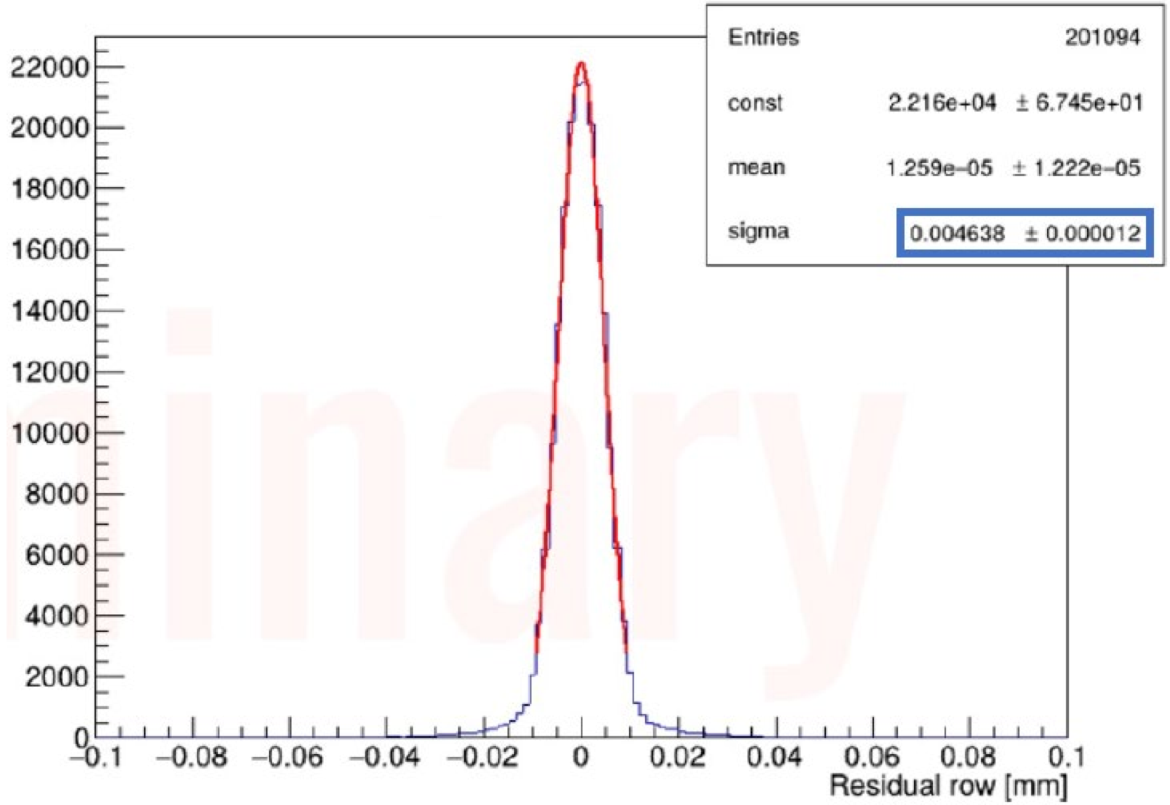
MD3 test beam at FNAL with 120 GeV protons



Spatial resolution with tilt = 0° and only 1 cluster per plane



final residual columns



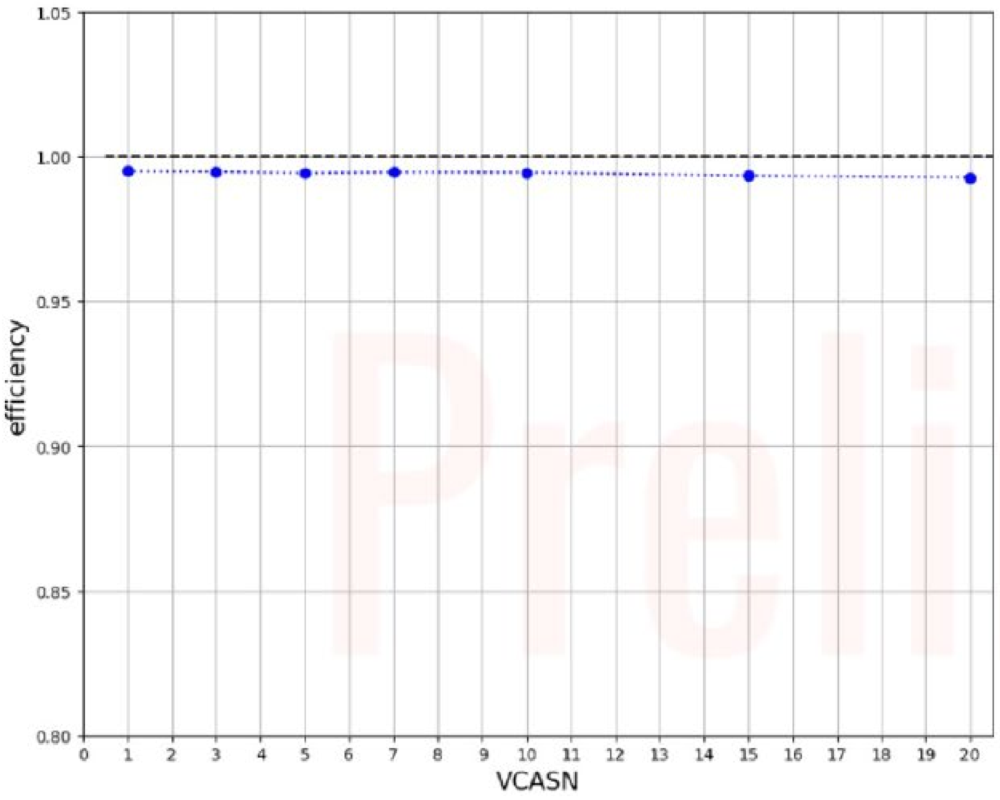
final residual rows

$\sigma \sim$ 4.7 µm

(< pitch / √12 ~ 7.2 µm)

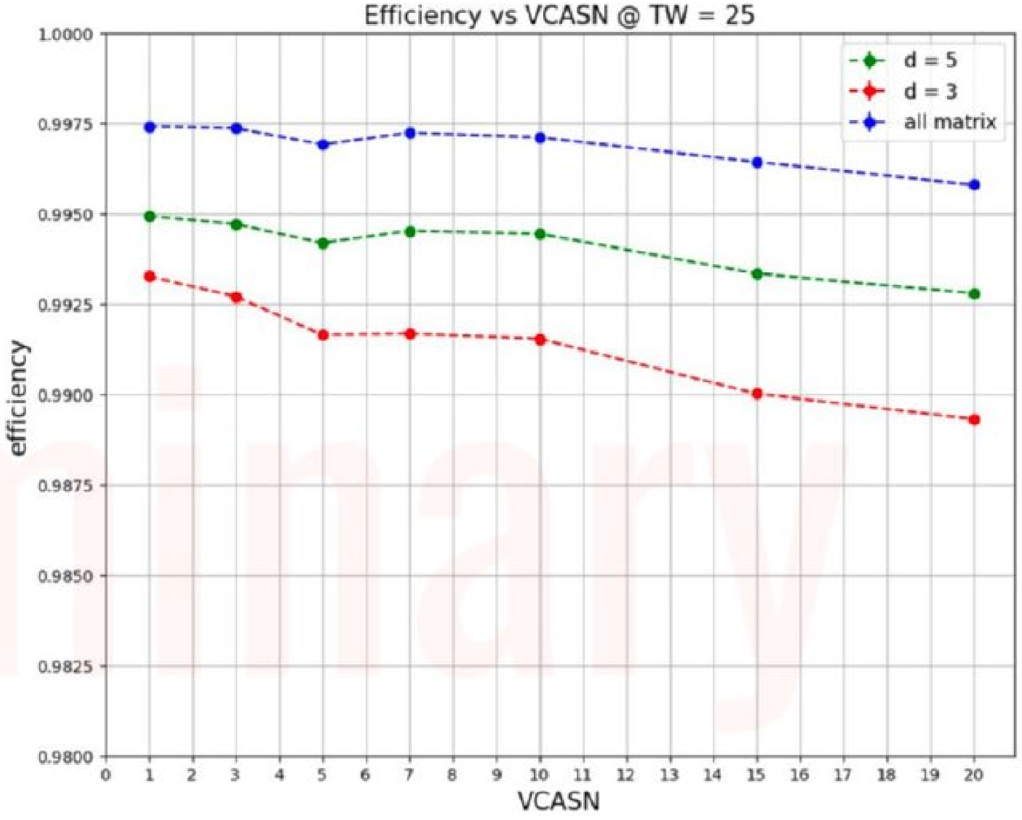
MD3 test beam at FNAL with 120 GeV protons

Collection efficiency versus discriminator threshold (time window 5 μs) and spatial cut



835 e-

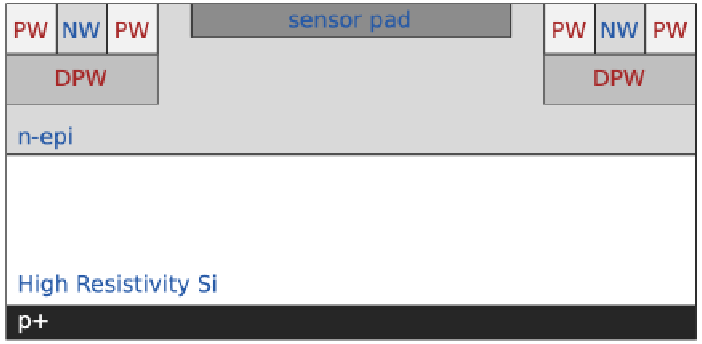
290 e-



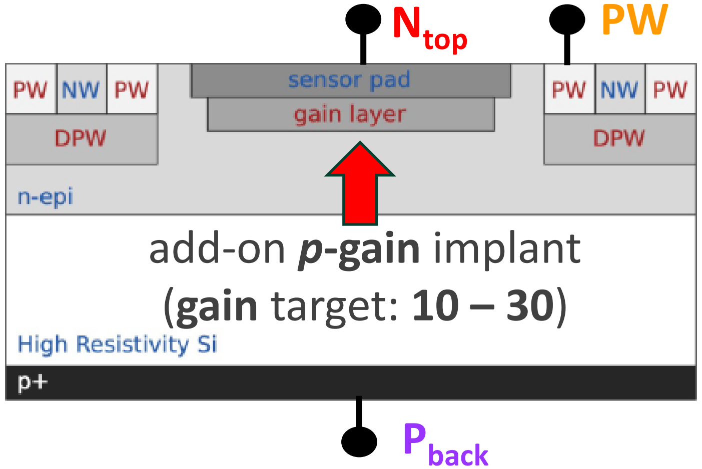
average efficiency: 0.9941 ± 0.0003

Arcadia R&D for fast timing

FD-MAPS

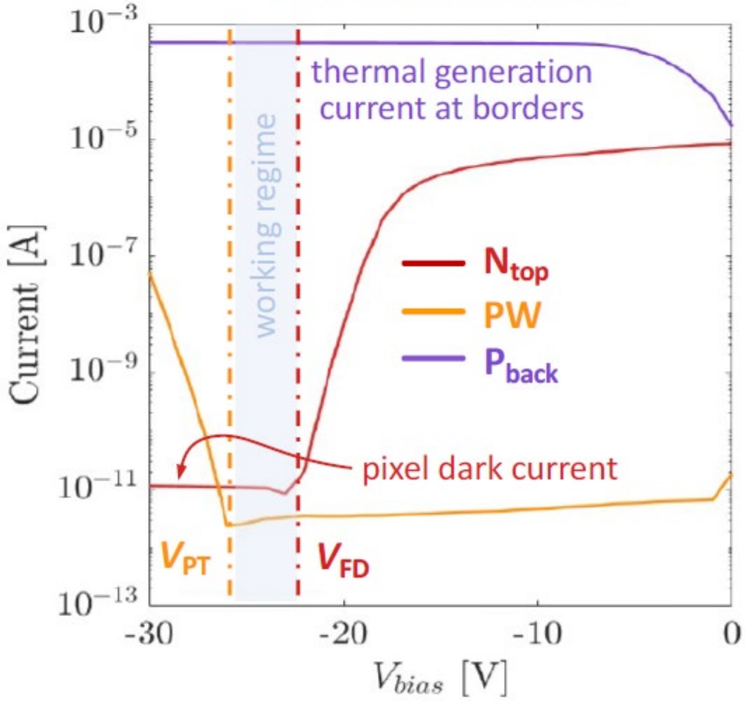


monolithic LGAD

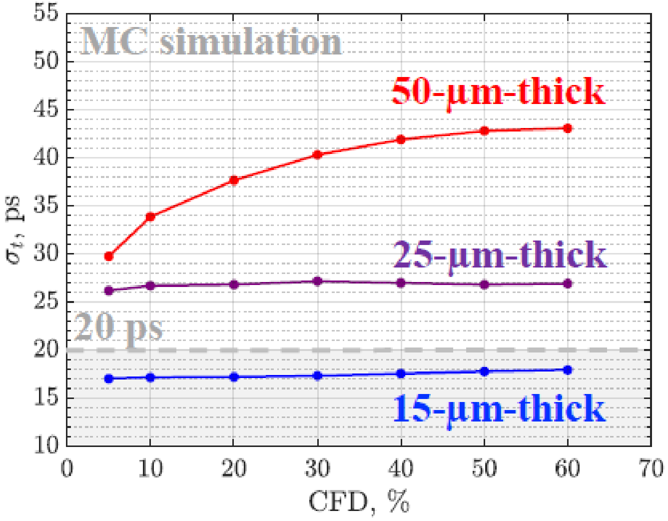


avalanche process → larger SNR
→ better time resolution

Operation regime



expected performances (simulation)



- **working regime between V_{FD} and V_{PT}**
- **full-depletion** condition
- **punch-through** driven by the **backside bias**, which defines the **field** in the substrate
- **edge breakdown** (due to gain) induced by the **topside voltage**

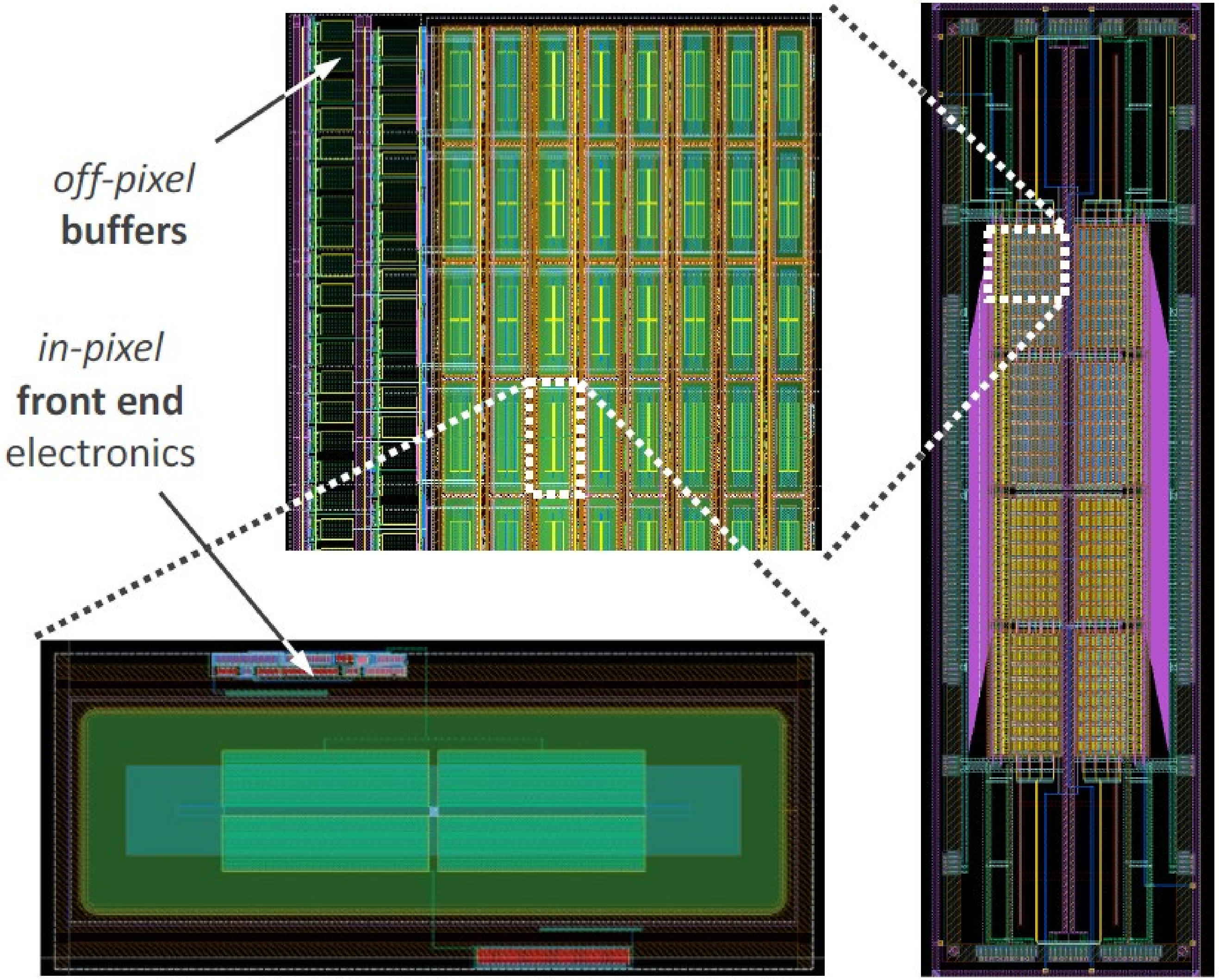
Arcadia R&D for fast timing

MADPIX:

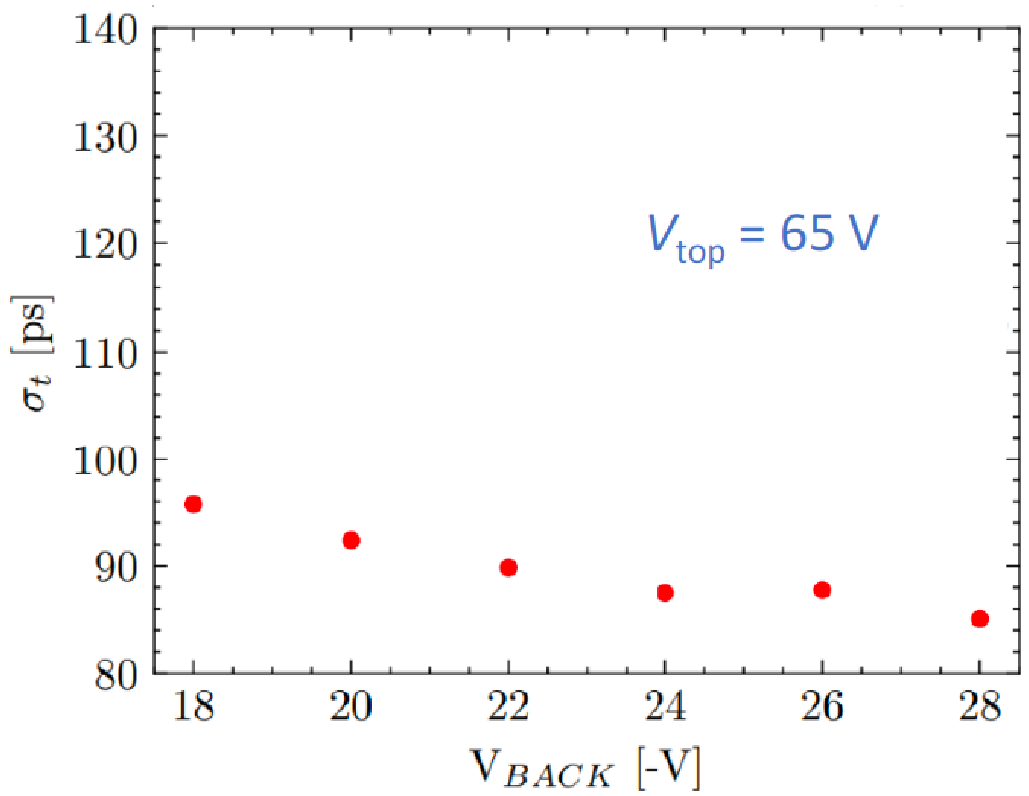
Monolithic CMOS **A**valanche **D**etector **PIX**elated Prototype for ps Timing Applications

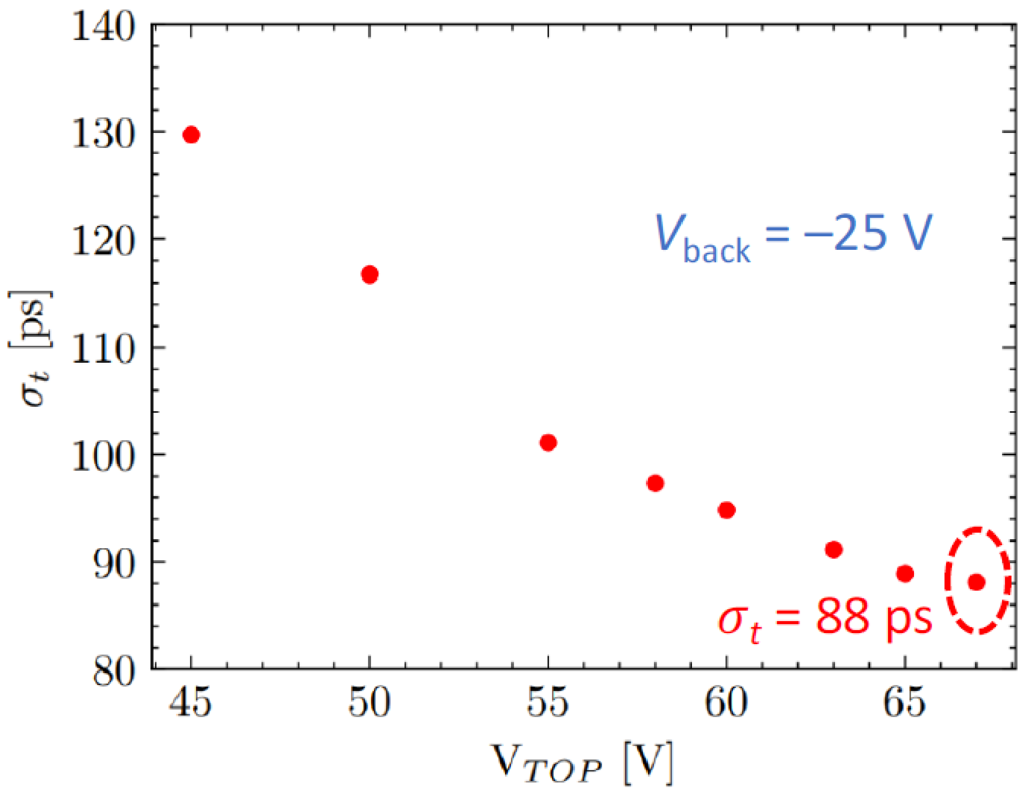
- first small-scale demonstrator 4 x 16 mm^2
- 8 matrices (64 pixels each) implementing different sensor and front-end flavours
- 250 x 100 μm^2 pixel pads
- active thickness 48 μm
- 64 analogue outputs on each side, rolling shutter of single matrix readout

- backside HV: allows full depletion (-20V to -40V)
- topside HV: manages the gain (35V to 65V)



MADPIX: test beam with 10 GeV pions at CERN PS (Oct 2024)





Time resolution (sensor + FE electronics) at V_{top} = 65 V and V_{back} = –25 V is σ_t = 88 ps
with boosted electronics: σ_t = 75 ps
still not optimized substrate and geometry ⇒ improvements are expected

Arcadia: status and outlook

INFN platform for R&D in fully-depleted monolithic CMOS sensor technology, IP and ASIC design, DAQ systems:

- Low-power FD-MAPS sensor architectures (10 mW/cm^2) for photon and charged particle detectors
- Innovative monolithic CMOS sensors with gain layer (CMOS LGAD)
- Deep-submicron monolithic CMOS sensor technology with high charge collection efficiency for X-ray imaging

Field of applications for the ARCADIA technology framework:

- X-ray imaging for industrial and medical applications (**CT**, **Tracking** and **Dosimetry** in HDR Brachytherapy)
- Space applications (low-power **monolithic active microstrips** with embedded readout electronics)
- MAPS technology for tracking and timing systems in future lepton colliders (Vertex and Si-wrapper for **IDEA**)
- Time-of-flight detector for ALICE3 (ARCADIA CMOS-LGAD is the baseline option for the **ALICE3 TOF**)

Ongoing and financed programs and projects:

- ALICE3 TOF (**INFN CSN3**) and RD_FCC IDEA Detector R&D (**INFN CSN1**)
- HyPoSiCX: Hybrid Perovskite on Silicon CMOS X-ray Detectors (**PRIN2022**)
- SpaceItUp “Spoke 4” Next Generation Detectors of Ionizing Radiation and Fields for Remote Sensing (**ASI**)
- “1MICRON” - New Technology for 1 Micron Resolution Biomedical Imaging, Call HORIZON-EIC-2024-PATHFINDEROPEN-01 (**EIC**)
- “Si3”- 3D silicon detector for imaging of diagnostic and therapeutic nuclear medicine radiotracers with outstanding efficiency and high spatial resolution Call ERC-2023-ADG (**ERC**)

Thanks for your time

Some references

ARCADIA fully depleted CMOS MAPS development with LFoundry 110 nm CIS
Front. Sens., 11 August 2025, Sec. Sensor Devices,
Volume 6 – 2025
https://doi.org/10.3389/fsens.2025.1603755

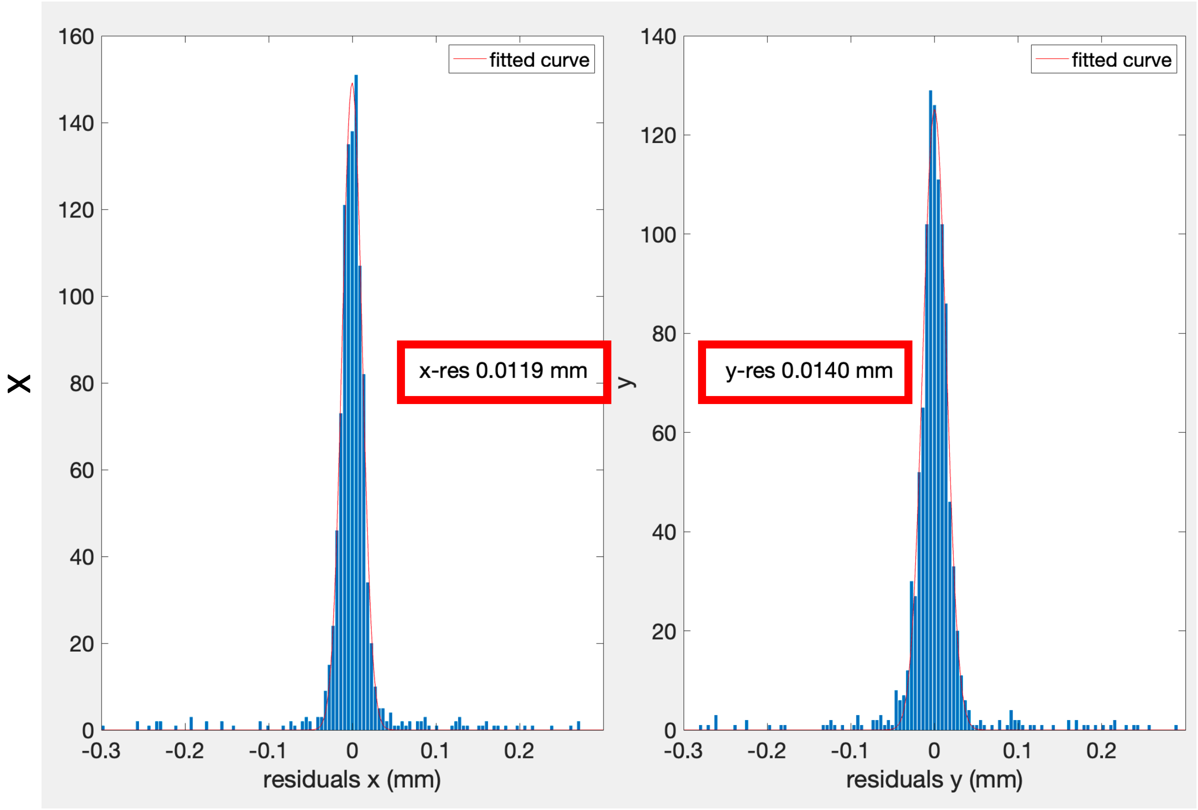
First characterization results of ARCADIA FD-MAPS after X-ray irradiation
Journal of Instrumentation, Volume 18, January 2023
JINST **18** C01066**DOI** 10.1088/1748-0221/18/01/C01066

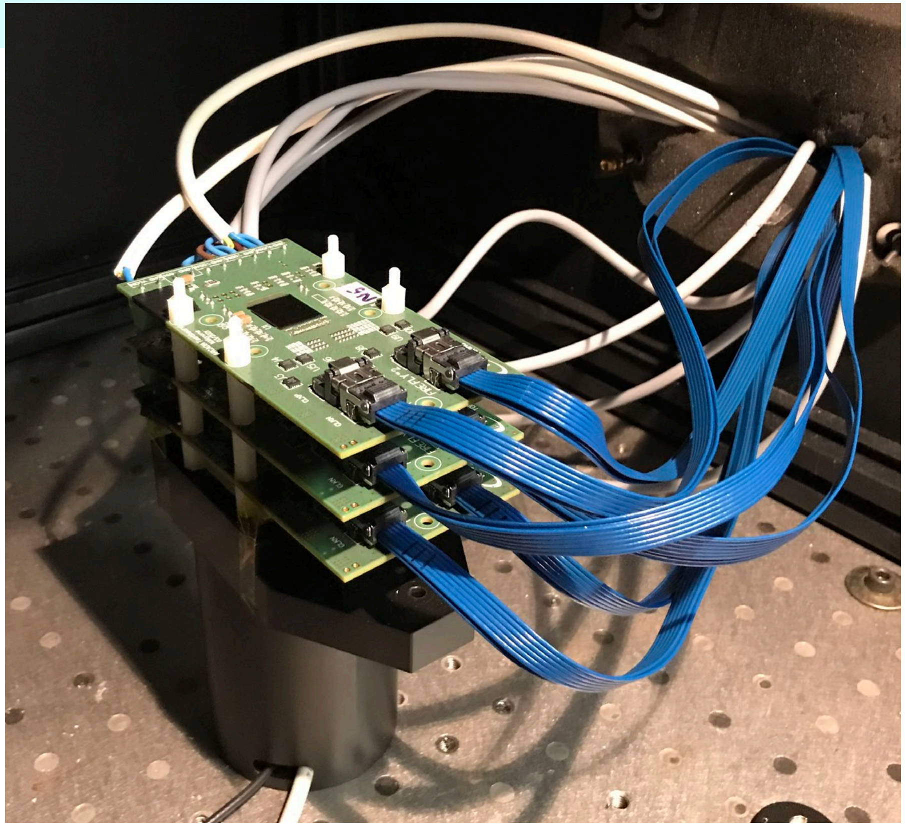
Backup

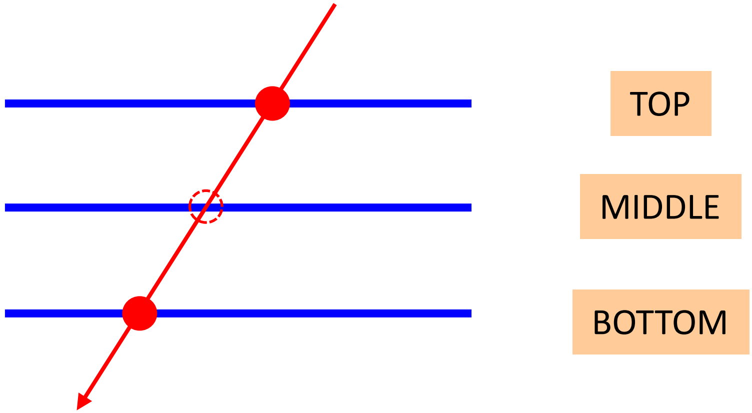
Arcadia MD3 cosmic data telescope

system mounted in a black box
typical HV = - 90 V
typical leakage current = 20 mA
threshold = 25 DAC (290 e-)

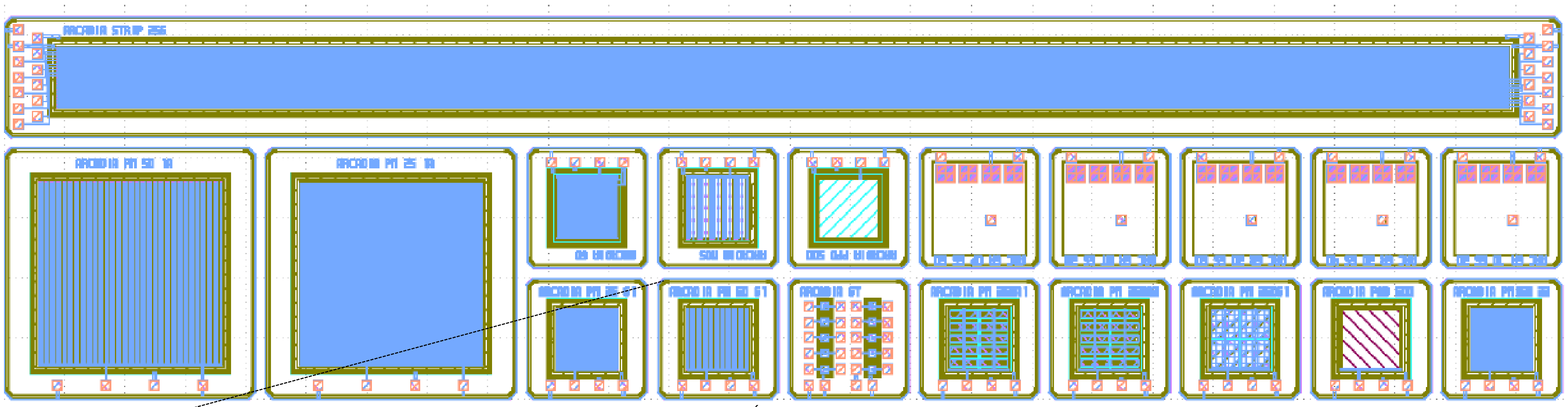
R. Santoro

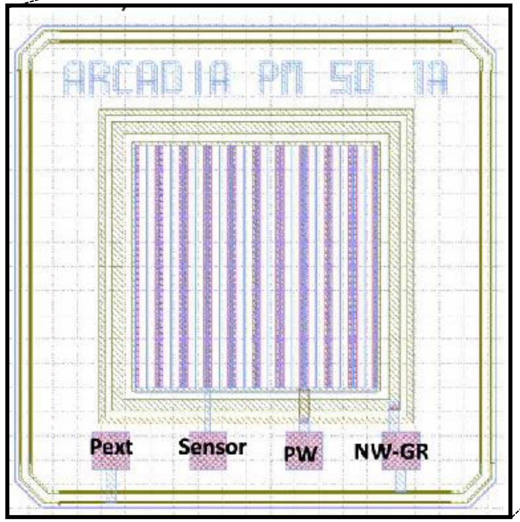






Pixel / strip test structures





strip flavours:

- 25 μm pitch pixelated
- 25 μm pitch continuous
- 10 μm pixelated

pixel flavours:

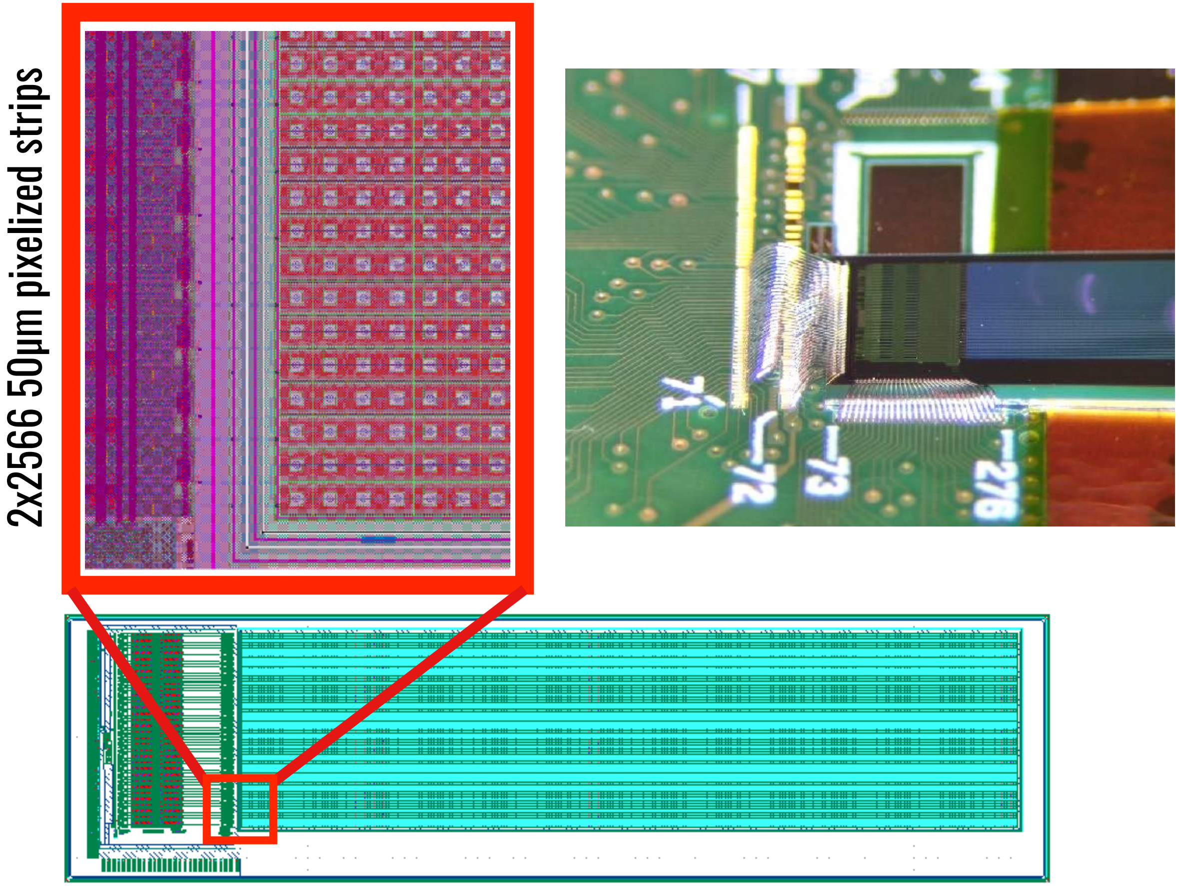
- pseudo-matrices of 1x1 and 2x2 mm^2
- 50 μm pitch
- 25 μm pitch
- 10 μm pitch

used for sensor characterization and process qualification with a probe station

FDMAMs (Fully Depleted Monolithic Active Microstrips)

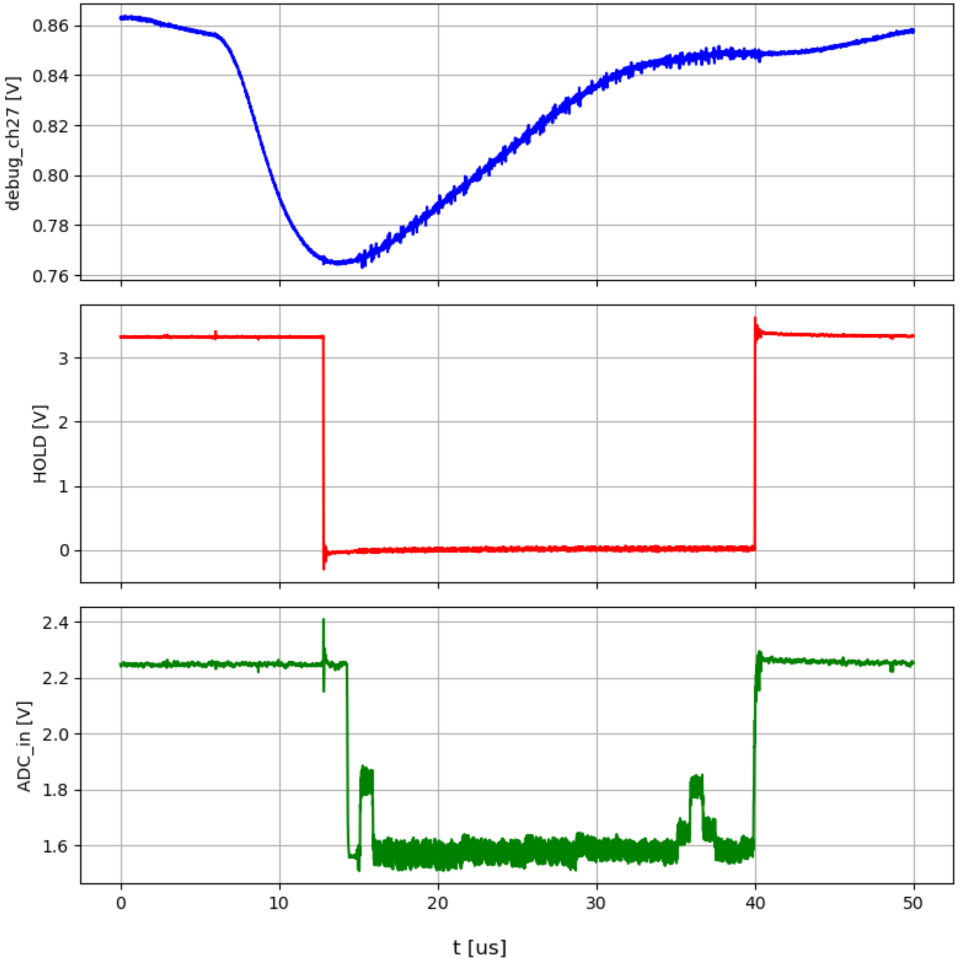
CMOS monolithic strips and embedded readout electronics (active area 12.8 × 3.2 mm^2)

Analogue (MUX-differential output buffer) and Digital readout (Wilkinson ADC + serializer)

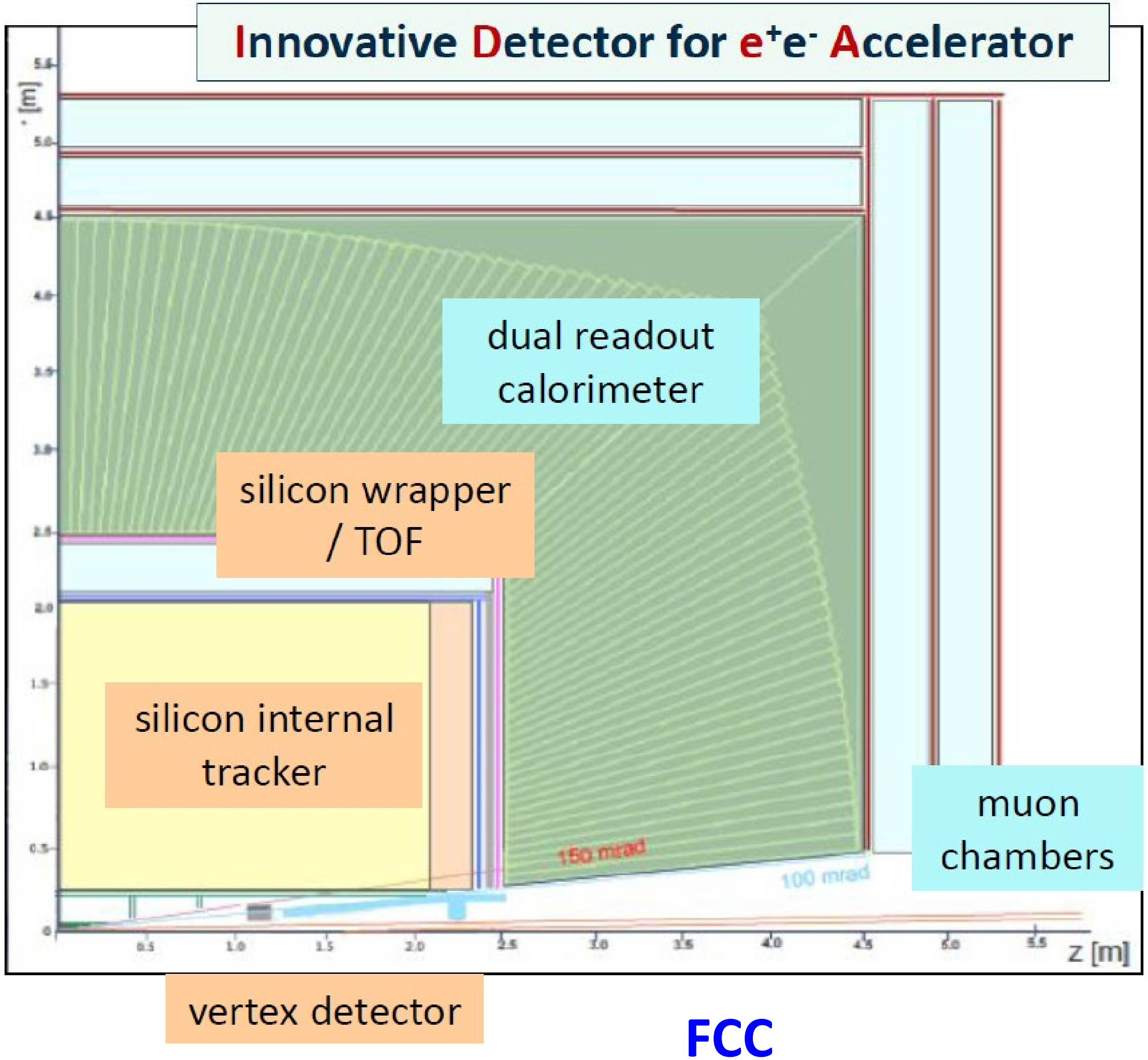


L. Pancheri

acquisition with beta-emitter source



Arcadia for IDEA (FCC) and ALICE3

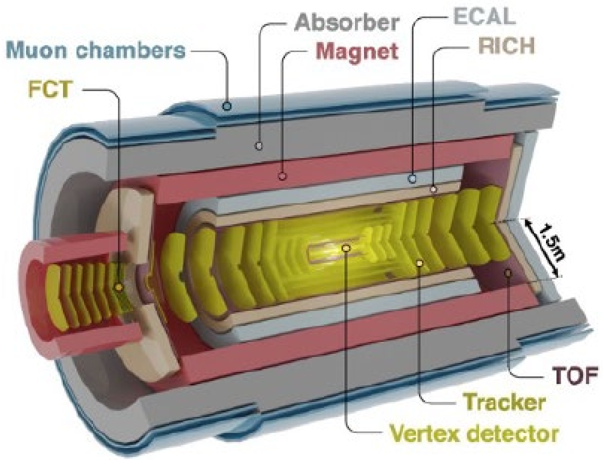


FCC

Arcadia is designing possible solutions for IDEA (FCC):

- vertex detector
  → pixel detectors (FD-MAPS)
- silicon internal tracker
  → strip detectors (FD-MAMs)
- silicon wrapper / TOF
  → pixel detectors with fast timing

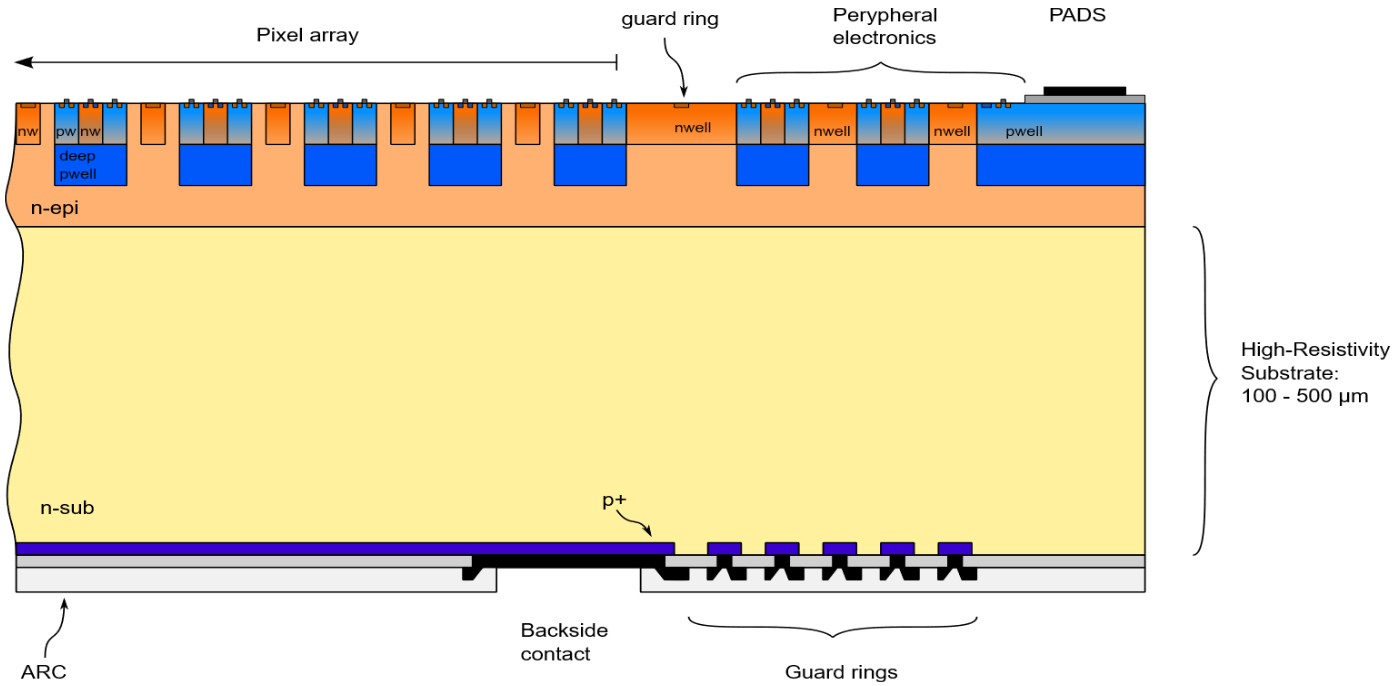
Possible application: **ALICE3 TOF detector**



Arcadia FD-MAPS

Fully Depleted Monolithic Active Pixel CMOS sensor technology platform:

- active sensor thickness in the range 50 μm to 500 μm;
- operation in **full depletion** with fast charge collection by **drift**
- **small collecting electrodes** for optimal SNR
- scalable readout architecture with ultra low-power capability (**O(10 mW/cm^2)**)
- compatible with standard CMOS fabrication process
- technology: **LF11s 110 nm CMOS node** (quad-well both PMOS and NMOS), high resistivity bulk
- custom patterned backside, patent developed in collaboration with L-Foundry



Sensor characteristics - IV curves

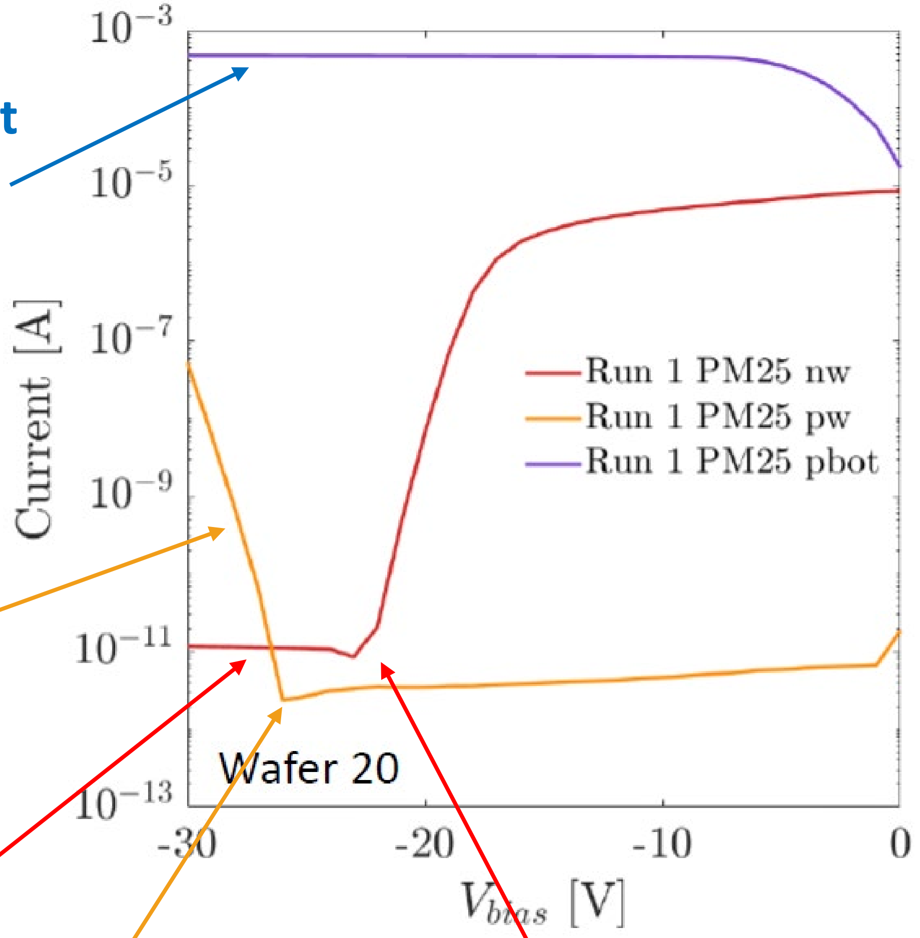
Backside bias current (thermal generation at the dicing line)

Pwell Punch-through current

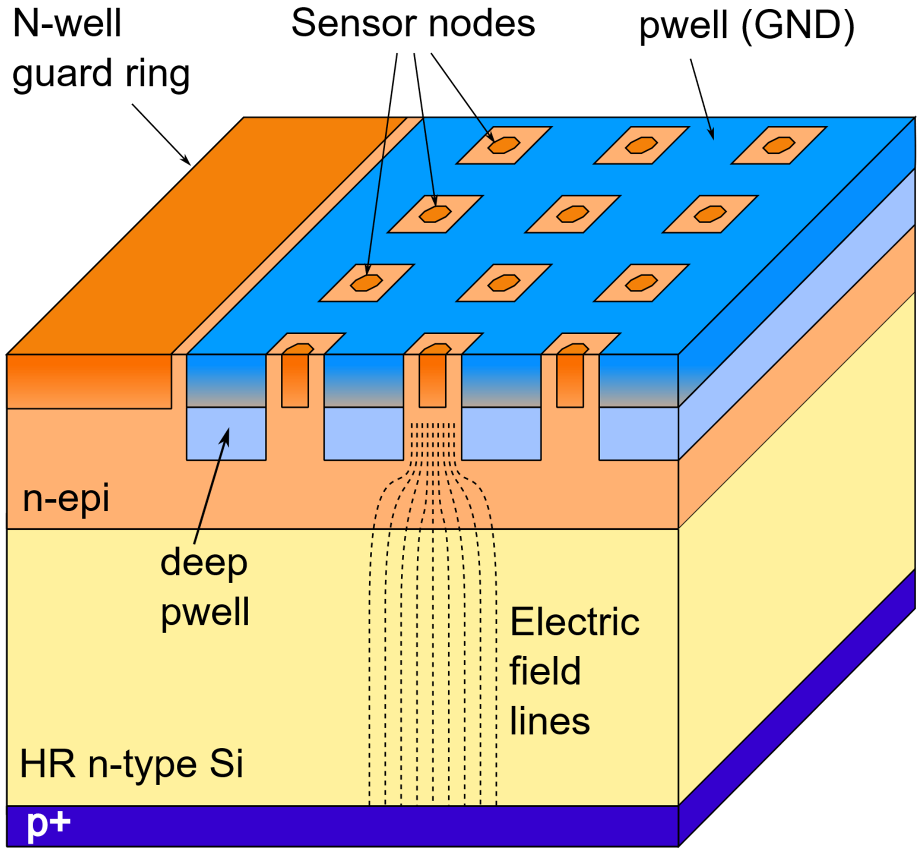
Pixel dark current

Punch-through onset voltage V_{PT}

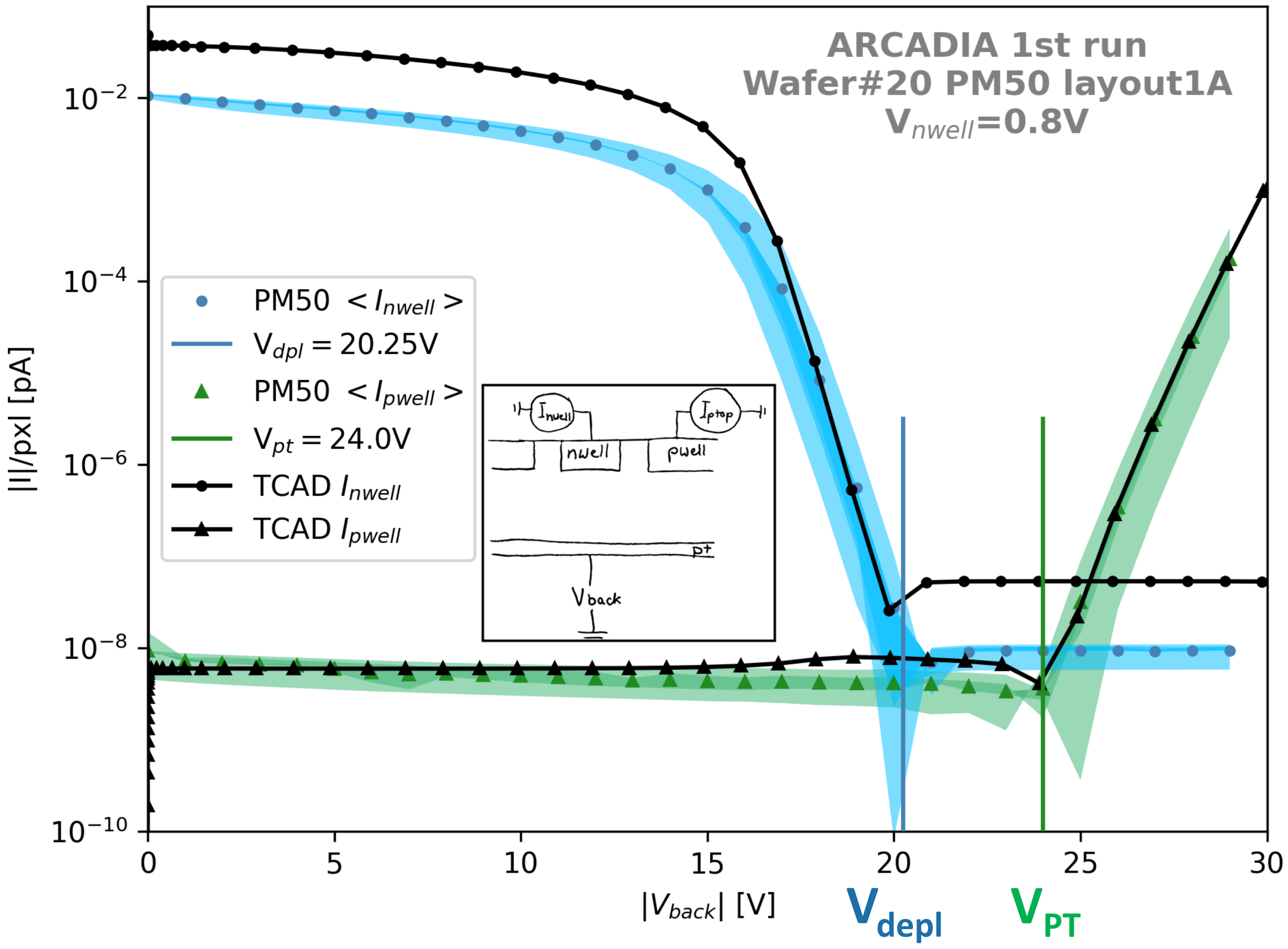
Full depletion voltage V_{depl}



Measured on pixel test structures (arrays of pixels connected in parallel)



Pixel Current-Voltage curves – comparison with TCAD models



Experimental data acquired for different pixel layouts

Intra-wafer and inter-wafer variations were evaluated

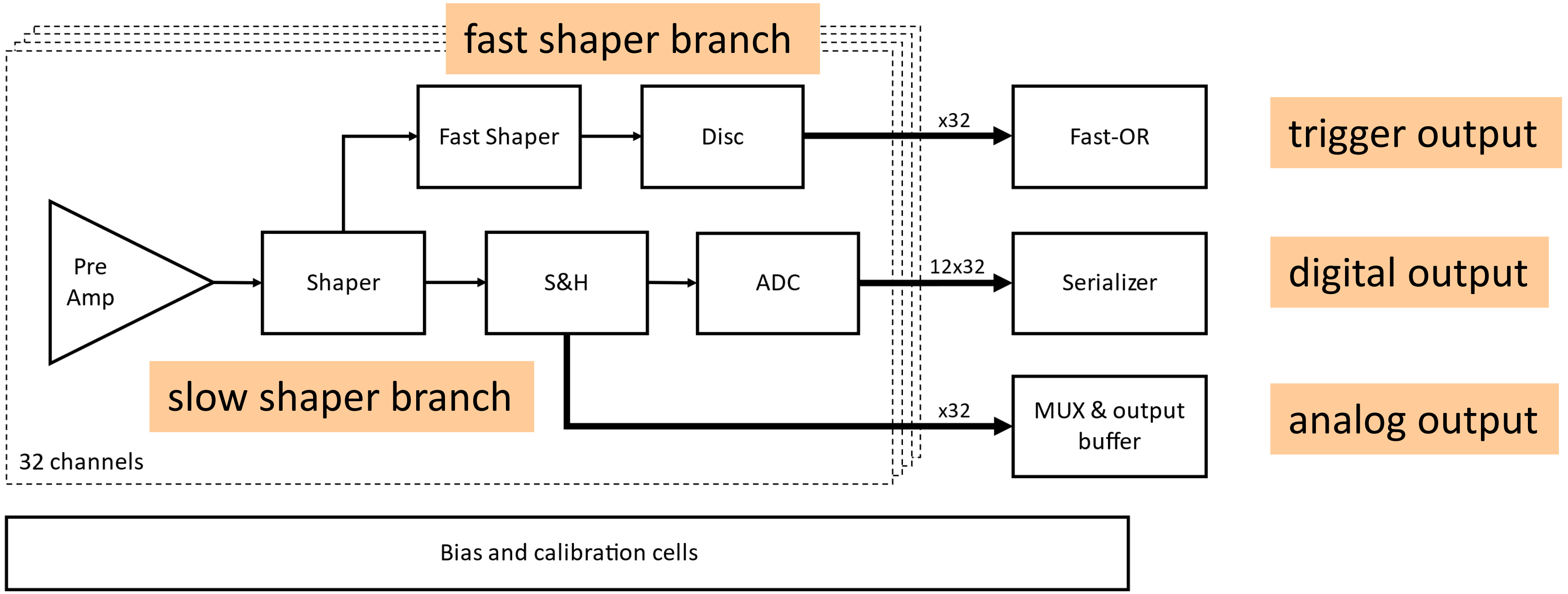
Process parameters in **TCAD simulations** adjusted on experimental results

C. Neubüser

FDMAMs (Fully Depleted Monolithic Active Microstrips)

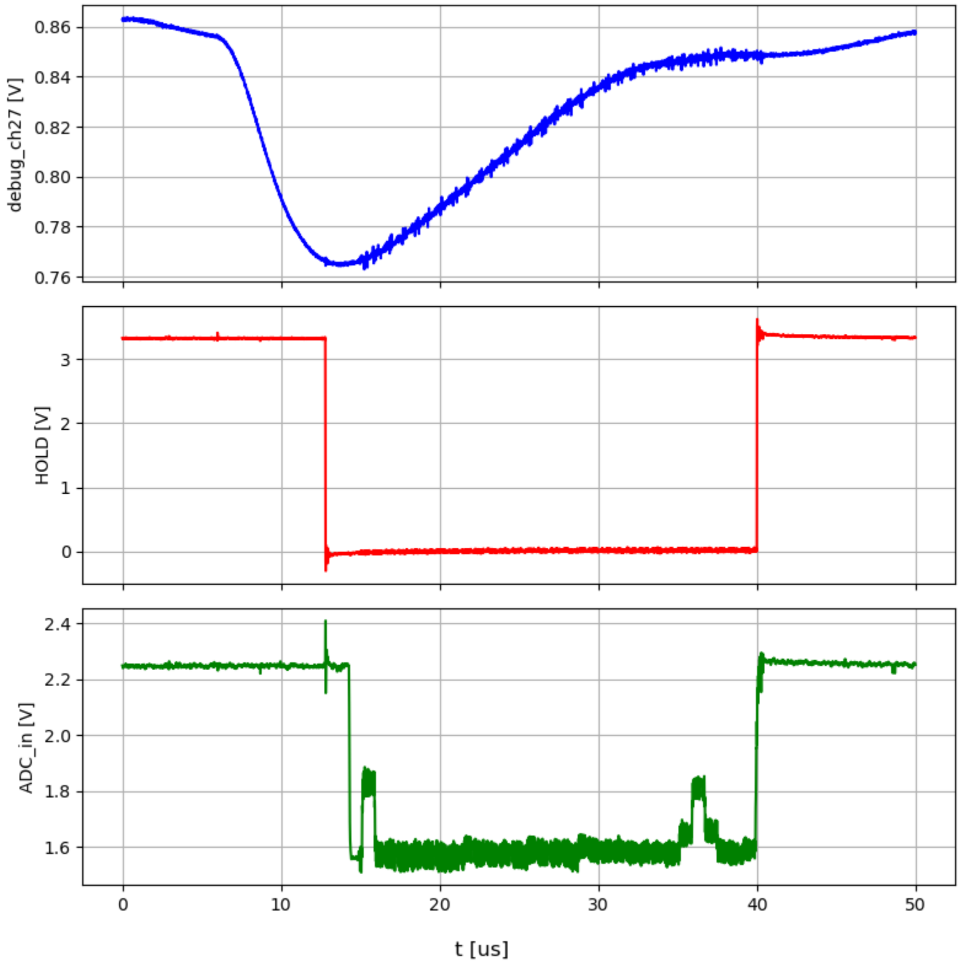
- **preamp**: CSA + testpulse injection circuit
- slow shaper branch for charge measurement with externally controlled S&H circuit
- **readout**:
  - analogue: mux-differential output buffer
  - digital: Wilkinson ADC and serializer
- **trigger output**:
  - fast shaper branch with fast-OR output

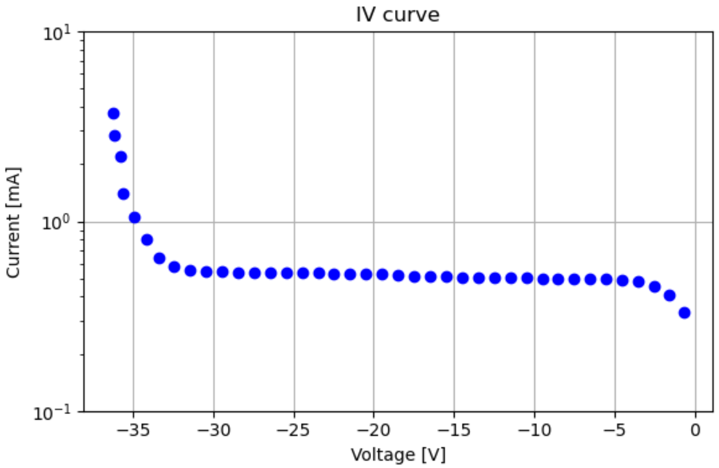
the same readout of the ASTRA chip is integrated into silicon in FDMAMs



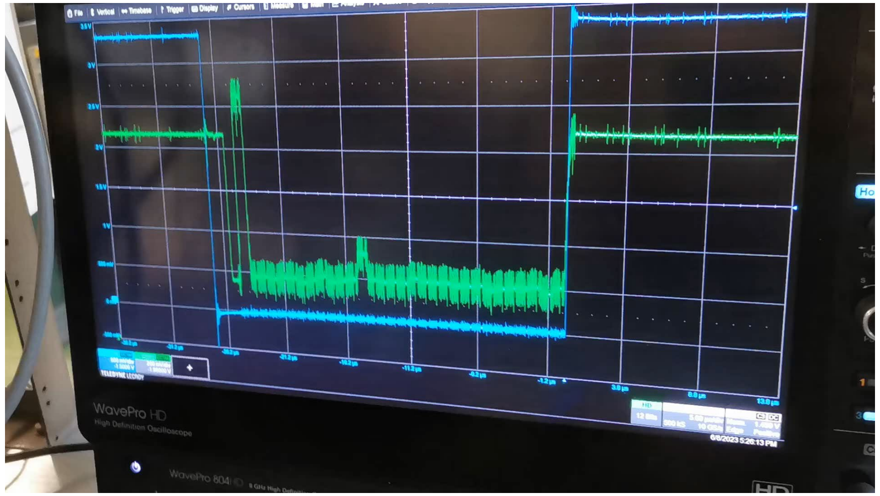
FDMAMs (Fully Depleted Monolithic Active Microstrips)

tests with Sr90



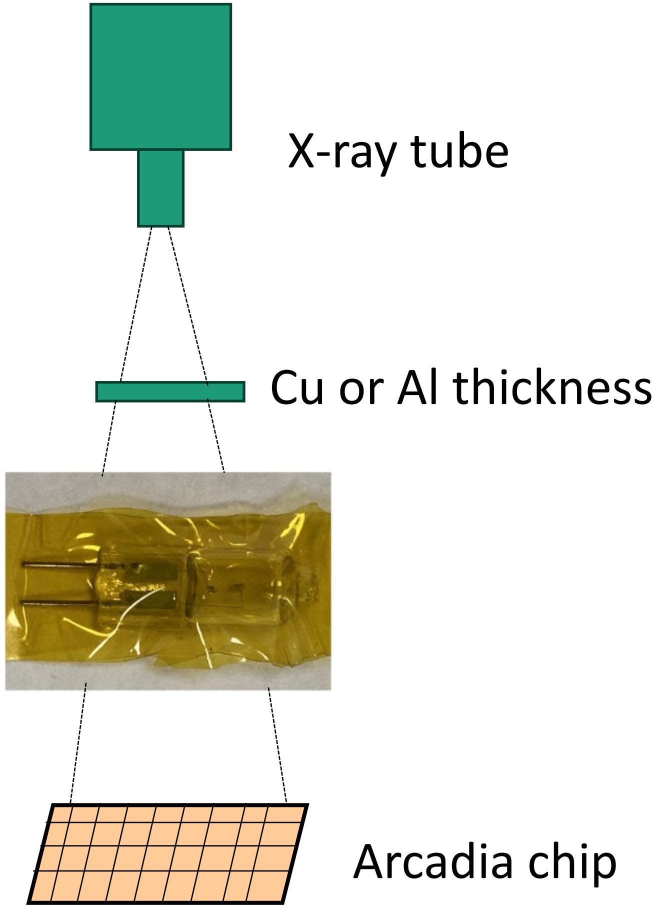


- ASTRA FastOR signals provides trigger to the FPGA
- FPGA sends HOLD signal and then starts readout of analogue MUX

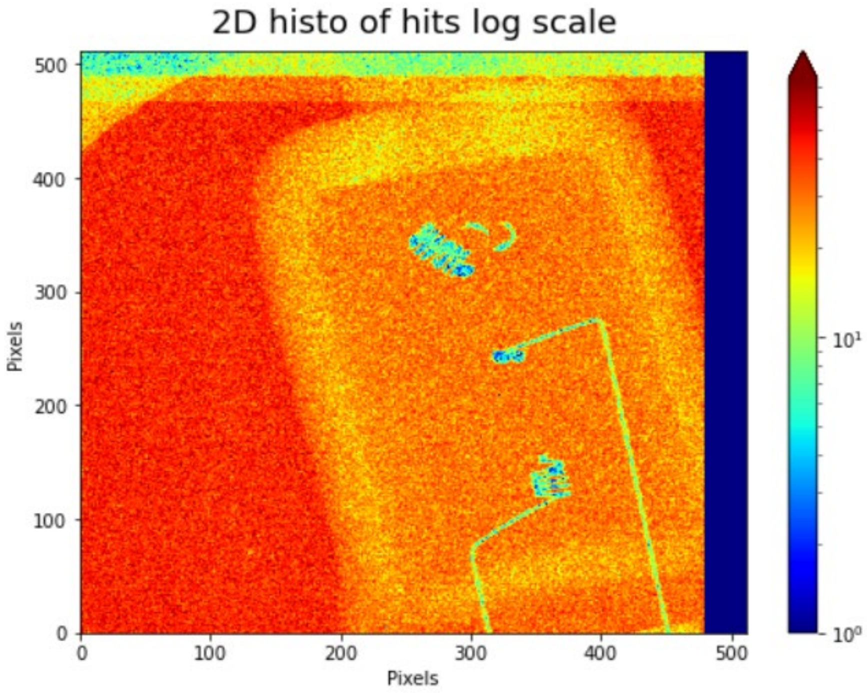


X-ray tube and CT with Arcadia MD3

- X-ray setup (2-10 mA, 40 kV)
- radiography samples and CT reconstruction (stepper motor)



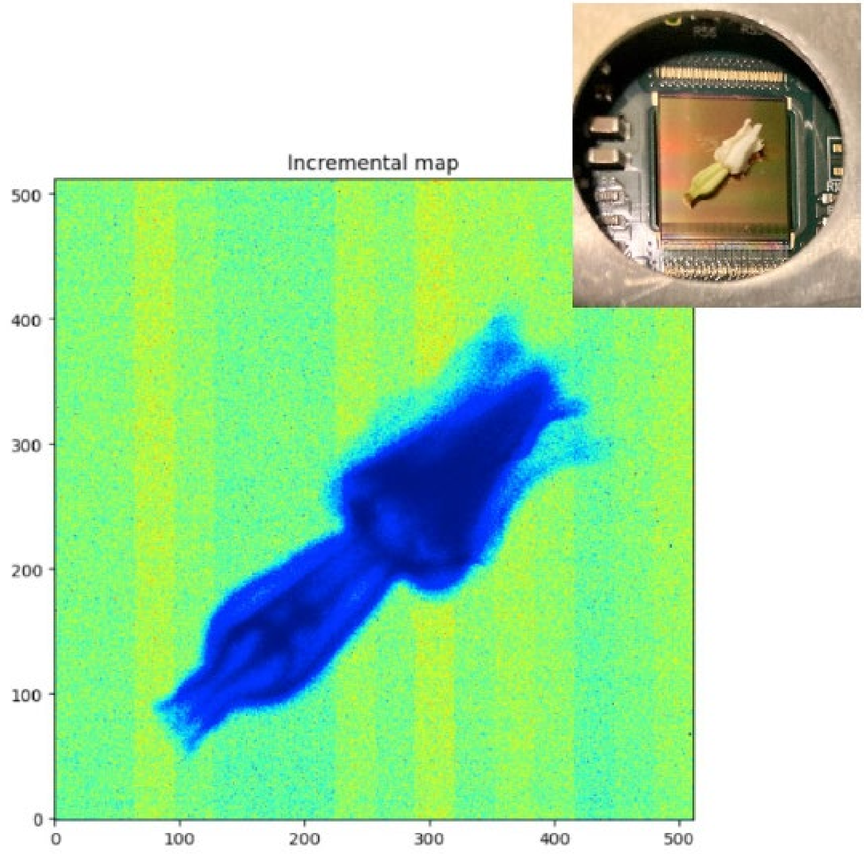
light bulb

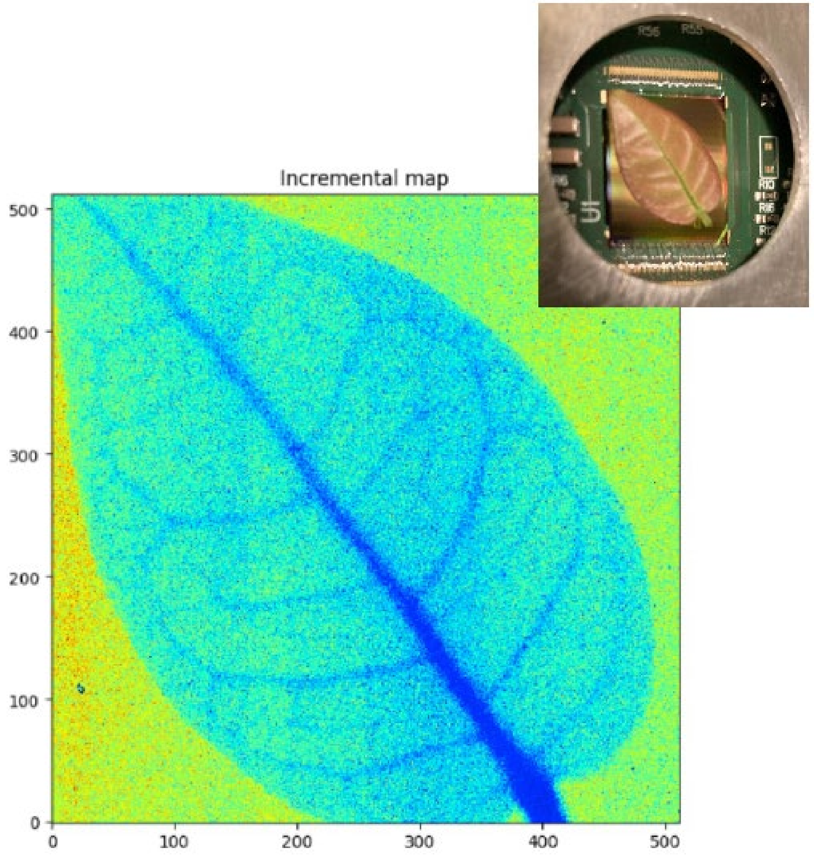


thickness: ~8 mm, height: 2.29 cm, glass + metal

MD3: radioactive source

^{55}Fe radioactive source (6 keV)



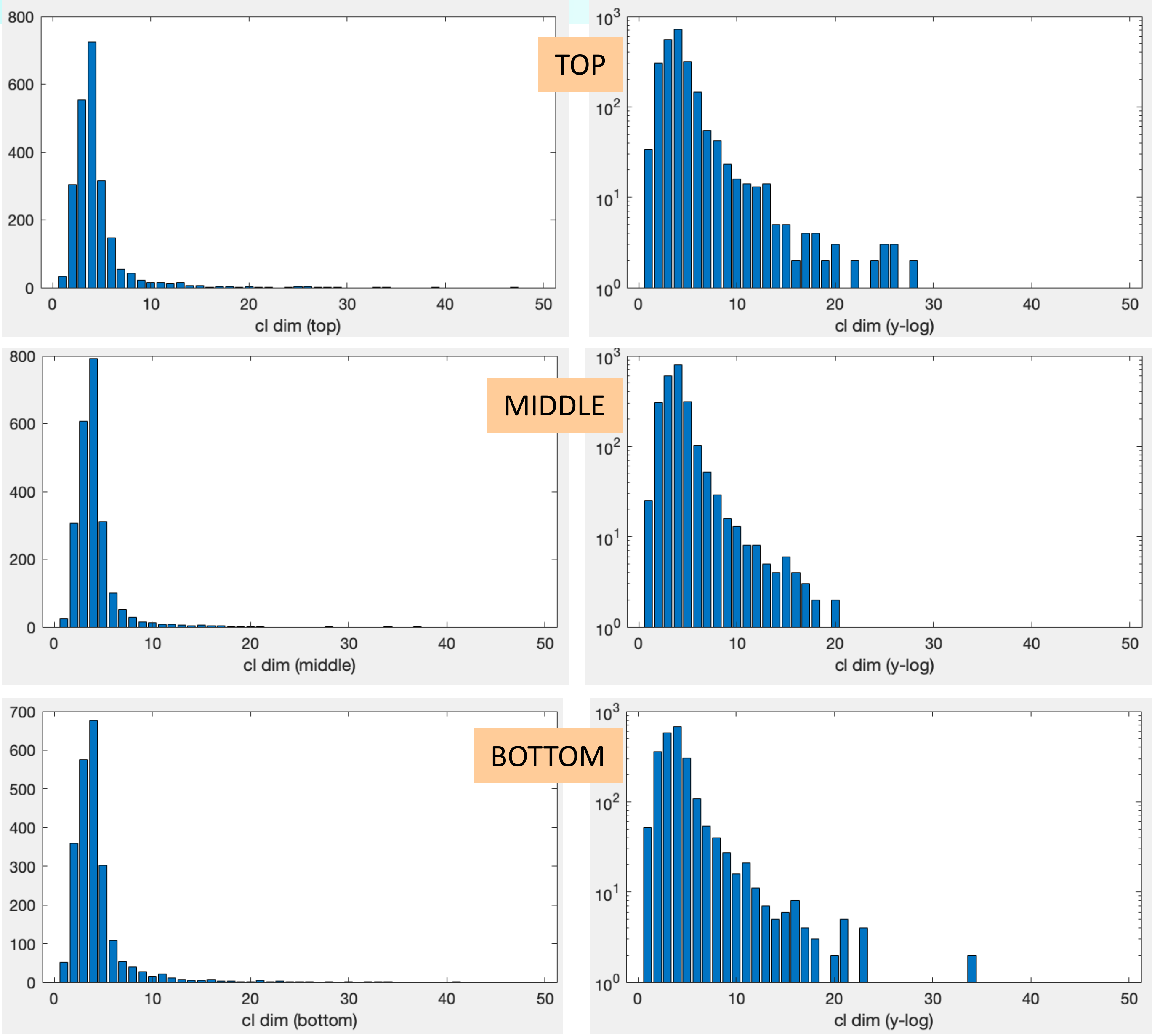


Cluster size

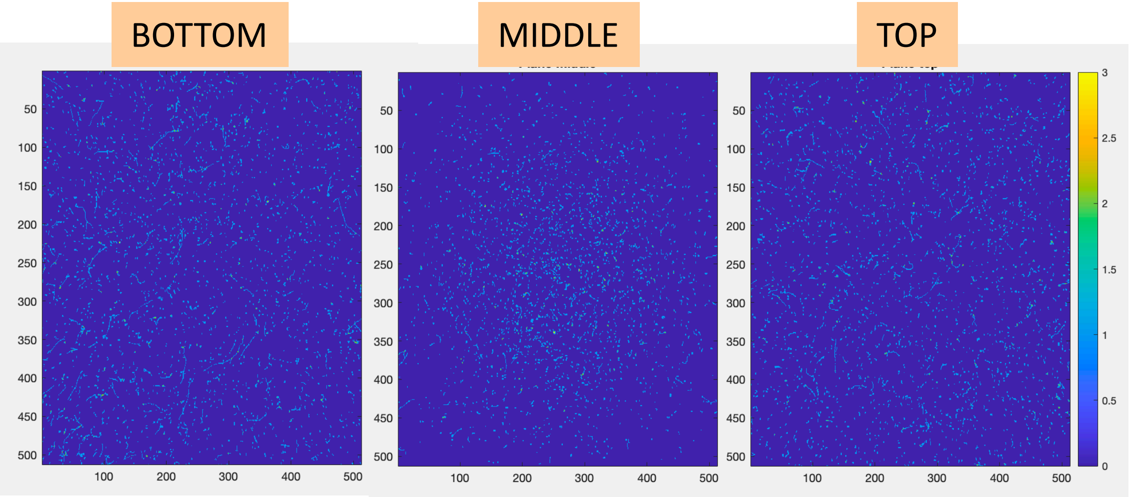
MPV = 4 pixels

more than 90% of clusters with less than 6 fired pixels

linear scale | log scale



matrices with synchronized data



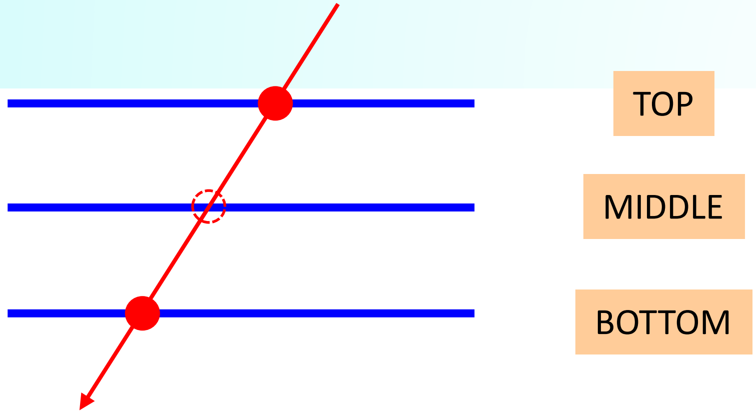
R. Santoro

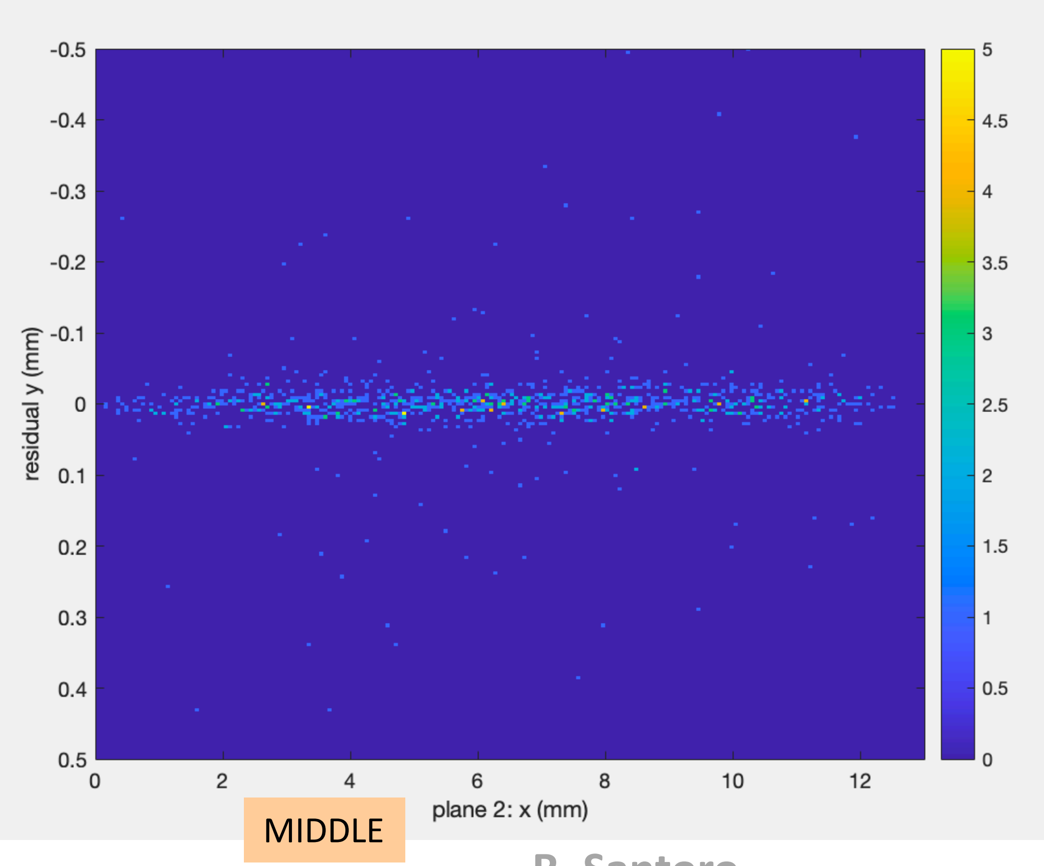
Residuals

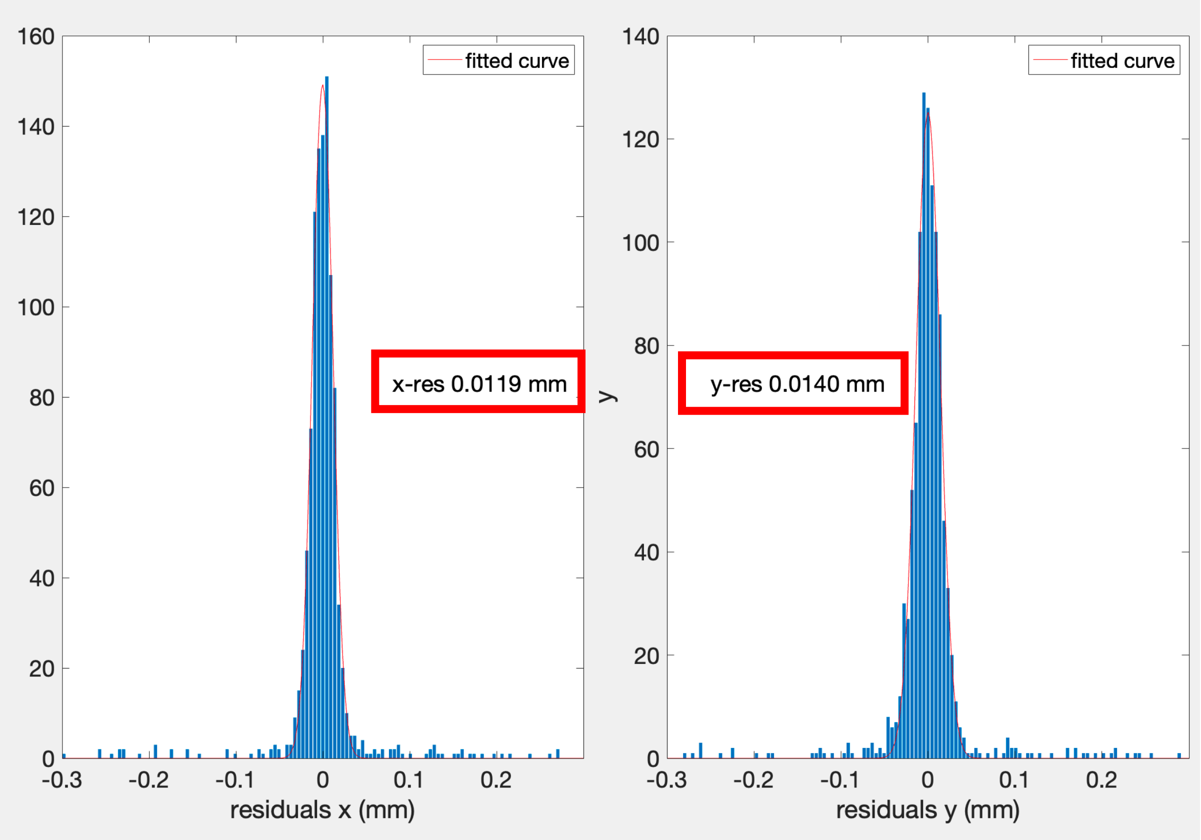
Selection criteria:

- 1 cluster per plane
- Δt <= 10 clock cycles
- cluster dimension <= 4 in tracking planes

Selected $\approx 46\%$ of the synchronized events







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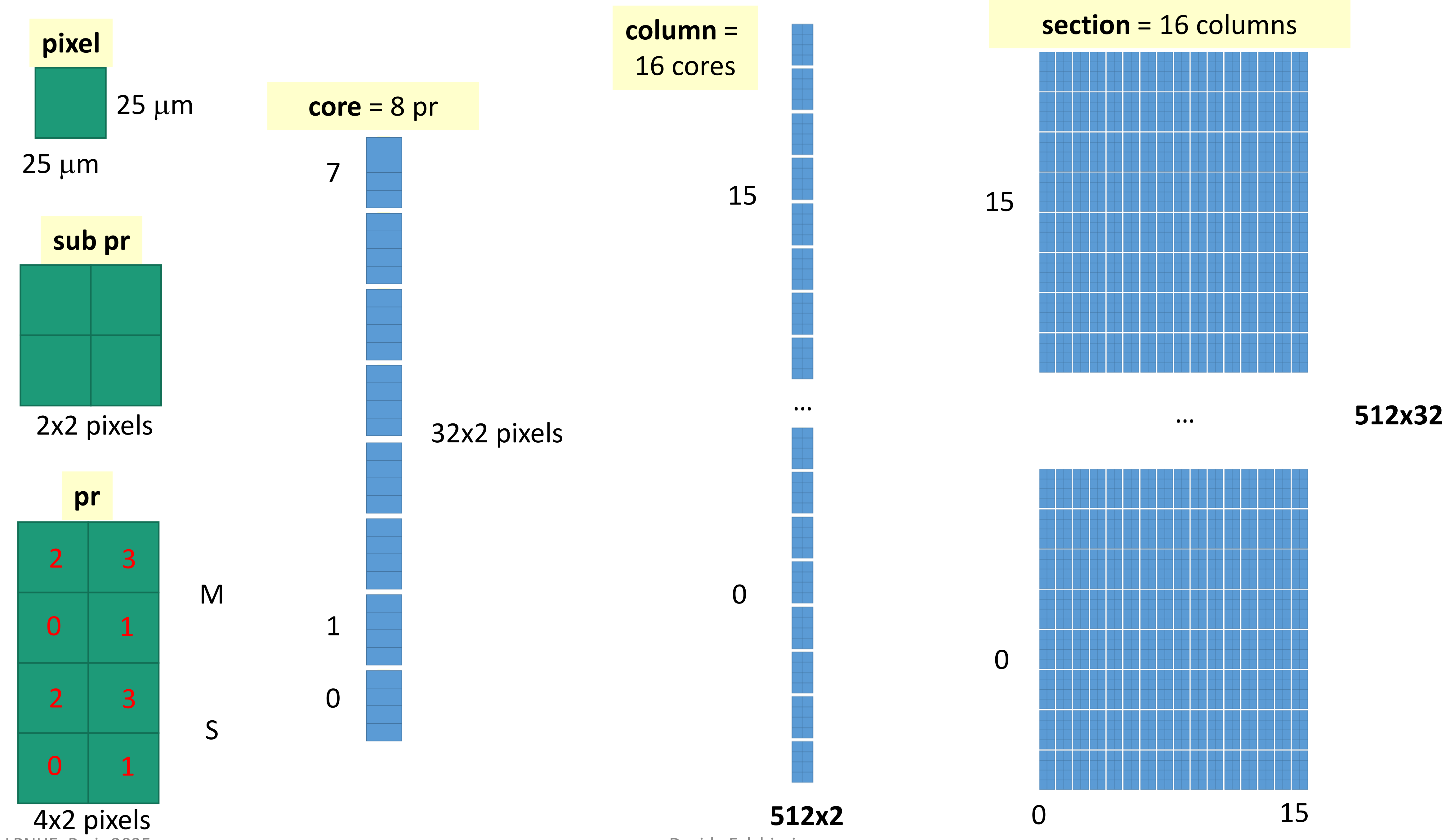
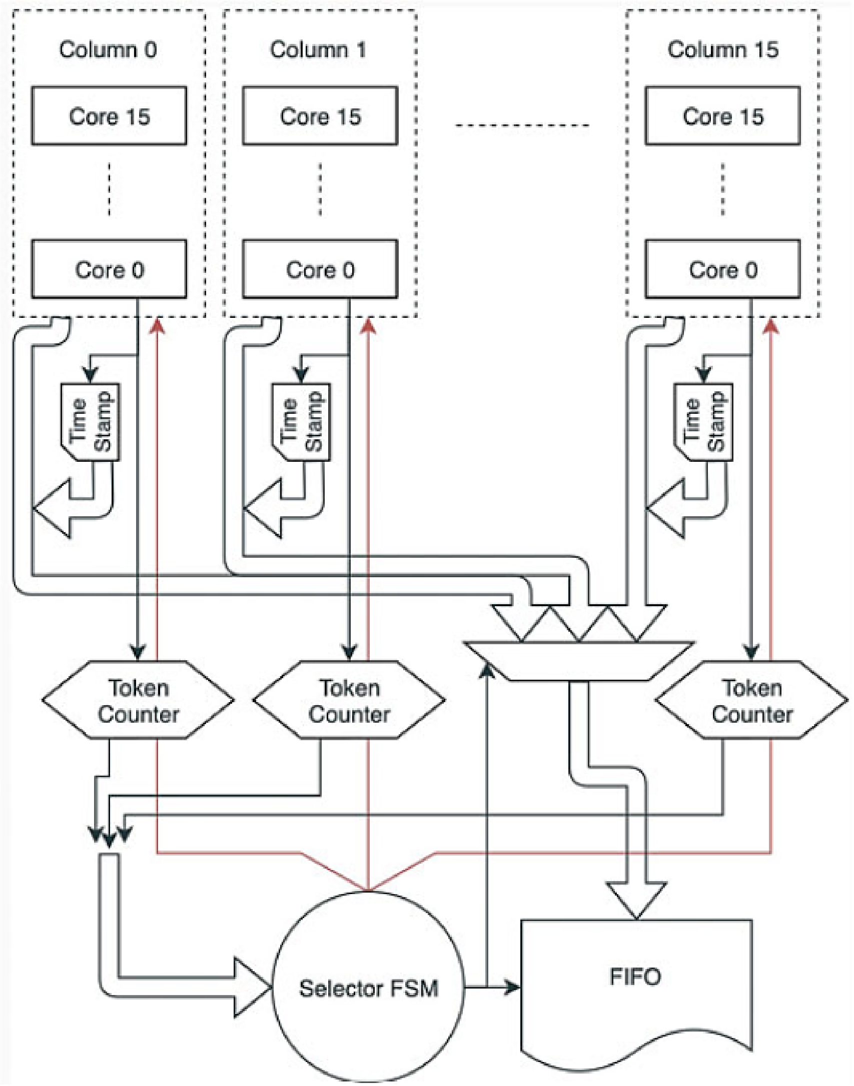

pixel
25 μm
25 μm
sub pr
2x2 pixels
pr
2 3
0 1
2 3
0 1
M
S
4x2 pixels
core = 8 pr
7
1
0
32x2 pixels
column = 16 cores
15
...
0
512x2
section = 16 columns
15
...
0
0
15
512x32

MD3: asynchronous architecture



frameless asynchronous readout with clockless matrix:

- if any **pixel** is **hit**, the pixel status register is set to high and the **full flag of the pixel region** is set.
- a **token chain** is created by summing the pixel region full flags starting from the top.
- the token signal is propagated to the **periphery section readout unit** and the timestamp is latched.
- the payload consisting of the column data, column address and timestamp is then sent to the **output FIFO** and will be sampled by the periphery circuits.

The 32-bit data words are 8B10B encoded in 40-bit packets and sent out via 320 MHz DDR serializers.