

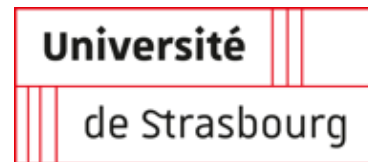
Development of MAPS with Intrinsic Amplification

A.Dorokhov on behalf of APICS project

IPHC/UdS C4Pi Strasbourg

18/11/2025

Bi-national conference on Detectors R&D



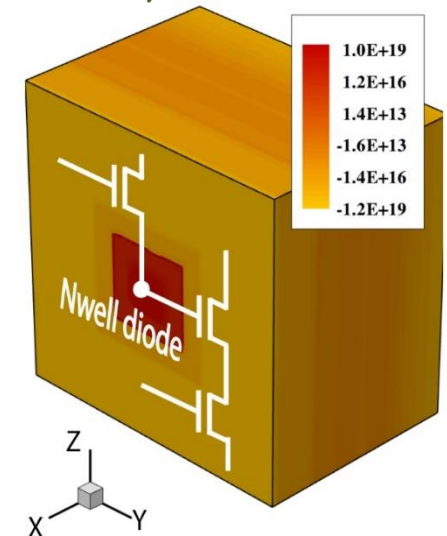
Sensor requirements for trackers in future experiments/upgrades

	Spatial resolution, μm	Consumption, mW/cm^2	Time resolution	Limit on FE power current, nA
ALICE3 tracker	10	20	100 ns	80
CBM Micro Vertex Detector	5	50	~ 25 ns	50
BELLE II VerteX Detector	15	50	~ 1 ns	450
LHCb Upstream Tracker	10	100	20 ns (1 μs)	400
FCCee VT/PID	10	20	1 ns / 100ps	80

CMOS pixels (MAPS) used as sensor

- ✓ Low material budget (<1 % X_0/layer)
- ✓ High granularity, enabling excellent spatial resolution (<10 μm)
- ✓ Low fabrication cost, CMOS technology

Image of one pixel containing sensing element (Nwell diode) and CMOS circuit, FE and readout



Assumptions:

- ✓ Expected pitch = $\text{sqrt}(12) \cdot \text{resolution}$
- ✓ FE current is 50% of total current
- ✓ Power $\sim 1.5\text{V}$

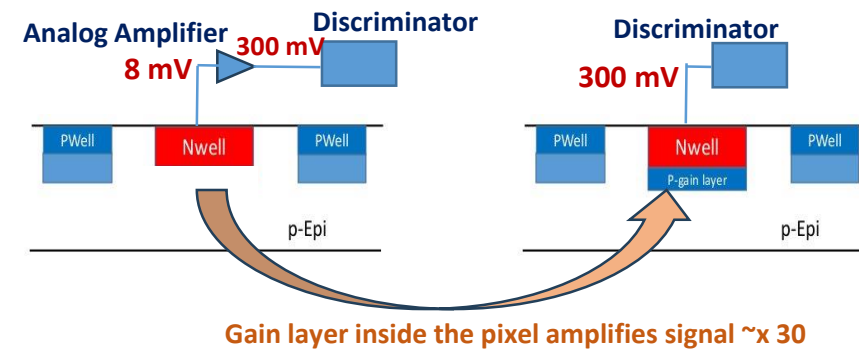
Same current, but 3 orders of timing:
What technology for analogue front end?

Typical FE in MAPS

CBM Micro Vertex Detector, real example, MIMOSIS2 chip:

1. Sensor thickness: $\sim 10\mu\text{m}$ \rightarrow sensor signal $\sim 800 - 2000e$ and due to charge sharing we need to detect $< 200 e$ signal
2. Input capacitance $\sim 4\text{ fF}$ \rightarrow $\sim 8\text{ mV}$ $\sim 10\text{ mV}$ input should be detected
3. For input of discriminator we need $\sim 300\text{ mV}$, $\sim 300\text{ mV}$

 FE voltage gain ~ 30



What if we would have 30 times more charge at the sensor?

We would no need FE at all (assuming input capacitance not changed much) ...



*Avalanche diodes can be used to multiply number of charges at the sensing node
Can we implement them in MAPS and what are the performances? \rightarrow APICS project*

APICS (Impact Amplification with CMOS pixel Sensor)

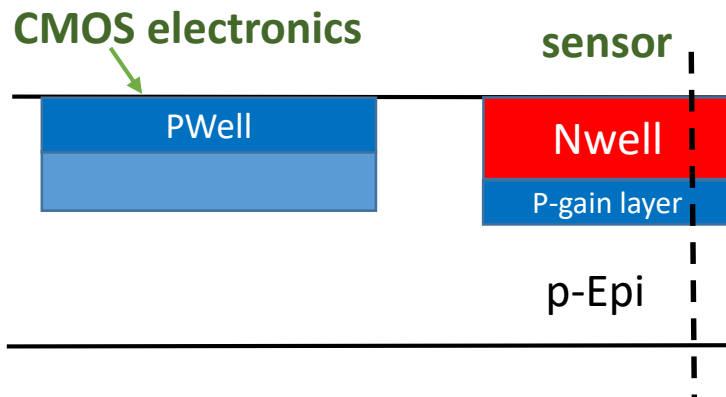
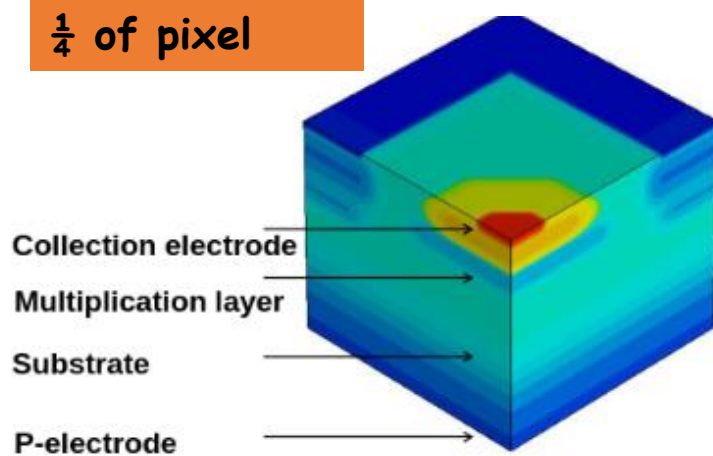
1. Simulate APD test structures, propose options for prototyping
2. Implement them in silicon, prepare for tests
3. Measure and compare with simulations: verify that we can match the required performances, make optimizations ...
4. Design complete pixel circuit with digital readout and characterize it in tests

Avalanche diodes

Challenges to achieve

/green: in general, red: in particular for APICS/:

1. Controlled gain $O(\sim 10)$
2. Charge collection efficiency (required nearly 100%)
3. Stability (temperature, power)
4. Low dark count rate, low noise
5. Radiation tolerance
6. Integrating to MAPS: fit high voltage device in CMOS circuit



Electric field $>10^5$
impact ionization



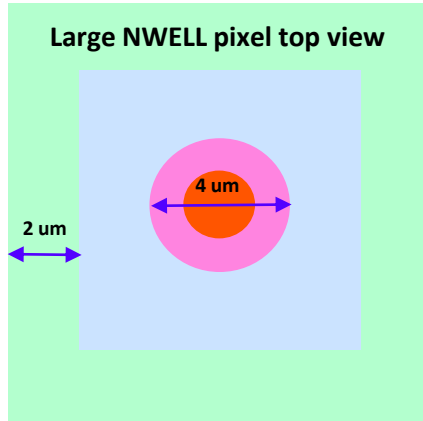
Advantages/benefits:

1. No FE: smaller pitch -> better spatial resolution
2. Lower power consumption -> more digital processing
3. Faster response: usually FE slope ~ 10 ns, without FE can be <1 ns

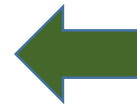
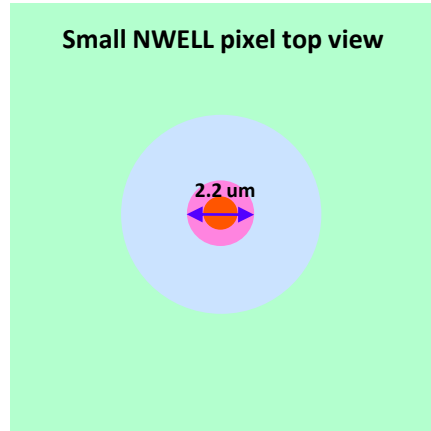
For some applications (picoseconds timing) may be the only way to go...

Avalanche diode structures simulated with TCAD

Structure 1

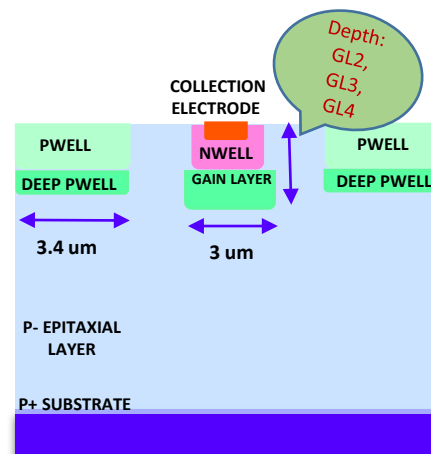
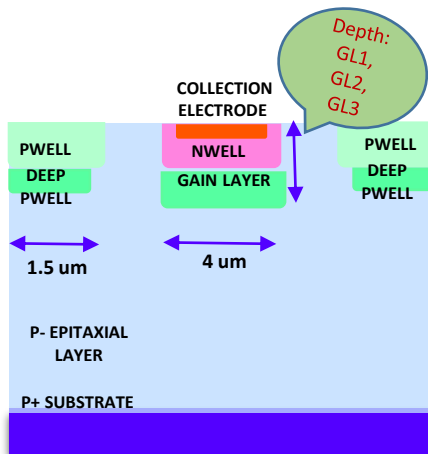


Structure 2



Considerations for geometry:

1. Reasonable pitch for majority of applications (15μm) and substrate (18μm)
2. Test several gain layer options, provided that we have limited number of tests structures
3. Compatibility with technology and design rules (180 nm) – makes some combinations not possible



Gain layer options:

changing depth of doping profile -> No info on exact doping : the expected closest options are: **Structure1(GL1)** and **Structure2(GL3)**

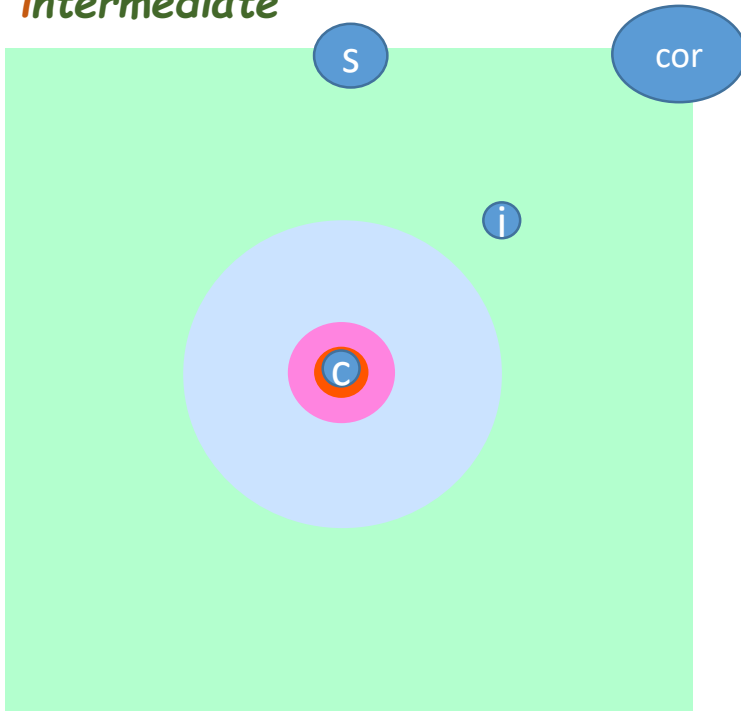
Simulation procedure

1. Build **3D mesh** with general doping profiles
2. Vary bias voltage (V) for DC and AC analysis:
 - ✓ and obtain **$I(V)$ curve**
 - ✓ determine sensor **capacitance $C(V)$**
3. For each bias voltage -> Transient analysis: $I(\text{time})$ - in response to m.i.p., collected charge **$Q(V) = \int I(\text{time})$**

SYNOPSYS® TCAD: Sentaurus structure/mesh editor and device simulator



- ✓ m.i.p. track is perpendicular to sensor and strikes at several fixed positions: **center**, **corner**, **side** and **intermediate**



$$\text{Gain (V)} = \frac{Q(V)}{Q \text{ (generated by m.i.p. and could be potentially collected by the pixel)}}$$

↳ the measure of multiplication, at low voltages ~ 1

$$\text{Signal(V)} = \frac{Q(V)}{C(V)}$$

From m.i.p. particle and taking into account of charge sharing and multiplication

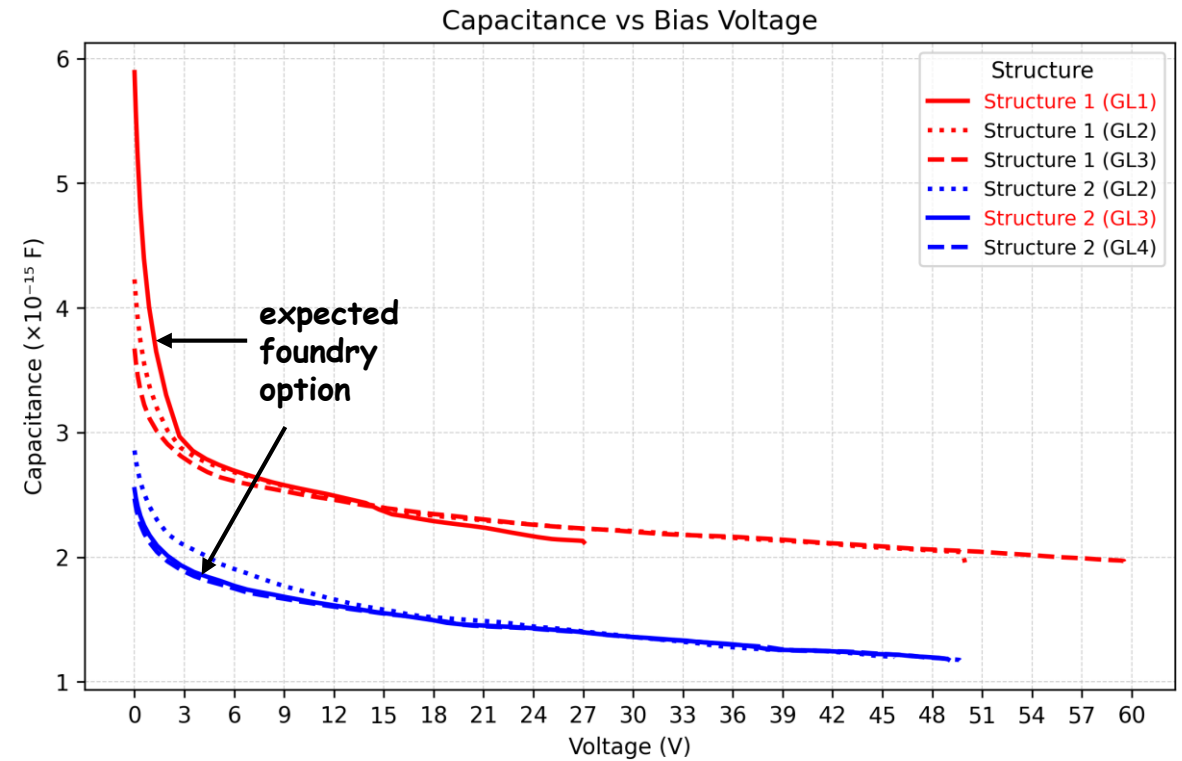
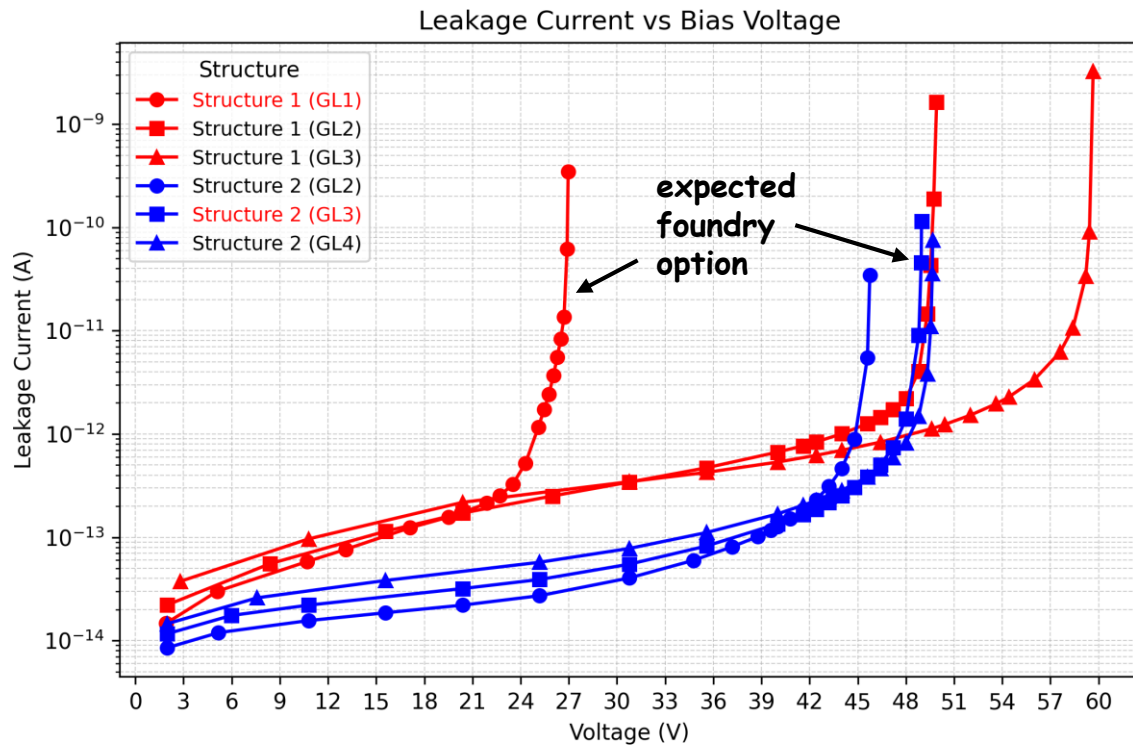


real voltage signal at sensing node for m.p.v. of m.i.p. particle

Results for DC/AC simulation I-V, C-V curves

- ✓ For diode without gain typical leakage current $< 1\text{pA}$, so the FE circuit should compensate it
- ✓ In case of APD, the current limit can be relaxed: we do not have FE, but dedicated compensation circuit, so we accept $< 1\text{nA}$, which happens nearly at breakdown

- ✓ Typical diode capacitance at low voltage $< 4\text{fF}$ and it is getting smaller with voltage
- ✓ It is not changing much in APD working range $> 20\text{ V}$ for all structures and gain layers

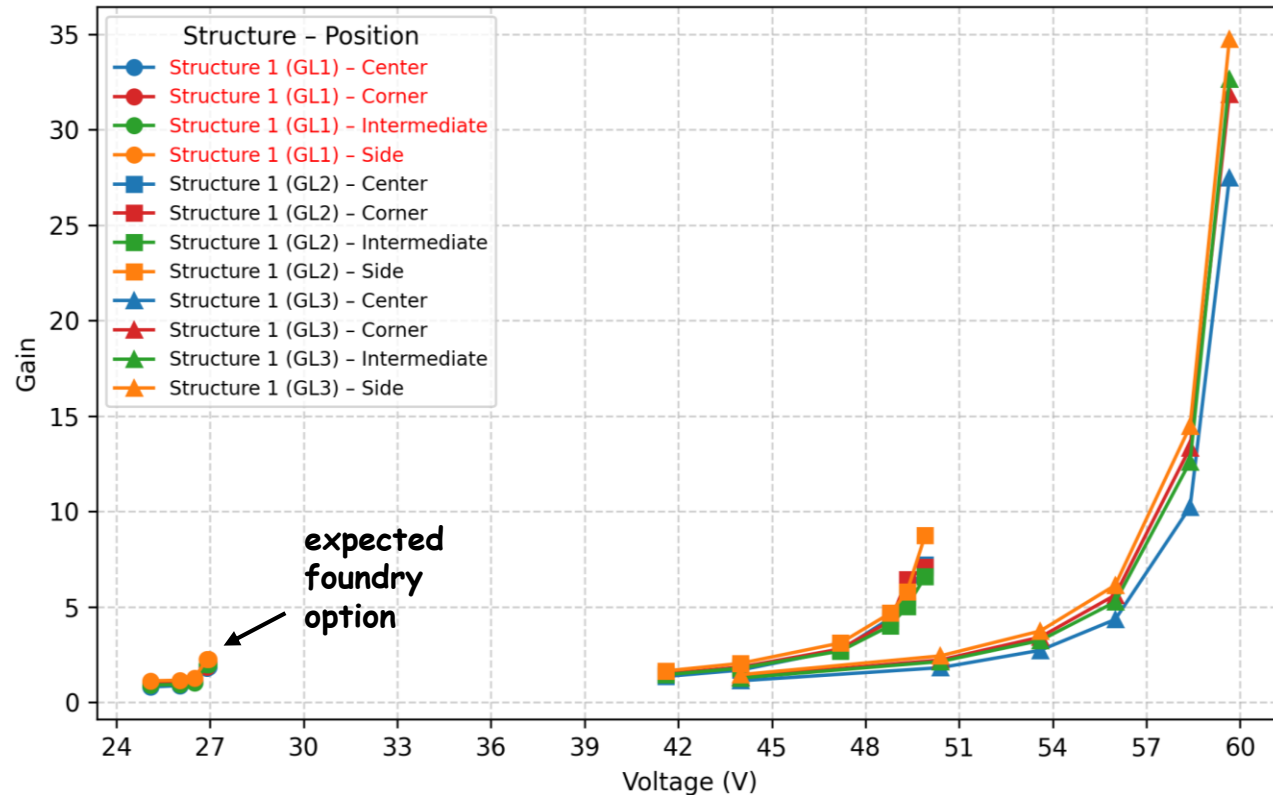


expected foundry options: *Structure1(GL1)* and *Structure2(GL3)*, but if GL varied still OK ➔ First checkpoint passed -> gain?

Results for transient simulation

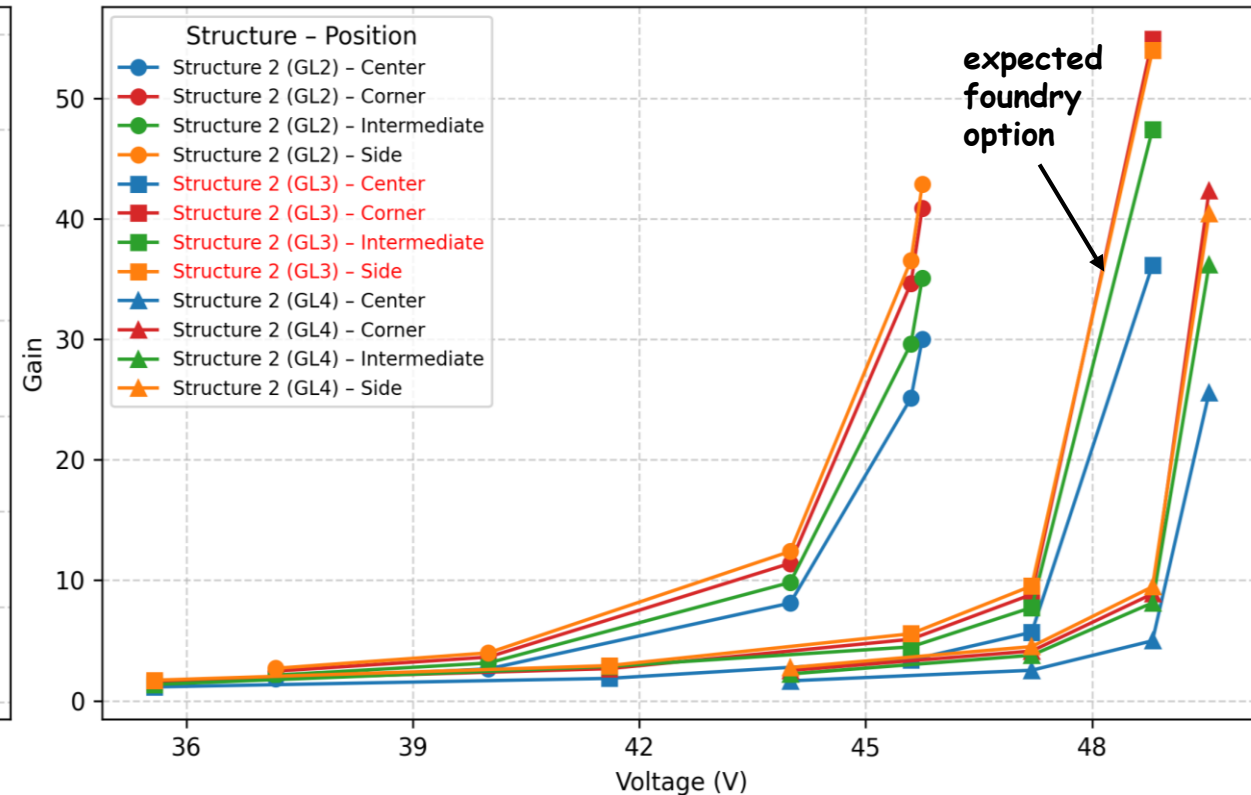
To work without FE, we need gain ~30

Avalanche Gain vs Voltage — Structure 1 & Variants



Geometry of Structure 1 is at the limit of acceptance, but if real gain layer doping profile is closer to GL2 still OK

Avalanche Gain vs Voltage — Structure 2 & Variants

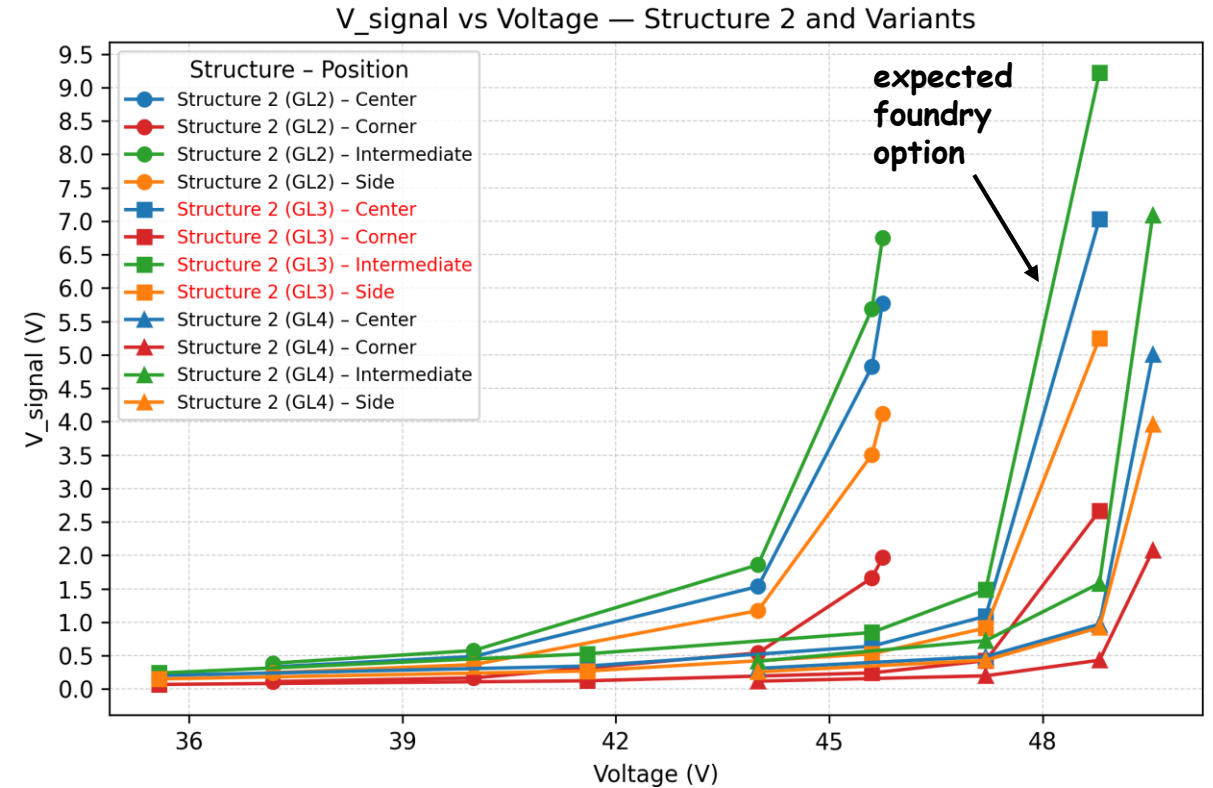
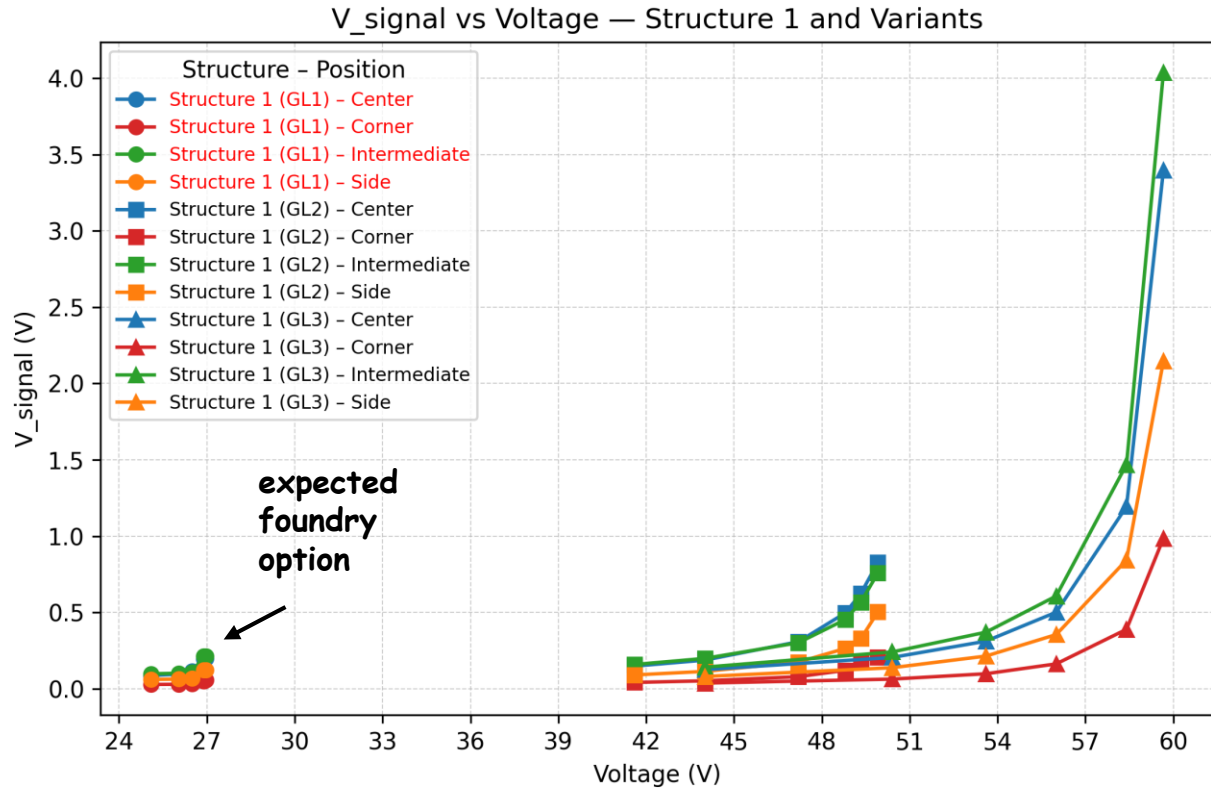


Structure 2 seems to be OK, even if GL varied, we can find the biasing which provides required gain

In all cases, we have sufficient gain for all particle track positions -> good efficiency for all tracks expected

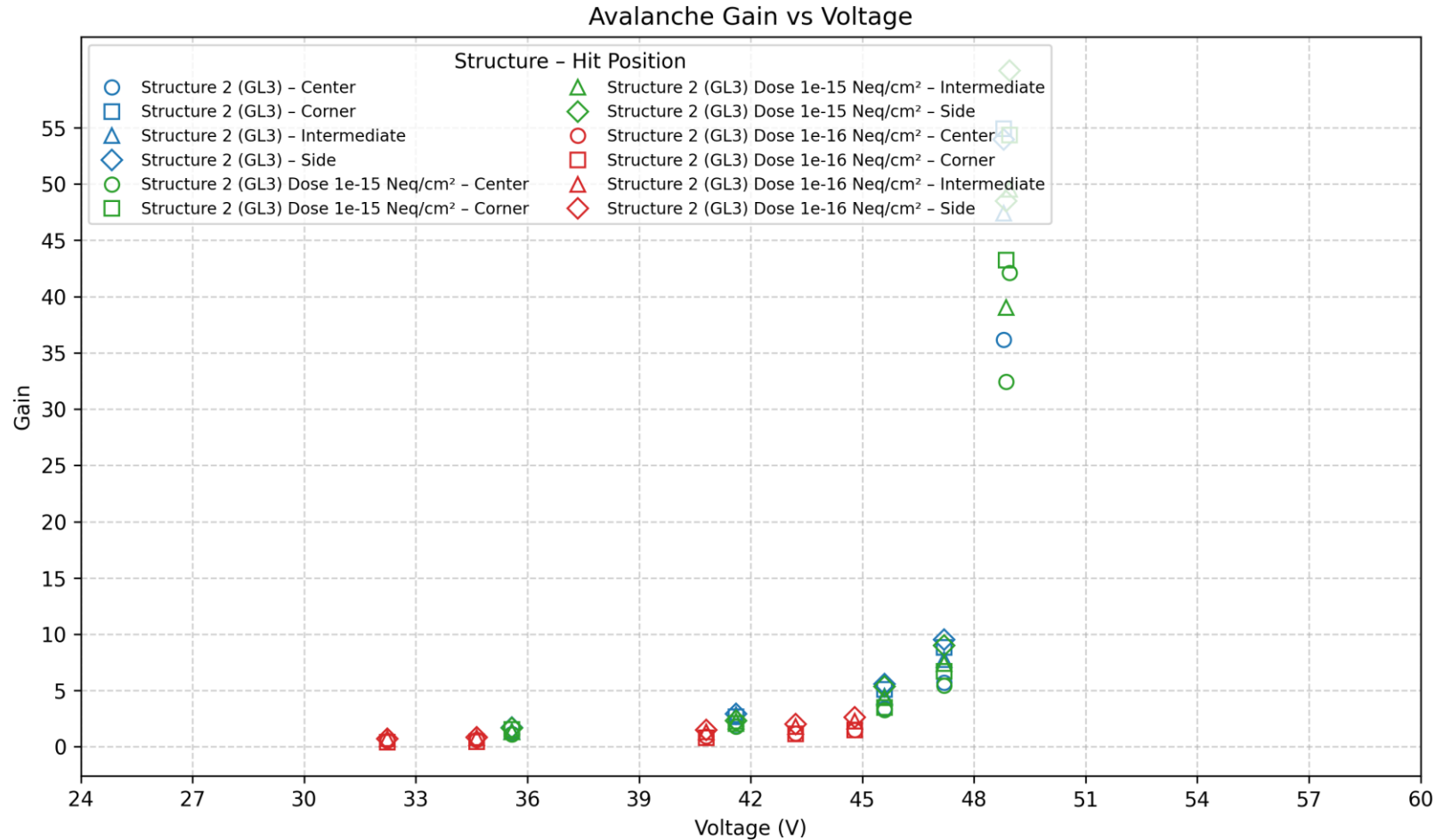
Results for transient simulation

To work without FE, we need ~300mV for simple discriminator



In all cases, we have sufficient voltage for discriminator, except structure1(GL1) which is at limit for our expectation of GL- \rightarrow not necessary precise, so still would check it

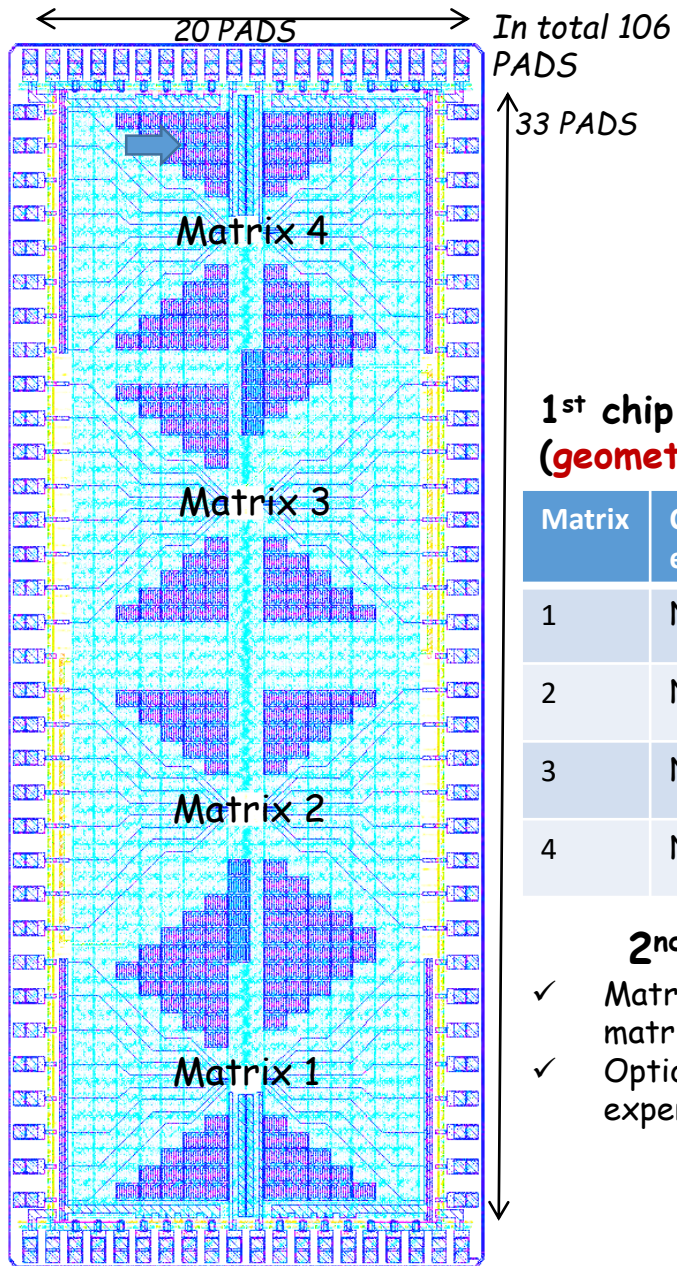
Results for transient simulation after damage from neutron irradiation



Perugia model for traps: F. Moscatelli et al., IEEE Trans. Nucl. Sci. 64 (2017) 2259

Ongoing simulations,
Preliminary results:
Gain is OK for up to
1e15neq/cm2

Chip submission Q4/2025



In total 106 PADS
33 PADS

- ✓ 2 chips of size ~2 X 5 mm
- ✓ in each chip 4 matrixes of 8x8 pixels of 15umx15um
- ✓ only internal part of matrix (4x4) read-out

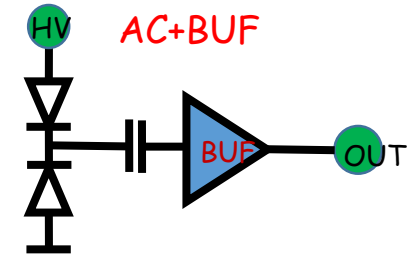
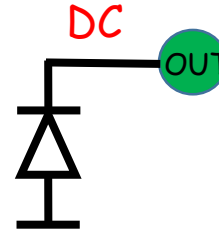
1st chip - Matrixes (geometry from simulations)

Matrix	Collection electrode	Gain layer	Circuit
1	Nwell, r=4um	GL1	AC+BUF
2	Nwell, r=4um	GL1	DC
3	Nwell, r=2.2um	GL3	DC
4	Nwell, r=2.2um	GL3	AC+BUF

2nd chip -

- ✓ Matrix 1 and 2 but with n-implant under matrix
- ✓ Optional 3 and 4 with n-implant and some experimental circuits (from KEK)

Readout variants: DC and AC with buffer



Parasitic capacitance is > 1000 compared to APD

Parasitic capacitance is comparable to APD



Use for depletion, leakage current study + laser pulse

Use for tests with particles

Conclusions & Future Work

1. Feasibility of introduction of APD structures into MAPS technology is confirmed by TCAD simulations: gain >30, pitch 15um, standard CMOS process, bias voltage 30.. 50V
2. The simulations guided the design choices : optimal gain layer width and electrode configurations: two chips are designed ready for submission

Next and ongoing steps:

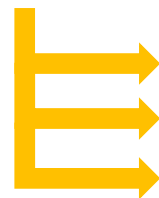
- Completion the study for radiation tolerance
- Development test system for measurements (current range from fA to uA)
- Characterization the structures which are fabricated within APICS and other (CASSIA) projects, comparison data with simulations
- Development the concept and design of next test chip with pixel circuitry, digital readout

Extra slides

Motivation-Overview of CPS Projects

Project	Year	Technology	Pitch	Spatial Res.	Time Res.	Power dissipation	Application
MIMOSIS	2025	TJ180 nm	~28 μm	~5 μm	~5 μs	<100 mW/cm ²	Vertex detector (CBM)
OBELIX	2027	TJ180 nm	~30 μm	~15 μm	~100 ns	<200 mW/cm ²	Tracking/counting (Belle II)
MOSAIX	2026	TPSCO 65 nm	~22 μm	~4 μm	~5 μs	<40 mW/cm²	ALICE ITS3
OCTOPUS	2028	TPSCO 65 nm	<20 μm	~3 μm	~5 ns	<50 mW/cm ²	FCCee collider
TRACKER	2028	TPSCO 65 nm	~25 μm	~10 μm	~100 ps	TBD	FCCee collider

Applications are becoming more demanding — driving the need for advanced CPS designs that require:



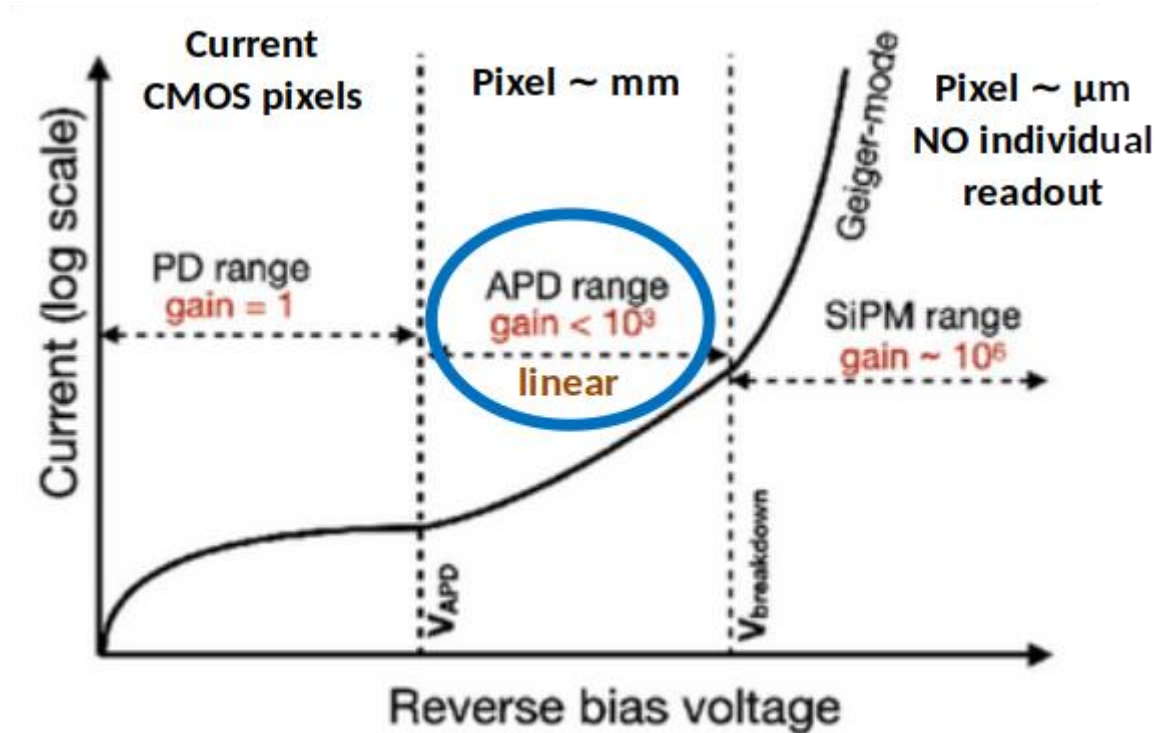
Smaller pixel pitch (higher spatial resolution)

Improved timing performance

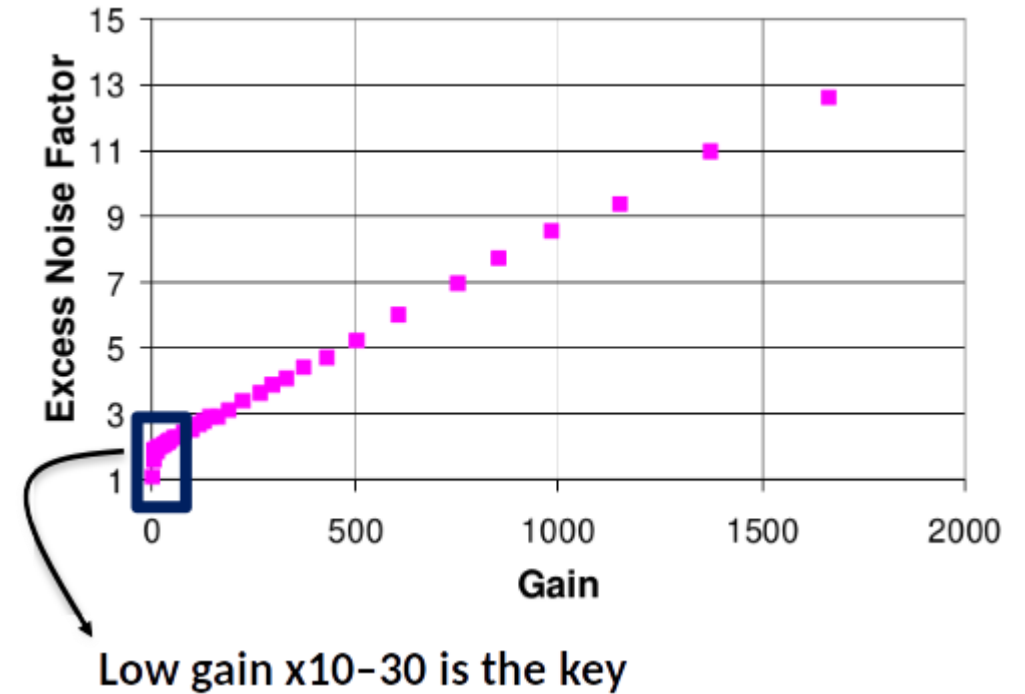
Lower power consumption

A Closer Look at Pixel Amplification Challenges

- Amplifications in small (10 μm) pixels ?



- Additional noise / thermal noise

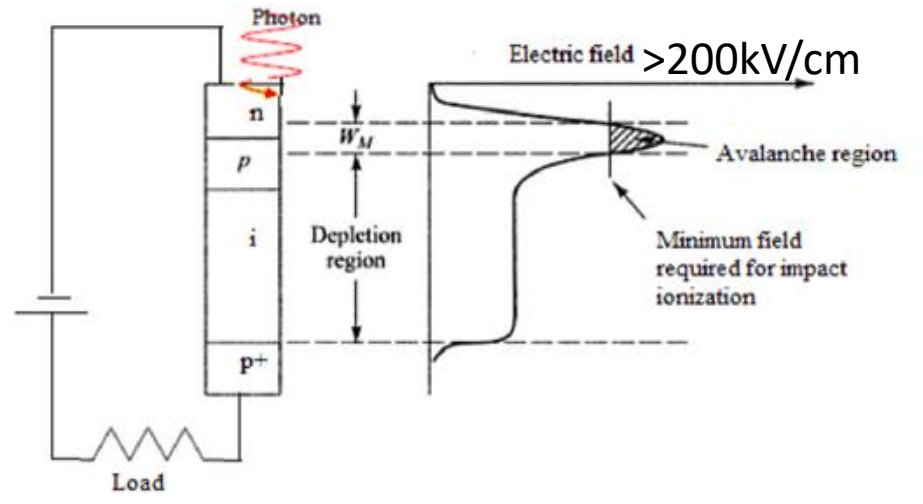
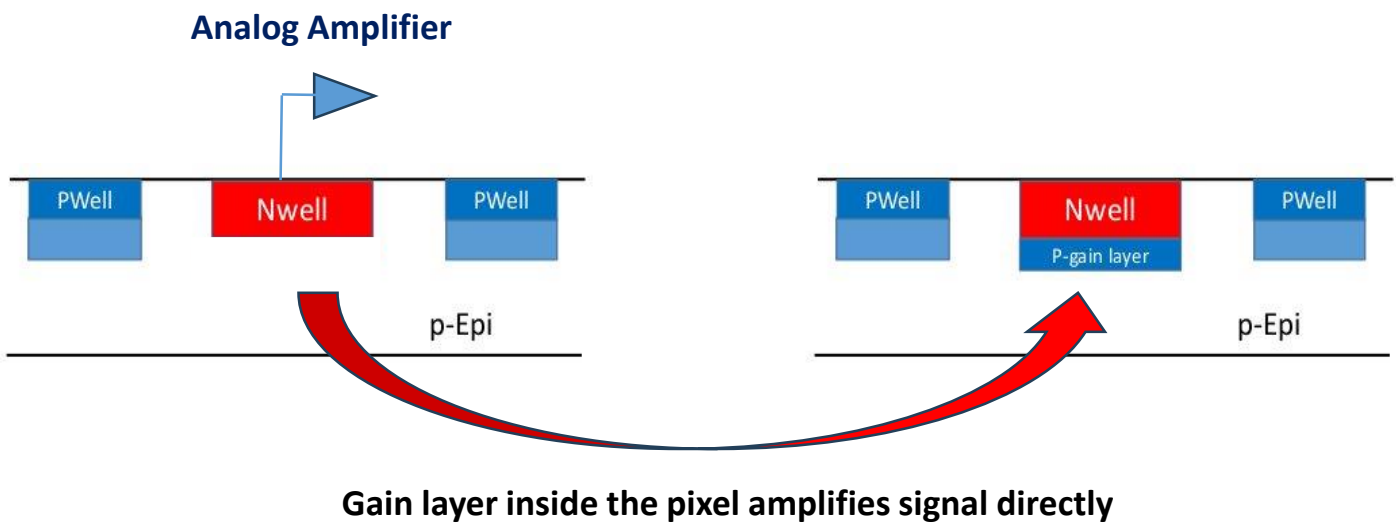


Issues with shrinking pixel size:

Border conditions
Uniformity over matrix

Internal Amplification as the Solution

- In-silicon amplification => no need for electronic amplifier



1500 e-
↓
 $\Delta V \sim 100 \text{ mV}$

1500 e-
↓
 $\Delta V \sim 1000 \text{ mV}$
trigs digital cell

This allows us to:
Gain on area
Gain on power dissipation