# TCAD Optimization of MAPS with Internal Low-Gain Amplification

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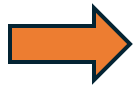
20 June 2025, GDR DI2I, Lyon

# Outline

1. **Motivation & Objectives**
   - Overview of CPS projects
   - Why internal amplification is needed



**APICS Project**

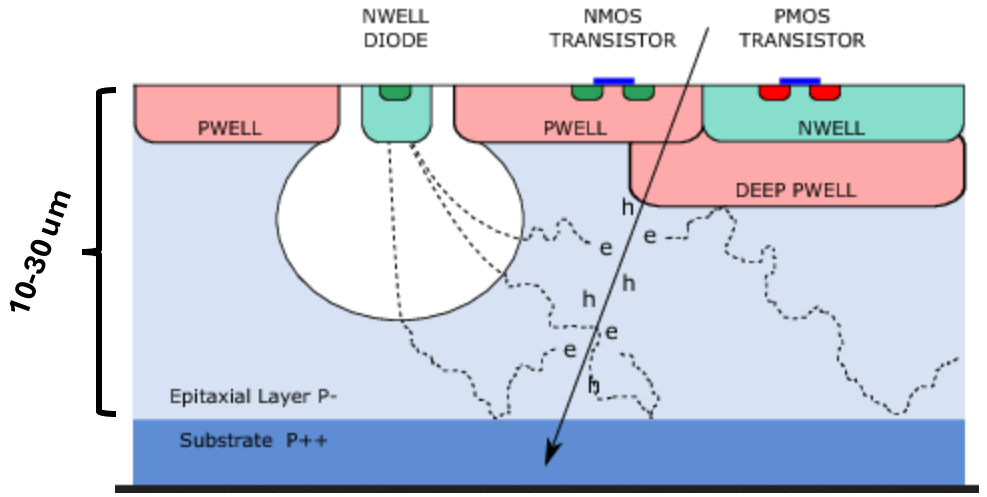
2. **Methodology-Initial step**
   - CERN prototypes (Measurements & Simulations)
3. **Simulated Structure & Electrical Characterization**
4. **Conclusion & Future Work**

# Motivation-CMOS Pixel Sensors (CPS) in Particle Detection

CPS are devices for charged particle or light detection where sensor and readout electronics are implemented in single chip

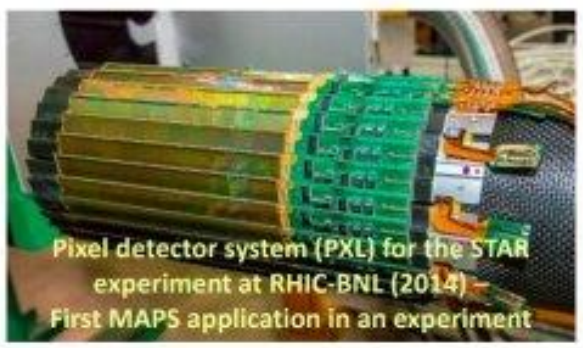
Main Advantages:

- **Low material budget** (<1 % X0/layer)
- **High granularity**, enabling excellent **spatial resolution** (<10 µm)
- **Low fabrication cost**
- **Fast evolution** of the CMOS technology provided by the industry



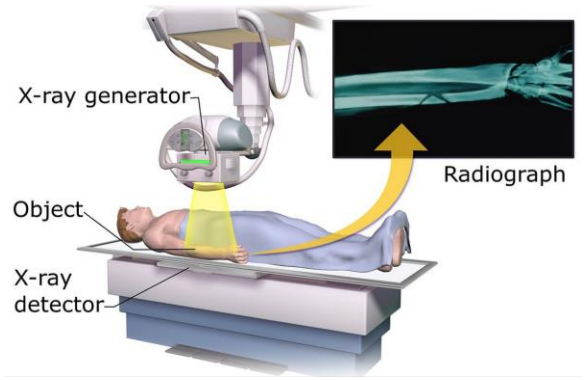

Widely used in:

Vertex and tracking detectors (ALICE ITS2, CBM, Belle II, etc..)





X-ray radiography and Industrial applications



# Motivation-Overview of CPS Projects

| Project | Year | Technology | Pitch | Spatial Res. | Time Res. | Power dissipation | Application |
|---|---|---|---|---|---|---|---|
| MIMOSIS | 2025 | TJ180 nm | ~28 um | ~5 µm | ~5 µs | <100 mW/cm$^2$ | Vertex detector (CBM) |
| OBELIX | 2027 | TJ180 nm | ~30 um | ~15 µm | ~100 ns | <200 mW/cm$^2$ | Tracking/counting (Belle II) |
| MOSAIX | 2026 | TPSCO 65 nm | ~22 um | ~4 um | ~5 us | **<40 mW/cm$^2$** | ALICE ITS3 |
| OCTOPUS | 2028 | TPSCO 65 nm | **<20 um** | **~3 um** | ~5 ns | <50 mW/cm$^2$ | FCCee collider |
| TRACKER | 2028 | TPSCO 65 nm | ~25 um | ~10 um | **~100 ps** | TBD | FCCee collider |

Applications are becoming more demanding — driving the need for advanced CPS designs that require:

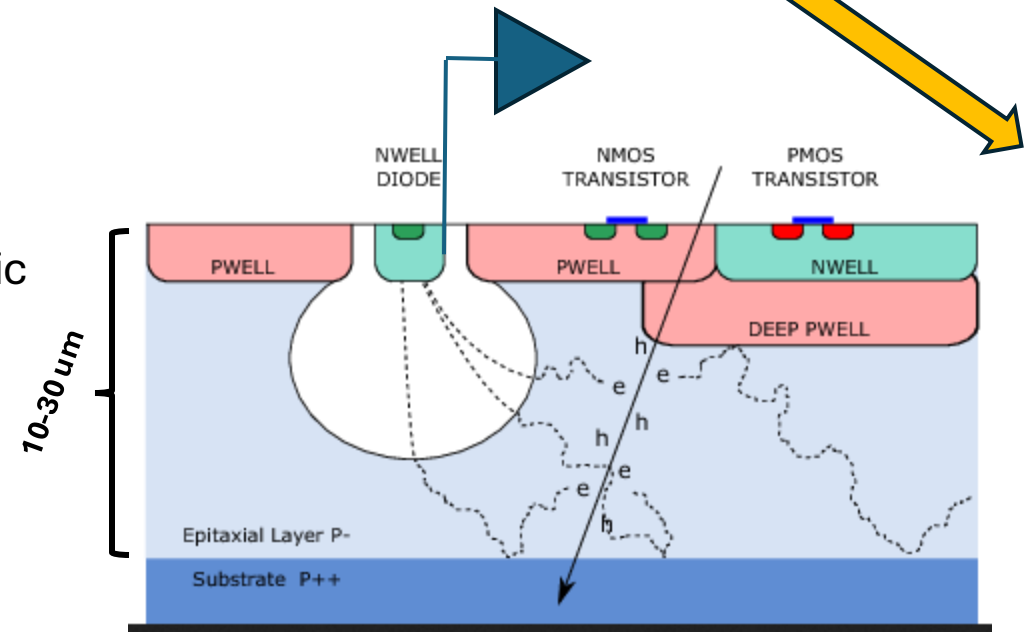
- **Smaller pixel pitch** (higher spatial resolution)
- **Improved timing performance**
- **Lower power consumption**

# Motivation-Technological Constraints in Advanced CPS Design

- Sensitive layer : 10-30 µm
- Charge from a MIP (minimum ionizing particle): ~600-1800 e-

↳ Signal too small to detect directly

↳ Requires electronic amplification




**Power Cost**

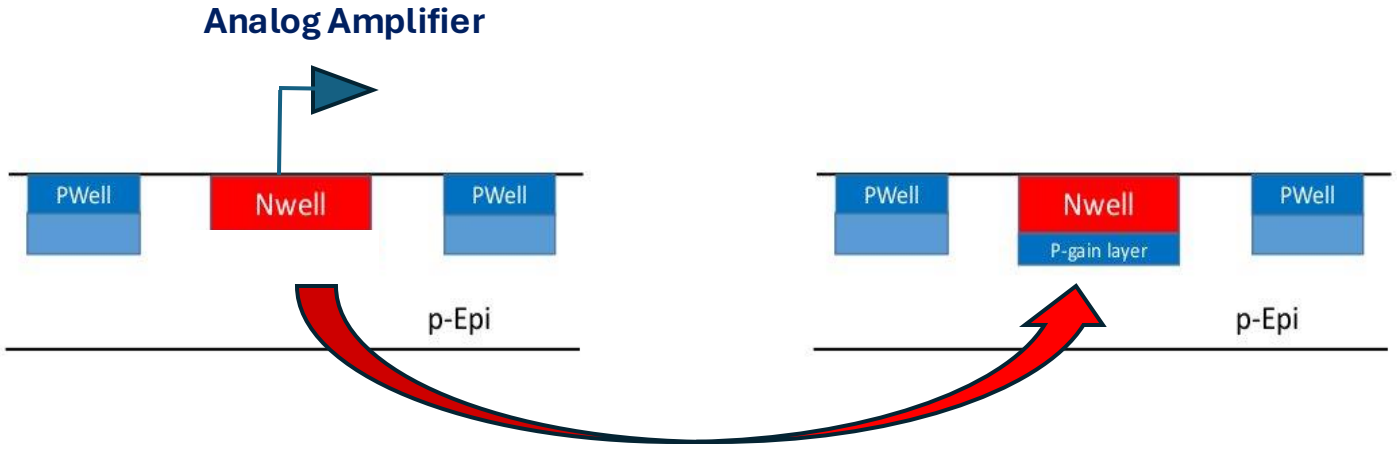
Hard to go below **50 mW/cm²** while maintaining nanosecond level timing performance

**Area Cost**

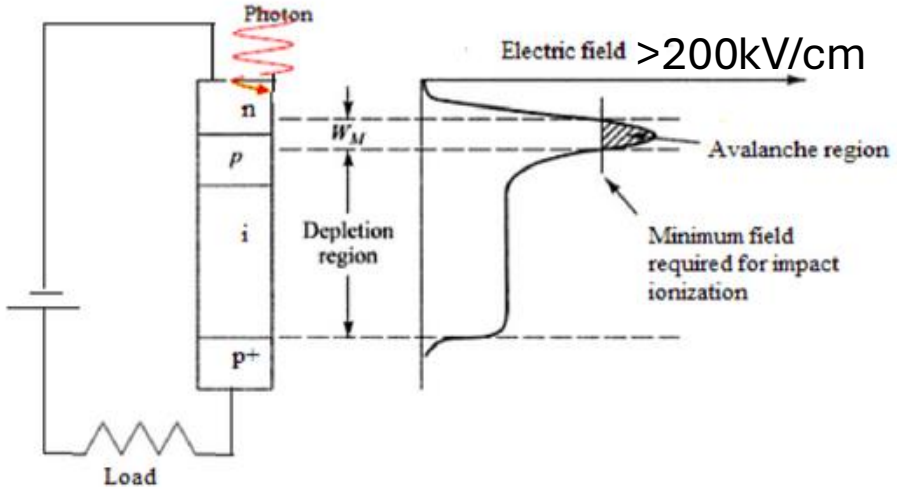
Limits ability to shrink **pitch below 20 µm**

# Internal Amplification as the Solution

- **In-silicon amplification => no need for electronic amplifier**




**Gain layer inside the pixel amplifies signal directly**



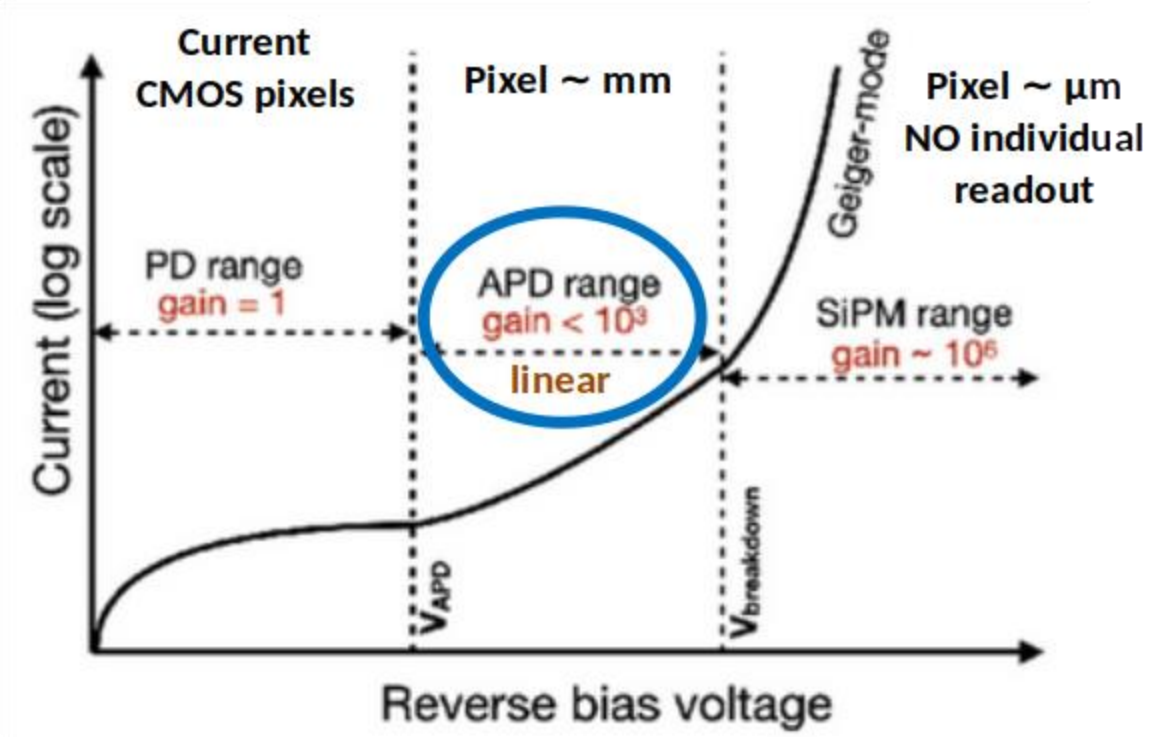

1500 e-
↓
ΔV ~ 100 mV

1500 e-
↓
ΔV ~ 1000 mV
trigs digital cell

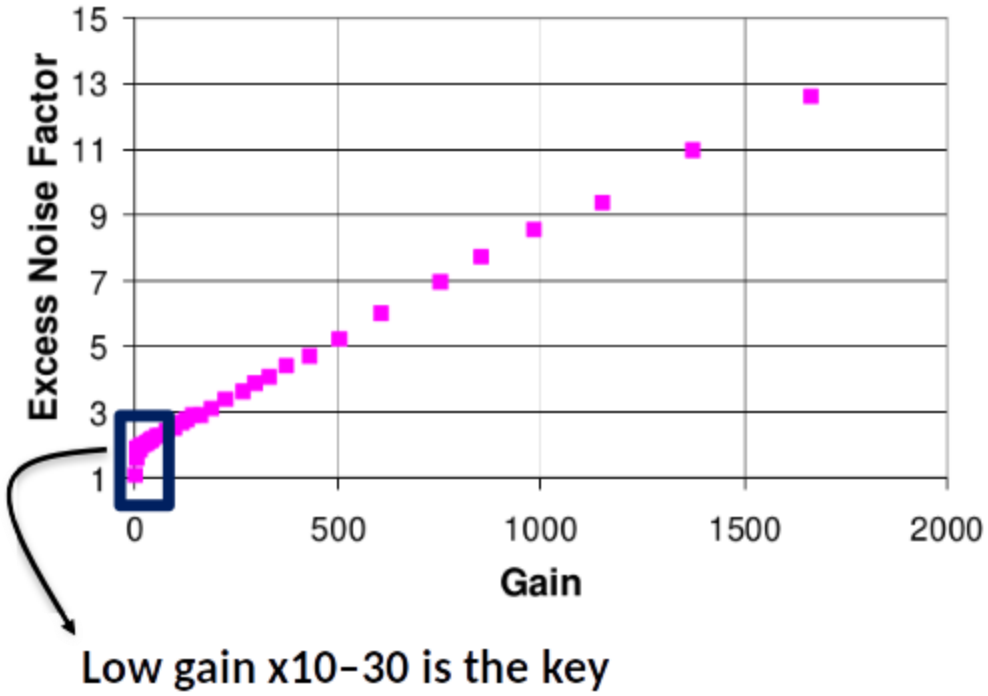
**This allows us to:**
**Gain on area**
**Gain on power dissipation**

# A Closer Look at Pixel Amplification Challenges

- **Amplifications in small (10 µm) pixels ?**




- **Additional noise / thermal noise**



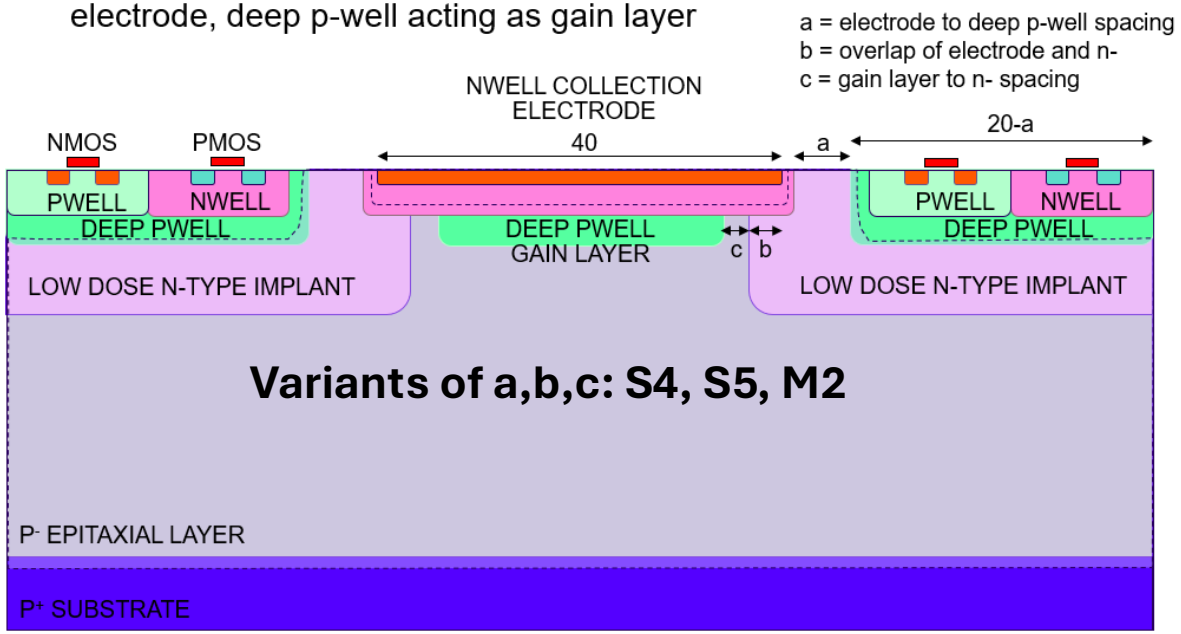

**Issues with shrinking pixel size:** Border conditions
Uniformity over matrix

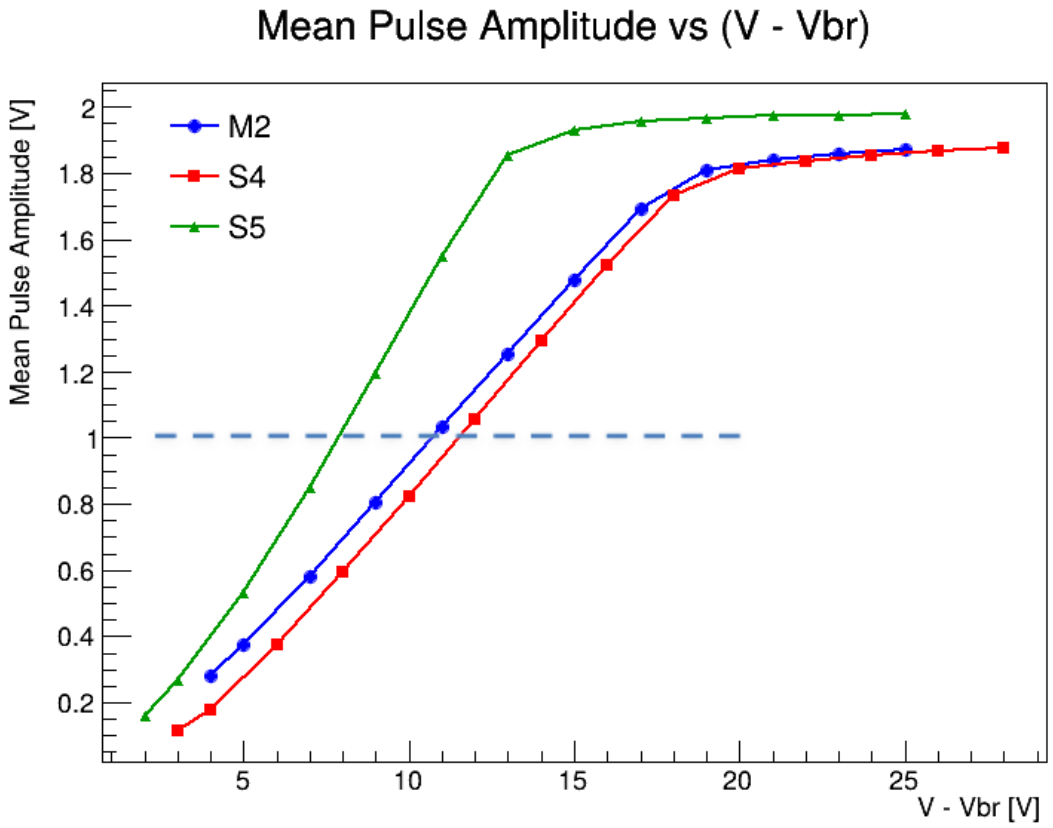
# Methodology & Initial step

- **R&D Steps:** Simulations , design/fabrication , tests

- **Prototypes from CERN – 2024 (CASSIA Project)**
  - Larger pitch ~ 80 μm

- gap in low-dose n-type implant underneath n-well collection electrode, deep p-well acting as gain layer

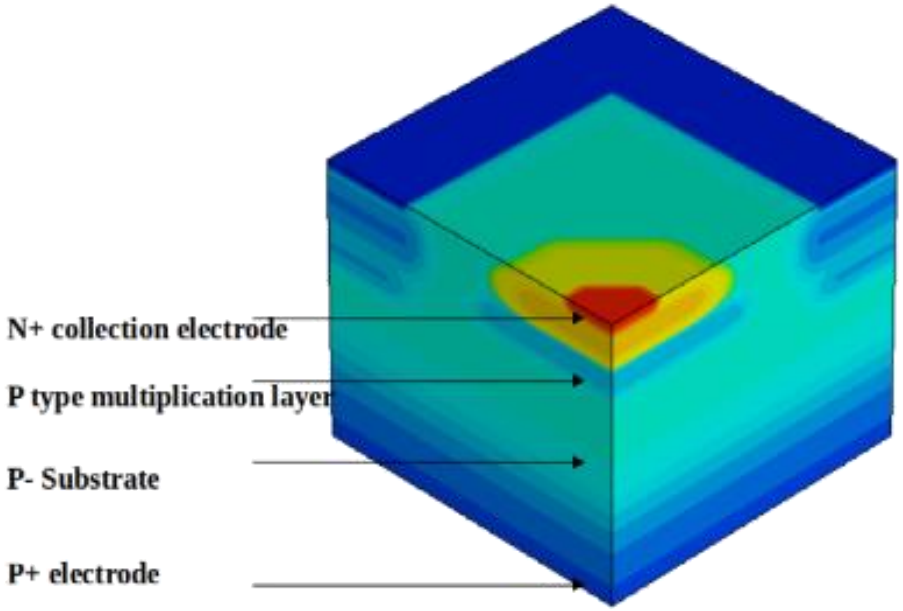


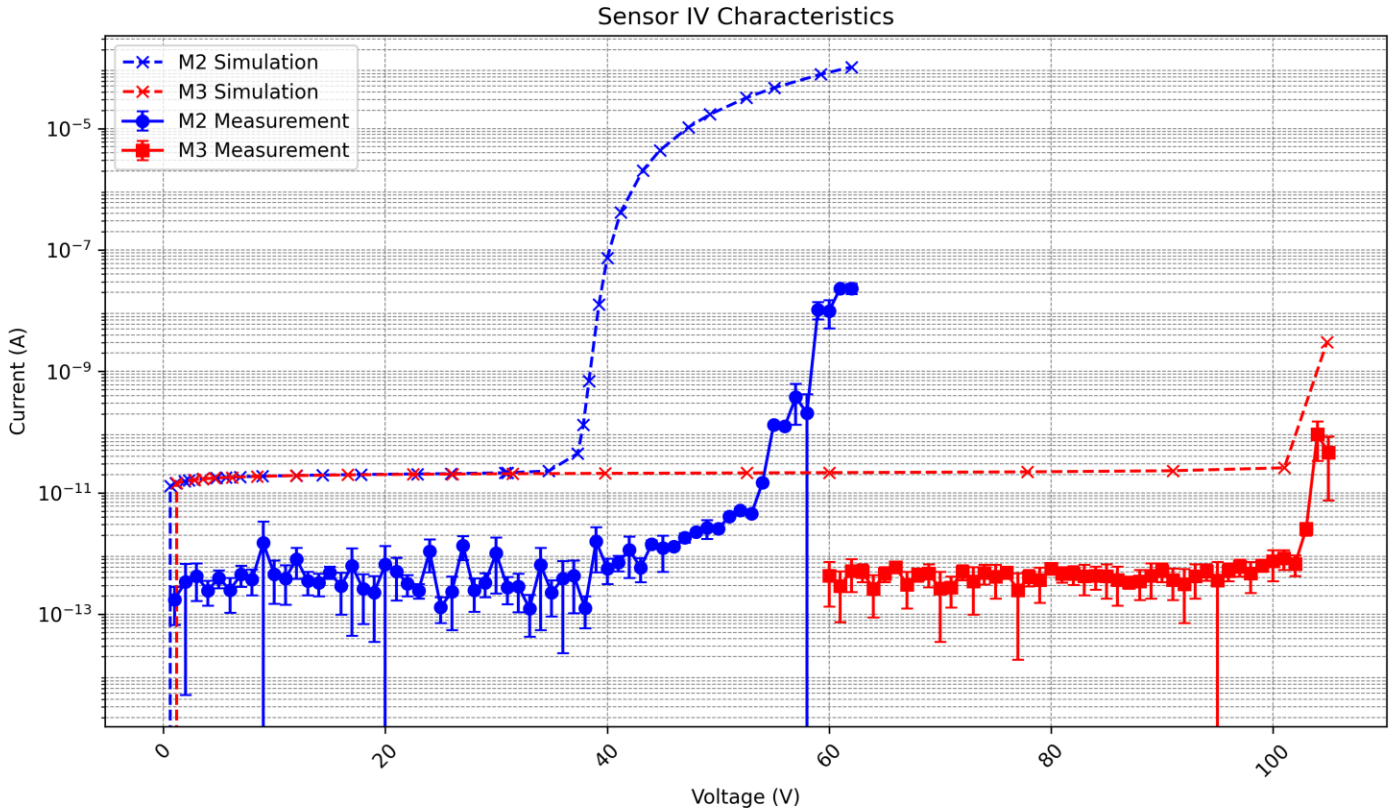




**Laser test ==>**

# Matching TCAD Simulations with Measured Data

**Baseline assumptions doping profiles**



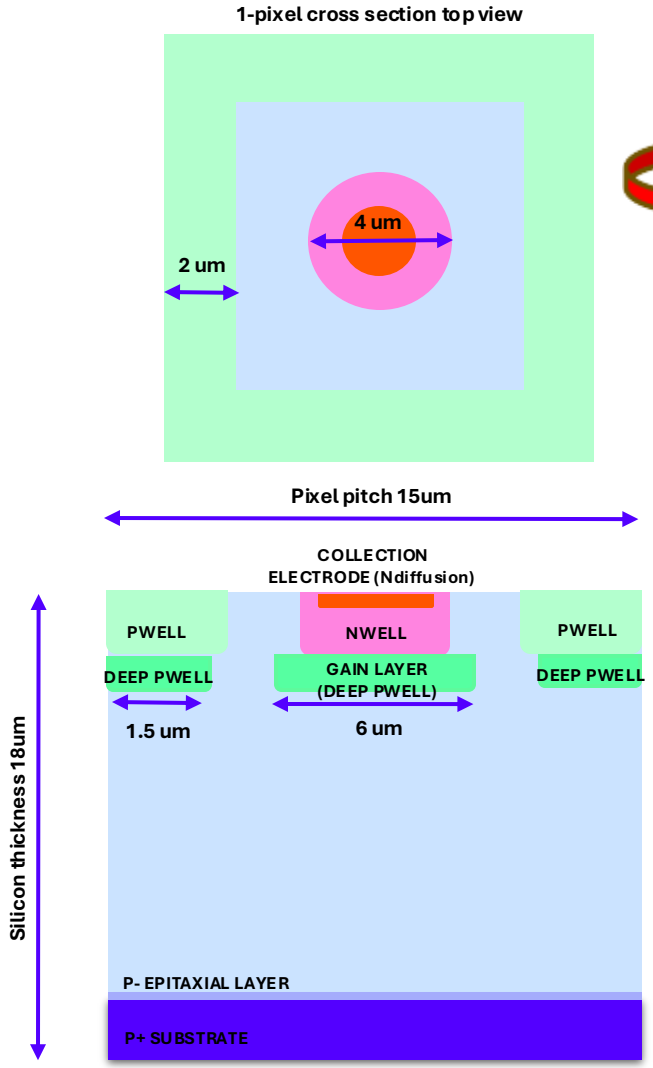




**Comparison between TCAD simulations and CERN laser measurement data**

# Planning Our Own Prototype (APICS)

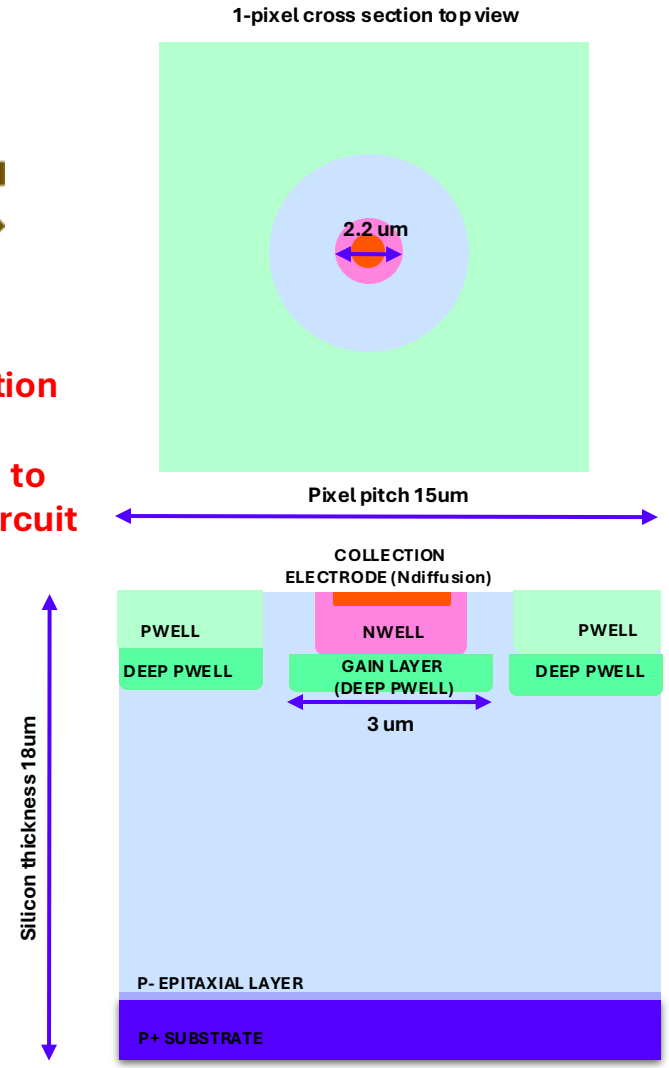
**-Pitch size 15 μm**
**-Thickness 18 um**

## Structure 1 (Nwell + deep Pwell)




- Larger collection electrode
- Less space for electronics inside

## Structure 2 (Smaller Nwell + deep Pwell)

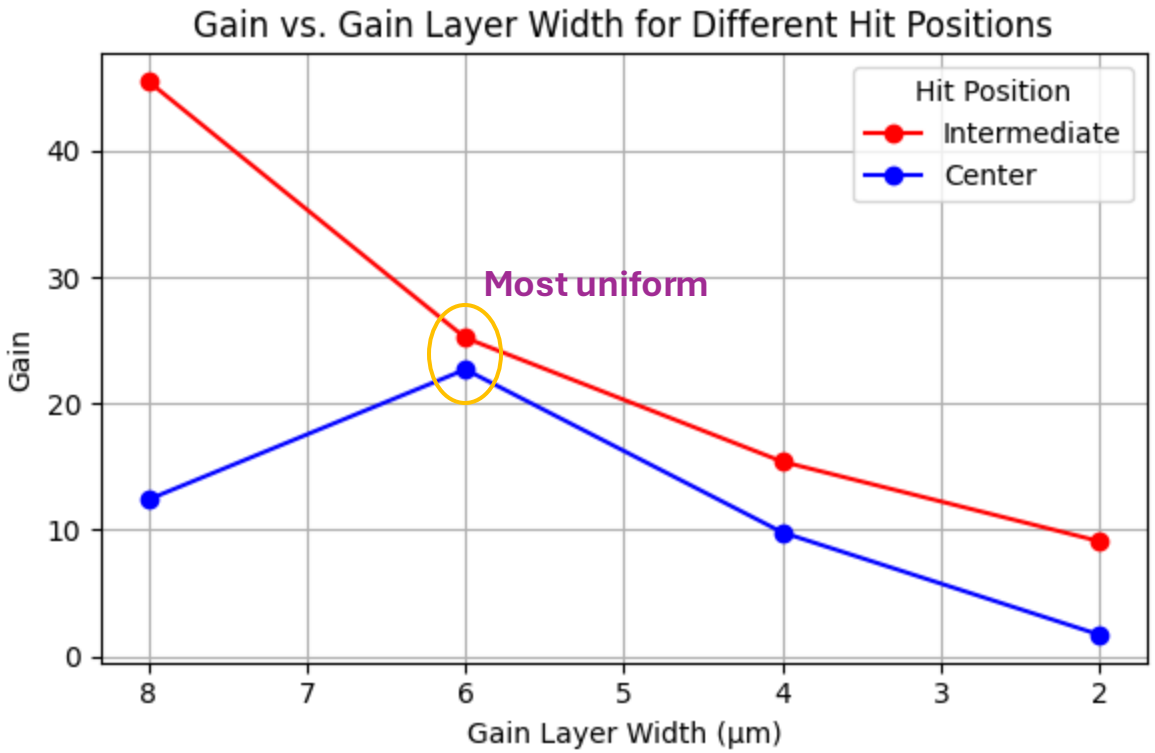



- Smaller collection electrode
- Lack of charge collection efficiency
- more space available to hold more complex circuit in future

# Design Considerations : Gain Layer Size

### Structure 1 (Nwell + deep Pwell)

- Best performance found at **6 µm** (gain & uniformity)
- Not permitted by foundry design rules → submitted version uses **4 µm**
- Current simulation results still correspond to **6 µm** case




### Structure 2 (Smaller Nwell + deep Pwell)

- **Deep Pwell gain layer (3um)** not allowed by design rules
- **Extra Deep Pwell** used instead (compatible)
- Contributed to measurements at CERN within the **CASSIA project** on structures using extra deep p-well → **more confidence** to simulate extra deep p-well configurations in Structure 2

# Definition of Gain, Charge Sharing, and Pixel Signal

**Gain Definition:**

$$G = \frac{Q_{\text{collected (with gain)}}}{Q_{\text{collected (no gain, single pixel)}}}$$

- $Q_{\text{collected (with gain)}}$ : Charge collected by a pixel with gain
- $Q_{\text{collected (no gain)}}$ :Charge that would be collected by the same pixel without gain
- $Q_{\text{generated}}$ : Total primary charge generated by the incident particle
- **C**: Capacitance of the pixel node

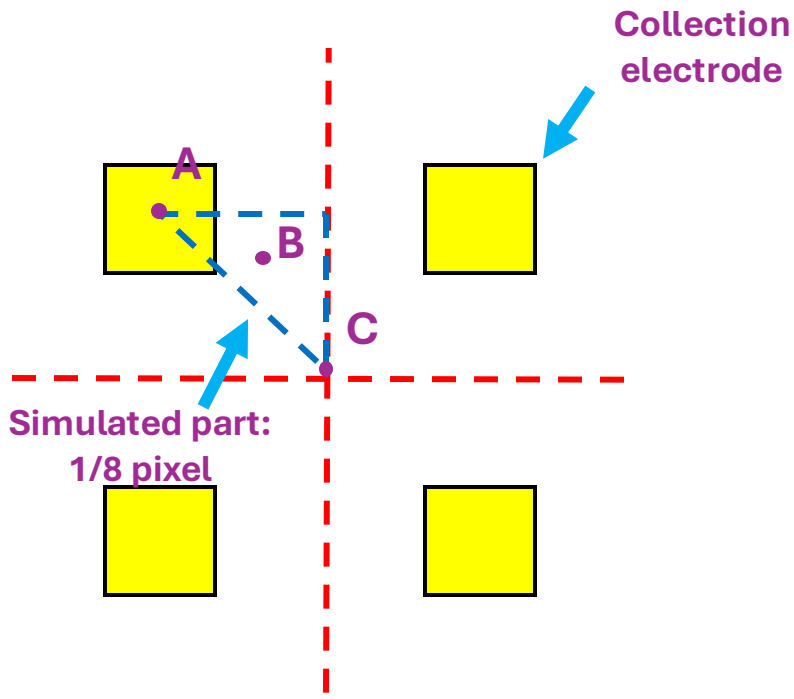
**Pixel Signal Voltage:**

$$V_{\text{signal}} = \frac{G \cdot CS \cdot Q_{\text{generated}}}{C}$$

**Charge Sharing:**

$$CS = \frac{Q_{\text{collected (no gain, single pixel)}}}{Q_{\text{generated}}}$$

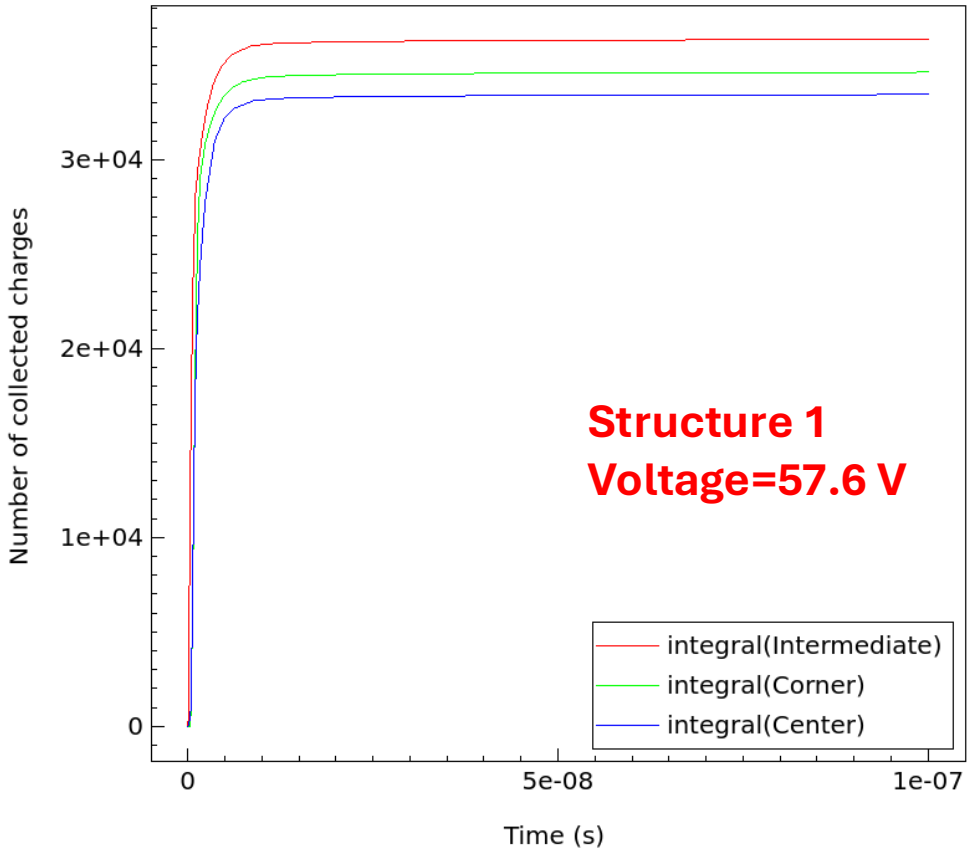
**At corner C:**
**CS = 1/4**



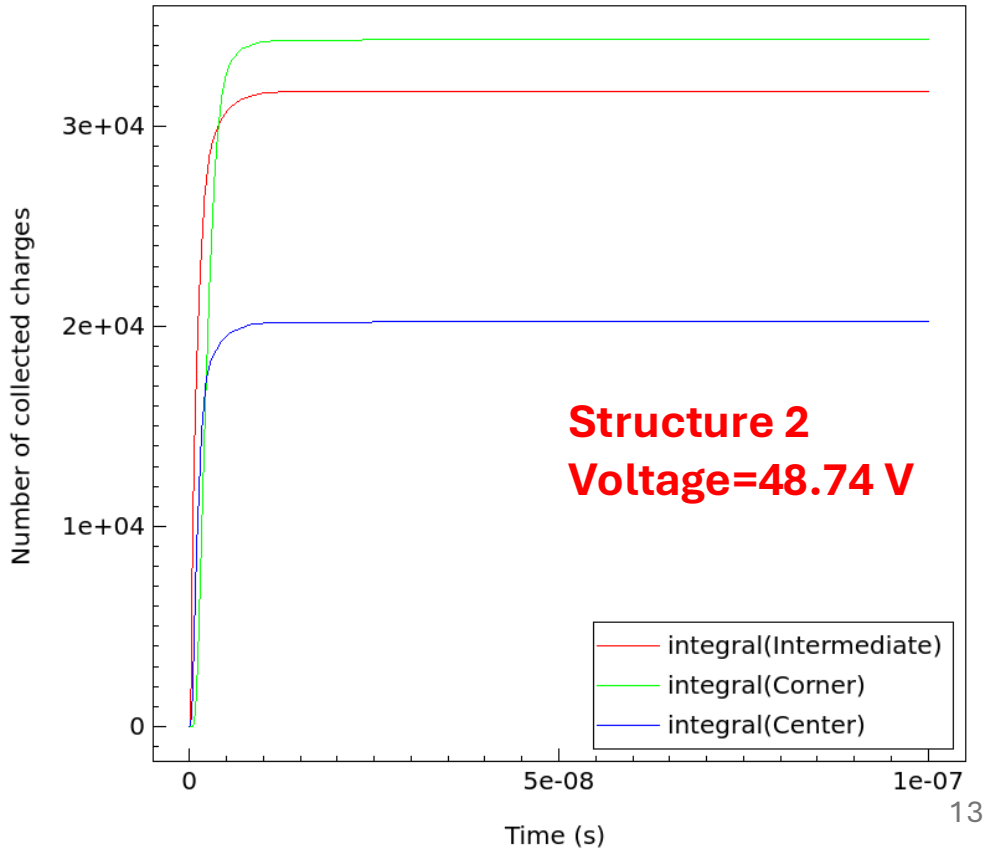

**A : Center**
**B : Intermediate**
**C: Corner**

# Gain Variation with Hit Position

- **Intermediate:** 36321e- ; gain~25
- **Corner:** 34587e- ; gain~23
- **Center**: 33406e- ; gain~22



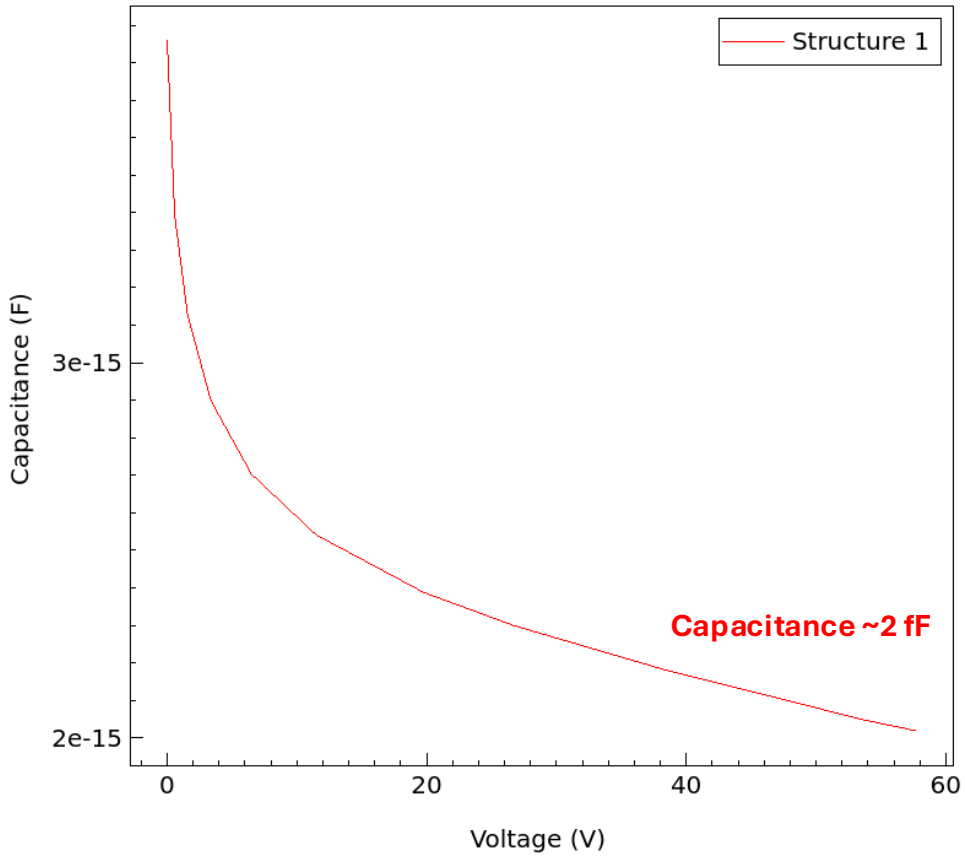

- **Intermediate:** 31736e- ; gain~22
- **Corner:** 34316e- ; gain~23
- **Center**: 20216e- ; gain~13



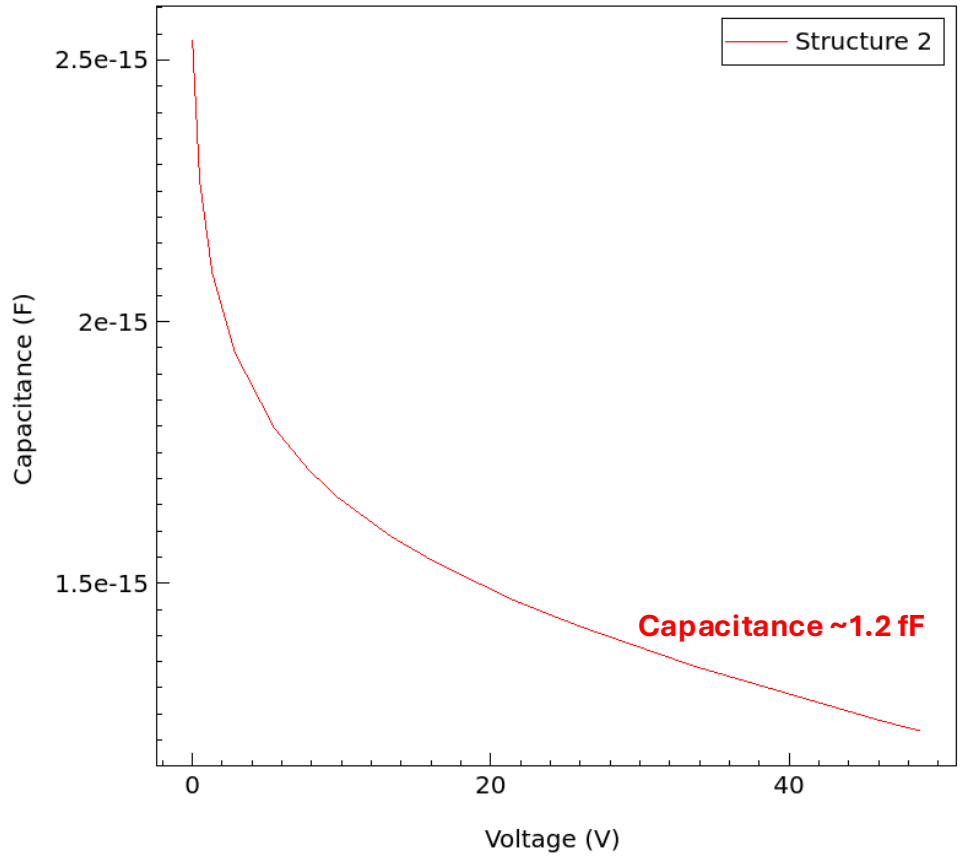
# C-V curve

$$V_{\text{signal}} = \frac{G \cdot CS \cdot Q_{\text{generated}}}{C}$$

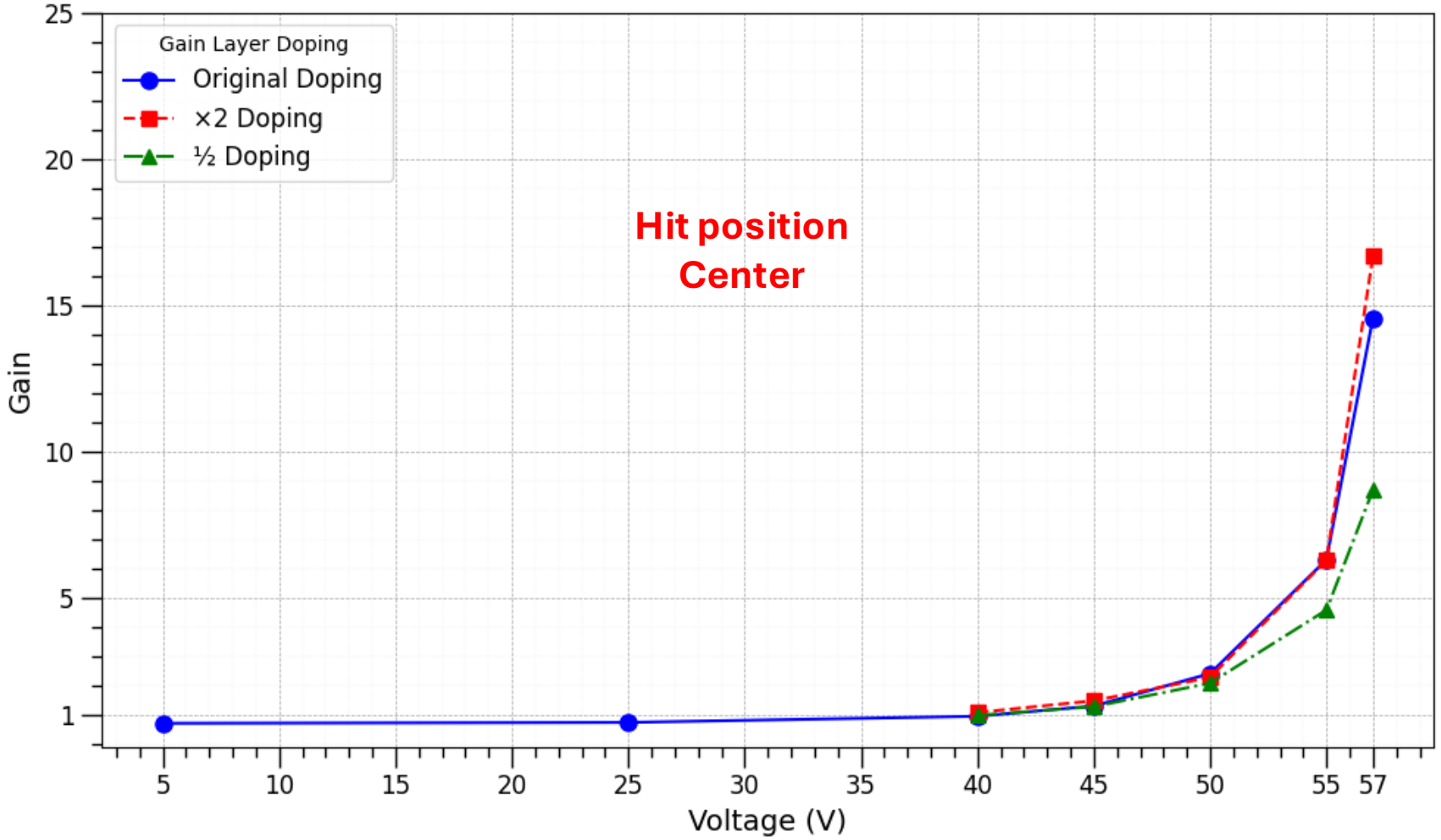
**Worst case (Corner) :**
**Vsignal(Pixel)~0.7V**




**Worst case (Corner) :**
**Vsignal(Pixel)~1.1V**



# Structure 1: Pixel-to-Pixel Gain Fluctuation with Varying Gain Layer Doping




- Simulation indicates a low gain mode voltage window of approximately 5V

# Conclusion & Future Work

- Standard CIS process can be used for LGAD fabrication
- TCAD simulations guided the design choices — optimal gain layer width and electrode configuration identified
- Simulation indicates a low gain mode voltage window of approximately 5V
- Simulated behavior shows good alignment with CASSIA measurements, validating simulations models
- Submission of test chip in Tower 180 nm technology for fabrication

**Next steps:**

- Simulations to study radiation tolerance
- Preparation of tests at Strasbourg
- Test the structures which are fabricated within APICS and CASSIA project

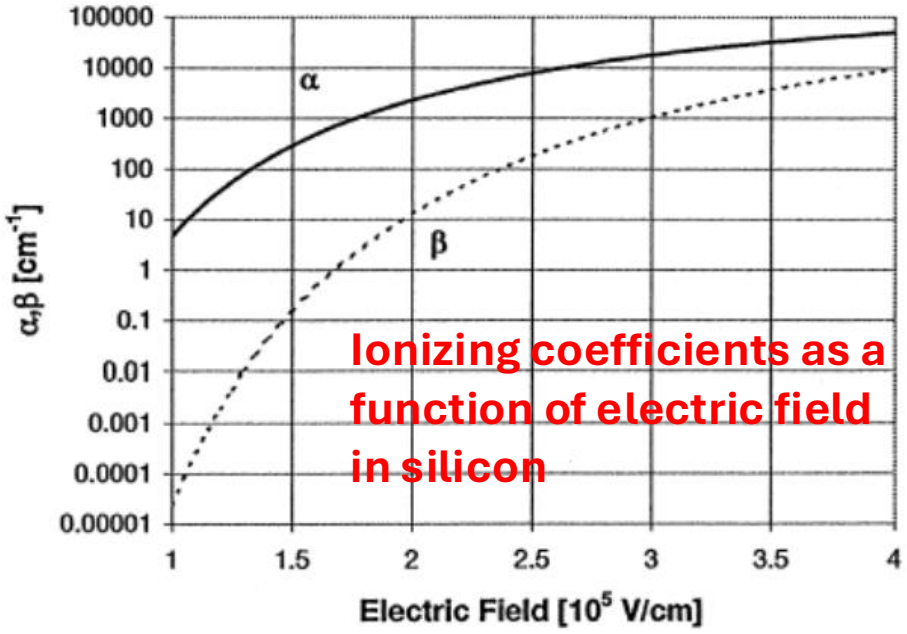
# Backup Slides

# APD Gain & Noise Expressions

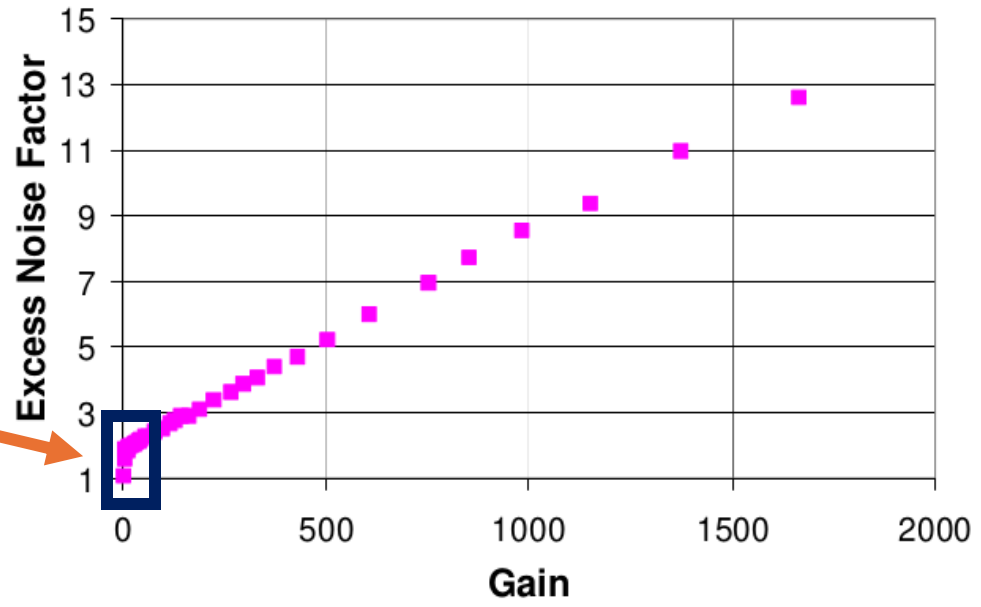
**Empirical Gain Formula:** $$M(V) = \frac{1}{1 - \left(\frac{V}{VB}\right)^n}$$

**$V_B$ : Breakdown voltage**
**n : Parameter depending on the APD structure**

***Excess Noise Factor:***
**F = k·M + (1 – k)(2 – 1/M)**
**k = β / α (k-factor)**
**β – ionization coefficient for holes**
**α – ionization coefficient for electrons**
**(see R.J. McIntyre, IEEE Tr. ED-13 (1972) 164)**

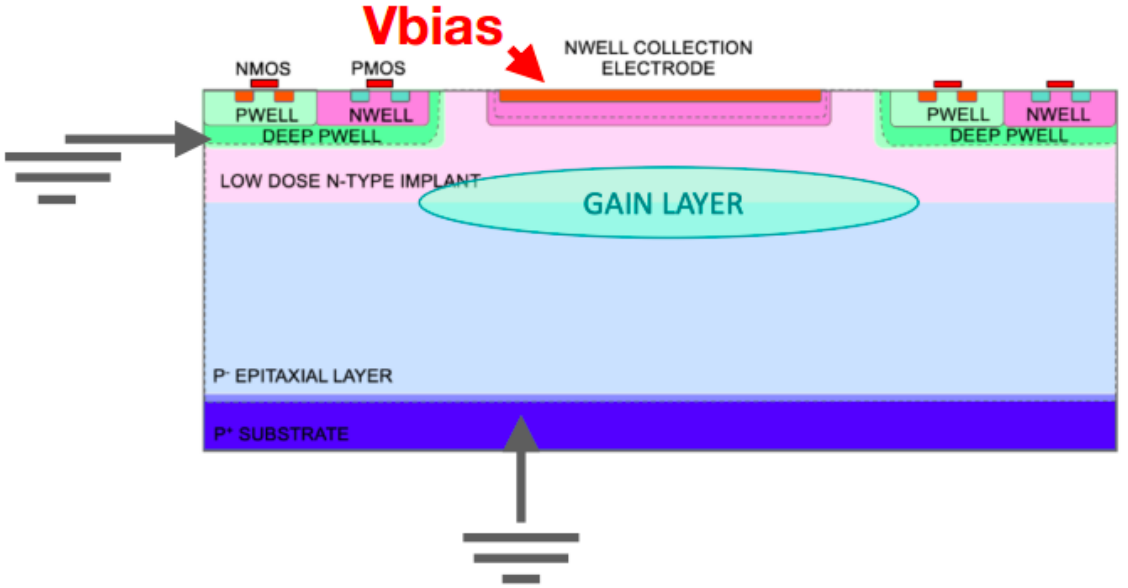



We target **low gain (~10–30)** to keep F(M) ≲ 2



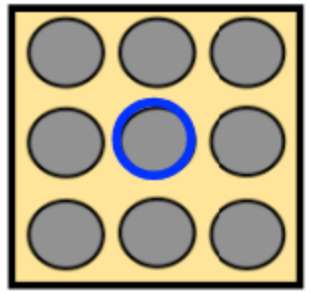
# Laser Setup

- Photons of ~ 1060 nm
- Central pixel biased
- P-well and sub set to 0V, only voltage applied through n-well to central pixel
- Cx amplifier (gain of 6.8 mV/fC), connected in series to central pixel only




3x3 matrix

Center pixel biased separately than rest of matrix

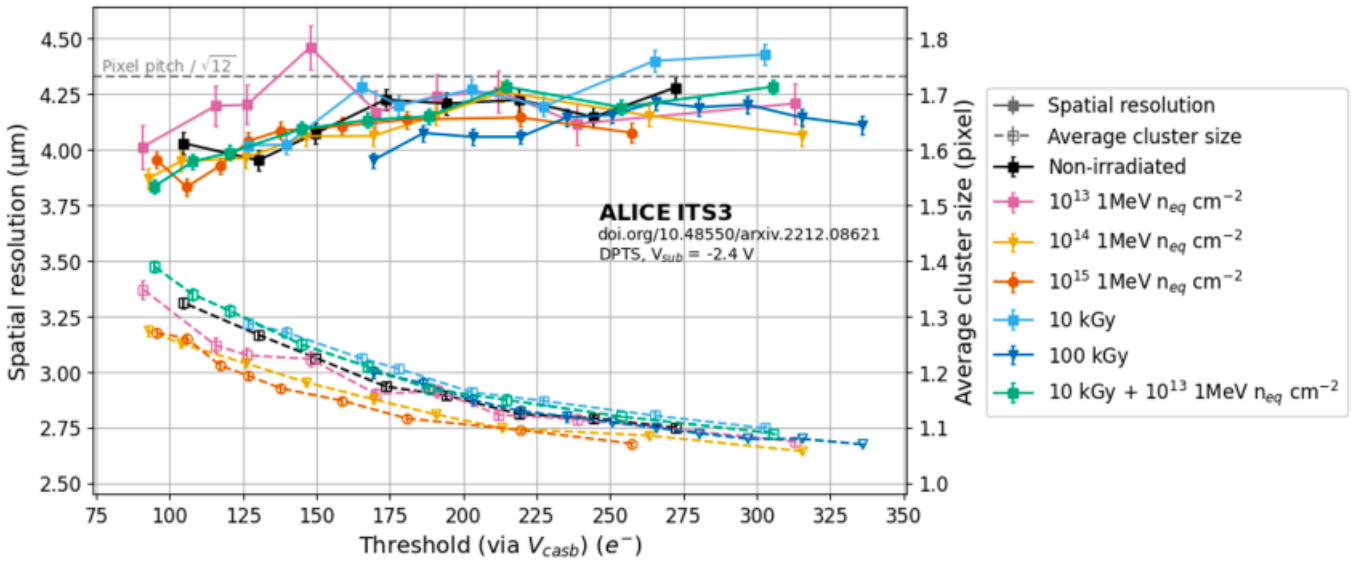


# 15 µm Pixels: A Path to 3 µm Resolution

**~3 um spatial resolution required by physics program (FCCee VTX requirments)**

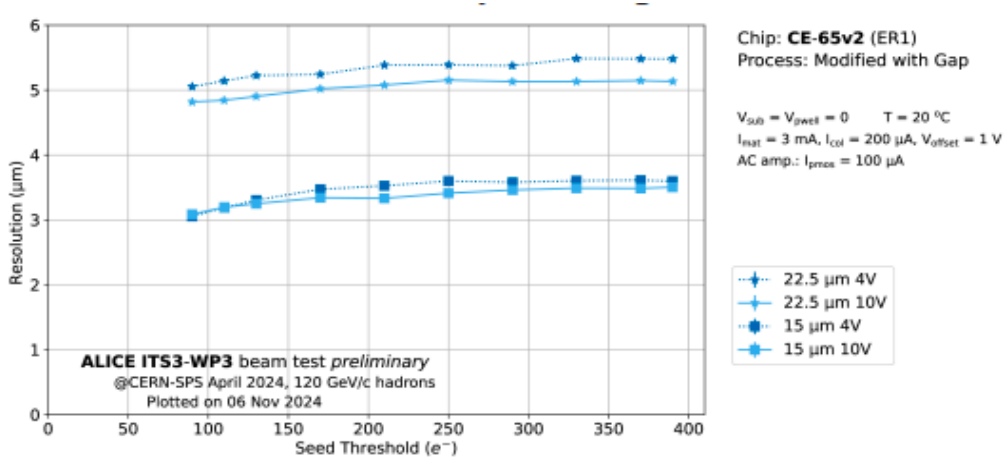
Represented by A.Besson at ECFA_Paris_2024 conference (https://indico.in2p3.fr/event/32629/overview)

DPTS (CERN)




Ref:arXiv:2309.14814

CE-65v2 (IPHC)




Ref:arXiv:2502.04070v5

# Structure 1: Exploring P-Gain Layer Parameters (Nwell + Extra deep P-well)

- **For Structure 1, instead of using a Deep P-Well (DPW) gain layer, we explore different gain layer with varying depth and doping concentrations.**

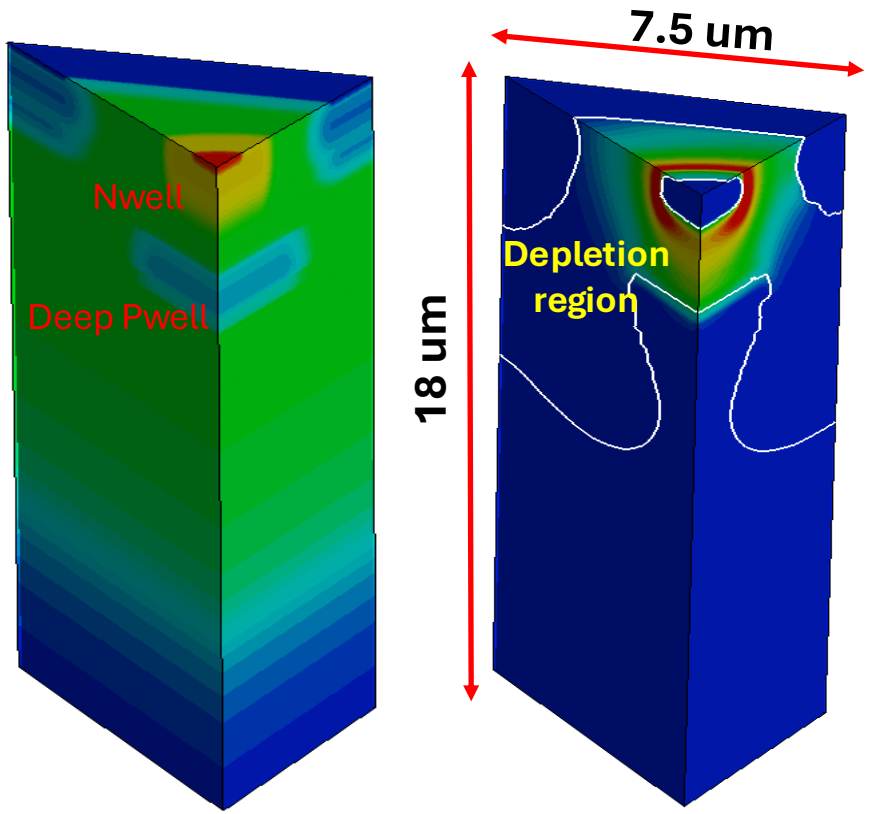
| Depth (um) \ Doping Conc. ($cm^{-3}$) | $1x10^{16}$ | $1x10^{17}$ | $1x10^{18}$ |
|---|---|---|---|
| 1.5 | **Gain : 8**<br>Voltage : 58.2 V<br>Leakage : 1.9e-12 A | **Gain : no gain**<br>Voltage :21.91 V<br>Leakage : 2.8e-12 A | **Gain : 2.7**<br>Voltage : 21.99 V<br>Leakage : 2.4e-11 A |
| 2 | **Gain : 10**<br>Voltage : 59.29 V<br>Leakage : 2.6e-12 A | **Gain : no gain**<br>Voltage : 31.8 V<br>Leakage : 2.6e-14 A | **Gain : no gain**<br>Voltage : 26.58 V<br>Leakage : 2.4e-11 A |
| 2.5 | **Gain : 10**<br>Voltage : 59.88 V<br>Leakage : 2.3e-12 A | **Gain : (Geiger mode)**<br>Voltage : 44.18 V<br>Leakage : 6e-14 A | **Gain : (Geiger mode)**<br>Voltage : 39.75 V<br>Leakage : 1e-14 A |
| 3 | **Gain : 5**<br>Voltage : 60 V<br>Leakage : 5e-13 A | **Gain : 21**<br>Voltage : 53.89 V<br>Leakage : 3e-12 A | **Gain : 20**<br>Voltage : 52.57 V<br>Leakage : 4.3e-12 A |
| 3.5 | **Gain : 3.5**<br>Voltage : 60 V<br>Leakage : 3e-12 A | **Gain : 23**<br>Voltage : 57.28 V<br>Leakage : 3.8e-12 A | **Gain : 26**<br>Voltage : 56.93 V<br>Leakage : 2.7e-12 A |

**Same study could be done for structure 2 replacing the deep Pwell gain layer by another P-gain layer (small Nwell + Extra deep P-well)**

# Simulating APICS-LGAD Structures: 15 µm Pixel Pitch, 18 µm Silicon Thickness (Round electrode)

## Structure 1

High electric field at the periphery




## Structure 2