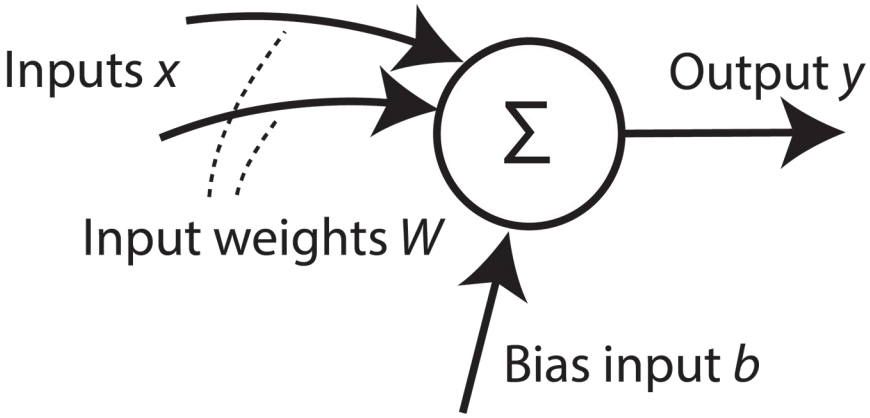
Prospectives de R&T pour futurs collisionneurs (mais peut-être pas que):

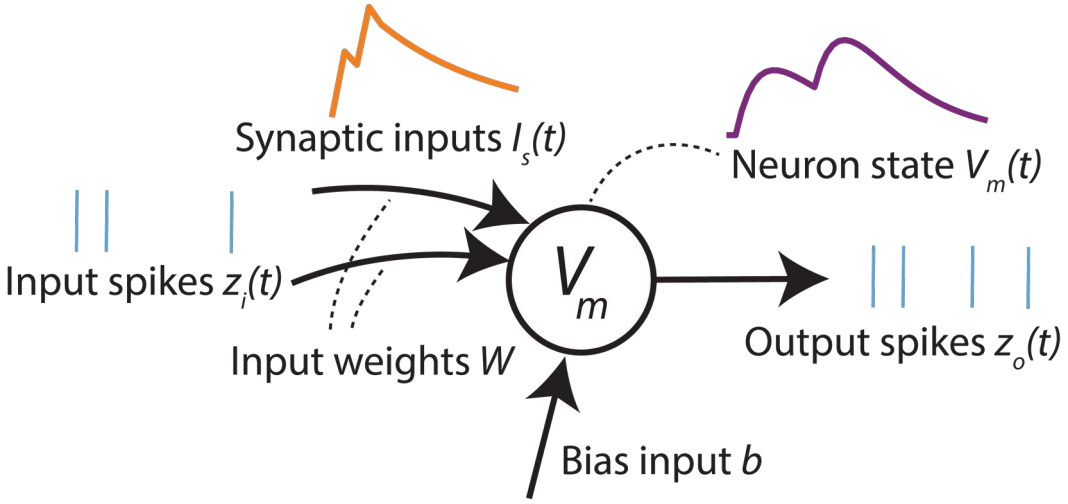
Détecteurs intelligents & Spiking Neural Networks

Spiking Neural Networks en 1 dessin



Dans un neurone “standard”, il n’y a pas d’état interne. Le résultat ne dépend que des entrées à l’instant t

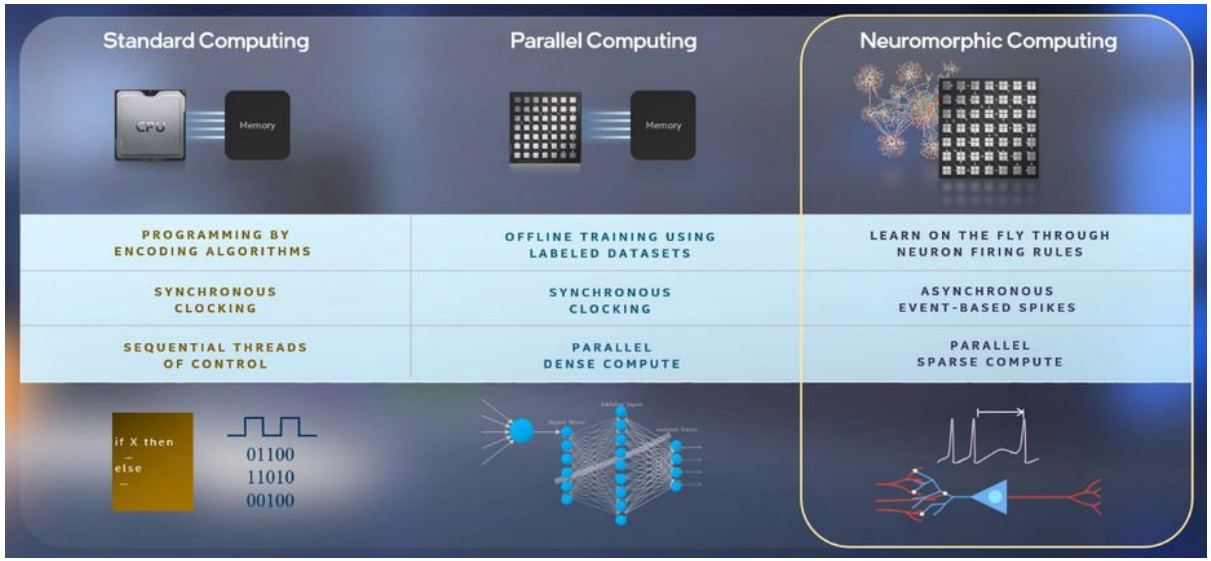
Dans un “spiking” neurone, les entrées sont intégrées, et l’état interne du neurone est dynamique. Le signal ne passe en sortie que lorsqu’il **franchit un seuil critique**



Processeurs neuromorphiques

Une puce neuromorphique présente la même structure physique qu'un réseau de neurones. Elle est composée de multiples unités de calcul correspondantes chacune à un neurone artificiel. Chaque unité a juste assez d'énergie pour effectuer la fonction mathématique d'un seul neurone.

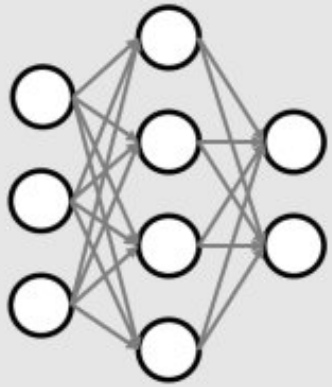
Une autre caractéristique essentielle de ces puces est la connexion physique entre ces neurones artificiels. Ces connexions rapprochent les puces neuromorphiques de véritables cerveaux, reposant sur les synapses reliant les neurones. Les modèles IA peuvent être exécutés à une vitesse plus importante que sur les CPU et GPU équivalents, tout en consommant moins d'énergie.



What is neuromorphic computing

Neuromorphic algorithms are embedded on low-power electronics to produce actionable decisions in real time

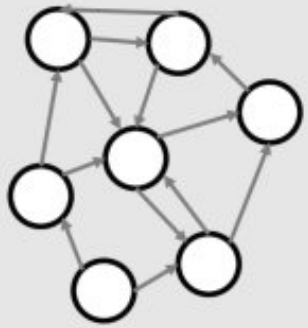
Traditional Neural Hardware



Accelerates traditional neural network and deep learning computation

- Current hardware is well-suited to existing algorithms
- Fast computation ***or*** low power
- Currently deployed in cloud or mobile devices

Neuromorphic Computing



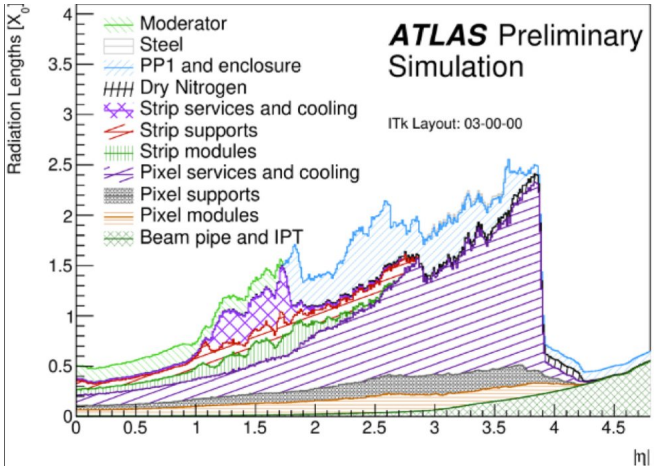
Implements spiking recurrent neural network computation and can be suitable for neuroscience simulation

- Significant promise for future algorithmic development
- Massively parallel & event-driven
- Co-located processing & memory
- Fast computation ***and*** low power
- Still in development

OAK RIDGE National Laboratory

Cas 1 : Détecteurs pixels pour FCC-ee

Détecteur ATLAS ITk pour le HL- LHC:
Contribution principale des câbles (alimentation, lecture) et des supports mécaniques (cooling et échelles)



Objectif FCC-ee :
0.3% X_0 par couche

- Développements mécanique "lightweight"
- Réduction du flux de données et de la consommation énergétique: moins de câbles
- Réduction de la structure mécanique due au refroidissement: en dessous de 50 mW/cm^2 le refroidissement par flux d'air devient possible

https://arxiv.org/pdf/2502.04071

Table 1. Global requirements of FCC-ee vertex detectors.

Physics challenges	Requirement
Coverage up to $\lvert\cos(\theta)\rvert = 0.99$	Long barrel, forward disks
High reconstruction efficiency	Hermeticity, small peripheries, > 99% hit eff., many layers
Asymptotic resolution of $a \approx 3\,\mu$m	3 µm single-hit resolution, first layer close to interaction point
Multiple scattering: $b \approx 15\,\mu\text{m GeV}$	Light beam pipe $\lesssim 0.3\,\%\ X_0$/layer $\rightarrow$ thin sensors, light support Air-cooling $\rightarrow$ Power consumption $\lesssim 50\,\text{mW cm}^{-2}$

Table 2. Requirements of FCC-ee vertex detectors at the Z pole.

Collision environment challenges	Requirement
High luminosity	Readout between 50 MHz (no trigger) and $\gtrsim$ 100 kHz (trigger)
Avoid pile-up of Z bosons	Integration time $\lesssim 1\,\mu$s
Beam backgrounds	Hit rate capability up to $\mathcal{O}(200\,\text{MHz cm}^{-2})$
Radiation environment	Few 10^{13} 1 MeV $n_{\text{eq}}\text{cm}^{-2}$ and $\mathcal{O}(100\,\text{kGy})$ per year

Cas 2: Calorimètres à haute granularité

Détecteur ATLAS Lar pour le HL- LHC: reconstrucrtion des OFCs par CNN dans des FPGAs. Meilleure reconstruction pour les pulses superposés.

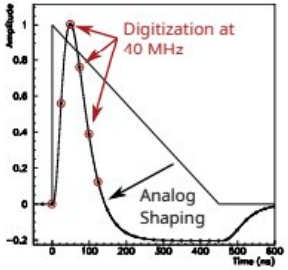
Futurs collisionneurs: utilisation d'ASICs, pour des cartes plus compactes et moins coûteuses en énergie ? Réduction des câbles ?

Digital energy reconstruction

- Digital energy reconstruction with Optimal Filter (OF)

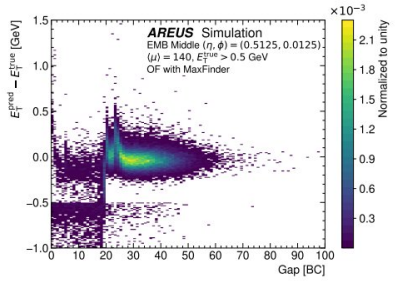
$$E_t = \sum_{i=1}^{5} c_i \cdot x_{t-i}$$

- Overlapping signals require better algorithm
- 556 high-performance FPGAs will be installed for real-time digital signal processing

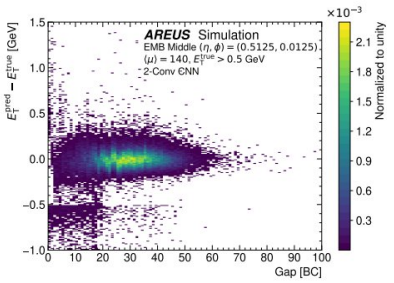


http://cds.cern.ch/record/1701107 [3]

Energy reconstruction performance as a function of gap between 2 pulses

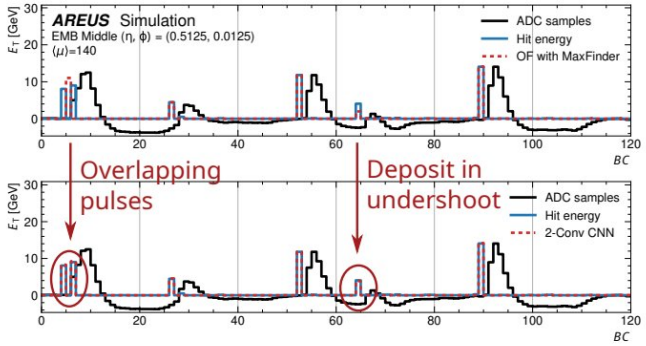


Optimal Filter



2-Conv CNN

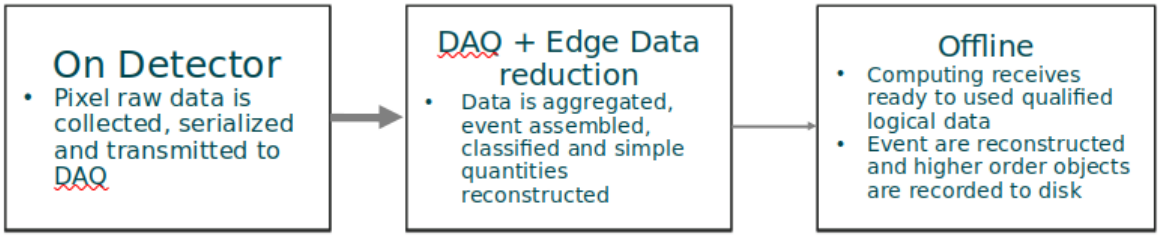
→ Improvements in reconstruction of overlapping pulses (gap < 20 BC)



https://cds.cern.ch/record/2863776

Changer de paradigme ?

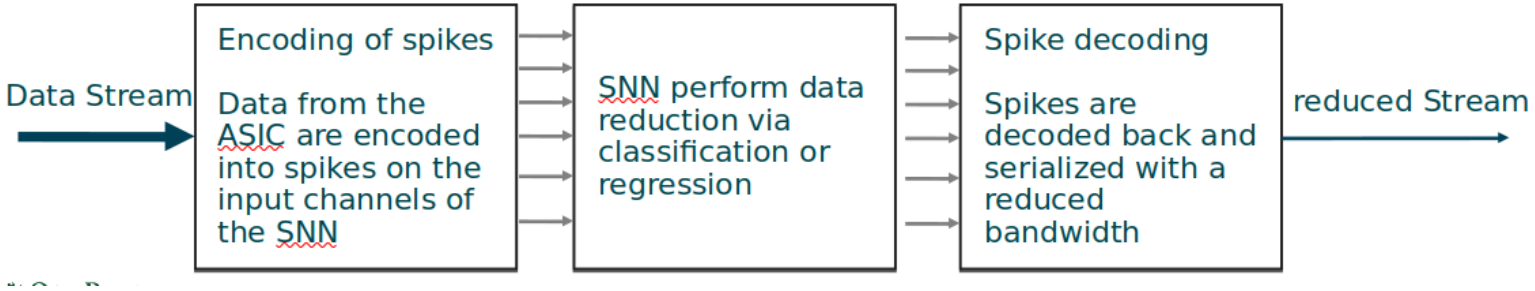
Classifying, encoding/decoding and compressing pixel data , at the edge



Change of paradigm ! Yes, we must throw away data, we already do !

With sufficiently smart and efficient algorithms , we can process data as it stream and reduce the data stream efficiently close to data acquisition

- Data is aggregated and transmitted to DAQ and stored in High-Speed Memory, accessible by a high-speed bus (For example PCI express and DDR4 memory)
- Commodity FPGA/Custom cards consume the data stream and reduce the data
- High performance network consumes the reduced data and transmit to offline



https://indico.cern.ch/event/1439336/contributions/6242186/

Exemple: On-Sensor Data Filtering

On-Sensor Data Filtering using Neuromorphic Computing for High Energy Physics Experiments

https://arxiv.org/pdf/2307.11242v1

ABSTRACT In this paper, we investigate the prospects of applying neuromorphic computing spiking neural network models to filter data on the readout electronics of the sensor in the high energy physics experiments at the High Luminosity Large Hadron Collider. We present our approach on developing a compact neuromorphic model that filters out the sensor data based on the particle's transverse momentum with the goal of reducing the amount of data being sent to the downstream electronics.

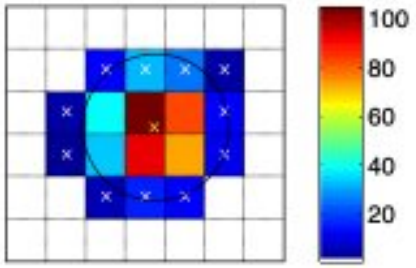


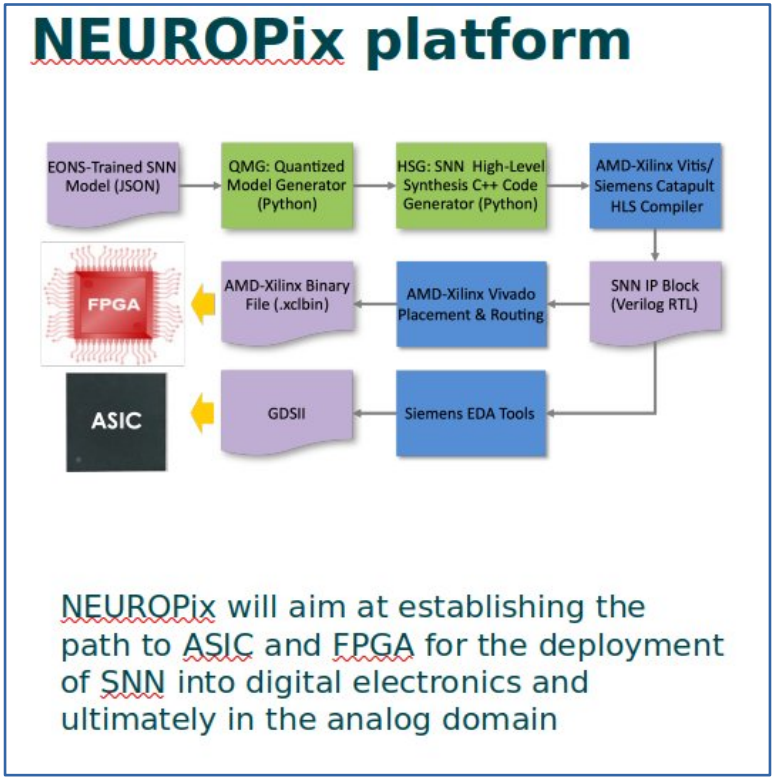
Table 2: Performance of SNN and DNN models

Models	DNN (full precision)	DNN (quantized (5-bit weights+ 10-bit activations)	SNN (this work)
Signal Efficiency	94.8%	91.7%	91.89%
Data Reduction	24.02%	25.72%	25.47%
Neurons	128	128	84
Parameters	2049	2561	930

Neuropix : présenté dans le DRD3 le 02/12/2024

DRD3 Week : https://indico.cern.ch/event/1439336/contributions/

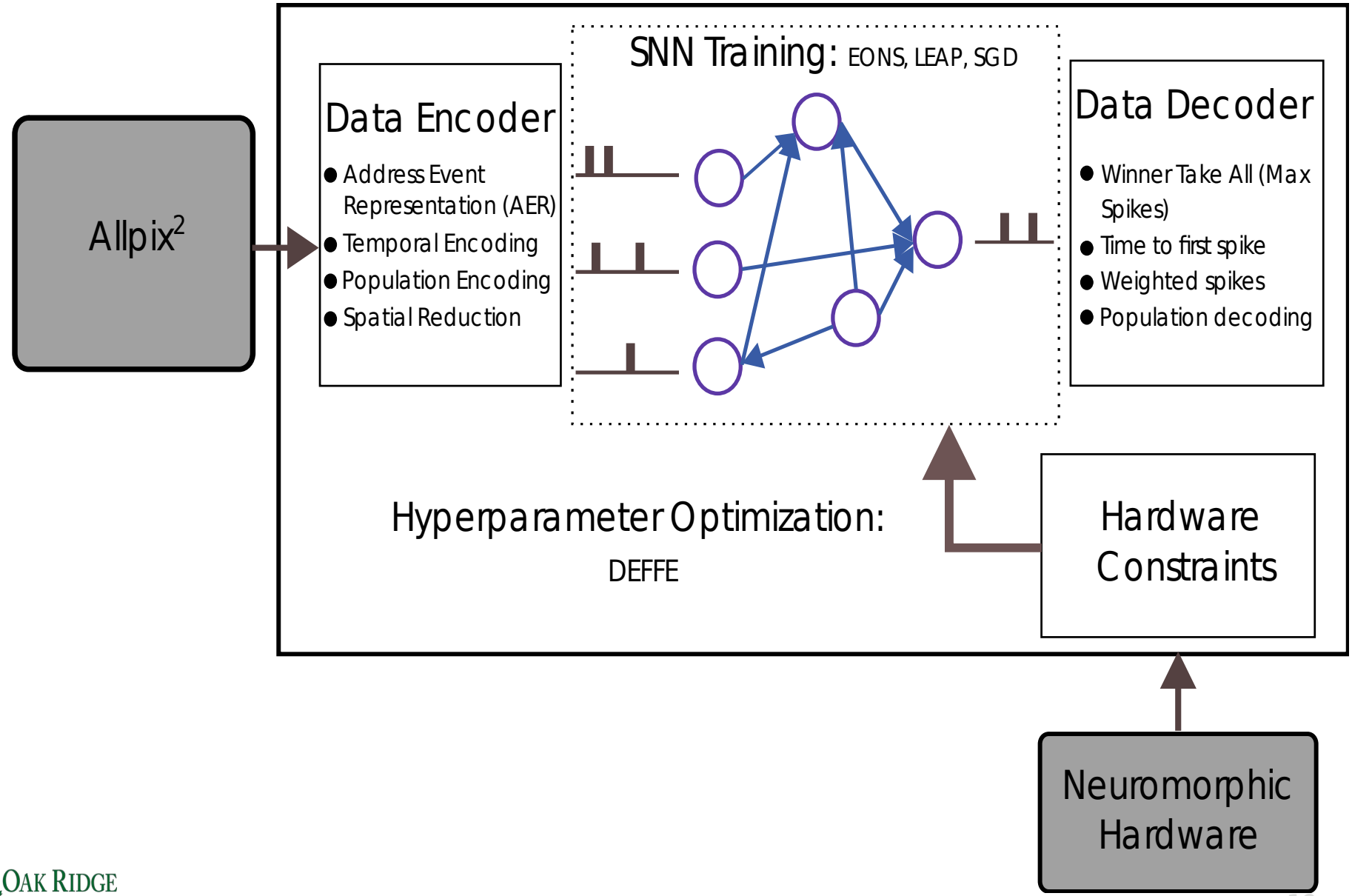
NEUROPIX: A neuromorphic computing framework for pixelated detector data processing



- SNN-based neuromorphic computing is novel emerging AI/ML technique that promise low-power compact implementation of computing that can be deployed in FPGA, ASIC, and can even operate in the analog domain
- University of Tennessee and ORNL have developed software and hardware for deployment of SNN algorithms to ASIC and FPGA
- **We are looking for good applications, collaborators to produce simulation, train networks and do testing in the lab**

https://indico.cern.ch/event/1439336/contributions/6242186/

NEUROPix platform



Discussion ?